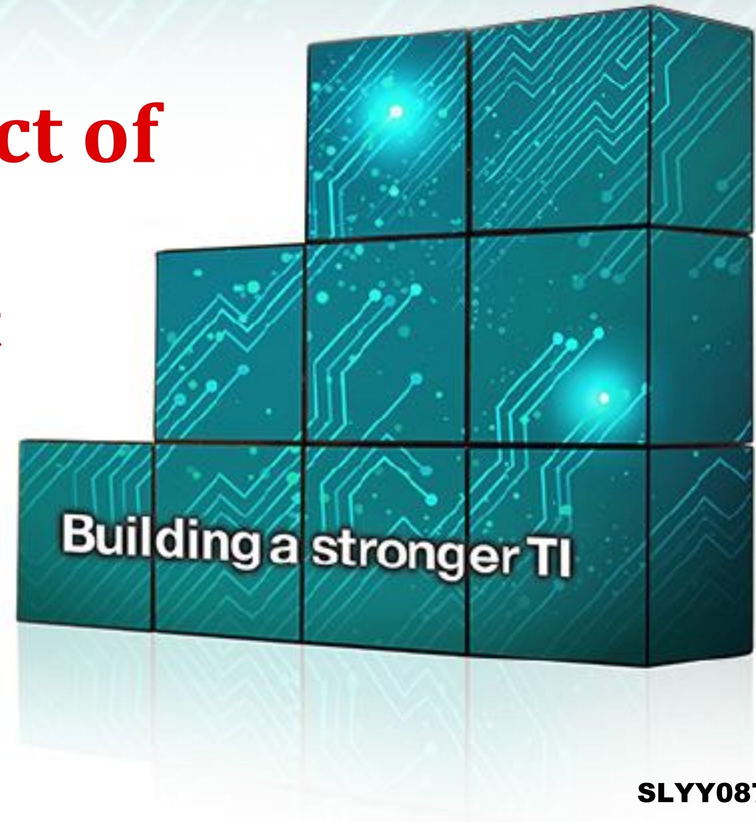
System-Level Crosstalk-Induced Efficiency Impact of DCDC Converter:

Simulation to Measurement Correlation



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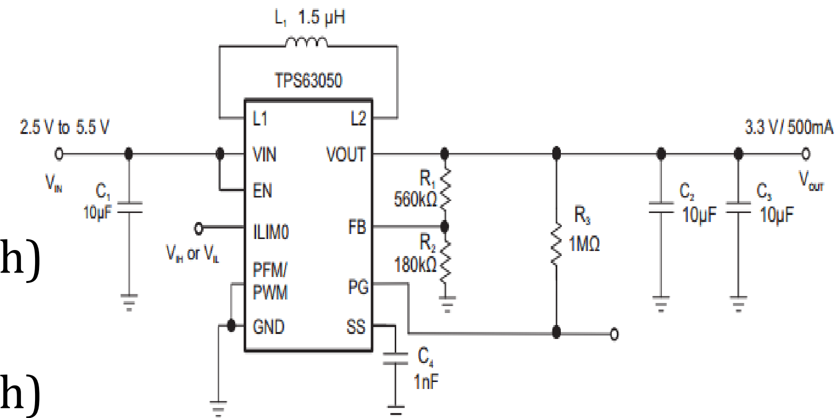
Synopsis

- Higher switching frequency, R_{DSON} , and gate charge (Q_g) are among some of the factors that contribute to efficiency impact.
- Additionally the system (i.e. package and PCB) electrical parasitics also contributes to efficiency performance degradation.
- In this work we show that 2nd order electromagnetic (EM) effects (viz. **mutual capacitive** and **inductive** parasitic coupling via crosstalk), beyond just self RLC, are becoming critical and can impact efficiency.
- Using co-design electrical modeling and simulation methodology, we demonstrate how crosstalk in the system impacted efficiency of the TPS63050™, a TI's buck-boost converter.
- Good correlation between simulation and lab measurements was achieved.
- It is critical to assess performance impact of the system. It is recommended to integrate system-level co-verification modeling early in the design development phase.

Background

- TPS63050^{TM} is a high efficiency, low quiescent-current buck-boost converter for consumer and industrial applications (0.5A, 2.5MHz).
- Support automatic PWM/PFM mode transition with fixed and adjustable output voltage versions.
- Packaged in:
  - WCSP (wafer-level chip scale)
    - Size: 1.6 x 1.2mm, 12-pin, 0.4mm pitch)
  - HotRod^{TM} QFN (quad-flat no leads)
    - Size: 2.5 x 2.5mm, 12-pin, 0.5mm pitch)



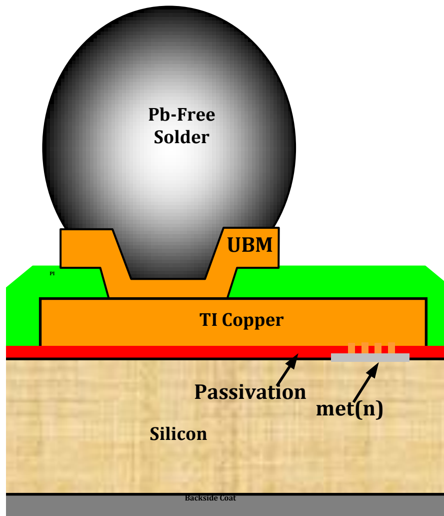
Simplified schematic (HotRod^{TM} QFN – [1])

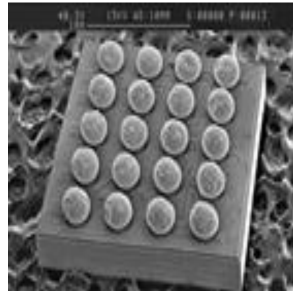
- Characterization of device packaged in HotRod^{TM} yielded in approximately **identical DC** parameters (e.g. overall R_{DSON}) vs.WCSP version.
- All **AC parameters are comparable** with the exception of **efficiency** - which was found to be considerably **lower** in the HotRod^{TM} packaged device!

Packaging Technologies

Wafer-level Chip Scale (WCS) Package [2]

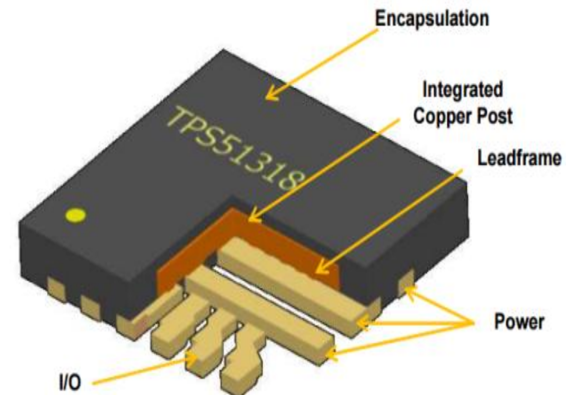
- Designed for minimum size and footprint.
- Die-pkg ratio is 1:1.
- Wirebonds are eliminated/replaced by thick copper redistribution and solder bumps.
- Good current capabilities but limited in comparison to HotRod.





HotRod™ QFN Package [3]

- Leadless packages specifically designed for power applications.
- Eliminates power device wire bonds by attaching the power device and/or die directly to the leadframe.
- Small foot-print, standard QFN pitch, low parasitics, and high-current capabilities.
- Connections to PCB via solder lands.

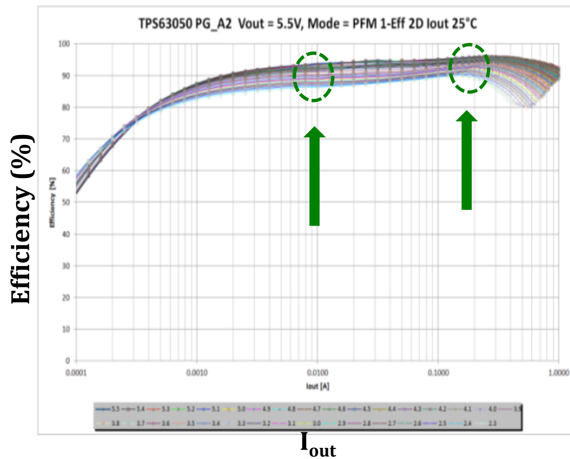


Efficiency (η) Measurement

WCSP | **HotRod**

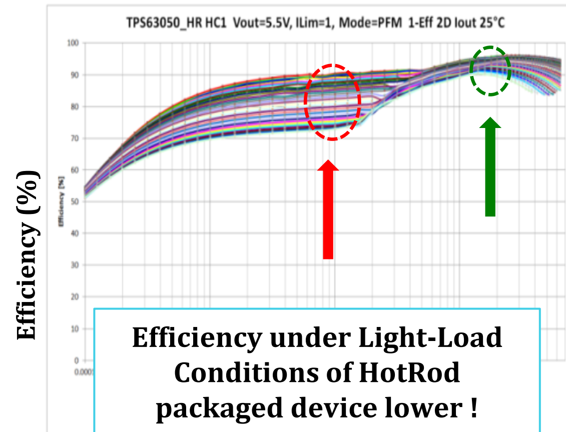
VOUT 5.5V

Efficiency (%)



I_{out}

Efficiency (%)

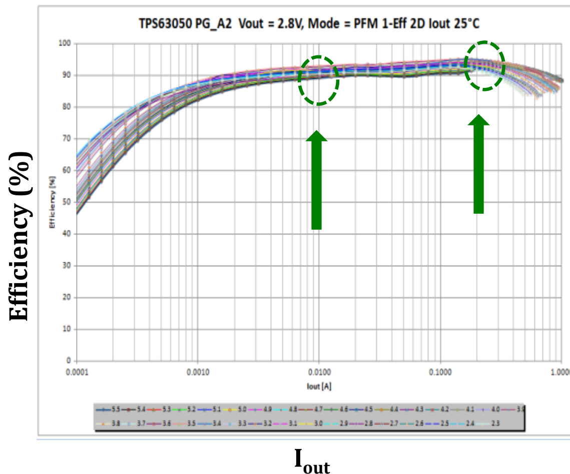


Efficiency under Light-Load Conditions of HotRod packaged device lower !

Reduced Efficiency under light load conditions - (PFM)

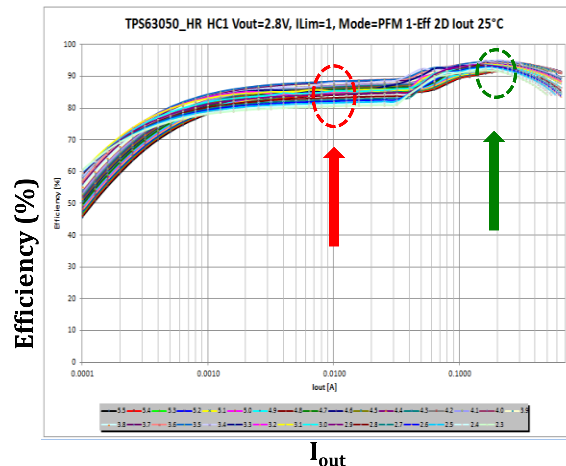
VOUT 2.8VV

Efficiency (%)



I_{out}

Efficiency (%)



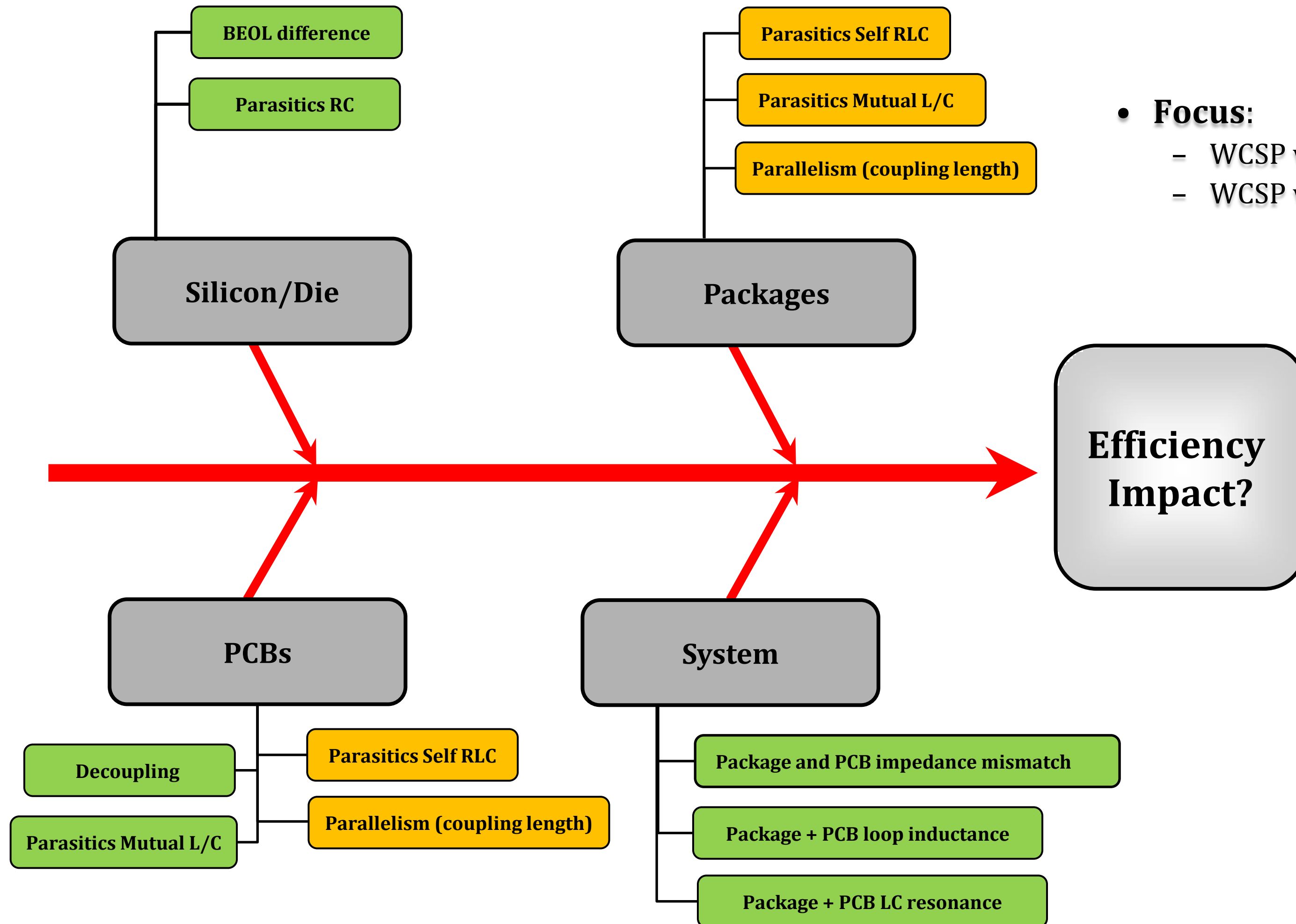
I_{out}

Identical Efficiency under high load conditions - (PWM)

Additional Background Data

- Some observations:
  - Under light load conditions only and when in PFM mode.
  - For adjustable VOUT version only which utilize external feedback resistor divider network. Fix voltage version does not show degradation which utilize internal feedback divider network.
  - Effect is temperature and VIN independent.
  - Fix voltage version and adjustable devices have identical silicon.
  - Baselayer are identical
  - Different package technologies (WCSP vs. HR)
  - Metal system differences:
    - Top metal layers changed for HotRod package options
    - While doing so, implemented some improvements for routing and shielding of critical signals such as FB (feedback)
  - Minor routing differences in EVM/Board layout due to different package break-out /fan-out

Debug/Investigative Fishbone



- **Focus**:
  - WCSP vs HotRod QFN packages
  - WCSP vs HotRod QFN PCBs

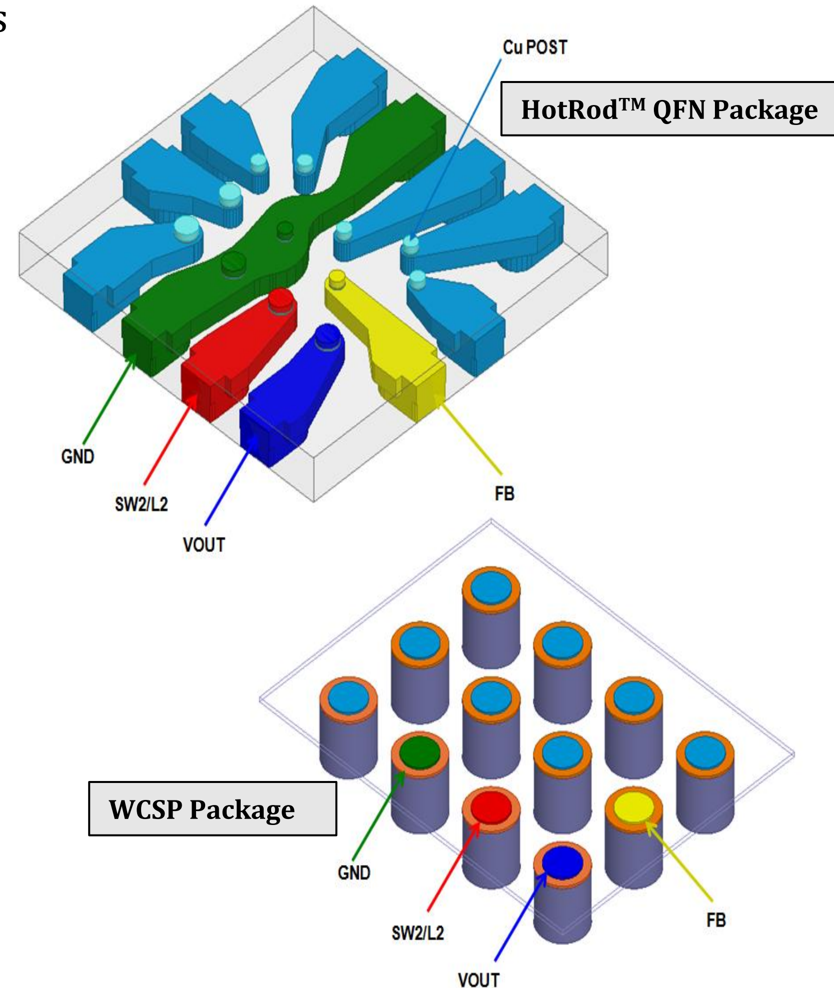
Package Parasitics Comparison

- Performed with 3D Quasi-Static electromagnetic s
- Employ volumetric meshing to capture 3D effect.
- Extracted self (RLC) and mutual (C_M and L_M).

— **Comparative results:**

WCSP (@ 2.5MHz)					
	R (mOhm)	**L (nH)**	**C (fF)**	**Lm (nH)**	**Cm (fF)**
FB	0.72177	0.043981	22.029		
SW2/L2	0.72049	0.043946	22.04	**0.0084**	**1.2027**
VOUT	0.72088	0.043924	20.278	0.011792	4.8096
HotRod (@ 2.5MHz)					
	R (mOhm)	**L (nH)**	**C (fF)**	**Lm (nH)**	**Cm (fF)**
FB	1.4394	0.22713	111.84		
SW2/L2	0.75544	0.13111	117.38	**0.0103**	**9.536**
Vout	0.80964	0.14179	94.664	0.016245	32.337

- $C_{MHR} > C_{MWCSP}$ (approximately 8X)
- $L_{MHR} > L_{MWCSP}$ (approximately 1.2X)

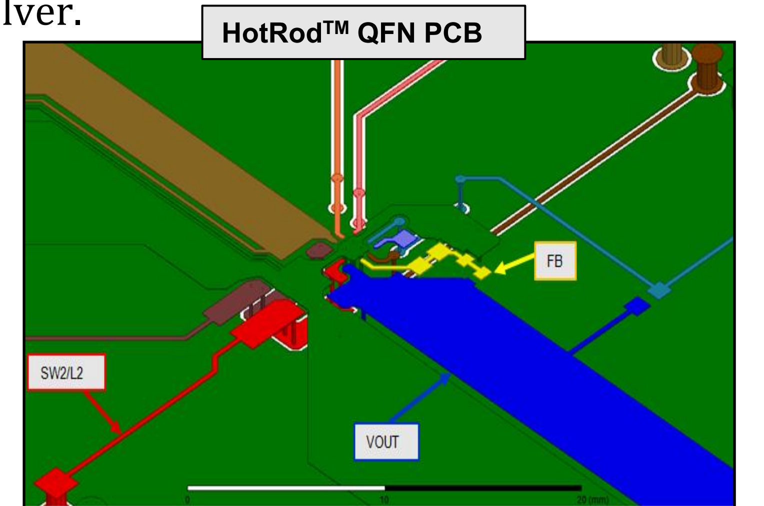


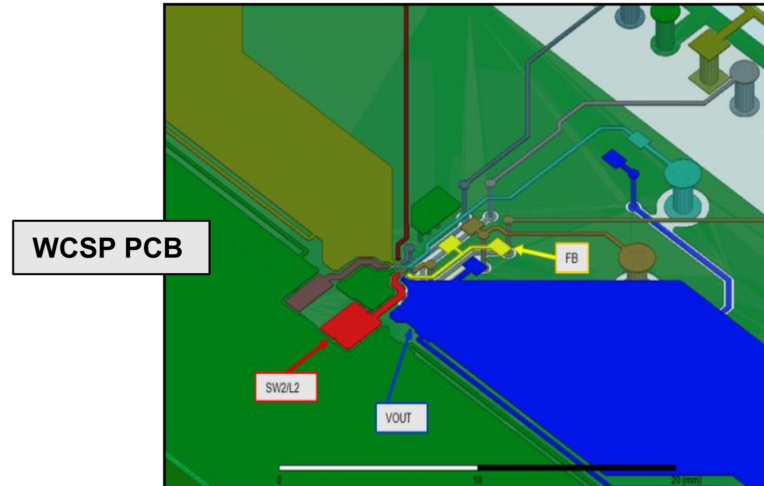
PCB Parasitics Comparison

- Performed with 3D Quasi-Static electromagnetic solver.
- Employ volumetric meshing to capture 3D effect.
- Extracted self (RLC) and mutual (C_M and L_M).

— **Comparative results:**

WCSP (@ 2.5MHz)					
	R (mOhm)	L (nH)	C (pF)	Lm (nH)	Cm (pF)
FB	15.551	3.258	0.641		
SW2/L2	8.409	1.866	1.056	0.0678	0.012
VOUT	7.394	8.663	13.348	0.4840	0.201
HotRod (@ 2.5MHz)					
	R (mOhm)	L (nH)	C (pF)	Lm (nH)	Cm (pF)
FB	6.561	1.268	0.753		
SW2/L2	6.164	2.637	2.823	0.0157	0.0031
Vout	10.525	8.352	8.840	0.1490	0.174

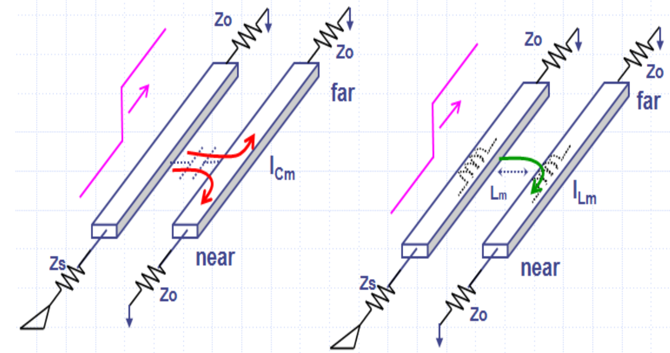




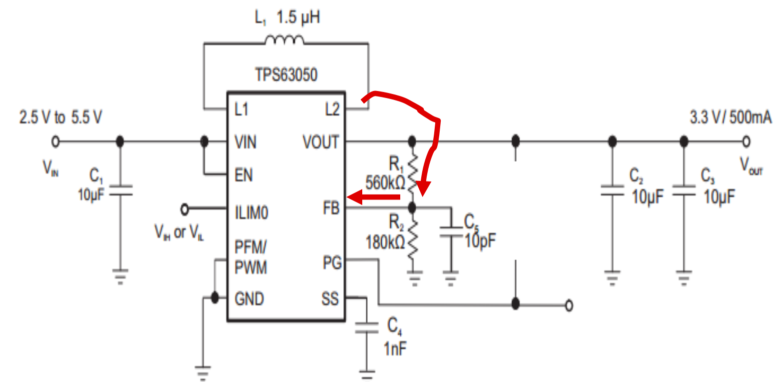
- HotRod™ LC_{SELF} > WCSP LC_{SELF}
- HotRod™ $L_M C_M$ < WCSP $L_M C_M$

Crosstalk Coupling Mechanisms

- Crosstalk (XTLK) is the electromagnetic coupling of energy from one line to another via:
  - Mutual inductance (magnetic field) → $V_{Lm} = L_m \frac{dI}{dt}$
  - Mutual capacitance (electric field) → $I_{Cm} = C_m \frac{dV}{dt}$
- Crosstalk generally depends on:
  - Edge rate (slew rate)
  - Voltage amplitude
  - Parallelism (coupling length)
- Near-end (NEXT) and Far-end (FEXT)
- Root cause of noise coupling:
  - SW pin coupled noise to FB pin.
  - **Parallelism higher** in HotRod package
  - **NEXT** (coupled to die EA/Comp)

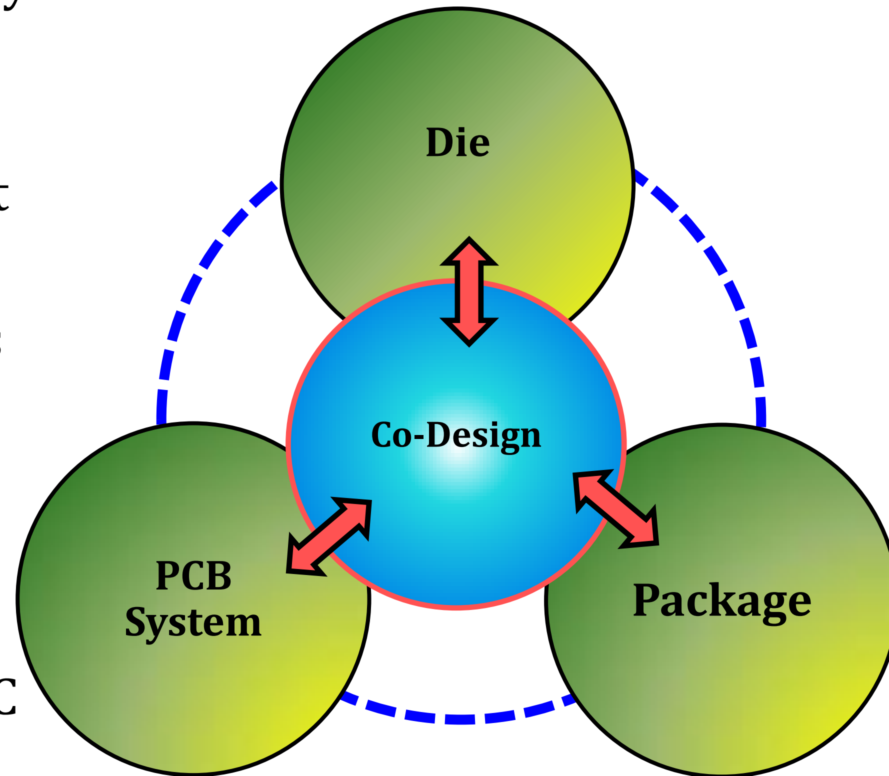


$$I_{near} = I_{Cm} + I_{Lm} \qquad I_{far} = I_{Cm} - I_{Lm}$$



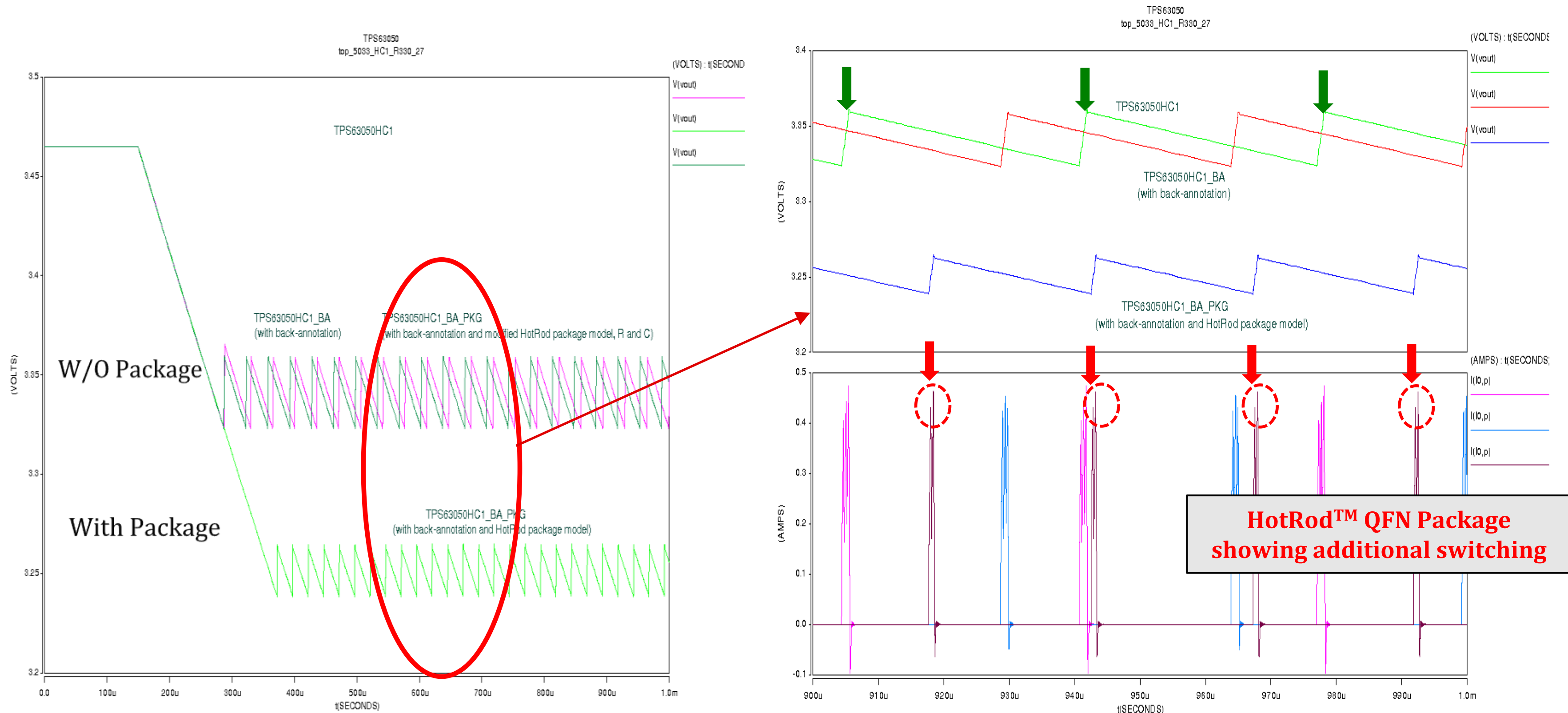
System-Level Modeling Methodology

- Use co-analysis methodology previously developed and correlated to silicon measurements [4-5].
- Employ Cadence Virtuoso environment for system-level analysis.
- Packages and PCBs electrical parasitics models extracted via a 3D quasi-static solver.
- Models include both parasitic self and mutual parasitics.
- Full system-level analysis include DCDC converter transistor spice network, package, and PCB spice netlist.



System-Level Modeling Results

- Performed using system-level co-design modeling methodologies.
- Noise coupling causes EA/Comparator to assume false VOUT and in turn **additional switching** to regulate. Observed in device packaged in HotRod™ QFN.

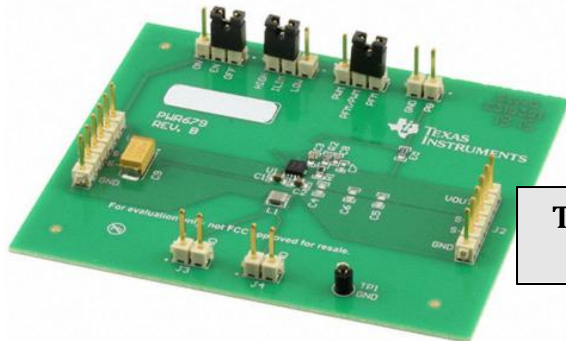


Simulation to Meas. Correlation

- Measurement performed on EVM system.
- Higher activity during PFM mode with HotRod™ QFN package yielding:
  - less efficiency vs WCSP.
- Good correlation between simulation and silicon meas.
- Package and PCB parasitics effect can impact efficiency.

WCSP

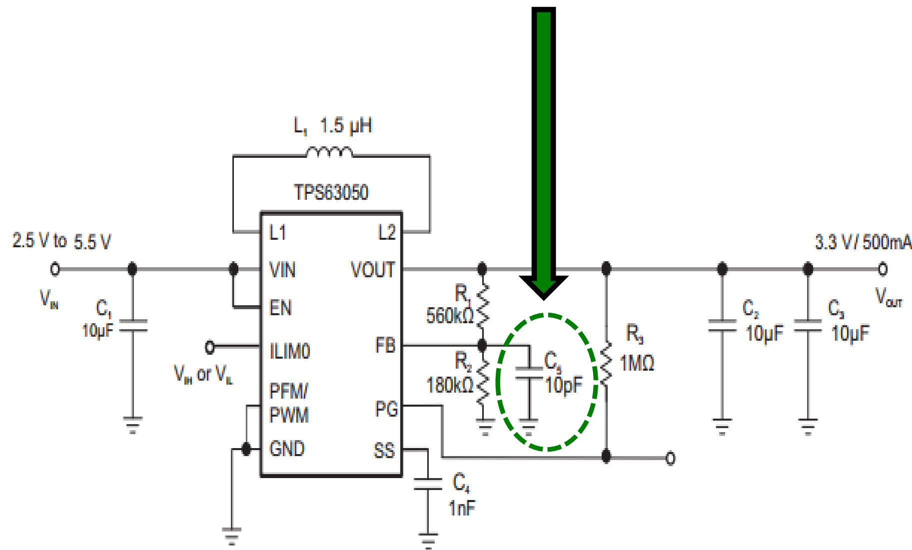
HotRod™



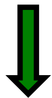
TPS63050 Evaluation Module (EVM)

The Work-Around

- Need to decouple/filter noise coupled to FB line on the HotRod QFN packaged device.
- Many external (i.e. on PCB) mitigation techniques were investigated.
- Optimal fix was to add an external decap (10pF) to FB pin on PCB (shown below)



Lab measurement shows efficiency Improvement with 10pF decap



		1) Standard Hardware Setup - Osci Pic Nr + Efficiency	2) 10pF placed in parallel with R2 - Osci Pic Nr + Efficiency
10mA - output current	VIN = 2.3 V	pic a.1	pic b.1
		Efficiency: 84.48086985 %	Efficiency: 85.67594242 %
	VIN = 2.5 V	pic a.2	pic b.2
		Efficiency: 85.22967672 %	Efficiency: 86.17005354 %
	VIN = 3.1 V	pic a.3	pic b.3
		Efficiency: 86.72348152 %	Efficiency: 87.53031552%
	VIN = 3.5 V	pic a.4	pic b.4
		Efficiency: 86.92023367%	Efficiency: 88.40760181 %
	VIN = 4.1 V	pic a.5	pic b.5
		Efficiency: 85.61944731 %	Efficiency: 89.85032771 %
	VIN = 4.5 V	pic a.6	pic b.6
		Efficiency: 88.81891933 %	Efficiency: 90.82384719 %
	VIN = 5.1 V	pic a.7	pic b.7
		Efficiency: 89.59131074 %	Efficiency: 91.58054242 %
	VIN = 5.5 V	pic a.8	pic b.8
		Efficiency: 90.41464509 %	Efficiency: 92.80062777 %

Summary

- Root cause of efficiency drop on TPS63050™ was primarily due to mutual capacitive (i.e. crosstalk) coupling on package.
- Coupling noise reduction achieved by decap filtering on PCB – not a cost-effective option!
- Issue missed in verification as initial simulations (using first order effect only) with chip-level back-annotation showed no efficiency issue.
- Second and higher order electromagnetic effects are becoming **critical**.
- Use co-design modeling and analysis methodologies to assess system (package and PCB) parasitic impact early in the design phase.
- Co-verification is a **MUST** for first pass design success.

References

[1] TPS6305x Single Inductor Buck-Boost With 1-A Switches and Adjustable Soft Start specification sheet - http://www.ti.com/product/tps63050

[2] AN-1112 DSBGA Wafer Level Chip Scale Package - http://www.ti.com/lit/an/snva009af/

[3] HotRod QFN Package PCB Attachment - http://www.ti.com/lit/an/slua715/

[4] R. Murugan, S. Chakraborty, S. Mukherjee, D. Gope, and V. Jandhyala, "Building IC-package-PCB-system EMI/EMC verification and early design flows: Challenges and Methods", Proceedings of DESIGNCON conf., Santa Clara, February 2010.

[5] J. Chen, R. DeMoor, M. Mi, and R. Murugan, "Using Co-Design Techniques to Minimize IC Package Cost Without Compromising Performance: Simulation and Measurement Validation", IEEE Symposium on Electromagnetic Compatibility & Signal Integrity, EMC&SI, April 28-30, 2015 – **Best Industry Paper Award**.

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