Primary Side Regulation in Flyback Converters Delivers Low Cost, High Reliability and Energy Efficiency

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Outline

• Background
• Primary side regulation Flyback basics
• Improve PSR performance in CCM Flyback
• PSR with minimum standby power without sacrificing transient
• Summary
Standby/Vampire/Idle Power Impact

Source NRDC, Home Idle Load Report, May 2015
Traditional Opto-Coupler Feedback Flyback

- Traditionally isolated flyback power supplies use opto-couplers to feed regulation information across the isolation barrier
- Higher component count and higher cost
- Lower reliability
Eliminating Opto-Coupler

• Higher Reliability
  - No Opto-coupler
    - The aging characteristic of the opto coupler in particular reduces the reliability of the design.
    - The opto-coupler CTR reduces over time which reduces the gain of the feedback loop.
    - The loop has to be overdesigned to account for this affect
  - Fewer components increases the MTBF of the design.

• Better Isolation
  - For applications with high surge or isolation voltage requirements, reducing the number of components crossing the isolation barrier reduces the number of areas of potential breakdown.
PSR Flyback Background

- Most flybacks derive their own bias supply from a bias winding which is in phase with the secondary winding.
- Bias winding voltage is a scaled replica of the secondary winding voltage and can be sensed via a resistive divider to regulate Vout.
Output Voltage Sampling in DCM Flyback

- The bias winding voltage is proportional to the output voltage, with some errors.
- In DCM condition, the output voltage can be sensed at the knee point and minimize the introduced error.
- This sensing method can only be implemented in Boundary Mode or DCM Flybacks.
- For high power designs it is often desirable to operate in CCM.

\[ V_{\text{sense}} = \left( \frac{R_b}{R_t + R_b} \right) \cdot \left( \frac{N_b}{N_s} \right) \cdot [V_{\text{out}} + V_{\text{rect}} + V_{\text{Rsec}} - V_{\text{Leak}} + V_{\text{Rcesr}}] \]
Output Voltage Sampling in CCM Flyback

The resistors are the major source of sensing error

\[ V_{\text{sense}} = \left( \frac{R_b}{R_t + R_b} \right) \cdot \left[ \frac{N_p}{N_s} \right] \cdot \left[ V_{\text{out}} + I_{\text{sec}} \cdot (R_{\text{sec}} + R_{\text{cesr}}) \right] \]

With fixed sampling delay

\[ I_{\text{tmp}} = \left( \frac{V_{\text{cspk}}}{R_{\text{cs}}} \cdot \left[ \frac{N_p}{N_s} \right] - \left[ \frac{(V_o + V_{\text{rect}}) \cdot t_{\text{tmp}}}{L_{\text{sec}}} \right] \right) \]

- For CCM operation the voltage must be sampled during the Off-time, typically a fixed time after turn off (of the Primary FET)
- The error is dominated by the resistive drop
- the current sense demand voltage allows the controller to predict the error in \( V_{\text{sense}} \) and used to improve the regulation accuracy
Output Voltage Regulation for CCM PSR

The voltage regulation accuracy can be significantly improved by using the error compensation.


Measured regulation performance of a 19V, 65 W nominal power stage, operating up to 120 W load, with input bulk capacitor voltage of 120 Vdc and 310 Vdc. Load current was varied from 0 A to 6 A.

<table>
<thead>
<tr>
<th>Lpri</th>
<th>260 µH</th>
<th>MOSFET</th>
<th>STF13NM60ND</th>
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</thead>
<tbody>
<tr>
<td>Res</td>
<td>200 mΩ</td>
<td>Diode</td>
<td>NTST30100CTG</td>
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<tr>
<td>Np</td>
<td>34</td>
<td>Cbulk</td>
<td>127 µF</td>
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<tr>
<td>Ns</td>
<td>6</td>
<td>Cout</td>
<td>1,360 µF</td>
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<tr>
<td>Nb</td>
<td>4</td>
<td>Cbias</td>
<td>22 µF</td>
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<tr>
<td>Transformer</td>
<td>RM10/1</td>
<td>Rsec</td>
<td>60 mΩ</td>
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Standby Power Consumption in Flyback

- Opto coupler consumes most of power during standby mode
- PSR eliminates the feedback components loss but there are plenty of other losses to be considered
- Pre-load is required for PSR Flyback and needs to be minimized

<table>
<thead>
<tr>
<th></th>
<th>X-cap</th>
<th>IC bias power</th>
<th>Start-up resistor loss</th>
<th>Bulk-cap leakage</th>
<th>Pre-load loss</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>~5 mW / 330 nF</td>
<td>10~20 mW</td>
<td>10~20 mW</td>
<td>~0.5 mW</td>
<td>1~10 mW</td>
</tr>
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</table>
Typical Control Law for DCM Flyback Controller

- **Frequency modulation**
  - Fixed peak current
  - Power is adjusted by switching frequency

- **Amplitude modulation**
  - Fixed switching frequency
  - Power is adjusted by peak current

- The switching frequency can’t be zero since PSR needs the switching to sense the output voltage
- At light load, it is desired to minimize the switching frequency for minimum loss associated with the switching frequency
Switching Frequency Considerations

• DCM-flyback $f_{SW}$ follows device Control Law, so $P_{MAX}$ should predict $P_{STBY}$

• First-order approximation using $P_{IN} \approx \frac{1}{2} L_p I_{PP}^2 f_{SW}$ in a ratio:

$$\frac{P_{STBY}}{P_{IN(max)}} = \left(\frac{I_{PP(min)}}{I_{PP(max)}}\right)^2 \frac{f_{STBY}}{f_{SW(max)}}$$

• Assume DCM flyback controller with
  • 3:1 peak current ratio
  • 80 kHz max switching frequency
  • 1 kHz min switching frequency

• There are other losses associated with the switching frequency such as the switch node capacitor discharge

• To further reduce the standby power, lower minimum switching frequency is required
PSR Slow Transient Response

- PSR is a sample-and-hold control system
- Output voltage is sampled only during output rectifier conduction
- Long idle time between pulses at light-load conditions
- When $V_{OUT}$ changes between samples
  - Feedback won’t respond until next sample
  - Results in excessive droop/under-shoot

![Diagram showing PSR Slow Transient Response](image)

![Graph showing Output cap vs. minimum $f_{SW}$](image)

Output cap vs. minimum $f_{SW}$

- $0.5V$ drop
- $1V$ drop
- $1.5V$ drop

Minimum Switching frequency (Hz)
Fast Transient Response using Output Voltage Monitoring

- Output voltage can be monitored all the time
- Once the output voltage drop is detected, the diode is shorted to send the wakeup signal
  - Speeds up Transient Response during light-load/no-load conditions
    - Even for 100% load steps
- Allows smaller $C_{OUT}$
- Low bias current for zero standby
Improved Transient Response

- $V_{OUT}$ is monitored each cycle
  - If $V_{OUT} < 97\%$ of previous $V_{OUT}$
  - Wake-up Pulse is generated

- PSR IC responds to Wake-up Pulse
  - Generates a few fast pulses to
    - Sample $V_{OUT}$
    - Adjust $f_{SW}$ and $D$
    - Faster recovery to heavy step
    - Avoids overreaction to light step
Compare No-Wake to Wake-Up

Response to 2-A load step on 5 V, 540 µF
- Wake-up function disabled
- Vout drops >1 V before detection
  ✓ Control Loop Can’t Respond

Response to 2-A load step on 5 V, 540 µF
- Wake-up function enabled
- Vout droops only 200 mV
  ✓ Regulation within 2 ms

Standby power is kept below 4mW for 85V~265VAC input
Improve Cross Regulation for Multiple Outputs

- PSR can’t assign a dedicated output voltage as regulation target
- Through the DC stacking technique, the output voltage cross regulation can be significantly improved
Summary

• Standby power savings can be a significant improvement for the electrical efficiency
• Primary side regulation Flyback eliminates the opto coupler and feedback components
  – Improves the reliability
  – Reduces the system cost
  – Reduces the standby power
• The PSR technology can be implemented in CCM Flyback but needs extra compensation
• The PSR technology can achieve minimum standby power without sacrificing the transient performance by using the wakeup concept
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