Understanding the Trade-offs and Technologies to Increase Power Density

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A key to design success is often to reduce the size of the power supply. Space is limited. There is constant pressure to do more with less. More broadly, the miniaturization of power supplies has and will continue to enable new markets and applications.

At a glance

This paper examines the limitations to increasing power density and provides technology examples that can help designers overcome these barriers.

1 **What is power density?**
Power density can be viewed several ways depending on the application, but the goal remains the same: Reducing solution size leads to improvements in power density.

2 **What limits power density?**
The primary factors limiting a designer's ability to improve power density are converter power losses — including conduction, charge-related, reverse-recovery, and turn-on and turn-off losses — and the thermal performance of the system.

3 **How to break through power density barriers**
Designers must attack each limiting factor in parallel: reducing switch losses; improving package thermal performance; adopting innovative topologies and circuits; and embracing more passive integration.

The trend toward higher power density has been present in the industry for decades and is projected to continue. Figure 1 shows the reduction in converter size over time for 6-A to 10-A power modules. Technological advancements can result in substantial leaps in size reduction or power output capabilities. Each solid line represents a new generation of technology and demonstrates the associated gains in power density.

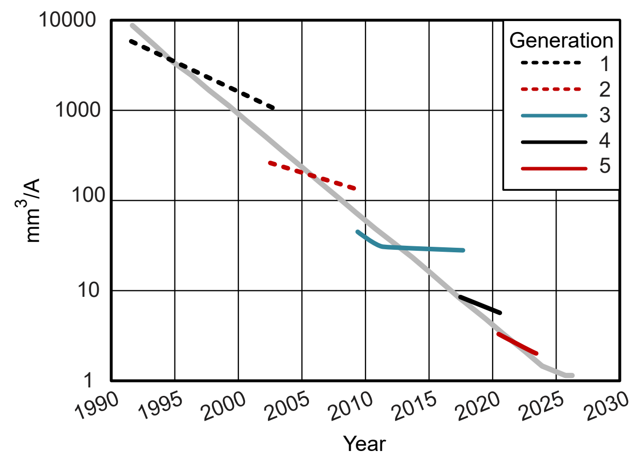


Figure 1. Reduction in power module size over time with new technology generations.

Advances in power density often go hand in hand with developments in other areas like efficiency or cost. Generally speaking, fundamental improvements in power-conversion efficiency enable solution size reductions. Such reductions then have a ripple effect, achieving cost savings through less physical material, fewer components, better cost structures, more solution integration and a lower total cost of ownership.

What is power density?

Power density is a measure of how much power can be processed in a given space, quantifiable as the amount of power processed per unit of volume in units of watts per cubic meter (W/m^3) or watts per cubic inch (W/in^3). These values are based on the converter power rating and the *box volume* (length × width × height) of the

power solution with all components included, as shown in **Figure 2**. It is possible to scale the units to the appropriate power level or size. For example, kilowatts per liter is a common figure of merit (FoM) for onboard battery chargers in electric vehicles because these power converters provide kilowatt levels of power (between 3 kW and 22 kW).

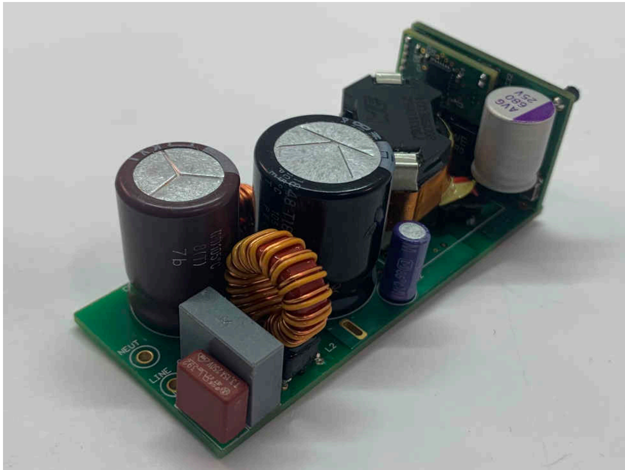


Figure 2. *A 65-W active clamp flyback converter measuring 65 mm by 28 mm by 25 mm.*

Current density is a metric related to power density and is quite useful, quantifiable as current per unit of volume in units of amperes per cubic inch or amperes per cubic millimeter. The converter current rating (usually either input current or output current) is used in the calculation of current density.

Current density is often a more appropriate FoM to apply in applications like point-of-load voltage regulators. The size of these designs scales with output current, and the output voltage levels are typically low, around 1 V. It is possible to artificially inflate power density numbers by assuming an unrealistically high output voltage; thus, current density is a more effectual metric because it removes the output voltage from consideration.

Sometimes volumetric density is not important. The power electronics may not be height-constrained, since other portions of the design are considerably taller. Instead, circuit board area could be the limiting factor. Improving power density in these situations could entail finding ways to stack or 3D-integrate components to reduce the power solution footprint. You would then modify the metrics used to compare solutions to watts per square millimeter or amperes per square inch, which highlights the key design goal (as shown in **Figure 3**).

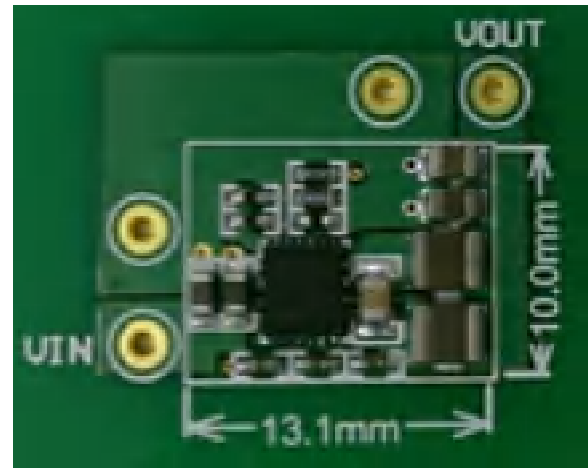


Figure 3. *A 10-A point-of-load converter measuring 13.1 mm by 10 mm in area, resulting in 76 mA/mm^2 of current density.*

You can view power density in a few different ways depending on the application, but the goal remains the same: Reducing solution size leads to improvements in power density. The question now is how to get those gains in power density.

What limits power density?

Engineers and researchers have focused on trying to find ways to improve power density for years. It is a challenging task. Most have focused their efforts on reducing the size of passive components used for energy conversion. Inductors, capacitors, transformers and heat sinks typically take up the largest portion of the power solution size, as shown in **Figure 4**. The semiconductor switches and control circuitry are considerably smaller and more integrated.

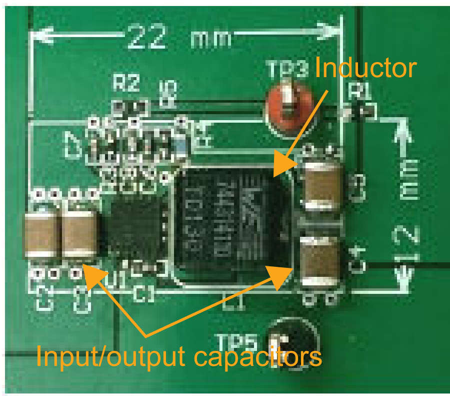


Figure 4. *Passive components such as inductors and capacitors can take up considerable space.*

How do you reduce the size of passive components? One simple solution is to increase the switching frequency. The passive components in switching converters store and release energy every switching cycle. Higher switching frequencies require less energy storage for each of those cycles. For example, consider **Equation 1**, the design equation for the inductor in a buck converter:

$$L = \frac{D \times V_L}{f_{SW} \times \Delta I_L} \quad (1)$$

where

- L is the inductance
- D is the duty ratio
- ΔI_L is the inductor current ripple
- f_{SW} is the switching frequency
- V_L is voltage across the inductor

The inductance needed (L) is inversely proportional to switching frequency (f_{SW}). As the switching frequency increases, the inductance decreases. Lower inductance leads to smaller inductors and space savings. Figure 5 illustrates the difference in size for the inductors needed in a 3-A, 36-V converter switching at 400 kHz versus 2 MHz.

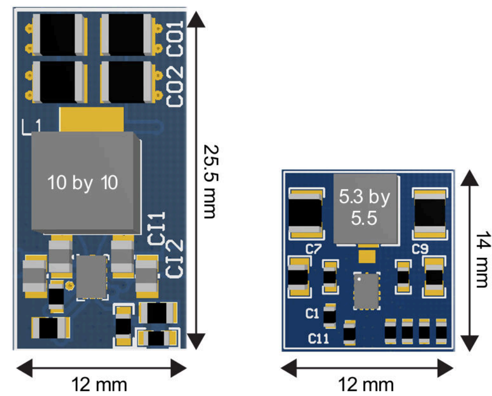


Figure 5. *Size comparison of a 3-A, 36-V converter switching at 400 kHz (left) and 2 MHz (right).*

There are other size benefits of higher switching frequencies. Increasing the switching frequency enables an increase in the control-loop bandwidth, which makes it possible to meet transient performance requirements with less output capacitance. You can design differential-mode electromagnetic interference (EMI) filters with less inductance and capacitance, and use smaller transformers without saturating the magnetic core material.

So why doesn't everybody just increase the switching frequency? As it turns out, it is much easier said than done. Even if you shrunk down all of the passive elements used in power converters to an insignificant size, there would still be opportunities to reduce the power solution size. Power switches, gate drivers, mode-setting resistors, feedback network components, EMI filters, current-sensing components, interfacing circuits, heat sinks and many other components take up valuable real estate. All of these aspects of the overall power design are areas where innovation leads to improved power density. Let's review the primary contributors that limit a designer's ability to improve power density.

What limits power density: switching losses

Although increasing the switching frequency can increase the power density, there is a reason why power converters today typically switch no higher than the megahertz range. Increasing the switching frequency comes with the undesired side effect of also causing increased switching losses and an associated temperature rise. This is largely caused by a few dominant switching losses.

To understand these switching losses, it is important to first introduce some industry nomenclature. In semiconductor devices, the amount of charge associated with that device is typically related to the on-state resistance. A lower resistance results in higher gate charge and parasitic capacitance. This trade-off of resistance and charge is often quantified by the RQ FoM, defined as a device on-resistance multiplied by the total charge that must be supplied to the terminal in order to switch the device at an operating voltage. In addition, the amount of area a device occupies to achieve a target resistance is often referred to as resistance times area (Rsp). You can reduce conduction losses by reducing the metal-oxide semiconductor field-effect transistor (MOSFET) on-state resistance ($R_{DS(on)}$). However, reducing the on-state resistance also causes the device switching-related losses to go up, and increase the overall die area and cost.

Depending on the implementation and application, the impact of different switching losses on the overall power loss can vary. For more details about each type of loss, see the application note ***Power Loss Calculation with Common Source Inductance Consideration for Synchronous Buck Converters***. For the purposes of this paper, we consider a buck converter example and highlight the key limiting factors associated with each loss component.

Key limiting factor No. 1: charge-related losses

In any hard-switched DC/DC converter, charging and discharging parasitic capacitances in the system requires some amount of energy. For a given switch technology and voltage rating, **Equation 2** and **Equation 3** estimate these losses as:

$$P_{SW} = \frac{1}{2} \times C_{DS} \times (V_{DS})^2 \times f_{SW} \quad (2)$$

$$P_{GATE} = Q_G \times V_G \times f_{SW} \quad (3)$$

where

- C_{DS} is the MOSFET drain-to-source capacitance
- V_{DS} is the MOSFET drain-to-source voltage
- f_{SW} is the switching frequency
- Q_G is the gate charge
- V_G is the gate-to-source voltage

As you can see from **Equation 2** and **Equation 3**, you can reduce these losses primarily by reducing the switching frequency (not desirable), improving the MOSFET charge-related FoMs (QG and CDS) or trading off conduction losses with switching losses.

Key limiting factor No. 2: reverse-recovery losses

In a buck converter, reverse recovery occurs when the high-side MOSFET turns on while the body diode of the low-side MOSFET is conducting current, thus forcing the low-side diode current to rapidly transition to the high-side MOSFET. In the process of this transition, a current is required to remove the low-side diode minority charge causing a direct switching loss, see **Equation 4**.

$$E_{RR} = (V_{IN} \times I_L \times t_{RR}) + (V_{IN} \times Q_{RR}) \quad (4)$$

One of the best approaches to reduce the impact of diode reverse recovery is to reduce the stored charge (Q_{RR}) through optimized MOSFET design, or to reduce or eliminate the rising edge dead time, thus negating the impact of the loss completely.

Key limiting factor No. 3: turn-on and turn-off losses

Parasitic loop inductances can cause a number of switching-related losses, which can significantly reduce efficiency. Consider again a buck converter with the high-side MOSFET conducting the inductor current. Turning the high-side switch off interrupts the current through the parasitic inductance. The transient currents (di/dt), along with the parasitic loop inductance, induce a voltage spike. The higher the di/dt, the lower the switching losses, with the consequence of higher device voltage stress. At some turn-off speeds, the buck converter highside switch suffers from breakdown. Thus, you must carefully control the switching speeds in order to maximize efficiency while keeping the DC/DC converter operating in its safe operating area. For more information, see the application note ***Understanding SOA Curves to Operate at High Output Currents and Temperature***.

Additionally, reducing the drain charge of the highside MOSFET can also lead to additional voltage spikes on it, given that there is less capacitance as part of the inductor-capacitor network to absorb the energy stored in the parasitic loop inductance. This presents an additional challenge, as it's best to keep the drain charge as low as possible to reduce the previously mentioned charge-related losses. Mitigating the overall losses associated with these parasitics typically requires that you reduce the loop inductance itself, along with employing other gate-driver techniques.

What limits power density: thermal performance

A key factor that plays into overall power density is the thermal performance of the system. The better the package is at getting heat out, the more power losses you can typically afford without seeing unreasonable temperature rises. These factors are typically captured in data-sheet parameters such as the junction-to-ambient thermal resistance ($R_{\Theta JA}$), along with careful estimates of application conditions. For more details on common thermal impedance values in MOSFET data sheets, watch the video: ***Understanding MOSFET data sheets: Thermal Impedances***.

The overall goal of the thermal optimization of a package and printed circuit board (PCB) is to reduce the temperature rise in the presence of the power converter losses. As the trends toward miniaturization and cost reduction have progressed, the overall size of the converter, power switch and gate driver solution has shrunk. This has caused system-level thermal designs to become increasingly difficult because smaller silicon and package sizes typically result in worse thermal performance, as indicated in **Figure 6**. As the die area shrinks, the associated junction-to-ambient thermal resistance ($R_{\Theta JA}$) gets exponentially worse.

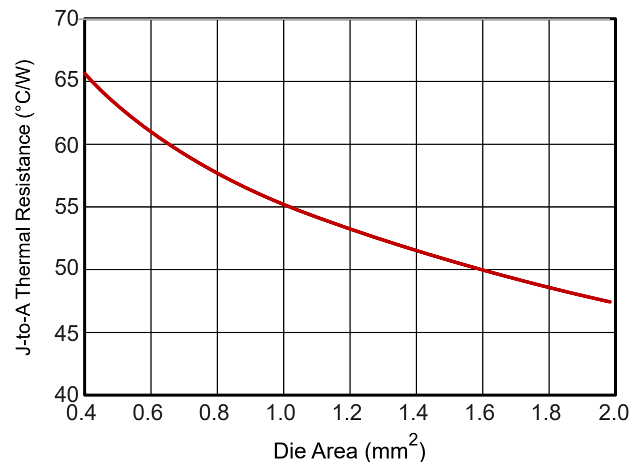


Figure 6. *Package $R_{\Theta JA}$ vs. die area.*

What this graph clearly shows is that as package size, die size and overall power density improve, the expected thermal performance degrades rapidly unless you prioritize innovations in package thermal performance (dissipating the heat) and reducing power losses (generating less heat).

How to break through power density barriers

Choosing to focus on just one of the key elements highlighted in the previous sections can result in overall power density improvements. To really achieve previously unreachable power densities, however, you must attack each factor limiting density in parallel: reducing switch losses; improving package thermal performance; adopting innovative topologies and circuits; and last but not least, integrating.

Switching loss innovations

Investments in semiconductor technology are clearly necessary in order to achieve excellent device performance and FoMs. This can include innovations to improve existing technologies or the development of new materials with fundamentally better performance, such as gallium nitride (GaN) technology for higher-voltage switching applications.

Figure 7 compares a 3.3-V to 1.8-V buck converter using different power process technologies from Texas Instruments (TI). The TPS54319 uses TI's previous power process node, while the TPS62088 uses TI's latest power process node with lower RQ FoMs. As the efficiency curve shows, the TPS62088 is able to switch at 4 MHz compared to the TPS54319 switching at 2 MHz while maintaining virtually the same efficiency. This can halve the size of the external inductor. In addition, because TI's new power process node also enables significant R_{SP} reduction, the overall package size drops from 4 mm^2 to 0.96 mm^2. Although this size reduction is very attractive from a power density perspective, it also introduces challenges with respect to temperature rise, which we will address in an upcoming section.

The TPS54319 switches at 2 MHz and is using TI's previous power process node, while the TPS62088 switches at 4 MHz using TI's newest power process with improved switching FoMs

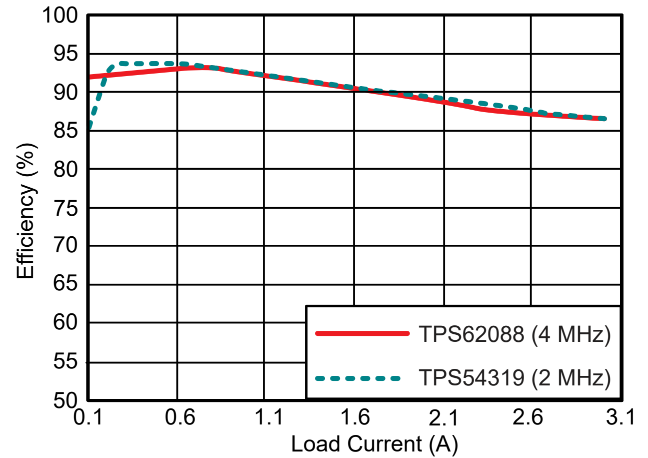


Figure 7. Comparison of DC/DC efficiency for a 3.3-V to 1.8-V buck converter.

GaN's unique combination of zero reverse recovery, low output charge and high slew rate enable new totem-pole topologies such as bridgeless power factor correction. These topologies have higher efficiency and power density that silicon MOSFETs cannot achieve. Figure 8 compares of TI GaN technology at 600 V compared to some of the industry's best silicon carbide (SiC) and superjunction silicon devices. TI GaN technology offers substantially lower losses and thus enables higher frequency.

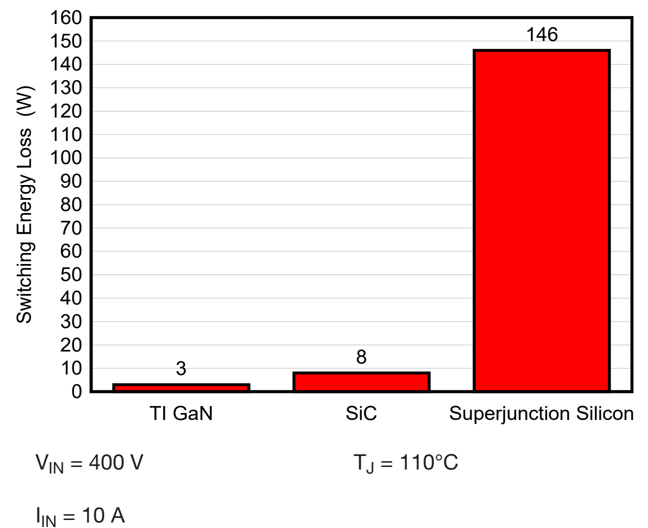


Figure 8. Switching energy losses comparison.

Package thermal innovations

The ability to get the heat out of an integrated circuit (IC) package directly impacts power density. As mentioned previously, this becomes an increasingly important problem as packages continue to shrink. Further, in a typical power converter, the semiconductor devices can often become the hottest part of the solution, especially with the Rsp shrinking rapidly.

TI has invested in the development and adoption of the HotRod™ package, which replaces typical bond-wire type quad flat no-lead packages (QFNs) with a flip-chip style package. Figure 9 and Figure 10 show how a HotRod QFN can eliminate the bond wires while keeping a QFN-like footprint. This results in a significant reduction in parasitic loop inductance, typical in flip-chip packages, while also keeping some of the benefits of the QFN package thermal performance. The HotRod QFN includes an interconnect between the leadframe and die.

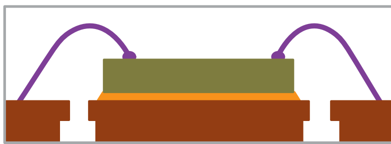


Figure 9. *Standard bond-wire QFN package with exposed pad.*

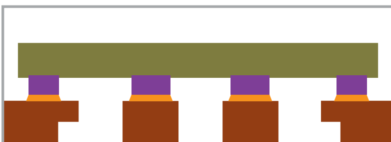


Figure 10. *HotRod interconnect package (flip-chip-on-lead) QFN package.*

One challenge with the HotRod package is that it becomes more difficult to build large die attach pads (DAPs), which are typically very helpful in improving package thermals. To overcome this challenge, TI recently enhanced the HotRod QFN to maintain its existing advantages while simultaneously enabling packages with large DAPs.

Figure 11, Figure 12 and Figure 14 show the 4-A LM60440 synchronous converter that includes these technology enhancements to improve thermal performance. You can see that the footprint is conducive to a large DAP in the center of the package. This DAP has about a 15% temperature rise benefit compared to the previous generation. You can read more about the evolution of these packages in our Analog Design Journal article, ***Designing with small DC/DC converters: HotRod™ QFN vs. Enhanced HotRod™ QFN Packaging***.

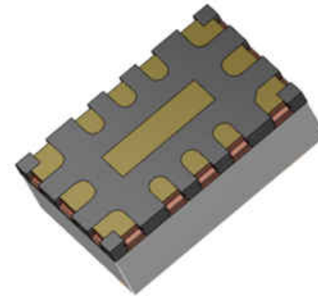


Figure 11. *Enhanced HotRod QFN with a large DAP.*

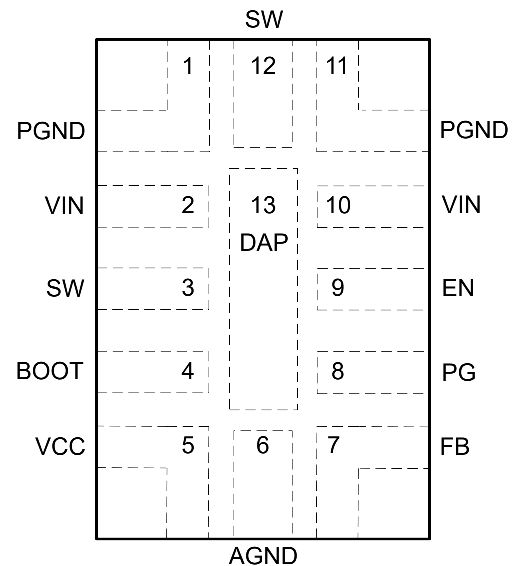


Figure 12. *Pinout of LM60440 in Enhanced HotRod QFN.*

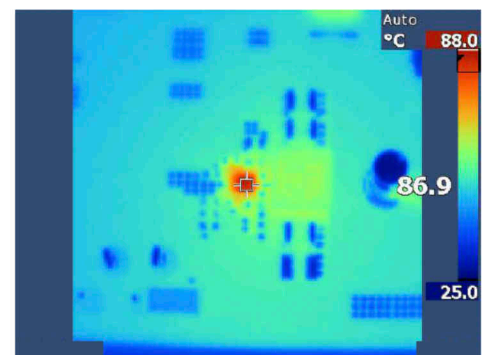


Figure 13. *Thermal performance of a conventional HotRod package.*

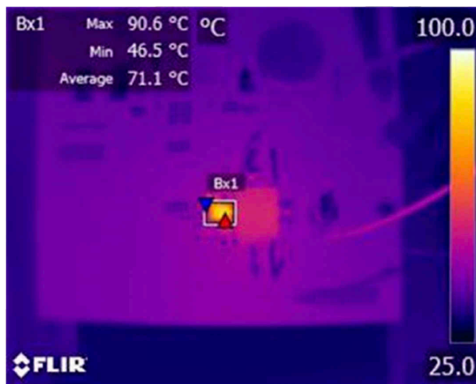
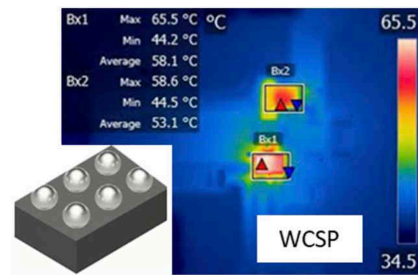


Figure 14. *Thermal performance of the LM60440 with DAP in the Enhanced HotRod QFN package, with average temperature lowered to 71.1°C.*

Additionally, many designers prefer to leverage small-outline transistor (SOT) surface-mount packages, as they tend to be low cost and their pin leads are easier to assemble with. TI has paired improved process technology and circuit IP with the SOT-563 package so that the low-profile, dual-row pin configuration can meet the demands for higher current density. The **TPS566242** 3-V to 16-V synchronous buck converter is one recent example. The device supports up to 6 A of continuous current at 98% duty cycle in a 1.6-mm x 1.6-mm SOT-563 (6-pin) footprint.

Similarly, when working with wafer chip-scale packages (WCSPs), most of the heat conducts directly out of the bumps, down to the PCB. The larger the bump area in a WCSP, the better the thermal performance. TI recently developed and released PowerCSP™ packaging, which aims to improve package thermals and electrical performance by replacing some of the typical circular bumps in a WCSP with large solder bars. **Figure 15** illustrates an example implementation of this technology in the **TPS62088**. **Figure 15** shows the standard WCSP, while **Figure 16** shows the same device with the PowerCSP packaging. The temperature rise is reduced by about 5% without any other changes in the system.

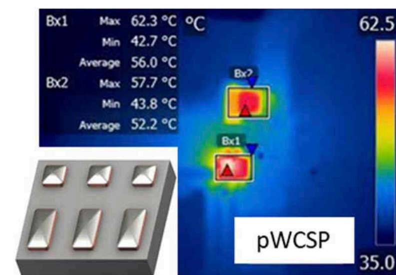


V_{IN} = 5 V | V_{OUT} = 1.8 V

I_{OUT} = 3 A | T_A = 25°C

Measurement point: Bx1

Figure 15. *Thermal performance of the TPS62088YFP WCSP version.*



V_{IN} = 5 V | V_{OUT} = 1.8 V

I_{OUT} = 3 A | T_A = 25°C

Measurement point: Bx1

Figure 16. *TPS62088YWC PowerCSP version.*

Advanced circuit design innovations

A negative byproduct of lower Rsp and lower RQ FoMs is the impact that a reduced drain charge has on transition losses. Looking at **Figure 17**, you can see that for a fixed amount of voltage overshoot, the turn-off loss of this buck converter goes up significantly as the drain charge reduces. In the presence of this trade-off, new and advanced gate driver intellectual property (IP) is necessary to switch the MOSFETs as fast as possible while keeping them inside their electrical safe operating area, despite a continued roadmap of improved RQ FoM MOSFETs. As the drain charge reduces, the turn-off energy increases in order to maintain a fixed drain-to-source voltage stress.

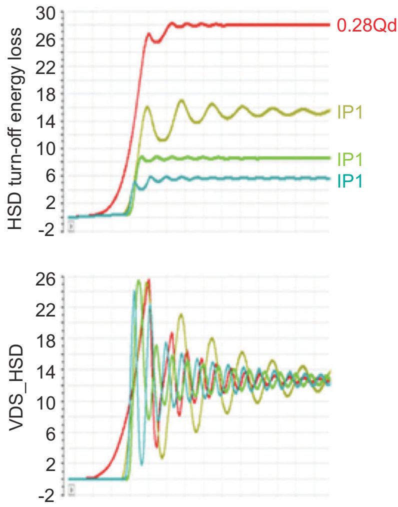


Figure 17. Turn-off energy losses for various MOSFET technologies.

Along these lines, TI has recently developed a family of gate-driver techniques that enables very fast switching despite the lower RQ FoM MOSFETs, resulting in better charge and transition losses but still keeping the MOSFETs in their electrical safe operating area. As you can see when comparing Figure 18 and Figure 19, it is possible to reduce the turn-off energy loss by as much as 79% while keeping the peak voltage stress fixed. In some designs, as shown in Figure 19, this reduction can result in efficiency gains as high as 4% at the peak efficiency point.

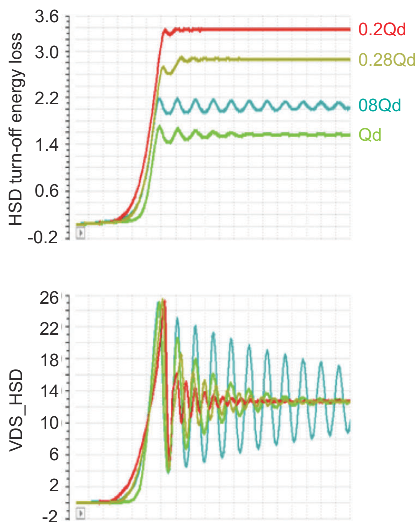


Figure 18. Comparison of gate-driver IP that enables low drain charge and low turn-off energy.

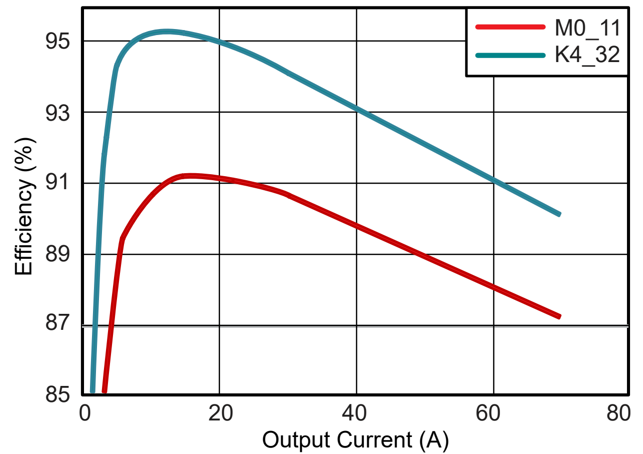


Figure 19. Impact of gate-driver IP on system efficiency.

In addition to advanced gate-driver technology, there is significant opportunity to improve power density through topology innovations. Figure 20 illustrates a flying capacitor four-level (FC4L) converter topology that enables a number of critical power density advantages, including better device FoMs through lower device voltage ratings, reduced magnetic filter sizes and better thermal distribution. These benefits translate into the improved power density shown in Figure 21. Compared to other topologies using SiC, the TI solution offers a significant volume reduction through the use of this particular topology, combined with GaN benefits and advanced packaging technologies. The FC4L GaN solution from TI offers the best power density.

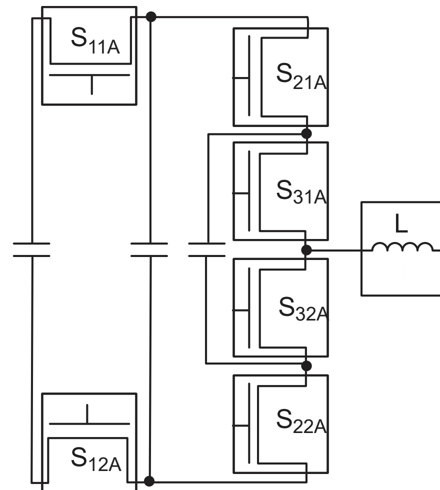


Figure 20. Flying capacitor four-level converter topology using GaN switches.

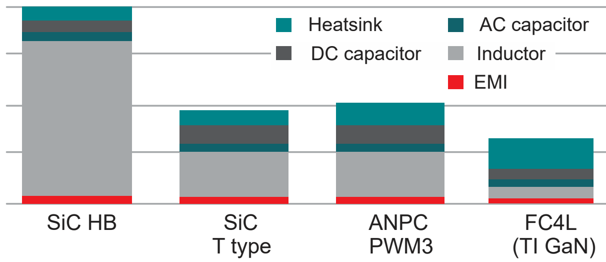


Figure 21. *Overall volume of topologies and switch types.*

Integration innovations

The final piece of the puzzle toward the best power density is integration. Cost-effective integration reduces parasitics, reduces the bill of materials, enables higher efficiency and saves space. Integration applies to several aspects of power management. It can entail including more electrical circuits in an IC, adding more components in a package, or packing more in the power solution through other physical or mechanical means. A few examples of technology leadership in this area are drivers integrated with GaN FETs, capacitor integration for critical loop inductance reduction, and 3D stacking of passive components.

Including gate drivers with switching power FETs has many benefits. The switching gate-drive loop inductance decreases, which enables higher switching speeds, more robust operation and fewer components. GaN FETs in particular benefit from this integration. Additional features like overcurrent protection, overtemperature protection and monitoring are included in devices like the **LMG3522R030-Q1** (see **Figure 22**). This integration significantly simplifies the power-management solution and enables designers to achieve all that GaN has to offer.

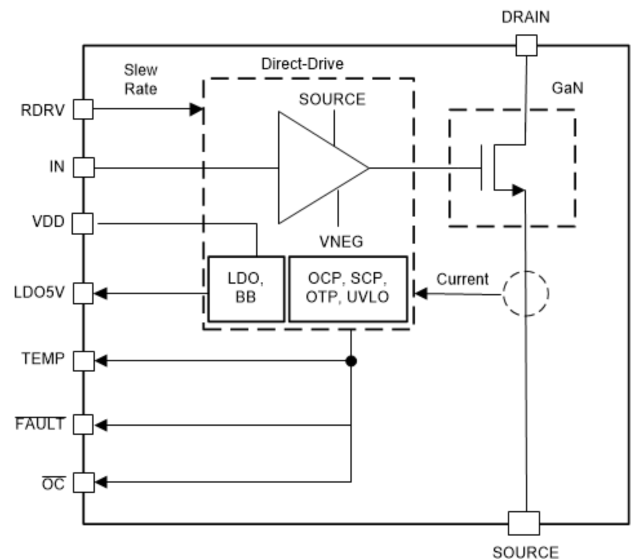


Figure 22. *Driver, protection and monitoring functions integrated with a GaN switch on the LMG3522R030-Q1.*

Another avenue of integration is including passive components in the IC package. Integrating high-frequency decoupling capacitors is one technique used in the LMQ61460-Q1, shown in **Figure 23**. Integrating the capacitors can improve efficiency by reducing critical loop parasitic inductance and reduce EMI. This power solution can also increase switching times without sacrificing system robustness or exceeding thermal limits, leading to higher switching frequencies and solution size reductions with less EMI filtering. The UCC14240 leverages magnetic component integration to provide an isolated bias supply without an external transformer. This approach reduces size, complexity and EMI.

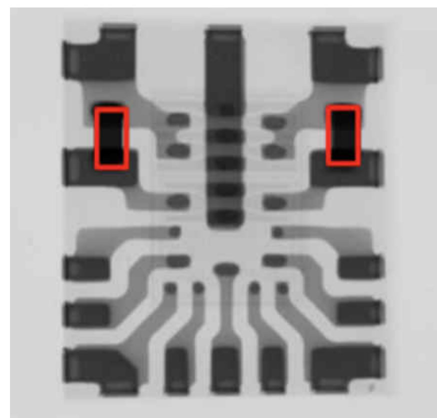


Figure 23. *X-ray photograph of the LMQ61460-Q1, with the integrated bypass capacitors highlighted.*

A final example of integration is 3D stacking of components, which occurs often in power modules with integrated passive components. Figure 24 uses the TPS82671 as an example. This device embeds the power IC in a laminate substrate and places an inductor and input and output capacitors on top. This incredibly small solution does not require additional components. A simple integration concept can achieve amazing results, saving PCB area and simplifying the power solution.

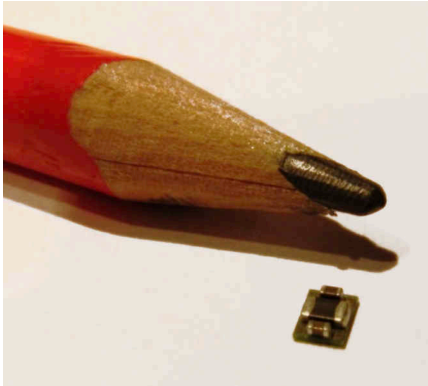


Figure 24. *Tiny power module with an integrated power IC, inductor and capacitors.*

Conclusion

The trend toward higher power density is clear. There are major limitations to achieving the more compact power solutions. Overcoming power losses and thermal performance challenges requires innovations in switching properties, IC packaging, circuit design and integration. Each of these puzzle pieces by itself provides significant improvement opportunities in power density, yet each technique is orthogonal from each other. As a result, you can obtain a distinct improvement in power density by combining technologies from each category.

Imagine a product with the best switching device FoMs and industry-leading package thermal capability, using multilevel topologies with the lowest loop inductance through passive integration. The technological advancements play off of each other and result in power density breakthroughs.

Achieving more power in smaller spaces, and enhancing system functionality at reduced system costs, are now possible using TI's advanced process, packaging and circuit-design technologies. To learn more, see ti.com/powerdensity.

Additional resources

- Battery charger ICs
- Buck-boost and inverting regulators
- Gallium nitride (GaN) ICs
- Isolated bias supplies
- Isolated gate drivers
- LED drivers
- Linear regulators (LDO)
- Multi-channel ICs (PMIC)
- AC/DC and isolated DC/DC controllers and converters
- Power switches
- Step-down (buck) regulators
- Step-up (boost) regulators
- USB Type-C and USB Power Delivery ICs

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