

**ADC08100,ADC12081,ADC12181,ADC12281**

*Easing the ADC Selection Process*



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# Technology Edge

## Easing the ADC Selection Process

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As system designers we like to use as few component types as we can. This simplifies and accelerates the design process and helps to minimize our total cost of ownership. During the design process we learn about the capabilities, limitations and quirks of the products we choose to use in the design. Using a common part for multiple designs means remembering fewer quirks and limitations. The icing on the cake is that purchasing a larger quantity of one device can reduce its unit cost.

### Many Design Issues

As an example of these "quirks", sampling analog-to-digital converters (ADCs) typically have a dynamic input capacitance that can make these inputs difficult to drive without adding noise to the conversion result. Not all amplifiers can drive this "flying capacitor" type of input. Of those that can, some handle the task better than others. It can take a lot of time to evaluate a lot of amplifiers and find an acceptable one to drive the chosen ADC. So, many times we rely upon the suggestion of the ADC manufacturer to save valuable time.

### The Current Solution

Whenever you design around an ADC you have not used before, you must learn to use that new device and work out an acceptable PCB layout. Whenever you can use a part you have used before, you are already familiar with the operation and layout requirements of that device. This can save a lot of time in a tight schedule.

However, there may be penalties for doing this. Sticking with older, familiar products has its price. Newer technology may reduce prices, increase performance and lower power consumption. In *Figure 1* you can see power consumption vs. sample rate for a family of 8-bit ADCs rated at 50MSPS (Megasamples per Second), 80MSPS and 100MSPS. There is a little power saving as sample rate is reduced below 80MSPS, but at 80MSPS the power consumption is the same as at 100MSPS. With the low slope of the power vs. sample rate curve, there is a power penalty for using these converters at lower than rated sample rate.

What you would really like is a "one size fits all" component. Suppose you have an application that needs an 8-bit, 100MSPS ADC and a 27MSPS ADC. Additionally, you know that you will be working on future designs requiring high-speed 8-bit ADCs. Using a single ADC family for all of these sockets will mean that you can reduce design time. This is because you only need to know how to best use a single device for all ADC sockets. Since these three products are pin-compatible with each other and are specified for a minimum sample rate of 1MSPS, they allow a single layout for 8-bit ADCs with sample rates from 1 MSPS to 100MSPS. Additionally, you might be able to realize a reduction in manufacturing costs if all sockets used the same part type. Repeated use of a family such as this is one approach taken by some designers to ease their design task.

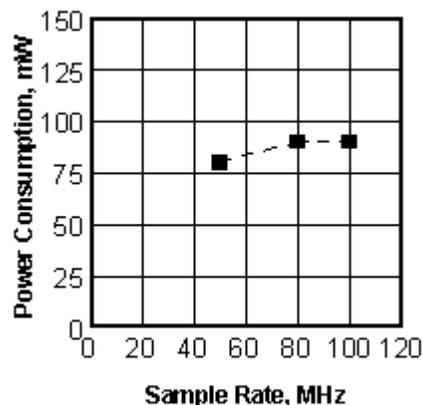


Figure 1. Using an ADC at sample rates below its rating

can result in the consumption of more power than needed.

Another example of a family of ADCs that designers have chosen with a common pin configuration to at least achieve a single layout is that family consisting of the [ADC12081](#), [ADC12181](#) and [ADC12281](#). These are pin-compatible 12-bit, 5MSPS, 10MSPS and 20MSPS analog-to-digital converters that permit a single layout for 12-bit ADCs with required sample rates from 0.5MSPS to 20MSPS. However, as good as these products are, there is, again, a power penalty to pay for using these ADCs at less than their specified sample rate.

### The Situation Has Changed

Even better than a family of part, which still requires multiple inventories and lower total volumes per part, would be a single device that can economically fit into all ADC sockets. There now is a single 8-bit ADC, the [ADC08100](#) from National Semiconductor Corporation, with virtually flat dynamic performance at sample rates from 20MSPS to 120MSPS. Performance of this device is guaranteed at 100MSPS. *Figure 2* shows how this new converter yields virtually the same performance over that 20MSPS to 120MSPS range. Note that the variation in SINAD (Signal to Noise and Distortion) over this range is only about 1.5dB.

*Figure 2* also shows the performance of other popular of 8-bit ADCs. The obvious advantage of the ADC08100 is the wide range of sample rates available with a single converter while maintaining essentially flat dynamic performance as measured by SINAD.

I chose SINAD for comparison because this parameter is widely considered to be the best single specification to describe how well an ADC performs. SINAD combines SNR and THD into one specification and can be calculated as

$$\text{SINAD} = -20 \times \log \sqrt{10^{\frac{\text{SNR}}{10}} + 10^{\frac{\text{THD}}{10}}}$$

The ADC08100 allows the circuit designer to learn the use and layout of a single high speed, 8-bit ADC for sample rates of 20MSPS to 120MSPS. In many cases this will incorporate all high speed 8-bit sample rates needed in all of your systems.

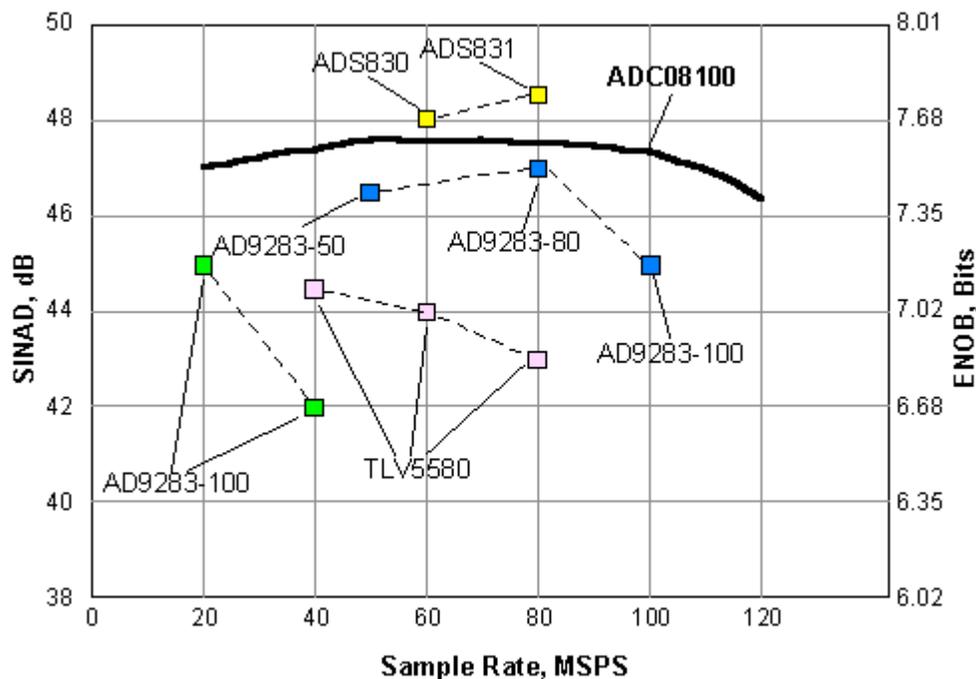


Figure 2. The ADC08100 provides a flatter performance response

over a wider range of sample rates than does competitive solutions.

The wide sample rate range, however, is not the only advantage of the ADC08100 over using a family of pin-compatible ADCs. Other ADCs have a power consumption that decreases with lower sample rates, but the amount of decrease is small such that the total power consumed conforms to the formula

$$P_C \text{ (mW)} = a + b \times f_{\text{CLK}}$$

where the "a" term is much larger than "b". This leads to a power consumption that is nearly independent of sample rate, resulting in a power penalty for using the product at sample rates lower than the specified maximum clock rate. For example, one popular ADC family of three converters exhibits a power curve between 50MSPS and 80MSPS that appears to be

$$P_C \text{ (mW)} = 63.33 + 0.33 \times f_{\text{CLK}}$$

The ADC08100 power consumption, on the other hand, is directly proportional to sample rate it consumes a very low 1.3mW per MSPS. The "a" term is *zero*, so there is no power penalty for operating the ADC08100 at sample rates below its rated 100MSPS! See *Figure 3*.

Many of the disadvantages of other approaches to multiple sample rate needs of 8-bit ADCs are eliminated by the ADC08100. Only the power needed for the actual sample rate used is consumed and dynamic performance is virtually flat. Additionally, all the advantages of using a family of ADCs is embodied in this single ADC.

As an added bonus, using a single part type for all 8-bit ADC needs often reduces the total cost of ownership. Purchasing a large quantity of one ADC type could enable a lower unit price than would the purchase of smaller quantities of more converter types. Inventory costs could be reduced with fewer part types. I have already described the design and layout advantages.

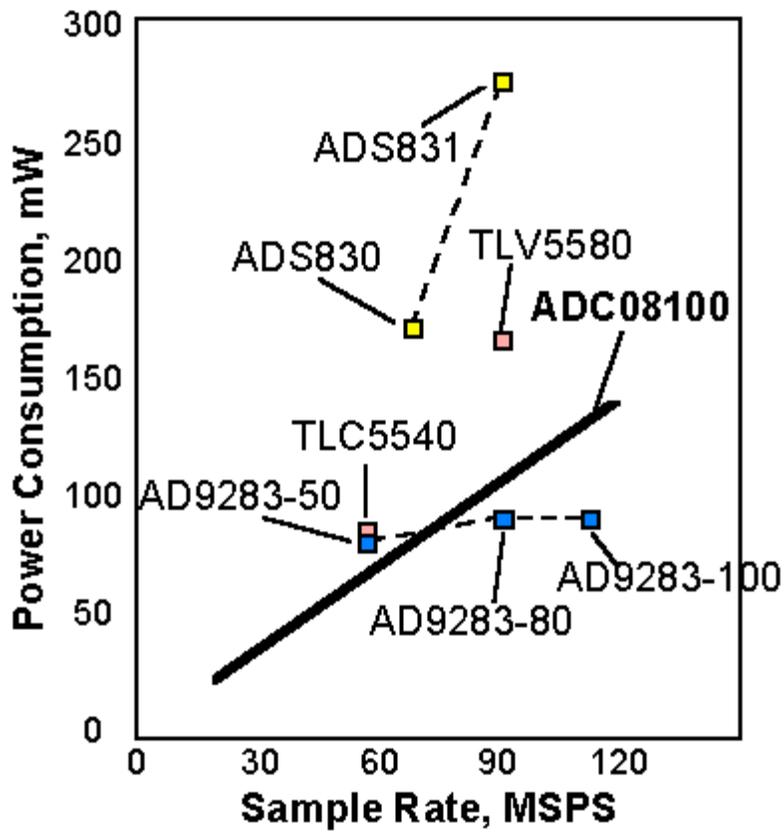


Figure 3. There is no power penalty when using the ADC08100 at lower than the rated sample rate, as is true of other approaches.

While using ADC families is a good strategy that allows shorter design times, there is now a better alternative in a single device. Undoubtedly, other ADC manufacturers will eventually provide similar solutions. For now, however, the [ADC08100](#) is the only universal high speed 8-bit ADC solution available.

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