Technical White Paper

Implementing Native PCIe Interconnects Over Automotive Cable Channels

ABSTRACT

As Peripheral Component Interconnect Express (PCIe®) continues to gain popularity with the automotive industry as a solution for addressing critical high-bandwidth and ultra-low latency computing demands of next-generation distributed automotive architectures, challenges for its widespread adoption remain. For automotive processors to take full advantage of this interface standard for shared processing, an automotive cabling interconnect must be defined that will help transform PCIe from an *intra*-Electronic Control Unit (ECU) interface to an *inter*-ECU interface. Realizing native PCIe over automotive cable channels - which we are defining for the purposes of this paper as the combination of automotive cables and connectors - involves careful consideration of the physical interconnect. As leading automotive industry vendors, TI, Rosenberger, and GG Group have developed a proposed PCIe specification for automotive cable channels to enable a reliable implementation in vehicles and help standardize adoption of this interface standard. This white paper outlines the key aspects of the proposed specification and addresses key considerations and challenges related to defining PCIe over cable channels.

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Trademarks

1 Introduction – Automotive Industry Trends in ADAS and Vehicle Connectivity

As Original Equipment Manufacturers (OEMs) and Tier-1 suppliers prepare to support technological advances in both Advanced Driver Assistance Systems (ADAS) and vehicle connectivity, they are rethinking the automotive data backbone architecture. Rather than rely on computing to be implemented based on domains (for example, ADAS domain), future automotive data backbones are shifting from domain to zonal architectures. This is accomplished by incorporating local computing nodes, or *zone controllers*, to connect Electronic Control Units (ECUs) and interfaces based on location within their *zone*, regardless of their respective domain. These zone controllers then connect to a powerful central compute node that handles the data accordingly.

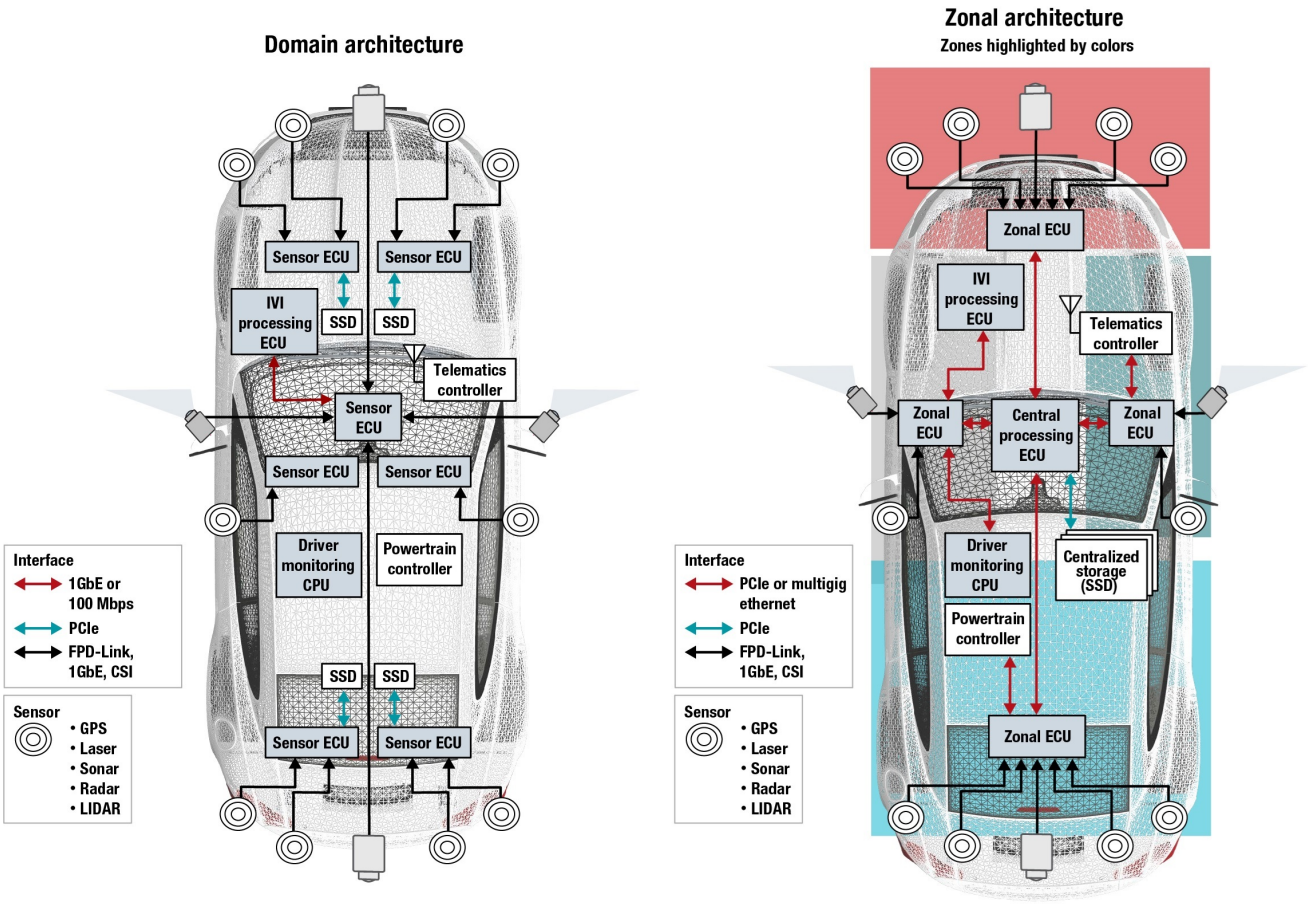

Figure 1-1. Domain Architecture vs. Zonal Architecture

To enable distributed processing in zonal architectures, the automotive data backbone must employ high-speed interfaces that support high bandwidth and low latency. In particular, careful consideration for ultra-low latency must be taken when the shared data is used for safety-critical real-time processing. The Peripheral Component Interconnect Express (PCIe) ecosystem has already addressed these types of high bandwidth, ultra-low latency performance demands for industrial data centers, and it is well-equipped to serve the automotive industry in the same way!

2 Realizing PCIe over Automotive Cable Channels

Realizing PCIe over automotive channels involves careful consideration of the entire physical interconnect. The complete end-to-end channel, or TX-to-RX link, consists of two PCB channels at both ends of the automotive cable channel. The PCB channel includes the section from the TX/RX PHY to the corresponding PCB header. The automotive cable channel may consist of a single cable assembly, such as a bulk cable with two assembled connectors, or several cable assemblies. In the case of several cable assemblies, the cable channel includes inline connections. The limit for the cable channel length is determined by high-speed properties such as insertion and return loss in accordance with the channel limits over the required bandwidth.

This technical white paper specifically addresses the challenges and considerations for implementing native PCIe over automotive cable channels.

2.1 Key PCIe Technology Considerations

Several tradeoffs are necessary to preserve the benefits of native PCIe connectivity while addressing OEM needs for a common cable channel solution and minimized cable cost and weight.

1. **Maintain Similar Cable Channel Type to Other High-Speed Interfaces:** The cable assembly solution used for PCIe should be as similar as possible to other high-speed interface technologies such as 2.5/5/10GBASE-T1 Ethernet. In this way, OEMs need only qualify a single connector interface plus cable type combination for a variety of high-speed interfaces throughout the vehicle.
2. **Only Connect Essential PCIe Signals:** To reduce cable count and weight, only essential high-speed in-band PCIe signals need be connected over automotive cable. Low-speed side-band signals on the local PCB may be left unconnected. To reduce the risk of EMI resonance, the 100 MHz PCIe reference clock may be omitted from the cable interconnect. The PCIe specification supports SRNS (Separate Reference Non-Spread) and SRIS (Separate Reference Independent Spread) for independent clocking on either side of the cable.
3. **Trade Cable Count for Native PCIe Performance**: Native PCIe transport requires dedicated TX and RX channels. As a result, two STP cables are needed per lane (one TX and one RX per lane), resulting in a comparative increase from the single cable used by other high-speed interfaces such as Multigig Ethernet. It is important to note that this trade-off in cable count comes with the value of preserving both native PCIe performance and a non-proprietary PHY interface over the cable while leveraging the full ecosystem.
4. **Maintain Similar PHY Layer Requirements**: Native PCIe implements NRZ signaling with dedicated TX and RX directions and has the ability to pass EMC requirements. NRZ signaling maximizes the vertical eye margin compared to PAM-4 or PAM-16 modulation schemes. With dedicated TX and RX channels, it is also not necessary to implement a separate automotive PCIe PHY to support full-duplex bidirectional signaling interfaces, where complex DSPs for noise and echo cancellation are needed.

2.2 Key Channel Specification Considerations

In order to make a reliable connection in millions of vehicles, it is important to determine the high-speed requirements of the PHYs for the link between them and align them with the performance that the cables and connectors can offer. Therefore, a channel specification is required to test high-speed channel parameters against the limits. High-speed channel specifications describe the requirements for the cable and PCB channel based on S-Parameters.

Key parameters are the required frequency bandwidth and primarily the insertion and return loss. Taking EMC behavior into account, it is beneficial to specify screening and coupling attenuation. Furthermore, a detailed description of measurement setups and procedures is necessary to compare different results.

TI, GG Group, and Rosenberger have partnered in preparing a proposed automotive PCIe channel specification alongside a measurement setup and procedure description, which can act as a future basis for a possible official PCI-SIG standardization for automotive use cases. The key requirements in Table 2-1 are proposed for automotive PCIe 3.0 cable channel limits:

Table 2-1. Proposed Automotive PCIe 3.0 Cable Channel Limits

Parameter/ Metric	Proposed Limits
Bandwidth	4.4 GHz (1)
Insertion Loss budget	26.4 dB @ 4 GHz
Return Loss budget	6 dB @ 4 GHz
Screening / Coupling attenuation	45 dB @ 4 GHz / 55.5 dB @ 4 GHz

(1) The cable channel must support an insertion loss that is free of suck-outs, dips, or notches up to at least 10% beyond the Nyquist frequency of the highest transfer rate for safety margin across temperature, aging, and manufacturing processes.

2.3 Key Automotive Cabling Considerations

It is not enough for the cable to meet performance needs in normal room temperature circumstances. Automotive qualification necessitates different aging tests, such as long-term aging for 3,000 hours at elevated temperatures, to characterize cable performance stability. Following all aging tests, pre-defined critical high frequencies limits are expected to be maintained. Different cable design parameters, such as twist length, dielectric constants of the cores, and isolation material selection must also be considered to meet interface performance requirements.

GG Group offers a vast amount of high-quality automotive cables for coaxial and differential applications at Gigabit speeds. To illustrate a suitable automotive cable for PCIe 3.0, the GG 2Speed® 251 STP cable (designed and manufactured by GG Group) may be considered. The shielding of the cable consists of aluminum–plastic foil that is wrapped around the two twisted cores shown in Figure 2-1. A copper braid follows as an additional shield and helps to meet the required EMC performance (screening and coupling attenuation) up to 4.4 GHz.

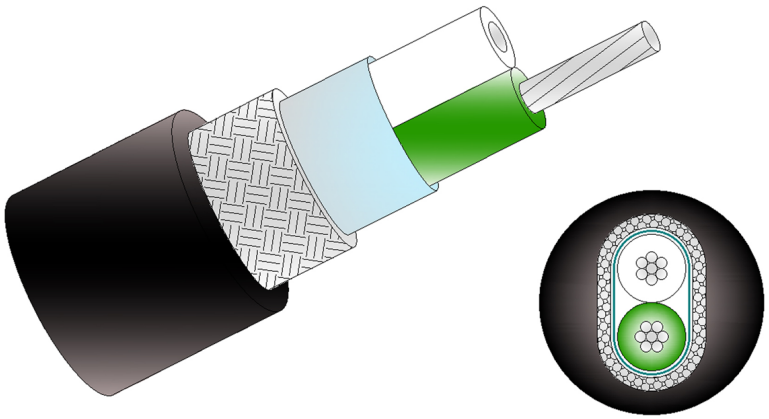

Figure 2-1. GG 2Speed® 251 STP Cable Construction Cross-Section

The GG 2Speed® 251 STP is suck-out free up to 5 GHz, showing a notch at around 5.2 GHz due to the cable construction. The notch is primarily affected by the lay length of the white and green wire. The GG 2Speed® 251 STP cable also shows good performance against the *Proposed Automotive PCIe 3.0 Raw Cable Limit* formula, as shown in Equation 1 and Figure 2-2.

$$IL\ [dB/10m] = -\left(0.69f^{0.45} + 0.0027f\right) / 15 \quad (1)$$

where

- f = Frequency in MHz up to 4400 MHz

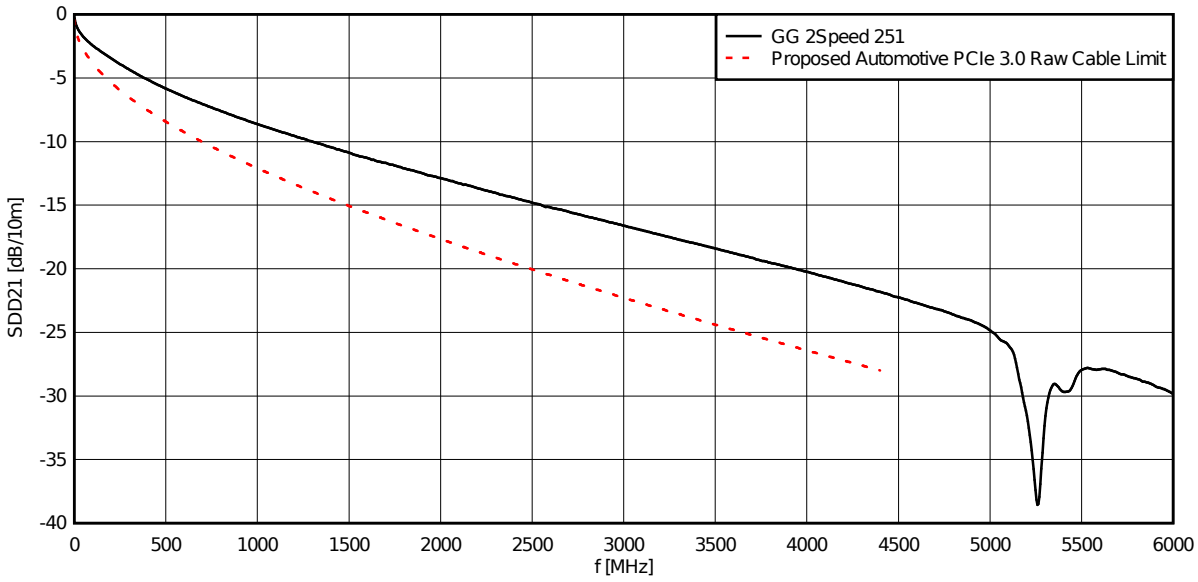

Figure 2-2. GG 2Speed® 251 – Insertion Loss vs. Proposed Automotive PCIe 3.0 Raw Cable Limit

Cables supporting higher frequencies than the GG 2Speed® 251 are also in development and will serve to enlarge the GG 2Speed® product family. For instance, first prototypes of the GG 2Speed® 256 meet the increased frequency needs of PCIe 4.0, with bandwidth to support a linear insertion loss up to 10 GHz.

2.4 Key Connector and Assembly Considerations

To meet the channel requirements, Rosenberger offers the high-speed connector duo of H-MTD® for differential signal transmission and HFM® in case a coax transmission is preferred. For best screening attenuation, both systems offer 360° shielding to sustain the excellent shielding behavior of the bulk cable.

Figure 2-3. H-MTD® Product Family Selection with Cable Assemblies and PCB Headers

Since return loss (RL) is mostly determined by connectors, the impedance along the H-MTD® and HFM® is precisely matched to the reference impedance of 100 and 50 Ohms, respectively. Figure 2-4 shows the corresponding gated RL of H-MTD® connectors on both ends of a cable assembly.

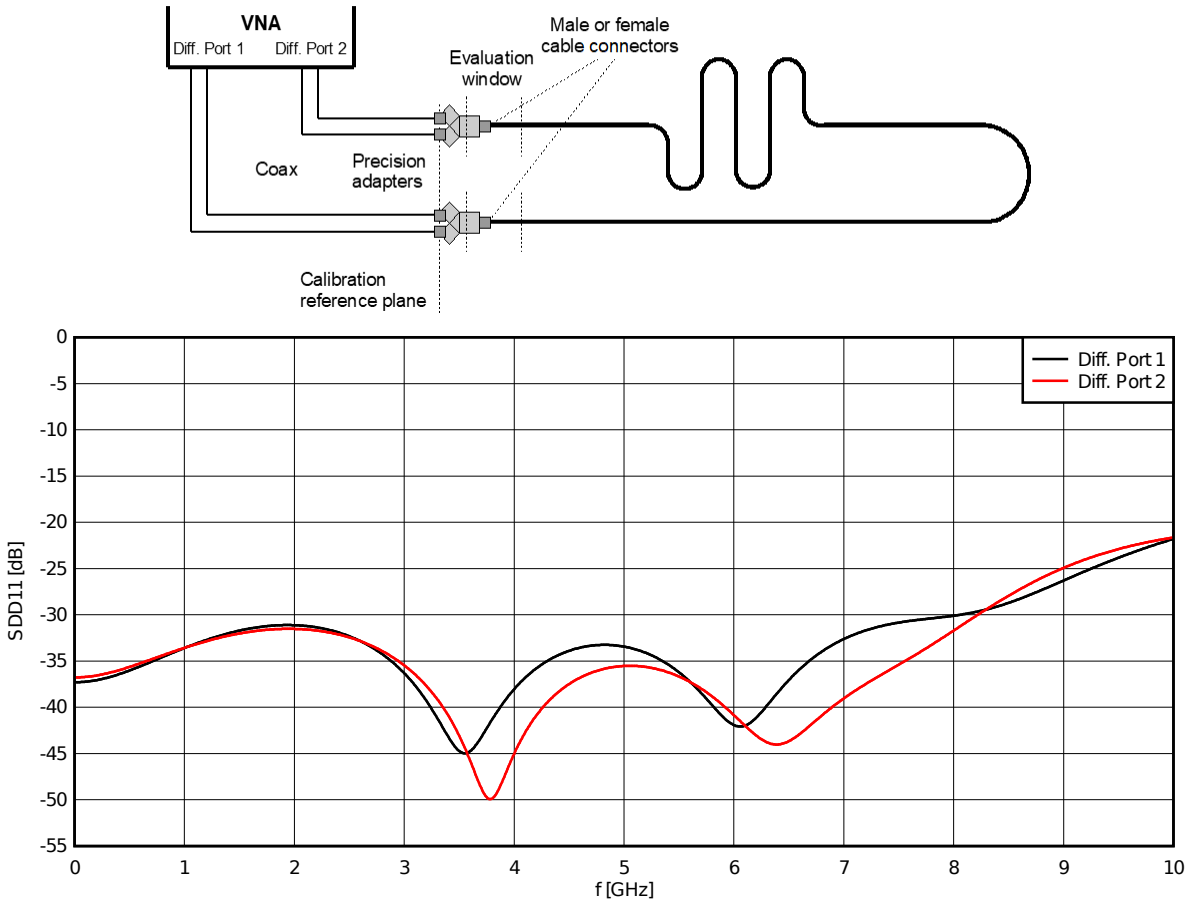

Figure 2-4. Gated Return Loss of the H-MTD® Connectors on Both Ends of the Cable Assembly

H-MTD® cable assemblies from Rosenberger come with the new GG 2Speed® 251 cabling solution as a standard. This combination covers a large landscape of protocols that already includes 100/1000BASE-T1 Ethernet, 2/5/10GBASE-T1 Ethernet, FPD-Link, and other next-generation SerDes. Given this versatility, the GG 2Speed® 251 cable and H-MTD® connector system can readily be used for future automotive PCIe systems as well.

2.5 Key Signal Conditioning Considerations

Redrivers and retimers are needed to recover and counteract the additional insertion loss and signal-to-noise ratio degradation that naturally occur when transporting PCIe over lossy media. Both redrivers and retimers have a deep-rooted history in the PCIe ecosystem. Redrivers have been a part of the PCI-SIG Integrator's List of approved components since PCIe 2.0. Meanwhile, retimers formally became part of the PCIe Base Specification since PCIe 4.0. As a semiconductor leader in signal conditioning technology, TI offers the industry's largest portfolio of PCIe redrivers, retimers, and passive switches to address a multitude of industrial and automotive use cases.

Table 2-2. Linear Redriver vs. Retimer Comparison

PCIe Linear Redriver (1)	PCIe Retimer
Low power consumption solution (no heat sink is required)	High power consumption solution (most cases require heat sink)
Ultra-low latency (100 ps)	Medium latency (less than or equal to 64 ns based on PCIe 4.0 Specification Requirement)
Does not participate in link training but is transparent to negotiations between Root Complex (CPU) and Endpoint (EP) (Protocol agnostic)	Fully participates in link training with Root Complex (CPU) and Endpoint (EP) (Protocol aware)
No 100-MHz reference clock is required	100-MHz reference clock is required

Table 2-2. Linear Redriver vs. Retimer Comparison (continued)

PCIe Linear Redriver (1)	PCIe Retimer
Helps with insertion loss	Helps with insertion loss, jitter, crosstalk, reflections and lane-to-lane skew
CTLE is the typical equalization circuit used	CTLE, DFE and transmitter FIR are typical equalization circuits used
Total solution cost is ~X	Total solution cost is ~(1.3X - 1.5X)

(1) For additional comparison details, refer to the technical article Signal Conditioning functions go mainstream in PCI Express Gen 4.

For intra-ECU and short cable reach applications, linear redrivers are a suitable fit. For native PCIe 3.0 transport, TI redrivers are targeting applications up to 5 m using GG 2Speed® 251 STP cable over Rosenberger H-MTD® connector system.

For longer cable reach applications, retimers are essential to maximize signal margin. PCIe retimers offer more complex capabilities, including adaptive EQ, DFE, and CDR compared to the redriver. Retimers also offer multiple link-monitoring diagnostic features to assist in system-level functional safety, including RX link margining, internal eye monitor, and cable fault detection. For native PCIe 3.0 transport, TI retimers are targeting applications up to 10 m using GG 2Speed® 251 STP cable over Rosenberger H-MTD® connector system.

Figure 2-5 illustrates target use cases for PCIe redrivers and retimers based on the expected total channel insertion loss. The following assumptions are used to estimate the maximum target cable length.

- PCIe specification insertion loss Rx limit for PCIe 3.0: 22 dB @ 4 GHz
- At 4 GHz, assume the following insertion loss (IL) characteristics in the link channel:
  - IL_{cable_m} = GG 2Speed® 251 STP cable: 2.75 dB/m
  - IL_{PCB} = FR4 PCB trace: 4 dB for 6" (152.4 mm)
  - IL_{conn} = Connector and Additional PCB Components: 1.5 dB
- Estimated maximum cable length (m) = (IL_{Total} - 2 x IL_{PCB} - 2 x IL_{conn}) / IL_{cable_m}

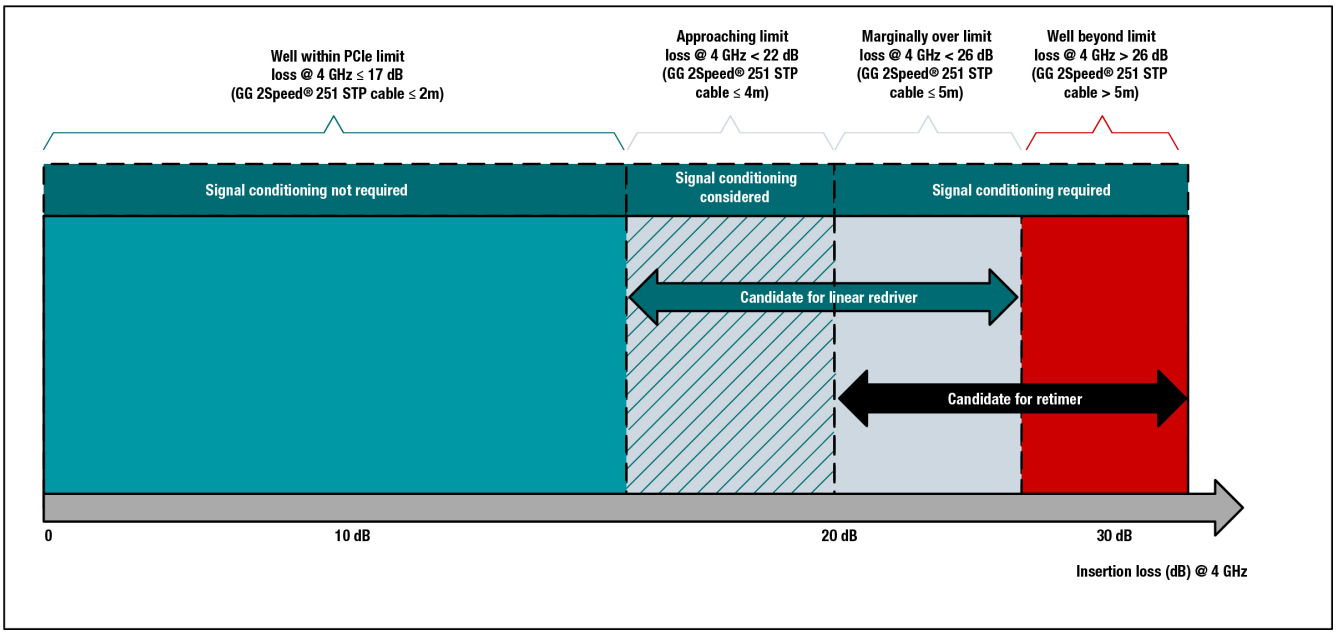

Figure 2-5. Target Use Cases for Signal Conditioning in PCIe Automotive Cable Applications

3 Conclusion

PCIe is an attractive interface for addressing critical high-bandwidth and ultra-low latency computing demands by next-generation distributed automotive architectures. For processors to take full advantage of the PCIe interface for shared processing, an automotive cabling interconnect has been defined in this paper to transform PCIe from an *intra*-ECU interface to becoming an *inter*-ECU interface. Leading automotive industry vendors such as TI, Rosenberger, and GG Group, have been developing innovative solutions to enable native PCIe transport over automotive cable channels based on H-MTD® connectors and GG 2Speed® cables. Together, these physical layer solutions will clear the path for automotive processors to realize their full computing, efficiency, and connectivity potential.

4 Key Contributors

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