

***It's a Buck; It's a Boost, No! It's a Switcher! (part three)***



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# Technology Edge

*Courtesy of PlanetAnalog/CMP Media*

## It's a Buck; It's a Boost, No! It's a Switcher! (part three)

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In previous parts of this series, we saw all the various possibilities using a Type 1 (Flyback/Boost) IC. We saw that the natural LSD cell for this IC happens to be the Type B cell corresponding to the primary intended application of this IC. The other possible LSD cell, Type A, is considered an unnatural or 'forced' choice for this IC. But because of the fact that in this IC the input to the power stage (SW pin) is separated from the input to the control, the IC becomes more versatile, allowing the IC to be floated on the switching node. And this is what ultimately makes it possible for it to handle a forced cell choice too (and all the corresponding topologies/configurations). Though we saw that in the process output regulation and EMI are likely to suffer for such 'forced' applications.

Coming to Buck ICs, hereby called Type 2 ICs, we see that the Drain/Collector of the switch is usually connected to the input to the control sections. Therefore the versatility of Type 1 ICs in handling 'forced' choices is lost. This IC cannot handle any configurations other than its natural LSD cell. The cell structure suited to this IC is the Type A LSD cell which happens to be the cell in a positive to positive Buck configuration, for which this IC is primarily designed.

### Buck IC Applications

This Type 2 IC shown as can be used for all the applications shown in this section. View the figures presented here along with the description and comments in Table 4. Note that for convenience, in all cases the main design equations are also provided within the figures themselves. They provide the required ratings of the IC/control pin ( $V_{ICmax}$ ) (measured with respect to the IC ground pin), and the maximum load possible (based on the set current limit of the switch 'ICLIM'). The maximum load current requires choosing inductance correctly. A current ripple ratio factor 'r' of 0.4 or less must be the target. Refer to [AN-1197](#) and [AN-1246](#) at <http://power.national.com> for more details.

Some of the configuration conditions may depend on the minimum input and/or maximum input voltages,  $V_{inmin}$  and  $V_{inmax}$  respectively. In addition, every controller has a maximum duty cycle limit 'Dmax'. Clearly, if the input and output voltages demand more than 'Dmax' the circuit cannot work. Therefore the equation to check this possible limitation is also provided. The feedback scheme is also shown, and the equations to set the resistor values are also provided. 'Vfb' is the voltage on the feedback pin of the IC under regulation (for example it is the reference voltage to the internal error amplifier for an Adjustable output part).

In all the equations presented, the switch and diode forward drops are generally assumed to be negligible. A little additional guardbanding may therefore be necessary to take these into account.

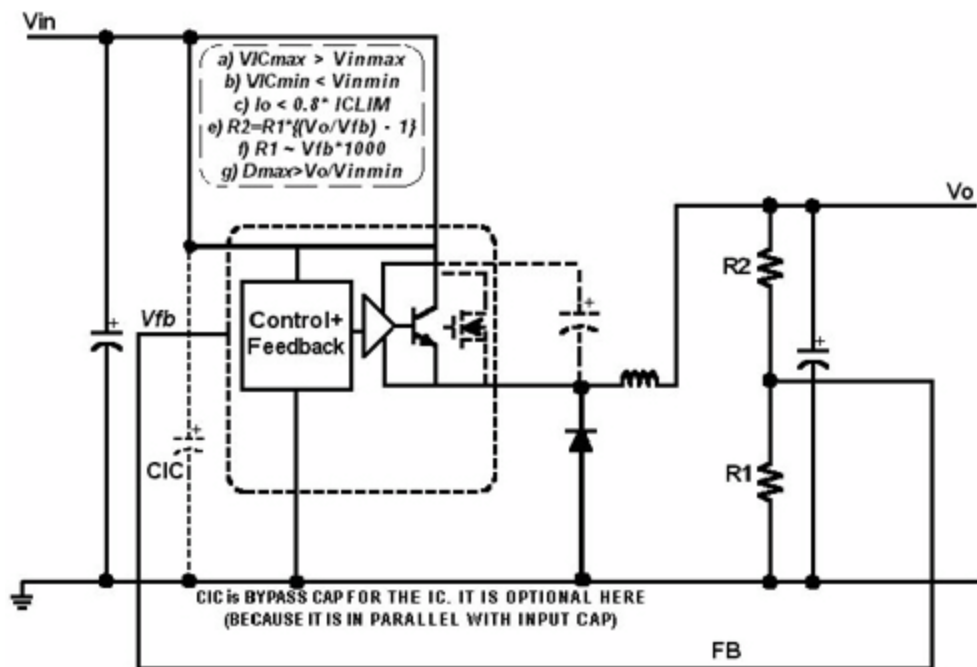
The primary intended application for this IC is the positive to positive Buck. This involves a 'N+' cell (Type A). Therefore this IC is most 'comfortable' with any topology/configuration, provided it involves a Type A cell. This cell is considered a 'natural choice' for the IC here. Note that we again see the advantage in talking in terms of LSD cells rather than directly in terms of topologies/configurations. This common thread would have been missed in that case.

The only other possible cell choice using an N-switch is the Type B (N-) cell. Topologies/configurations requiring a Type B cell are therefore considered a 'forced' choice for a Type 2 IC. But in fact a Type 2 IC cannot implement the forced choices, because the inputs to the power section and the control section are not separated out as in Type 1 ICs.

The possibilities for Type 2 (Buck) ICs are limited to the following natural LSD cell choice applications:

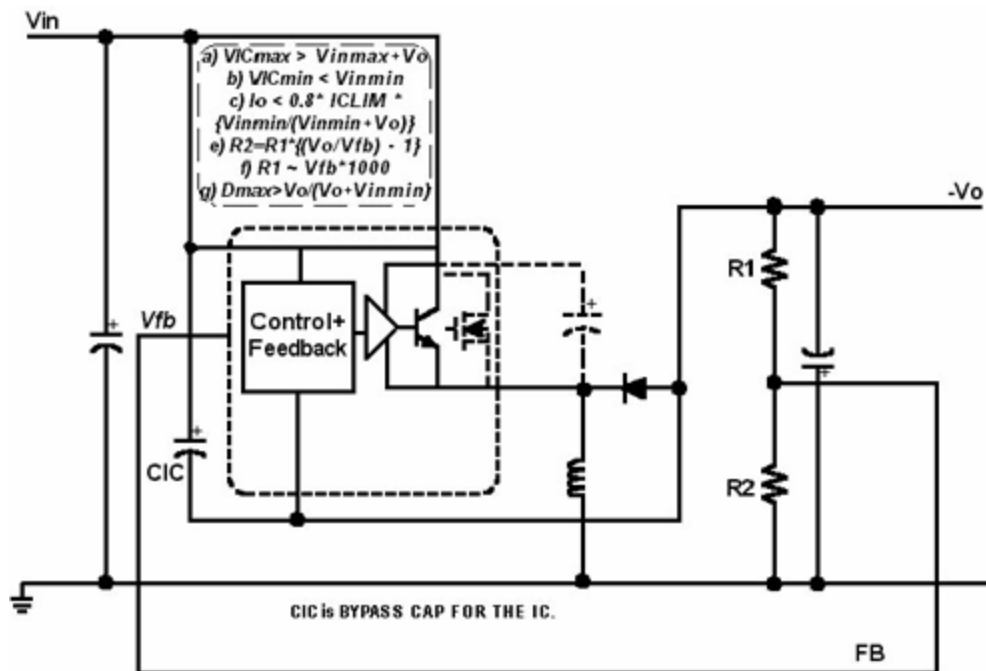
- a) Positive to Positive Buck: Uses a Type A cell. The primary intended Application for a Type 2 IC. See [Figure 19](#). Uses a simple resistive divider to implement feedback.
- b) Positive to Negative Buck-Boost: Uses a Type A cell. See [Figure 20](#). Uses a simple resistive divider to implement feedback. Additional IC bypass capacitor required.
- c) Negative to Negative Boost: Uses a Type A cell. See [Figure 21](#). Uses a simple resistive divider to implement feedback. Additional IC bypass capacitor required.

[Figure 22](#) summarizes these possibilities. The P-switches are grayed out as it was indicated earlier how they can be derived, and we are not discussing them in this article. The configurations with the natural N-switch LSD cell choice (Type A) are shown with bold arrows and yellow highlighting. Note that 'forced' choices are not indicated in [Figure 22](#) as possibilities.



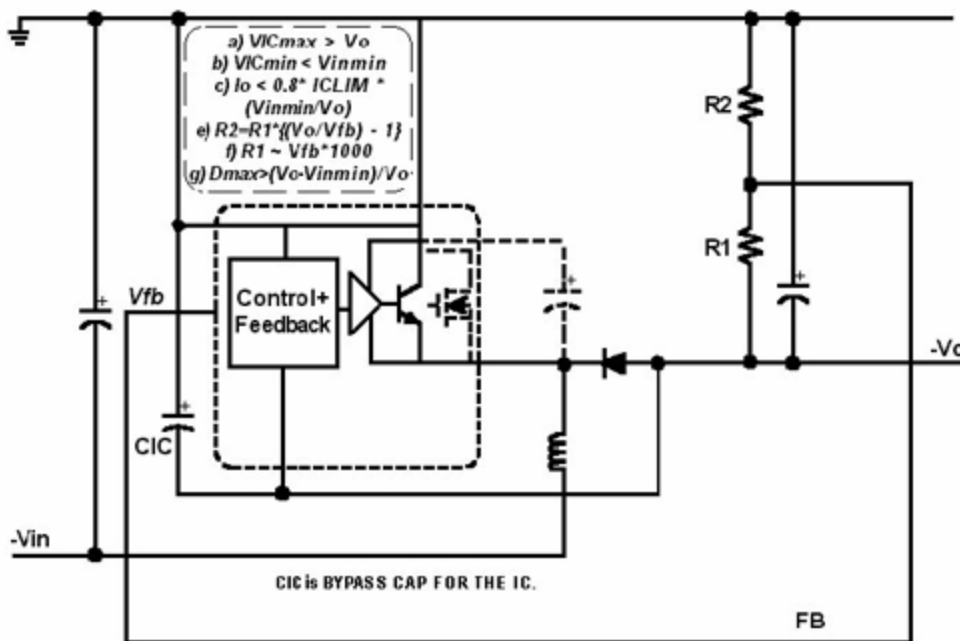
Positive to Positive Buck  
using a Buck (Type 2) IC

FIGURE 19



Positive to Negative Buck-Boost  
using a Buck (Type 2) IC

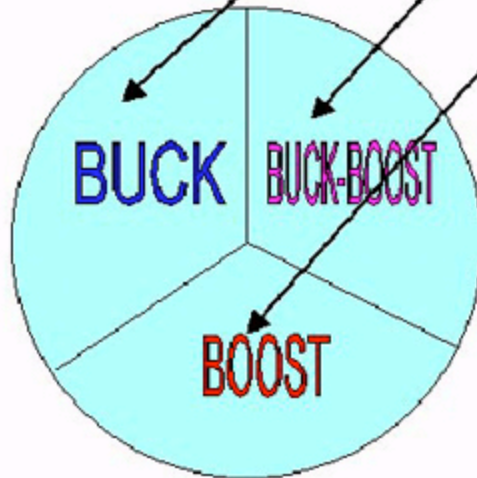
FIGURE 20



Negative to Negative Boost  
using a Buck (Type 2) IC

FIGURE 21

BUCK	Positive to Positive	(N-switch)	Type A	Fig. 19
	Negative to Negative	(N-switch)	Type B	
	Positive to Positive	(P-switch)	Type D	
	Negative to Negative	(P-switch)	Type C	
BUCK-BOOST	Positive to Negative	(N-switch)	Type A	Fig. 20
	Negative to Positive	(N-switch)	Type B	
	Positive to Negative	(P-switch)	Type D	
	Negative to Positive	(P-switch)	Type C	
BOOST	Negative to Negative	(N-switch)	Type A	Fig. 21
	Positive to Positive	(N-switch)	Type B	
	Negative to Negative	(P-switch)	Type D	
	Positive to Positive	(P-switch)	Type C	



**BOLD ARROWS:**  
 'Natural' Choice (Ground of  
 IC is NOT swinging,  
 feedback method direct)

**TYPE 2 APPLICATIONS**

***FIGURE 22***

Table 3: With Inductor

<b>BUCK</b>	Positive to Positive	Type 1	Figure Fig 15	Equation Set 1 $V_{sw\ max} \geq V_{in\ max}$ $V_{IC\ max} \geq V_{in\ max}$ $V_{IC\ min} \leq V_{in\ min}$	Equation Set 2 $I_o \leq 0.8 \cdot ICLIM$ $R2 \approx R1 \cdot \left[ \frac{V_o}{V_{fb}} - 1 \right]$ $D_{max} \geq \frac{V_o}{V_{in\ min}}$
		Type 2	Figure Fig 19	$V_{IC\ max} \geq V_{in\ max}$ $V_{IC\ min} \leq V_{in\ min}$	$I_o \leq 0.8 \cdot ICLIM$ $R2 = R1 \cdot \left[ \frac{V_o}{V_{fb}} - 1 \right]$ $D_{max} \geq \frac{V_o}{V_{in\ min}}$
	Negative to Negative	Type 1	Figure Fig 12 **	$V_{sw\ max} \geq V_{in\ max}$ $V_{IC\ max} \geq V_{in\ max}$ $V_{IC\ min} \leq V_{in\ min}$	$I_o \leq 0.8 \cdot ICLIM$ $R2 \approx R1 \cdot \left[ \frac{V_o - 0.6}{V_{fb}} - 1 \right]$ $D_{max} \geq \frac{V_o}{V_{in\ min}}$
		Type 2	X		
<b>BOOST</b>	Positive to Positive	Type 1	Figure Fig 10	$V_{sw\ max} \geq V_o$ $V_{IC\ max} \geq V_{in\ max}$ $V_{IC\ min} \leq V_{in\ min}$	$I_o \leq 0.8 \cdot ICLIM \cdot \frac{V_{in\ min}}{V_o}$ $R2 = R1 \cdot \left[ \frac{V_o}{V_{fb}} - 1 \right]$ $D_{max} \geq \frac{V_o - V_{in\ min}}{V_o}$
		Type 2	X		
	Negative to Negative	Type 1	Figure Fig 13	$V_{sw\ max} \geq V_o$ $V_{IC\ max} \geq V_o$ $V_{IC\ min} \leq V_{in\ min}$	$I_o \leq 0.8 \cdot ICLIM \cdot \frac{V_{in\ min}}{V_o}$ $R2 \approx R1 \cdot \left[ \frac{V_o}{V_{fb}} - 1 \right]$ $D_{max} \geq \frac{V_o - V_{in\ min}}{V_o}$
Type 2		Figure Fig 21	$V_{IC\ max} \geq V_o$ $V_{IC\ min} \leq V_{in\ min}$	$I_o \leq 0.8 \cdot ICLIM \cdot \frac{V_{in\ min}}{V_o}$ $R2 = R1 \cdot \left[ \frac{V_o}{V_{fb}} - 1 \right]$ $D_{max} \geq \frac{V_o - V_{in\ min}}{V_o}$	

<b>BUCK-BOOST</b>	Positive to Negative	Type 1	Fig 14	$V_{sw\ max} \geq V_{in\ max} + V_o$ $V_{IC\ max} \geq V_{in\ max} + V_o$ $V_{IC\ min} \leq V_{in\ min}$	$I_o \leq 0.8 \cdot I_{CLIM} \cdot \frac{V_{in\ min}}{V_{in\ min} + V_o}$ $R2 = R1 \cdot \left[ \frac{V_o}{V_{fb}} - 1 \right]$ $D_{max} \geq \frac{V_o}{V_{in\ min} + V_o}$
		Type 2	Fig 20	$V_{IC\ max} \geq V_{in\ max} + V_o$ $V_{IC\ min} \leq V_{in\ min}$	$I_o \leq 0.8 \cdot I_{CLIM} \cdot \frac{V_{in\ min}}{V_{in\ min} + V_o}$ $R2 = R1 \cdot \left[ \frac{V_o}{V_{fb}} - 1 \right]$ $D_{max} \geq \frac{V_o}{V_{in\ min} + V_o}$
	Negative to Positive	Type 1	Fig 11 **	$V_{sw\ max} \geq V_{in\ max} + V_o$ $V_{IC\ max} \geq V_{in\ max}$ $V_{IC\ min} \leq V_{in\ min}$	$I_o \leq 0.8 \cdot I_{CLIM} \cdot \frac{V_{in\ min}}{V_{in\ min} + V_o}$ $R2 \approx R1 \cdot \left[ \frac{V_o - 0.6}{V_{fb}} - 1 \right]$ $D_{max} \geq \frac{V_o}{V_{in\ min} + V_o}$
		Type 2	X		

Table 4: With Transformer

<b>BUCK-BOOST</b>	Positive to Positive	Type 1	Fig 16	$V_{sw\ max} \geq V_{in\ max} + V_z$ $V_{IC\ max} \geq V_{in\ max}$ $V_{IC\ min} \leq V_{in\ min}$ $n = N_p / N_s$ $V_r = V_o \cdot n$ $V_z > V_r$	$I_o \leq [0.8 \cdot I_{CLIM} \cdot \frac{V_{in\ min}}{V_{in\ min} + V_r}] \cdot n$ $R2 = R1 \cdot \left[ \frac{V_o}{V_{fb}} - 1 \right]$ $D_{max} \geq \frac{V_r}{V_{in\ min} + V_r}$
		<b>FLYBACK</b>	Type 1	Fig 17***	$V_{sw\ max} \geq V_{in\ max} + V_z$ $V_{IC\ max} \geq V_{in\ max}$ $V_{IC\ min} \leq V_{in\ min}$ $n = N_p / N_s$ $V_r = V_o \cdot n$ $V_z > V_r$

Note: By convention, R2 is always connected to the higher voltage rail of output and R1 to the lower.

\* Type 1 IC is a 'Boost/Buck-Boost/Flyback IC'. Type 2 IC is a 'Buck IC'.

\*\* For Figure 11 and 12, more accurate differential amplifier sensing can be used: see Table 3.

\*\*\* Vfb is NOT the voltage on feedback pin of IC in Figure 17. Also, set zener voltage Vz significantly higher than Vr (typically 20-30% higher) to minimize losses in zener and to maximize efficiency.

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Next issue - [Part 4: It's A Switcher](#)

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