CMOS will reign in 2020

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About the author

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It's clear that consumers want access to digital voice and video services without restriction. Even the 40-somethings are sharing YouTube clips over coffee and at dinner parties. The younger generations, who have grown up with wireless access and downloadable content, will most certainly continue to stretch the limits of technology. Without question, computing and communication will reach everywhere as soon as technology can make it possible.

The year 2020 is not so far away, but ITRS (International Technology Roadmap for Semiconductors) projections of advances in process technology suggest that bulk CMOS will still be the mainstream technology of choice for a number of key reasons. Specifically, Moore's law will continue to hold, leading to several significant trends over the next 12 years:

- Assuming chip size at production of high-performance SoCs remains constant at 246 mm^2 through 2020, the number of functions per chip is expected to increase as transistor count jumps from 1.1 billion transistors in 2008 to 17.696 billion transistors in 2020
- DRAM cost/bit at production, measured in packaged microcents, will drop from 0.68 in 2008 to 0.01 by 2020
- Cost-performance of MPUs at production (including on-chip SRAM) will decrease from 9.4 microcents per transistor in 2008 to only 0.15 in 2020

Together, these trends predict that processing performance will be not only be cheap, it will be cheaper with the typical system-on-chip (SoC) architecture comprised of billions of transistors. Such capacity will increase functional integration, and systems will drive much harder circuits and devices. Power will, of course, become a major design concern for both chip- and system-level design.

However, increases in available processing potential also increases system complexity. Therefore, it will be critical for silicon manufacturers like TI to design efficient data flow within their architectures to ensure that instructions and data are in the right place at the right time with the lowest possible overhead. The key to enabling optimal performance will be to focus on adaptive, fault-tolerant and distributed computing.

Ease-of-use and time-to-market will continue to dictate hardware architectures, and one of the most important factors affecting design will be the trade-off of increased hardware complexity for software simplification. Despite design platform and programming methodology advances, software investment will continue to scale at a faster rate than hardware. Since software will be the key differentiator for OEMs, managing, leveraging and protecting software investment will be their biggest care about.

As a consequence, OEMs will not abide complex development paradigms that lock software to a particular platform. To stay successful, silicon manufacturers will need to do everything they can in hardware to ease design and speed time-to-market while ensuring the longevity and viability of customer application software.

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