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### About the author

Alan Gatherer is the CTO for the Communications Infrastructure Group at TI and is responsible for all strategic development of TI's digital baseband modems for 3G wireless infrastructure. Since joining TI in 1993, he has worked on various digital modem technologies including cable modem, ADSL and 3G handset and basestation modems. In addition, he holds 33 patents and is author of the book "The Application of Programmable DSPs in Mobile Communications."

Predicting the future is primarily an act of the imagination. However, accurately forecasting when it might actually be possible to produce a cost-effective model that matches that vision requires following and understanding the different evolutionary stages processors will pass through.

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## From 2008 to 2020: A history of developments in programmability

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Here are my thoughts on the next 12 years.

- **2008: Multi-core is here.** With the increase in SoC architectures, single-core CPU devices have become more the exception than the rule.
- **2010: Network-on-Chip (NoC) arrives.** A NoC is a high-performance device, which is really a grouping of processing islands connected by packet-based, point-to-point asynchronous communication highways.
- **2010–2015: Component-based software.** The number of cores on a device is still fairly modest, and individual software components are developed for a single computational cluster by "component developers" and then "assembled" onto a multi-core system. Development tools for this methodology improve steadily as virtualization of hardware through middleware is driven by efforts such as the SCA (Software Communications Architecture) for SDR (software-defined radio). Auto generation of glue code between components is the norm.
- **2010–2015: Single Program Multiple Data (SPMD).** The component-based approach begins to fail as the number of cores reaches 32. Turning to techniques used in high-performance computing (HPC), the embedded software community develops the SPMD approach where a program can be compiled to run over multiple cores. While initially requiring explicit description of the communication flow, pragmas are now employed to enable the parallel nature of algorithms to be exploited by a variety of multi-core devices.

- **2015: The Death of the FPGA.** An important footnote in the history of programmability is the demise of the FPGA. Small multi-core CPUs consume significantly less power as well as provide a richer set of mapping options for complex algorithms and communication patterns than does the distributed fabric of ALUs and LUTs that make up FPGAs.
- **2020: The CPU disappears.** Spreading functionality across multiple CPUs drastically simplifies the silicon overhead on each CPU, and hardware-based OS support manages NoC traffic efficiently. Programmers are unaware of the communication between CPUs and can develop/debug code without having to know which individual execution units are involved. Programming follows more the overall flow of data than its individual parts.

The range of devices available in 2020 will be about the same as it is in 2008. In 2020, embedded DSPs will still be a heterogeneous combination of CPUs and accelerators. Even though programmers are unaware of the individual devices when programming, it will still stand true that some devices perform certain tasks much better than others.

Since much of the value of SoCs is placed in the careful choice of peripherals, CPU and DSP manufacturers differentiate themselves by providing the best combination of different IP blocks and how they connect. In the end, the quality of development tools and application software support will determine the first-tier players.

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