

# Ultrasonic sensing solution submodules overview



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# Introduction

The [MSP430FR604x](#) family of microcontrollers (MCUs) includes an integrated ultrasonic sensing solution (USS) subsystem typically used for ultrasonic flow-meter applications. However, the USS block consists of several submodules, including the sigma-delta high-speed (SDHS) analog-to-digital converter (ADC), the high-speed phase-locked loop (HSPLL) and programmable pulse generator (PPG) that when used together or separately can address applications beyond ultrasonic flow metering. In this white paper, we will give a basic overview of the capabilities of different USS submodules and provide some examples of how you can use them for other purposes, such as high-speed, high-accuracy data acquisition and processing, pulse generation and high-speed clock generation. **Figure 1** below shows an overview of the ultrasonic sensing subsystem module.

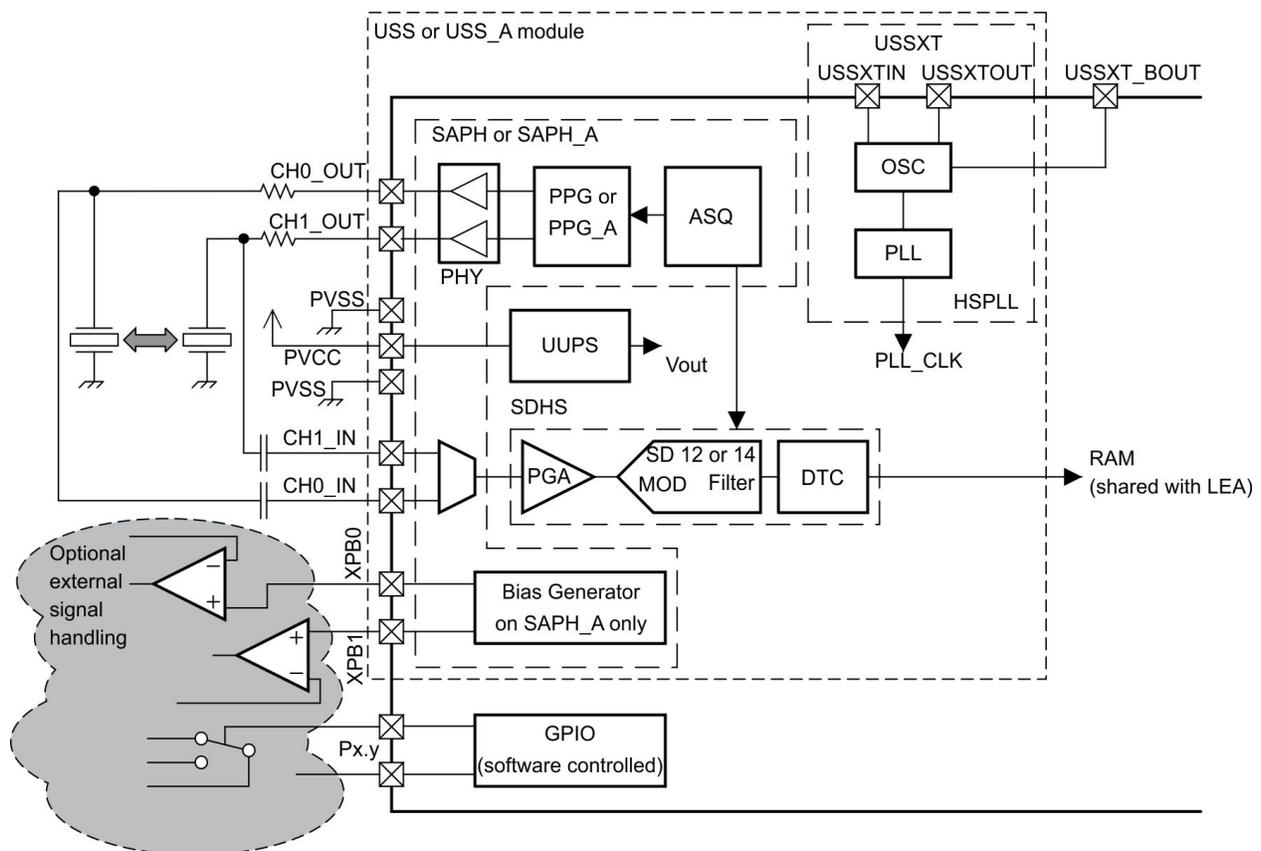


Figure 1: Ultrasonic sensing solution (USS) block diagram.

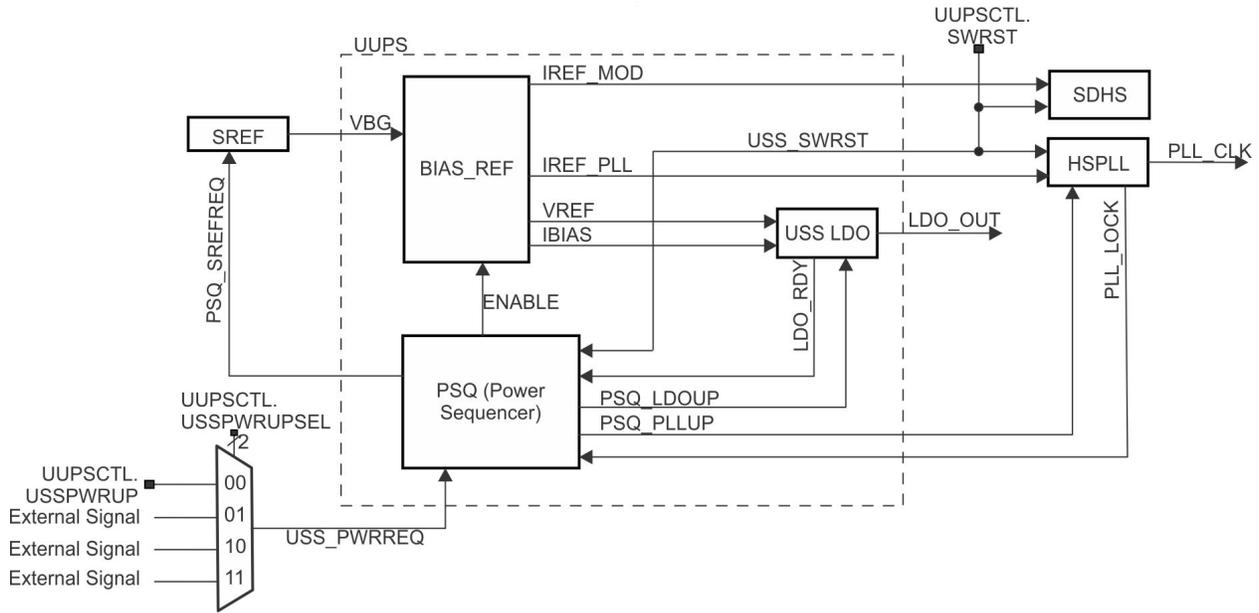


Figure 2: UUPS block diagram.

## Universal ultrasonic sensing solution power supply submodule

The universal ultrasonic sensing solution power supply (UUPS) submodule powers blocks in an ultrasonic sensing subsystem. It generates a regulated 1.6 V that the USS submodules use—therefore, most submodule functions in a USS subsystem require the power up of the UUPS, regardless of whether the USS is used for ultrasonic flow-metering applications. The UUPS also generates required reference voltages and currents for the sigma-delta high-speed (SDHS) ADC and high-speed PLL (HSPLL) submodules. **Figure 2** shows the UUPS block diagram.

## High-speed PLL submodule

The high-speed PLL (HSPLL) submodule contains the clock generation for the ultrasonic sensing solution module. A dedicated high-speed external crystal or ceramic oscillator (USSXT) of any frequency

between 4 MHz and 8 MHz drives the high-speed PLL. Using this oscillator, the high-speed PLL can generate many frequencies between 68 MHz and 80 MHz. In turn, the sampling timing for the sigma-delta high-speed ADC uses this high-speed PLL output frequency, so select this frequency accordingly. The high-speed PLL block diagram is shown in **Figure 3** below.

The USSXT frequency can also serve as an external buffered output clock on a pin, which you can then use to clock other devices in your application or to provide an external input clock to the high-speed XT2 oscillator on the MSP430™ MCU in bypass mode for use by other modules in the MSP430

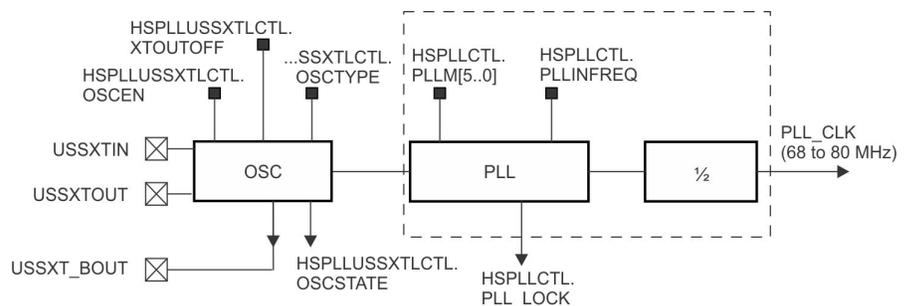


Figure 3: High-speed PLL block diagram.

device such as timers. This feature enables you to get the accuracy benefit of a high-speed crystal for other parts of your application (such as generating accurate pulse-width modulators [PWMs]) without having to add an additional high-speed crystal—you can simply reuse the USS oscillator. See the application note, “[How to Synchronize the MSP430FR6047 Clock System Domains with the Ultrasonic Sensing Oscillator](#)” for more details.

## Sigma-delta high-speed ADC submodule

The 12-bit sigma-delta high-speed (SDHS) ADC typically provides a signal-to-noise ratio (SNR) of around 63 dB up to a signal bandwidth of about 1.5 MHz. The ADC is modulated using the high-speed PLL with a frequency range from 68 MHz to 80 MHz. The output data rate can be as high as 8 MHz and supports oversampling rates (OSRs) ranging from 10 to 160. There is also a programmable gain amplifier (PGA) built into the sigma-delta high-speed ADC that allows for configurable gain on the input signal. **Figure 4** shows an overview of the sigma-delta high-speed ADC block diagram.

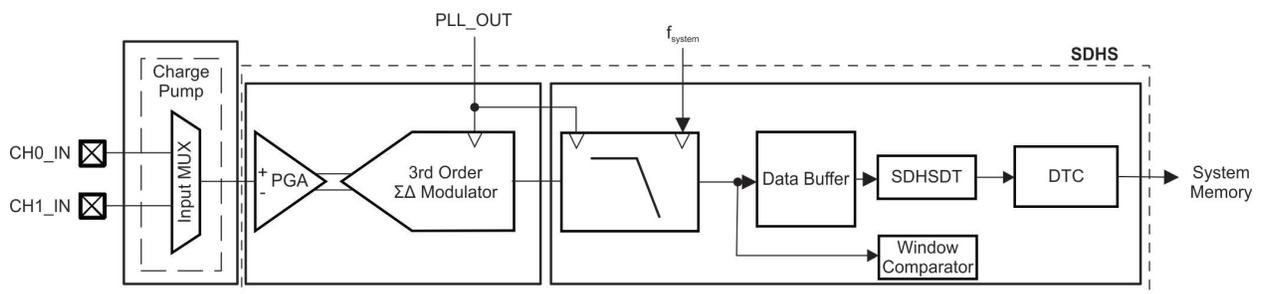
You can use the sigma-delta high-speed ADC in non-ultrasonic applications—it supports a stand-alone mode that can operate separately from other functions in the ultrasonic sensing solution module. When used in stand-alone mode, the UUPS will still have to power and generate the reference

voltage for the sigma-delta high-speed ADC. The high-speed PLL will need to provide the modulator frequency and you will need to configure the physical layer (PHY) to make the appropriate input connections and bias voltages.

The sigma-delta high-speed ADC also features a data transfer controller (DTC) that can transfer conversion results directly to the low-energy accelerator (LEA)-shared RAM without central processing unit (CPU) intervention, so that the low-energy accelerator can quickly process the data. Therefore, a sigma-delta high-speed ADC + low-energy accelerator can be a good option for a variety of applications that require fast, accurate data acquisition with some digital signal processing (DSP) performed on the results.

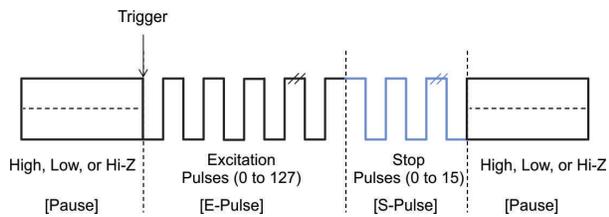
## Programmable pulse generator submodule

The Programmable pulse generator (PPG) generates excitation pulses, which in ultrasonic applications drive the transducer. However, you could use the PPG pulses for any application that requires pulse generation. **Figure 6** on the following page shows the block diagram of the PPG within the sequencer for acquisition, programmable pulse generation, and physical interface (SAPH) module. You can program the PPG to generate anywhere from one to 127 excitation pulses at a specified frequency. It also has the ability to generate one to 15 stop pulses (with a 180-degree phase shift from the excitation pulses)



**Figure 4:** Sigma-delta high-speed ADC block diagram.

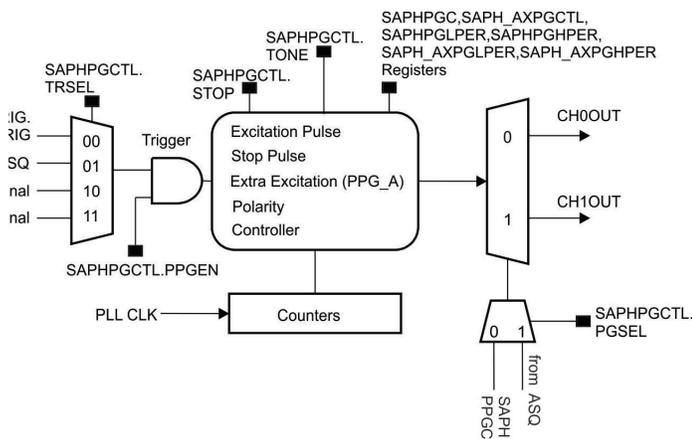
immediately succeeding the in-phase pulses. An example of PPG single-tone generation with low polarity is shown in **Figure 5** below.



**Figure 5:** PPG single-tone generation with  $SAPHPGC.PPOL = 1$  (starts with low polarity).

The PPG can generate pulses in a frequency ranging from 133 kHz to 2.5 MHz. The resolution of the frequency of the pulses depends on the frequency of the HSPLL and the high and low periods set in the module. Equation 1 for resolution is:

$$\Delta F = \frac{HSPLL\_Frequency}{high\_period+low\_period} - \frac{HSPLL\_Frequency}{high\_period+1+low\_period} \quad (1)$$



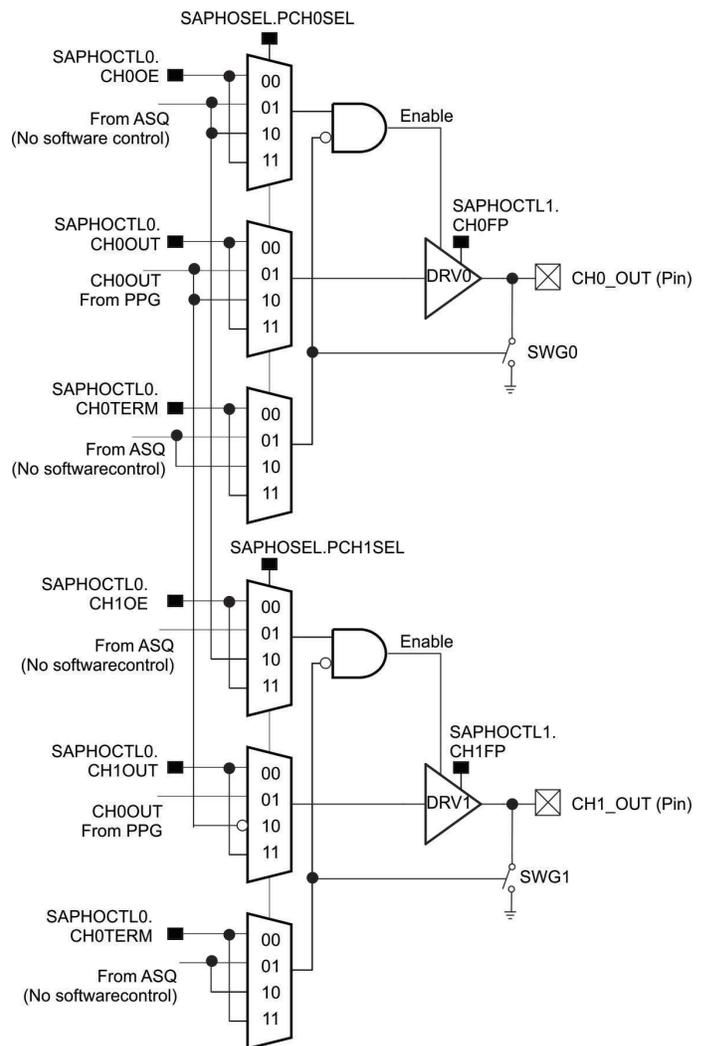
**Figure 6:** PPG block diagram.

## PHY driver and impedance matching

The PHY has the ability to control a two-channel transducer input and output. It contains a single driver and receive path shared between the transducer pair. The PHY also includes a multiplexer

that controls switching of the driver from channel 1 to channel 2 while simultaneously switching the receive path from channel 2 to channel 1. It includes drivers with impedance as low as  $4 \Omega$  that can drive up to 120 mA of current. This enables direct interfacing of the transducers with the device, without any external analog components other than a termination resistor and capacitor. The PHY output pin muxing is shown in **Figure 7**.

Because a flow-meter application includes upstream and downstream firing across two different transducers, it is important to match the electronics impedance that the transducers see across the two paths. The ultrasonic sensing module



**Figure 7:** PHY output pins.

device-specific trim capability that enables matching across the two channels. This trimming is part of the manufacturing process by the automated test equipment (ATE).

Although the PHY is typically most important for flow-metering applications, you can also use it with the SDHS ADC in stand-alone mode to configure the inputs provided to the ADC. Additionally, you should configure the PHY if you are using the PPG in stand-alone mode in order to control the output pins for pulse generation.

### Acquisition sequencer submodule

The acquisition sequencer (ASQ) shown in **Figure 8** controls the measurement sequence and specific instances when each of the modules activates. Once programmed, sequencing occurs independent of the CPU, enabling the MSP430 device to go into low-power mode. The acquisition sequencer has sufficient programmability to independently specify the start of pulse generation, enable the sigma-delta high-speed ADC, apply receive-chain biasing and start the receive signal capture by the ADC, whose outputs are stored in RAM. The acquisition sequencer is not used when modules are configured in stand-alone mode.

### Conclusion

The ultrasonic sensing solution subsystem integrated in MSP430FR604x MCUs contains a

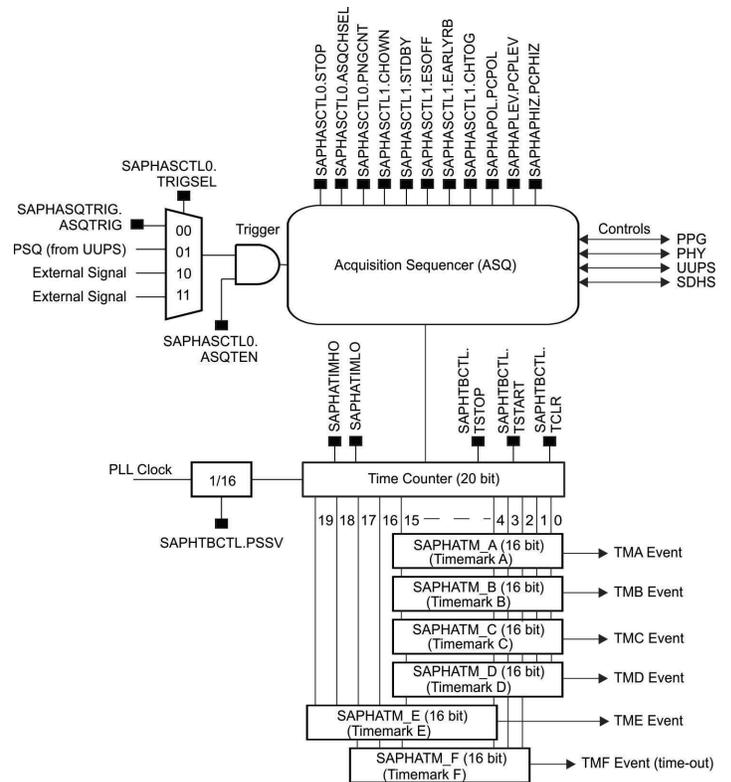


Figure 8: Acquisition sequencer block diagram.

number of advanced peripherals that you can use not only for high-performance flow metering, but to enable a number of other applications requiring high-speed, high-accuracy data acquisition and processing, pulse generation and high-speed clock generation.

For more details on the subsystem blocks of the MSP430FR604x MCUs, refer to the [user's guide](#).

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