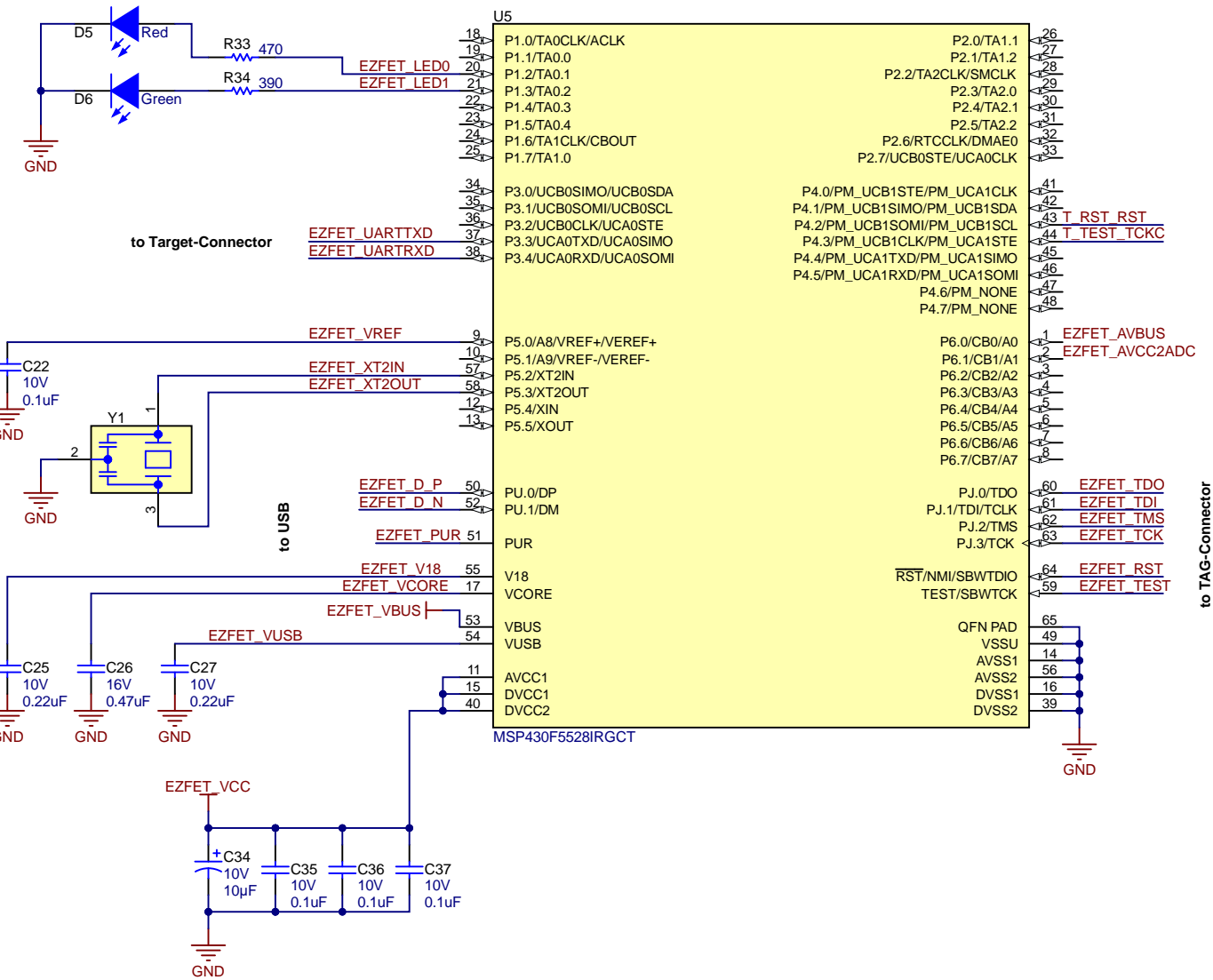


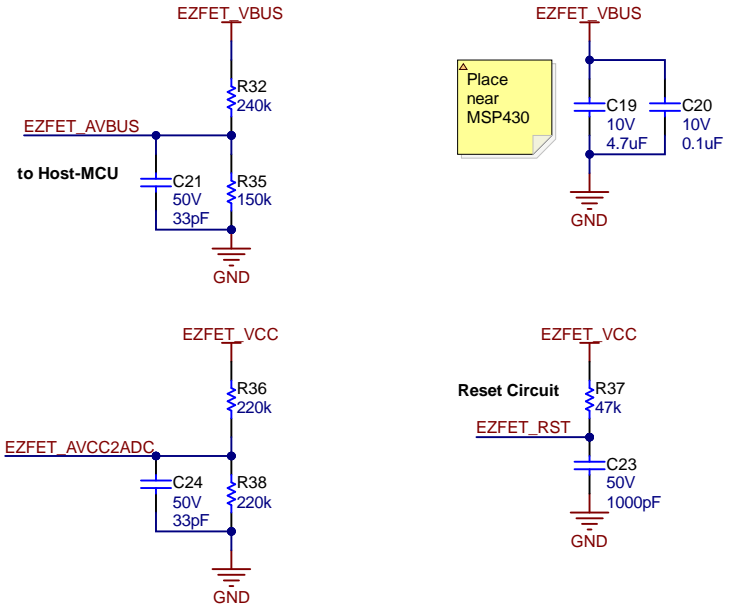
Host MCU for Emulation



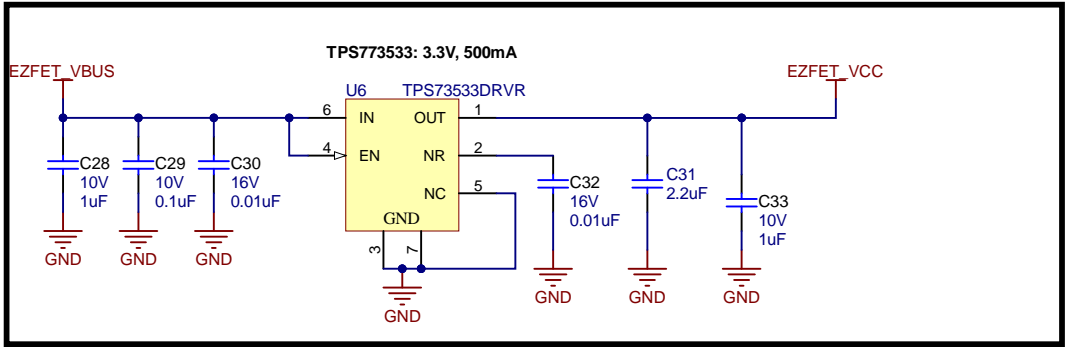
to Target-Connector

to Voltage-Divider

to TAG-Connector



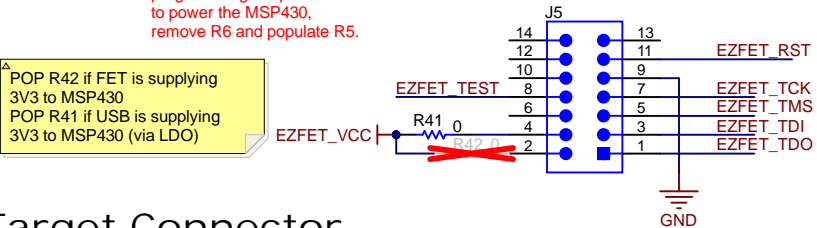
3.3V Power (EZFET_VCC)



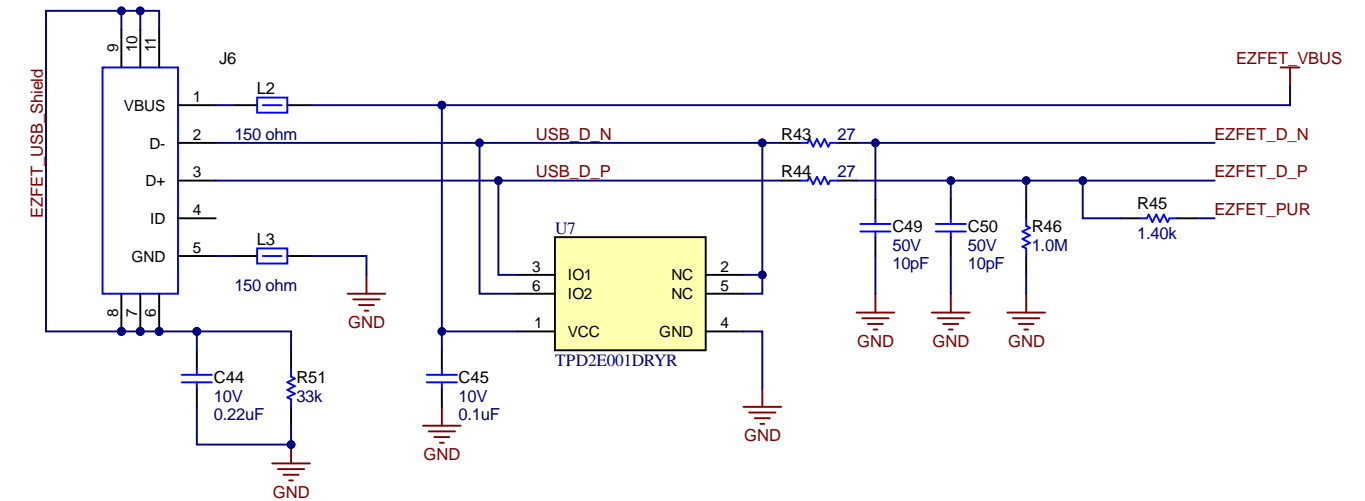
JTAG-Connector (Host Debug)

DNPed R5. If debug or programming adapter is used to power the MSP430, remove R6 and populate R5.

Host-MCU Debug Connector



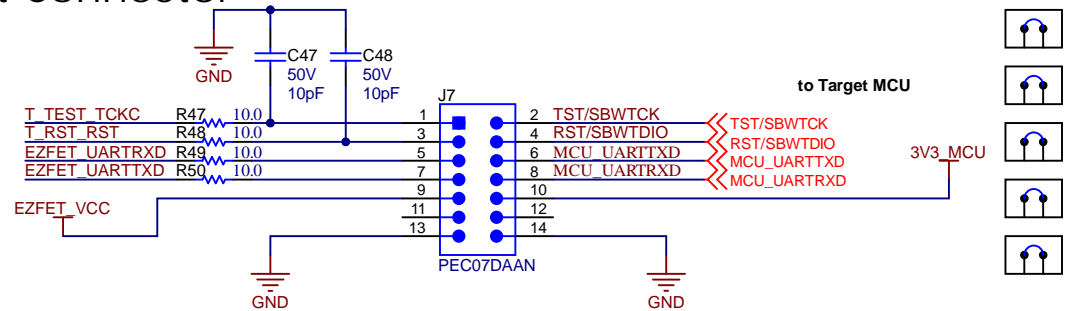
USB-I-Interface



to Host-MCU

Target Connector

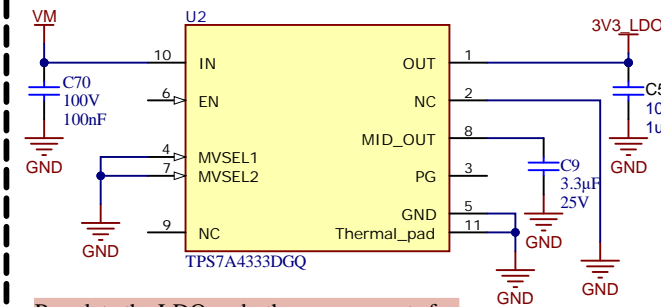
to Host-MCU
to Target
to Host-MCU



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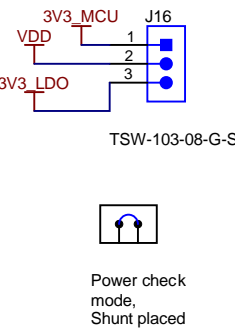
Orderable: DRV8263H-Q1EVM	Designed for: Public Release	Mod. Date: 6/20/2024
TID #: N/A	Project Title: DRV8263S/H-Q1EVM VQFN	
Number: MD093	Rev: E1	Sheet Title:
SVN Rev: Unknown revision	Assembly Variant: 002	Sheet: 1 of 3
Drawn By:	File: ezFET.SchDoc	Size: B
Engineer: Jacob Thompson	Contact: http://www.ti.com/support	© Texas Instruments 2024

3.3V LDO



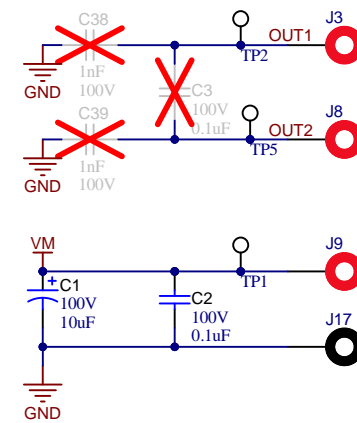
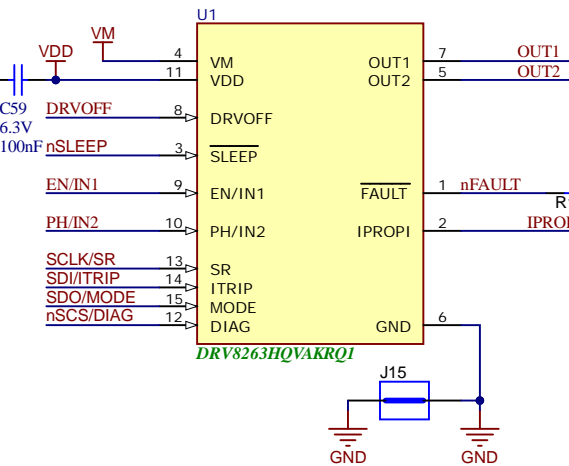
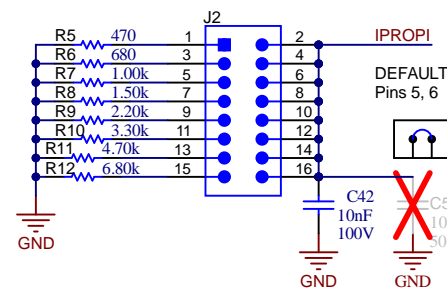
Populate the LDO and other components for prototype testing. Consider DNP it for production.

Power Check

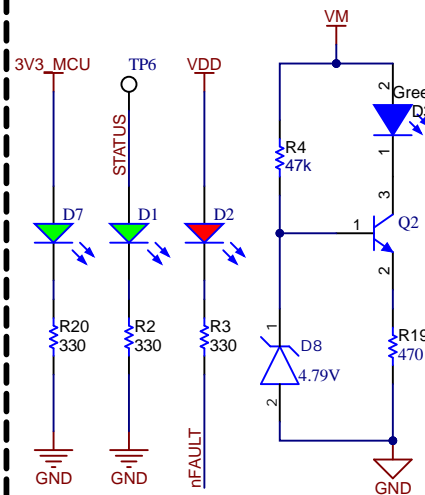


DRV8263S/H-Q1 VQFN

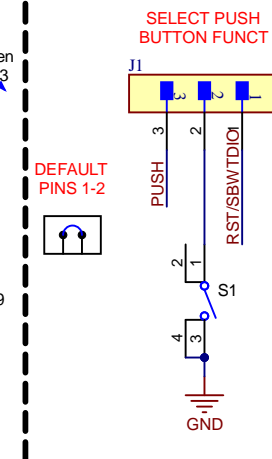
$$ITRIP = V(TRIP)/R(IPROP) * A_IPROP$$



LEDS



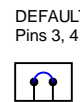
BUTTON



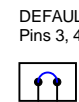
ANALOG CONTROL SIGNALS (H-variant only)

ITRIP Levels
1 0v
2 1.65v
3 1.98v
4 2.31v
5 2.64v
6 2.97v

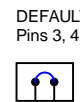
PINS	ITRIP
1, 2	LVL1
3, 4	LVL2
5, 6	LVL3
7, 8	LVL4
9, 10	LVL5
DNI	LVL6



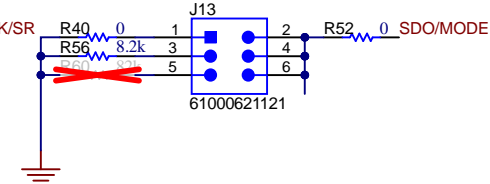
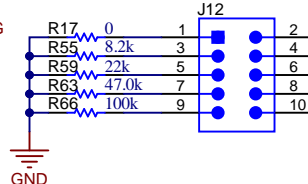
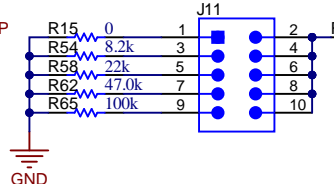
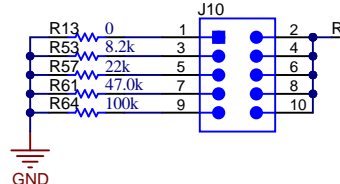
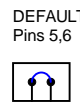
PINS	DIAG
1, 2	LVL1
3, 4	LVL2
5, 6	LVL3
7, 8	LVL4
9, 10	LVL5
DNI	LVL6



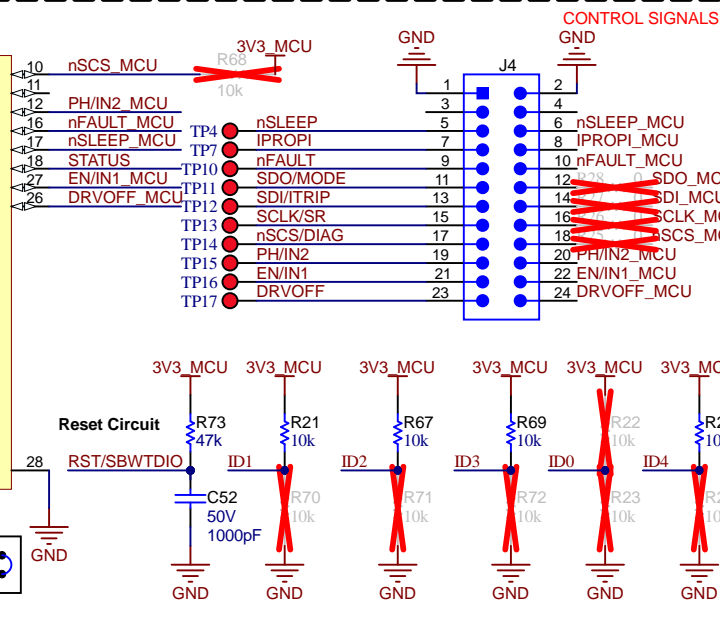
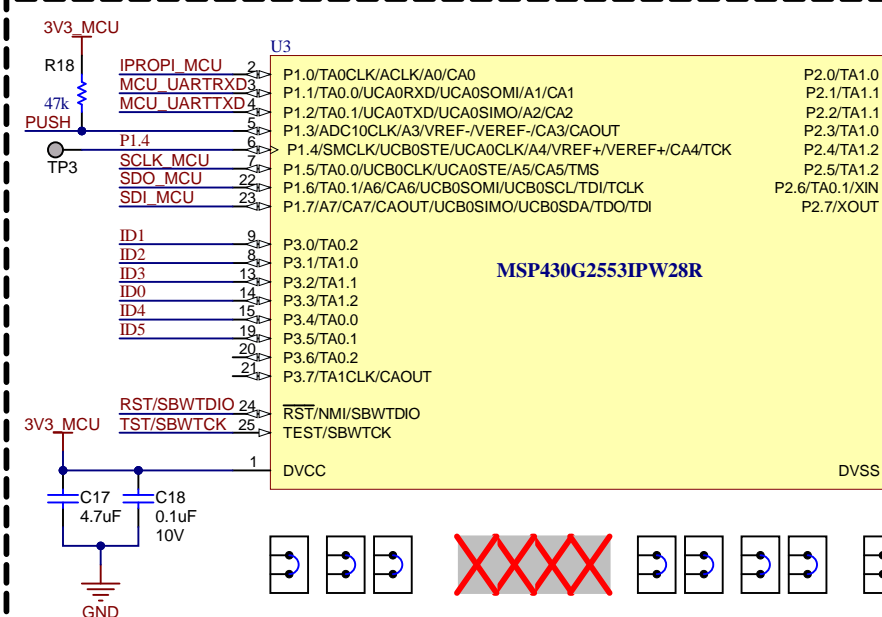
PINS	SR
1, 2	LVL1
3, 4	LVL2
5, 6	LVL3
7, 8	LVL4
9, 10	LVL5
DNI	LVL6



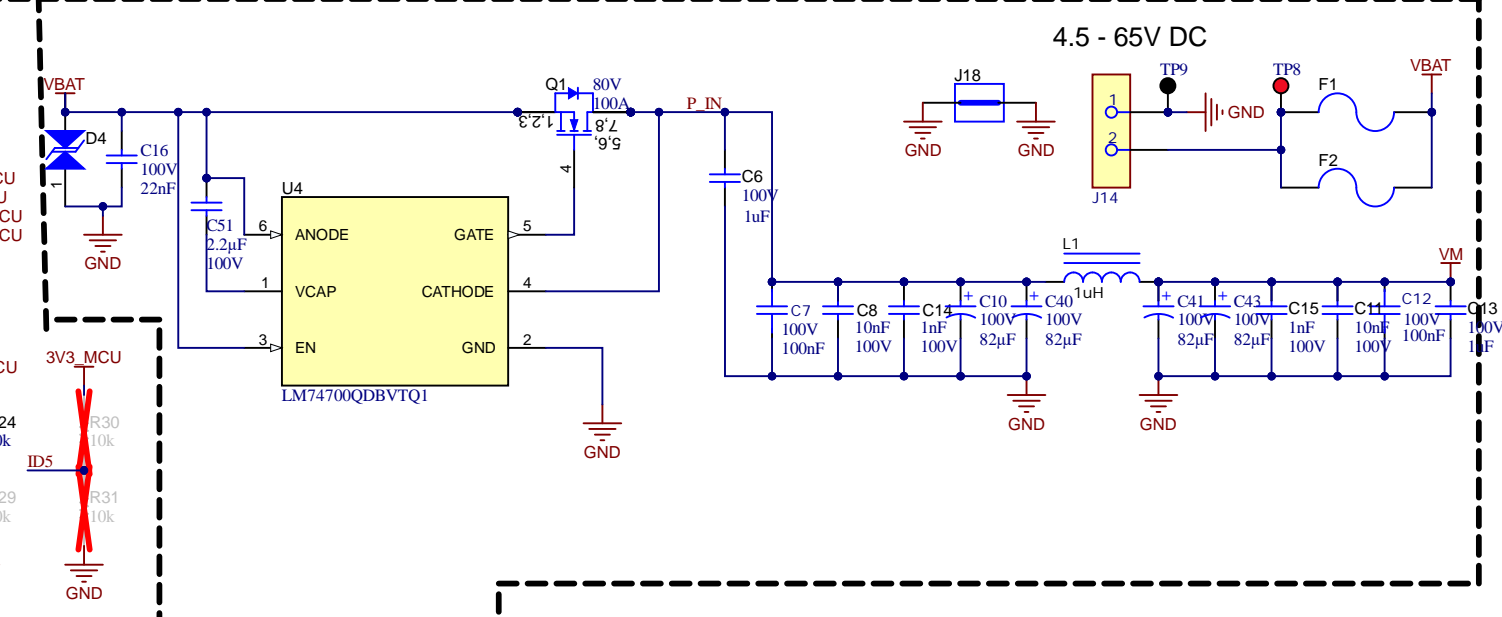
PINS	MODE
1, 2	LVL1
3, 4	LVL2
5, 6	LVL3
DNI	LVL4



MSP430



MAIN INPUT SUPPLY REVERSE PROTECTION & FILTER



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Orderable: DRV8263H-Q1EVM	Designed for: Public Release	Mod. Date: 6/26/2024
TID #: N/A	Project Title: DRV8263S/H-Q1EVM VQFN	
Number: MD093	Rev: E1	Sheet Title:
SVN Rev: Unknown revision	Assembly Variant: 002	Sheet: 2 of 3
Drawn By:	File: MD093E1_DRV8263-Q1EVM_VQFN.SchDoc	Size: B
Engineer: Jacob Thompson	Contact: http://www.ti.com/support	

H1
SJ-5303 (CLEAR)

H2
SJ-5303 (CLEAR)

H3
SJ-5303 (CLEAR)

H4
SJ-5303 (CLEAR)

FID1

FID2

FID3

PCB Number: MD093

PCB Rev: E1

PCB
LOGO

Texas Instruments



PCB
LOGO

FCC disclaimer

PCB
LOGO

WEEE logo



CAUTION HOT SURFACE

PCB
LOGO

CAUTION. READ USER GUIDE BEFORE USE

LBL1

PCB Label

THT-14-423-10

Size: 0.65" x 0.20 "

ZZ1

Label Assembly Note

This Assembly Note is for PCB labels only

ZZ2

Assembly Note

These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Variant/Label Table	
Variant	Label Text
001	DRV8243S-Q1EVM
002	DRV8243H-Q1EVM