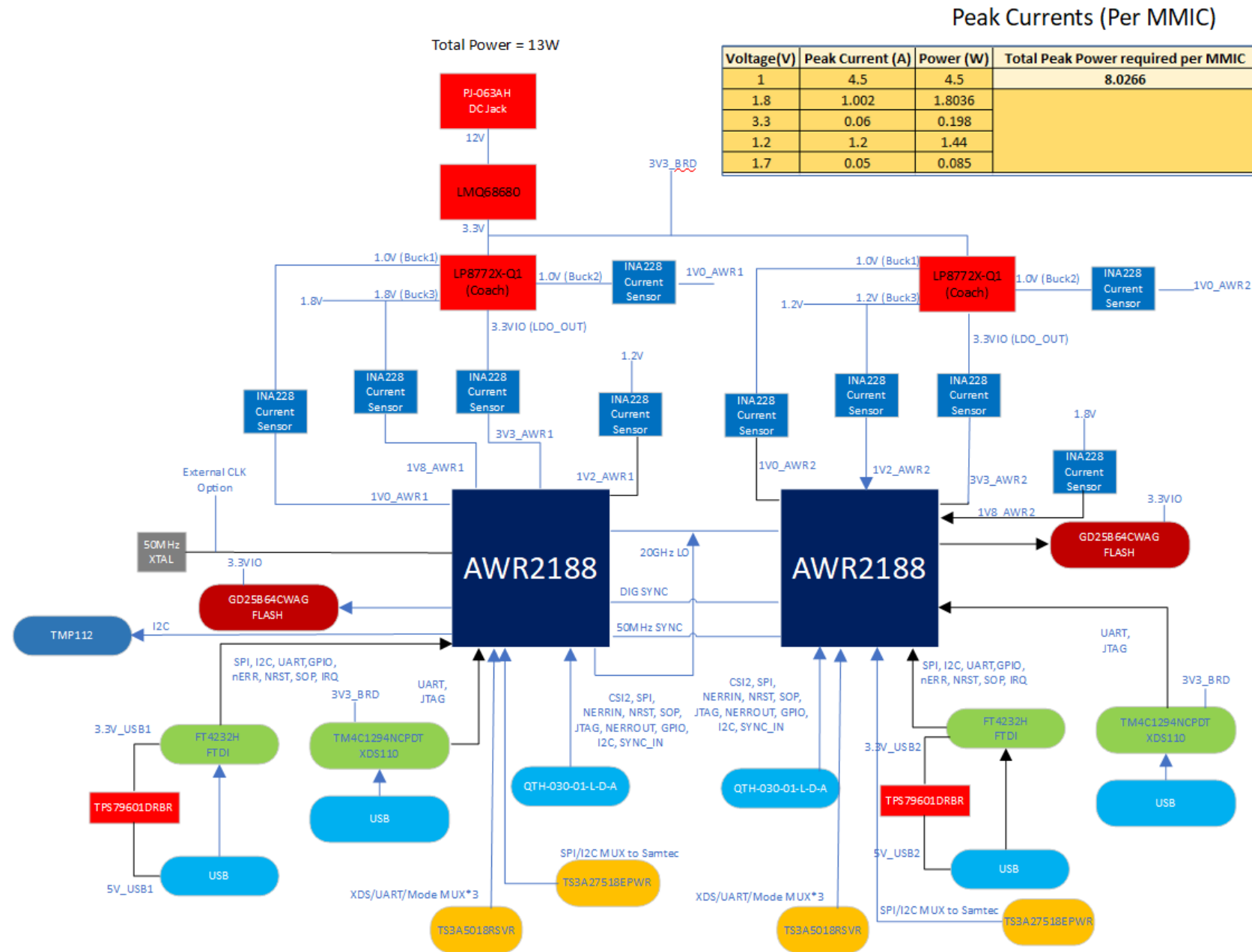
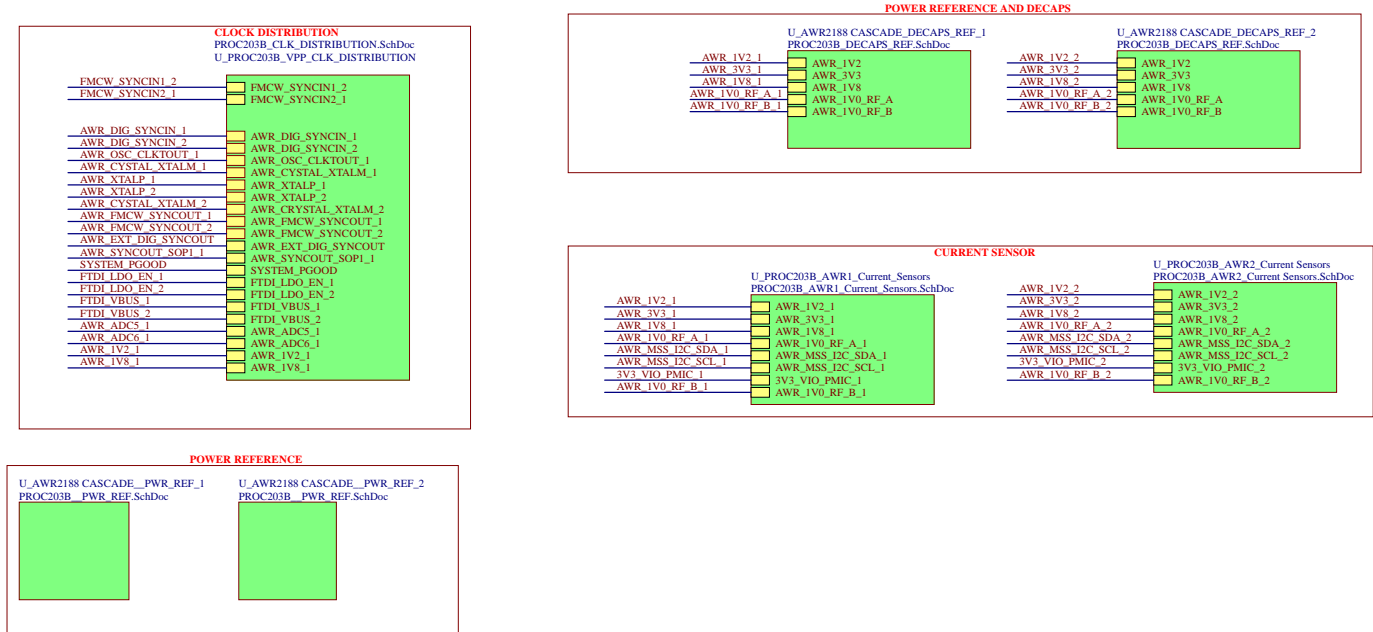
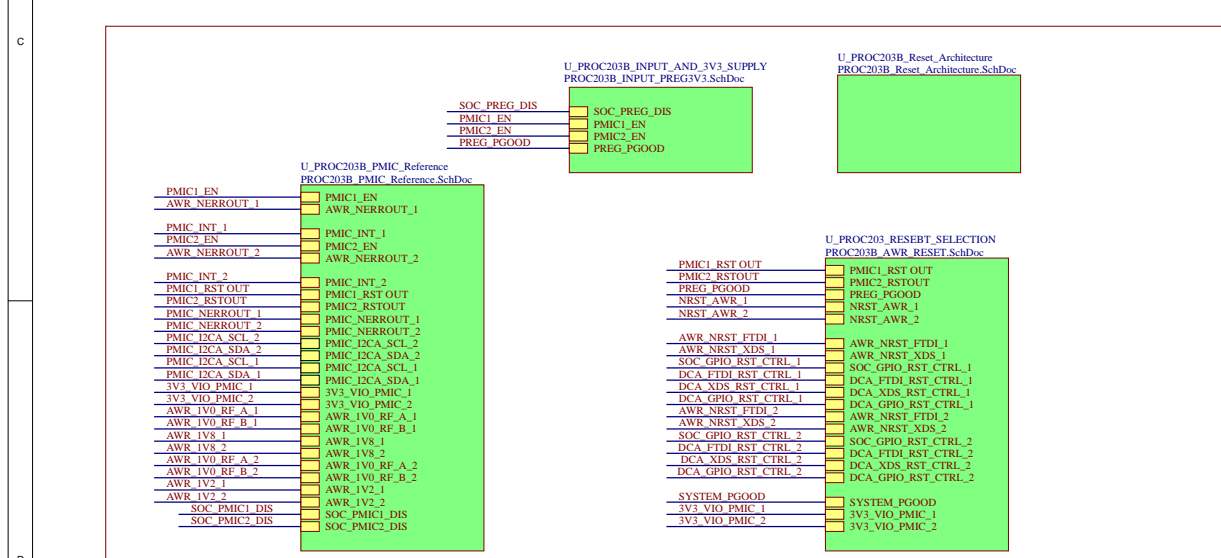
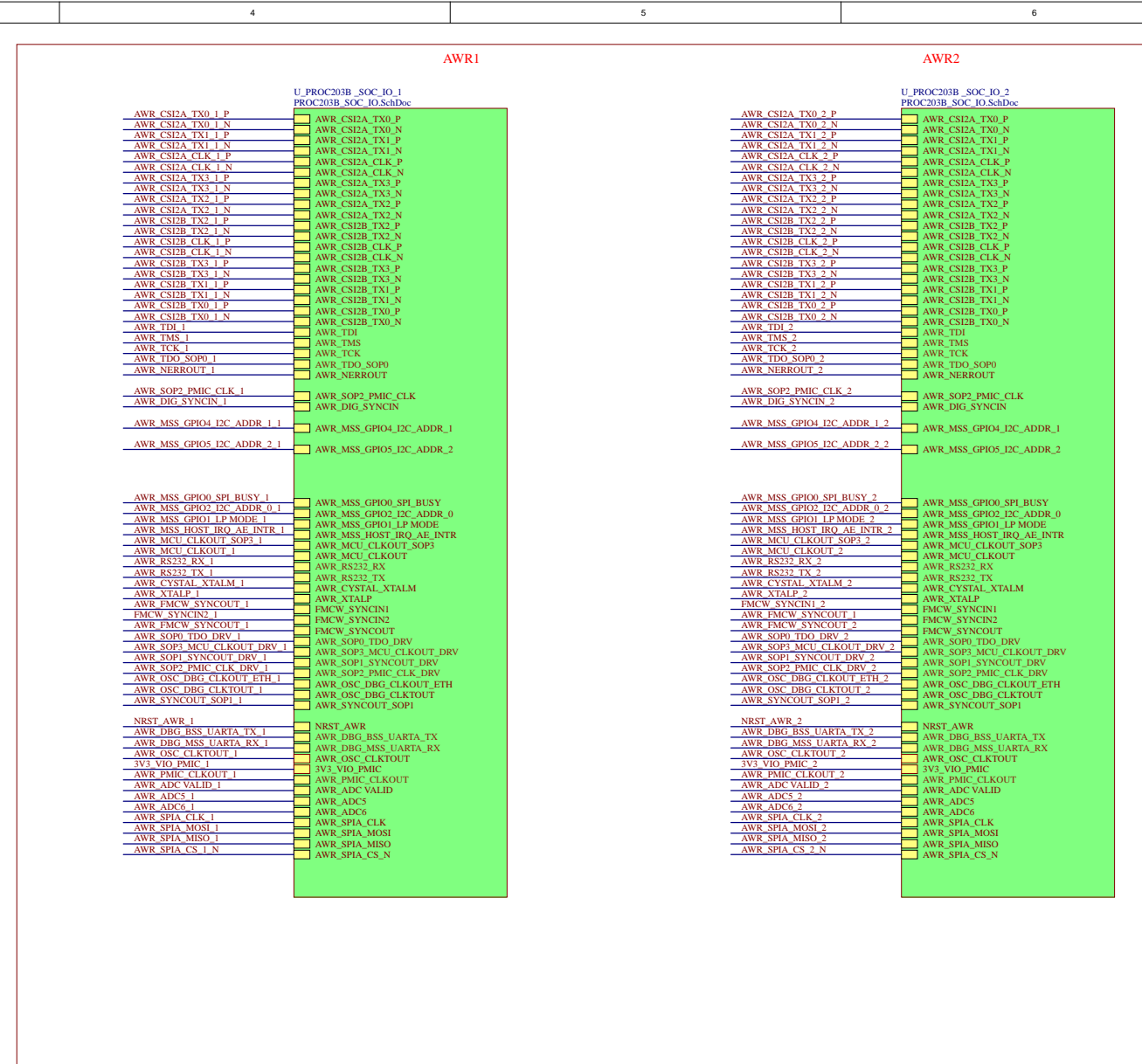
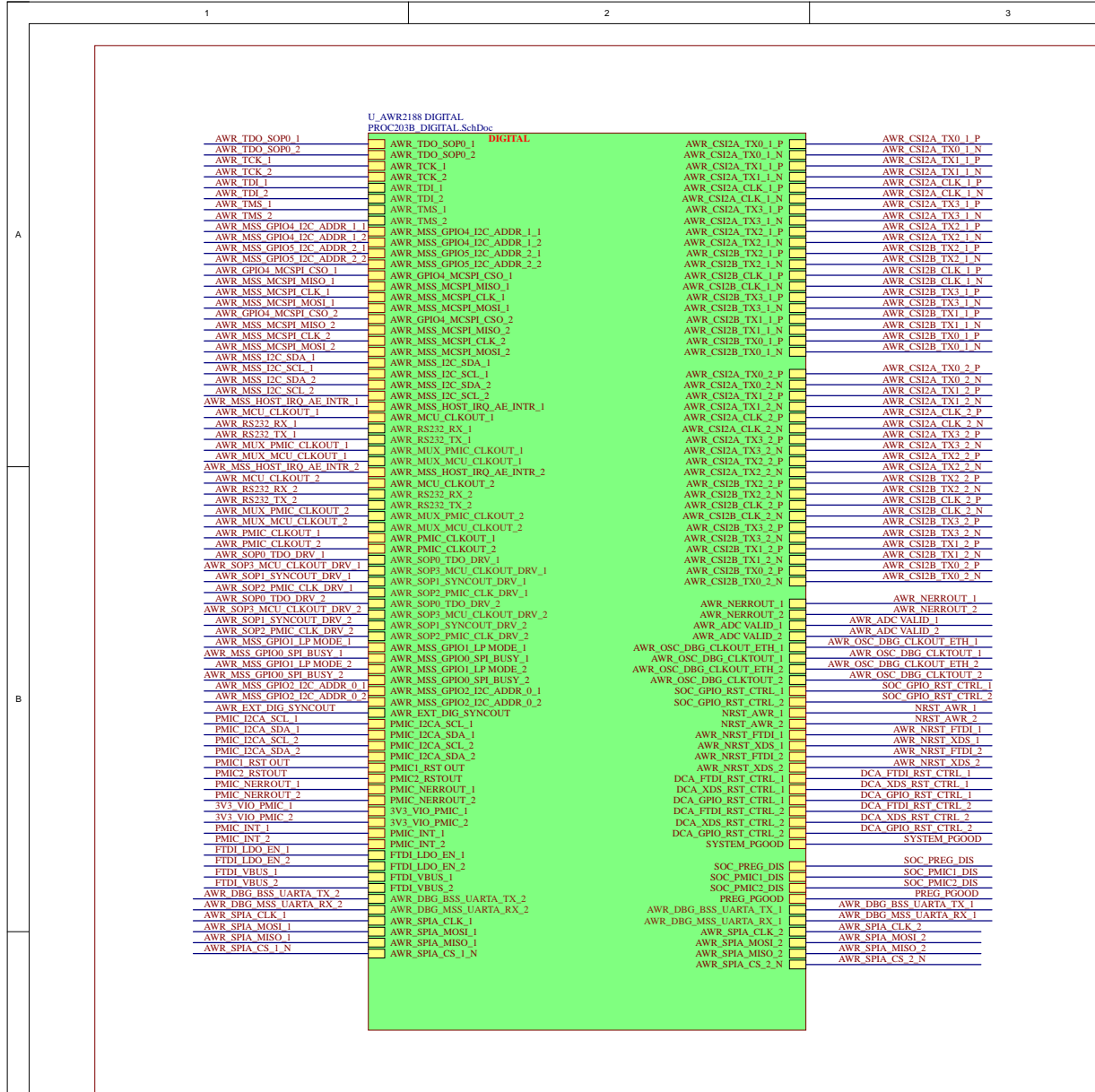


## AWR2188LOPEVM BLOCK DIAGRAM

## TABLE OF CONTENTS









# AWR2188\_ IO REFERENCE

Class Name: AWR\_20GHZ\_LO

This schematic diagram illustrates the IO reference for the AWR2188 device. It shows the internal connections of the AWR2188 chip to various external components and signals. The diagram is organized into several sections:

- Top Section:** Shows the connection of the AWR2188 chip to the AWR2188\_10 reference. It includes signals like FMCW\_SYNCOUT, FMCW\_SYNCIN1, FMCW\_SYNCIN2, and AWR\_OSC\_CLKTOUT. A note indicates that R2 and R6 should be placed without any stub, and R8 and R11 should be placed without any stub.
- Left Section:** Shows the connection of the AWR2188 chip to the AWR2188\_10 reference. It includes signals like AWR\_ADC5, AWR\_ADC6, AWR\_DIG\_SYNCIN, and AWR\_DIG\_SYNCIN2. A note indicates that R2 and R6 should be placed without any stub, and R8 and R11 should be placed without any stub.
- Right Section:** Shows the connection of the AWR2188 chip to the AWR2188\_10 reference. It includes signals like AWR\_OSC\_CLKTOUT, AWR\_OSC\_CLKOUT\_ETH, AWR\_MCU\_CLKOUT, AWR\_PMIC\_CLK\_OUT, and AWR\_SYNCOUT\_SOP1. A note indicates that R2 and R6 should be placed without any stub, and R8 and R11 should be placed without any stub.
- Bottom Section:** Shows the connection of the AWR2188 chip to the AWR2188\_10 reference. It includes signals like AWR\_SYNCOUT\_SOP1, AWR\_SYNCOUT\_SOP2, AWR\_SYNCOUT\_SOP3, AWR\_SYNCOUT\_SOP4, AWR\_SYNCOUT\_SOP5, AWR\_SYNCOUT\_SOP6, AWR\_SYNCOUT\_SOP7, AWR\_SYNCOUT\_SOP8, AWR\_SYNCOUT\_SOP9, AWR\_SYNCOUT\_SOP10, AWR\_SYNCOUT\_SOP11, AWR\_SYNCOUT\_SOP12, AWR\_SYNCOUT\_SOP13, AWR\_SYNCOUT\_SOP14, AWR\_SYNCOUT\_SOP15, AWR\_SYNCOUT\_SOP16, AWR\_SYNCOUT\_SOP17, AWR\_SYNCOUT\_SOP18, AWR\_SYNCOUT\_SOP19, AWR\_SYNCOUT\_SOP20, AWR\_SYNCOUT\_SOP21, AWR\_SYNCOUT\_SOP22, AWR\_SYNCOUT\_SOP23, AWR\_SYNCOUT\_SOP24, AWR\_SYNCOUT\_SOP25, AWR\_SYNCOUT\_SOP26, AWR\_SYNCOUT\_SOP27, AWR\_SYNCOUT\_SOP28, AWR\_SYNCOUT\_SOP29, AWR\_SYNCOUT\_SOP30, AWR\_SYNCOUT\_SOP31, AWR\_SYNCOUT\_SOP32, AWR\_SYNCOUT\_SOP33, AWR\_SYNCOUT\_SOP34, AWR\_SYNCOUT\_SOP35, AWR\_SYNCOUT\_SOP36, AWR\_SYNCOUT\_SOP37, AWR\_SYNCOUT\_SOP38, AWR\_SYNCOUT\_SOP39, AWR\_SYNCOUT\_SOP40, AWR\_SYNCOUT\_SOP41, AWR\_SYNCOUT\_SOP42, AWR\_SYNCOUT\_SOP43, AWR\_SYNCOUT\_SOP44, AWR\_SYNCOUT\_SOP45, AWR\_SYNCOUT\_SOP46, AWR\_SYNCOUT\_SOP47, AWR\_SYNCOUT\_SOP48, AWR\_SYNCOUT\_SOP49, AWR\_SYNCOUT\_SOP50, AWR\_SYNCOUT\_SOP51, AWR\_SYNCOUT\_SOP52, AWR\_SYNCOUT\_SOP53, AWR\_SYNCOUT\_SOP54, AWR\_SYNCOUT\_SOP55, AWR\_SYNCOUT\_SOP56, AWR\_SYNCOUT\_SOP57, AWR\_SYNCOUT\_SOP58, AWR\_SYNCOUT\_SOP59, AWR\_SYNCOUT\_SOP60, AWR\_SYNCOUT\_SOP61, AWR\_SYNCOUT\_SOP62, AWR\_SYNCOUT\_SOP63, AWR\_SYNCOUT\_SOP64, AWR\_SYNCOUT\_SOP65, AWR\_SYNCOUT\_SOP66, AWR\_SYNCOUT\_SOP67, AWR\_SYNCOUT\_SOP68, AWR\_SYNCOUT\_SOP69, AWR\_SYNCOUT\_SOP70, AWR\_SYNCOUT\_SOP71, AWR\_SYNCOUT\_SOP72, AWR\_SYNCOUT\_SOP73, AWR\_SYNCOUT\_SOP74, AWR\_SYNCOUT\_SOP75, AWR\_SYNCOUT\_SOP76, AWR\_SYNCOUT\_SOP77, AWR\_SYNCOUT\_SOP78, AWR\_SYNCOUT\_SOP79, AWR\_SYNCOUT\_SOP80, AWR\_SYNCOUT\_SOP81, AWR\_SYNCOUT\_SOP82, AWR\_SYNCOUT\_SOP83, AWR\_SYNCOUT\_SOP84, AWR\_SYNCOUT\_SOP85, AWR\_SYNCOUT\_SOP86, AWR\_SYNCOUT\_SOP87, AWR\_SYNCOUT\_SOP88, AWR\_SYNCOUT\_SOP89, AWR\_SYNCOUT\_SOP90, AWR\_SYNCOUT\_SOP91, AWR\_SYNCOUT\_SOP92, AWR\_SYNCOUT\_SOP93, AWR\_SYNCOUT\_SOP94, AWR\_SYNCOUT\_SOP95, AWR\_SYNCOUT\_SOP96, AWR\_SYNCOUT\_SOP97, AWR\_SYNCOUT\_SOP98, AWR\_SYNCOUT\_SOP99, AWR\_SYNCOUT\_SOP100.

The diagram includes various components such as resistors (R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100), capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100), and other components like the AWR2188 chip, AWR2188\_10 reference, and various IO signals.

[illegible]

## QSPI FLASH REFERENCE

The schematic diagram illustrates the QSPI Flash Reference circuit for the GD25B64CWAG chip. The chip is connected to a 3V3\_VIO\_PMIC power supply and a GND. The circuit includes several resistors and capacitors for signal conditioning and timing.

**Power and Ground Connections:**

- VCC (Pin 8):** Connected to 3V3\_VIO\_PMIC through resistor R24\_1 (0Ω).
- EP VSS (Pin 9):** Connected to GND.

**Signal Connections:**

- IO2 (Pin 3):** Connected to AWR\_QSPI\_D2 through resistor R37\_1 (33.2Ω).
- IO3 (Pin 7):** Connected to AWR\_QSPI\_D3 through resistor R40\_1 (33.2Ω).
- IO1 (Pin 2):** Connected to AWR\_QSPI\_D1 through resistor R40\_1 (33.2Ω).
- CS (Pin 1):** Connected to AWR\_QSPI\_CS through resistor R36\_1 (33.2Ω).
- SCLK (Pin 6):** Connected to AWR\_QSPI\_SCLK through resistor R33\_1 (33.2Ω).
- SI(IO2) (Pin 5):** Connected to AWR\_QSPI\_D0\_SOP4 through resistor R34\_1 (33.2Ω).
- SO(IO1) (Pin 4):** Connected to AWR\_QSPI\_D1 through resistor R35\_1 (33.2Ω).

**Timing and Decoupling Components:**

- Capacitors:** C1\_1 (1uF) and C2\_1 (0.1uF) are connected between the VCC line and GND.
- Resistors:** R31\_1 (10.0kΩ) and R32\_1 (10.0kΩ) are connected between the 3V3\_VIO\_PMIC supply and the CS line. R29\_1 (10.0kΩ) and R30\_1 (47.5kΩ) are connected between the 3V3\_VIO\_PMIC supply and the SCLK line.

**Chip Information:**

- Chip Model:** GD25B64CWAG
- Pin Count:** 8 pins (VCC, EP VSS, IO2, IO3, CS, SCLK, SI(IO2), SO(IO1))

## NERROROUT LED

3V3\_VIO\_PMIC

R46\_1  
510

DS1\_1  
Red

AWR\_NERROUT

## DEBUG CONNECTOR

3V3\_VIO\_PMIC

R58\_1  
0

C12\_1  
1uF

GND

AWR\_NERROUT

AWR\_DBG\_BSS\_UARTA\_TX

AWR\_DBG\_MSS\_UARTA\_RX

AWR\_MSS\_GPIO1\_LP\_MODE

AWR\_MSS\_GPIO0\_SPI\_BUSY

AWR\_ADC\_VALID

NRST\_AWR

SSM-110-L-DV-A-K-TR

AWR\_MSS\_GPIO2\_I2C\_ADDR\_0

AWR\_MSS\_GPIO4\_I2C\_ADDR\_1

AWR\_MSS\_GPIO5\_I2C\_ADDR\_2

AWR\_MSS\_HOST\_IRQ\_AE\_INTR

AWR\_RS232\_TX

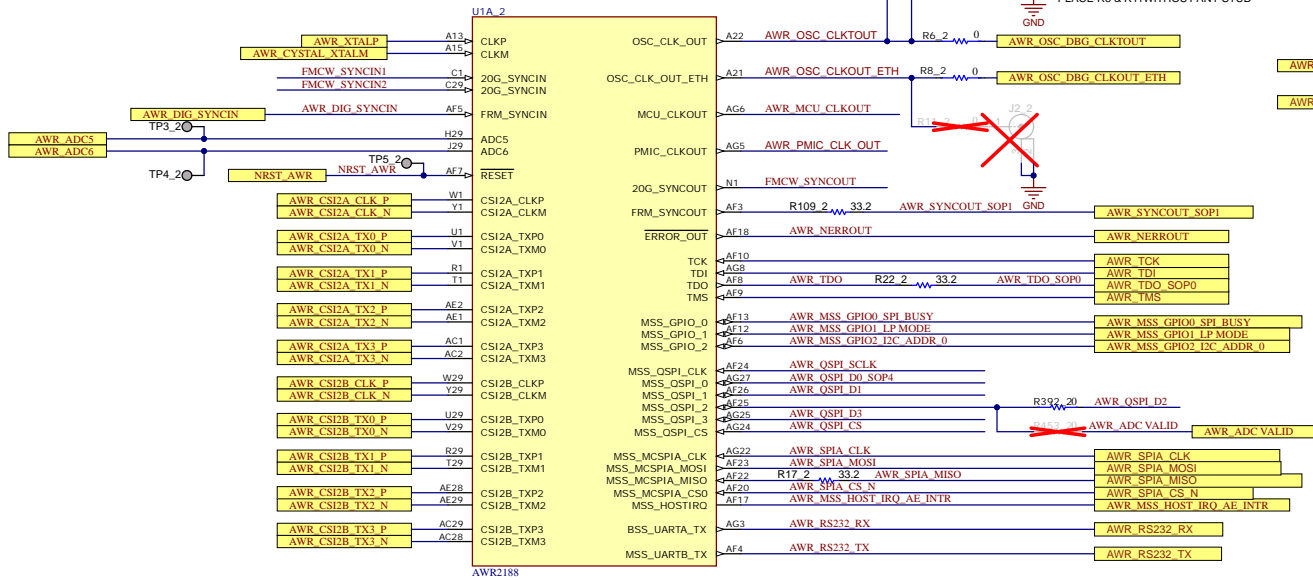
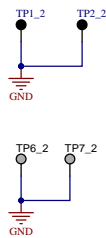
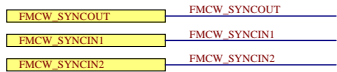
AWR\_RS232\_RX

VPP\_IP7

SSM-110-L-DV-A-K-TR

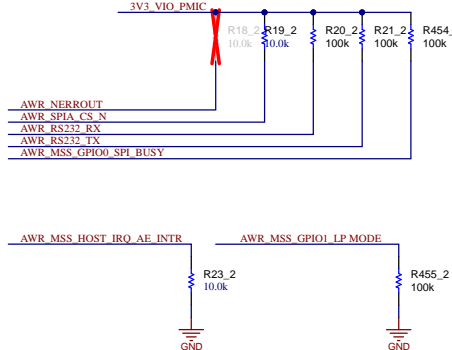


# AWR2188\_ IO REFERENCE

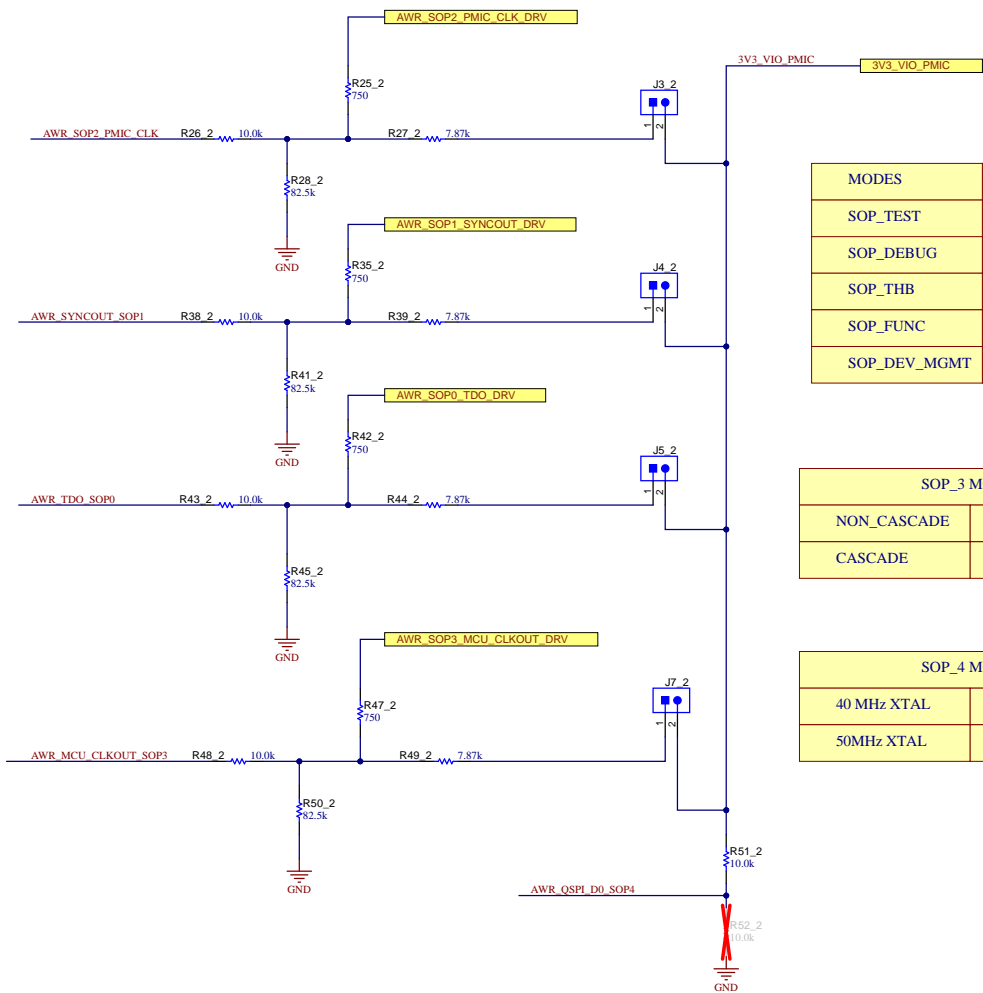


NOTE: PLACE R2 & R6 WITHOUT ANY STUB,  
PLACE R8 & R11 WITHOUT ANY STUB

## PULL UP & PULL DOWN OPTIONS



## SOP REFERENCE

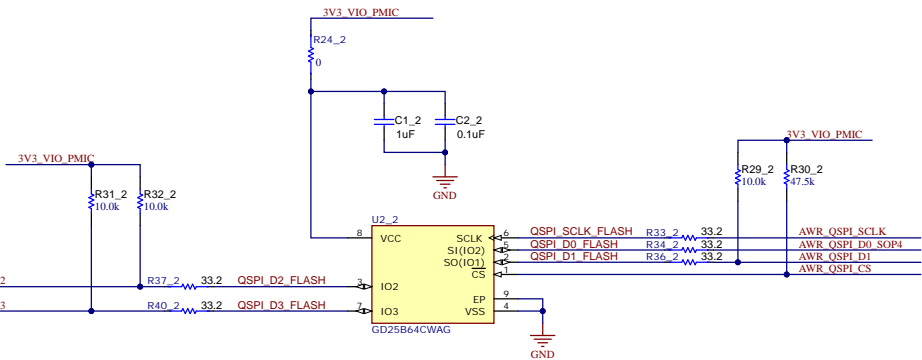


MODES	SOP(2,1,0)
SOP_TEST	0 1 0
SOP_DEBUG	0 1 1
SOP_THB	0 0 0
SOP_FUNC	0 0 1
SOP_DEV_MGMT	1 0 1

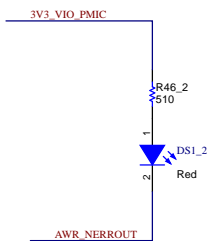
SOP_3 MODES	
NON_CASCADE	0
CASCADE	1

SOP_4 MODES	
40 MHz XTAL	0
50MHz XTAL	1

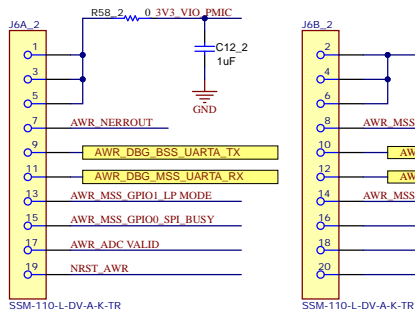
## QSPI FLASH REFERENCE



## NERROROUT LED

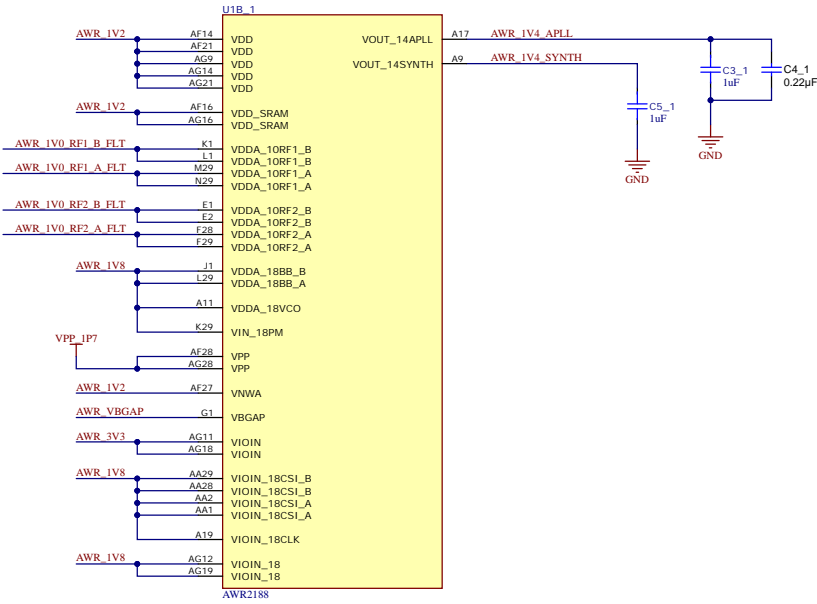


## DEBUG CONNECTOR

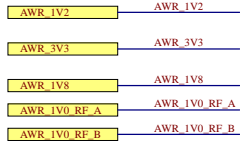




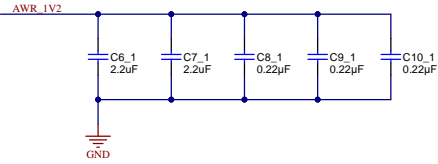
POWER REFERENCE



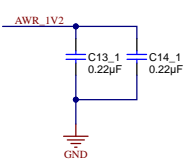
DECOUPLING REFERENCE



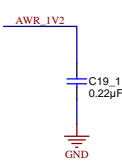
1.2V DIGITAL SUPPLY



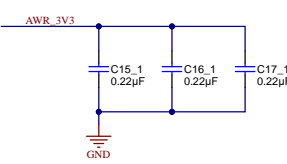
SRAM SUPPLY



VNWA SUPPLY



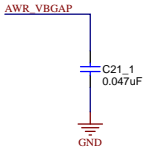
3.3V IO SUPPLY



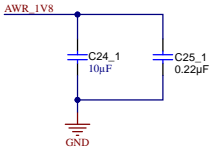
VPP SUPPLY



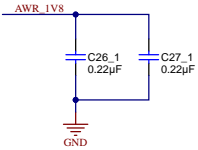
BANDGAP SUPPLY



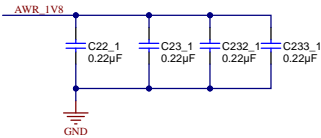
1.8V CLOCK SUPPLY



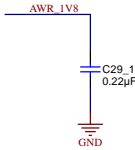
1.8V IO SUPPLY



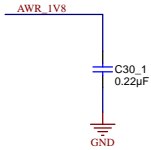
1.8V CSI SUPPLY



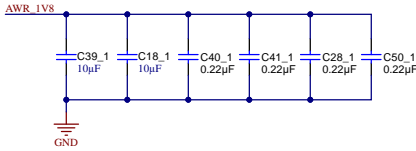
1.8V PM SUPPLY



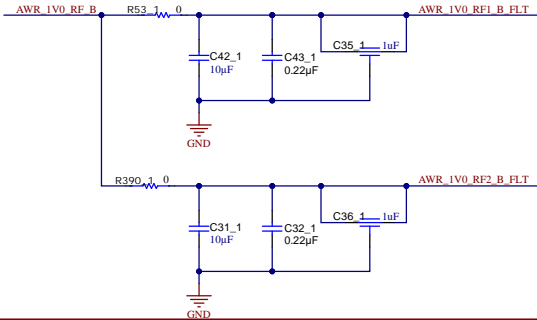
1.8V VCO SUPPLY



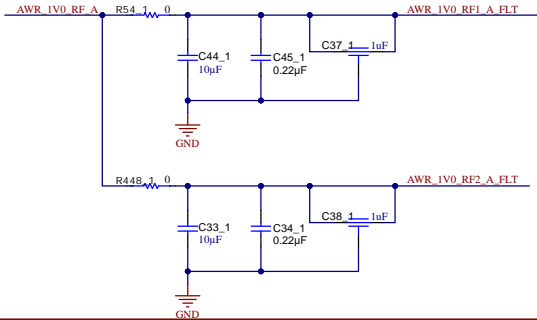
1.8V BB SUPPLY



RF\_B SUPPLY

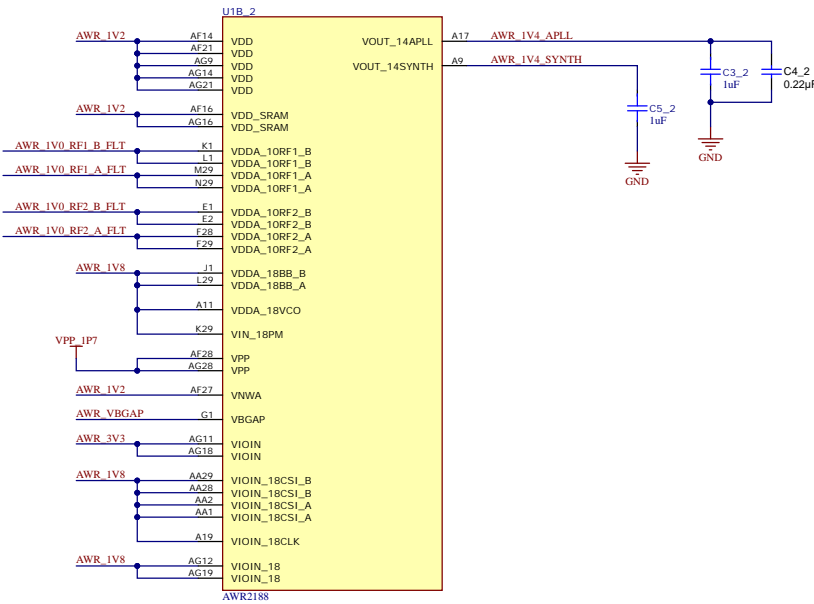


RF\_A SUPPLY

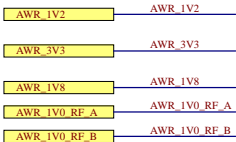




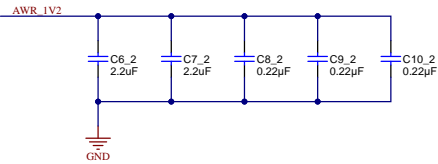
POWER REFERENCE



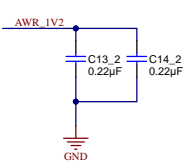
DECOUPLING REFERENCE



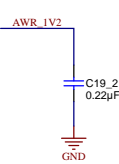
1.2V DIGITAL SUPPLY



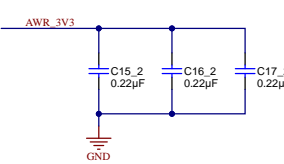
SRAM SUPPLY



VNWA SUPPLY



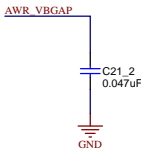
3.3V IO SUPPLY



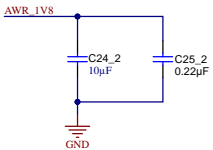
VPP SUPPLY



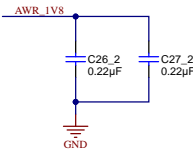
BANDGAP SUPPLY



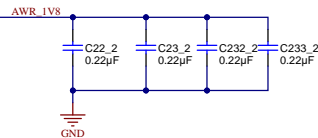
1.8V CLOCK SUPPLY



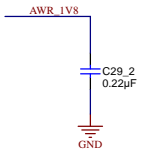
1.8V IO SUPPLY



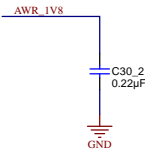
1.8V CSI SUPPLY



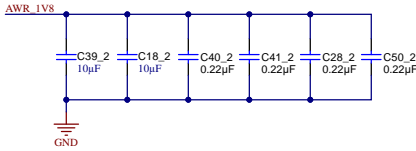
1.8V PM SUPPLY



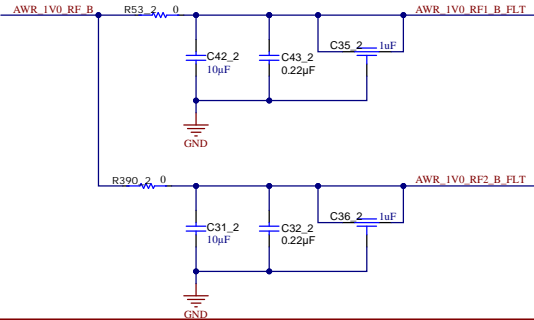
1.8V VCO SUPPLY



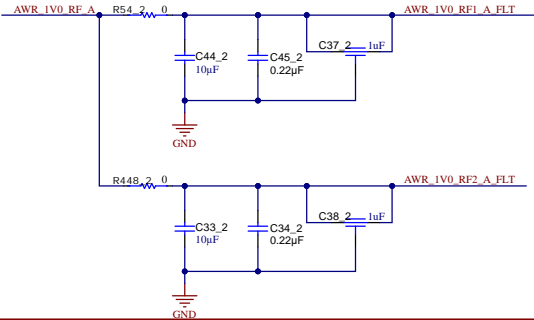
1.8V BB SUPPLY



RF\_B SUPPLY



RF\_A SUPPLY



Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

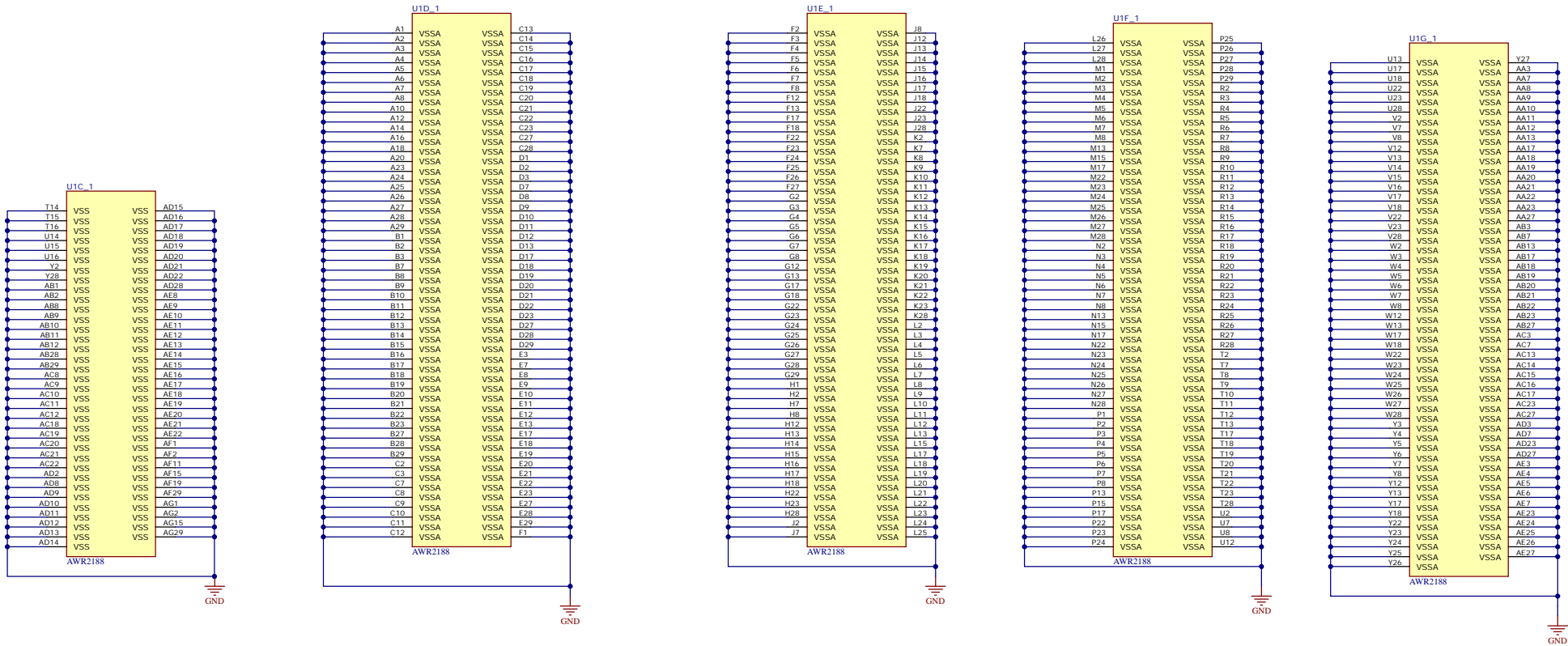
Orderable: AWR2188LOPEVM	Designed for: Public Release	Mod. Date: 15-05-2025
TID #: N/A	Project Title: AWR2188LOPEVM	
Number: PROC203	Rev: B	Sheet Title: DECAPS
SVN Rev: 468	Assembly Variant: 001	Sheet: 4 of 19
Drawn By: Aydin Kiasat	File: PROC203B_DECAPS_REF_SchDoc	Size: C
Engineer: Aydin Kiasat	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	



© Texas Instruments 2024

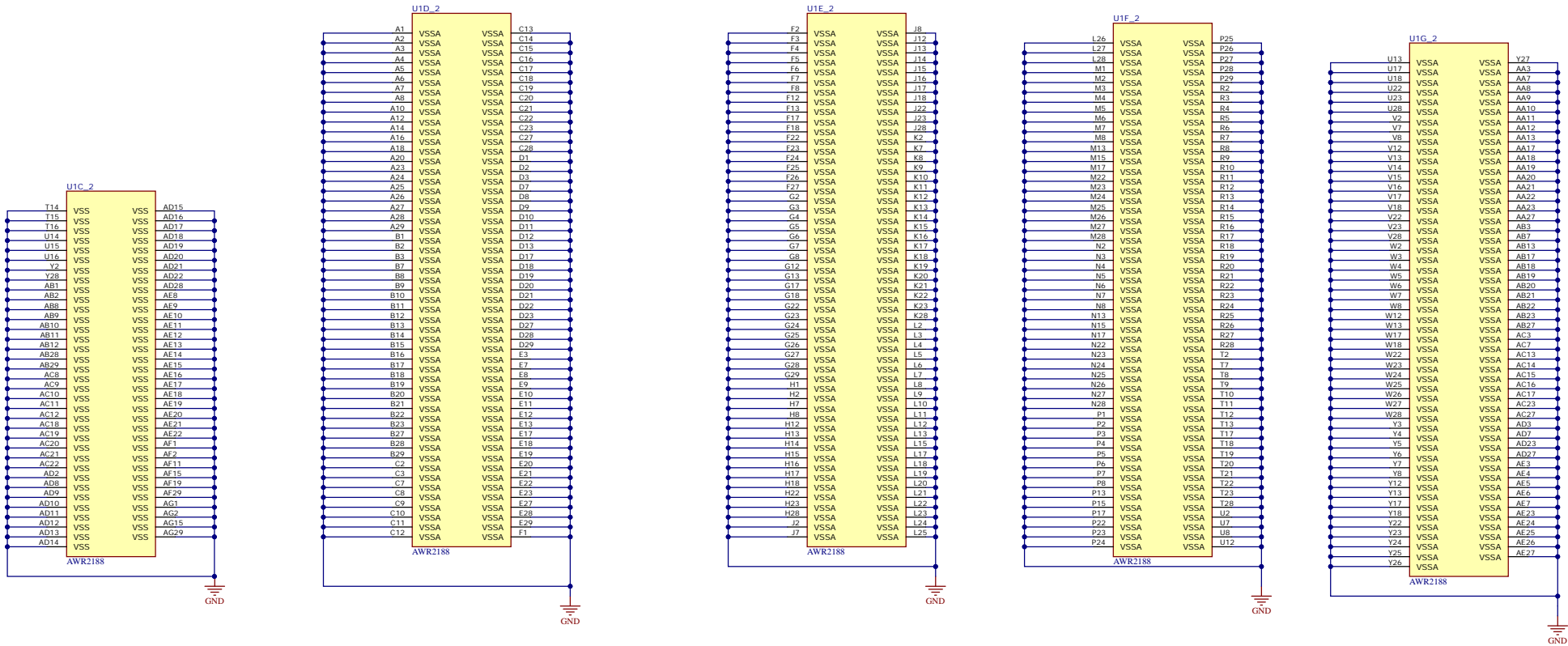


AWR 2188 PWR REFERENCE





AWR 2188 PWR REFERENCE



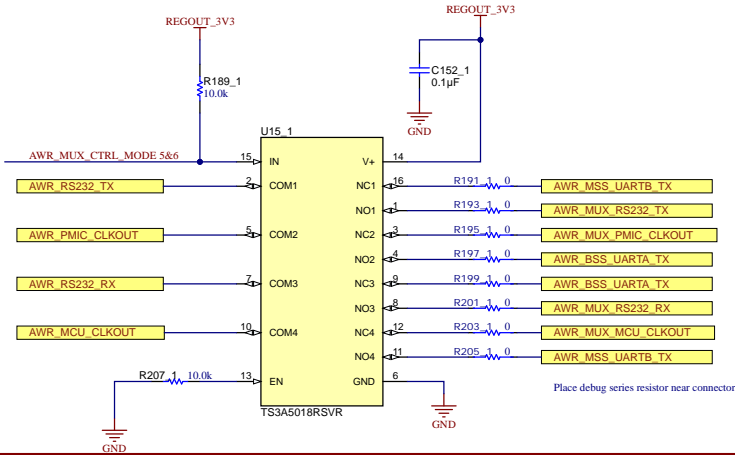




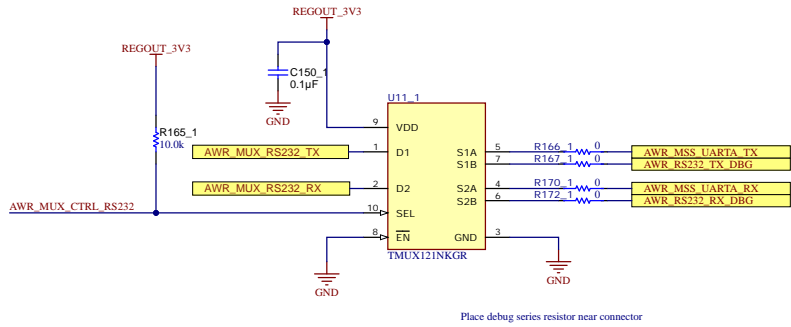


AWR MUX SELECTION

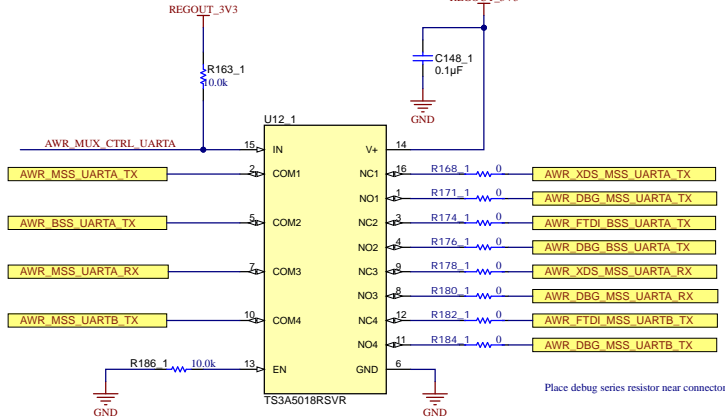
MUX BETWEEN MODE 5 AND MODE 6



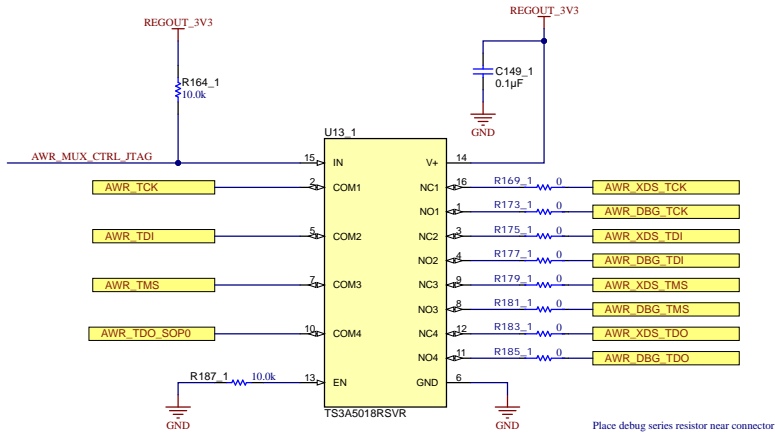
MUX BETWEEN MODE 3 AND MODE 6



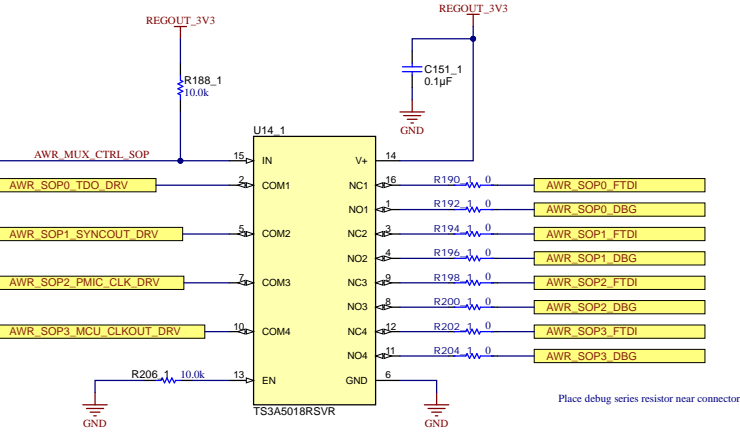
UART MUX BETWEEN XDS110 AND DBG CONNECTOR



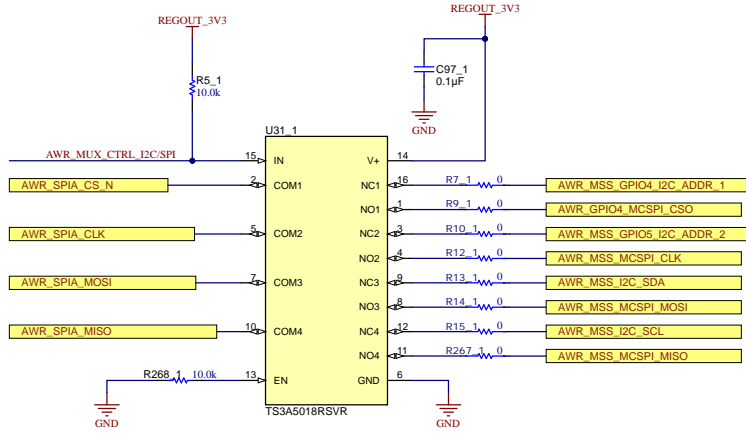
JTAG MUX BETWEEN XDS110 AND DBG CONNECTOR



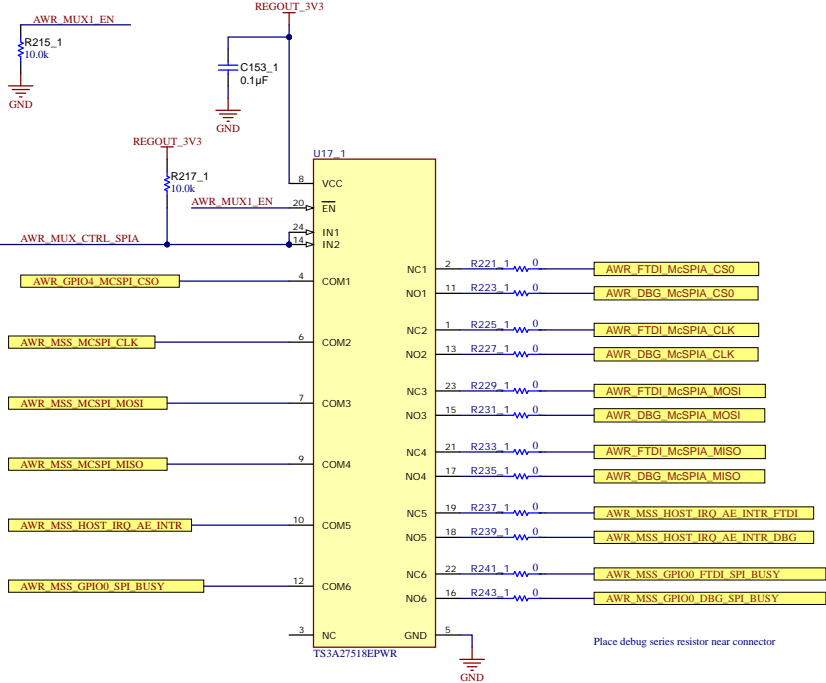
MUX FOR SOP BETWEEN DBG CONNECTOR AND FTDI



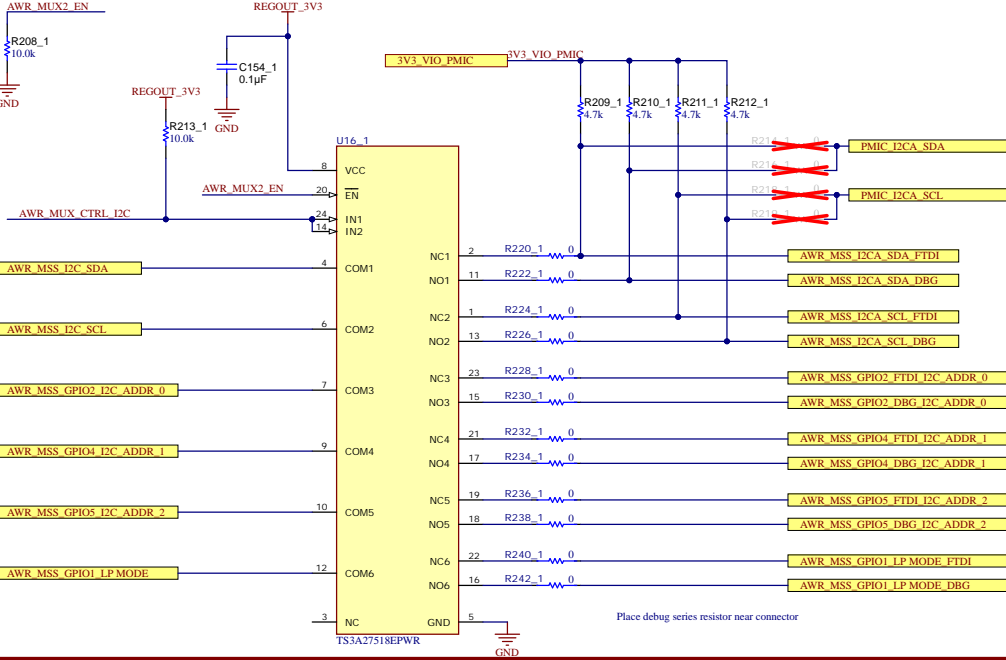
MUX BETWEEN SPI AND I2C



MUX FOR SPIA BETWEEN DBG CONNECTOR AND FTDI

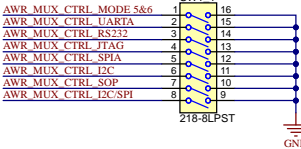


MUX FOR I2C BETWEEN DBG CONNECTOR AND FTDI



REF DESG	IN	MODES	SIGNALS
U15	HIGH	MODE 6	RS232 TX/RX, BSS UARTA TX & MSS UARTB TX
	LOW	MODE 5	MSS UARTB TX, PMIC CLKOUT, MCU CLKOUT & BSS UARTA TX
U11	HIGH	MODE 6	RS232 TX/RX
	LOW	MODE 3	MSS UARTA RX/TX

SWITCH FOR MUX INPUT SELECTION

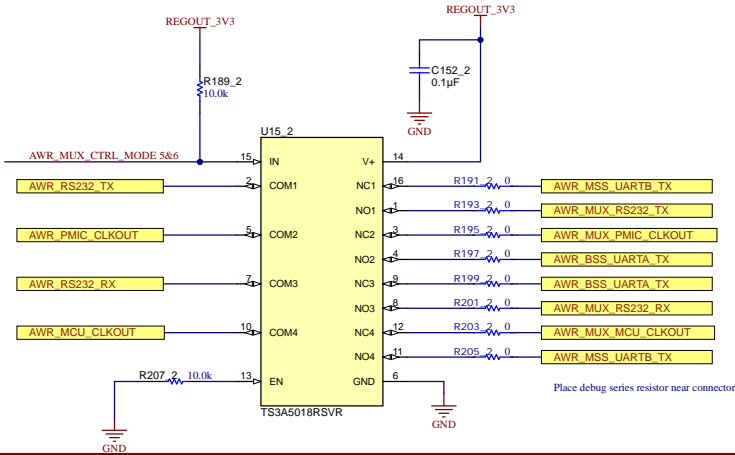


IN	NC to COM, COM to NC	NO to COM, COM to NO
H	OFF	ON
L	ON	OFF

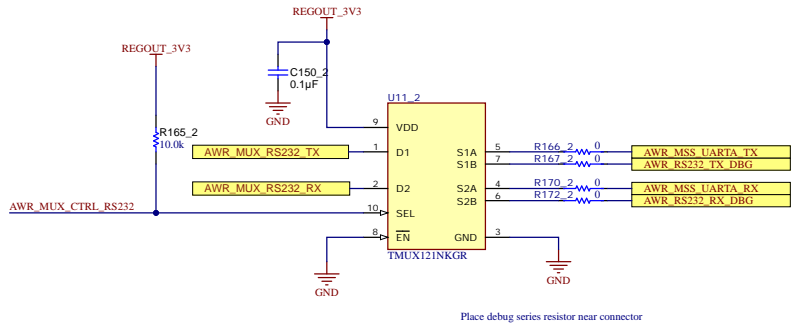


AWR MUX SELECTION

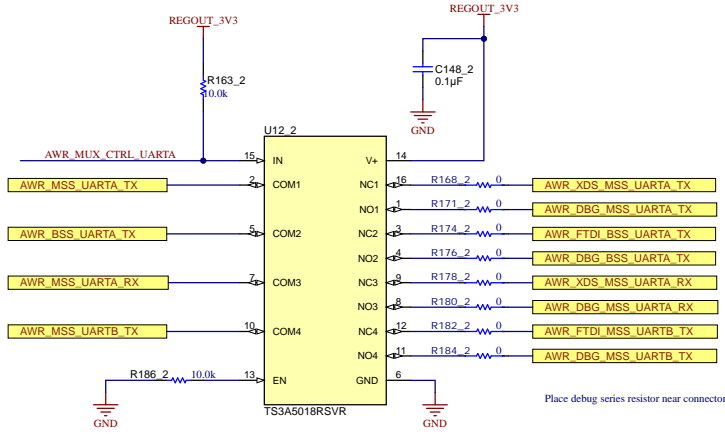
MUX BETWEEN MODE 5 AND MODE 6



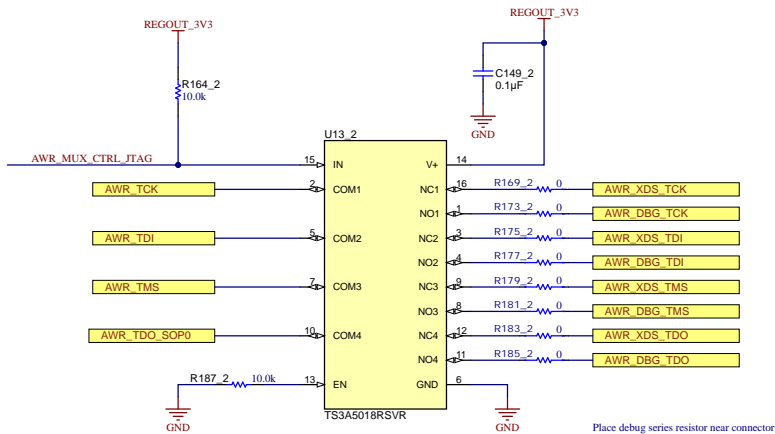
MUX BETWEEN MODE 3 AND MODE 6



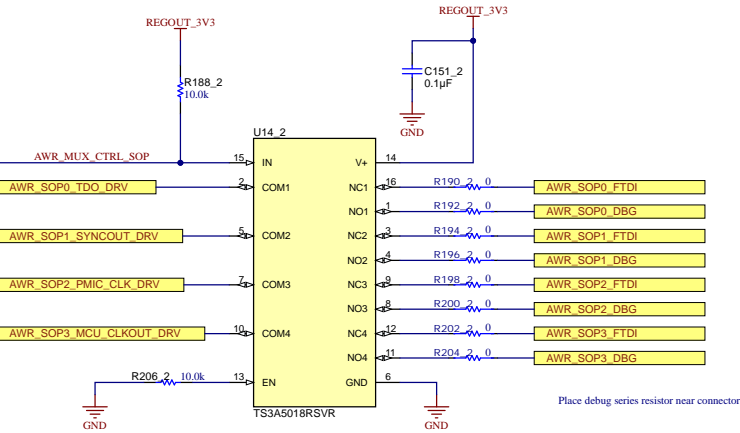
UART MUX BETWEEN XDS110 AND DBG CONNECTOR



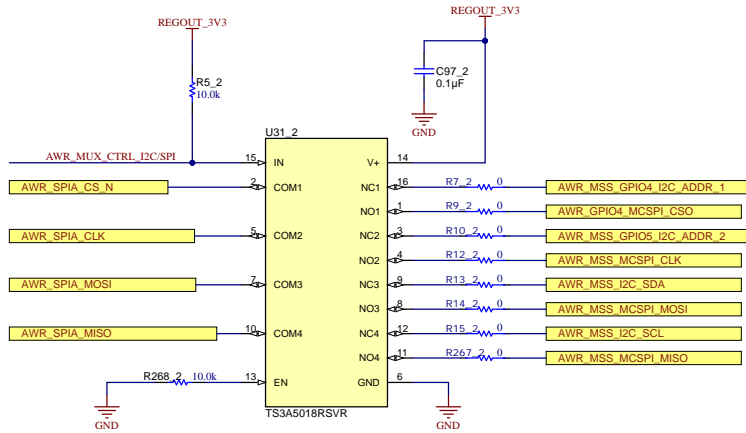
JTAG MUX BETWEEN XDS110 AND DBG CONNECTOR



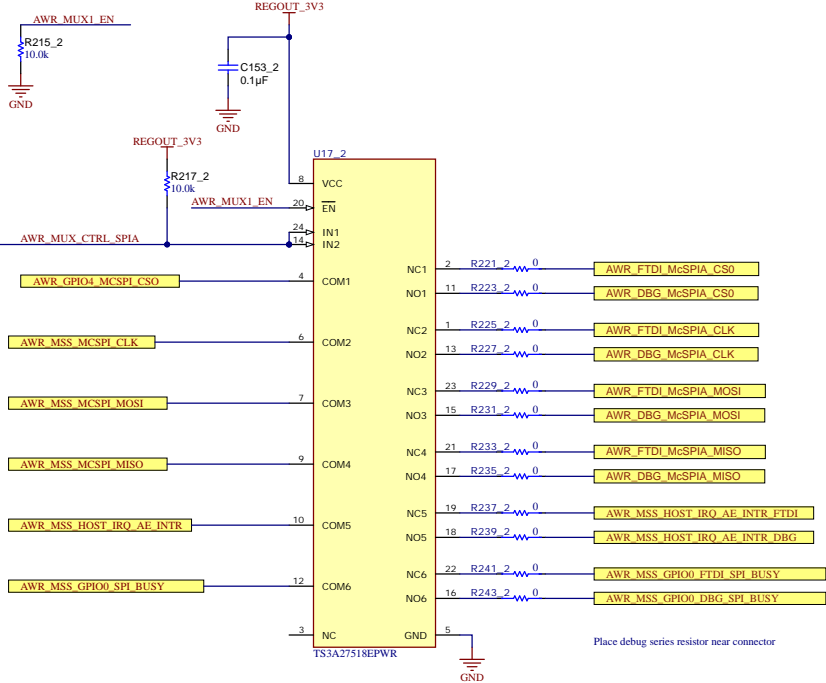
MUX FOR SOP BETWEEN DBG CONNECTOR AND FTDI



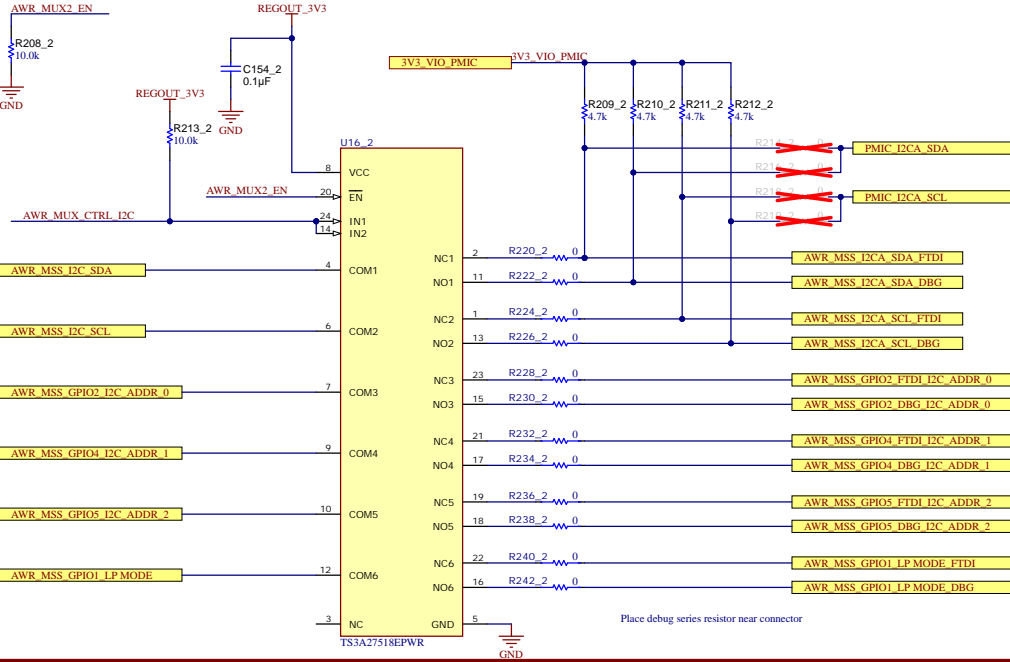
MUX BETWEEN SPI AND I2C



MUX FOR SPIA BETWEEN DBG CONNECTOR AND FTDI

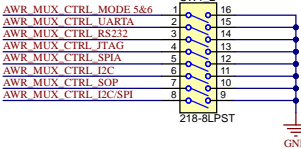


MUX FOR I2C BETWEEN DBG CONNECTOR AND FTDI



REF DESG	IN	MODES	SIGNALS
U15	HIGH	MODE 6	RS232 TX/RX, BSS UARTA TX & MSS UARTB TX
	LOW	MODE 5	MSS UARTB TX, PMIC CLKOUT, MCU CLKOUT & BSS UARTA TX
U11	HIGH	MODE 6	RS232 TX/RX
	LOW	MODE 3	MSS UARTA RX/TX

SWITCH FOR MUX INPUT SELECTION

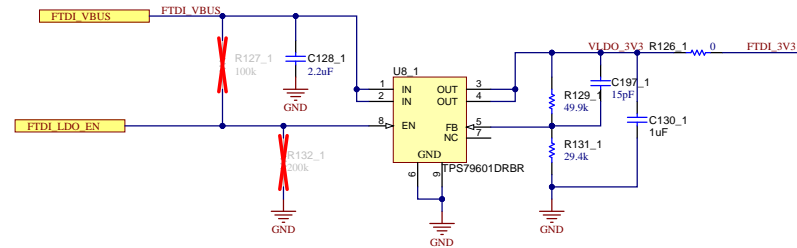


IN	NC to COM, COM to NC	NO to COM, COM to NO
H	OFF	ON
L	ON	OFF

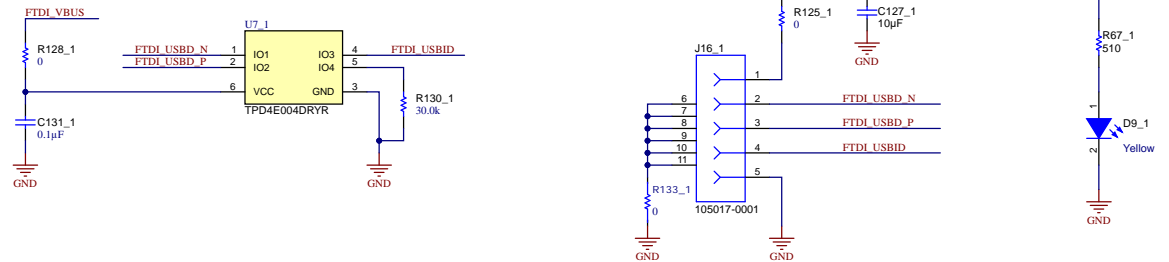


**AWR FTDI**

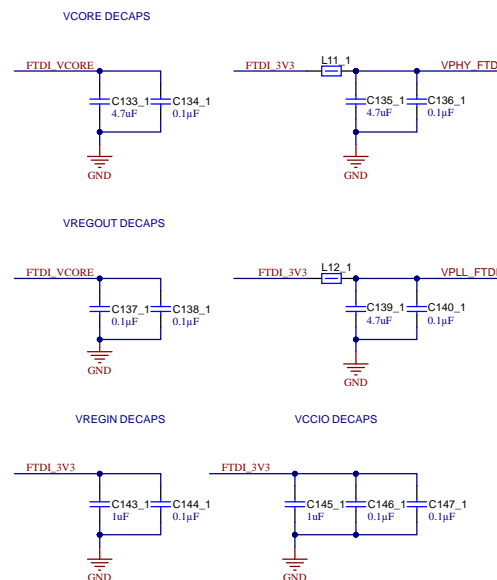
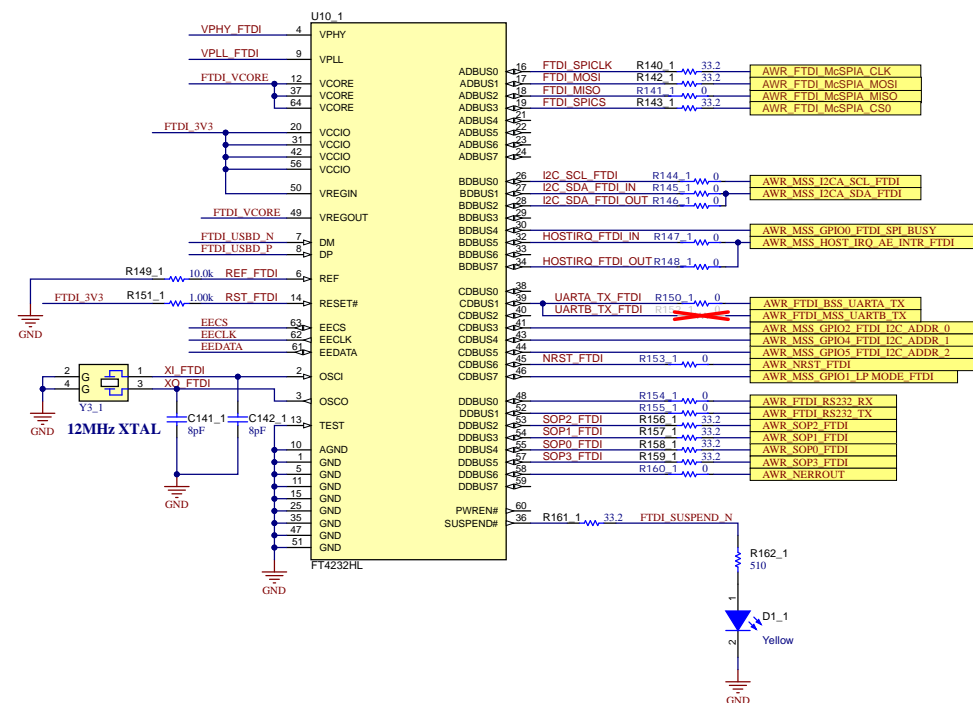
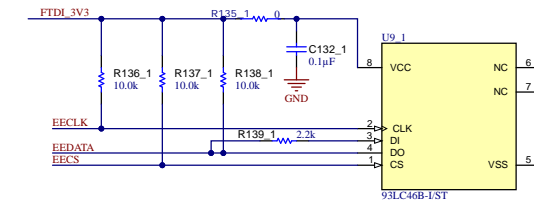
### 3.3V LDO FOR FTDI



## FTDI USB PORT



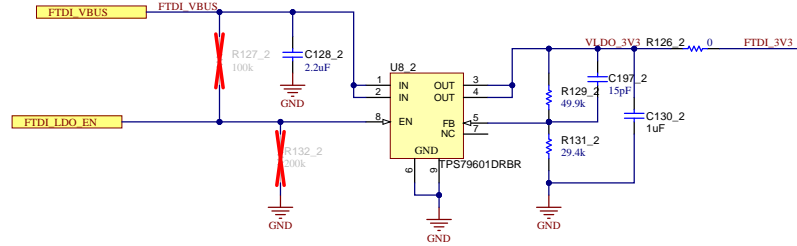
## FTDI SUPPLY DECAPS

**FTDI EEPROM**

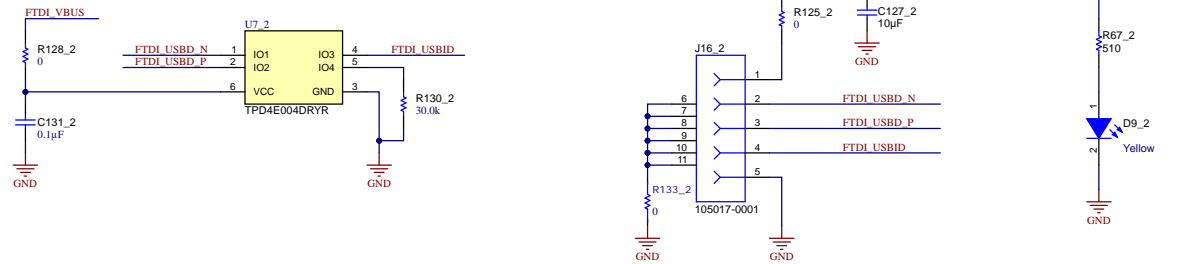


**AWR FTDI**

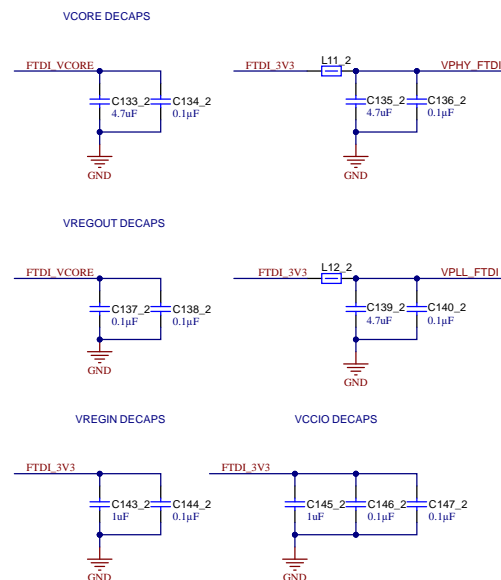
### 3.3V LDO FOR FTDI



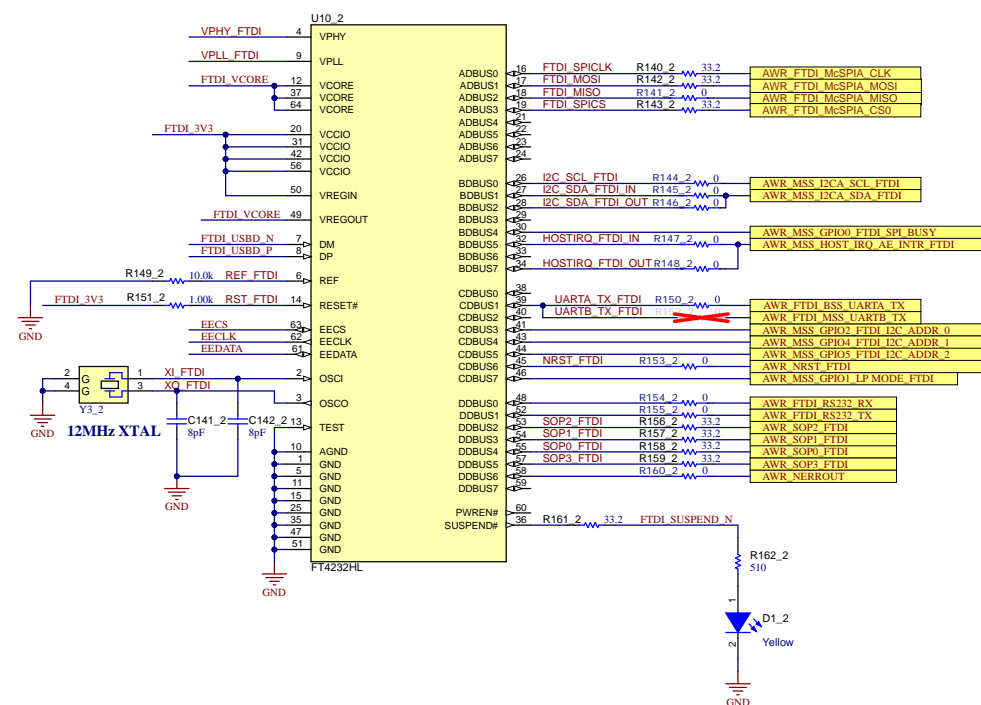
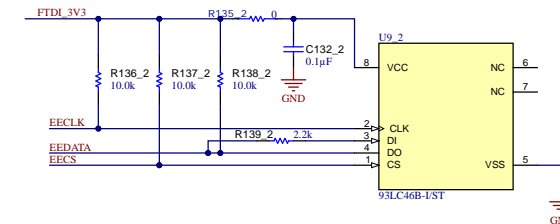
## FTDI USB PORT



## FTDI SUPPLY DECAPS



## FTDI EEPROM

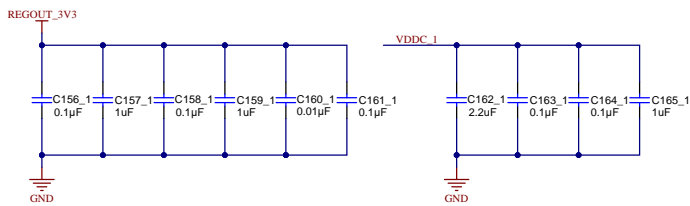




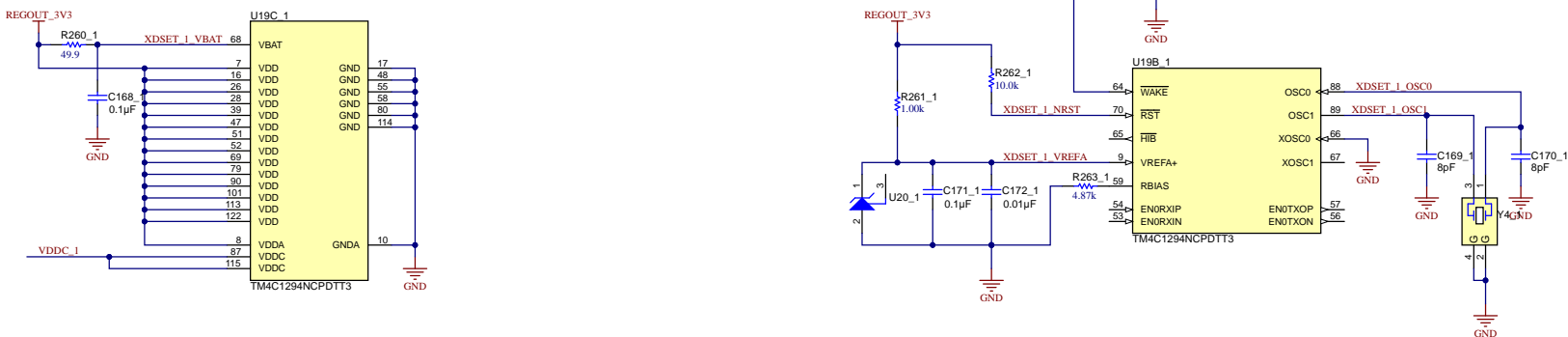
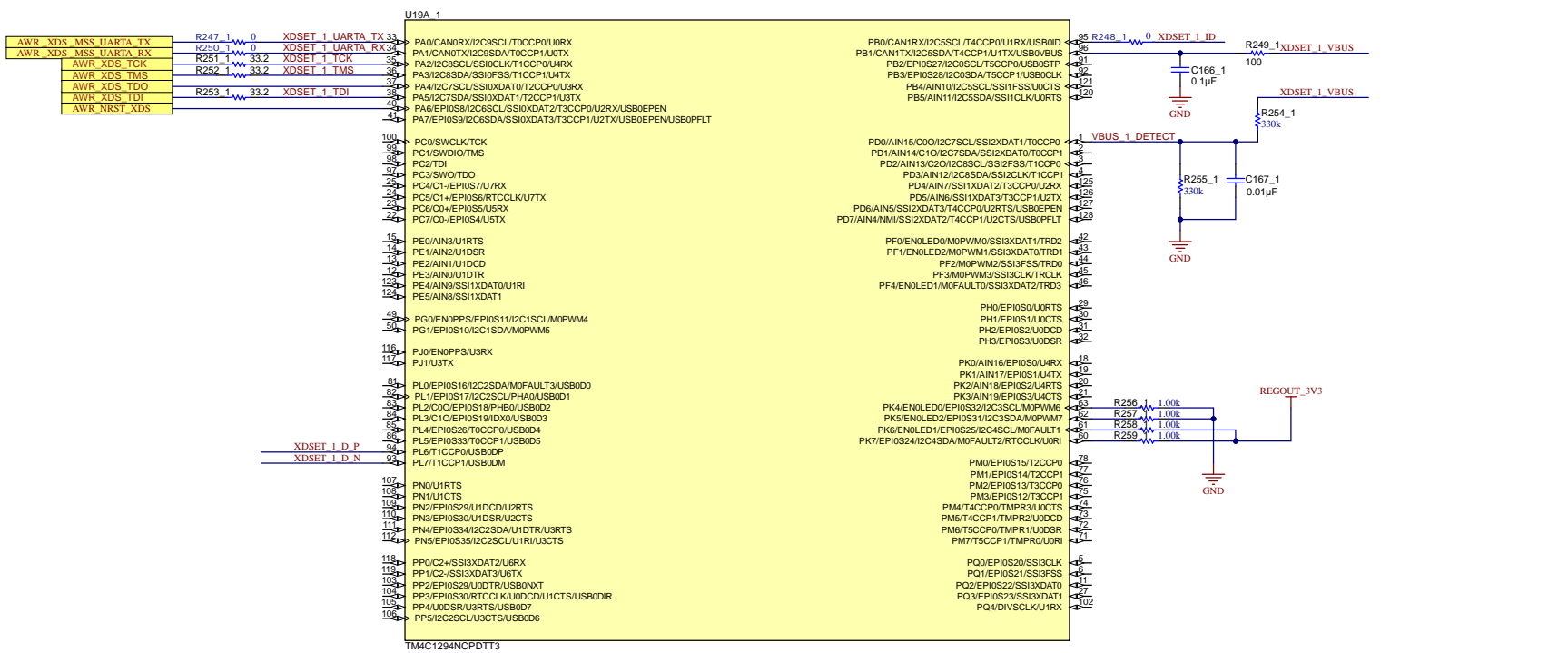
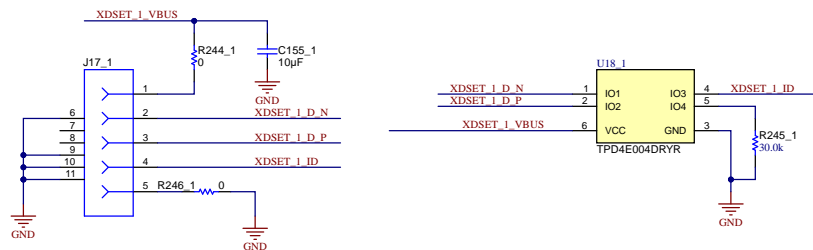
[TM4C1294NCPDT Datasheet](#)

## AWR XDS110

## XDS110 DECOUPLING CAPS



## XDS110 USB PORT



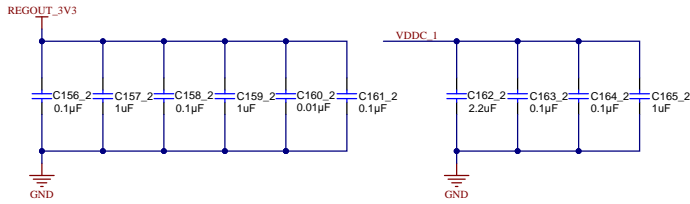


References

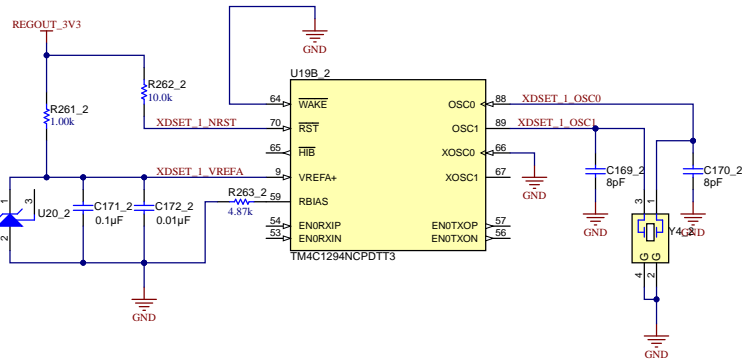
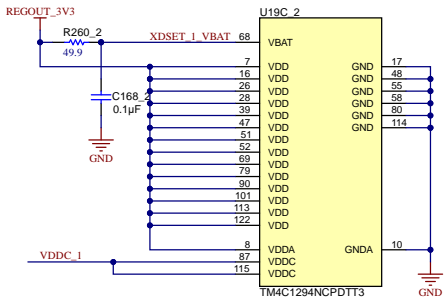
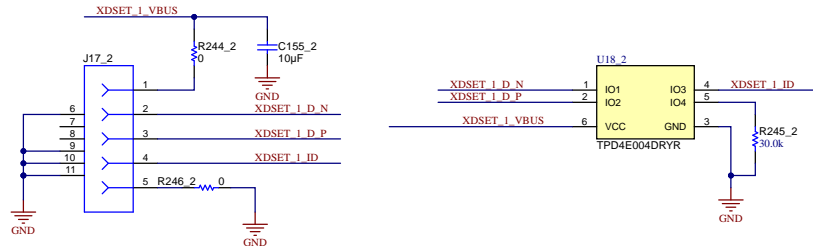
TM4C1294NCPDT Datasheet

AWR XDS110

XDS110 DECOUPLING CAPS



XDS110 USB PORT





## AWR1





## DIG\_SYNC Distribution

The schematic diagram illustrates the DIG\_SYNC Distribution circuit. It features a power supply section with a 3V3 regulator (REGOUT\_3V3) and a 3V3 supply (VDD\_3V3). The regulator output is connected to the 1G pin of the LMK1C1102PWR IC. The 1G pin is also connected to the 1G pin of the LMK1C1102PWR IC. The CLKIN pin of the LMK1C1102PWR IC is connected to the DIG\_SYNCOUT\_RS signal. The Y0 and Y1 outputs of the LMK1C1102PWR IC are connected to the AWR\_DIG\_SYNCIN\_1 and AWR\_DIG\_SYNCIN\_2 signals, respectively. The AWR\_SYNCOUT\_SOP1\_1 and AWR\_EXT\_DIG\_SYNCOUT blocks are connected to the DIG\_SYNCOUT\_RS signal through resistors R60 and R61. The AWR\_DIG\_SYNCIN\_1 and AWR\_DIG\_SYNCIN\_2 signals are connected to the AWR\_SYNCOUT\_SOP1\_1 and AWR\_EXT\_DIG\_SYNCOUT blocks through resistors R462 and R463.

## 20GHz LO Distribution

The diagram illustrates the 20GHz LO Distribution circuit. It features two Wilkinson Power Dividers. The first divider, labeled "Wilkinson Power Divider", has a Class Name of "AWR\_FMCW\_20G". It takes an input signal "AWR\_FMCW\_SYNCOUT\_2" and splits it into two outputs: "AWR\_FMCW\_SYNCOUT\_1" and "AWR\_FMCW\_SYNCOUT\_1". The second divider, also labeled "Wilkinson Power Divider", has a Class Name of "AWR\_FMCW\_20G". It takes an input signal "AWR\_FMCW\_SYNCOUT\_1" and splits it into two outputs: "FMCW\_SYNCIN1\_2" and "FMCW\_SYNCIN2\_1". The circuit includes a 50 ohm termination resistor (R63) and a 49.9 ohm resistor (R64). A note indicates that the unused SYNCOUT2 of AWR1 and SYNCIN1 of AWR2 are shorted to GND. The circuit is powered by a 50 ohm termination resistor (R63) and a 49.9 ohm resistor (R64).

Class Name: AWR\_FMCW\_20G

AWR\_FMCW\_SYNCOUT\_2

R63 49.9

GND

Class Name: AWR\_FMCW\_20G

AWR\_FMCW\_SYNCOUT\_1

AWR\_FMCW\_SYNCOUT\_1

R64 100Ω

AWR\_FMCW\_SYNCOUT\_1

AWR\_FMCW\_SYNCOUT\_1

50 ohm termination for unused SYNCOUT2 transmitters. Place with no minimal length routing near AWR U1\_2 BGA.

NOTE: AWR\_FMCW\_SYNCIN2 of AWR1 and SYNCIN1 of AWR2 unused. Shorted to GND

FMCW\_SYNCIN1\_2

FMCW\_SYNCIN2\_1

NT9

Net-Tie

NT10

Net-Tie

GND

## 50MHz Clock Distribution

### 50MHz CLK Source for Primary device

CAD NOTE: Place the crystal close to the Primary soc

### 50MHz CLK Source for Secondary device

CAD NOTE: Place the crystal close to the secondary soc

CAD NOTE: Place the crystal close to the Primary soc

CAD NOTE: Place the crystal close to the secondary soc

To provide 50 MHZ crystal input to secondary device mount Y2,R73,R70,R75 ,C53,C54and unmount R71 & C56

CAD NOTE: Place the crystal close to the Primary soc

CAD NOTE: Place the crystal close to the secondary soc

To provide 50 MHZ crystal input to secondary device mount Y2,R73,R70,R75 ,C53,C54and unmount R71 & C56

CAD NOTE: Place the crystal close to the Primary soc

CAD NOTE: Place the crystal close to the secondary soc

To provide 50 MHZ crystal input to secondary device mount Y2,R73,R70,R75 ,C53,C54and unmount R71 & C56

CAD NOTE: Place the crystal close to the Primary soc

CAD NOTE: Place the crystal close to the secondary soc

To provide 50 MHZ crystal input to secondary device mount Y2,R73,R70,R75 ,C53,C54and unmount R71 & C56

CAD NOTE: Place the crystal close to the Primary soc

CAD NOTE: Place the crystal close to the secondary soc

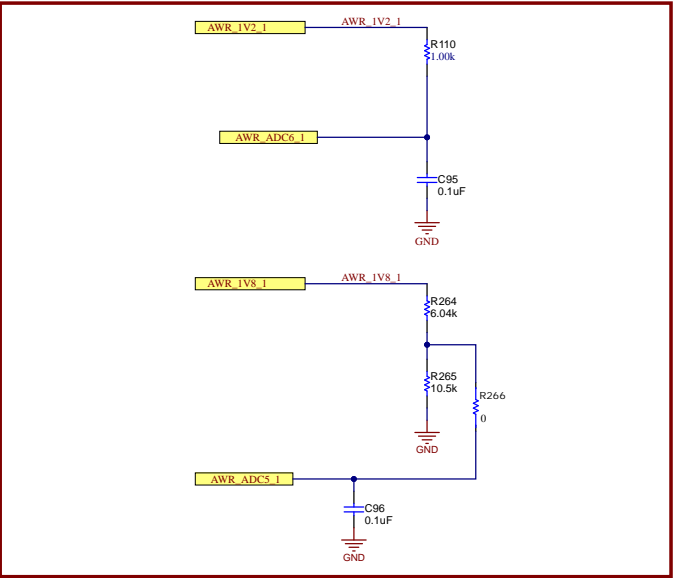
To provide 50 MHZ crystal input to secondary device mount Y2,R73,R70,R75 ,C53,C54and unmount R71 & C56

CAD NOTE: Place the crystal close to the Primary soc

CAD NOTE: Place the crystal close to the secondary soc

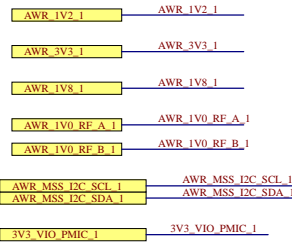
To provide 50 MHZ crystal input to secondary device mount Y2,R73,R70,R75 ,C53,C54and unmount R71 & C56

CAD NOTE: Place the crystal close to the Primary soc



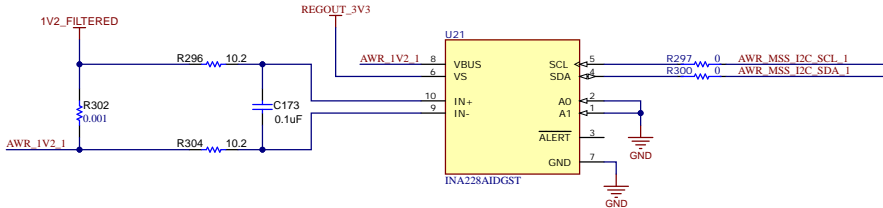


AWR1 CURRENT SENSORS



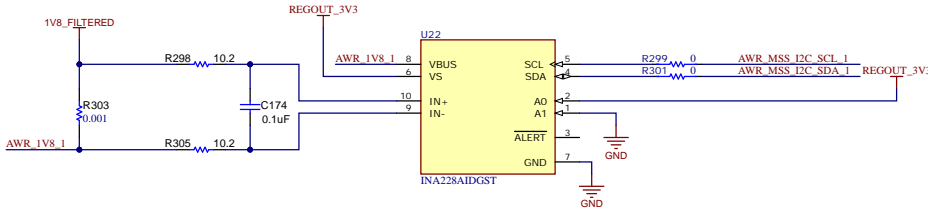
1.2V SUPPLY CURRENT SENSOR

I2C ADDRESS 0x40



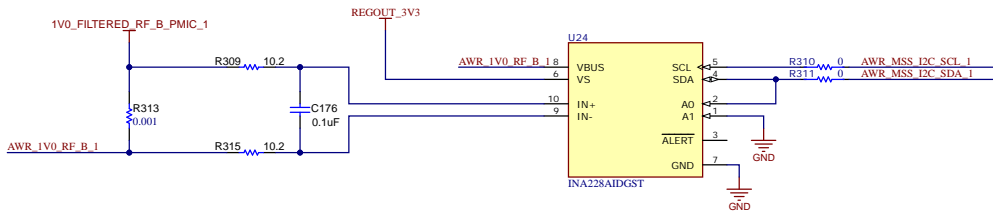
1.8V SUPPLY CURRENT SENSOR

I2C ADDRESS 0x41



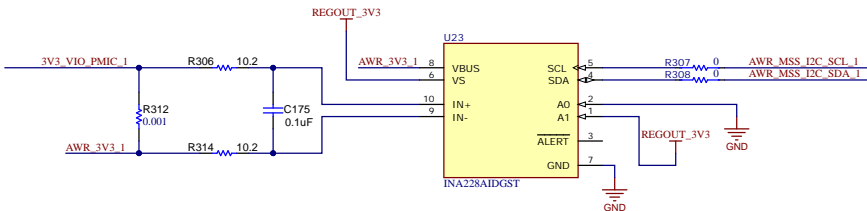
1.0V RFB SUPPLY CURRENT SENSOR

I2C ADDRESS 0x42



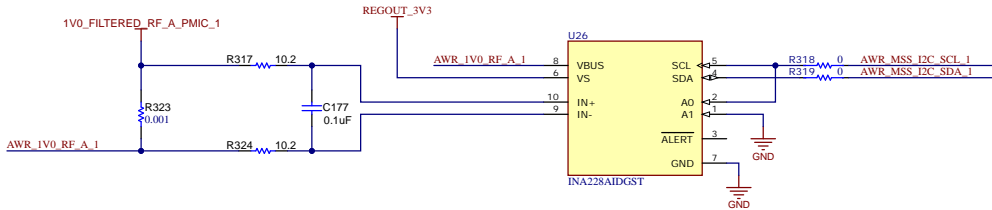
3.3V SUPPLY CURRENT SENSOR

I2C ADDRESS 0x44



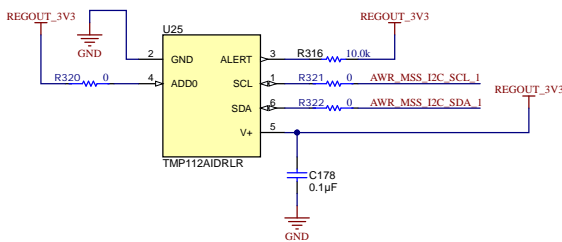
1.0V RFA SUPPLY CURRENT SENSOR

I2C ADDRESS 0x43



TEMP SENSOR

I2C ADDRESS 0x49

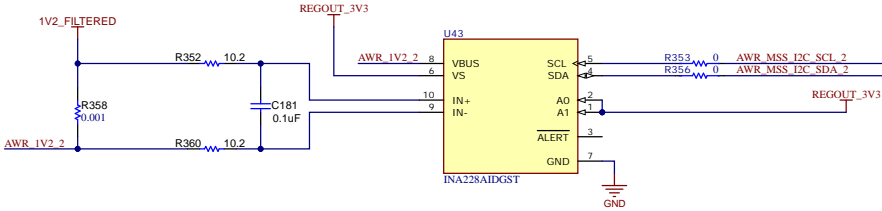




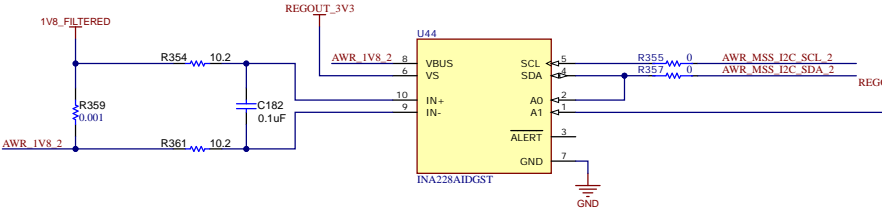
AWR2 CURRENT SENSORS

AWR_1V2_2	AWR_1V2_2
AWR_3V3_2	AWR_3V3_2
AWR_1V8_2	AWR_1V8_2
AWR_1V0_RF_A_2	AWR_1V0_RF_A_2
AWR_1V0_RF_B_2	AWR_1V0_RF_B_2
AWR_MSS_I2C_SCL_2	AWR_MSS_I2C_SCL_2
AWR_MSS_I2C_SDA_2	AWR_MSS_I2C_SDA_2
3V3_VIO_PMIC_2	3V3_VIO_PMIC_2

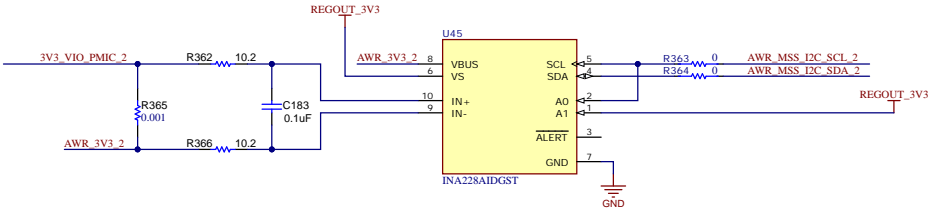
1.2V SUPPLY CURRENT SENSOR  
I2C ADDRESS 0x45



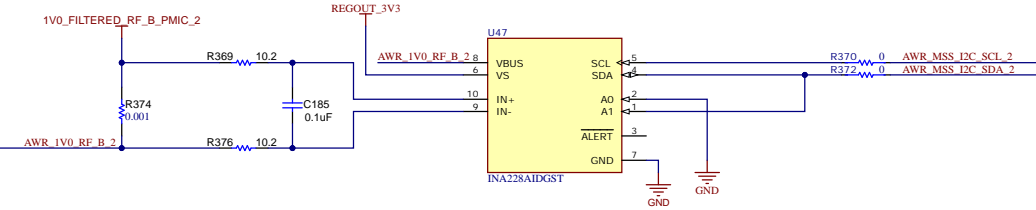
1.8V SUPPLY CURRENT SENSOR  
I2C ADDRESS 0x46



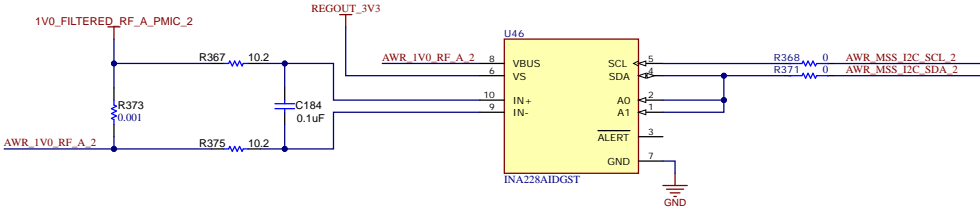
3.3V SUPPLY CURRENT SENSOR  
I2C ADDRESS 0x47



1.0V RFB SUPPLY CURRENT SENSOR  
I2C ADDRESS 0x48

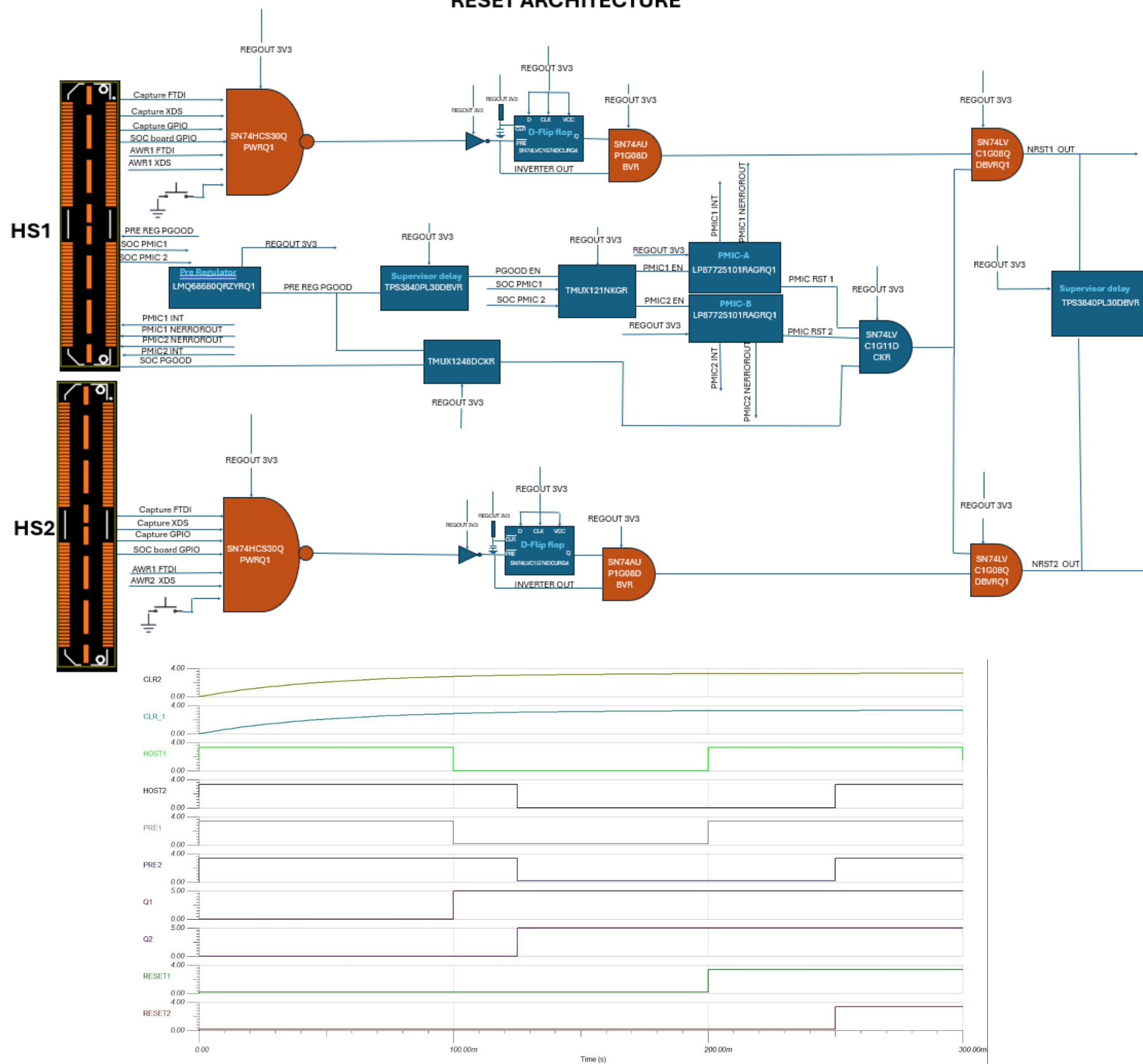


1.0V RFA SUPPLY CURRENT SENSOR  
I2C ADDRESS 0x4A



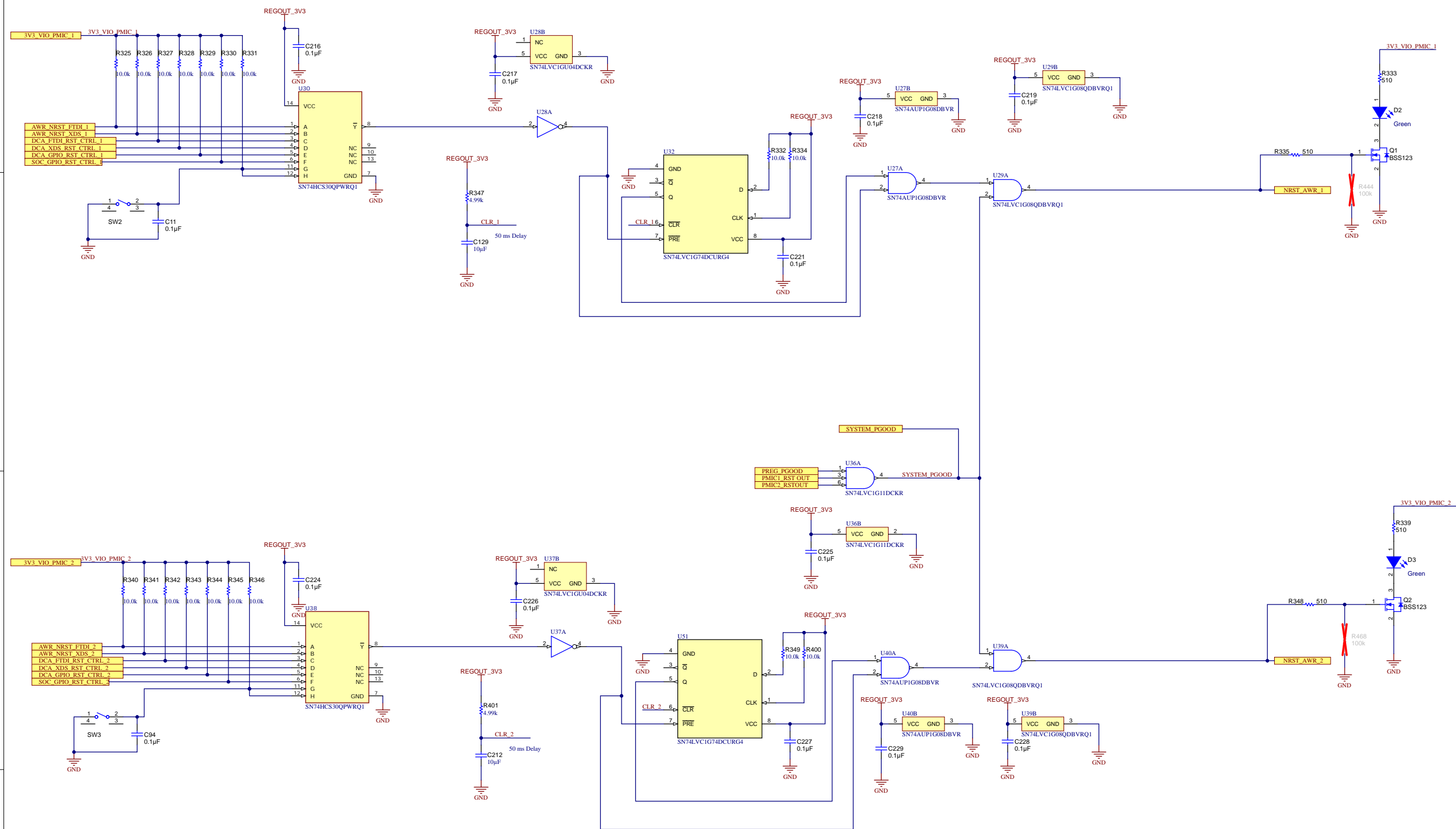


## RESET ARCHITECTURE





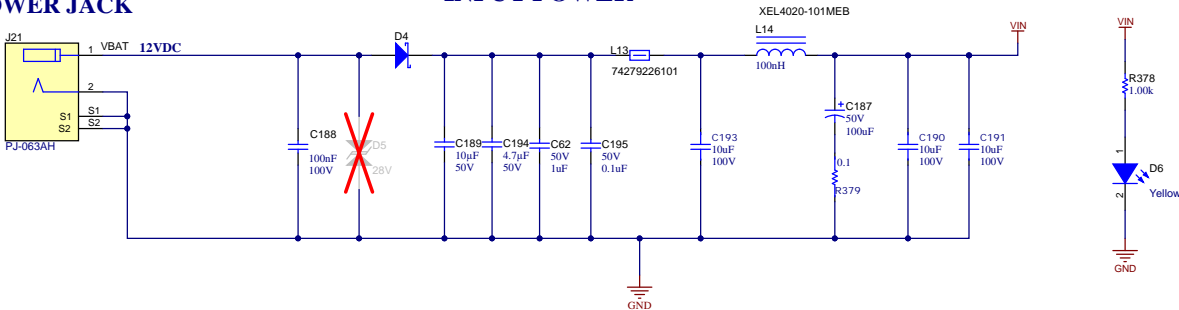
## RESET SELECTION



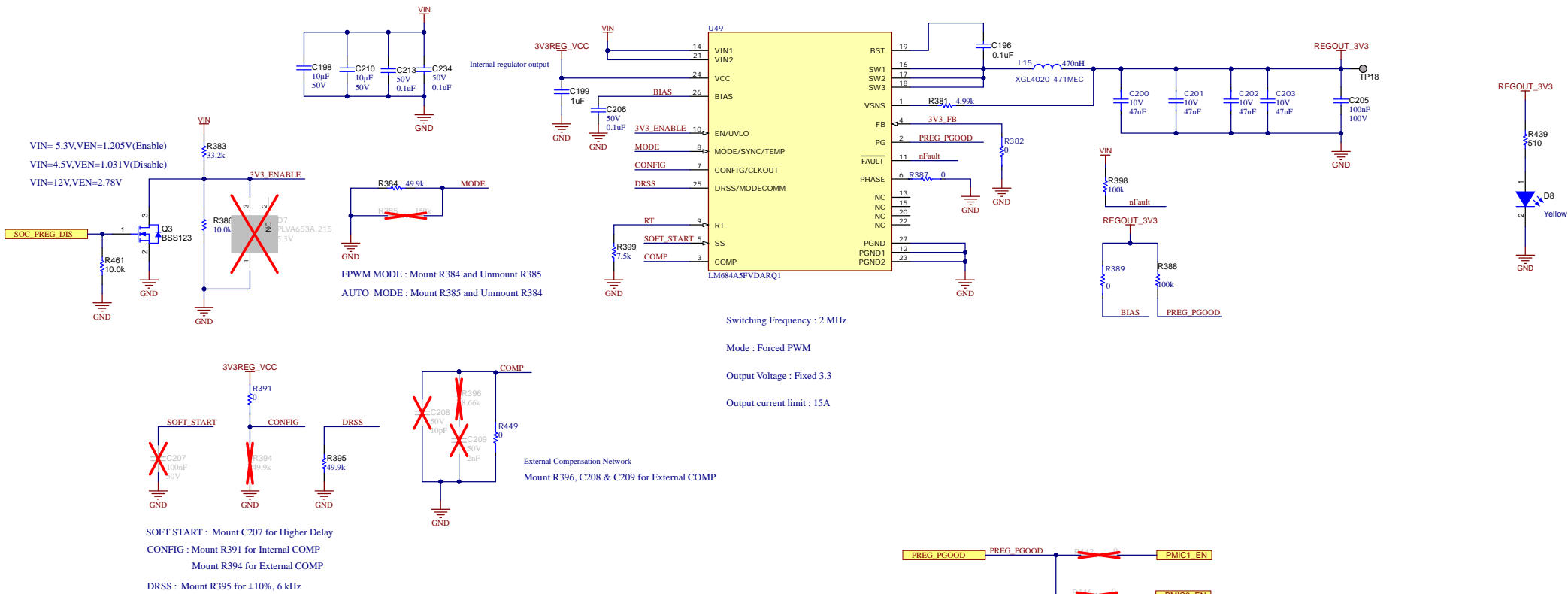


POWER JACK

INPUT POWER



3V3 SUPPLY REFERENCE



Switching Frequency : 2 MHz

Mode : Forced PWM

Output Voltage : Fixed 3.3

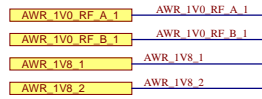
Output current limit : 15A

External Compensation Network  
Mount R396, C208 & C209 for External COMP

SOFT START : Mount C207 for Higher Delay  
CONFIG : Mount R391 for Internal COMP  
Mount R394 for External COMP  
DRSS : Mount R395 for  $\pm 10\%$ , 6 kHz



For IF bandwidth  $< 17.6 \text{ MHz}$  the secondary LC filter is not needed



Connect C71 and C72 directly to the AGND pad of the PMIC

Connect AGND to PGND in inner layer GND. In any case, PGND should not be connected to power pad on layer on which PMIC is placed



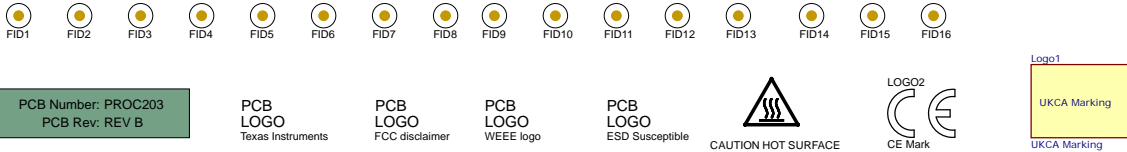
For IF bandwidth  $< 17.6\text{MHz}$  the secondary LC filter is not needed



Connect AGND to PGND in inner layer GND. In any case, PGND should not be connected to power pad on layer on which PMIC is placed







LBL1  
PCB Label  
THT-14-423-10  
Size: 0.65" x 0.20"

ZZ1  
Label Assembly Note  
This Assembly Note is for PCB labels only

ZZ2  
Assembly Note  
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3  
Assembly Note  
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4  
Assembly Note  
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Variant/Label Table	
Variant	Label Text
001	AWR2188LOPEVM



REVISION B HISTORY

- 1.Added a 10k pull down on AWR\_DIG\_SYNCIN\_1/2
- 2.Removed SW5 and C51 ,Shorted PRE\_PGOOD to PGOOD\_EN through a 0ohm
- 3.Added a pull down on Q3 gate
- 4.Added 0 ohms on the CSI lanes
- 5.Removed the back up RESET circuitry (RESET Supervisor), R421,R423,R422,R444,R350 and R351
- 6. Added MUX selection between SPI and I2C instead of 0ohm resistors
- 7.Added Buffer for System\_PGOOD,NERROR\_OUT 1/2 and RESET Signals from the DCA & SOC boards to avoid toggling RESET
- 8.Removed U48,U35 and directly connected the preg\_pgood signal to AND gate input and removed SW4 & SOCP\_GOOD signal
- 9.Given 0 ohms connection for PMIC1\_EN and PMIC2\_EN from PREG\_PGOOD and made DNP
- 10.Changed pullups from 100k to 10k in input and output of buffer
- 11.Renamed SOC\_PMIC1/2\_EN and SOC\_PREG\_EN to SOC\_PMIC1/2\_DIS & SOC\_PREG\_DIS
- 12.Added MOSFET for SOC\_PMIC1/2\_DIS
- 13.Changed the reset signals netname coming from DCA and SOC boards
- 14.Added 100k pull down for system pgood mosfet and NRESET mosfet (Made DNI)