TPS548x23_PSPICE_Transient_Model_Features_and_Limitations

A. Features Modeled

1. TPS548623, TPS548A23, TPS548B23 device variants are supported. VIN = 4 V to 16 V; IOUT = 100 mA to 6 A (TPS548623), 12 A (TPS548A23), 20 A (TPS548B23)

2. Output voltage can be configured using the VFB_CONFIG parameter. Switching frequency, soft-start time, Mode (PFM/FCCM) and overcurrent limit can be configured using Schematic parameters.

3. Output overvoltage and undervoltage protection behavior is modeled.

B. Features Not Modeled

1. Operating quiescent current.

2. Shutdown current.

3. Thermal shutdown and other temperature-dependent characteristics.

4. Inverting topologies. The model is intended for the grounded, non-inverting buck configuration shown in the supplied testbench

APPLICATION NOTES

1. The TPS548x23 model is encrypted and requires Cadence PSpice version 17.4 or later.

2. The reference design is based on the TPS548B23 EVM schematic and uses similar input-voltage, output-voltage, and load conditions.

3. The supplied testbench is configured for VIN = 12 V, VOUT = 1.0 V, and IOUT = 20 A for each simulated output.

4. The model has been corner tested over VIN = 4 V to 16V and IOUT = 100 mA to the rated output current of each variant (6 A TPS548623, 12 A TPS548A23, 20 A TPS548B23). Operation outside these ranges has not been validated.

5. Select exactly one device variant by setting its parameter to 1 and the other two parameters to 0:

TPS548A23: TPS548A23=1, TPS548B23=0, TPS548623=0

TPS548B23: TPS548A23=0, TPS548B23=1, TPS548623=0

TPS548623: TPS548A23=0, TPS548B23=0, TPS548623=1

6. Set STEADY_STATE=0 to observe the complete startup sequence. Set STEADY_STATE=1 to shorten the startup interval and reach steady state more quickly. Do not use STEADY_STATE=1 when evaluating startup timing or startup waveforms.

7. Select VFB_CONFIG (0 for internal FB divider and 1 for external FB divider), T_SS, FSW, OCL, Mode (set to 1 to enable PFM, set to 0 for FCCM) according to the device datasheet and the intended operating configuration. For TPS548623 the overcurrent limit (10 A valley), negative current limit (4 A) and power-stage on-resistance (21 mΩ / 7 mΩ) are fixed inside the model; the OCL and NOCL schematic parameters are not used.

8. Modeled behavior includes output-voltage programming, switching-frequency and control-loop configuration, FCCM/DCM mode selection, overcurrent protection, soft start, PGOOD, output overvoltage and undervoltage protection, and enable behavior.

9. When a modeled PVIN overvoltage, VOUT undervoltage, or VOUT overvoltage fault is configured as latching, the device remains disabled until the simulation is restarted after the fault condition has been removed.

10. Operating quiescent current, shutdown current, thermal shutdown, temperature-dependent characteristics, telemetry, and input-power monitoring are not modeled.

11. The supplied transient simulation runs for 1.8ms and requires approximately 10 minutes on a four-core, 2.8 GHz computer. Actual runtime depends on the computer, PSpice version, simulation settings, and saved waveform count.