

TPS544x28 PSpice Transient Model

Features, Application Notes, and Limitations

Devices covered	TPS544B28, TPS544A28, TPS544B26, TPS544A26 (one .OLB symbol)
Simulator	Cadence PSpice 17.4 or later
Model scope	Single-phase transient operation (non-inverting buck)
Default testbench	VIN = 12 V, VOUT = 1.0 V, IOU = 0 A to 20 A (load step)
Validated range	VIN = 4 V to 16 V; IOU = 100 mA to 20 A

A. Features Modeled

- 1 TPS544B28, TPS544A28, TPS544B26, and TPS544A26 device variants are supported.
- 2 Output voltage can be configured using the internal feedback divider (INT_FB=1) or an external feedback network (INT_FB=0).
- 3 Switching frequency, control-loop ramp selection, and soft-start time are configured through subcircuit parameters (FSW, RAMP, T_SS).
- 4 FCCM and auto-skip (Eco-mode / PFM) operating-mode behavior is configured through the MODE parameter.
- 5 Overcurrent protection (positive valley current limit) is configured through the OCL parameter, with a grade-dependent default (21 A for the B-grade, 13 A for the A-grade).
- 6 Low-side FET zero-crossing detection and low-side FET negative current limit are modeled.
- 7 Power-good behavior is modeled.
- 8 Output overvoltage protection (OVP) and undervoltage protection (UVP) behavior is modeled.
- 9 EN/VIN UVLO protection, BOOT functionality, and pre-bias startup are modeled.

B. Features Not Modeled

- 1 Operating quiescent current.
- 2 Shutdown current.
- 3 Thermal shutdown and other temperature-dependent characteristics.
- 4 Hiccup/latch-off fault-recovery behavior.
- 5 PMBus/I2C communication and telemetry. The ADR/MS1/MS2/SCL/SDA pins are placeholders (leave open); configuration is applied through subcircuit parameters, not by measuring strap resistors or the digital bus.
- 6 Output voltage discharge.
- 7 Multiphase operation and current sharing between multiple devices. Inverting topologies are not supported.

C. Application Notes

- 1 This PSpice transient model is encrypted and requires Cadence PSpice version 17.4 or later.
- 2 The reference design is based on the TPS544B28 EVM schematic and uses similar input-voltage, output-voltage, and load conditions.
- 3 The supplied testbench is configured for VIN = 12 V, VOUT = 1.0 V, and a 0 A to 20 A load-transient step.
- 4 The model has been corner tested over VIN = 4 V to 16 V and IOU = 100 mA to 20 A. Operation outside these ranges has not been validated.
- 5 One .OLB symbol represents all four orderable parts. Select the current-limit grade by setting exactly one of the two device-select parameters to 1 and the other to 0:
20 A grade (TPS544B28 / TPS544B26): TPS544B2x=1, TPS544A2x=0
12 A grade (TPS544A28 / TPS544A26): TPS544B2x=0, TPS544A2x=1

- 6 The 28 and 26 suffixes differ only in host interface (PMBus vs. I2C). The digital interface is not modeled, so within each current-limit grade the 28 and 26 devices behave identically in simulation.
- 7 Set STEADY_STATE=0 to observe the complete soft-start sequence. Set STEADY_STATE=1 to start pre-biased near regulation and reach steady state more quickly. STEADY_STATE=1 should not be used when evaluating startup timing or startup waveforms.
- 8 Configure FSW, MODE, VREF_CTRL, VOSCL, INT_FB, RAMP, T_SS, and OCL according to the device datasheet and the intended operating configuration. The ADR/MS1/MS2/SCL/SDA pins are placeholders and should be left open.
- 9 Modeled behavior includes output-voltage setting, programmable soft start, switching-frequency and mode selection, low-side zero-crossing detection, current sense and positive overcurrent protection, low-side negative current limit, power good, output overvoltage and undervoltage protection, EN/VIN UVLO, BOOT functionality, and pre-bias startup.
- 10 Operating quiescent current, shutdown current, thermal shutdown, temperature-dependent characteristics, hiccup/latch-off behavior, PMBus/I2C telemetry, and output-voltage discharge are not modeled.
- 11 The model supports single-phase operation only. Multiphase and inverting topologies are not supported.
- 12 The supplied transient simulation runs for 1.5 ms and requires approximately 15 minutes on a four-core, 2.8 GHz computer. Actual runtime depends on the computer, PSpice version, simulation settings, and saved waveform count.

Model-use guidance: This behavioral model is intended for transient evaluation of startup, steady-state switching behavior, configuration settings, and the supported protection functions. It is not intended for thermal, efficiency, quiescent-current, or telemetry analysis.