

J742S2/TDA4VPE/TDA4APE Evaluation Module

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REV	E2
VER	1.7

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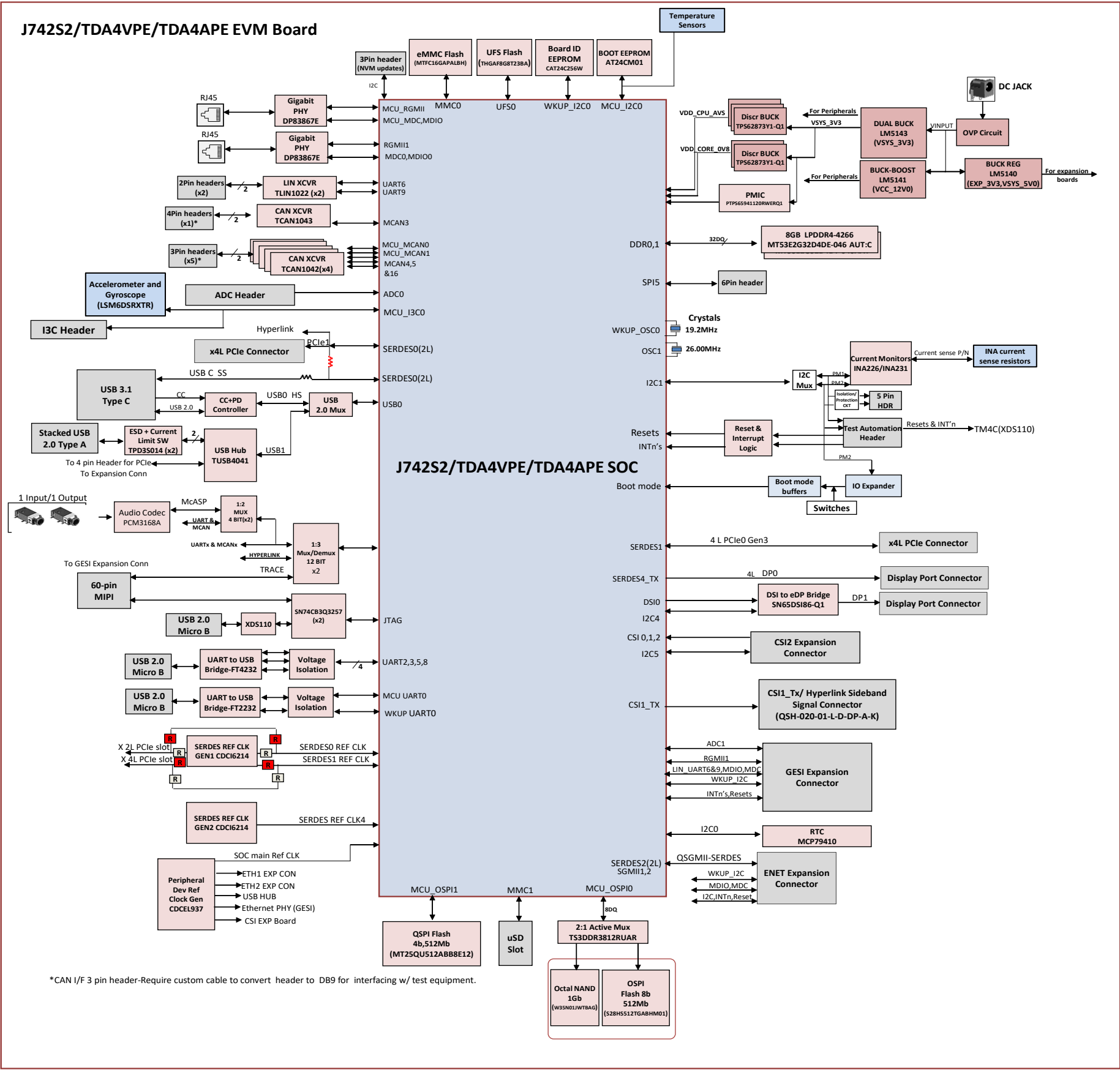
REVISION HISTORY #1

	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	0.1	14 DEC 2023	Updated SOC Symbol into TI Breakout schematics drafted from PROC141E4A. Deleted unused sections of the schematics; DDR2, DDR3, ENET-EXP-1, ENET-EXP-2, and corresponding SOC power sections	Mistral Design Team		
	0.2	19 DEC 2023	Deleted SERDES4 Rx testponints. Deleted unused 0.1uF caps on: VDD_CORE: C869, C987, C871, C956, C924, C771 VDD_CPU: C964, C961, C903 VDDSHV0_MCU: C1030 VDDSHV0: C945 VDDS_MMC0: C868 VDDSHV5: C975 VDDS_DDR: U50155, U50190, C1013, U50173, U50181, C946, U50182, U50180, C1061 VDDA_0P8_PLL_DDR2: C991, C1076, C1087, FL195	Mistral Design Team		
	0.3	24 JAN 2024	Updated TI review comments: SOC symbol SERDES PCIe clock out section is updated along with removal of symbol documentation	Mistral Design Team		
E1A	0.4	16 MAY 2024	Updated TI comments DNI - U229 and Populated U230	Mistral Design Team		
E1B	0.5	07 JUN 2024	Updated TI comments DNI - R49 to support TIVA	Mistral Design Team		
E2	0.6	19 AUG 2024	SCH updates aligned to "J7AHP EVM SoM PROC141E5 ECN1.xlsx" Remove optional 0.01uF Feed-Forward Caps on discrete TPS74501P-Q1 LDOs (U41, U66 & U85) to reduce Vo ramp-up times as follows: C192 for VDA_PHY_1V8_REG C274 for VDD_GPIORET_WK_0V8_REG C334 for VDD1_DDR_1V8_REG	TI Mistral Design Team		
	0.7	19 AUG 2024	Update BOM description to "NVM rev5 or higher" for TPS6594133A-Q1 PMIC (U68) to ensure: 1. VDA_DLL_0V8 is disabled at time = 1.0ms (due to ~1ms RC discharge < 0.6V FET Vgs) to disable VDD_CPU_AVS & VDD_CORE_0V8 at ~2.0ms. 2. VDD_MCU is enabled at least 0.5ms before VDD_CORE during pwr up seq per SOC's i2406 Errata. 3. WDog timer is enabled by NVM/default to avoid possibility a unit might never see a WDog timer flag if a fault (I2C) keeps SW from enabling Wdog Timer. Disabling WDog timer during pwr up seq needs a GPIO to latch a logic high (Rpu to VSYS_3V3) vs a low level (internal Rpdn to Gnd) keeps WDog enabled. So PMIC_WDOG_DISABLE net moved to GPIO9 from GPIO8 since a logic low on Main_Pwr_Grp_IRQn net would abort a pwr up seq. Added SCH note above existing "OR Gate Logic Table" on Discrete LDO page 33 as follows: "Alternative discrete OR gate circuit using Bipolar Junction Transistors (BJT) can be used instead of FETs for improved low temp robustness."	TI Mistral Design Team		
	0.8	19 AUG 2024	Updated Safety Voltage Suervisors (SVS-A, U87 & SVS-B, U89) as follows: 1. Remove net on SLEEP (pin 7) & connect to VDD (pin 8) supply per data sheet when not used. 2. Remove net on SYNC (pin 9) & make it a No Connect per data sheet when not used. 3. Remove net on ACT (pin 5) & connect to VDD supply using in-line 0-ohm R per typ data sheet use. 4. Replace power on VDD (pin 8) with VDD_MCUIO_3V3 using an in-line 0-ohm R. This allows an asserted IRQn to be reset by power cycling SVS if a MCU group fault occurs or the PMIC enters into safe recovery state & attempts to reinitialize the PMIC.	TI Mistral Design Team		
	0.9	19 AUG 2024	Add 1x 80.6-ohm resistor to TPS6594133A-Q1 PMIC's (U68) LDO3 Vo to a draw 10mA load at 0.8V. This ensures stability due to total capacitance > data sheet 20uF max value.	TI Mistral Design Team		
	1.0	19 AUG 2024	Add 1x thru-hole Test Point connected to GND & placed near OBSCLK0 TP93. Add note: "Place OBSCLK & GND TPs aligned with 100mil pitch to enable 2-pin header install for probing."	TI Mistral Design Team		
	1.1	19 AUG 2024	Update VPP_EFUSE_1V8 power rail supply source & SoC connection as follows: 1. Replace 300mA LDO TLV73318-Q1 (U67) with a more robust 500mA LDO TPS7A2118P-Q1. 2. Add 22uF, 0805 cap to Vo of new TPS7A2118P-Q1 as option for reducing transient noise. 3. Make R1016 a "Do Not Install" component in SCH & BOM since customers only access MCU Efuses.	TI Mistral Design Team		
	1.2	19 AUG 2024	I2C address of U229 connection is changed due to address conflict. Unconnected net (A0) of U83 is been updated.	Mistral Design Team		
	1.3	19 AUG 2024	Tulip Buck comp values optimized per AHP load step results VDD_CPU_AVS: 3-Ph buck converters (U35, 36 & 37) comp R & C values: 1. Replace R186 value from 1.8k to 2.4k 2. Replace C155 value from 3,300pF to 1,500pF VDD_CORE_0V8: 2-Ph buck converters (U42, 48) comp R & C values: 3. Replace R247 value from 1.8k to 1.2k 4. Replace C189 value from 3,300pF to 4,700pF 5. Replace C198 & 226 value from 10pF to 20pF	TI Mistral Design Team		
	1.4	19 AUG 2024	U10 IC - DIR pin connected to GND to support TIVA.	TI Mistral Design Team		
	1.5	19 AUG 2024	Change R673 Rpu to connect to VSYS_3V3 to enable latching a logic high on PMIC_WDOG_DISABLE net. Add R2400 10k Rpu to VCCA_3V3 connected to MCU_PWRGRP_IRQn net for initial testing of SVS-B.	TI Mistral Design Team		
	1.6	20 AUG 2024	Added J58 - ENET Expanison Connector	TI Mistral Design Team		
	1.7	11 SEP 2024	Populated Caps - C1290,C2582,C2583,C2584,C2585,C1292,C1293 to align with the latest ECN.	TI Mistral Design Team		

REVISION HISTORY #2

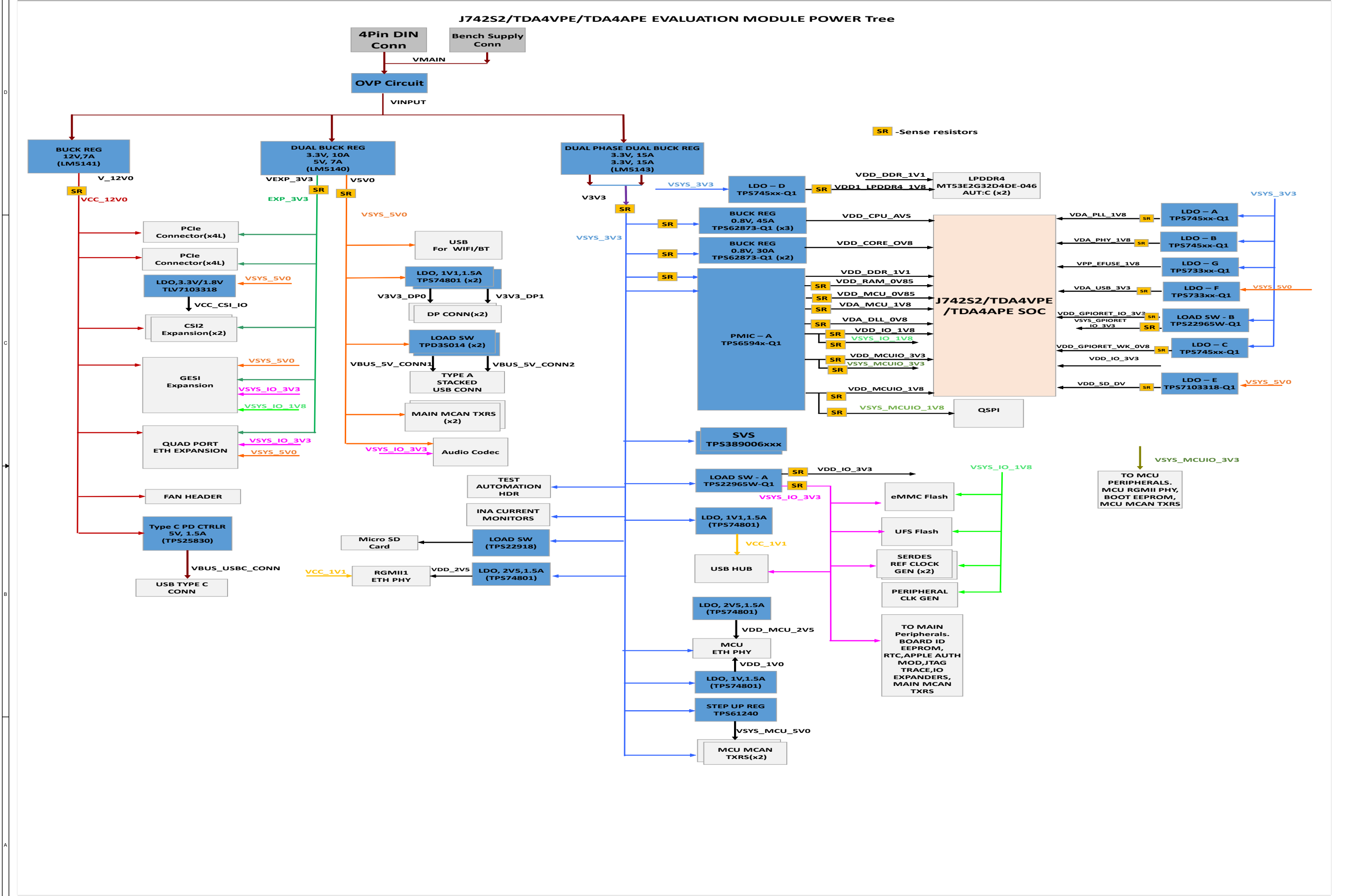
Project : J7 EVM			Title REVISION HISTORY			
			Size	PROC184 002		Rev
			C			E2
			Date:	Thursday, August 22, 2024		Sheet 3 of 85

BLOCK DIAGRAM



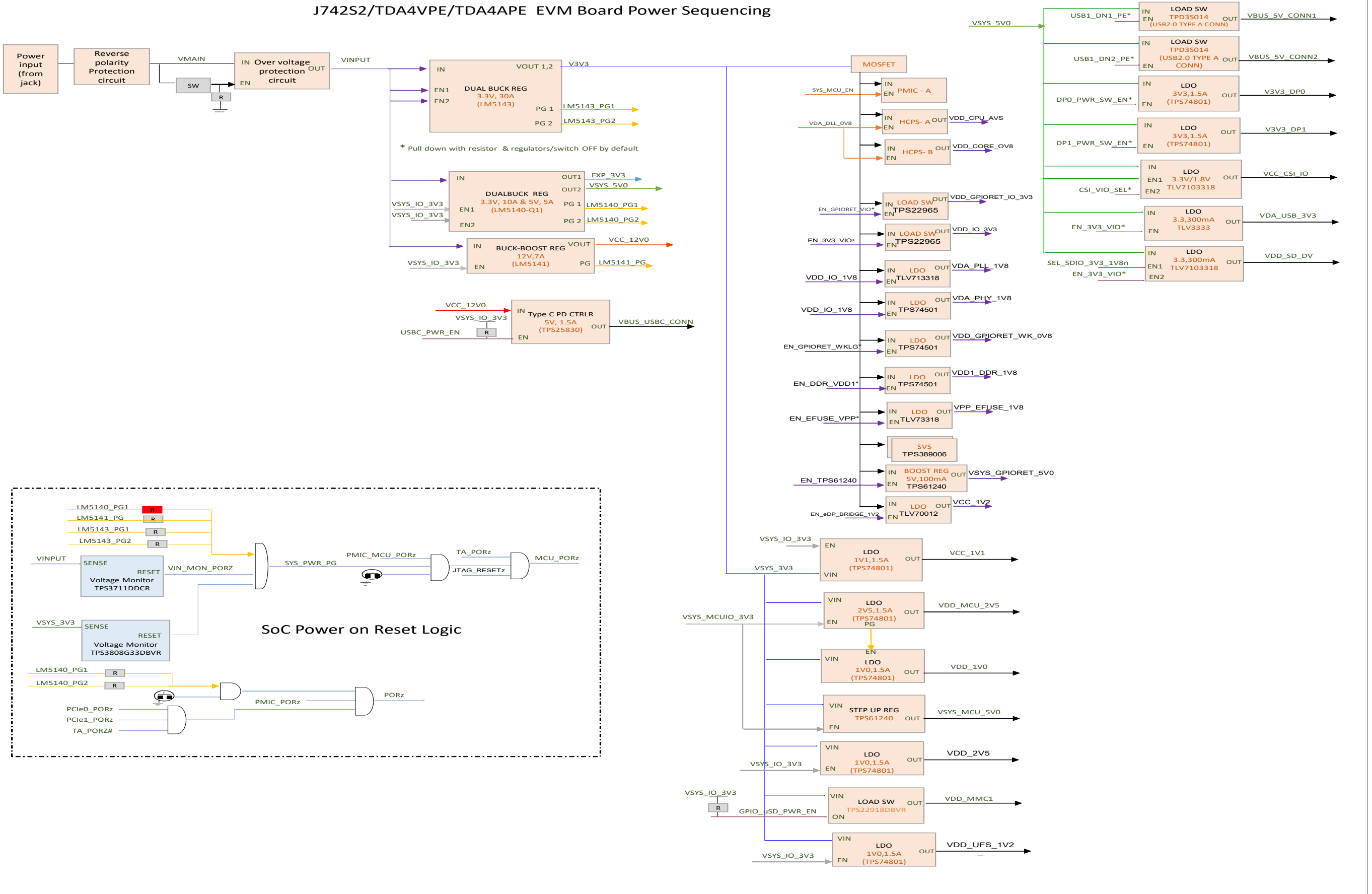
POWER FLOW DIAGRAM

J742S2/TDA4VPE/TDA4APE EVALUATION MODULE POWER Tree




POWER SEQUENCE

J742S2/TDA4VPE/TDA4APE EVM Board Power Sequencing

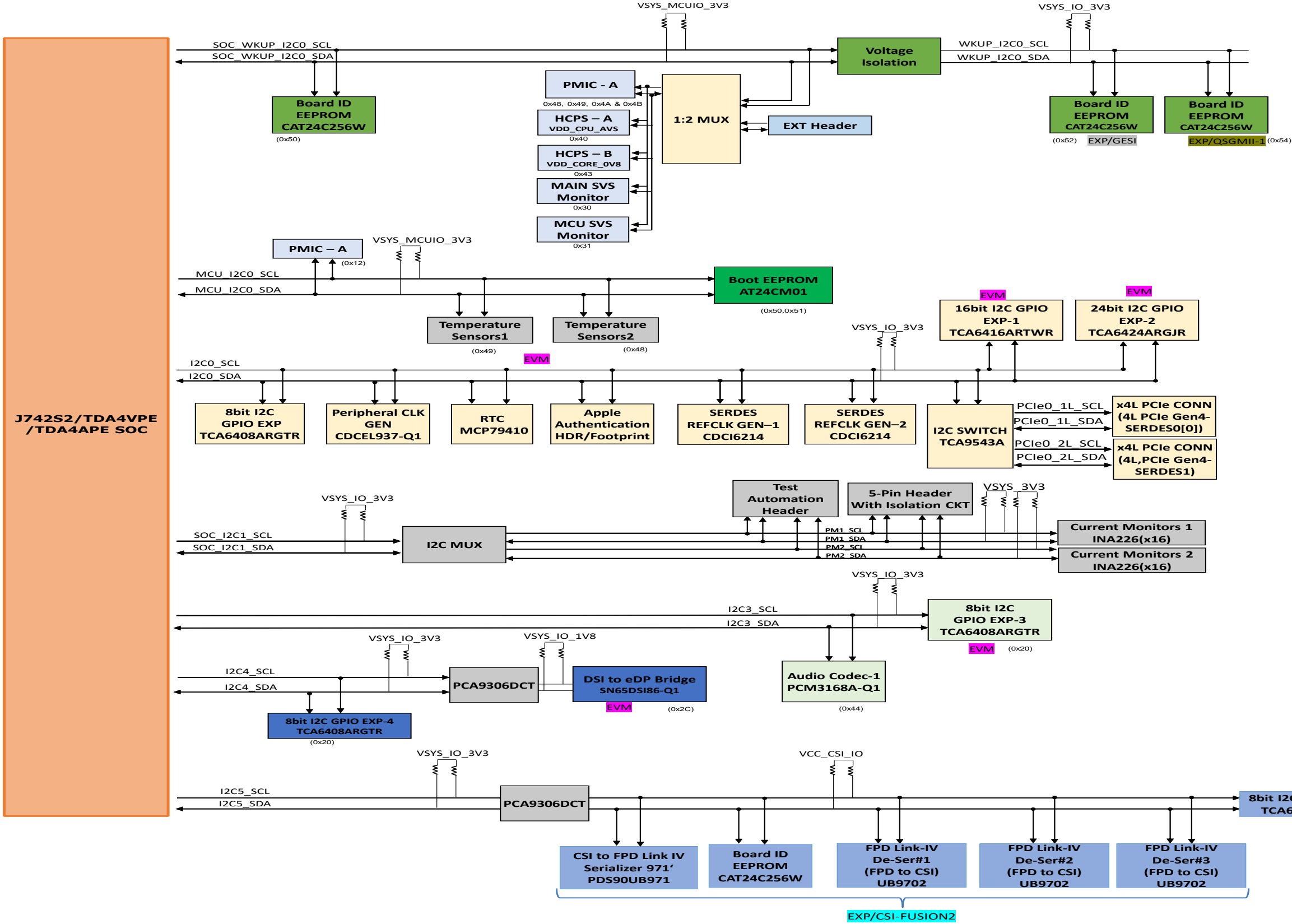


PDN

“Refer to PDN file entitled 'J742S2 Single Leo Dual HCPS PDN-3A v0.26' which is included in the released design zip file.”
“The J742S2 EVM SCH & PCB have implemented the PDN-3A variant that supports all PDN features & low power modes.”

Project : J7 EVM		Title PDN			
		Size	PROC184 002		Rev
		C			E2
		Date:	Tuesday, October 08, 2024		Sheet 7 of 85

I2C TREE



I2C TABLE

Board	Interface name	Part#	Address	J7AHP27 Port mapping
EVM	Board ID EEPROM	CAV24C256WE-GT3	0x50	WKUP_I2C0
EXP/GESI	Board ID EEPROM	CAT24C256W	0x52	
EXP/QSGMII	Board ID EEPROM	CAT24C256WI-GT3	0x54	
EVM	PMICs	PMIC A: TPS659413	PMIC A: 0x48, 0x49, 0x4A & 0x4B	
EVM	Tulip - VDD_CPU_AVS Regulator	TPS62873	0x40	
EVM	Tulip - VDD_CORE_OV8 Regulator	TPS62873	0X43	
EVM	MAIN SVS Monitor	PPS38900603NRTERQ1	0X30	
EVM	MCU SVS Monitor	PPS38900603NRTERQ1	0X31	
EVM	Temperature Sensors	TMP100NA/3K	0x48, 0x49	MCU_I2C0
EVM	Boot EEPROM	AT24CM01	0x50, 0x51	
EVM	I2C Switch for PCIe	TCA9543APWR	0x70	Main I2C0
EVM	RTC Clock	MCP79410-I/SN	0x57,0x6F	
EVM	SerDes Clock gen #1 Optional	CDCI6214	Optional	
EVM	SerDes Clock gen #2	CDCI6214	0x77,0x76	
EVM	Pheriphal Clock Gen	CDCEL937-Q1	0x6D	
EVM	16bit I2C GPIO EXPANDER1	TCA6424ARGJR	0x20	
EVM	24bit I2C GPIO EXPANDER2	TCA6424ARGJR	0x22	
EVM	8 bit I2C GPIO Expander4	TCA6408ARGTR	0x20	Main I2C4
EVM	DSI TO eDP BRIDGE	SN65DSI86IPAPQ1	0x2C	
EVM	DSI FPC Connector	<connector interface>		
EVM	I2C Switch for Automation header		0x22	Main I2C1
EVM	Current Monitors and Header		0x40 to 0x4F	
EVM	8bit GPIO Expander3	TCA6408ARGTR	0x20	Main I2C3
EVM	AUDIO IF Codec	PCM3168A-Q1	0x44	
EXP	8bit GPIO Expander5	TCA6408ARGTR	0x20	Main I2C5
EXP/CSI-FUSION2	Board ID EEPROM (Fusion2 Serial Capture)	CAT24C256W	0x52	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #1 (FPD to CSI)	UB9702	0x3D	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #2 (FPD to CSI)	UB9702	0x30	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #2 (FPD to CSI)	UB9702	0x32	
EXP/CSI-FUSION2	CSI to FPD Link IV Serializer 971	UB971	0x18	

GPIO EXPANDER MAP/TABLE

J742S2 EVM - GPIO Mapping Table						
WKUP Domain						
Net name	J742S2Mapping					
	Package Signal Name	GPIO Number	Input/Output	Default	State	Remarks
EN_EFUSE_VPP	WKUP_GPIO0_54	WKUP_GPIO0_54	Output	BOOTMODE	Active High	VPP_EFUSE_LDO enable
BOOT_EEPROM_WP	WKUP_GPIO0_1	WKUP_GPIO0_1	Output	BOOTMODE	Active High	Boot_EEPROM_Write protect
MCU_CAN1_STB	WKUP_GPIO0_2	WKUP_GPIO0_2	Output	BOOTMODE	Active High	MCU_CAN1_Standby
GPIO_MCU_RGMII1_RST#	WKUP_GPIO0_56	WKUP_GPIO0_56	Output	BOOTMODE	Active low	MCU_RGMII1_Reset
SYS_IRQz	WKUP_GPIO0_7	WKUP_GPIO0_7	Input	PU	Active low	Push-button Interrupt, User Defined/Wake S2R ('0'>'1' - interrupt pending, '1' - normal operation)
OSPI/HYPER_MUX_SEL	WKUP_GPIO0_6	WKUP_GPIO0_6	Output	DIP_SEL	NA	Flash Memory Selection ('0' - OSPI0, '1' - OCTAL NAND)
PMIC_MCU_INT# / H_MCU_INT#	MCU_OSP11_CSN1	WKUP_GPIO0_39	Input	PU	Active low	Interrupt from PMIC
MCU_RGMII1_INT#	WKUP_GPIO0_3	WKUP_GPIO0_3	Input	PU	Active Low	MCU_Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
SYS_MCU_PWRDN	MCU_SPI0_D0	WKUP_GPIO0_55	Output	BOOTMODE	Active low	System Power Down ('0' - normal operation, '1' - system power down)
MCU_CAN0_STBz	MCU_SPI0_D1	WKUP_GPIO0_69	Output	BOOTMODE	Active low	MCU_CAN0_Standby
LSM6DSOX_INT/LSM6DSRX_INT	WKUP_GPIO0_57	WKUP_GPIO0_57	Input	BOOTMODE	NA	Interupt from I3C Gyroscope sensor(*LSM6DSRX)
PM_I2C_SEL	WKUP_GPIO0_66	WKUP_GPIO0_66	Output	BOOTMODE	Active High	PM_I2C_Mux selection, ('0' - SOC_I2C2_SCL/SDA -> PM1_SCL/SDA, '1' - SOC_I2C2_SCL/SDA -> PM2_SCL/SDA)
USBC_DIR_SOC	MCU_OSP10_CSN1	WKUP_GPIO0_28	Input	PU	Active High	USB_C direction pin
ENET_EXP_INTB	MCU_ADC1_AIN5	WKUP_GPIO0_84	Output	PU	Active low	ENET_expansion Interrupt signal
I2C0_IOEXP_INT#	MCU_ADC1_AIN7	WKUP_GPIO0_86	Output	PU	Active Low	I2C0_IO_expander interrupt signal
CANIO_RET_WAKE	MCU_SPI0_CS0	WKUP_GPIO0_70	Input	PU	NA	Push-button wake signal
Main Domain						
MAIN_RET_WAKE	GPIO0_11	GPIO0_11	Input	PU	NA	Push-button wake signal
HYP1_RXFLCLK_MUX	MCASP0_AXR2	GPIO0_18	Input	PU	Active Low	I2C5_IO_expander interrupt, Muxed with trace and Hyperlink signals
SEL_SDIO_3V3_1V8n	MCAN15_RX	GPIO0_8	Output	NA	Active low	SW_controls & transition Sd card to high speed 1.8V signaling if card type supports
CSI2_EXP_A_GPIO2(MCASP4_AXR1/T_RC_DATA16_MUX)	MCAN0_RX	GPIO0_26	I/O	NA	NA	CSI2_Expansion Board Specific, Muxed with trace and Hyperlink signals
CSI2_EXP_A_GPIO4(MCASP4_AXR3/T_RC_DATA5_MUX)	MCAN1_RX	GPIO0_28	I/O	NA	NA	CSI2_Expansion Board Specific, Muxed with trace and Hyperlink signals
TRC_DATA0_MUX	MCAN13_TX	GPIO0_3	Input	PU	NA	Interrupt signal from DSI to eDP bridge
SOC_GPIO0_21_MUX	MCASP2_ACLKX	GPIO0_21	Input	PU	Active Low	RGMII1_INT signal
GPIO Expander - 1 Part#TCA6416ARTWR						
I2C0/0x20	P00	PCIe1_2L_MODE_SEL	Input	DIP_SEL	NA	PCIe1_4-Lane Mode Select ('0' - Root Complex, '1' - End Point)
	P01	PCIe1_4L_PERSTz	Input	PD	Active low	PCIe1_4-Lane Bus Reset ('0' - device reset, '1' - normal operation)
	P02	PCIe1_2L_RC_RSTz	Output	PD	Active low	PCIe1_4-Lane RC Reset Control ('0' - device reset, '1' - normal operation)
	P03	PCIe1_2L_EP_RST_EN	Output	PD	Active low	PCIe1_4-Lane EP Reset Enable ('0' - PERSTz isolated from PORz, '1' PERSTz connected to PORz)
	P04	PCIe0_4L_MODE_SEL	Input	DIP_SEL	NA	PCIe0_2-Lane Mode Select ('0' - Root Complex, '1' - End Point)
	P05	PCIe0_4L_PERSTz	Input	PD	Active low	PCIe0_2-Lane Bus Reset ('0' - device reset, '1' - normal operation)
	P06	PCIe0_4L_RC_RSTz	Output	PD	Active low	PCIe0_2-Lane RC Reset Control ('0' - device reset, '1' - normal operation)
	P07	PCIe0_4L_EP_RST_EN	Output	PD	Active low	PCIe0_2-Lane EP Reset Enable ('0' - PERSTz isolated from PORz, '1' PERSTz connected to PORz)
	P10	PCIe1_4L_PRSENT#	Input	PU	Active High	PCIe1_4-Lane Hot Plug/Card Detect ('0' - PCIe Card Detected, '1' - no card detected)
	P11	PCIe0_4L_PRSENT#	Input	PU	Active High	PCIe0_2-Lane Hot Plug/Card Detect ('0' - PCIe Card Detected, '1' - no card detected)
	P12	CDC11_OE1/OE4	Output	PU	Active High	PCIE_2L_Reference_Clock_Enable ('0 - clock disabled, '1' - clock enabled)
	P13	CDC11_OE2/OE3	Output	PU	Active High	PCIE_1L_Reference_Clock_Enable ('0 - clock disabled, '1' - clock enabled)
	P14	AUDIO_MUX_SEL	Output	PU	Active High	Mux select for McASP and trace signals
	P15	EXP_MUX2	Output	NA	NA	Expansion Board Mux control1 GESI - MDIO_MDC_SEL0
	P16	EXP_MUX3	Output	NA	NA	Expansion Board Mux control1 GESI - MDIO_MDC_SEL1
	P17	GESI_EXP_PHY_RSTz	Output	PU	Active High	EXP_RSTz - Terminated with Test point
GPIO Expander - 2 Part#TCA6424ARGJR						
I2C0/0x22	P00	R_GPIO_RGMII1_RST	Output	PU	Active low	Routed to INFO/GESI expansion connector, GESI - Used for GPIO_PRG0_RGMII1_RST; INFO - Not used
	P02	GPIO_USD_PWR_EN	Output	PU	Active High	MicroSD Card Power Enable ('0' - power off, '1' - power on)
	P03	USBC_PWR_EN	Output	PU	Active High	USB-TypeC VBUS Controller Power Enable ('0' - power off, '1' - power on)
	P04	USBC_MODE_SEL1	Output	DIP_SEL	NA	USB-Type C Mode Select
	P05	USBC_MODE_SEL0	Output	DIP_SEL	NA	USBC_MODE_SEL[1:0]: '00' =DFP, '01' =DRP, '1x' =UFP
	P06	GPIO_LIN_EN	Output	PD	Active High	LIN transceiver enable
	P07	R_CAN_STB	Output	PU	Active High	Standby signals for On BOARD and GESI CAN Transceiver
	P10	CTRL_PM_I2C_OE#	Output	PD	Active High	Gate drive for enable signal of PM_I2C_mux select
	P13	CDC12_RSTZ	Output	PU	Active low	Peripheral Clock Generator ('0' - device reset, '1' - normal operation)
	P14	USB2.0_MUX_SEL	Output	PD	Active High	Signal Mux Control ('0' - USBC, '1' - USB Hub)
	P15	CANUART_MUX_SEL0	Output	PD	Active High	Select line for both the CANUART_MUX
	P16	CANUART_MUX2_SEL1	Output	PU	Active High	Select line for CANUART_MUX2
	P17	CANUART_MUX1_SEL1	Output	PU	Active High	Select line for CANUART_MUX1
	P20	ENET_EXP_PWRDN	Output	PU	Active High	Ethernet Expansion1_PHY Powerdown ('0' - normal operation, '1' - device power down)
	P21	ENET_EXP_RESETZ	Output	PD	Active low	Ethernet Expansion1_Reset ('0' - device reset, '1' - normal operation)
	P22	ENET_I2CMUX_SEL	Output	PD	NA	Signal Mux Control ('0' - No Connect, '1' - I2C0)
	P23	ENET_EXP_SPARE2	Output	NA	Active low	Ethernet Expansion Spare2 ('0' - not defined, '1' - not defined)
	P25	USER_INPUT1	Input	DIP_SEL	NA	User Dip Switch Input1 ('0' - User Define, '1' - User Define)
	P26	USER_LED1	Output	PD	Active High	User LED1 Enable ('1' - LED Off, '0' - LED On)
	P27	USER_LED2	Output	PD	Active High	User LED2 Enable ('1' - LED Off, '0' - LED On)
GPIO Expander - 3 Part#TCA6408ARGTR						
I2C3/0x20	P0	CODEC_RSTZ	Output	PD	Active low	Audio Codec Reset ('0' - device reset, '1' - normal operation)
	P1	CODEC_SPARE1	NA	UNUSED	NA	Not used (test point)
GPIO Expander - 4 Part#TCA6408ARGTR						
I2C40x20	P0	DP0_PWR_SW_EN	Output	PD	Active High	DisplayPort0 Power Enable ('0' - power off, '1' - power on)
	P1	DP1_PWR_SW_EN	Output	PD	Active High	DisplayPort1 Power Enable ('0' - power off, '1' - power on)
	P2	GPIO_eDP_ENABLE	Output		Active High	DSI to eDP bridge enable
GPIO Expander - 5 Part#TCA6408ARGTR						
I2C5/0x20	P0	CSI2_EXP_RSTZ	Output	PD	Active low	CSI2_Expansion Interface Reset ('0' - device reset, '1' - normal operation)
	P1	CSI2_EXP_A_GPIO0	IO	NA	NA	CSI2_Expansion Board Specific.
	P2	CSI2_EXP_A_GPIO1	IO	NA	NA	CSI2_Expansion Board Specific.
	P3	CSI2_EXP_A_GPIO3	IO	NA	NA	CSI2_Expansion Board Specific.
	P4	CSI2_EXP_B_GPIO1	IO	NA	NA	CSI2_Expansion Board Specific.
	P5	CSI2_EXP_B_GPIO2	IO	NA	NA	CSI2_Expansion Board Specific.
	P6	CSI2_EXP_B_GPIO3	IO	NA	NA	CSI2_Expansion Board Specific.
	P7	CSI2_EXP_B_GPIO4	IO	NA	NA	CSI2_Expansion Board Specific.

Project :

J7 EVM



Title
GPIO_EXPANDER_MAP/TABLE

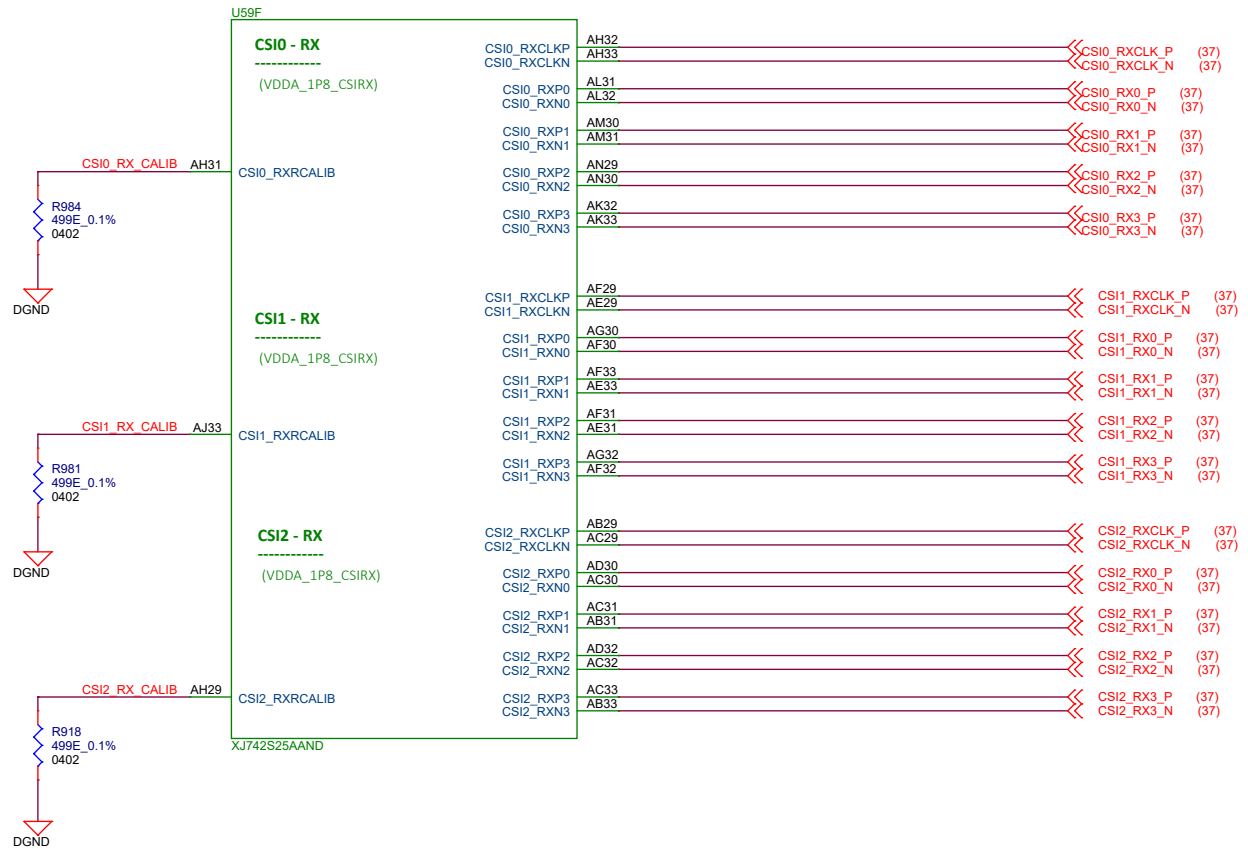
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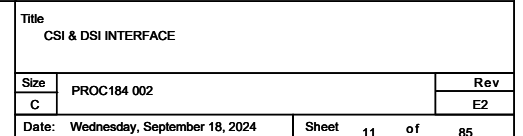
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CSI

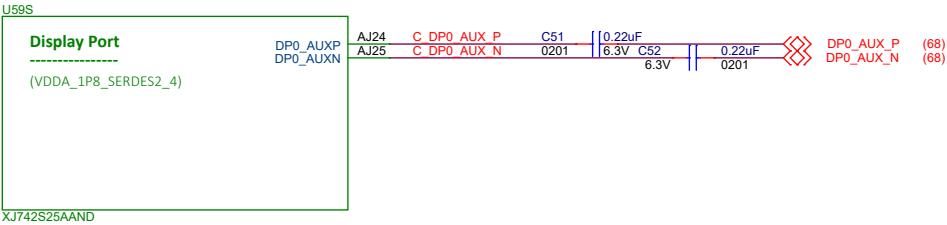
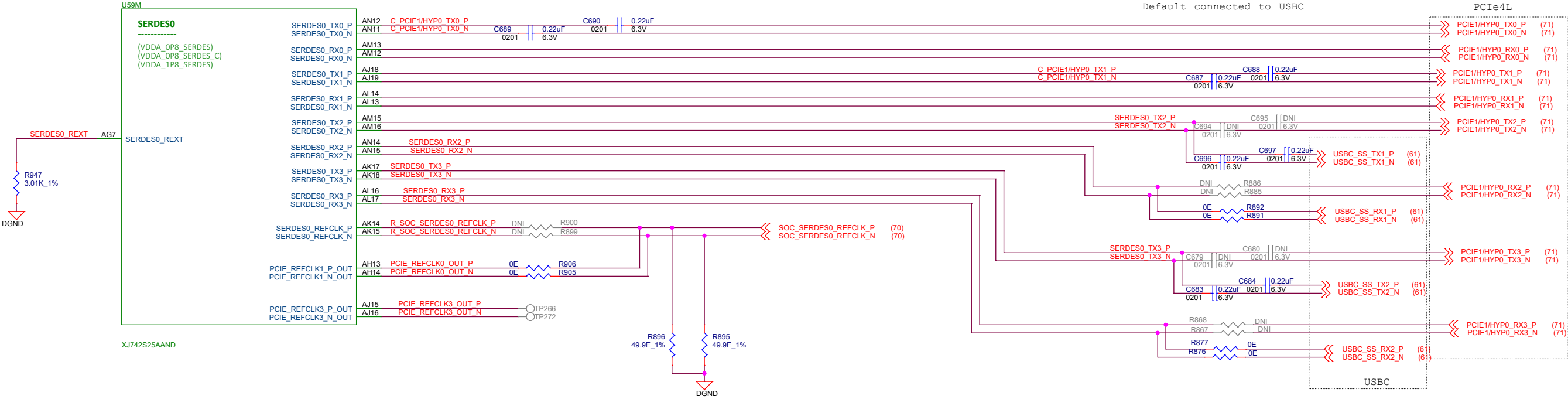


J7 EVM

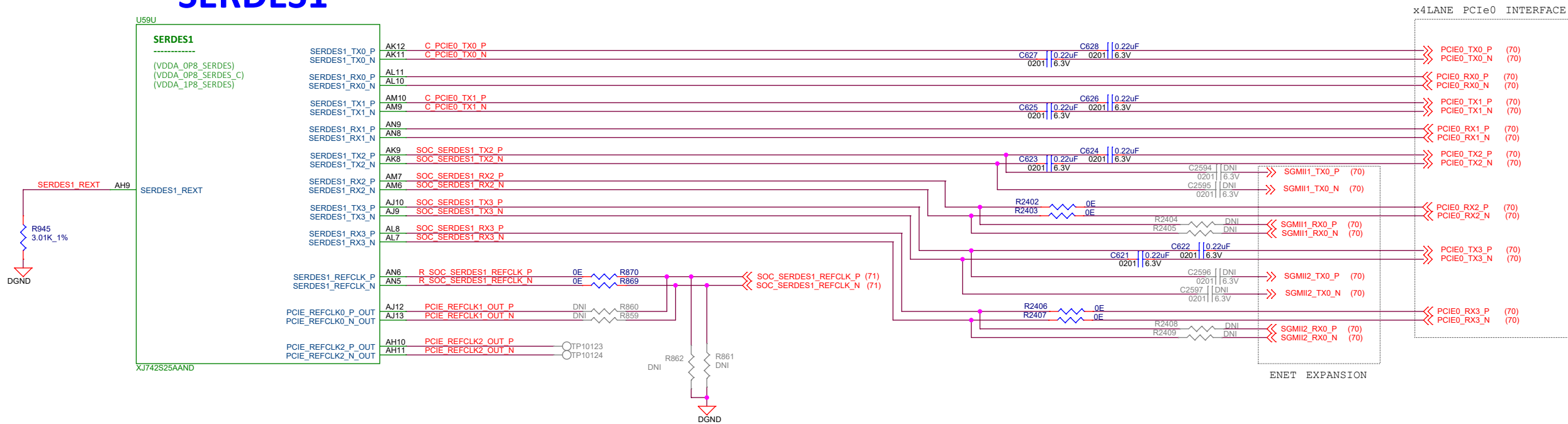


SERDES0

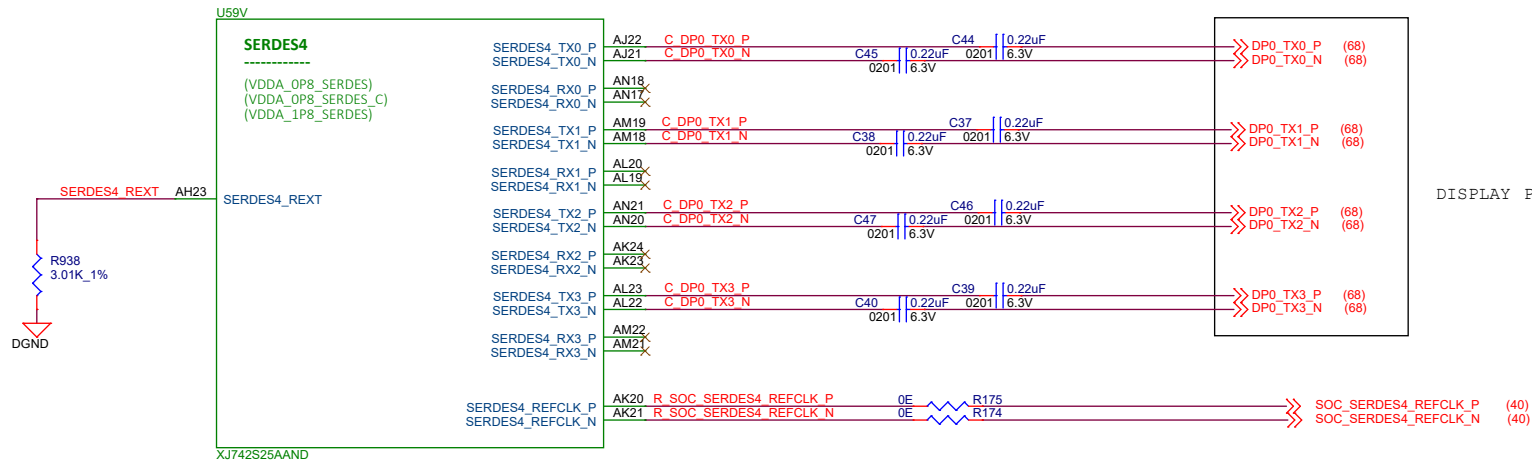
Dedicated 2L to PCIe4L connector, x2L
will be resistor muxed with USBC
Default connected to USBC



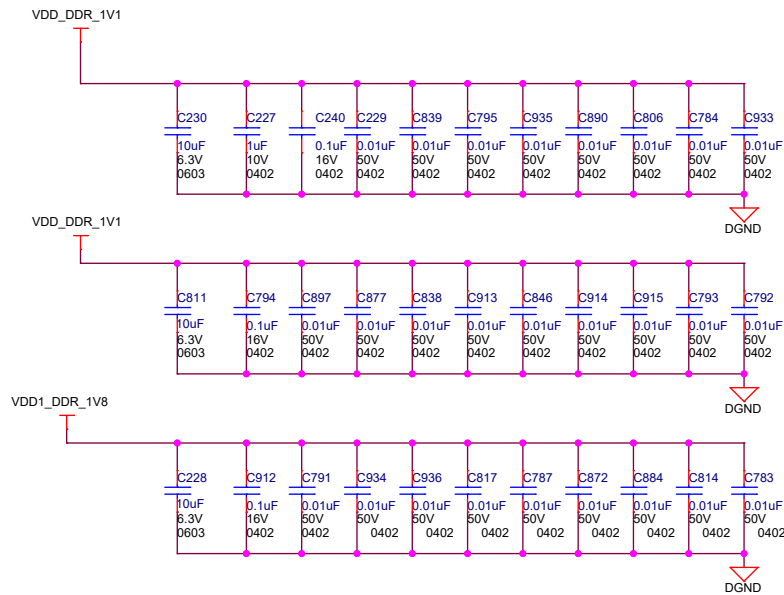
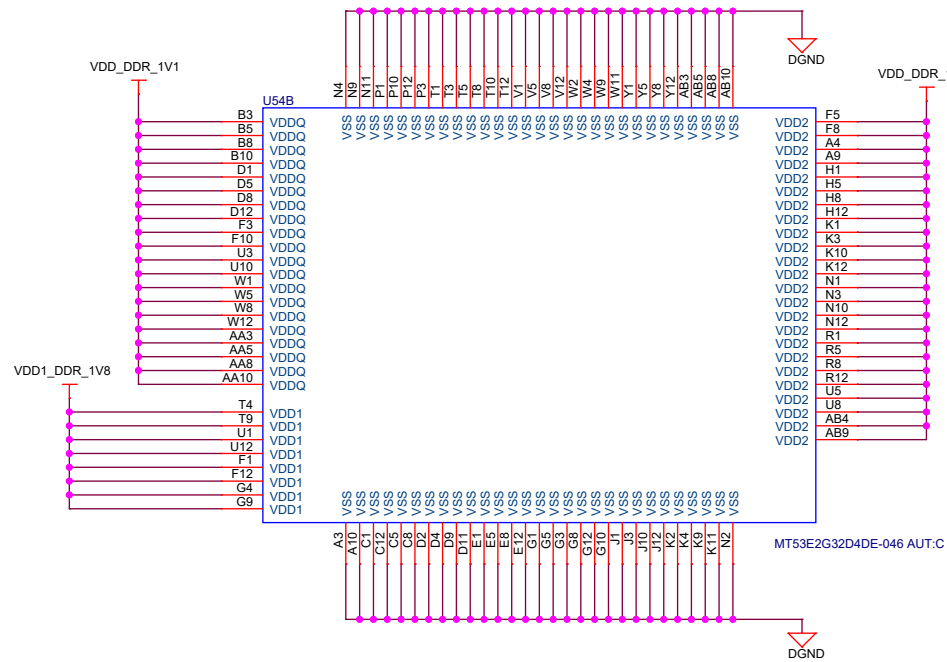
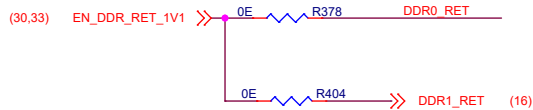
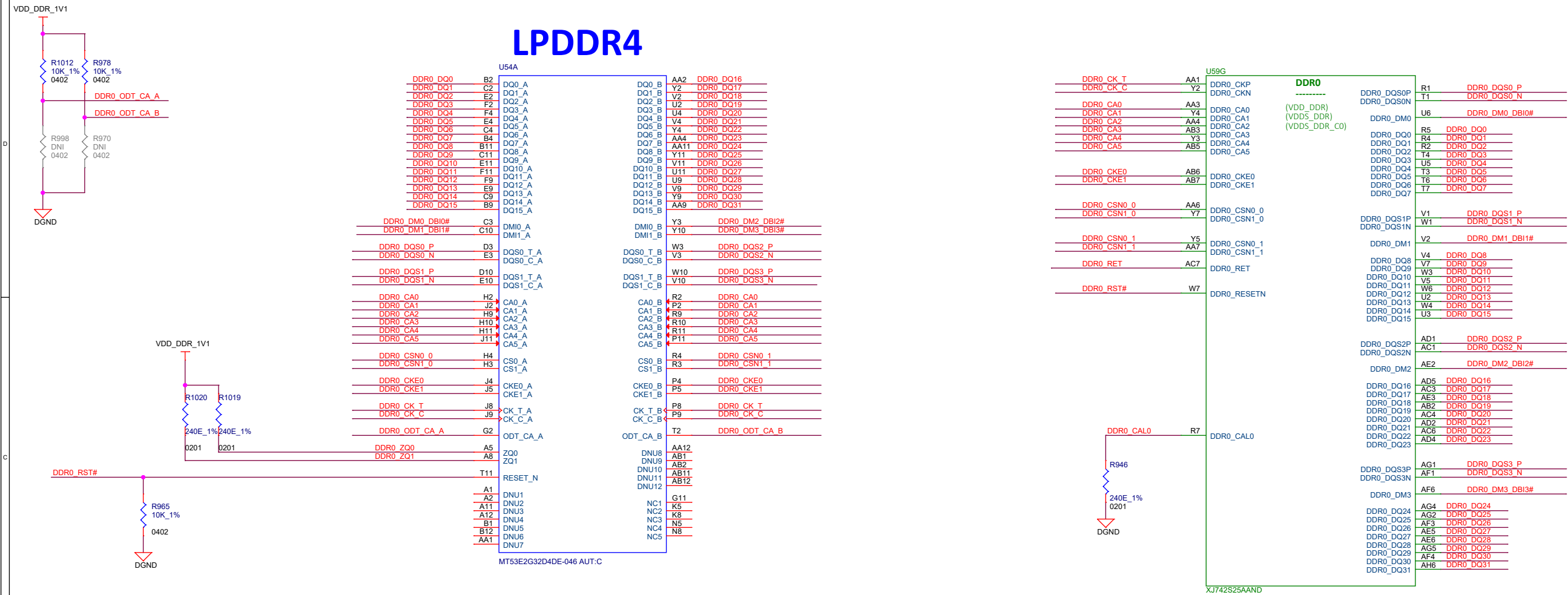
SERDES1



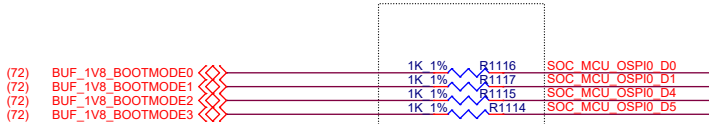
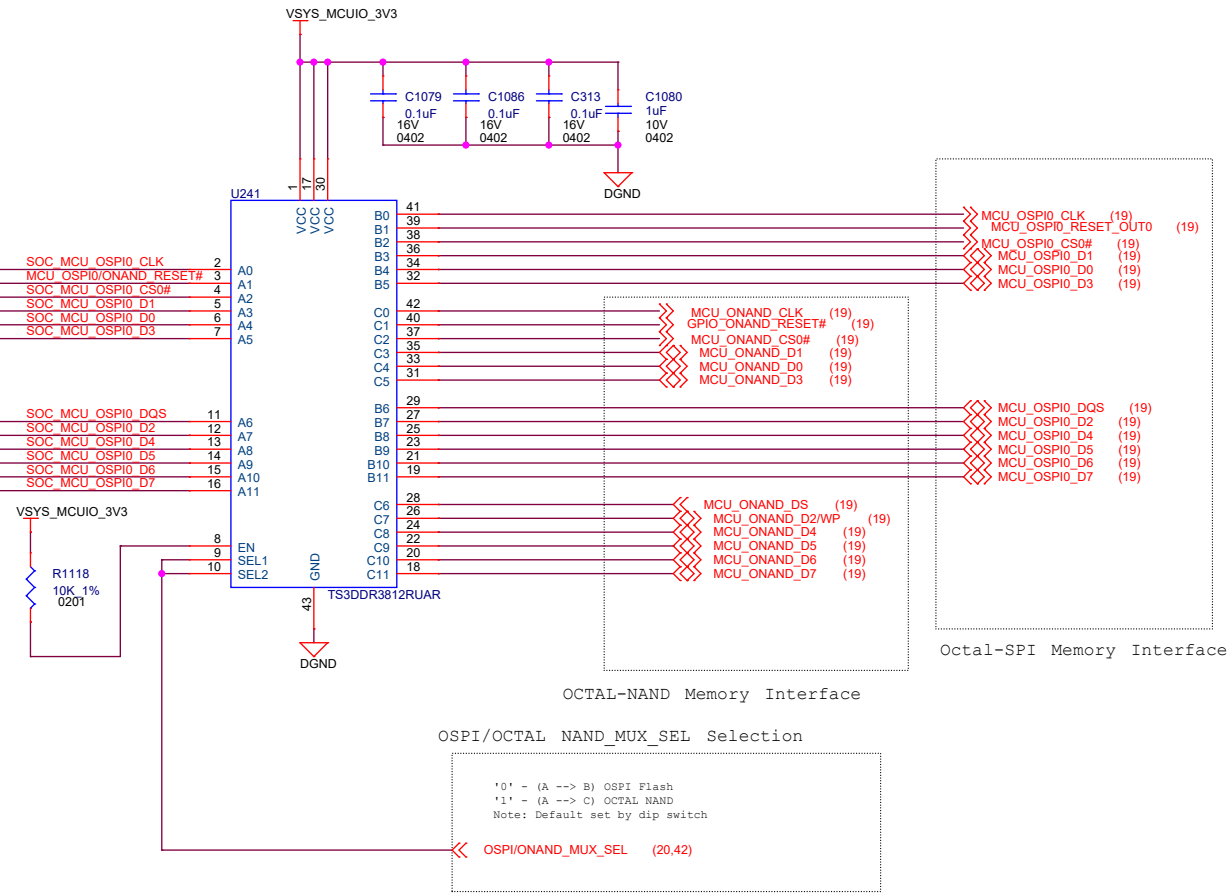
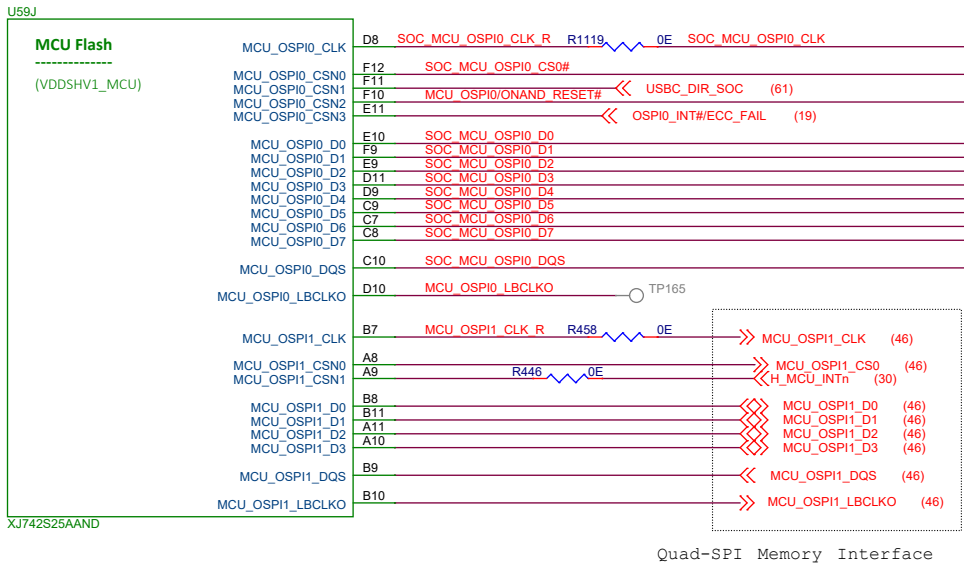
SERDES4



LPDDR4

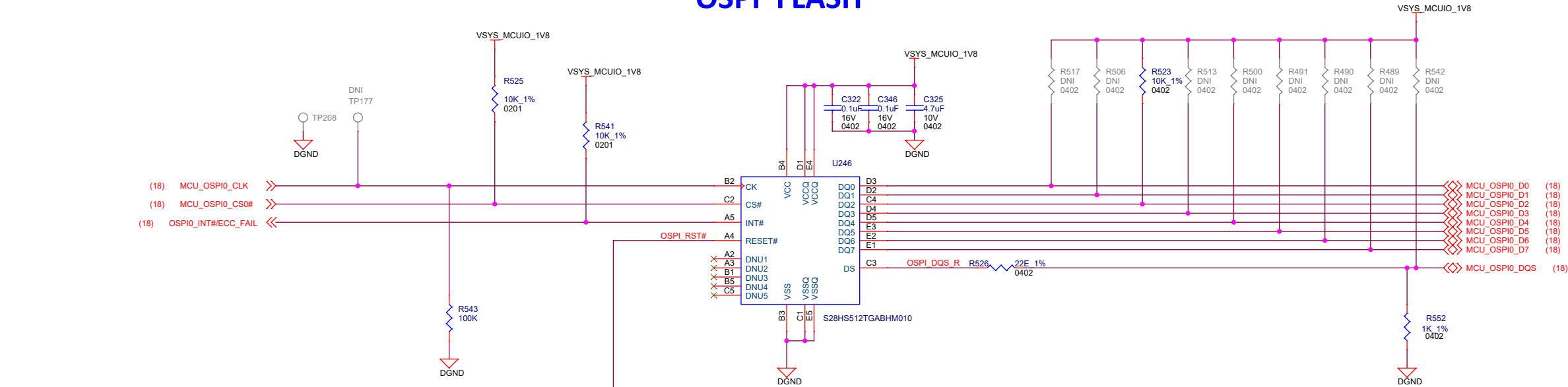


MCU FLASH

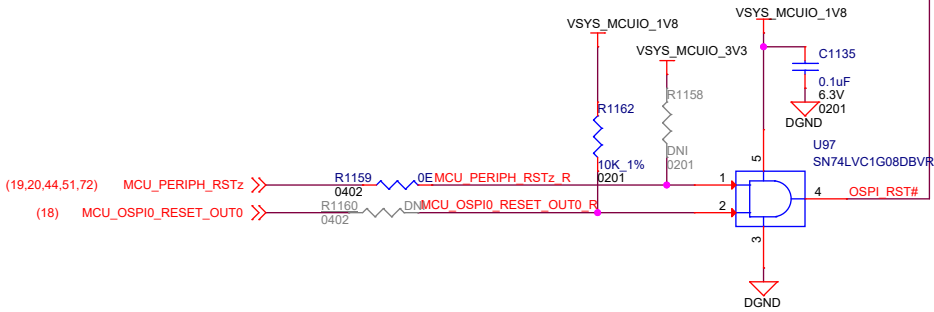


Note: 1K resistors are used to isolate the BOOTMODE control logic after the value is latched.

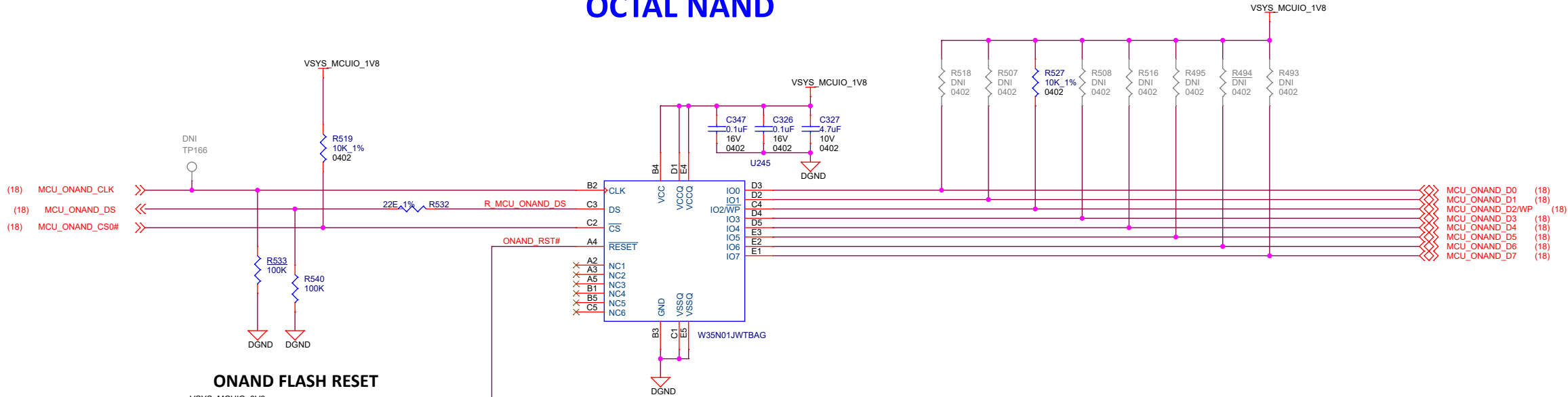
OSPI FLASH



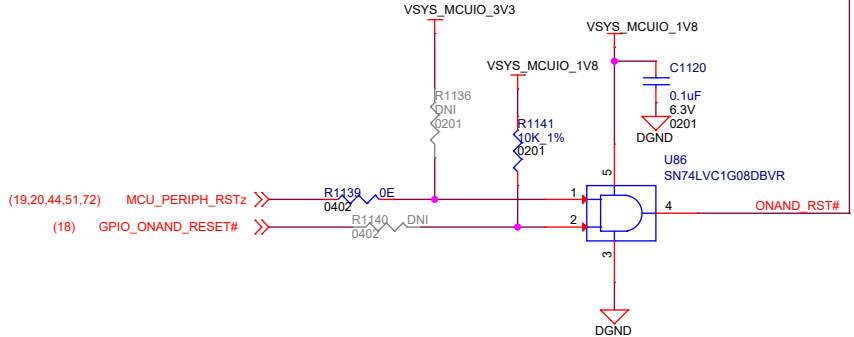
OSPI FLASH RESET



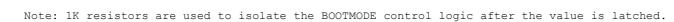
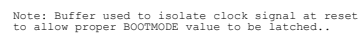
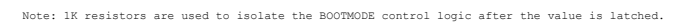
OCTAL NAND



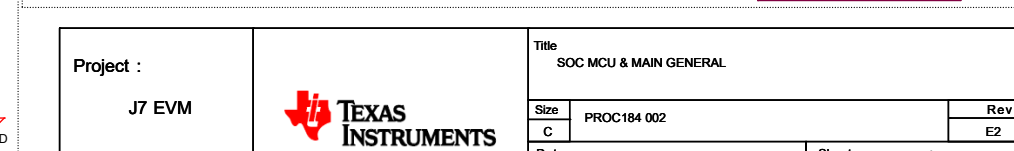
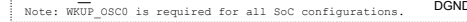
ONAND FLASH RESET



D

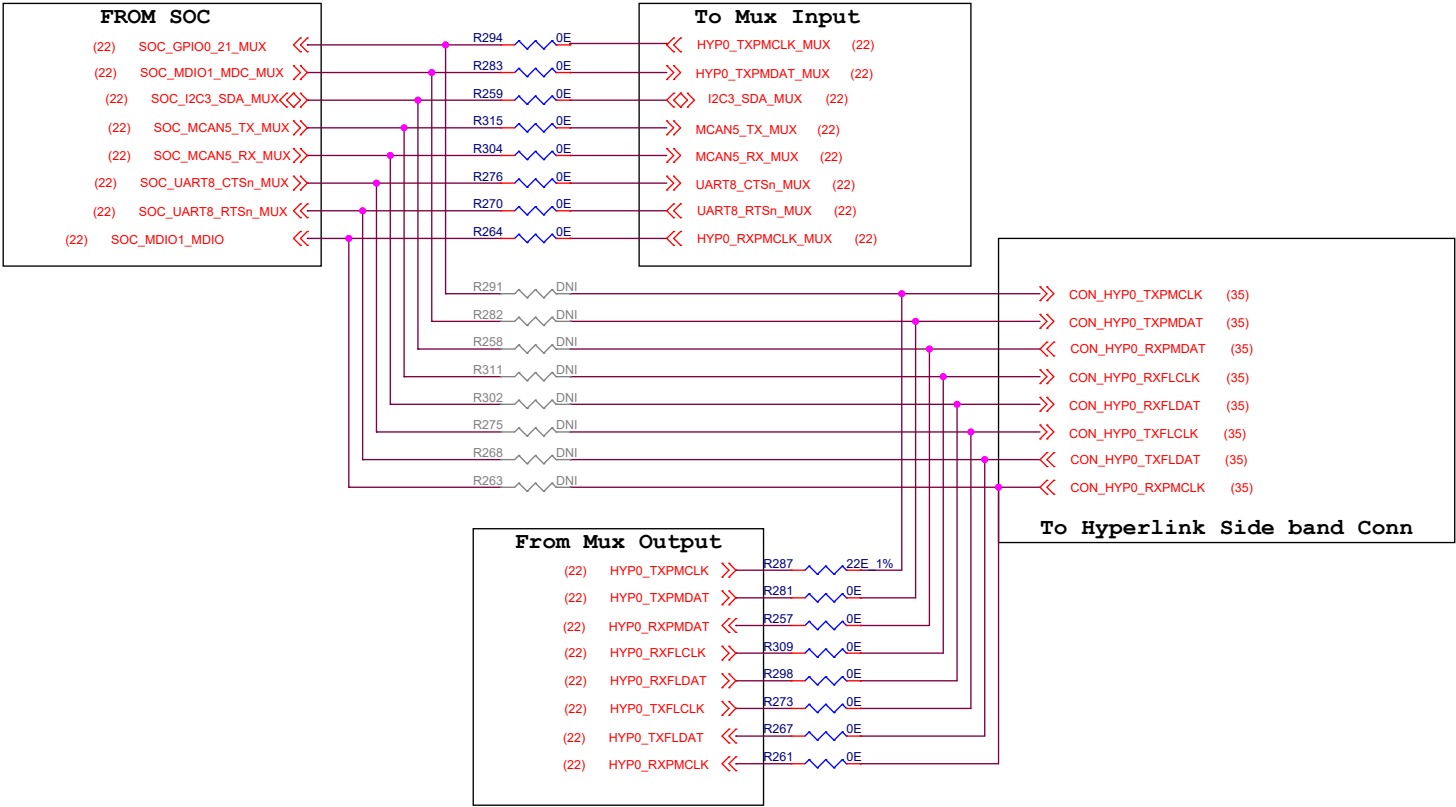


B

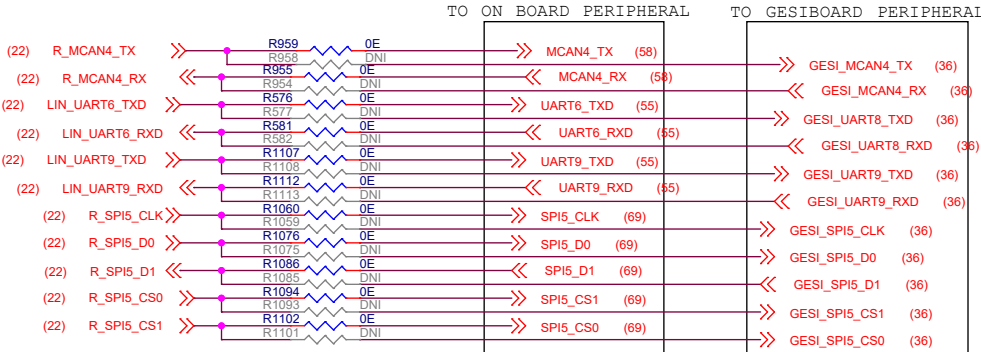


Sheet		of	
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Resistor Mux option to By-pass MUX for Hyperlink sideband signals



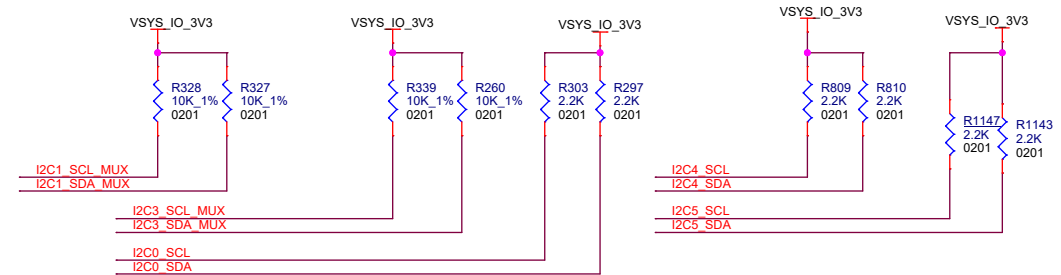
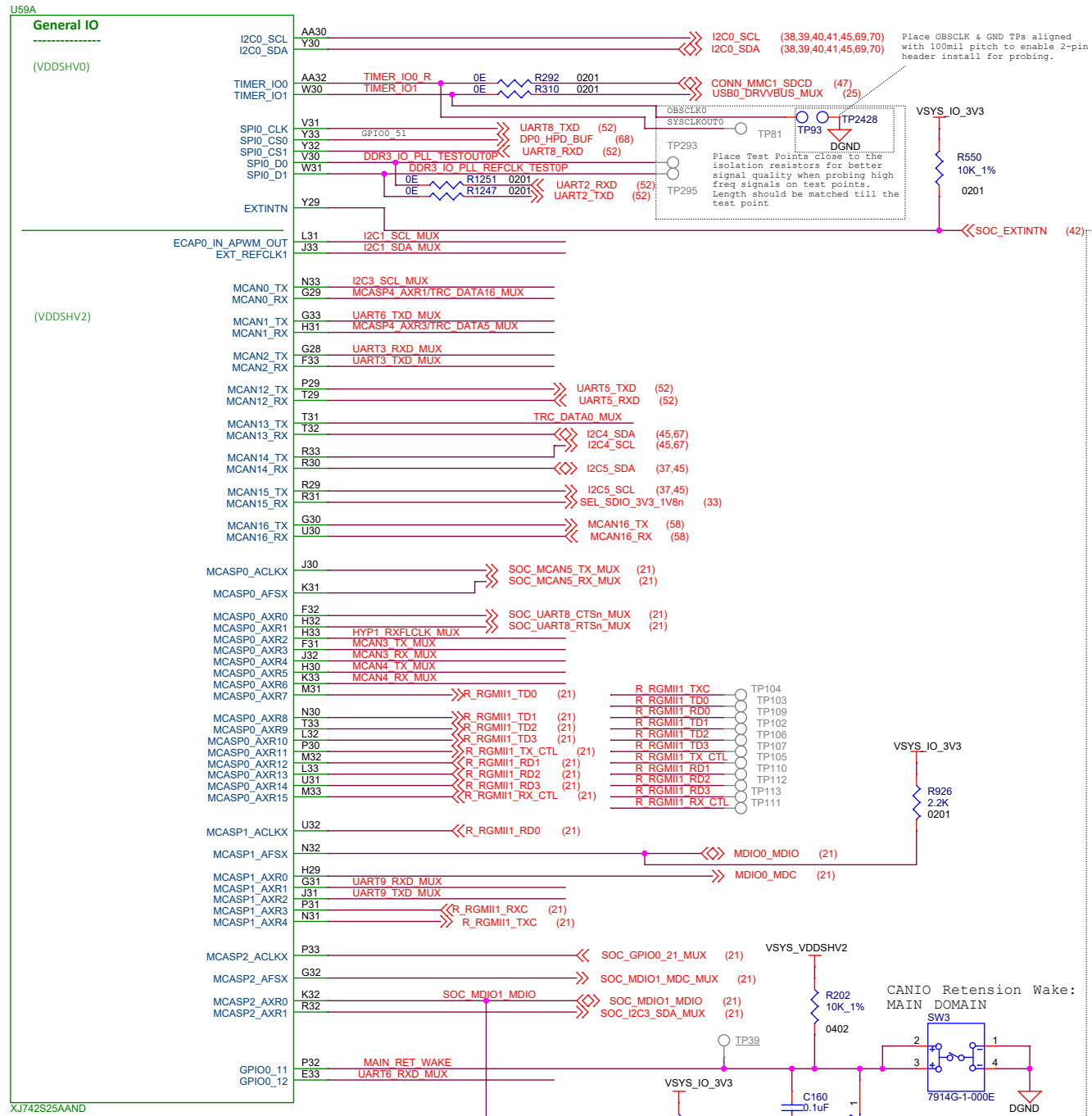
RESISTOR MUX BETWEEN GESI BOARD AND ON BOARD PERIPHERALS



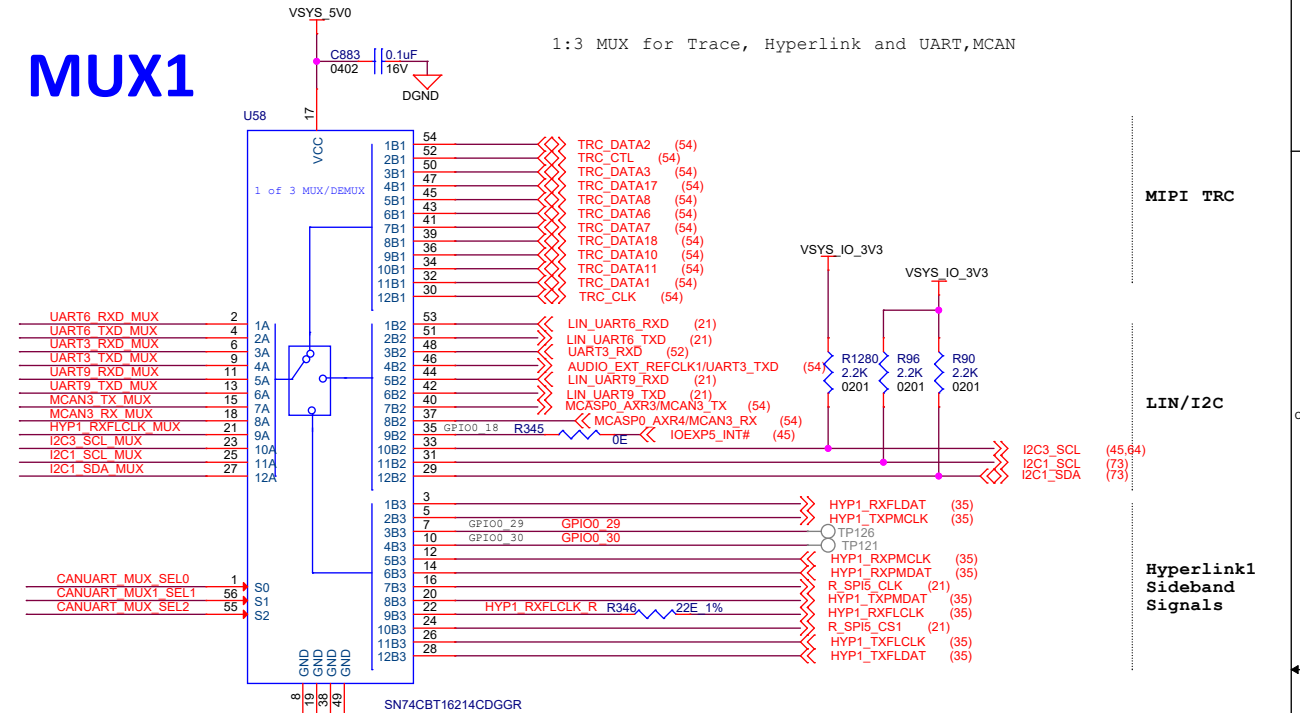
RESISTOR MUX BETWEEN ON BOARD RGMII AND GESI RMII



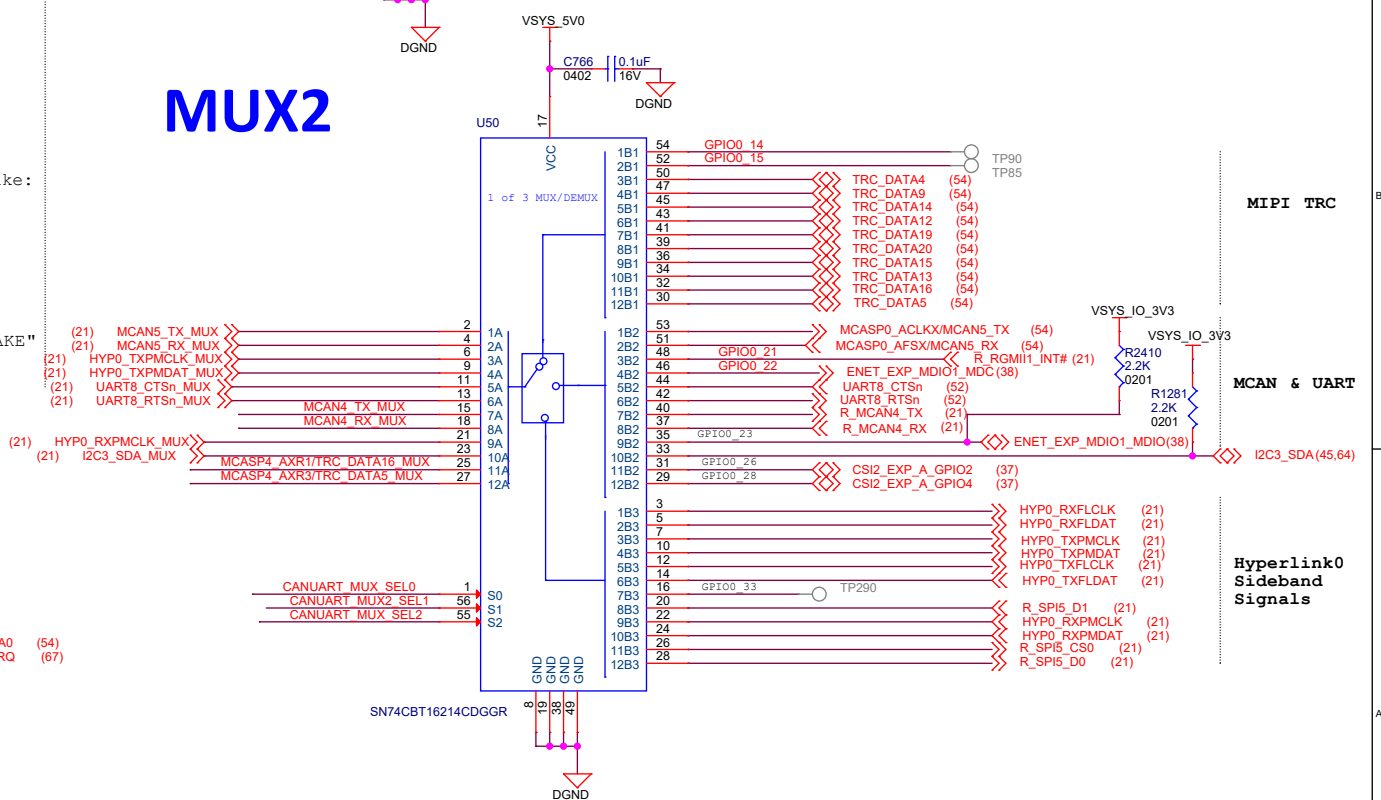
GENERAL IO



MUX1



MUX2

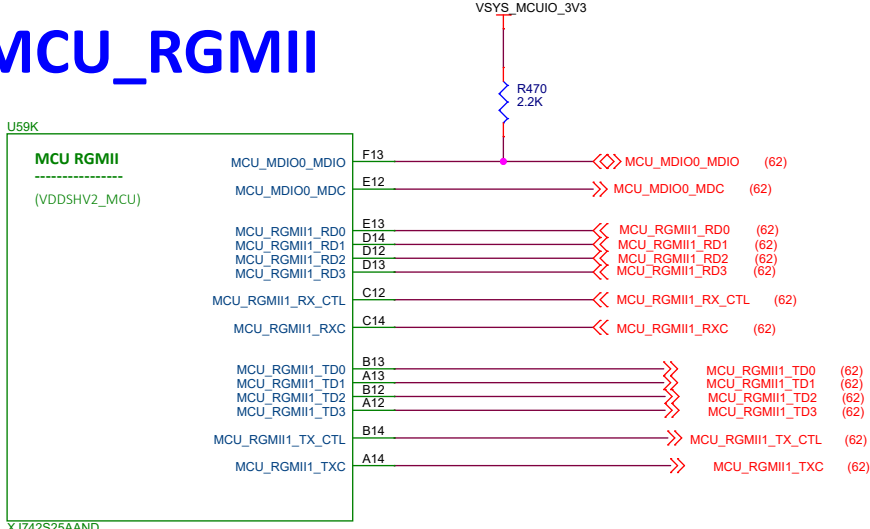


HYPERLINK/TRACE/MCAN/LIN - 1:3 MUX : Truth Table

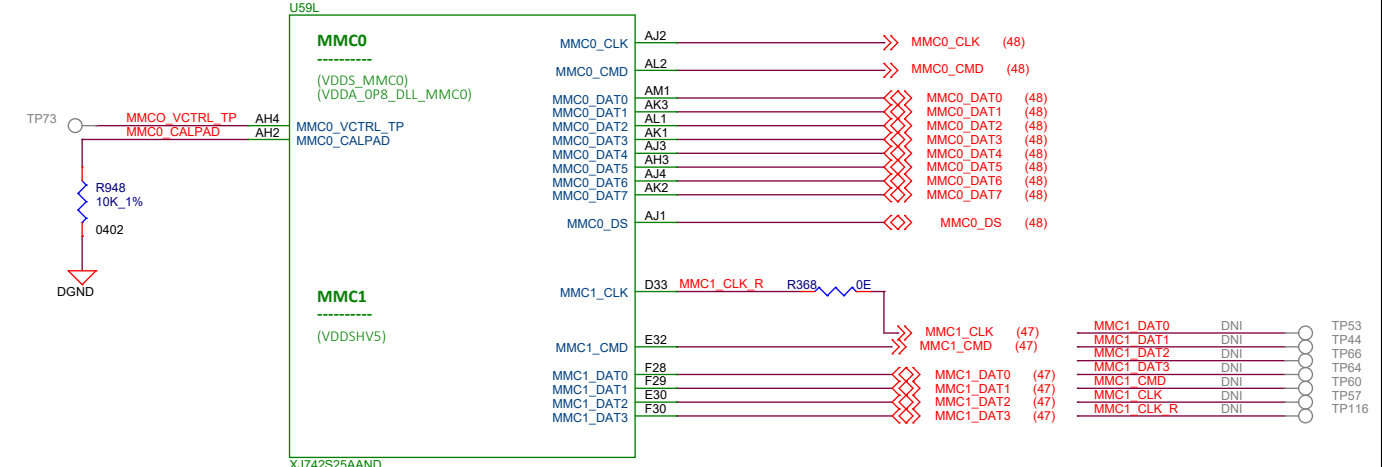
MUX_SEL2	MUX_SEL1	MUX_SEL0	FUNCTION
HIGH	HIGH	LOW	A port = B1 port
HIGH	HIGH	HIGH	A port = B2 port
HIGH	LOW	HIGH	A port = B3 port

(default)

MCU_RGMII



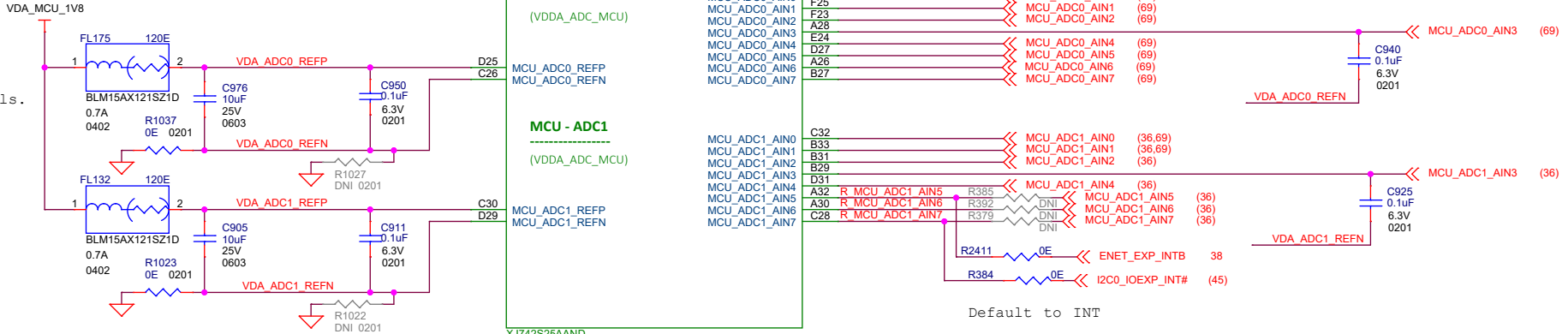
MMC0 and MMC1



MCU_ADC

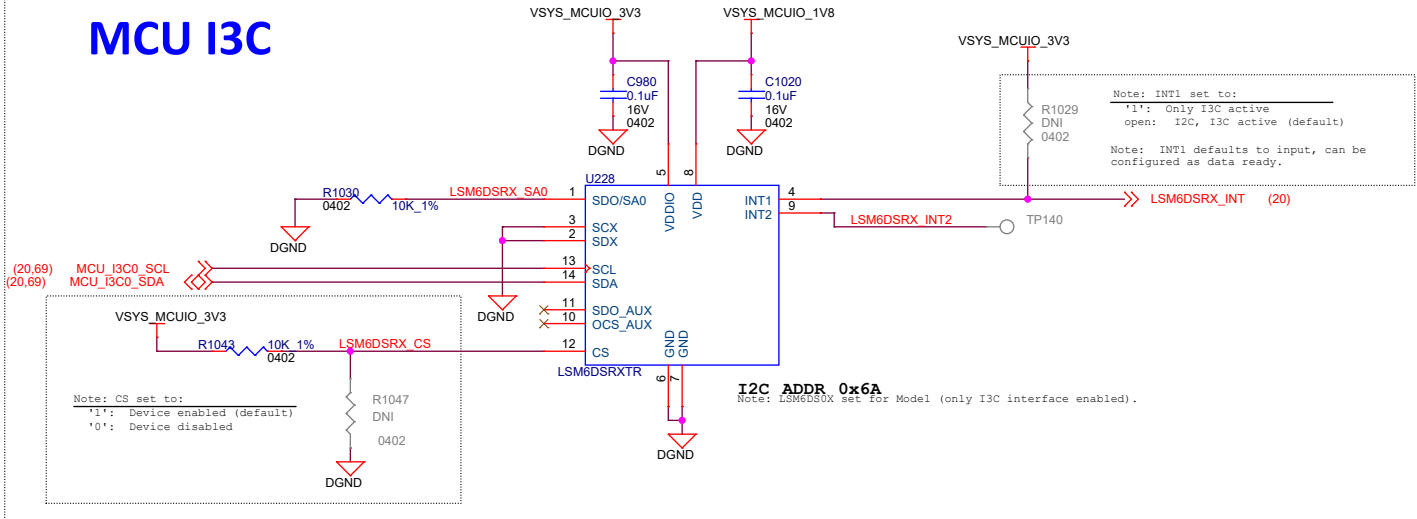
Place Beads, 0402 Cs & 0E Rs outside SoC at FP edge BOM = Install 0E Rs as default	Place 0.1uF Cs across bkout vias & 0E Rs next to Dcaps under SoC BOM = DNI for 0E Rs (testing option)
--	---

ADC 0 & 1 Filtering Scheme:
 ADC0/1 VREF P have 2x independent input balls with same
 in-line supply filtering as common VDA ADC1V8 pwr rail supplying VDDA_ADC0/1 balls.
 (Provisioned supply filtering for PCB layout pending
 fdbk from TI analog design team.)
 -1x Ferrite bead to filter & reduce noise
 -1x 0402 (2.2-10uF), SoC perimeter/near end
 -1x 0201 for 0.1uF per pwr ball, far end
 -1x 0201 0E R to optional short REFN to board GND
 (as area under SoC allows)



Place 0.1uF Cs across AINx to VREFN nets as close to breakout vias as possible.
BOM = DNI for 0E Rs (testing option)

MCU I3C



Project :

J7 EVM



Title	MCU RGMII & ADC
-------	-----------------

Size	PROC184 002
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Date: Wednesday, September 18, 2024

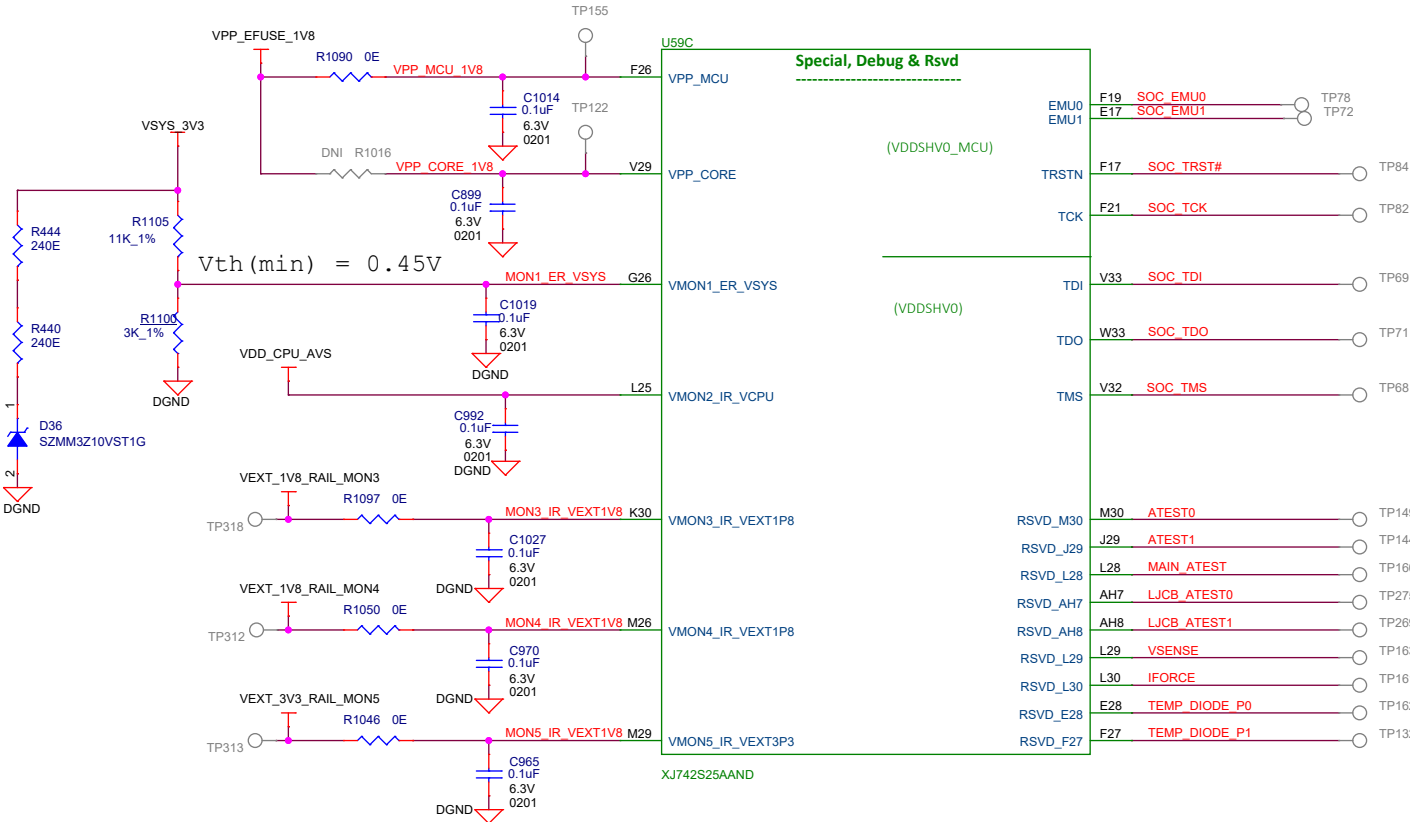
Rev

85

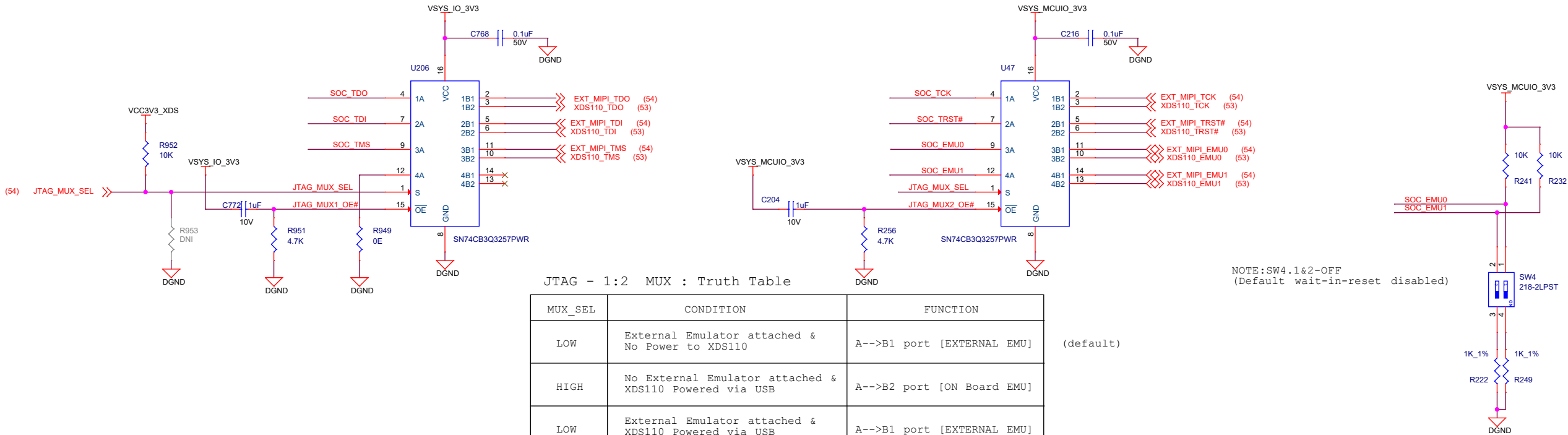
21 of 85

SPECIAL, DEBUG & RSVD

If monitoring VSYS_3V3, protect SoC from 1st stage fault. Alternatively, monitoring protected VCCA_3V3 requires no Zener diode.



JTAG AND TRACE MUX



JTAG - 1:2 MUX : Truth Table

MUX_SEL	CONDITION	FUNCTION
LOW	External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]
HIGH	No External Emulator attached & XDS110 Powered via USB	A-->B2 port [ON Board EMU]
LOW	External Emulator attached & XDS110 Powered via USB	A-->B1 port [EXTERNAL EMU]
LOW	No External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]

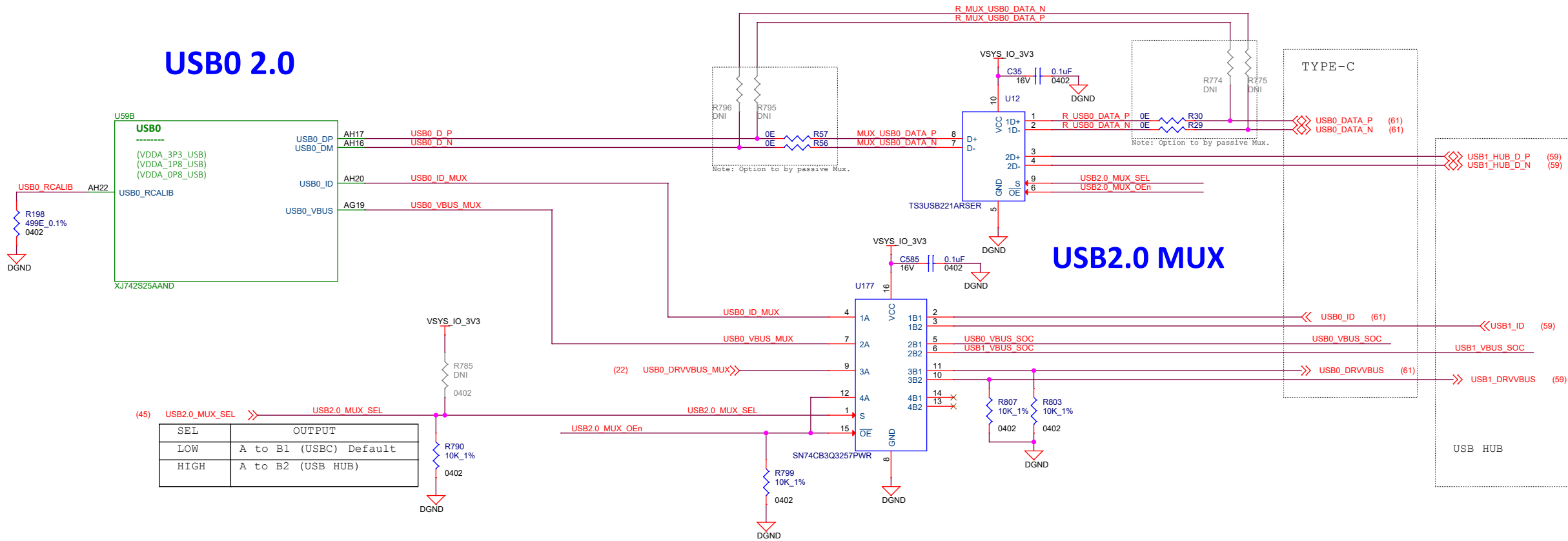
(default)

NOTE:SW4.1&2-OFF
(Default wait-in-reset disabled)

USB0 2.0

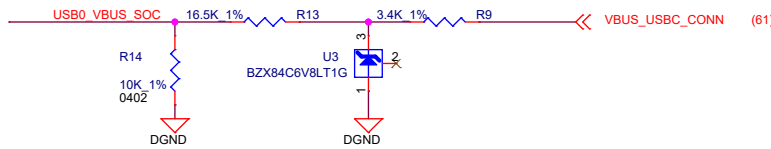
By Pass USB MUX	Mount - R796,R795,R774,R775 DNI -R57,R56,R30,R29
USB MUX (Default)	Mount -R57,R56,R30,R29 DNI - R796,R795,R774,R775

USB0 2.0

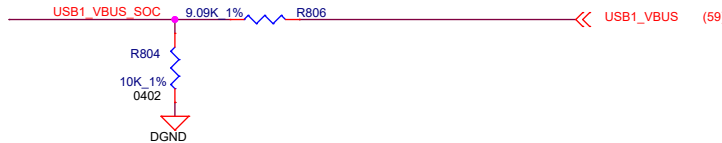


USB VBUS Resistor divider circuit

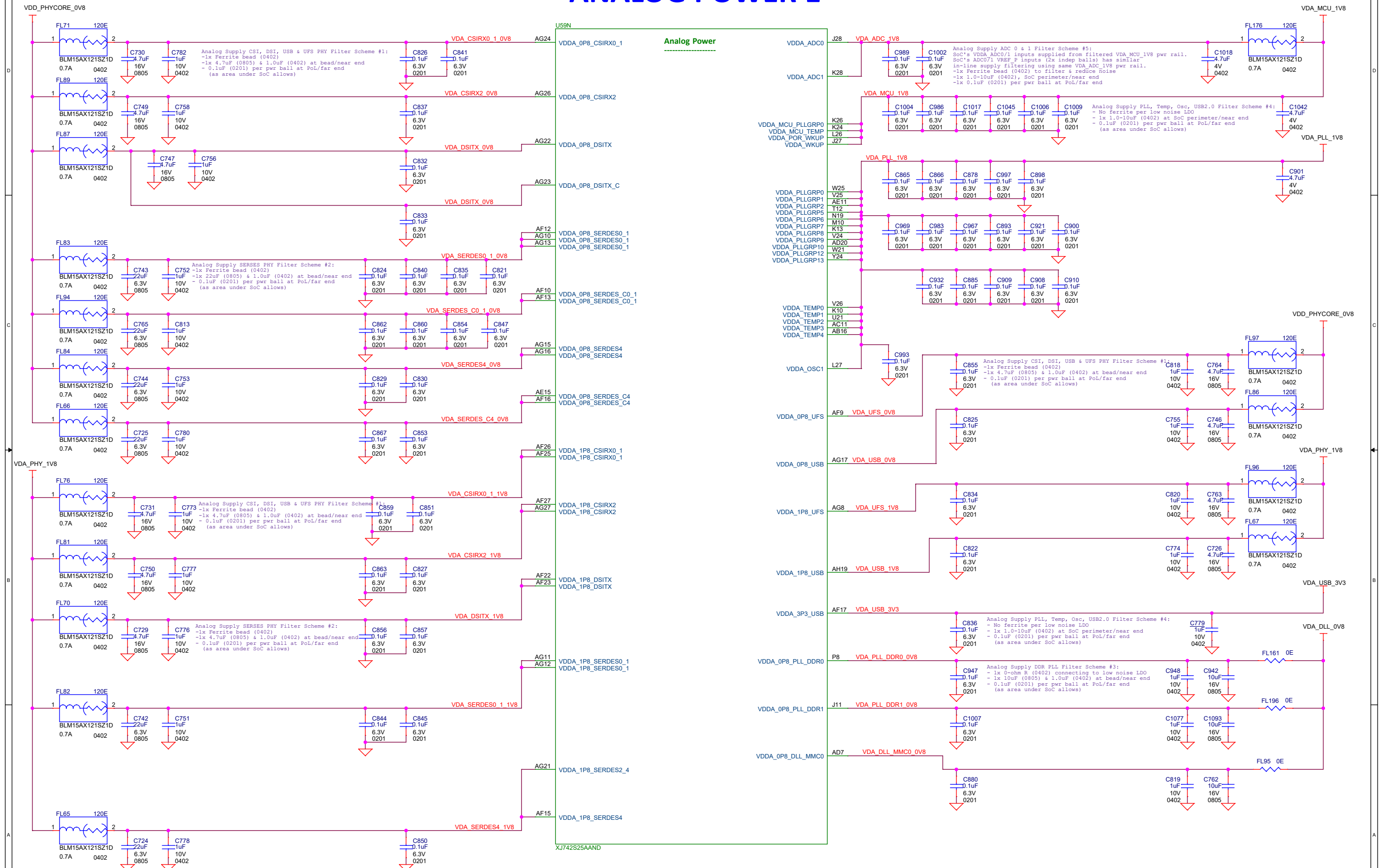
Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS



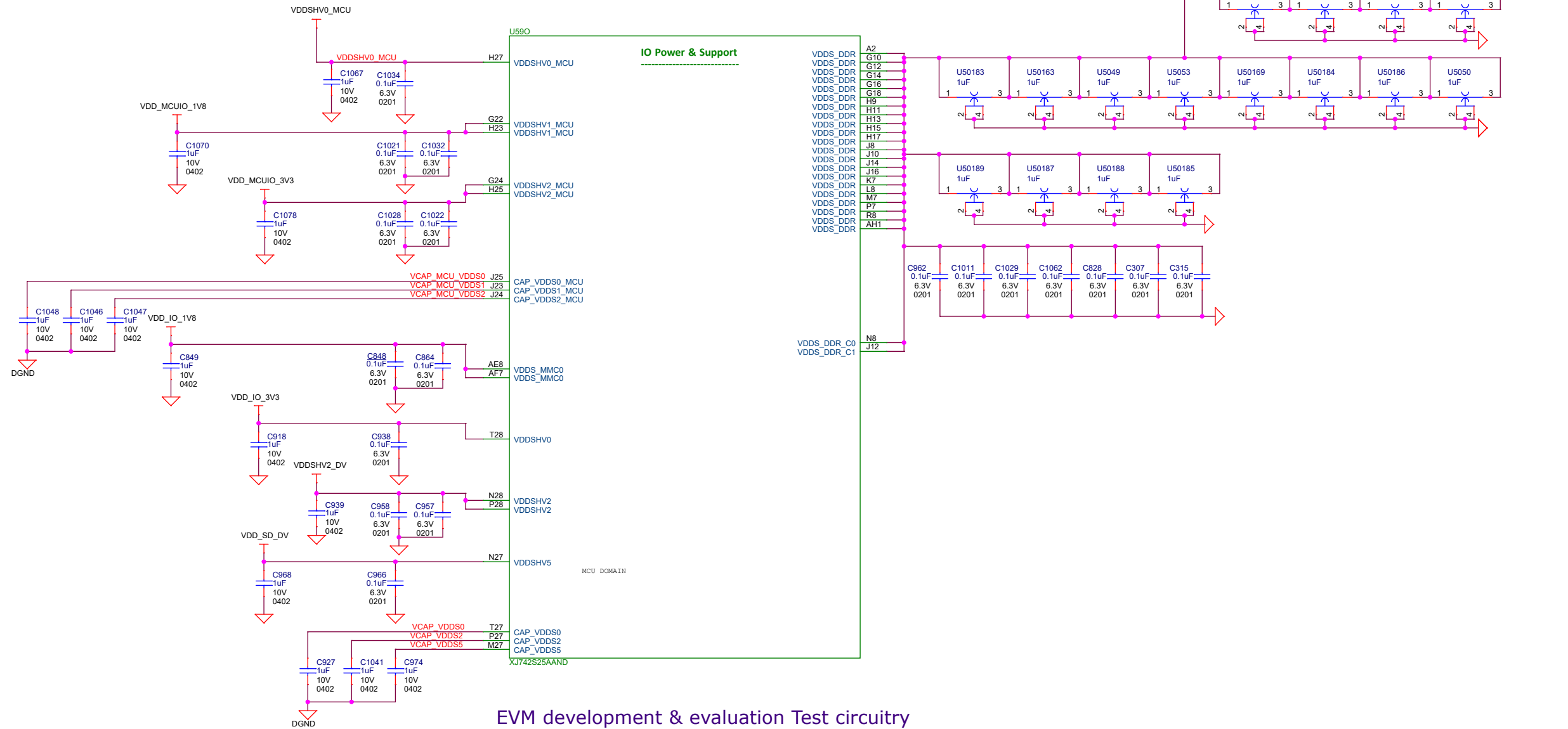
Note: Recommended VBUS circuit for embedded Hub



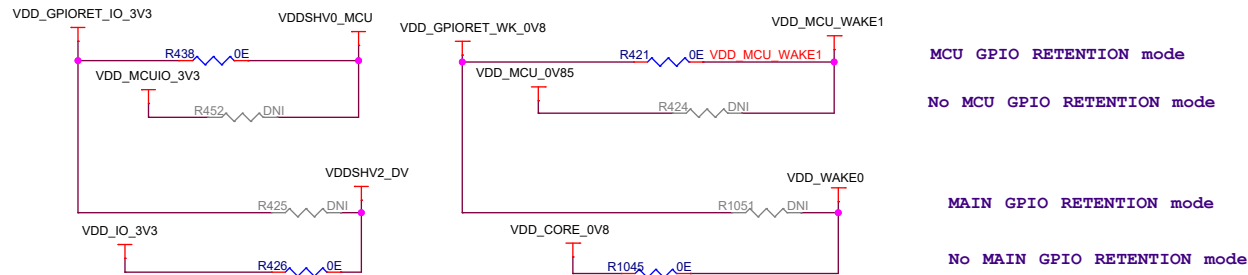
ANALOG POWER 1



IO POWER 2



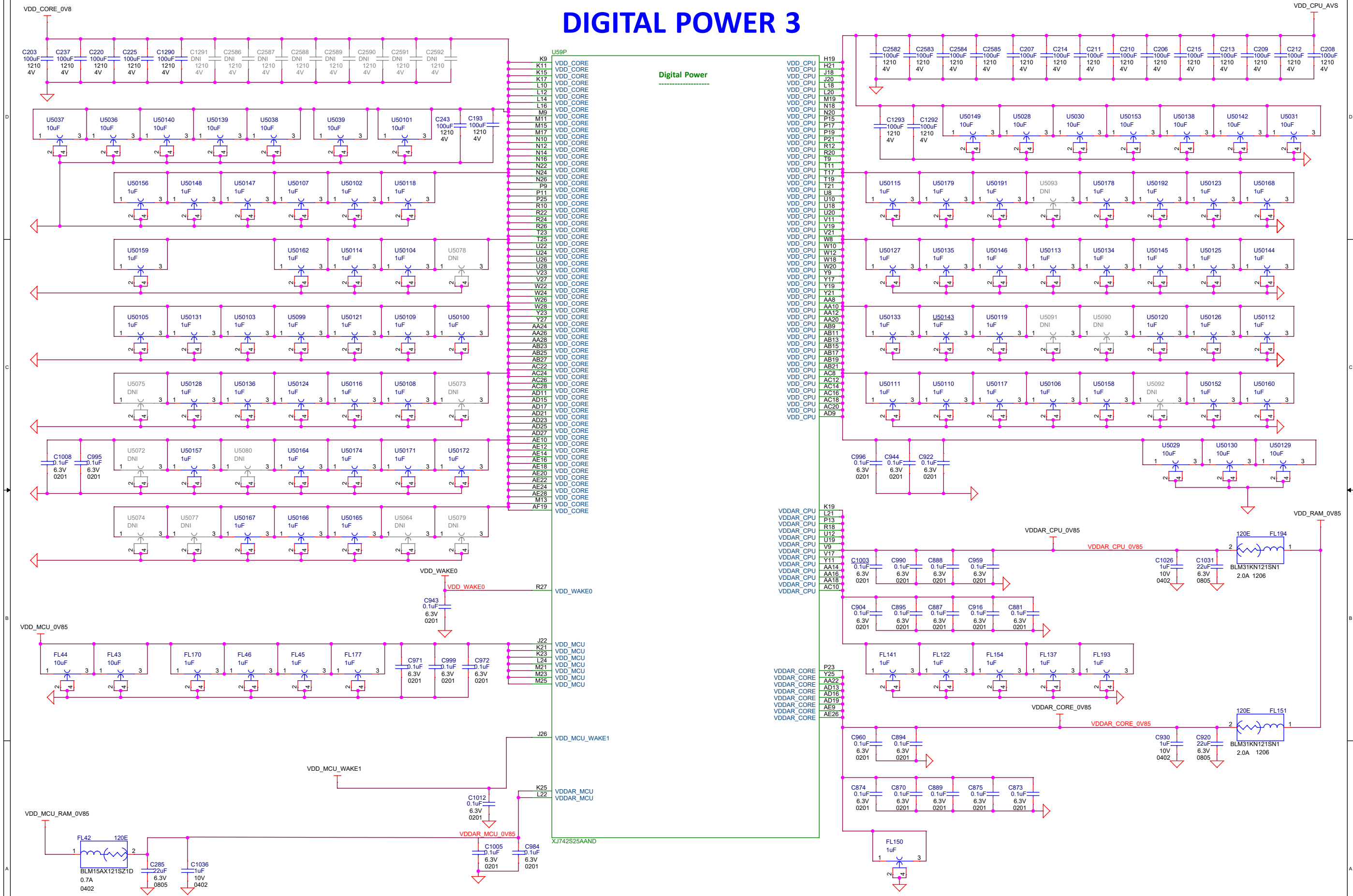
EVM development & evaluation Test circuitry
EVM GPIO Retention testing option
(TI EVM Only)



Note:
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.
Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Low power modes	Resistors to be Populated	Resistors to be DNI'd
No GPIO RET	R452, R424, R426, R1045	R438, R421, R425, R1051
MCU GPIO RET only	R438, R421, R426, R1045	R452, R424, R425, R1051
MAIN GPIO RET only	R452, R424, R425, R1051	R438, R421, R426, R1045
MCU & MAIN GPIO RET	R438, R421, R425, R1051	R452, R424, R426, R1045

DIGITAL POWER 3

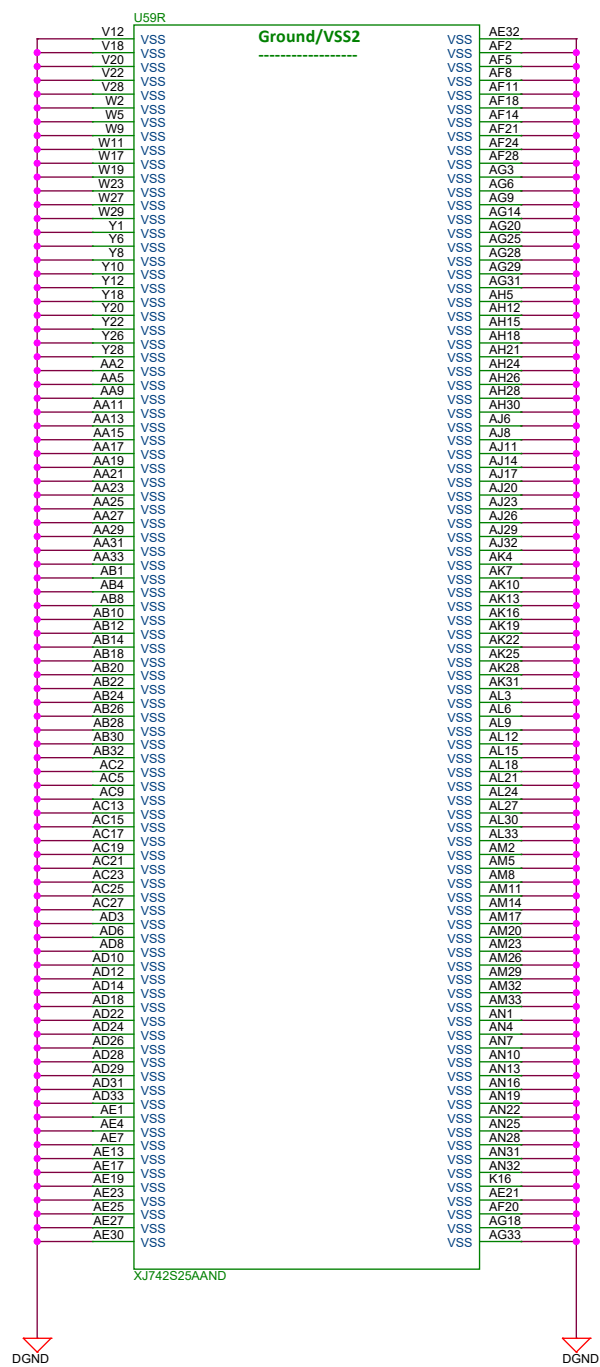
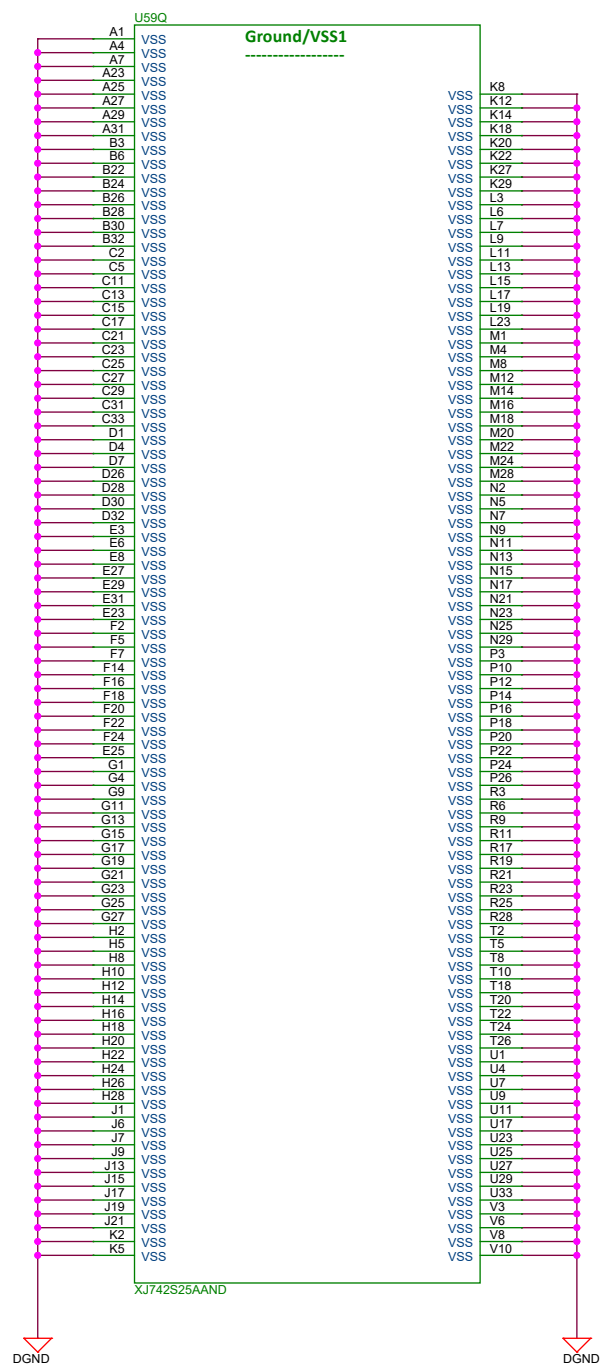


Note:

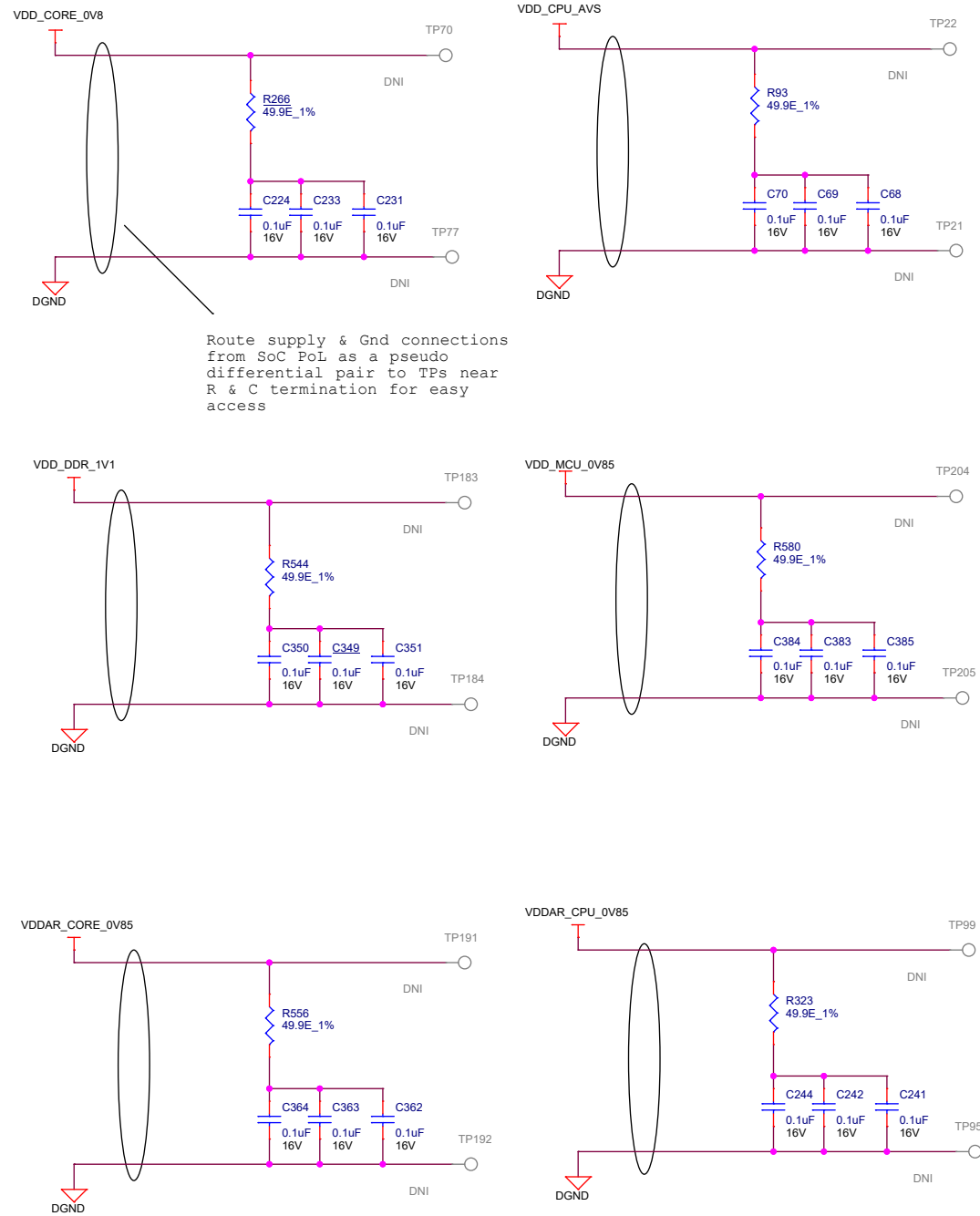
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

SOC GROUND



SoC Supply Noise Kelvin Sensing



PMIC

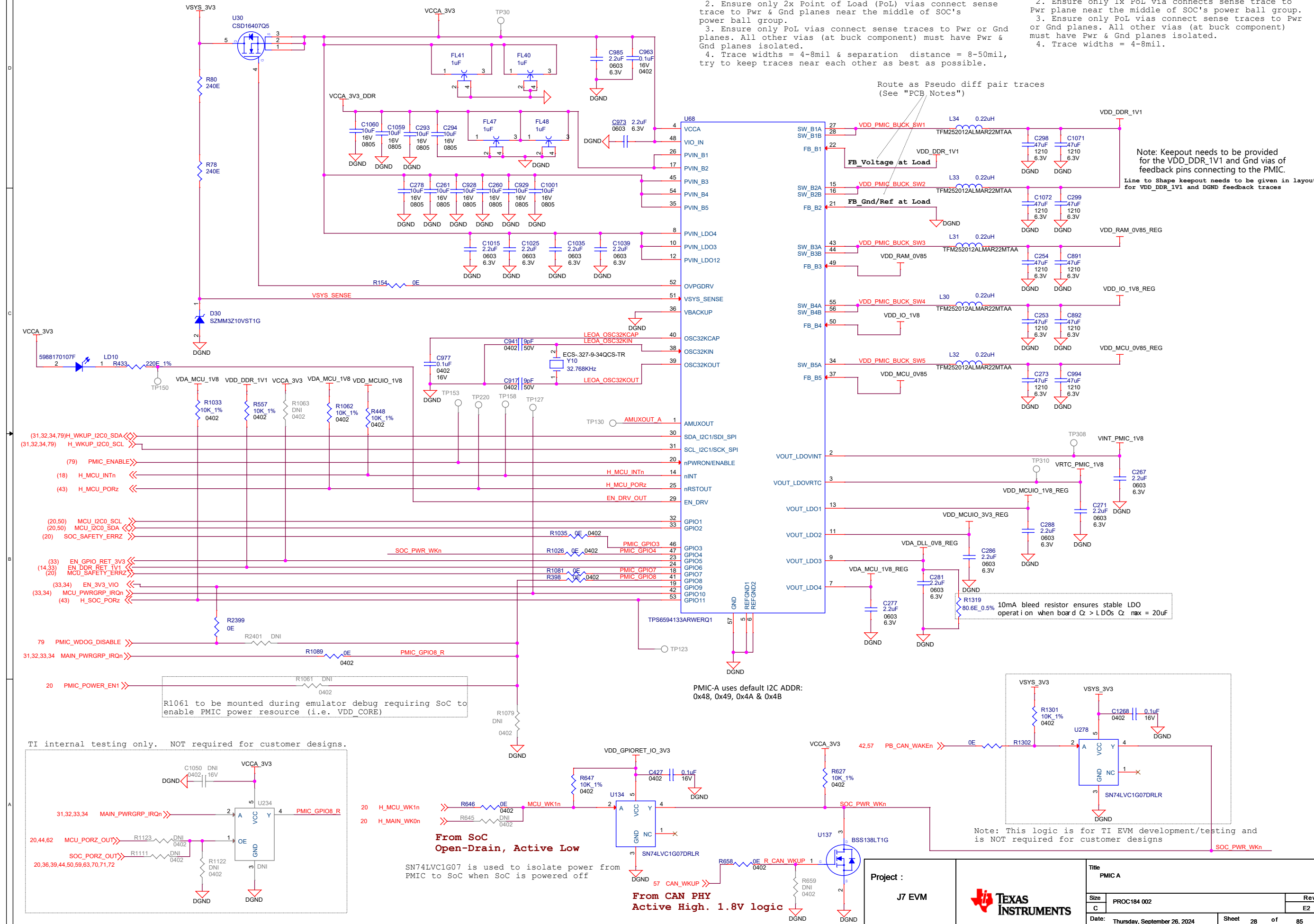
"PCB Notes":

For multi-phase Buck converter configs, route remote sense feedback as follows:

1. Use pseudo differential pair traces on same layer & net to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Ensure only 2x Point of Load (PoL) vias connect sense trace to Pwr & Gnd planes near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
4. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible.

For single-phase Buck converter configs,
route remote sense feedback as follows:

1. Use single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Ensure only 1x PoL via connects sense trace to Pwr plane near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
4. Trace widths = 4-8mil.



VDD_CPU_AVS High-Current Power Stage A (HCPS-A)

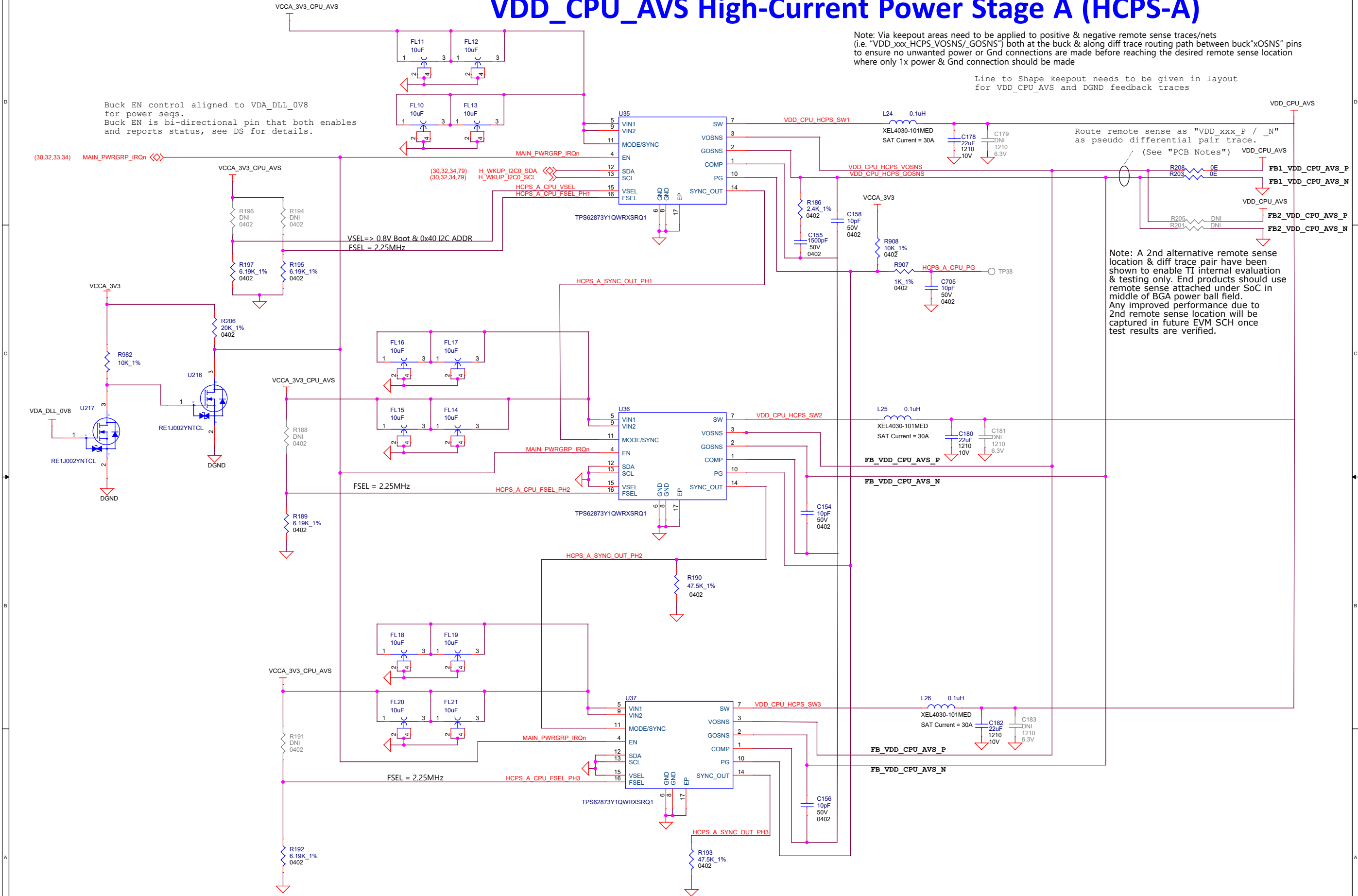
Note: Via keepout areas need to be applied to positive & negative remote sense traces/nets (i.e. "VDD_XXX_HCPS_VOSNS/_GOSNS") both at the buck & along diff trace routing path between buck"xOSNS" pins to ensure no unwanted power or Gnd connections are made before reaching the desired remote sense location where only 1x power & Gnd connection should be made

Line to Shape keepout needs to be given in layout for VDD_CPU_AVS and DGND feedback traces

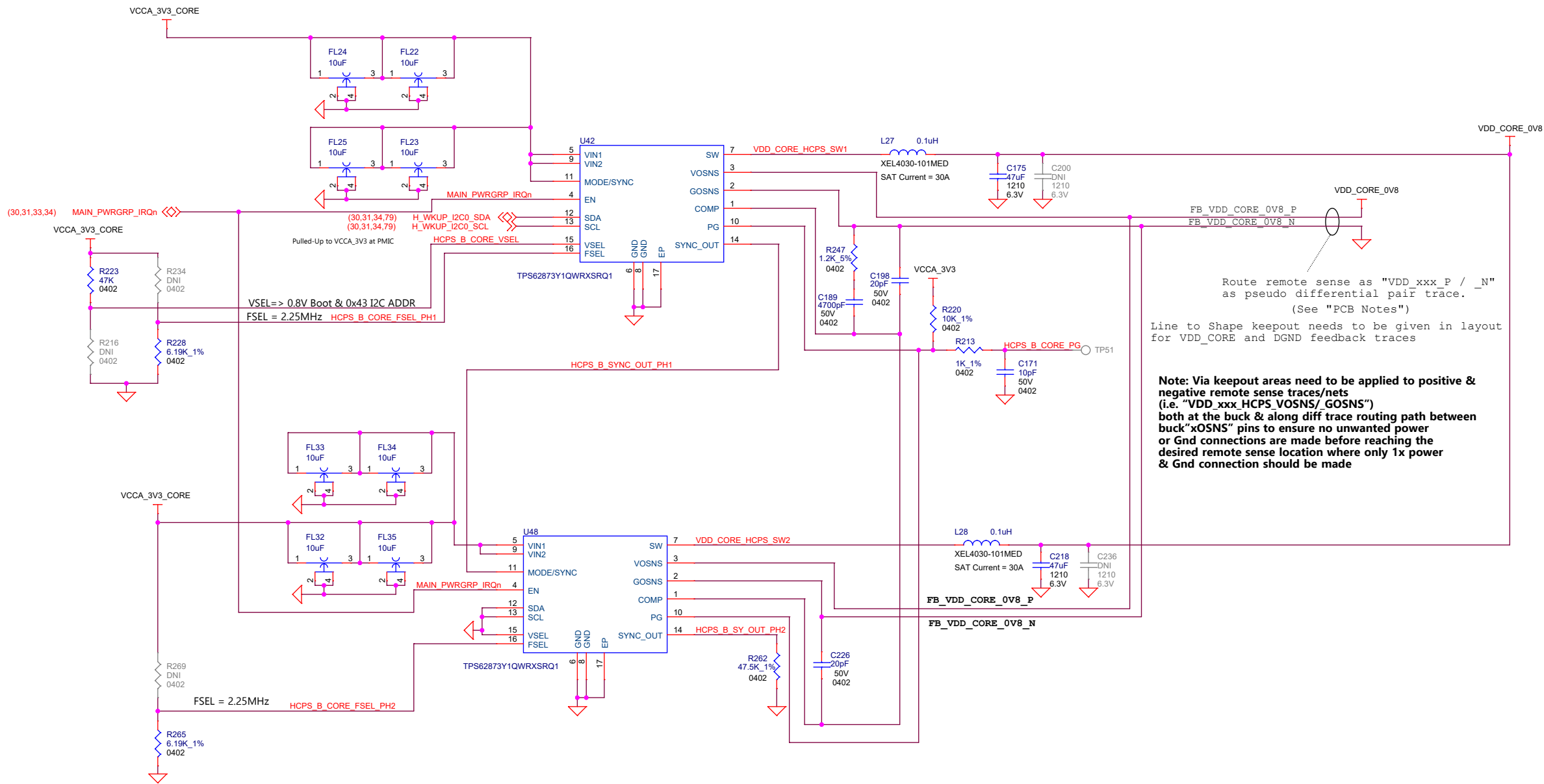
Buck EN control aligned to VDA_DLL_0V8 for power seqs.
Buck EN is bi-directional pin that both enables and reports status, see DS for details.

Route remote sense as "VDD_XXX_P / _N" as pseudo differential pair trace.
(See "PCB Notes")

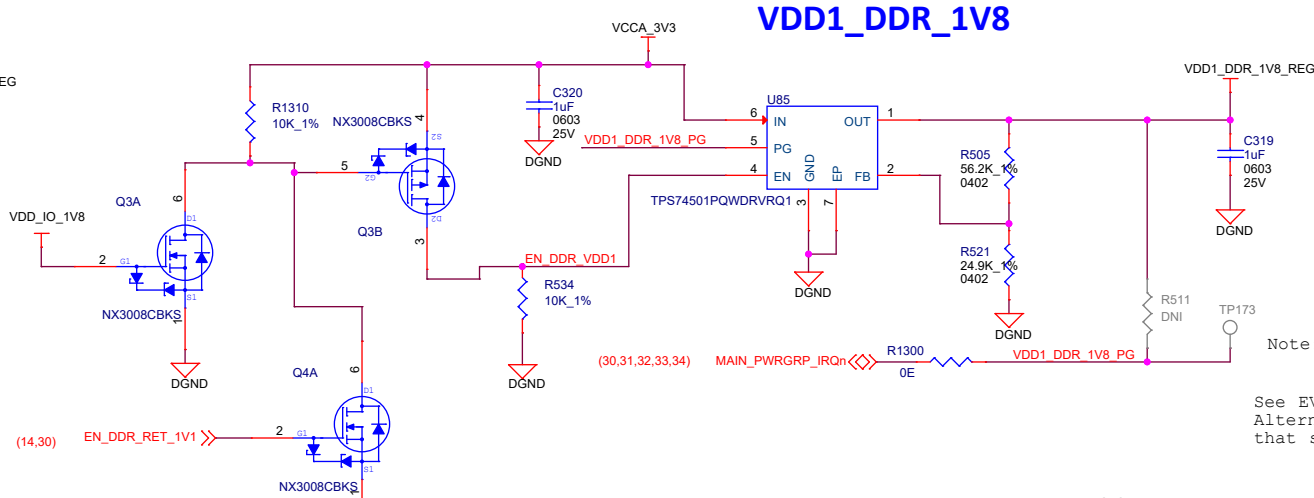
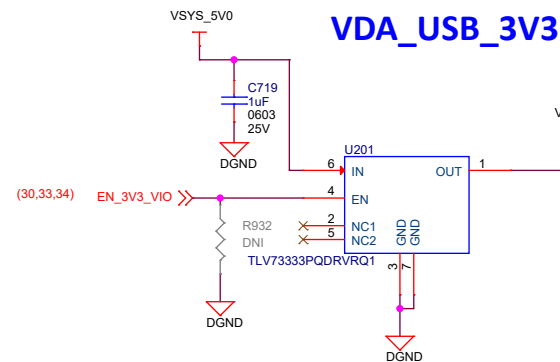
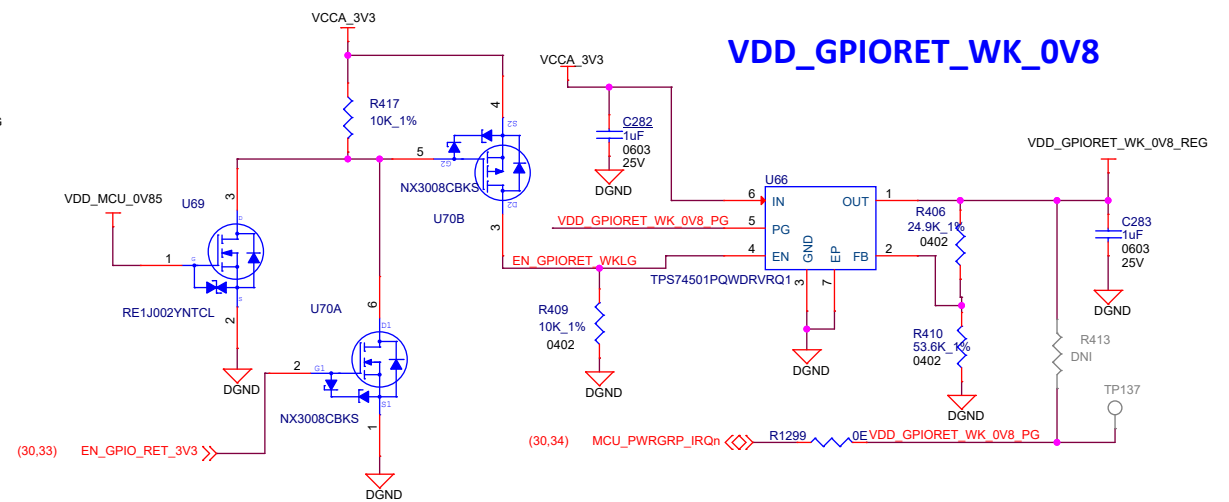
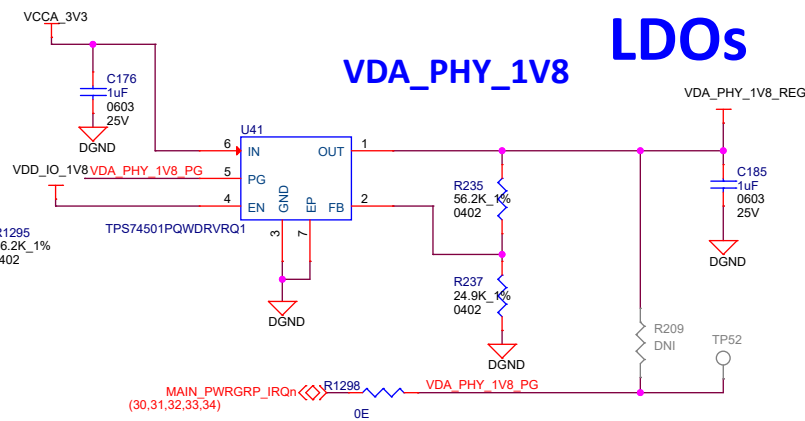
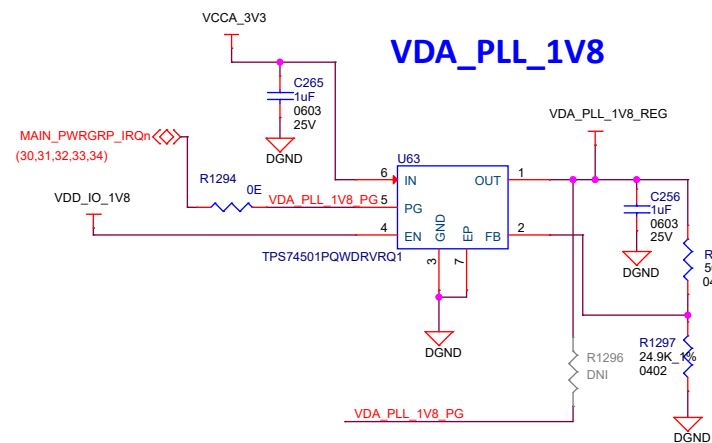
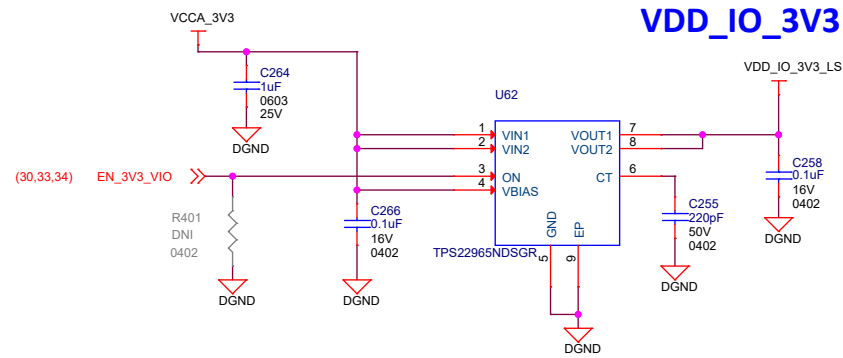
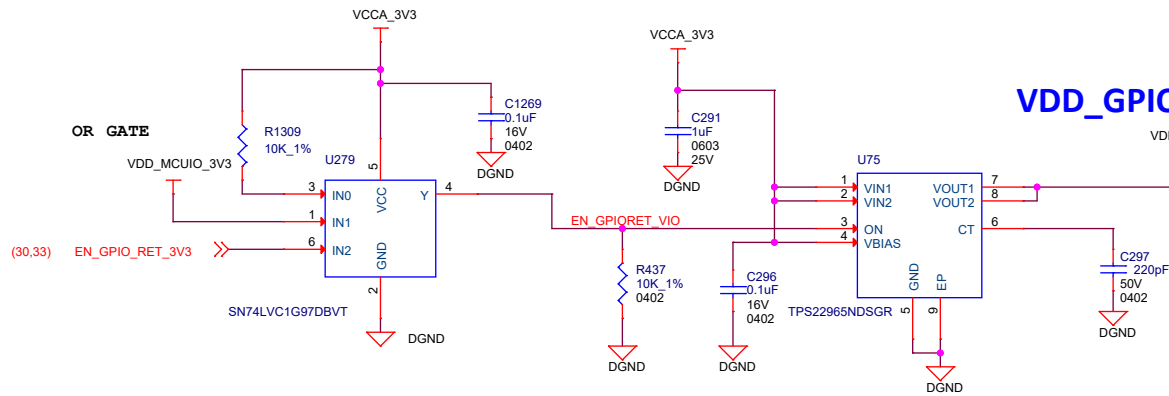
Note: A 2nd alternative remote sense location & diff trace pair have been shown to enable TI internal evaluation & testing only. End products should use remote sense attached under SoC in middle of BGA power ball field.
Any improved performance due to 2nd remote sense location will be captured in future EVM SCH once test results are verified.



VDD_CORE_0V8 High-Current Power Stage A (HCPS-B)



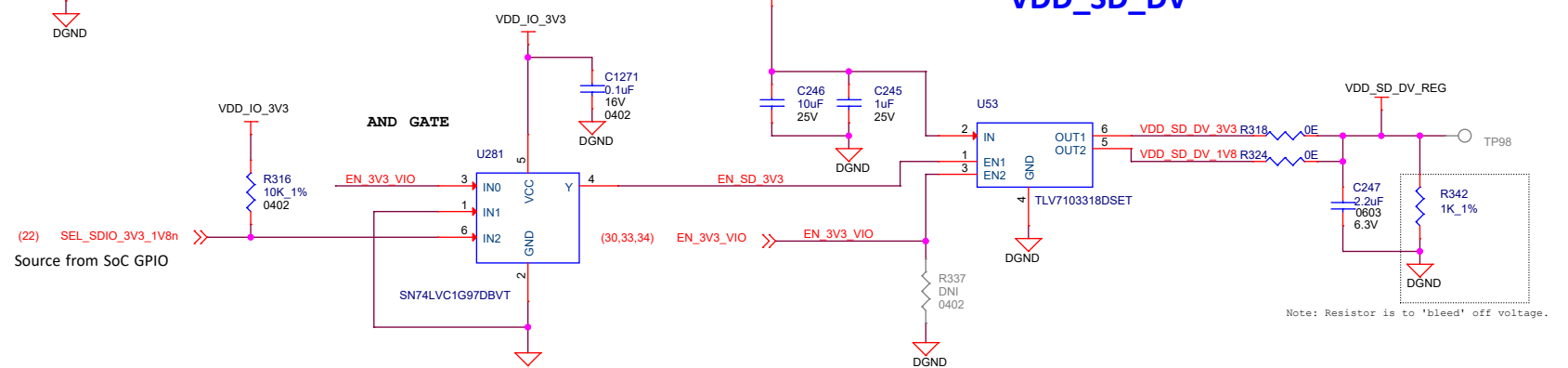
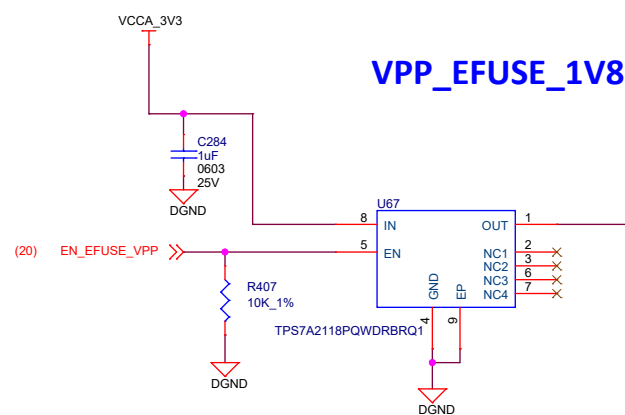
LOAD SWITCHES



EN_GPIORET_VIO & EN_GPIORET_WKLG & EN_DDR_VDD1 Truth table

"OR" Gate Logic			States		
X	Y	OUTPUT	Input - X	Input - Y	Output
0	0	0	OFF	OFF	OFF
0	1	1	OFF	ON	ON
1	0	1	ON	OFF	ON
1	1	1	ON	ON	ON

Note: An alternative discrete OR gate circuit using Bipolar Junction Transistors (BJT) can be used instead of FETs for improved low temp robustness. See EVM User's Guide for more details. Alternative OR Gate Circuit" description to the User's Guide that shows the BJT OR gate circuit with PNs and simulation results.

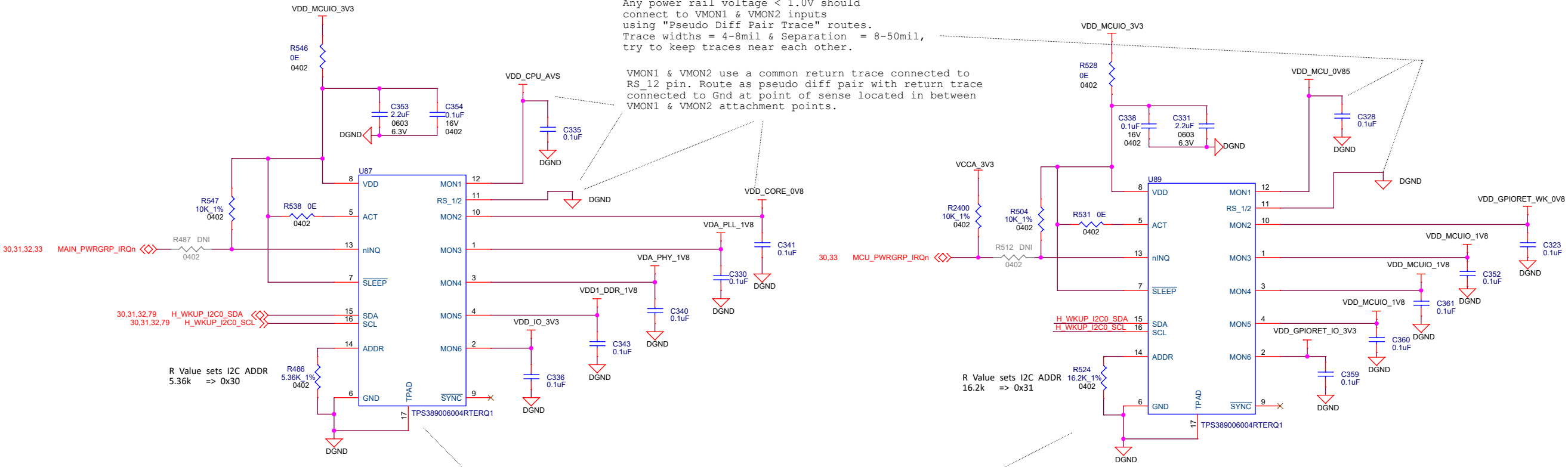


Safety Voltage Supervisors

Power rail voltage > 1.0V can connect to VMON3-6 inputs using single-ended traces. Trace widths = 4-8mil, as short as possible & try to avoid routing near HF signals.

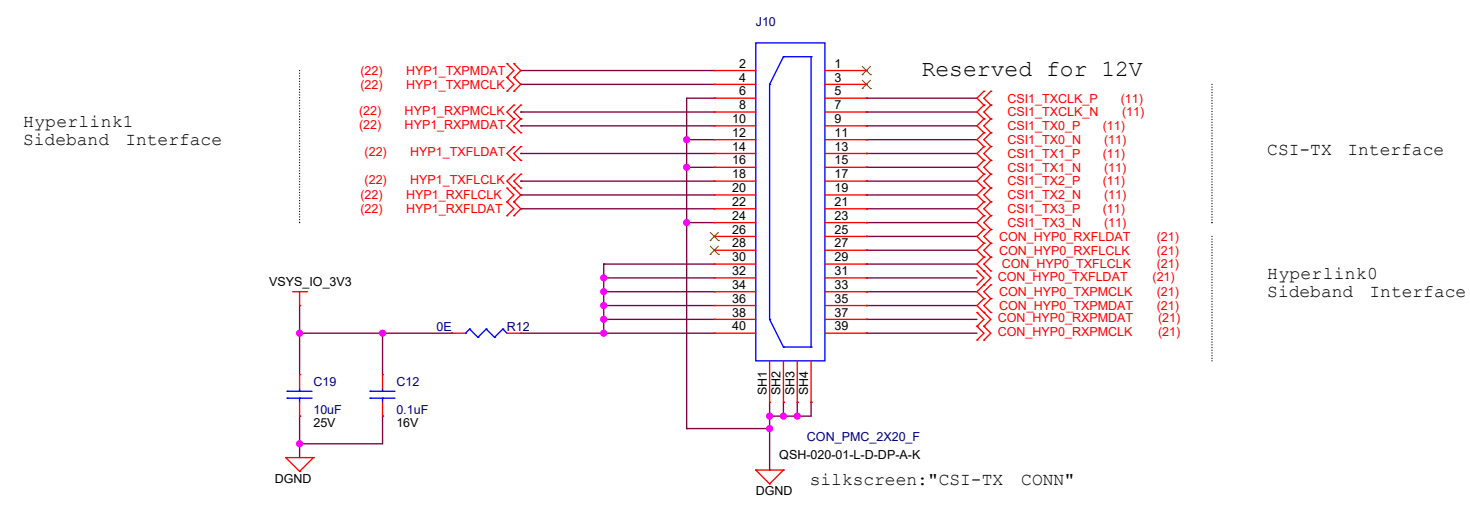
Any power rail voltage < 1.0V should connect to VMON1 & VMON2 inputs using "Pseudo Diff Pair Trace" routes. Trace widths = 4-8mil & Separation = 8-50mil, try to keep traces near each other.

VMON1 & VMON2 use a common return trace connected to RS_12 pin. Route as pseudo diff pair with return trace connected to Gnd at point of sense located in between VMON1 & VMON2 attachment points.

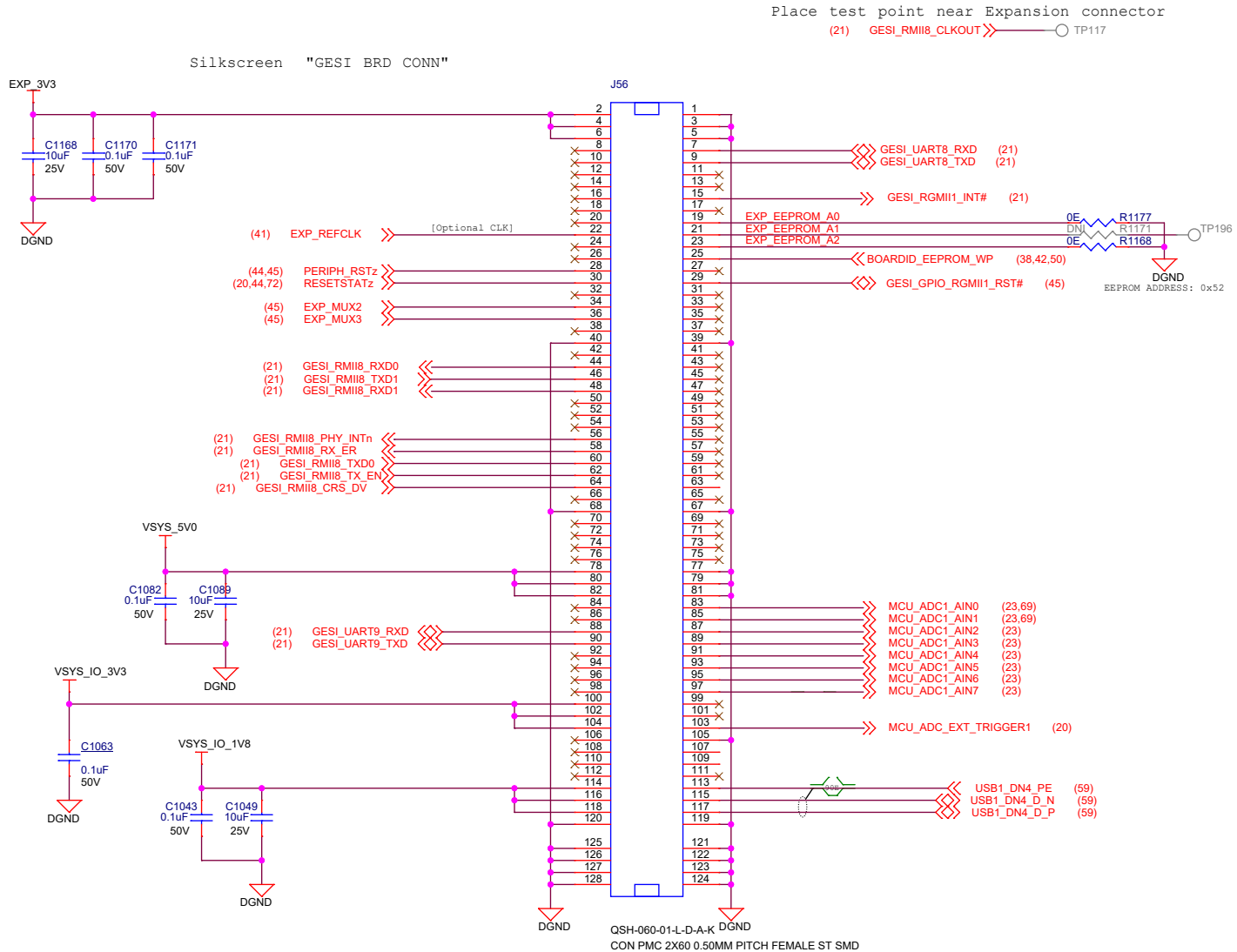
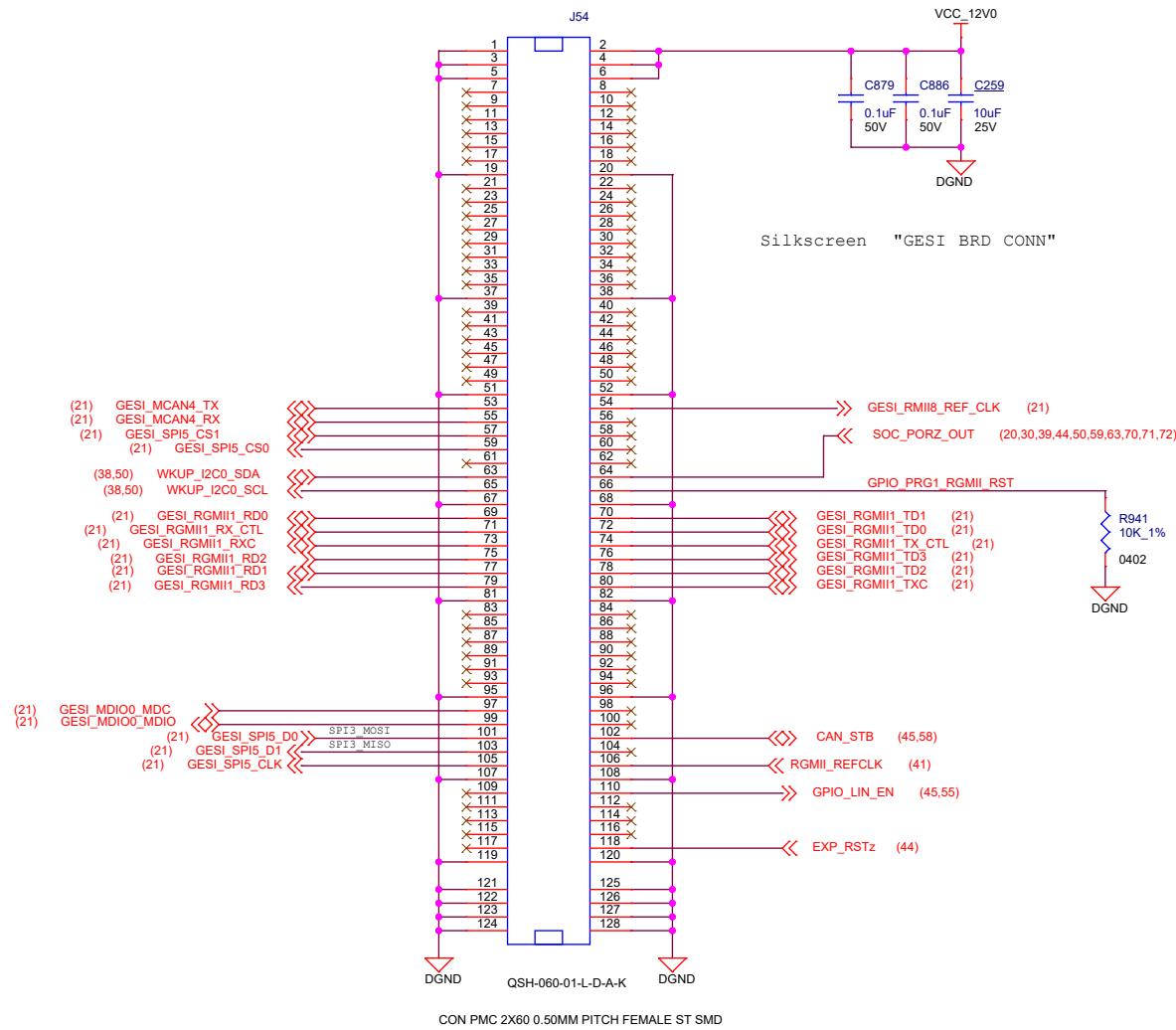


- Before SVS-A (U87) & SVS-B (U89) VMON system integration:
1. DNI R487 & R512 to avoid possible unwanted SVS IRQs
 2. Install 10k Rpu R547 to pull-up SVS-A (U87) nIRQ for testing
 3. Install 10k Rpu R504 to pull-up SVS-B (U89) nIRQ for SVS-B testing
 4. Add 10k Rpu R2400 to pull up MCU_PWRGRP_IRQn net while SVS-B is isolated for initial testing.
- After verifying valid SVS-A & SVS-B VMON operation:
1. Install R487 & R512 with 0-ohms to connect IRQs to PMIC GPIOs
 2. DNI Rpu R547 & R2400
(R547 is not needed since MAIN_PWRGRP_IRQn net has a Rpu at discrete voltage translator used to enable HCPS bucks with VDA DLL 0V8.)
 3. Install 10k Rpu R504

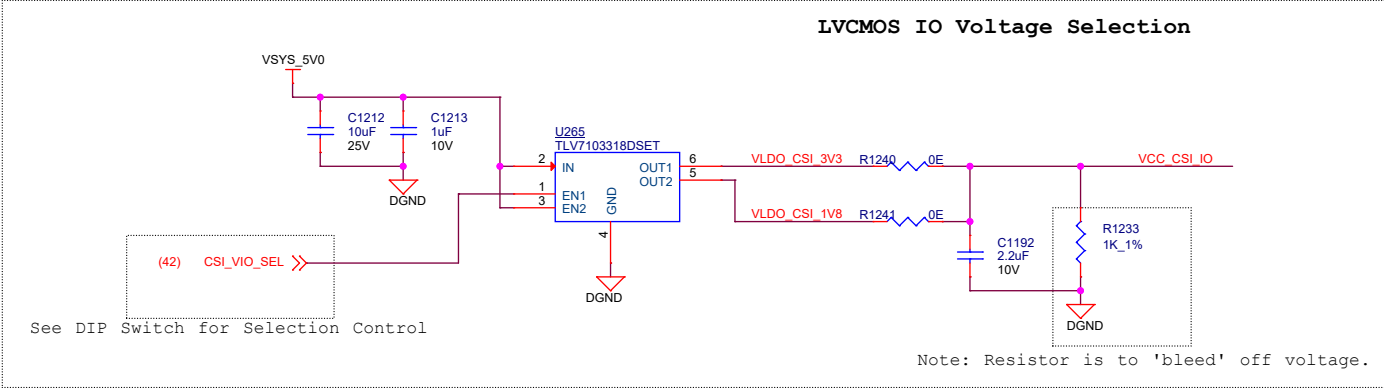
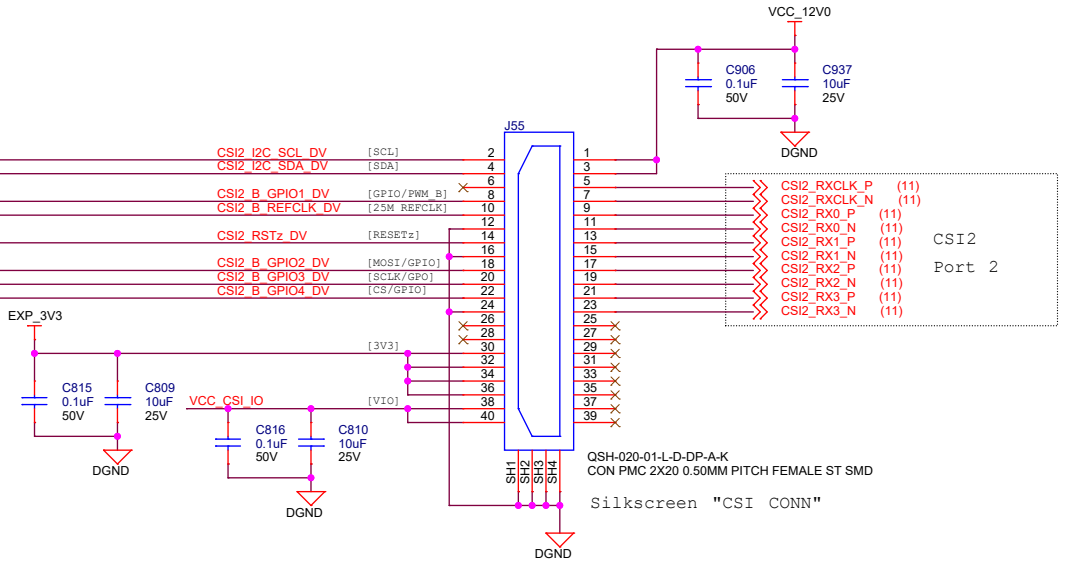
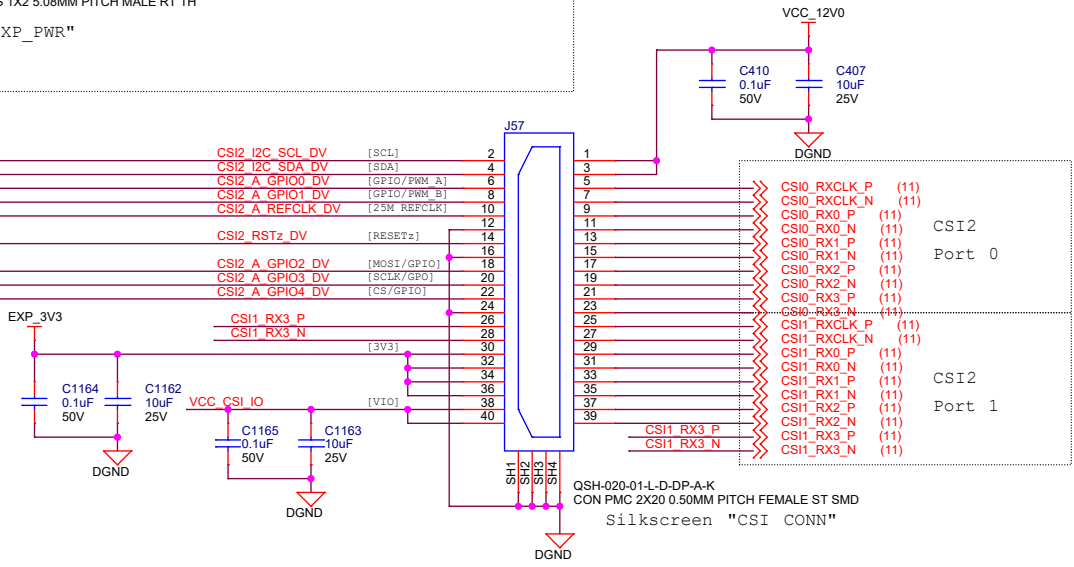
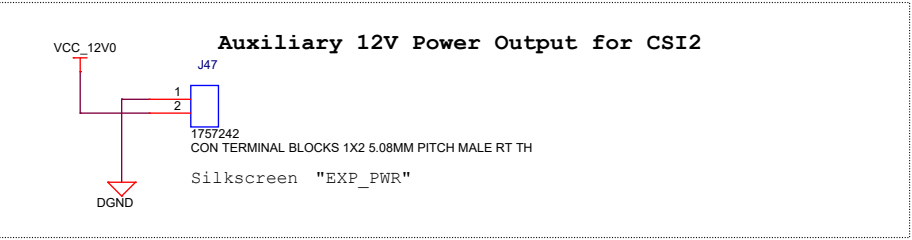
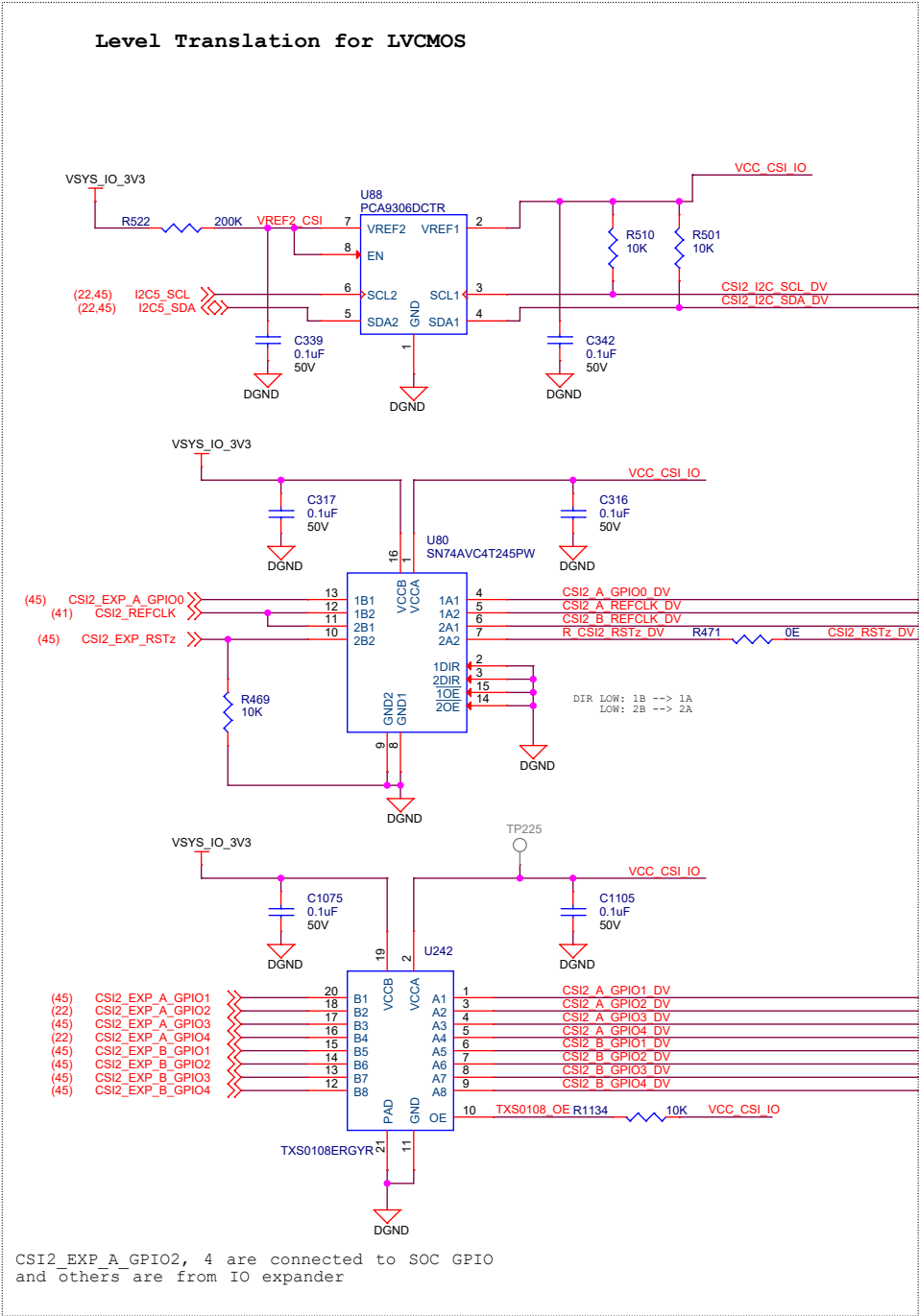
HYPERLINK SIDEBAND CONNECTOR



GESI_EXP_CONN

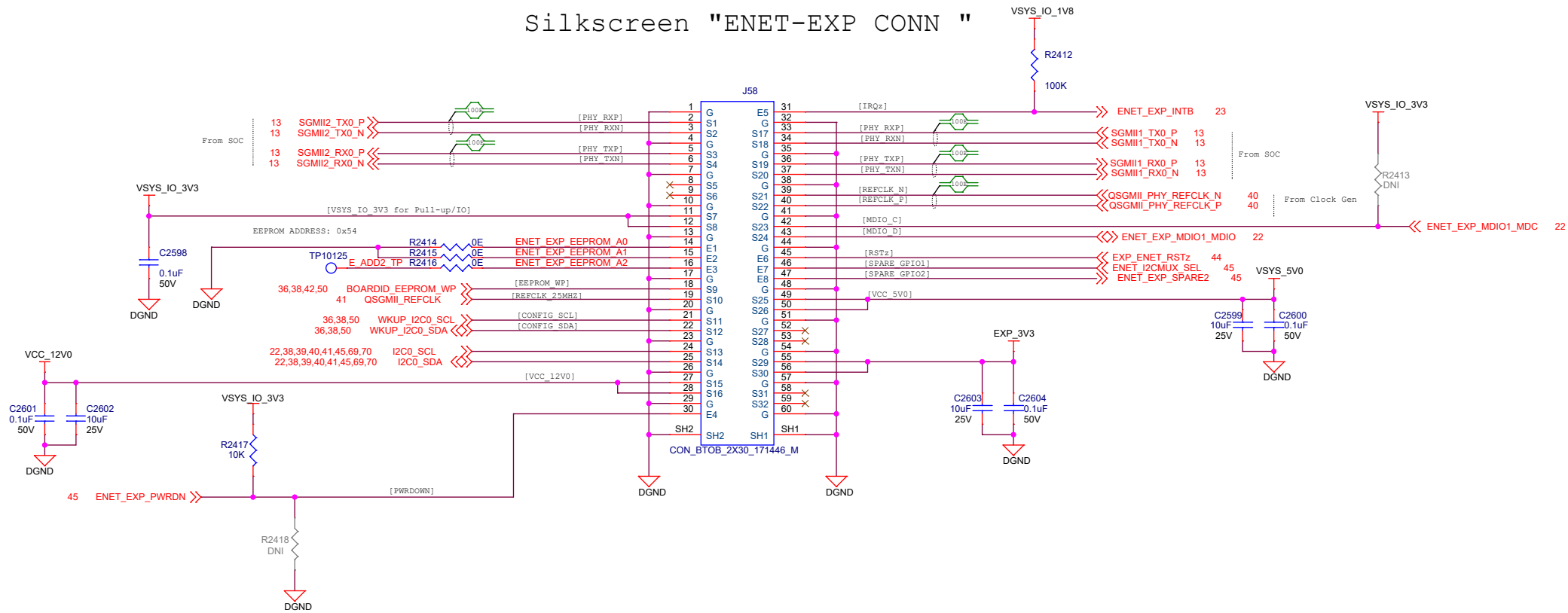


CSI2 EXPANSION CONNECTORS

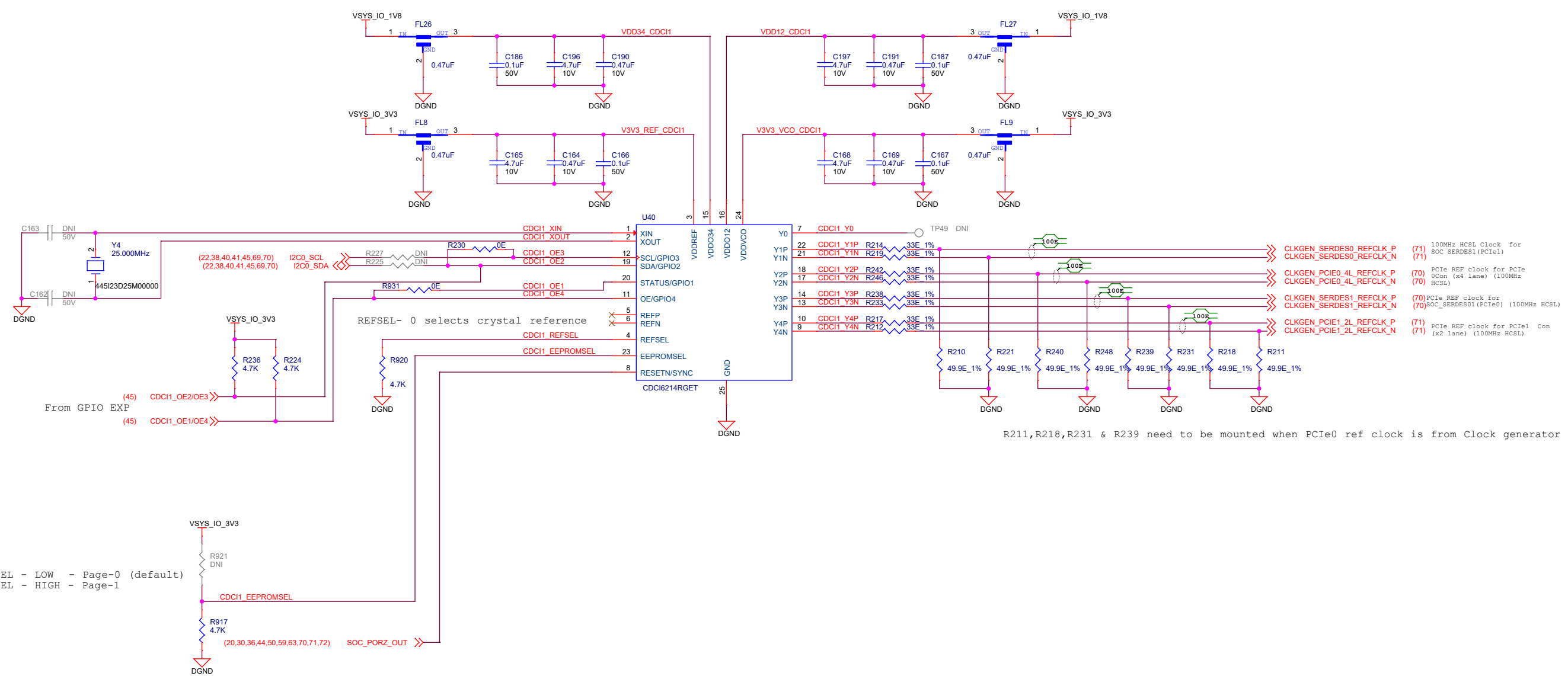


ENET EXPANSION CONNECTOR

Silkscreen "ENET-EXP CONN "

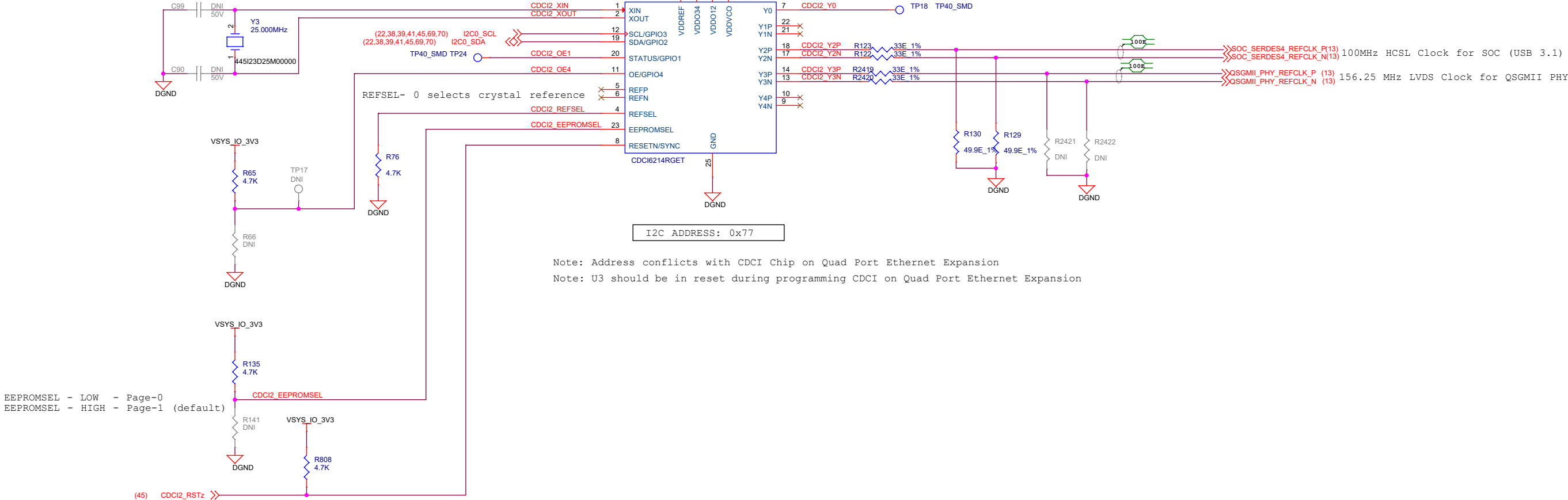


SERDES CLOCK GENERATOR #1

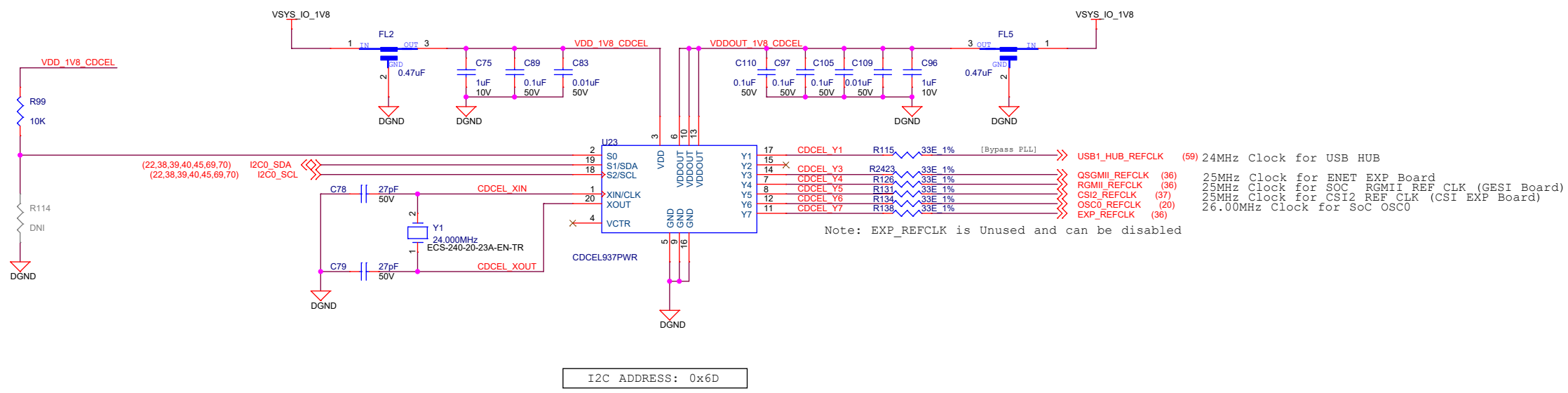


EEPROMSEL - LOW - Page-0 (default)
EEPROMSEL - HIGH - Page-1

SERDES CLOCK GENERATOR #2

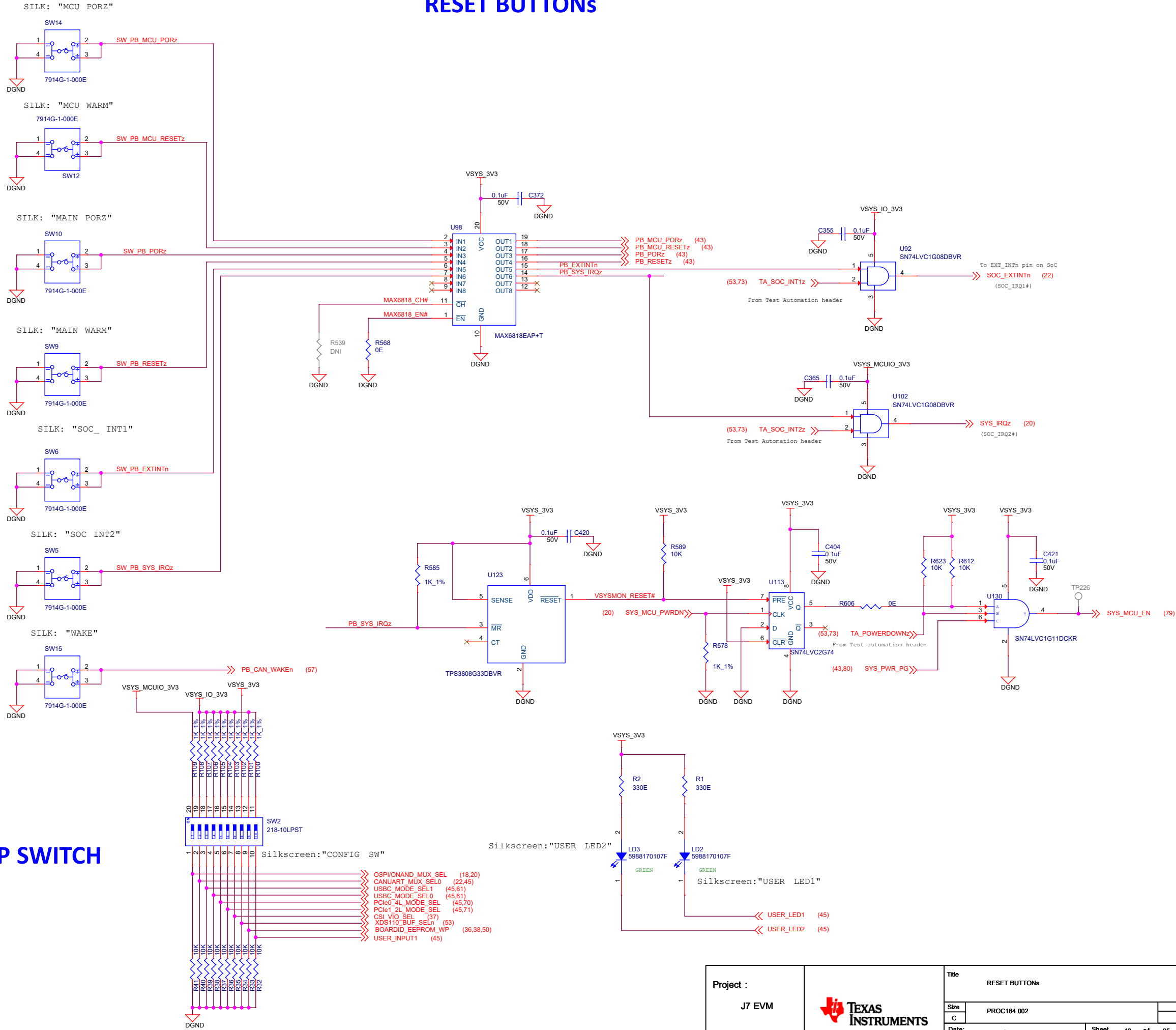


PERIPHERAL CLOCK GENERATOR



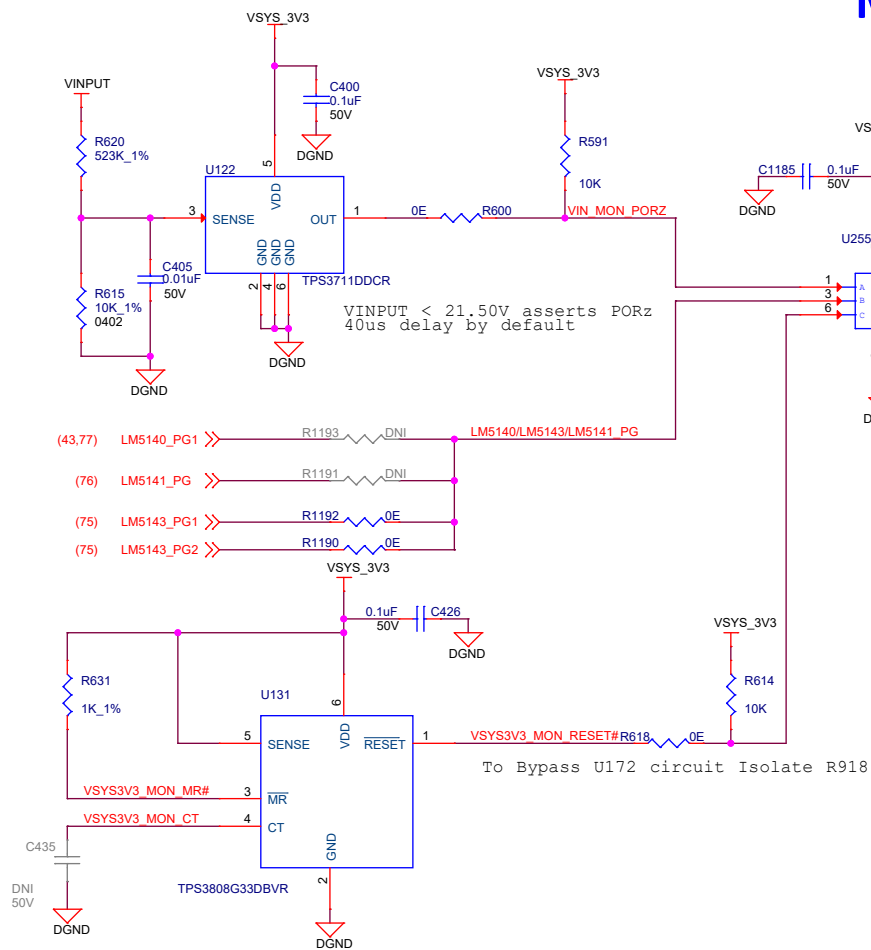
RESET BUTTONs

CONFIG DIP SWITCH

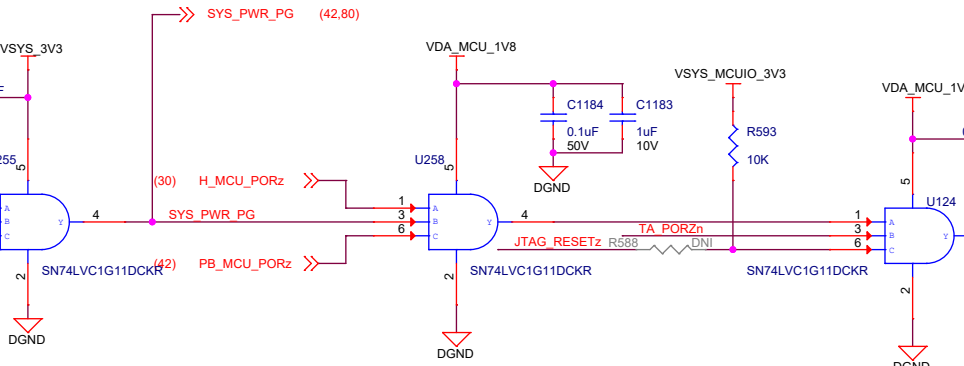


RESET INPUTS

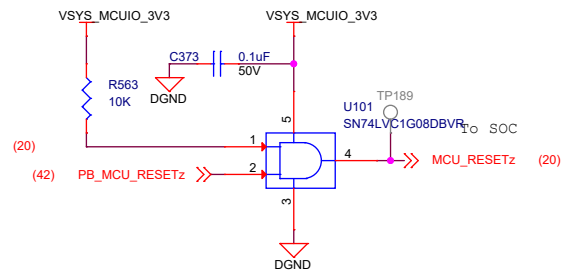
Under Voltage Monitor (VINPUT)



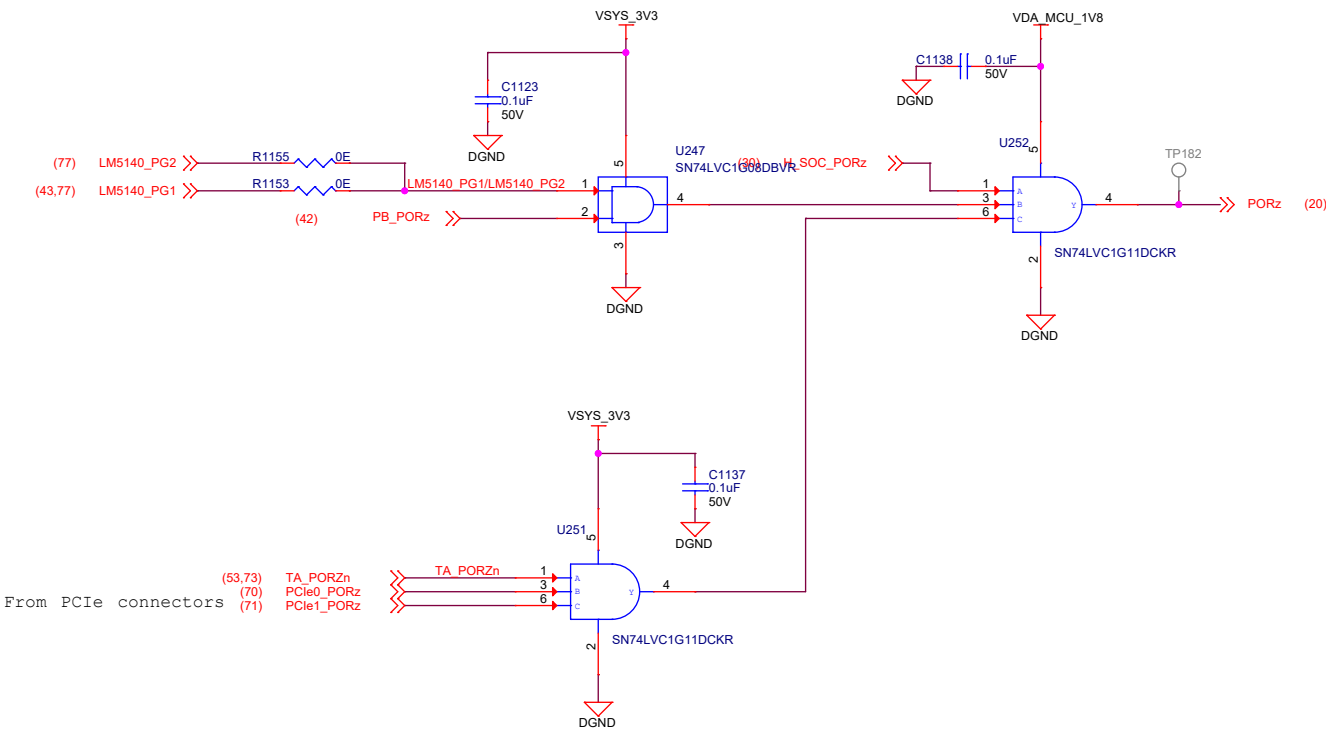
MCU PORz



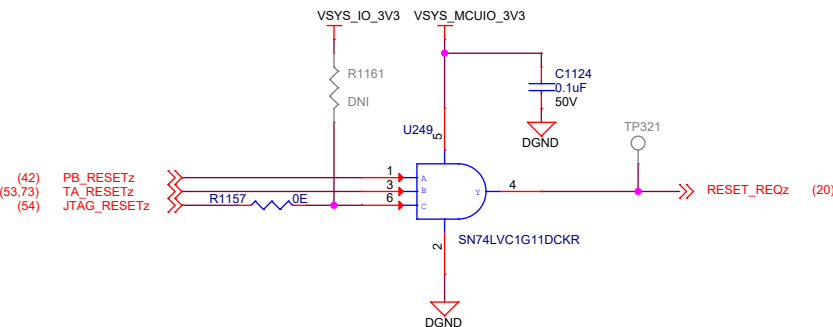
MCU_RESET



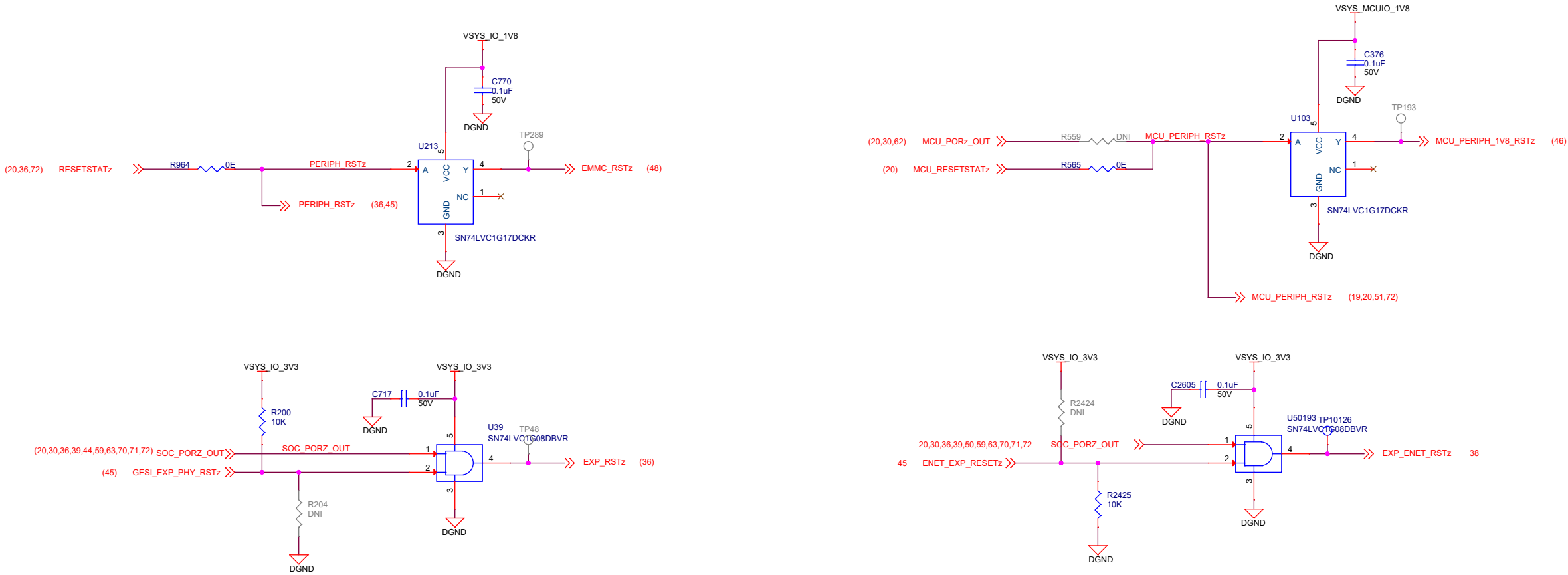
SOC PORz



SOC RESET

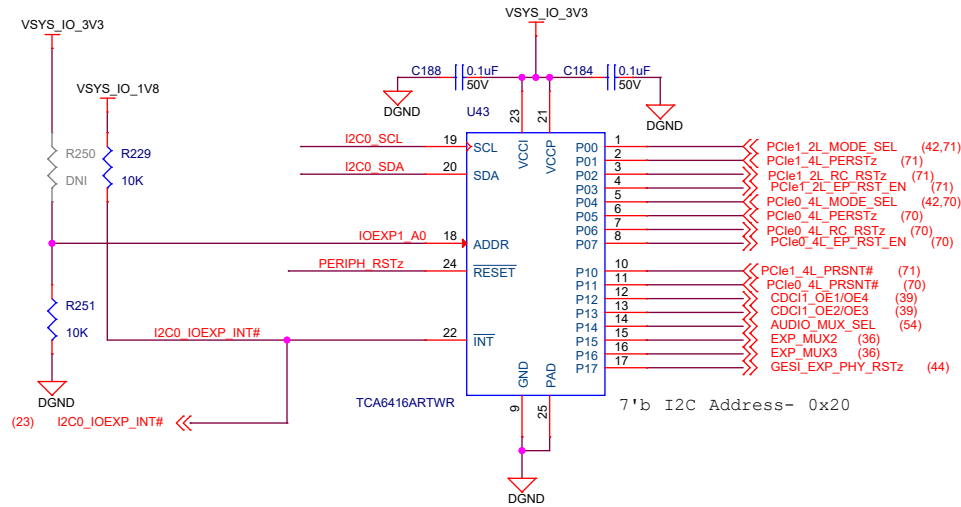


RESET OUTPUTS

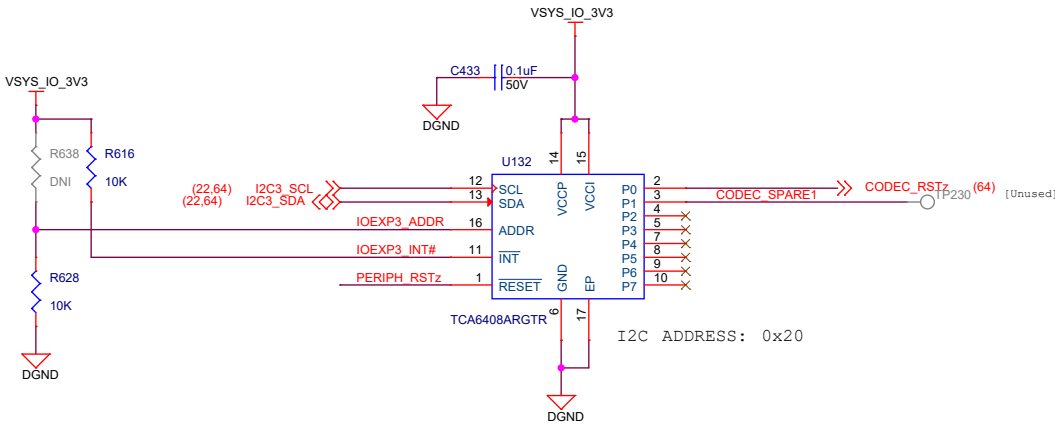


GPIO EXPANDERS

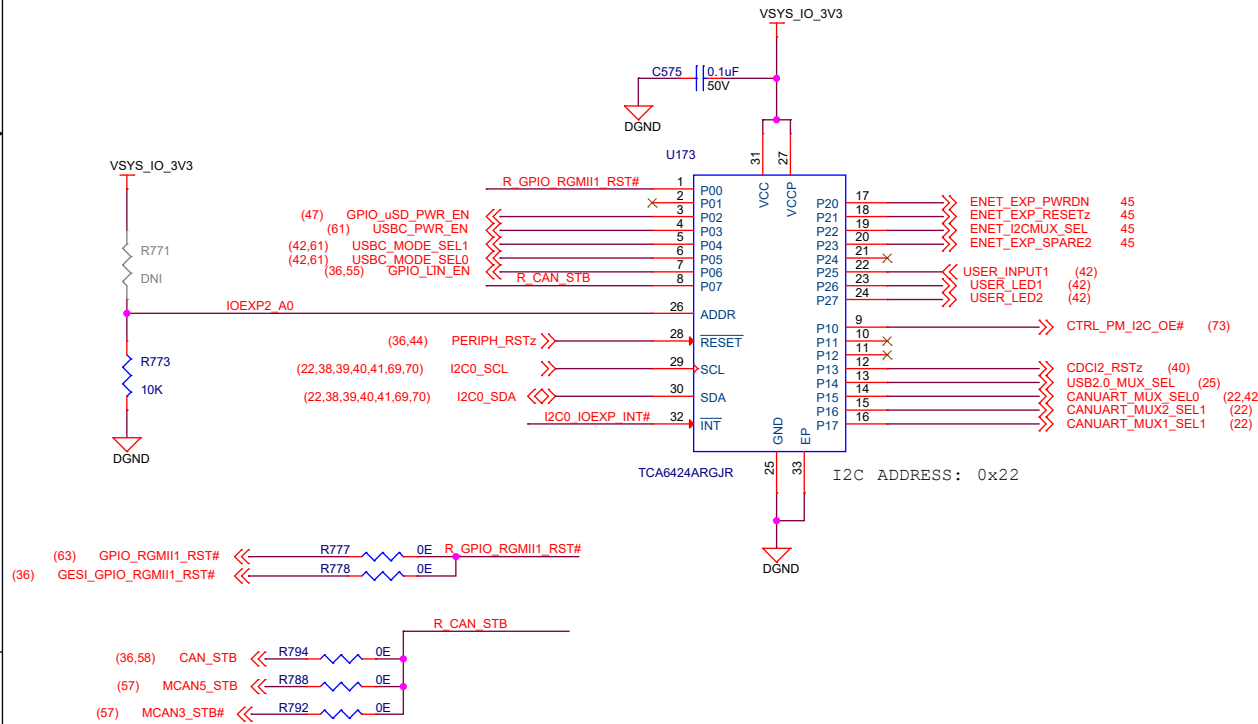
I2C GPIO EXPANDER1



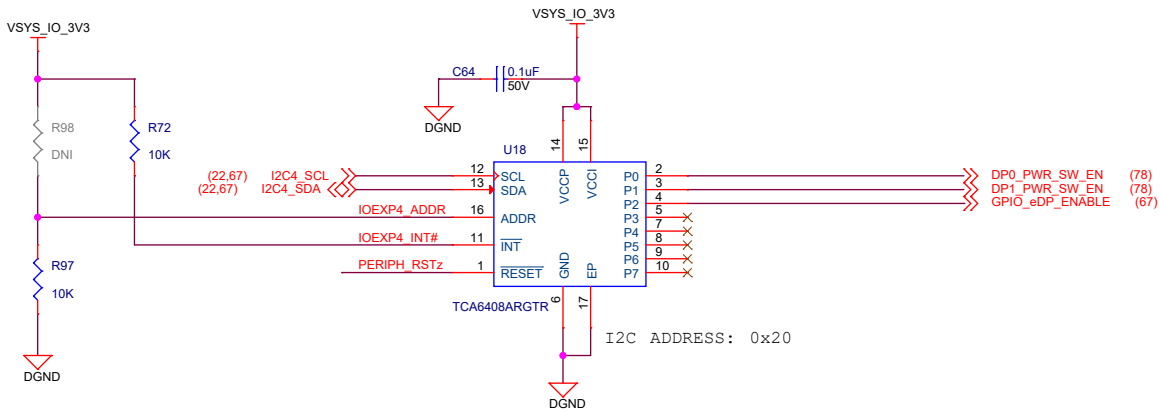
I2C GPIO EXPANDER3



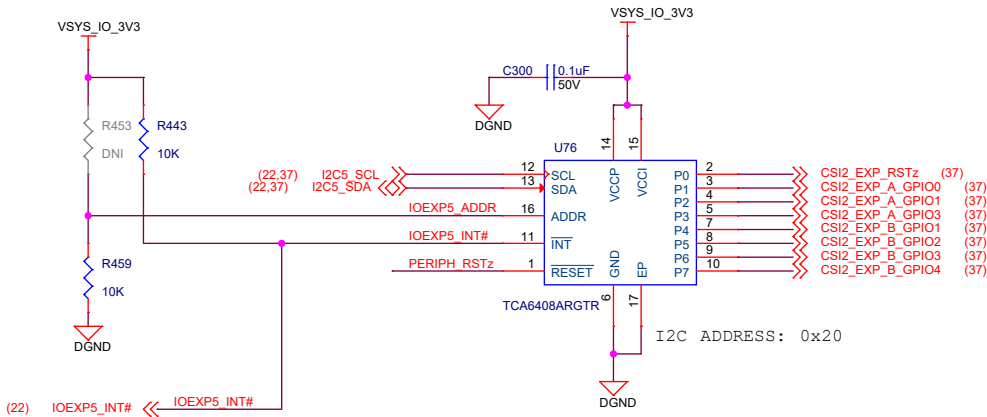
I2C GPIO EXPANDER2



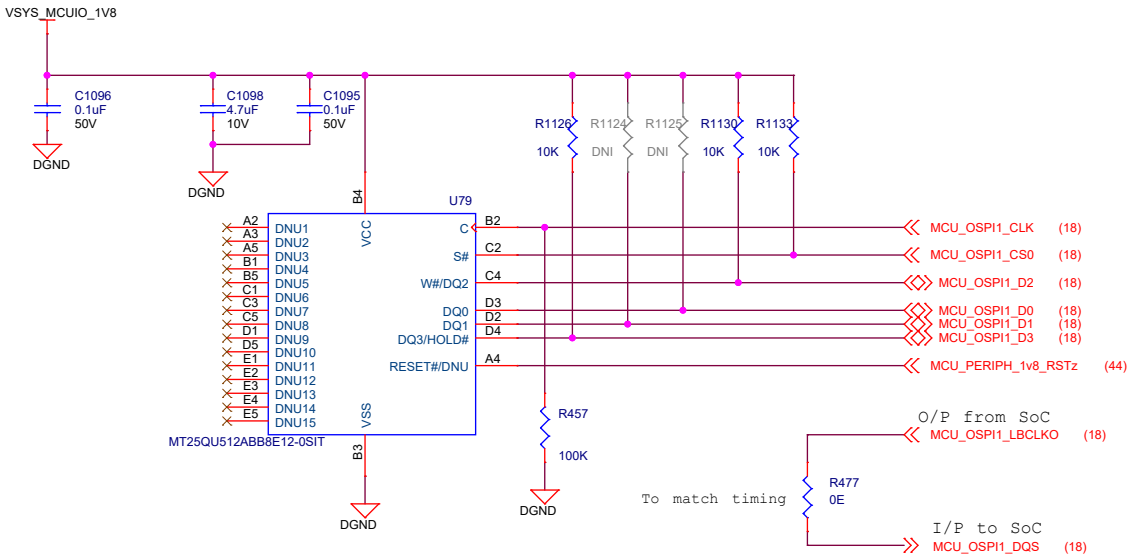
I2C GPIO EXPANDER4



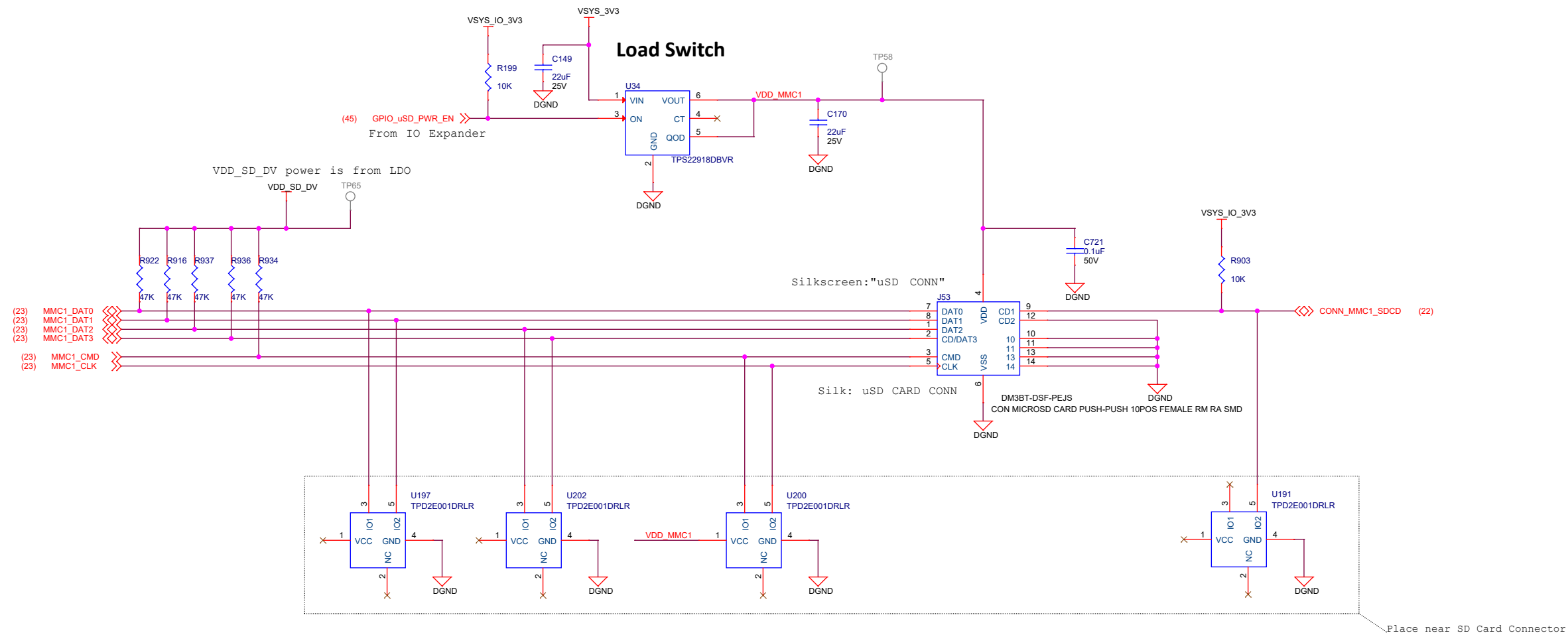
I2C GPIO EXPANDERS



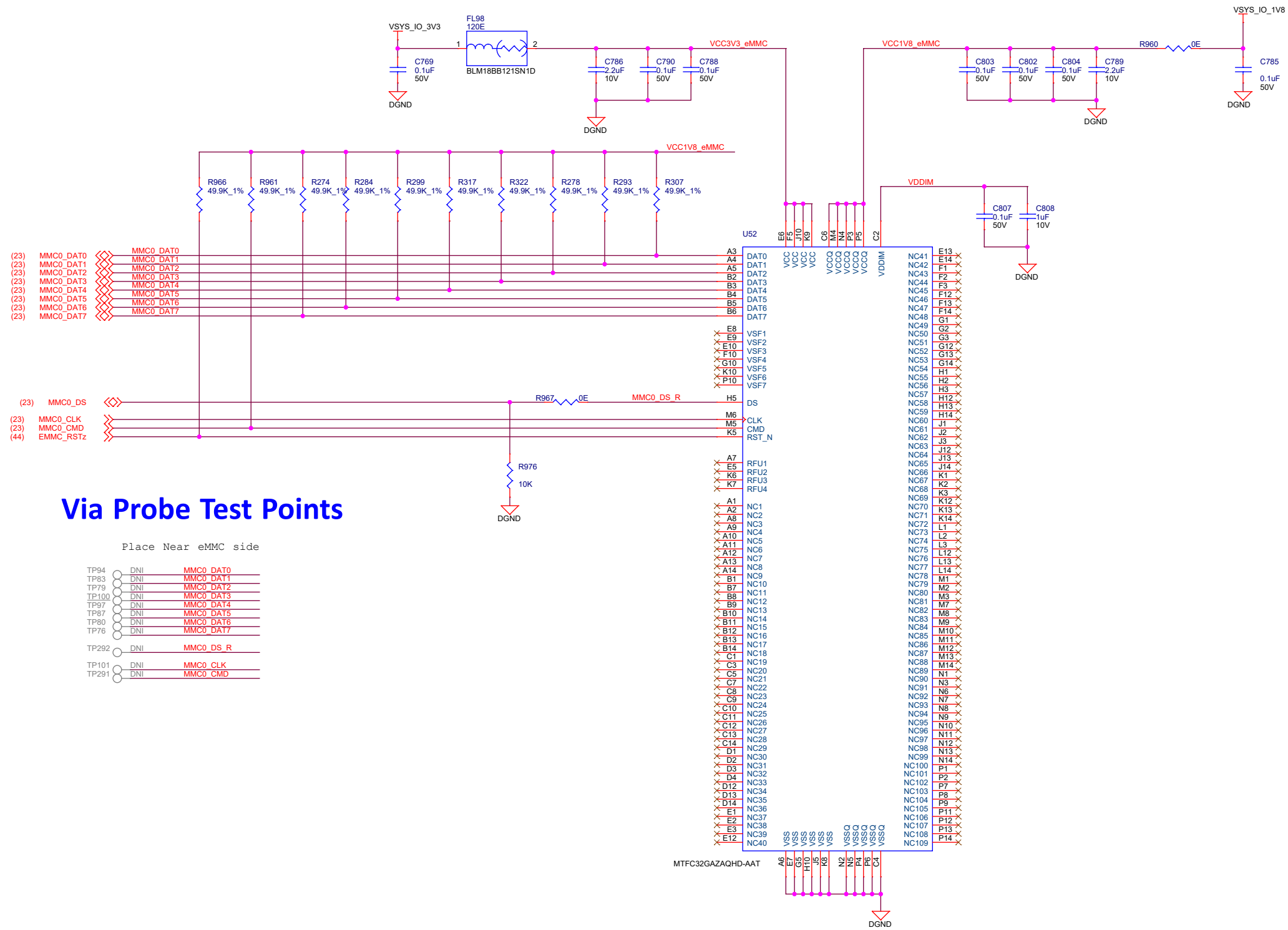
SPI NOR Flash



Micro SD CARD INTERFACE



eMMC FLASH

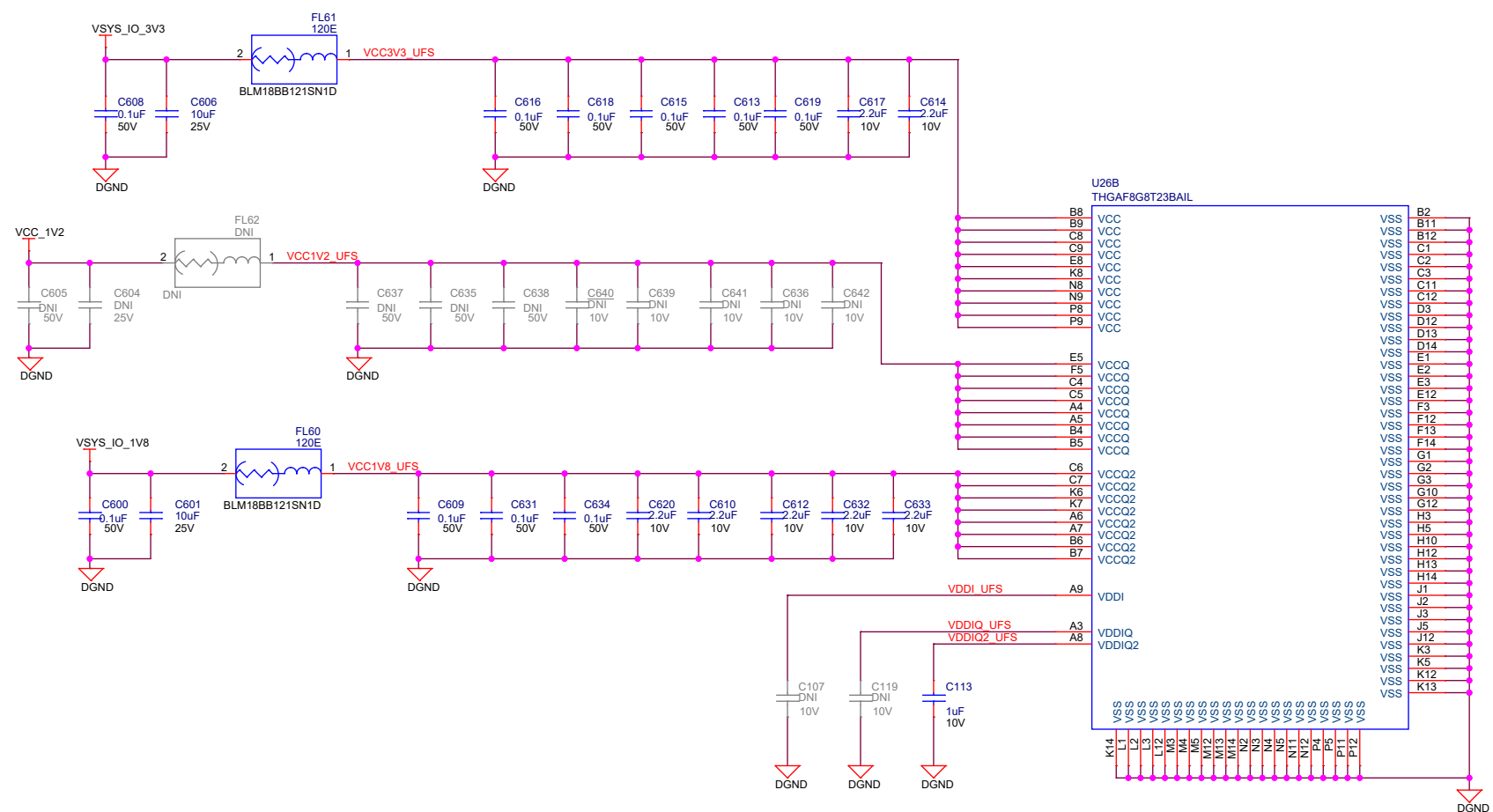
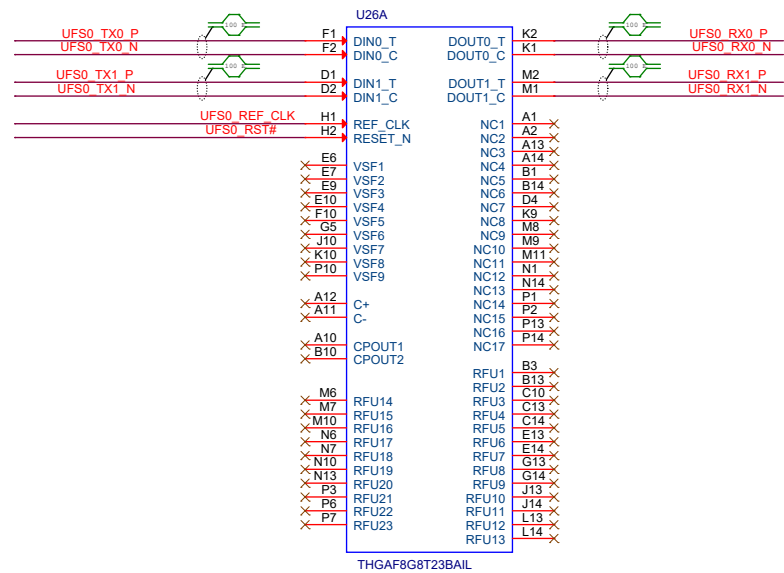
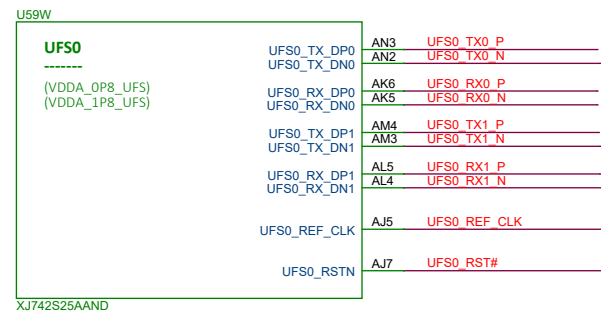


Via Probe Test Points

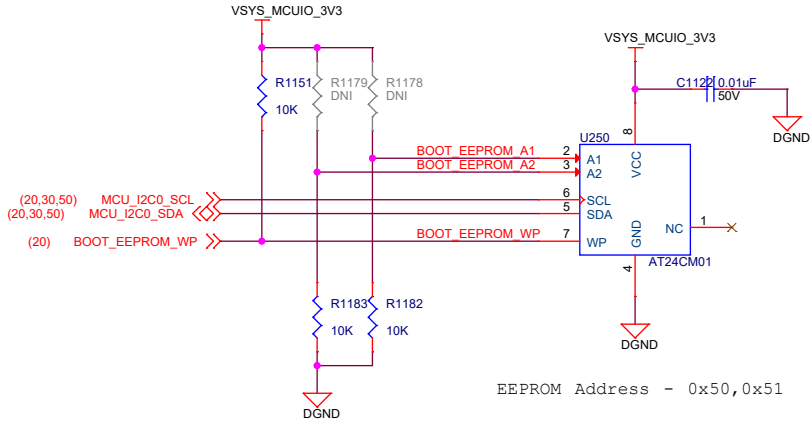
Place Near eMMC side

TP94	DNI	MMC0_DAT0
TP83	DNI	MMC0_DAT1
TP79	DNI	MMC0_DAT2
TP100	DNI	MMC0_DAT3
TP97	DNI	MMC0_DAT4
TP87	DNI	MMC0_DAT5
TP80	DNI	MMC0_DAT6
TP76	DNI	MMC0_DAT7
TP292	DNI	MMC0_DS_R
TP101	DNI	MMC0_CLK
TP291	DNI	MMC0_CMD

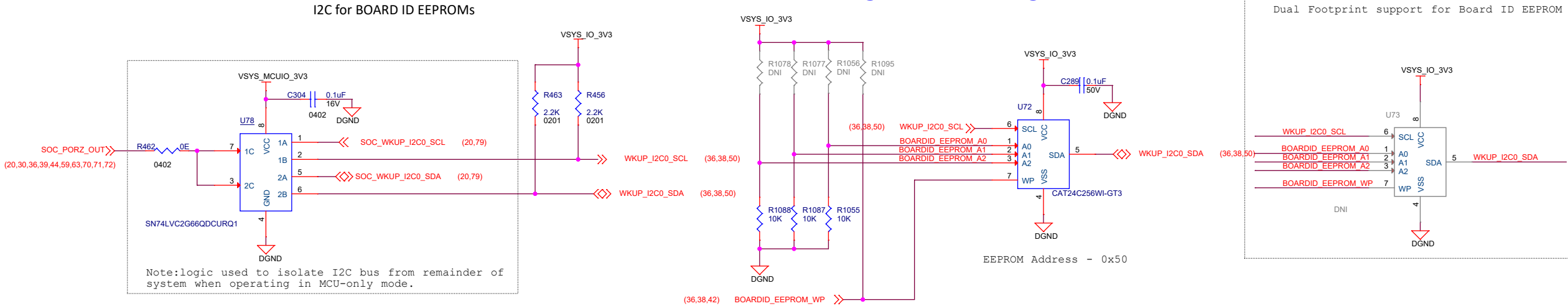
UFS FLASH



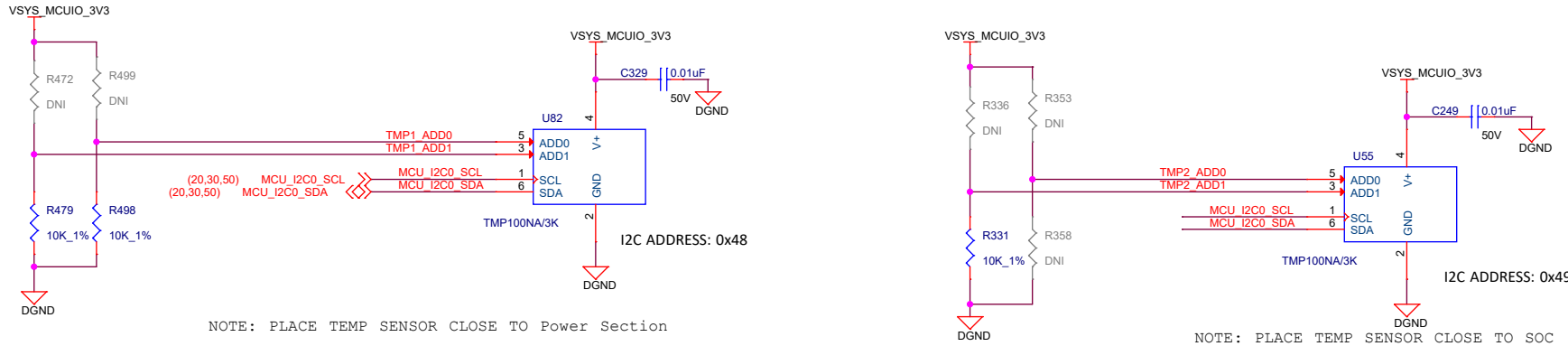
BOOT EEPROM



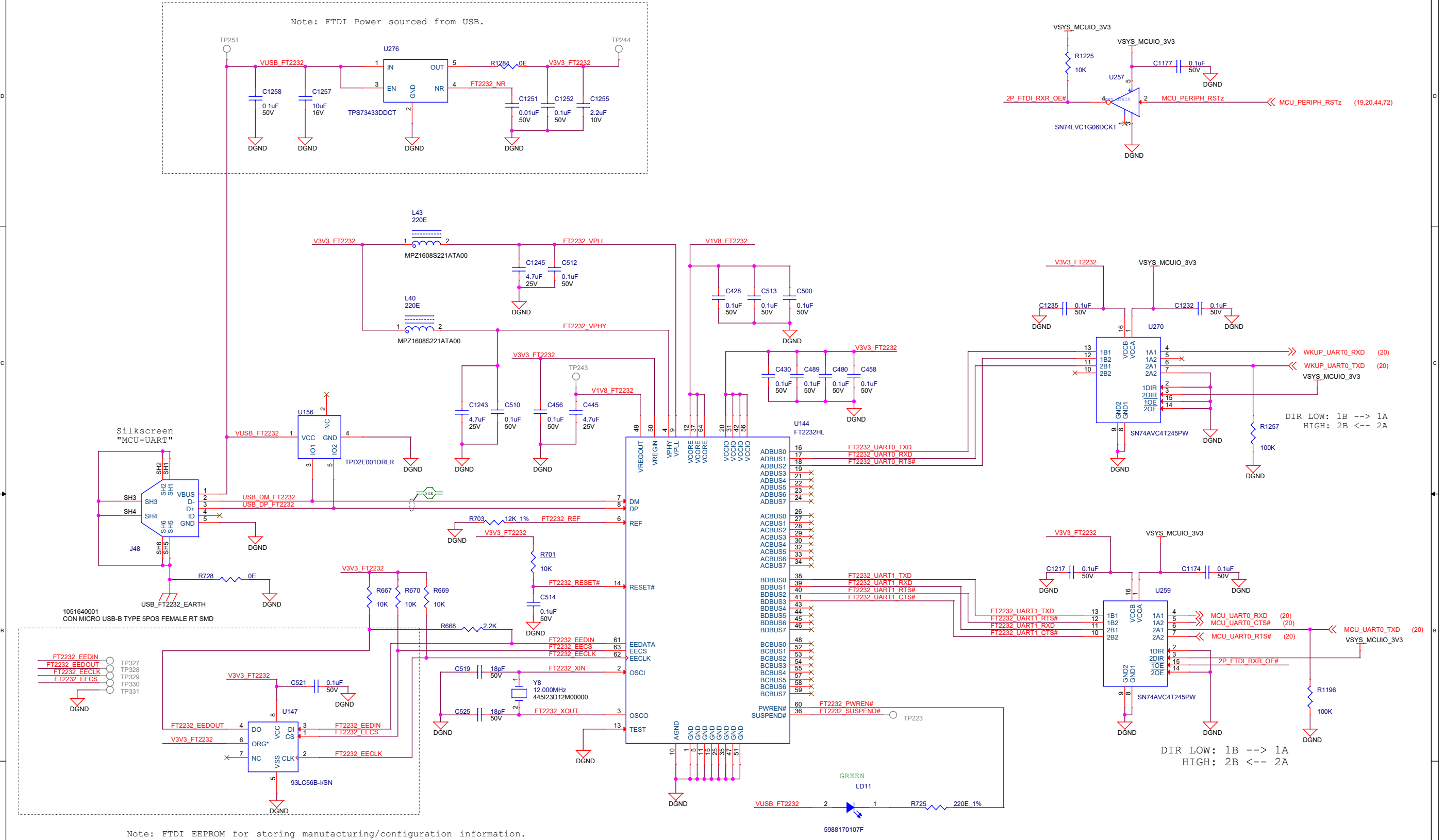
BOARD ID EEPROM



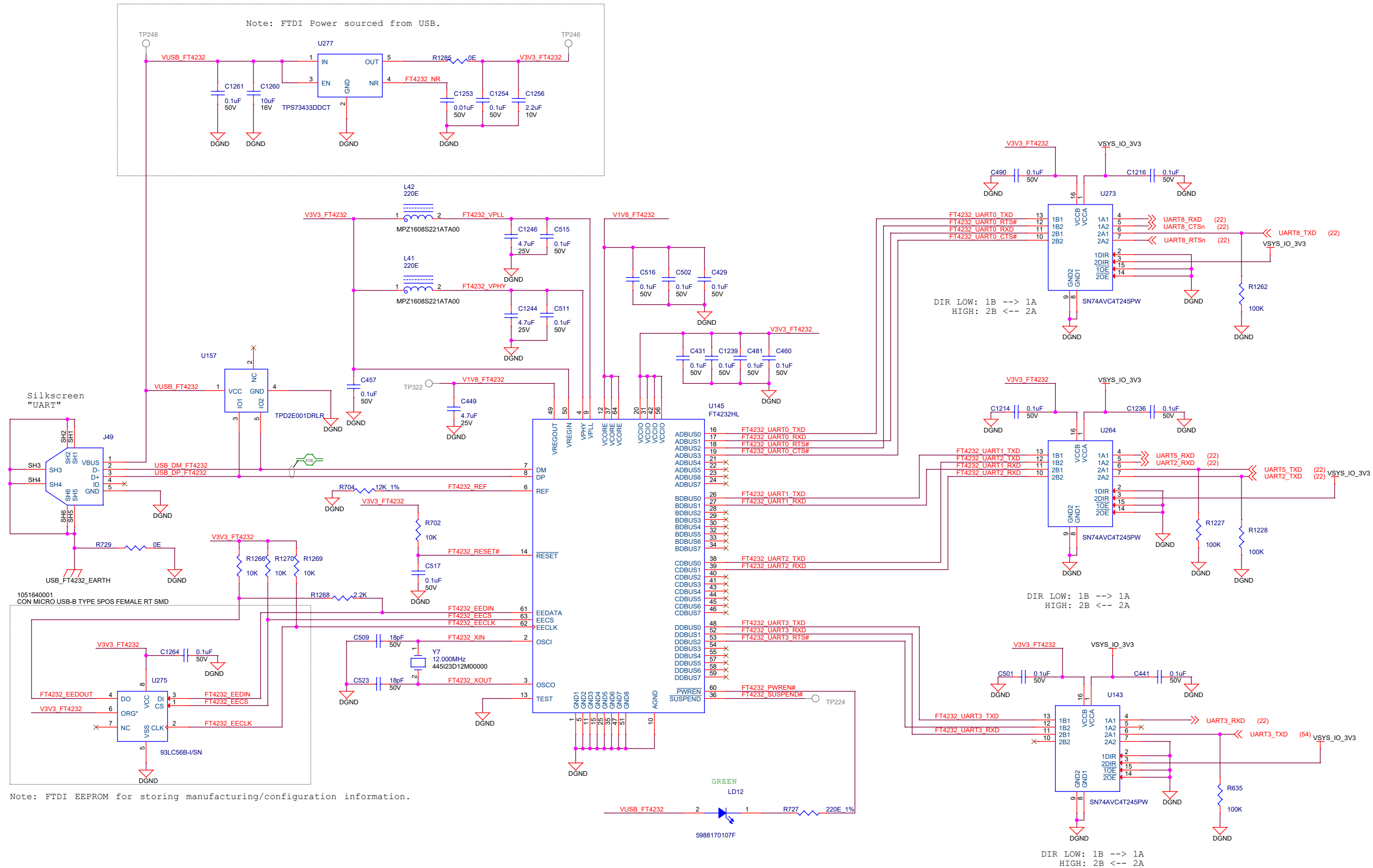
TEMPERATURE SENSORS (TI EVM Only)



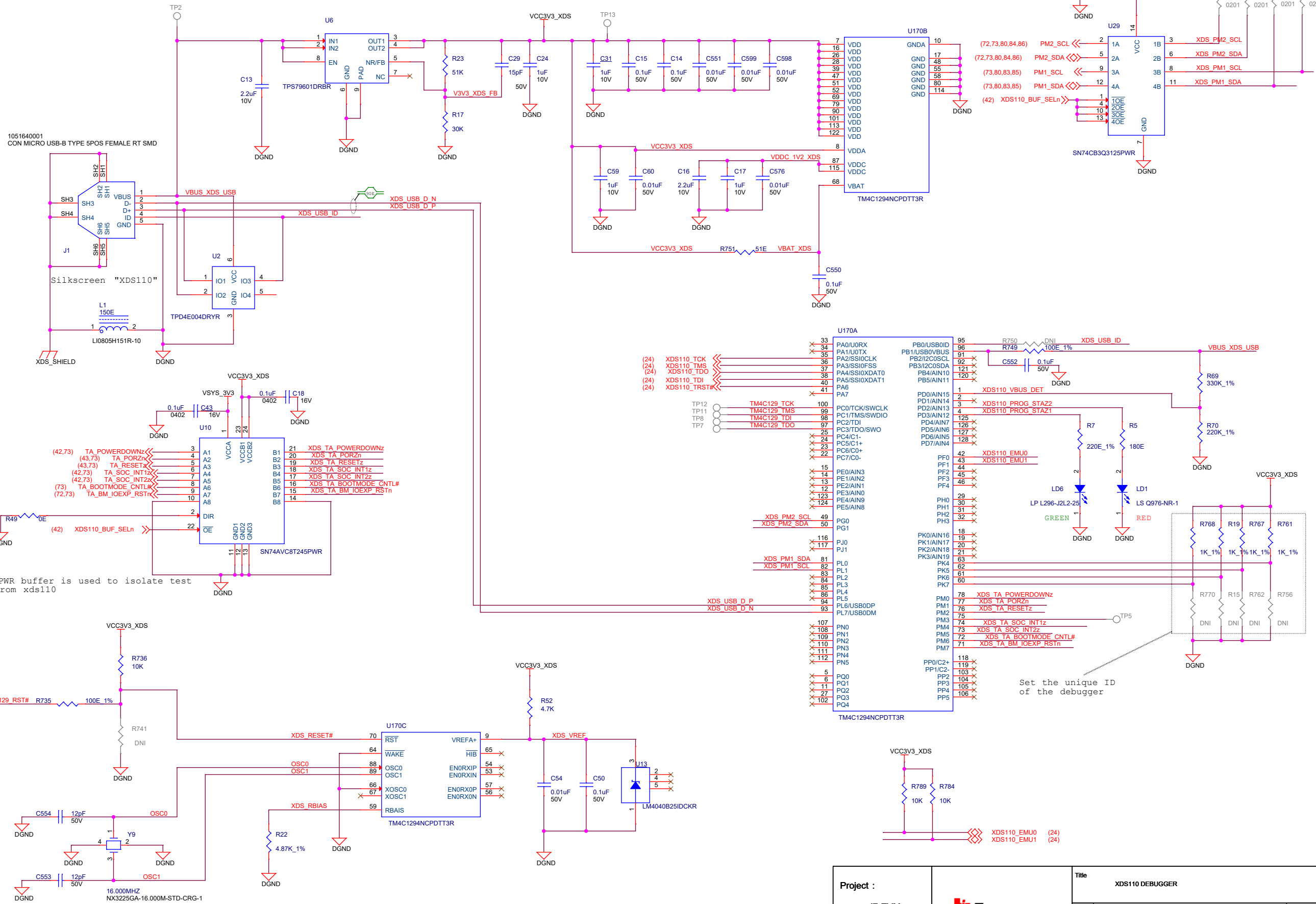
DUAL PORT FTDI



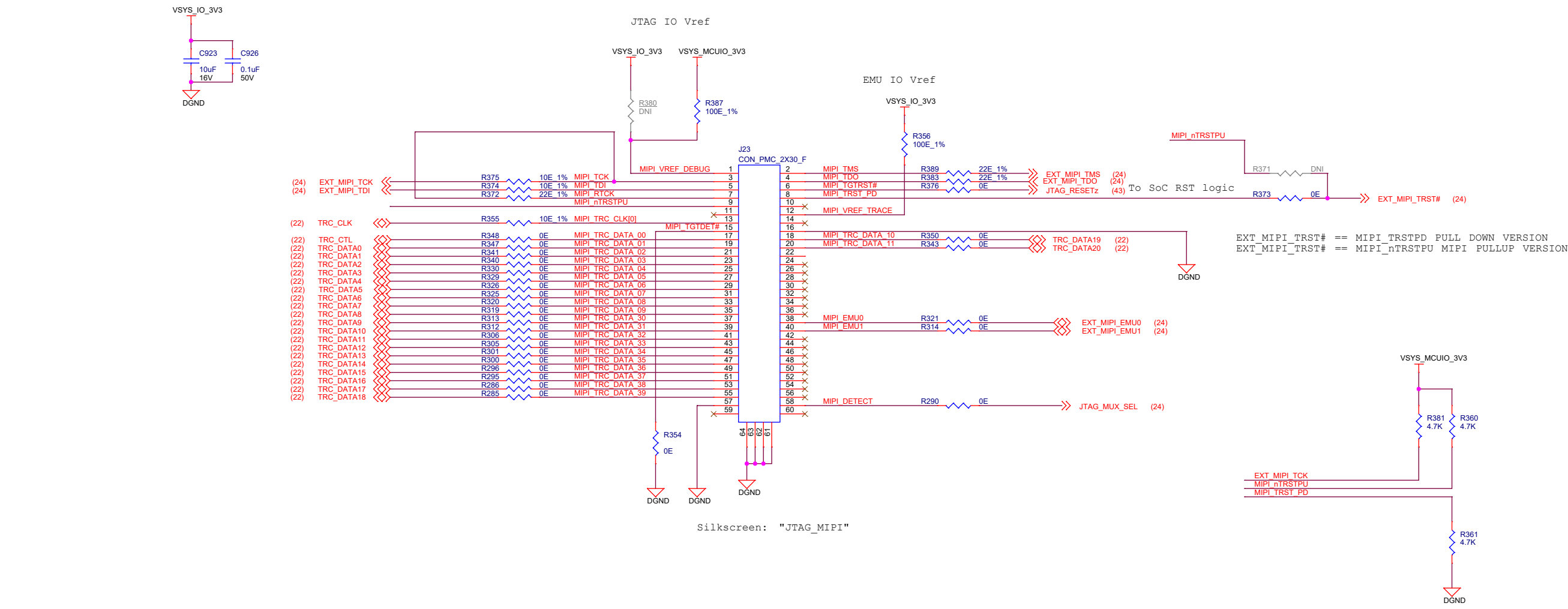
QUAD PORT FTDI



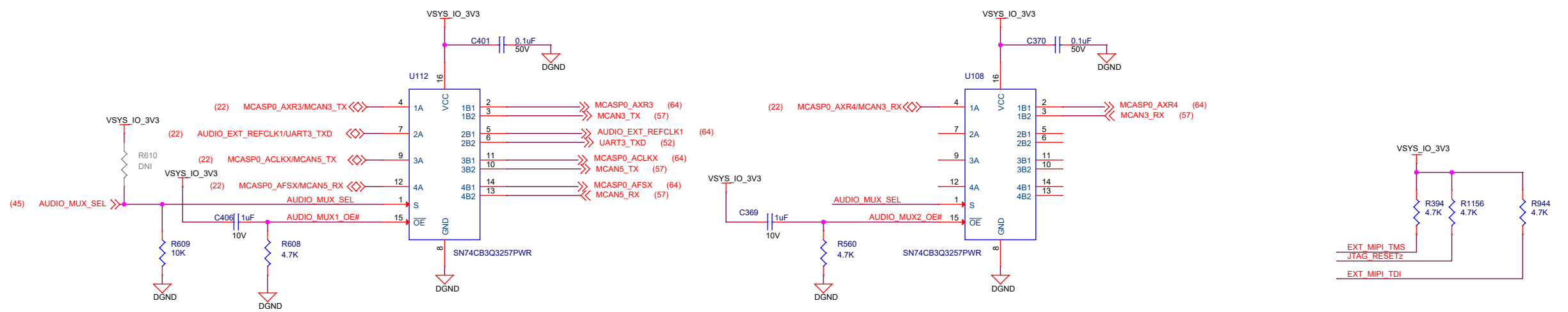
XDS110 DEBUGGER



JTAG MIPI60 CONNECTOR

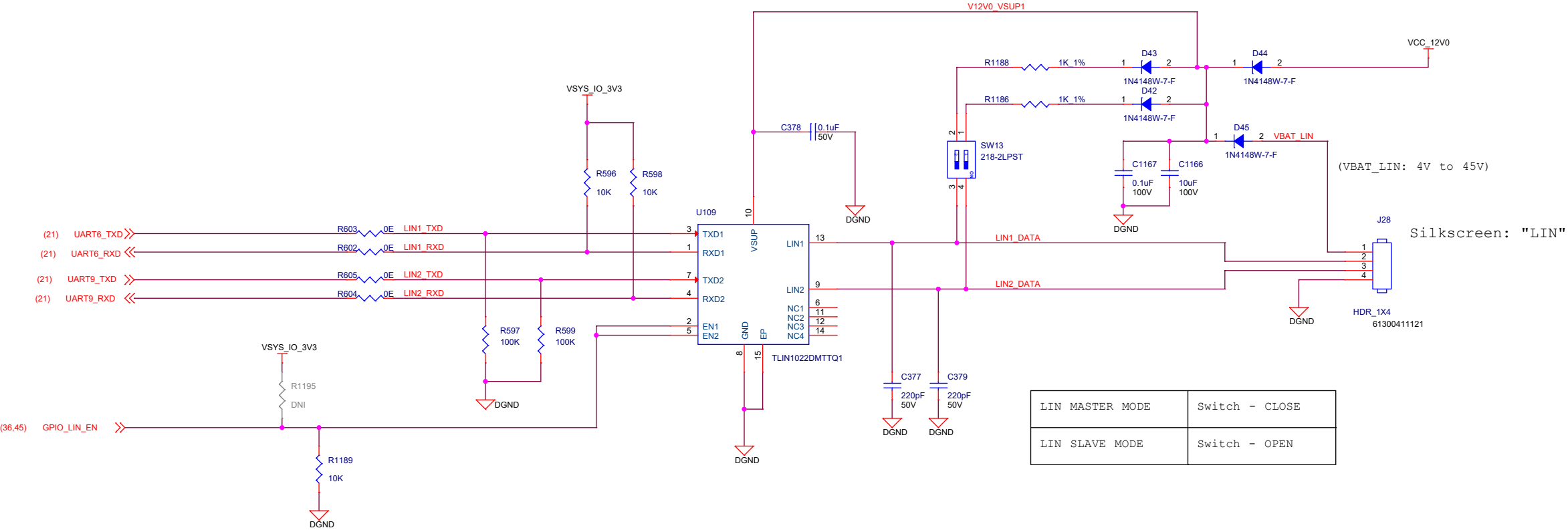


Silkscreen: "JTAG_MIPI"



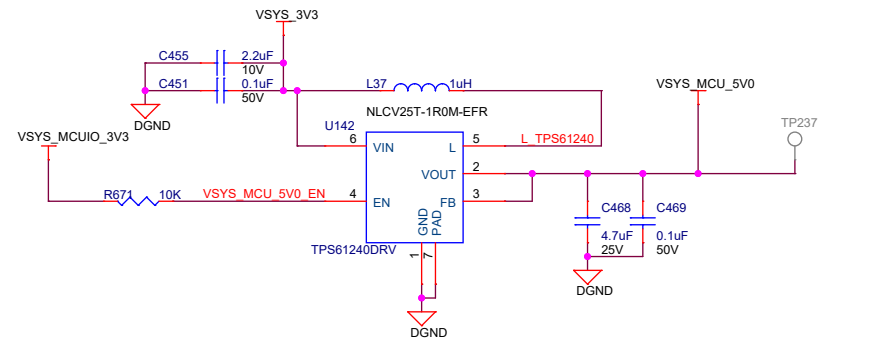
JTAG - 1:2 MUX : Truth Table

LIN INTERFACE

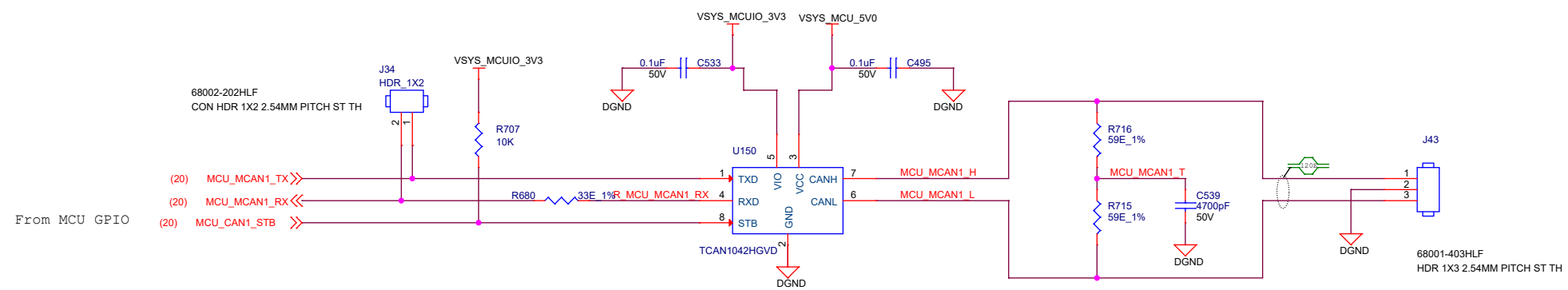
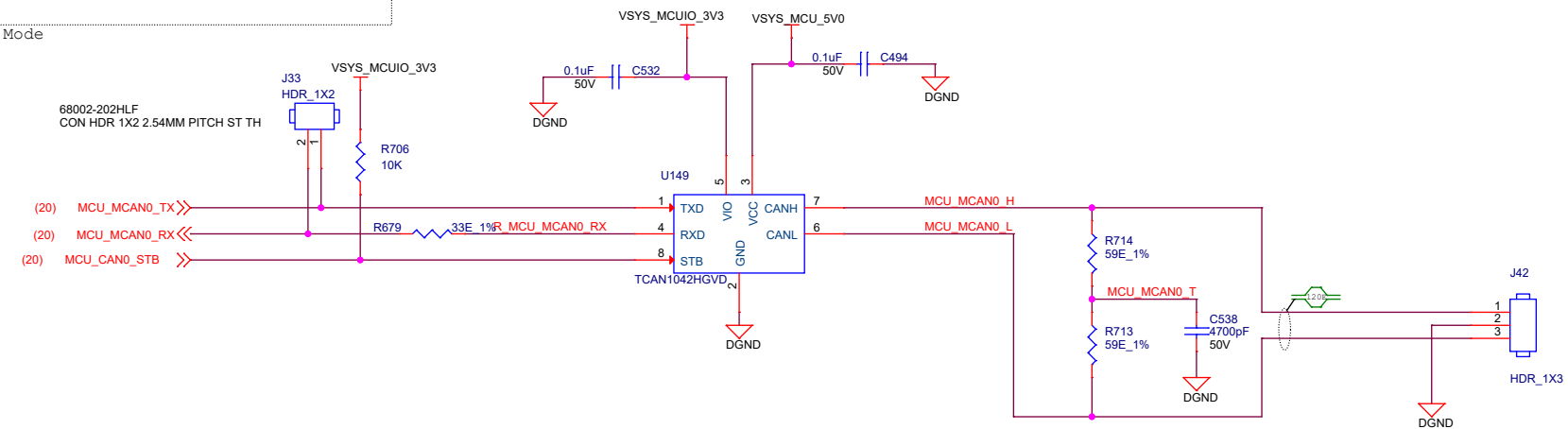


CAN TRANSCEIVERS #1-MCU DOMAIN

VSYS_MCU_5V0 GENERATION



Separate 5V0 supply required for MCU-Only Mode



Project :

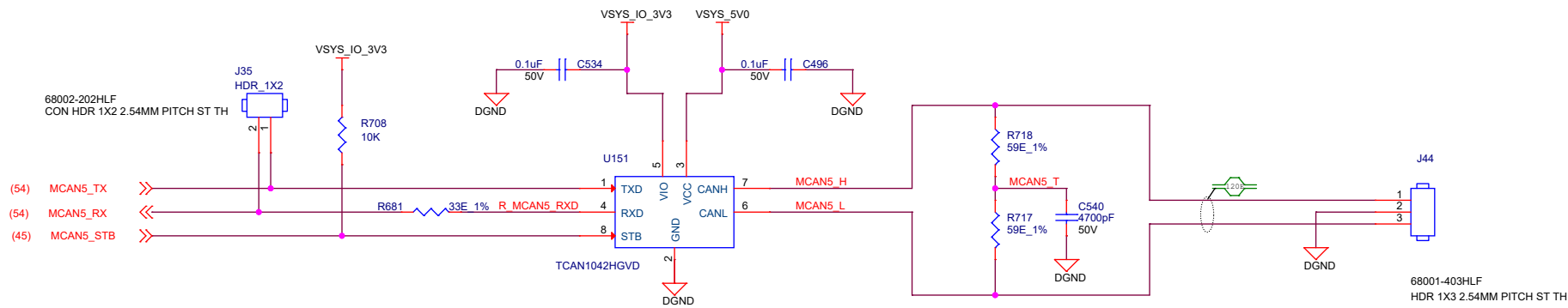
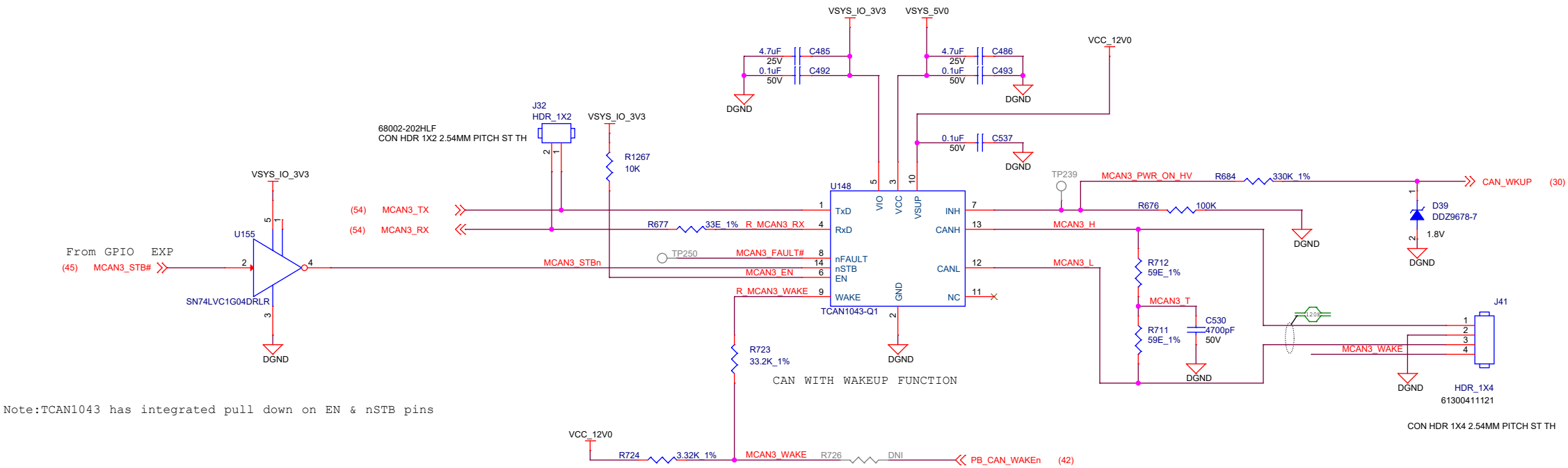
J7 EVM



Title	CAN TRANSCEIVERS #1
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Size	PROC184 002	Rev
C		E2
Date:	Thursday, August 22, 2024	Sheet 54 of 85

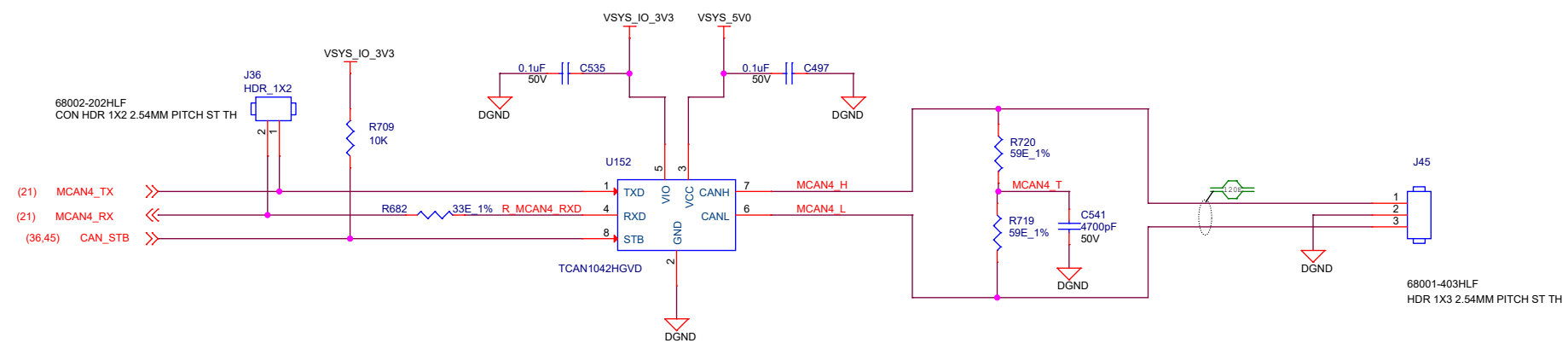
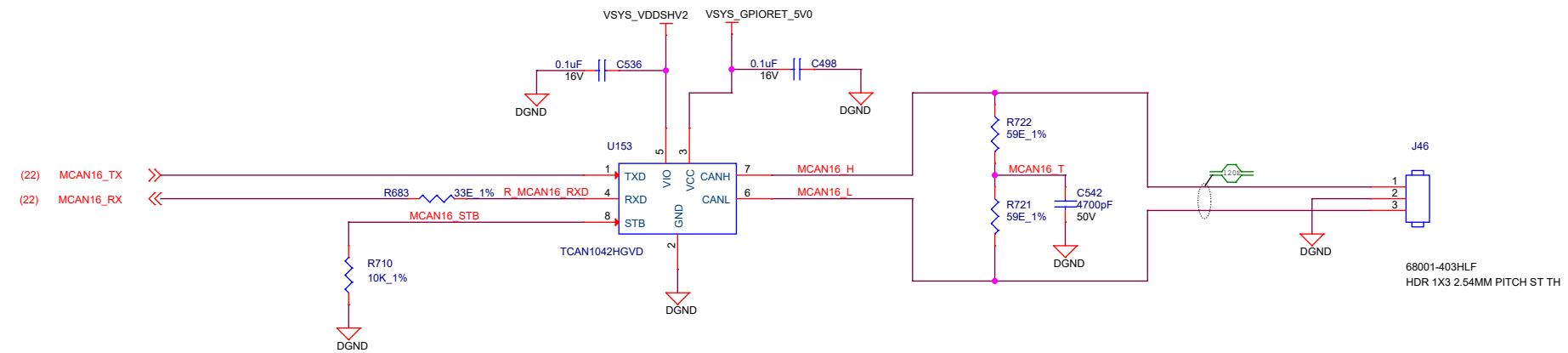
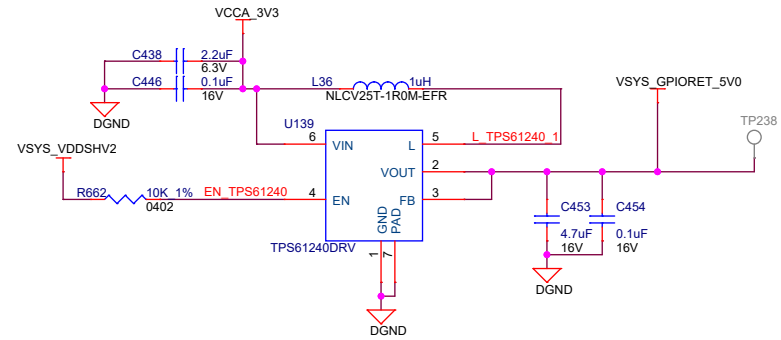
CAN TRANSCEIVERS #2-MAIN DOMAIN



CAN TRANSCEIVER

VSYS_GPIORET_5V0 GENERATION

Note: Booster convertor required for EVM due to system 5V supply shutting down in retention mode



Project :

J7 EVM



Title	CAN TRANSCEIVER #3
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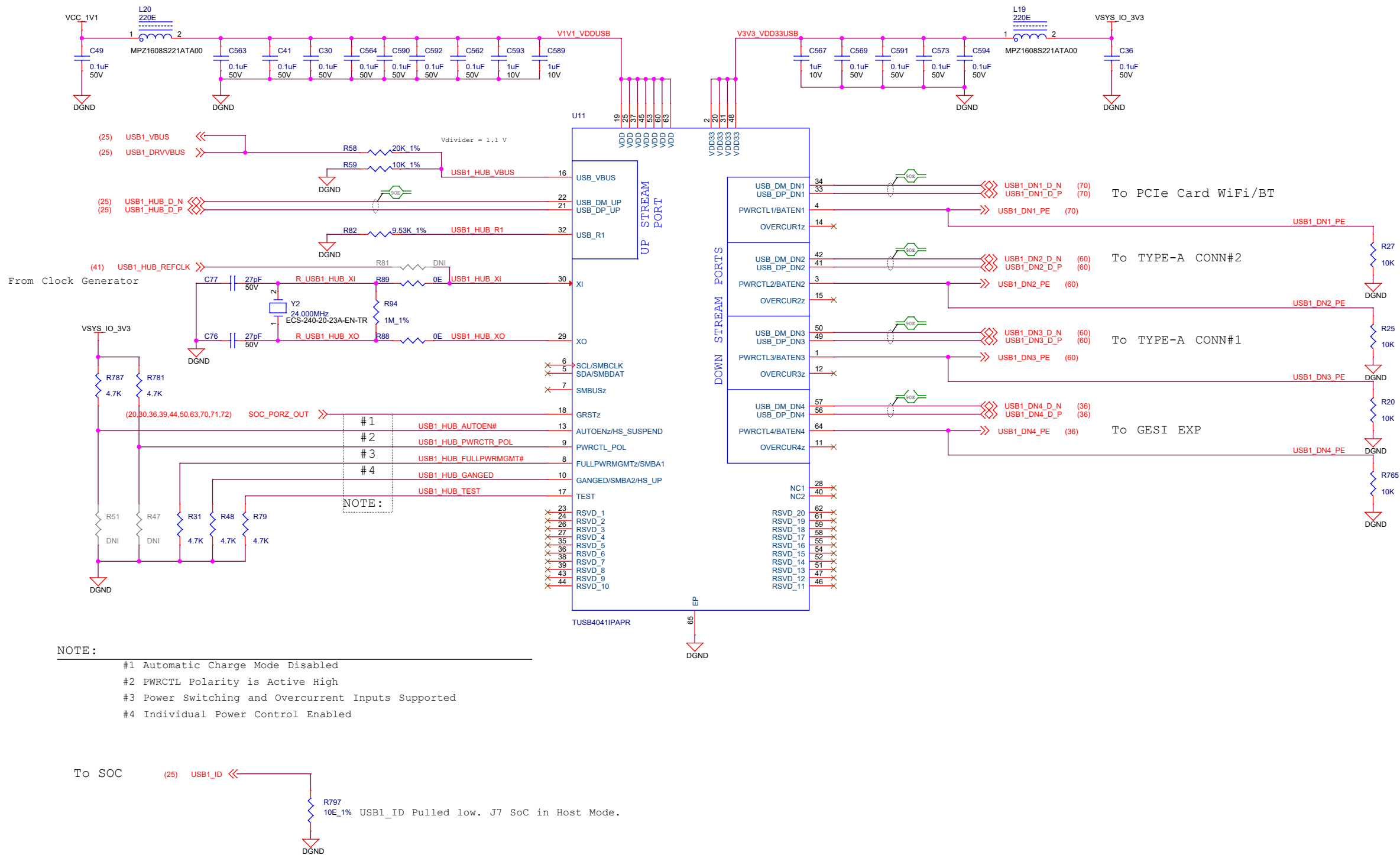
Size	PROC184 002
C	

Date: Thursday, August 22, 2024

Rev
E2

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USB HUB



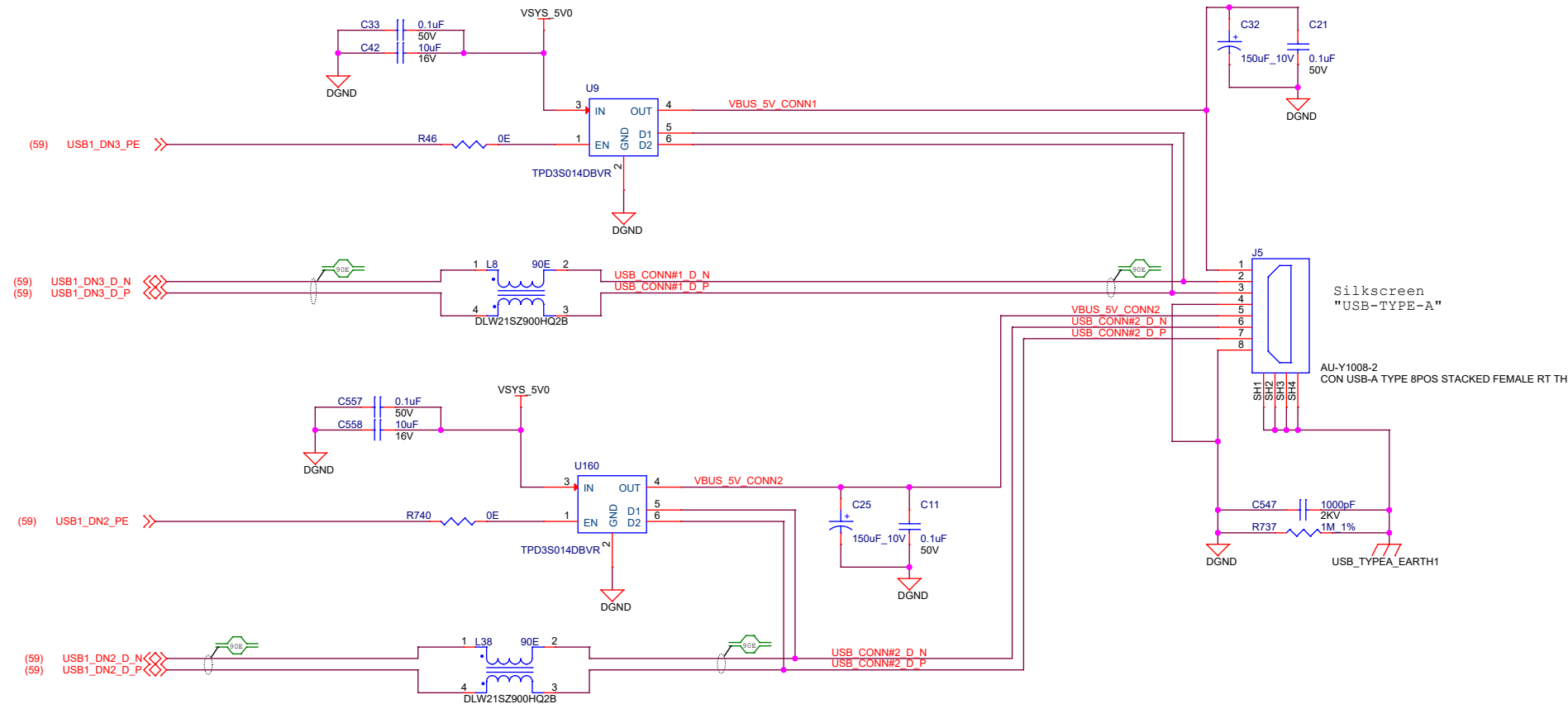
NOTE:

- #1 Automatic Charge Mode Disabled
- #2 PWRCTL Polarity is Active High
- #3 Power Switching and Overcurrent Inputs Supported
- #4 Individual Power Control Enabled

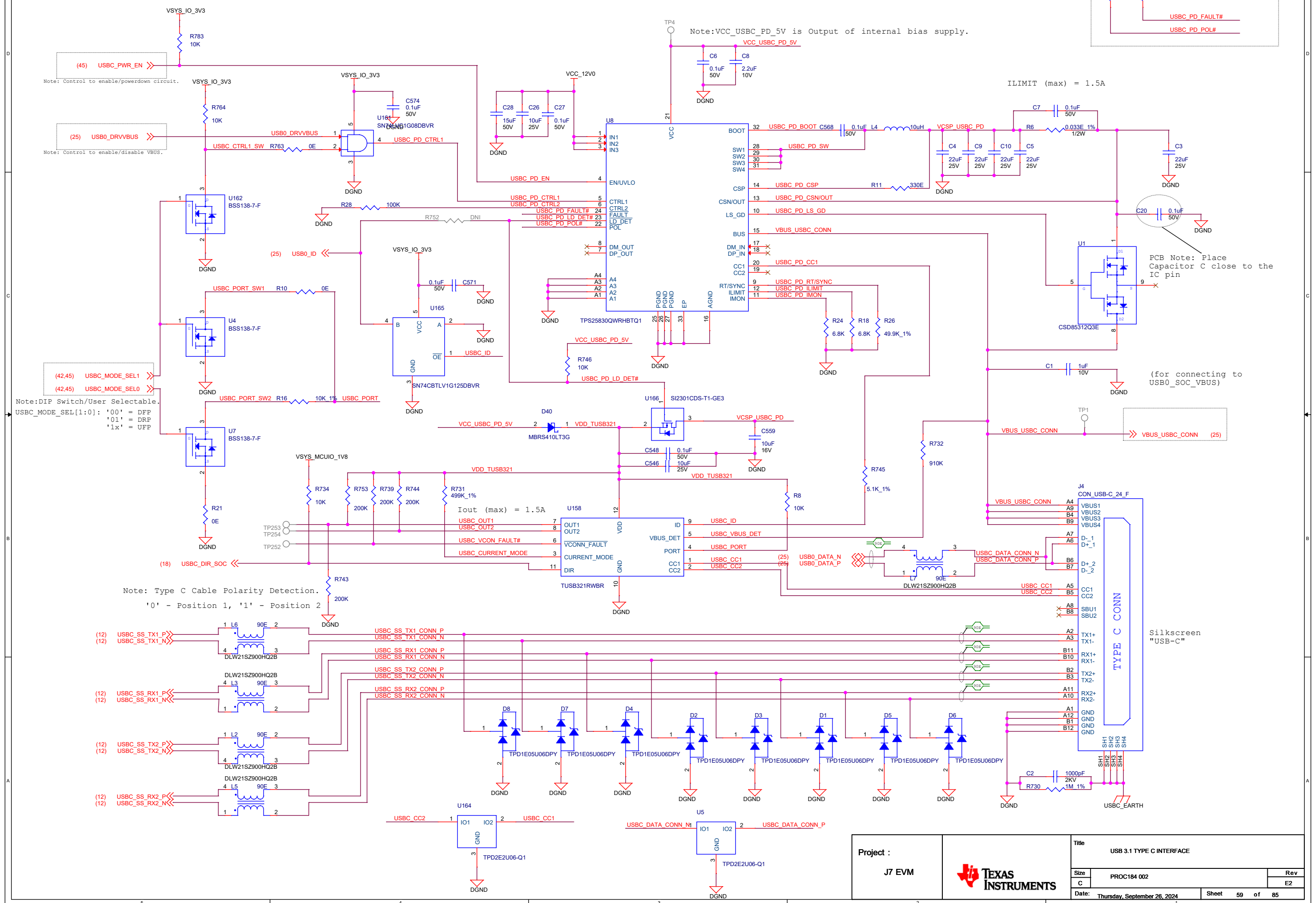
To SOC (25) USB1_ID

R797 10E_1% USB1_ID Pulled low. J7 SoC in Host Mode.

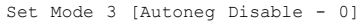
USB 2.0 TYPE-A CONNECTORS



USB 3.1 TYPE C INTERFACE

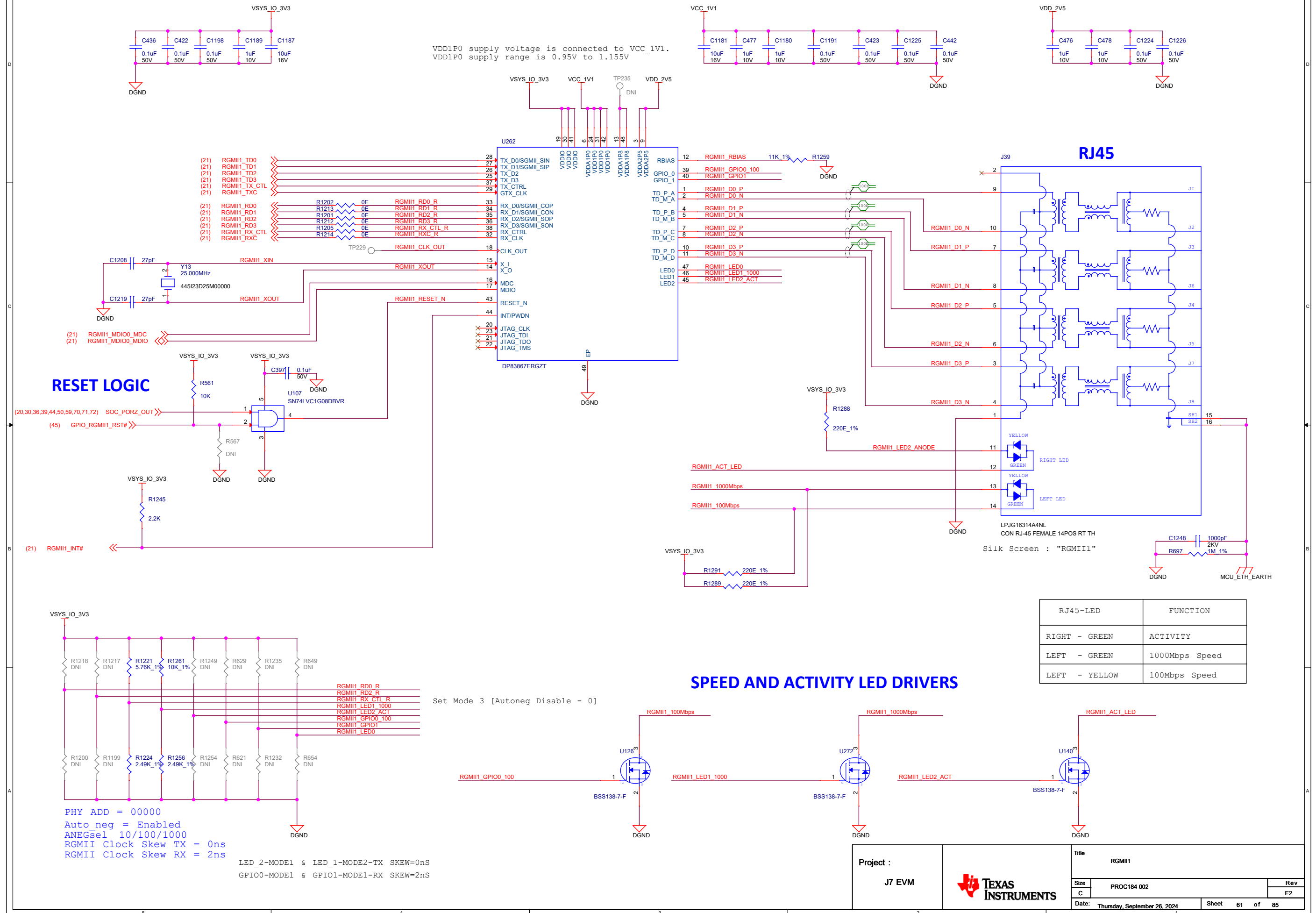


MCU GB ETHERNET

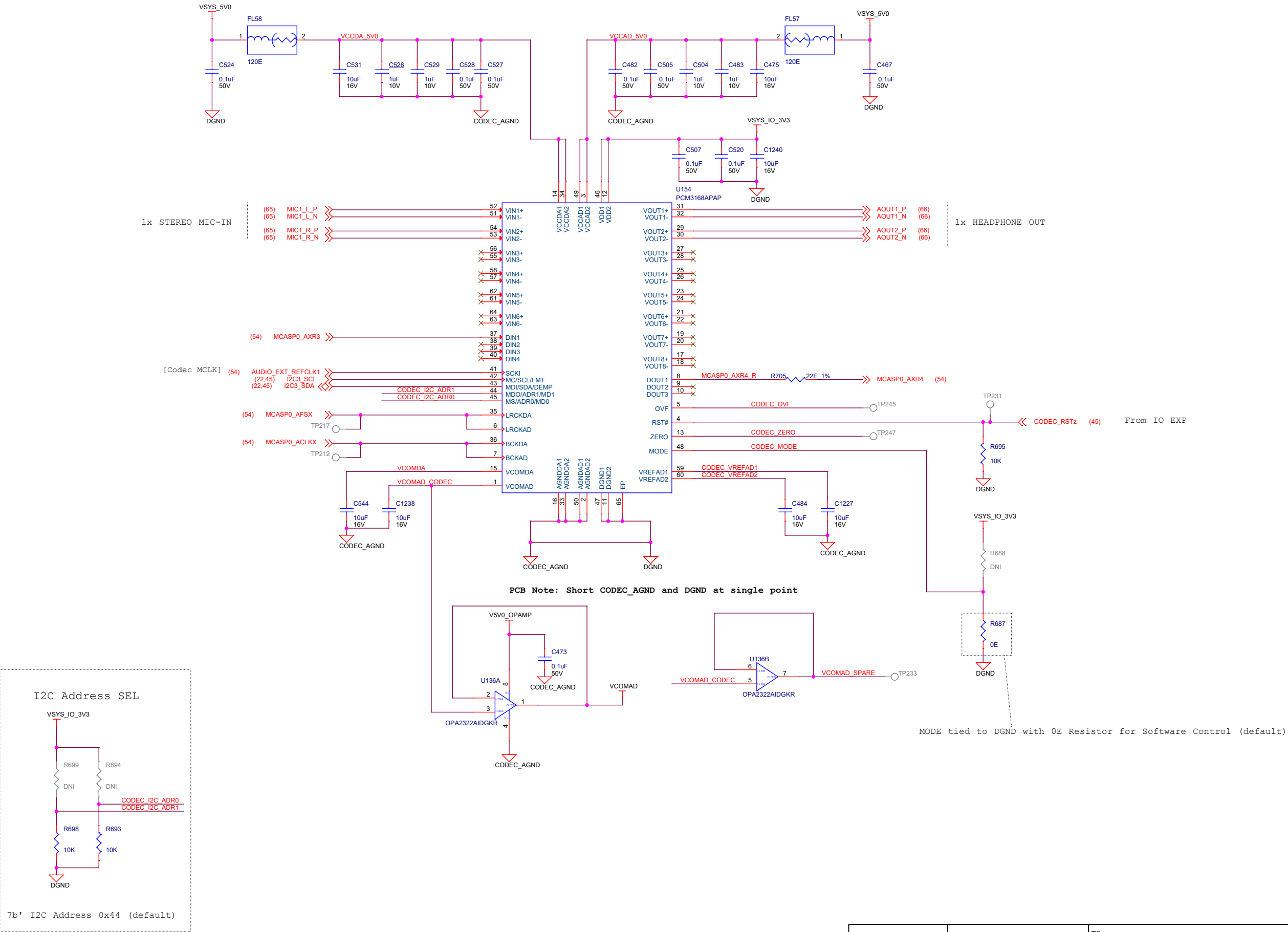


RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	100Mbps Speed
LEFT - YELLOW	100Mbps Speed

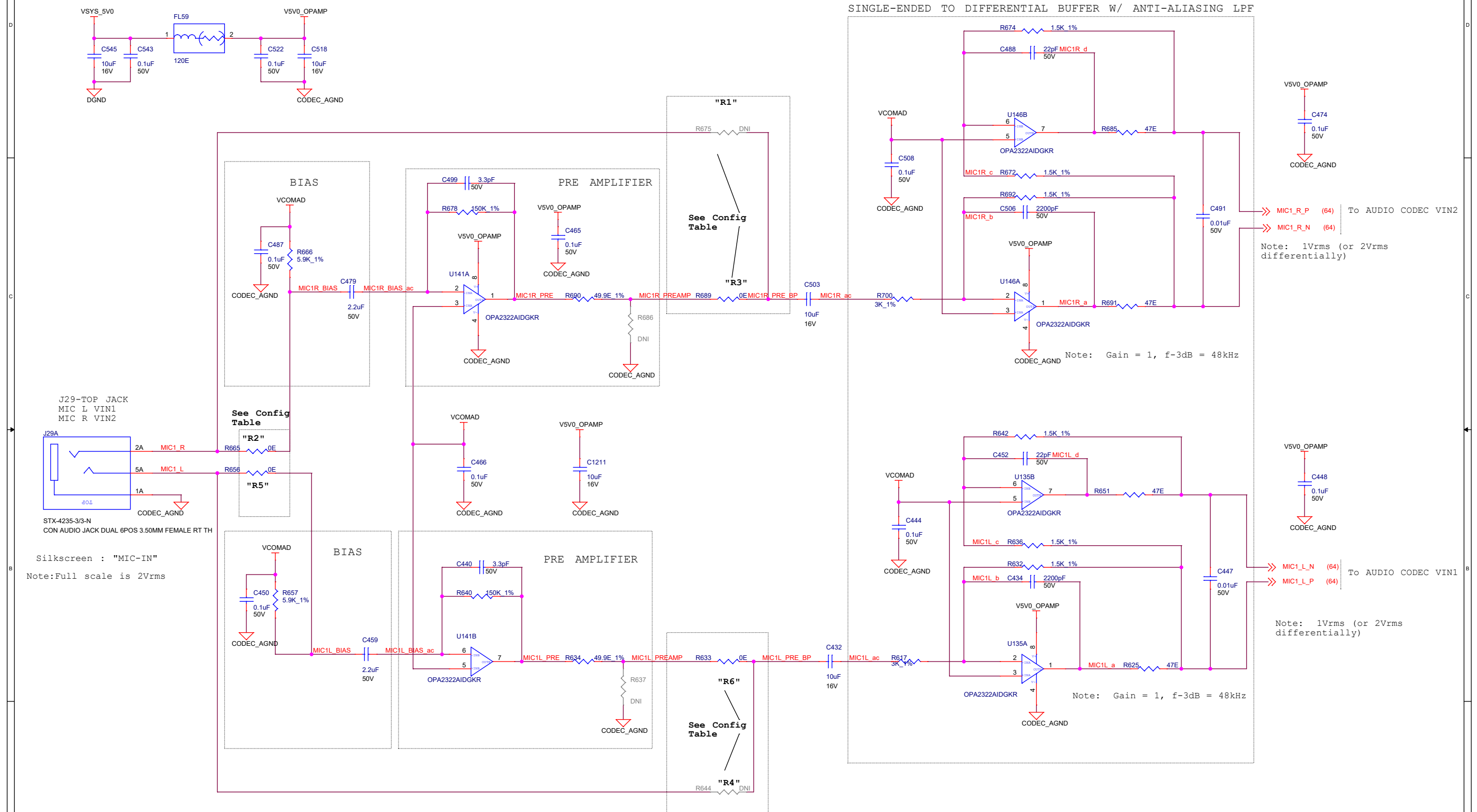
RGMII1



AUDIO I/F CODEC



AUDIO I/F - STEREO MIC #1



Config Table

		Install	Remove
PASSIVE-MIC (default)	BIAS + PREAMP	R2,R3,R5,R6	R1,R4
ACTIVE-MIC	BIAS ONLY	R1,R2,R4,R5	R3,R6
LINE-INPUT	NO BIAS/PREAMP	R1,R4	R2,R3,R5,R6

Project :

J7 EVM



Title	AUDIO I/F - STEREO MIC #1
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Size	PROC184 002
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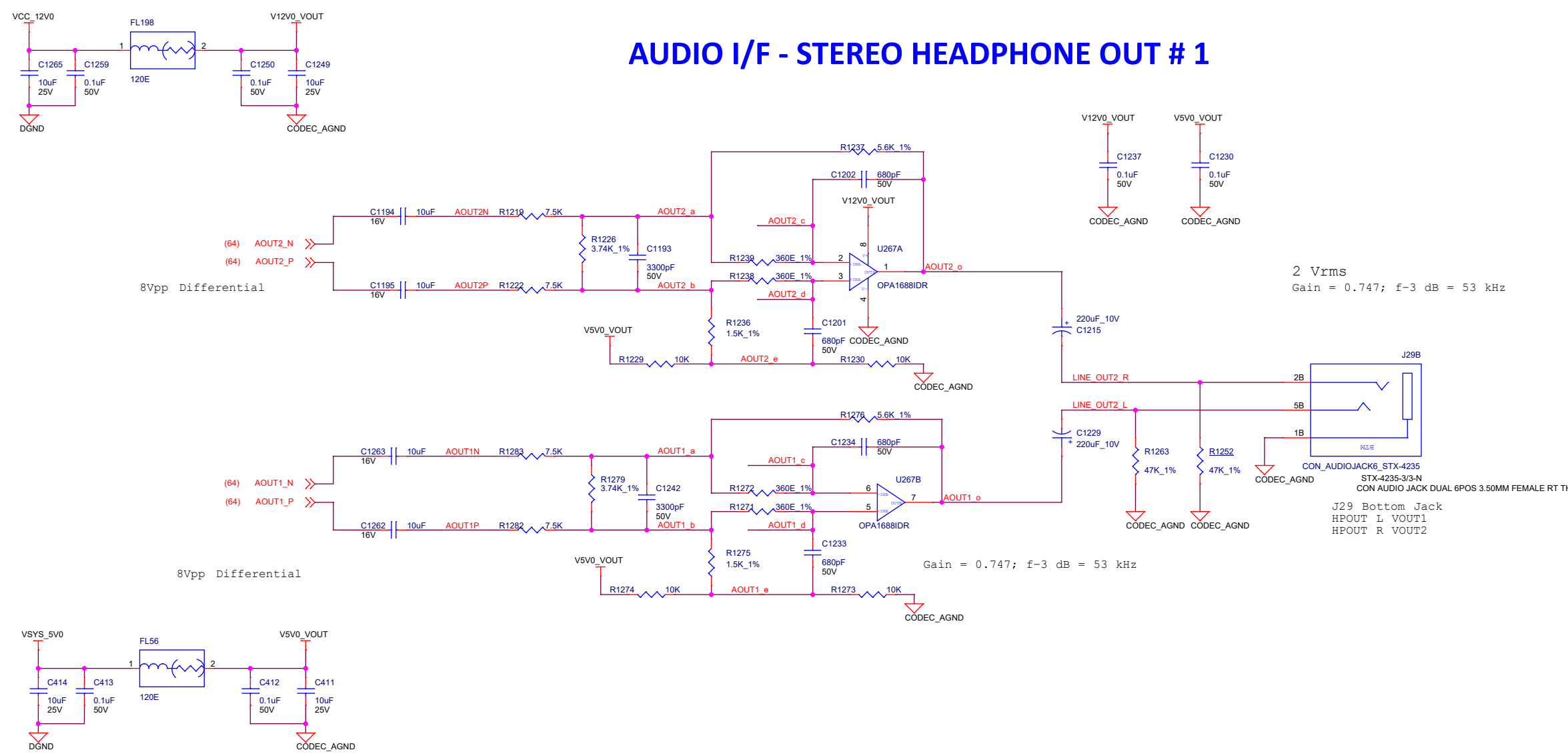
Date: Thursday, August 22, 2024

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Rev

E2

AUDIO I/F - STEREO HEADPHONE OUT # 1

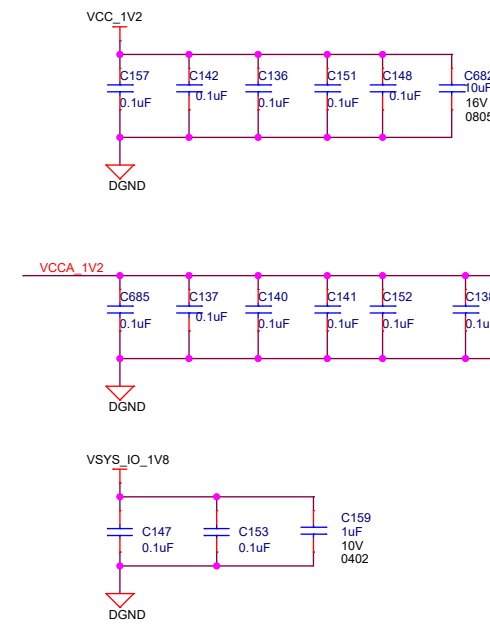
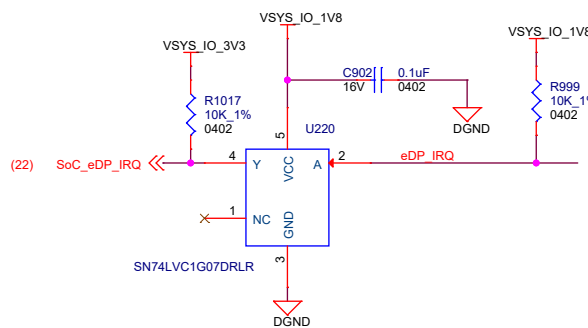
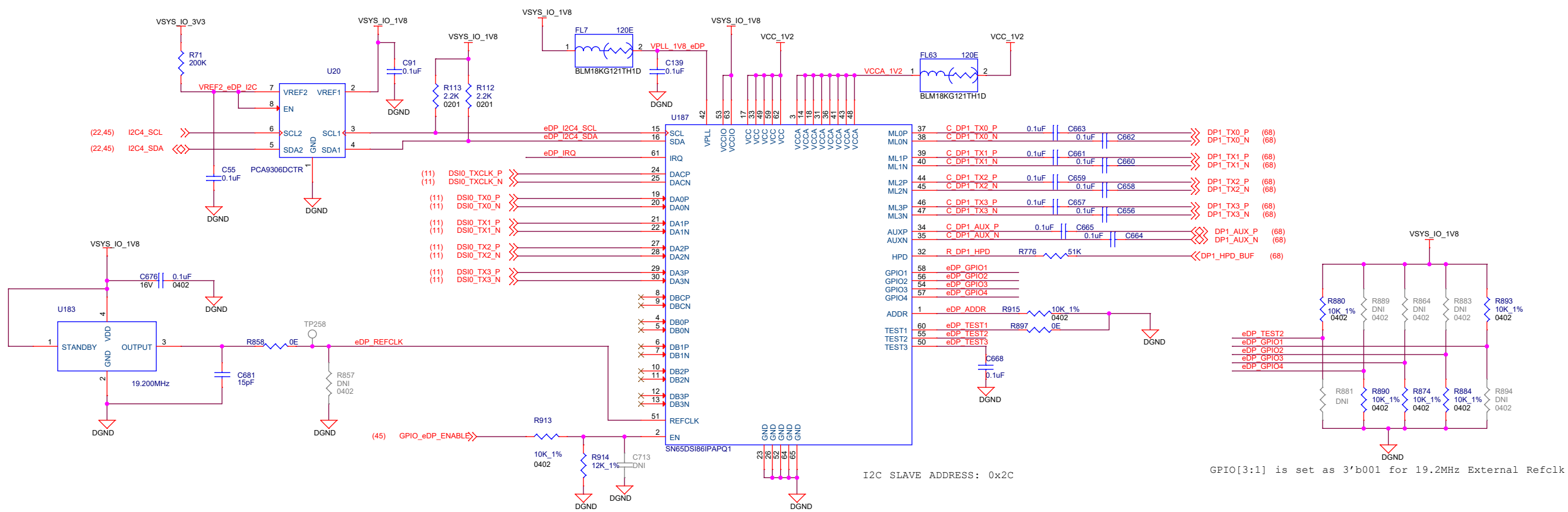


2 Vrms
Gain = 0.747; f-3 dB = 53 kHz

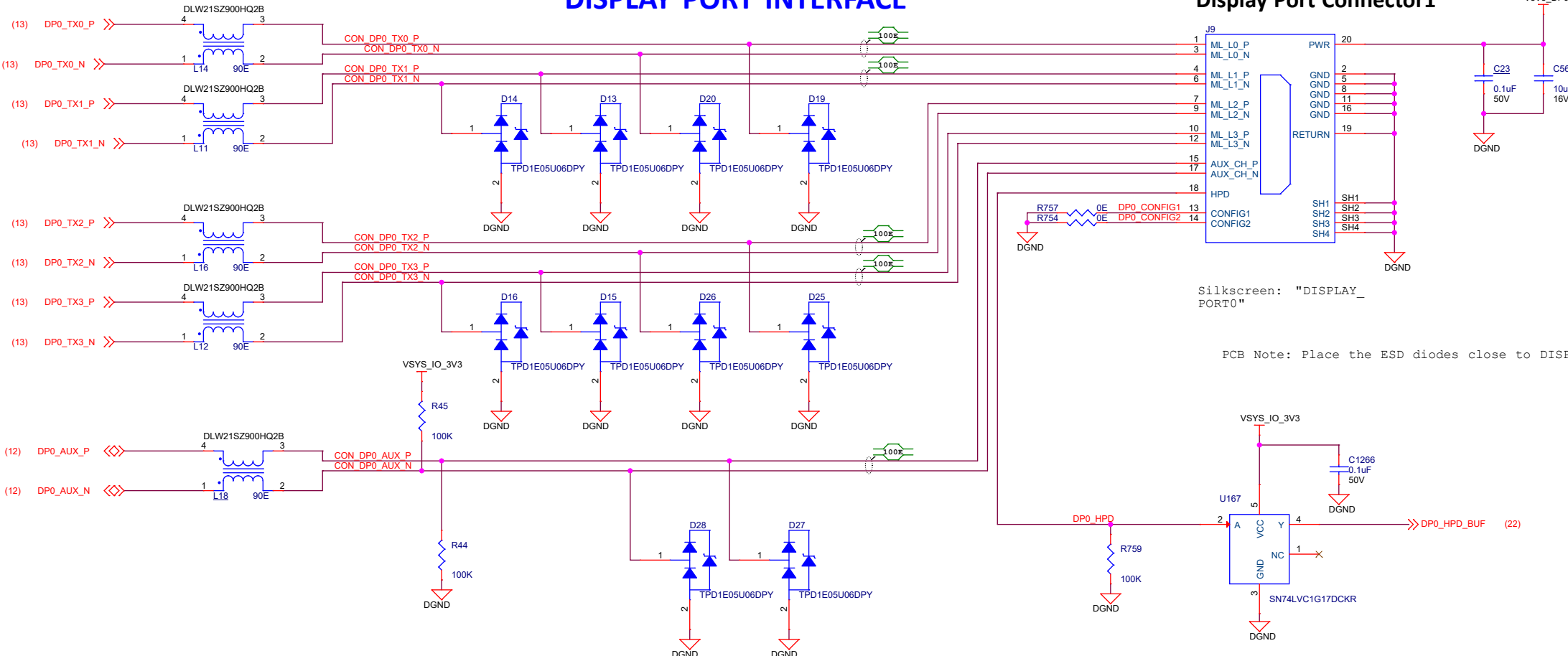
Gain = 0.747; f-3 dB = 53 kHz

J29 Bottom Jack
HPOUT L VOUT1
HPOUT R VOUT2

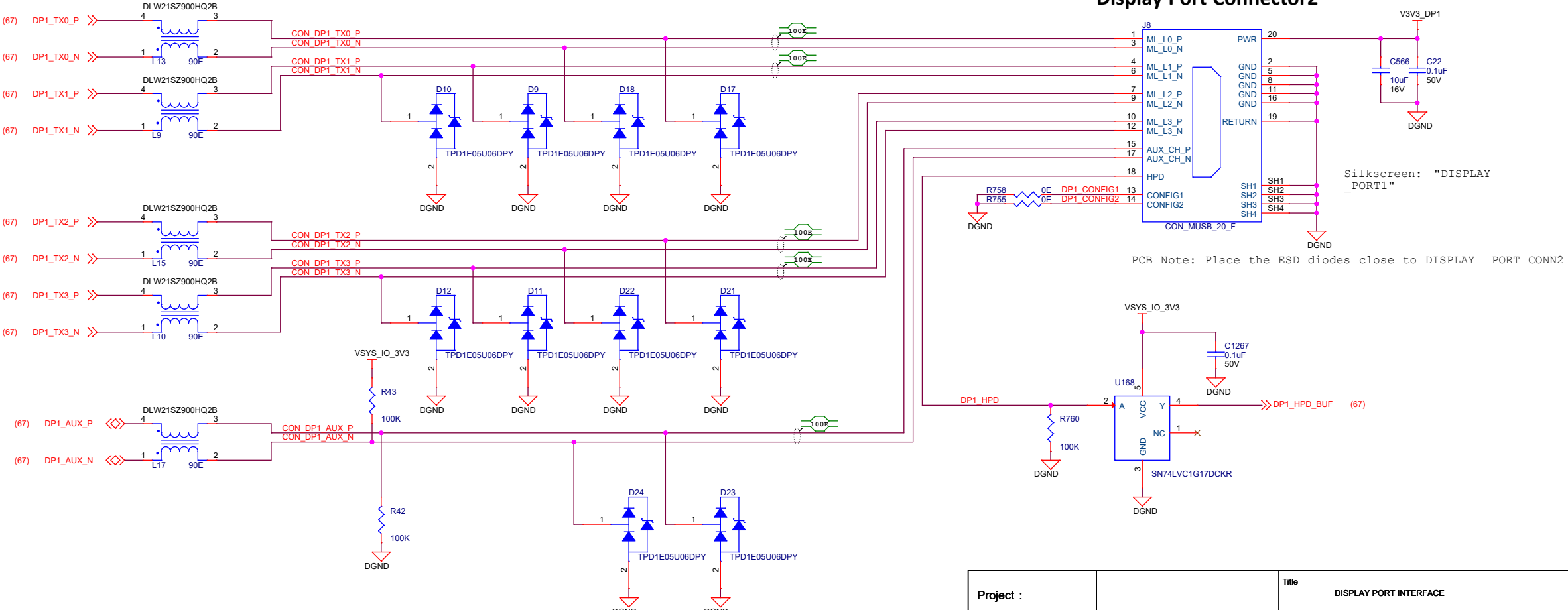
DSI to eDP Bridge



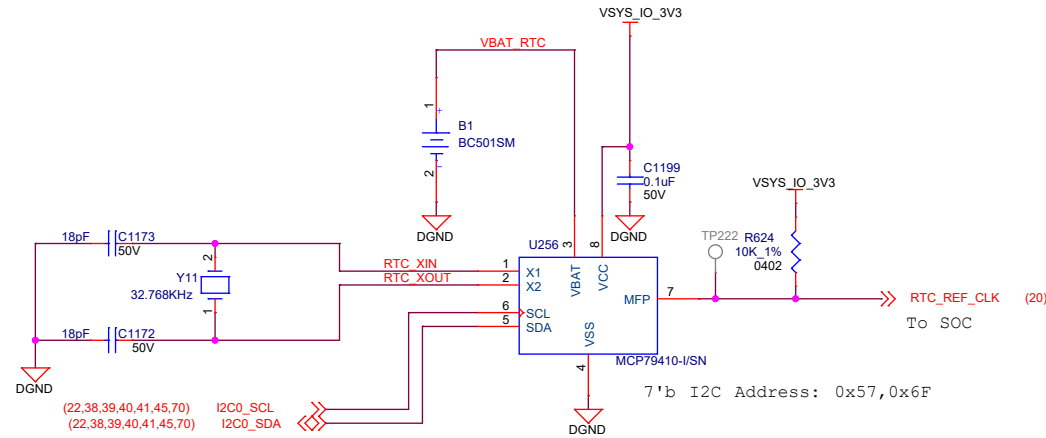
DISPLAY PORT INTERFACE



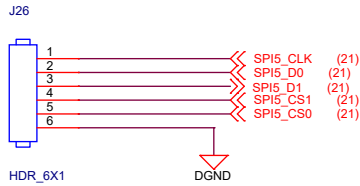
Display Port Connector



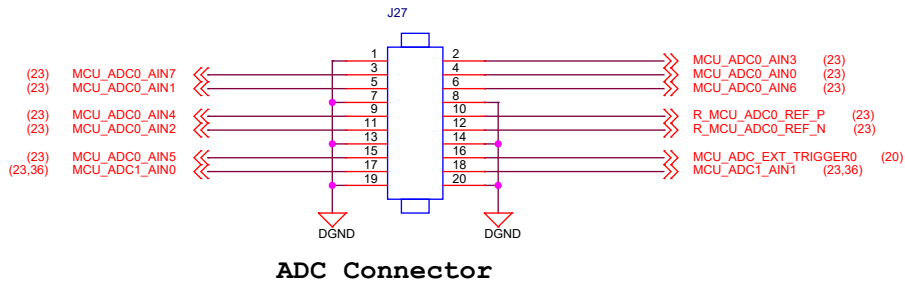
RTC



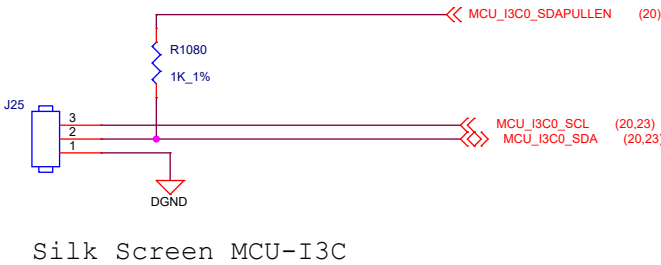
SPI Header



ADC INTERFACE



I3C Header



Silk Screen MCU-I3C

x4 Lane PCIe Connector

```
(default
```



I2C MUX

Place R1,R2 close to SOC

```
to SOC (13) SOC_SERDES1_REFCLK_P <=
(13) SOC_SERDES1_REFCLK_N <=
```

"Added to avoid stub"
Place R3,R4 close to SOC

Place C1, C2 close to PCIe connector

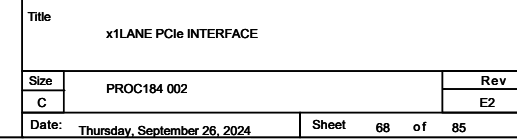
Place R5,R6 close to PCIe connector

to PCIe Con (x4 Lane

CON_PCIE0_4L_REFCLK_M

Project :

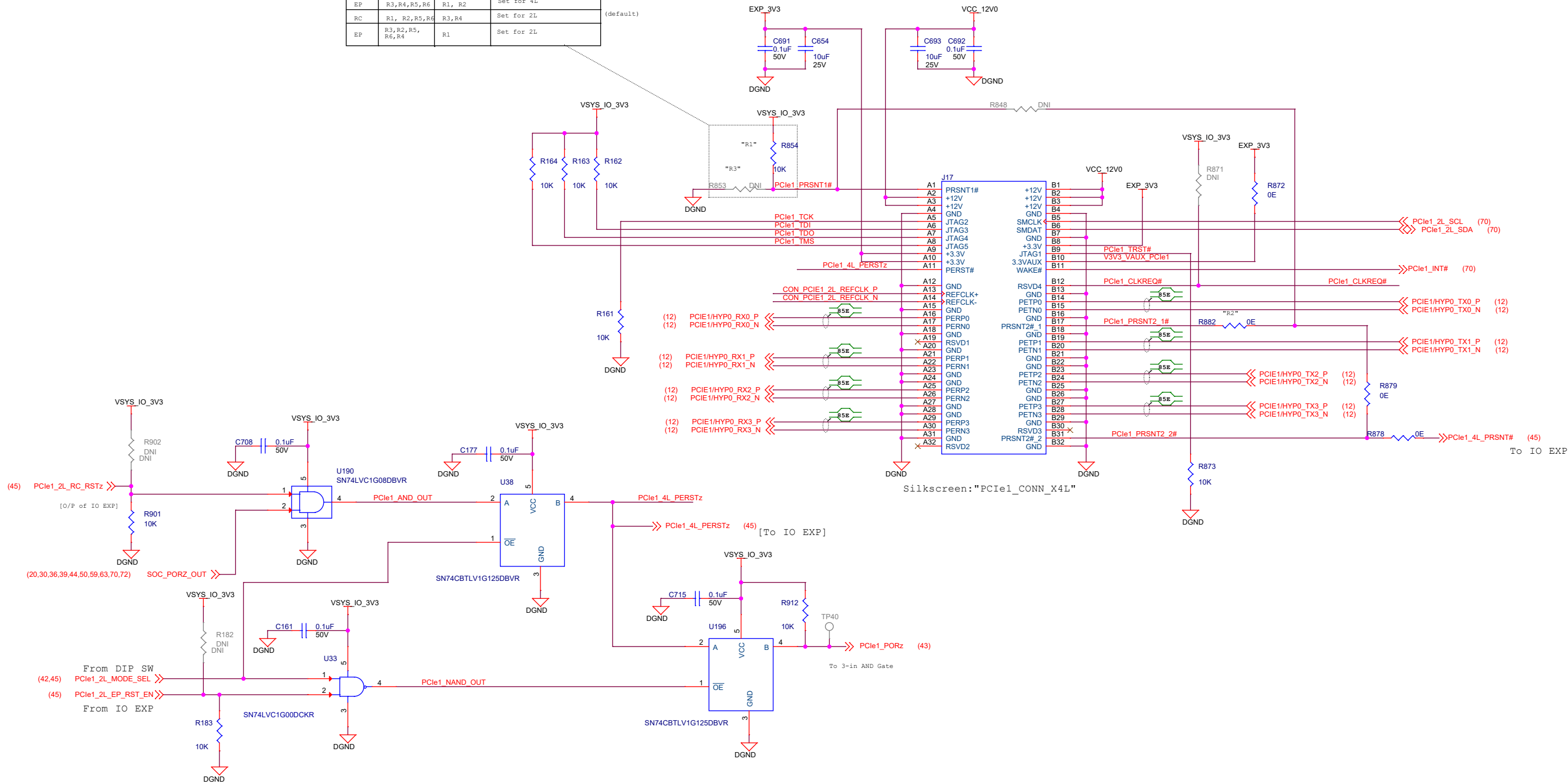
J7 EVM



x2LANE PCIe1 Interface(J17)
x4 Lane PCIe Connector

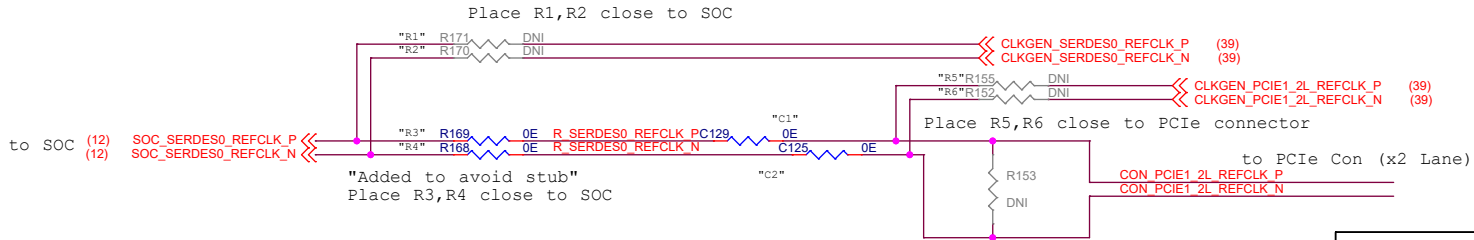
MODE	INSTALL	DNI	PCIe Lanes
RC	R1, R6	R3,R4,R2,R5	Set for 4L
EP	R3,R4,R5,R6	R1, R2	Set for 4L
RC	R1, R2,R5,R6	R3,R4	Set for 2L
EP	R3,R2,R5, R6,R4	R1	Set for 2L

(default)

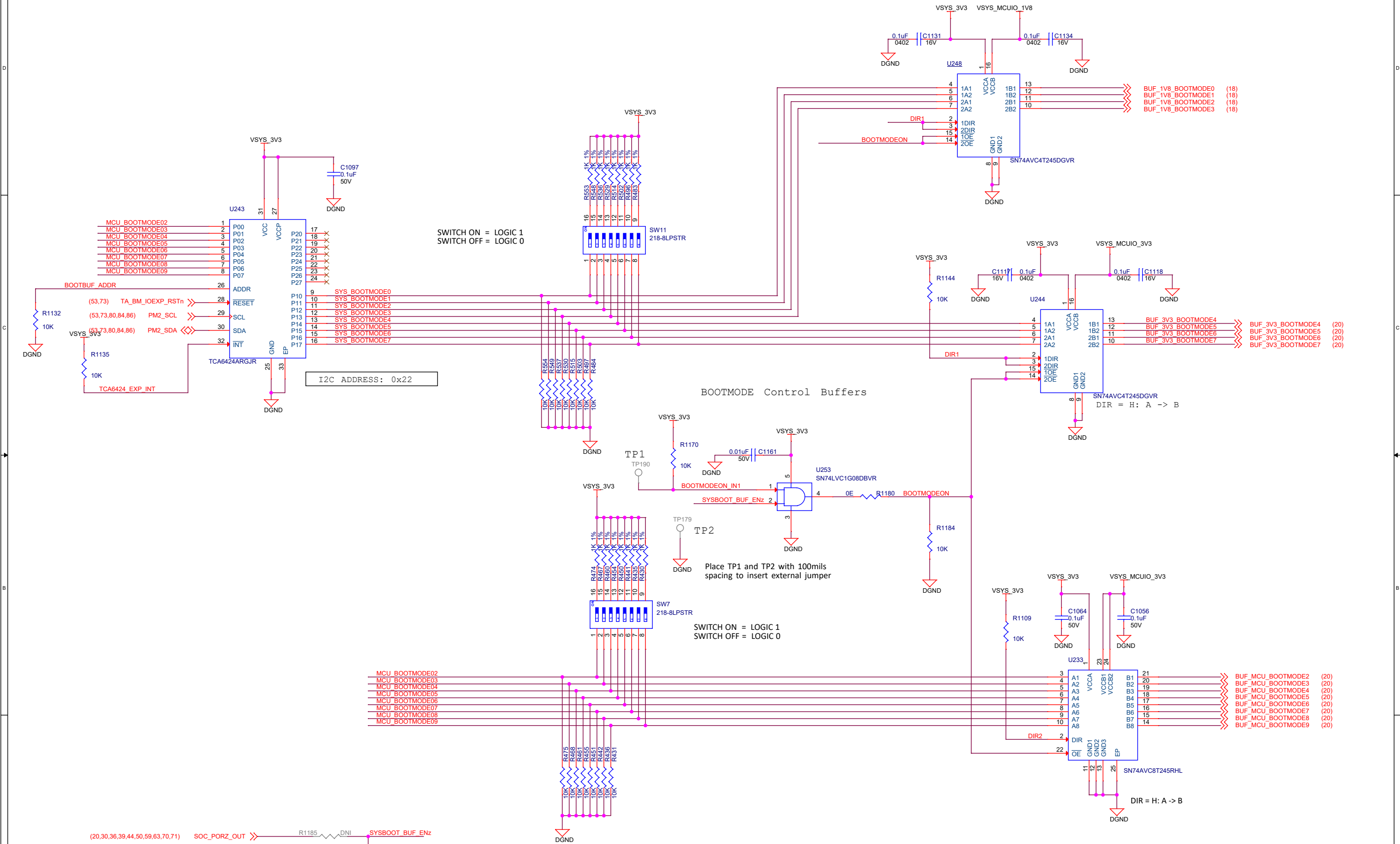


CLOCK ROOT SELECTION

	Install	Remove
PCIe root complex	R1,R2,R5,R6	R3,R4,C1,C2
PCIe end point	R3,R4,C1,C2	R1,R2,R5,R6



BOOT MODE BUFFER & SWITCHES



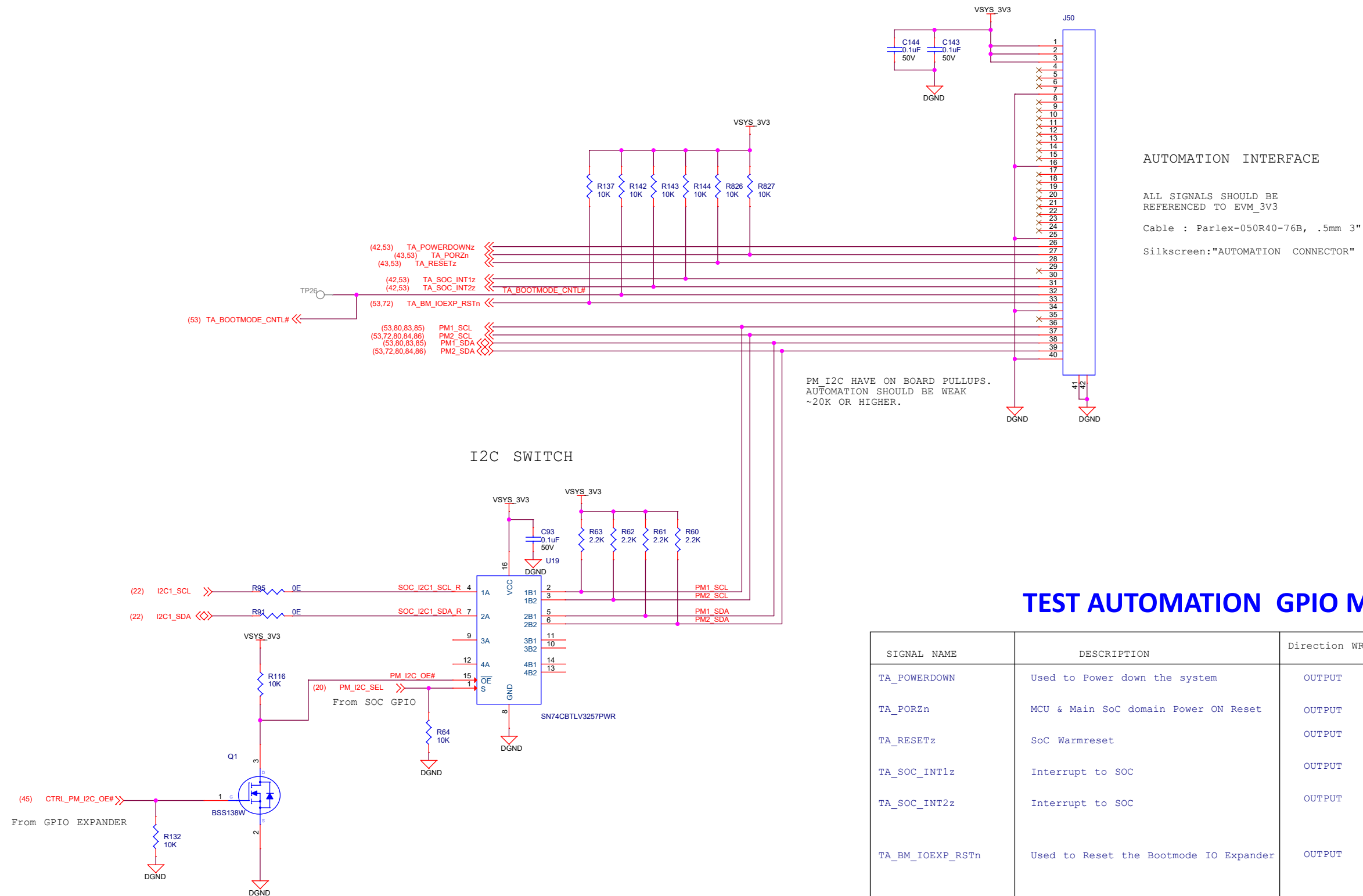
TA_BM_IOEXP_RSTn	SOC_PORZ_OUT	BOOTMODE Control from Test Automation HDR
HIGH	LOW	Enabled
HIGH	HIGH	Disabled

Project :
J7 EVM

TEXAS
INSTRUMENTS

Title BOOT MODE BUFFER & SWITCHES	
Size C	PROC184 002
Date: Thursday, September 26, 2024	Sheet 70 of 85
Rev E2	

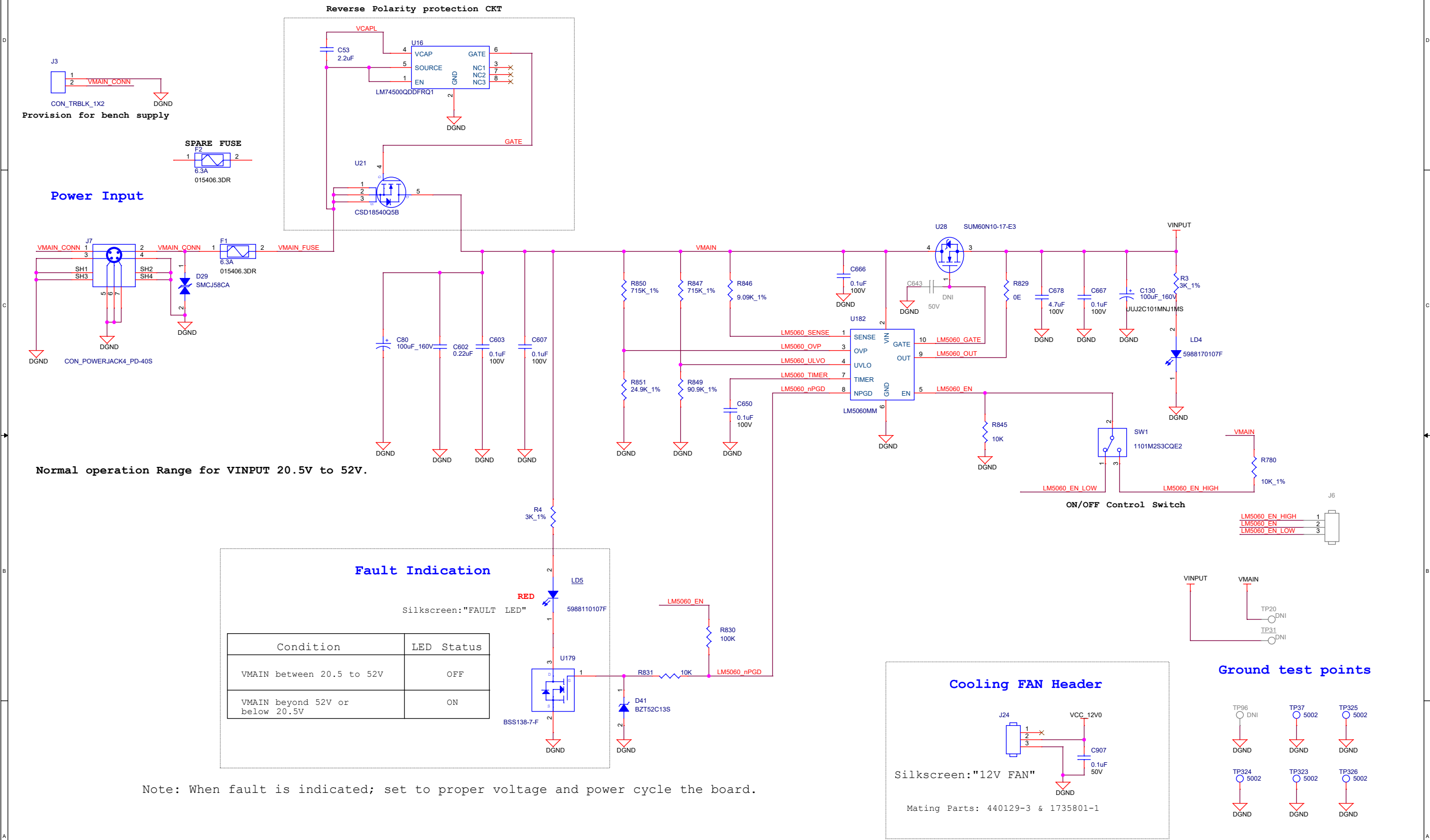
TEST AUTOMATION HEADER



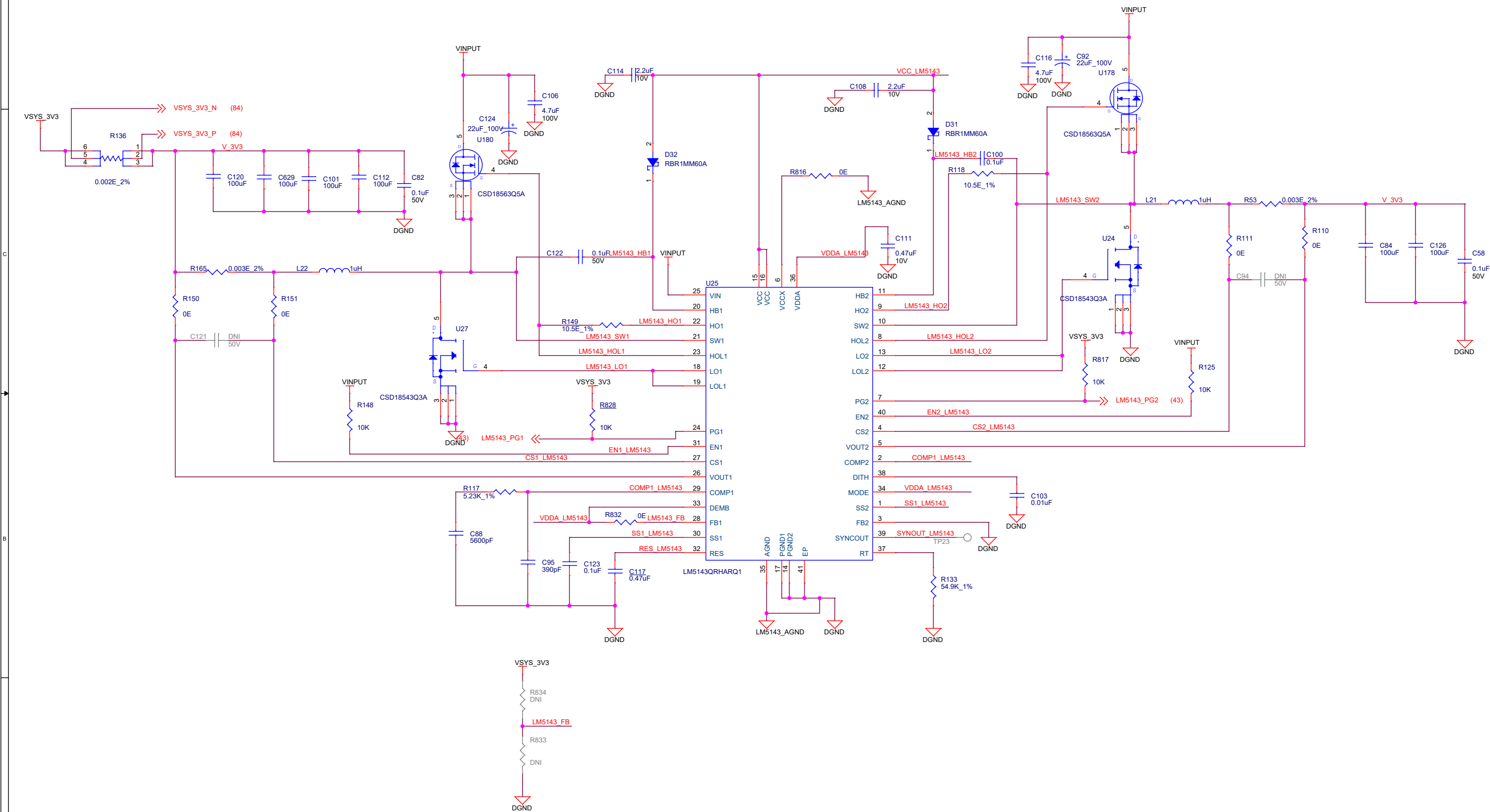
TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESEtZ	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

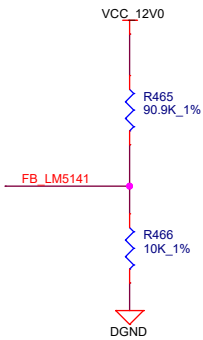
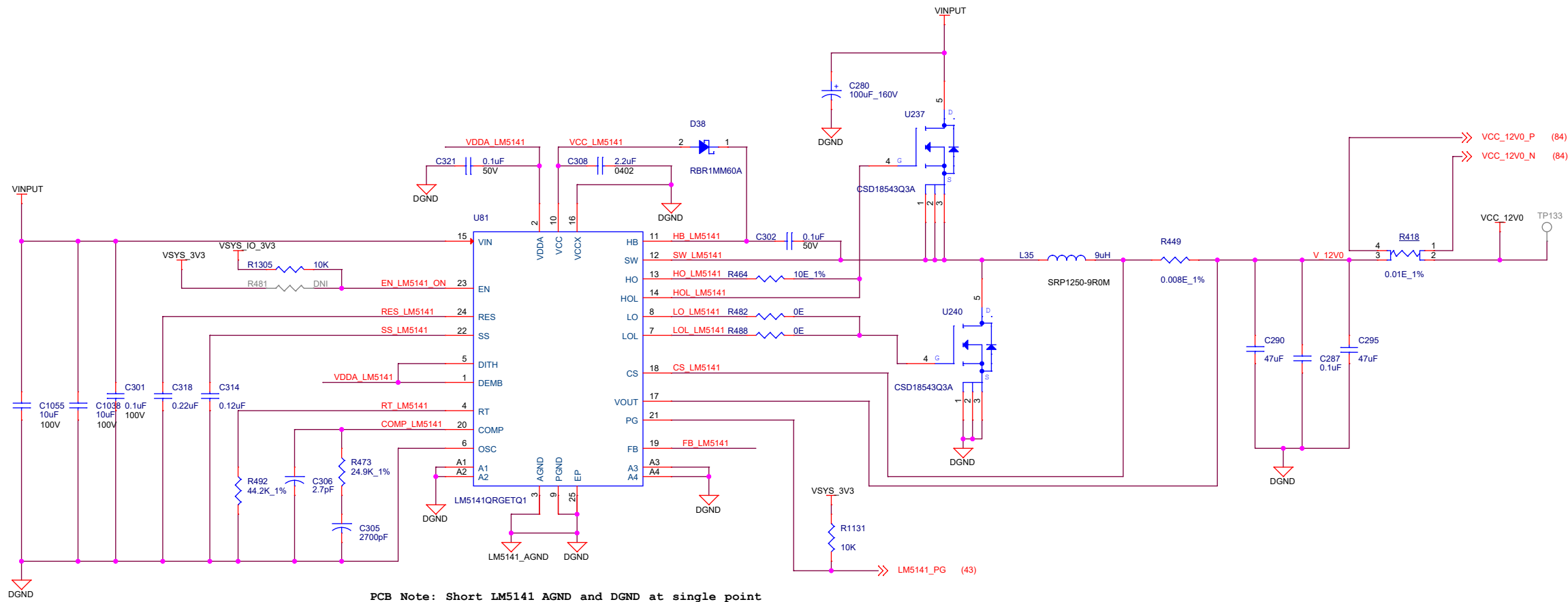
OVER VOLTAGE PROTECTION CIRCUIT



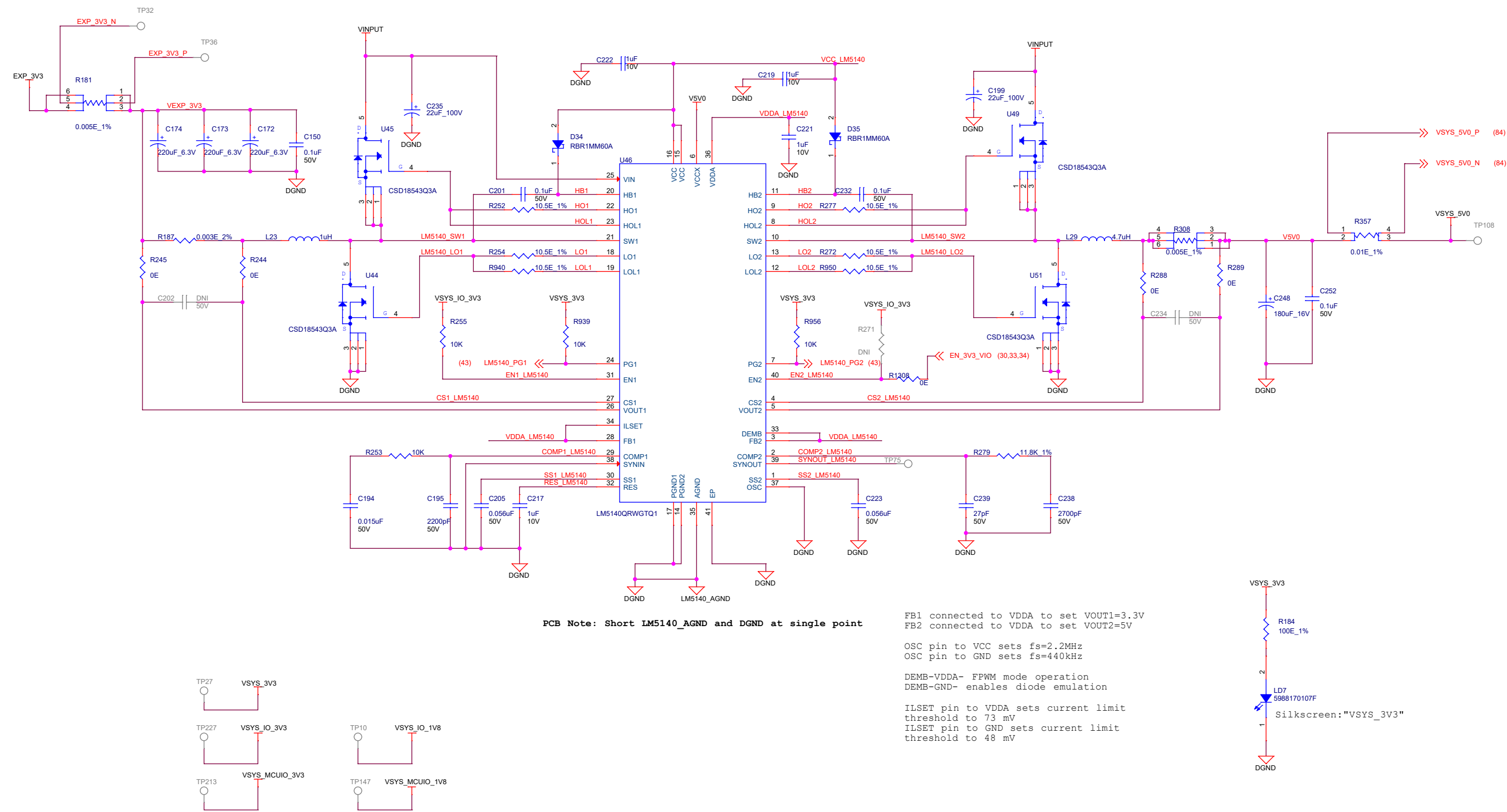
POWER SUPPLY #1



POWER SUPPLY #2



POWER SUPPLY #3
3.3V AND 5V GENERATION



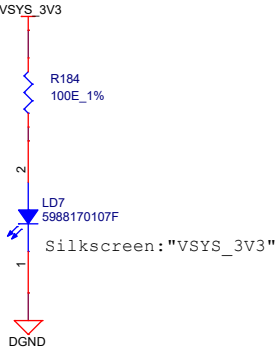
PCB Note: Short LM5140_AGND and DGND at single point

FB1 connected to VDDA to set VOUT1=3.3V
FB2 connected to VDDA to set VOUT2=5V

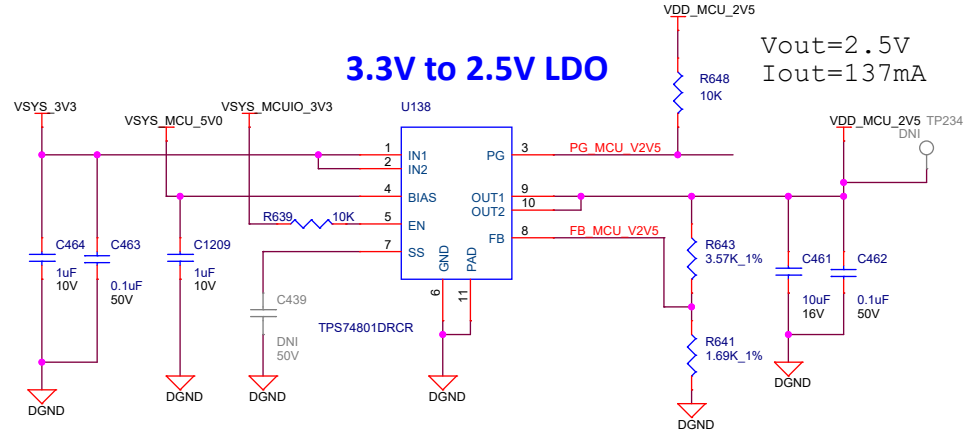
OSC pin to VCC sets fs=2.2MHz
OSC pin to GND sets fs=440kHz

DEMB-VDDA- FPWM mode operation
DEMB-GND- enables diode emulation

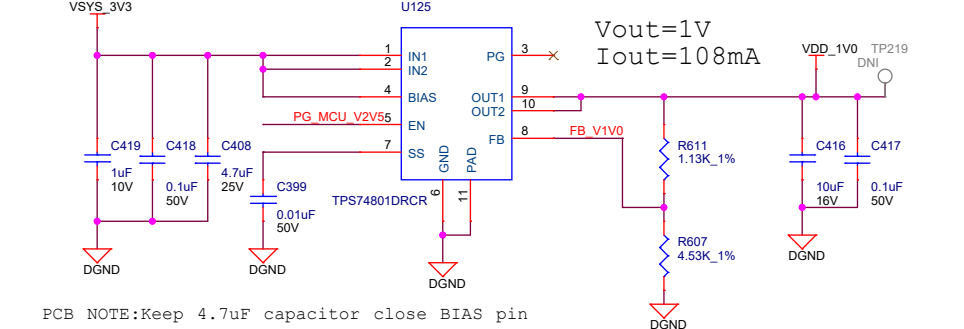
ILSET pin to VDDA sets current limit threshold to 73 mV
ILSET pin to GND sets current limit threshold to 48 mV



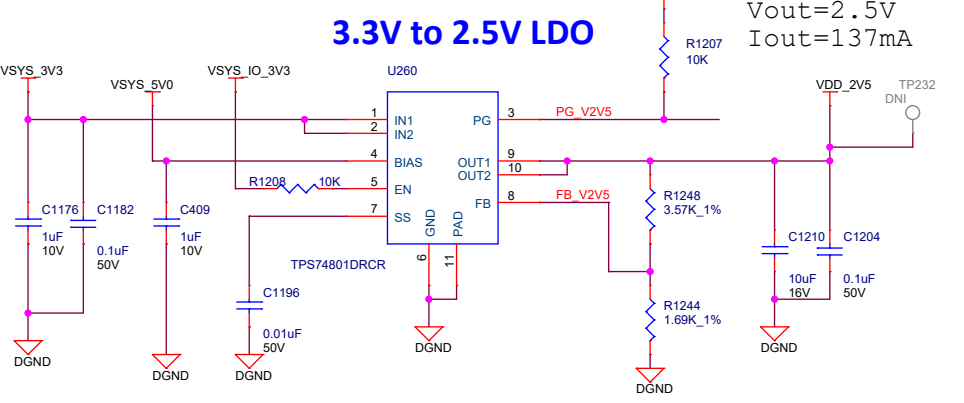
ETHERNET POWER- MCU RGMII



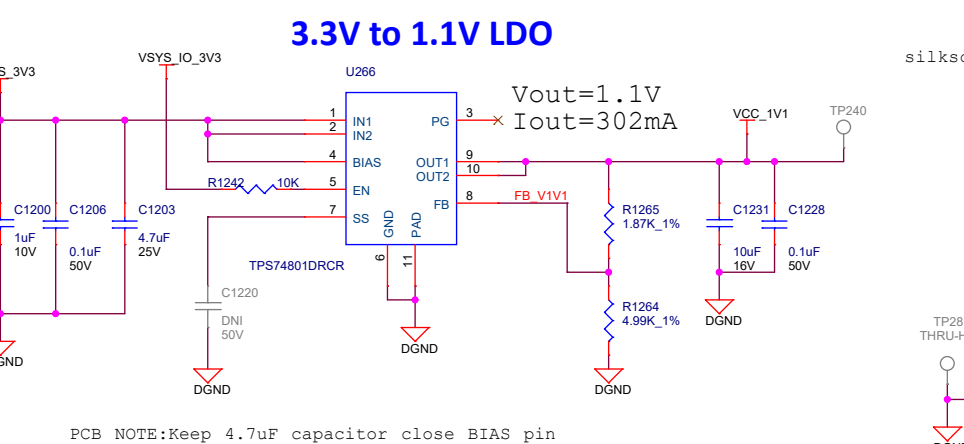
3.3V to 1.0V LDO



ETHERNET POWER- RGMII1

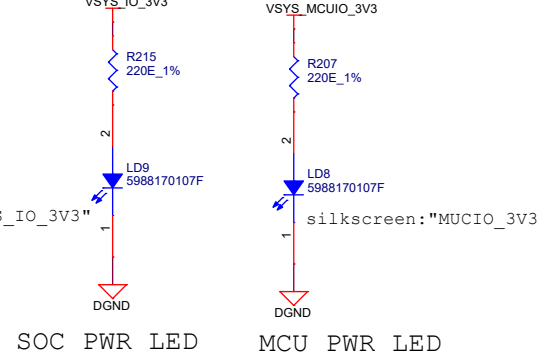


USB HUB POWER & ETHERNET POWER - RGMII1

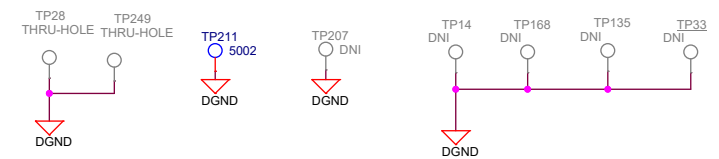


POWER SUPPLY #4

POWER INDICATION LED's

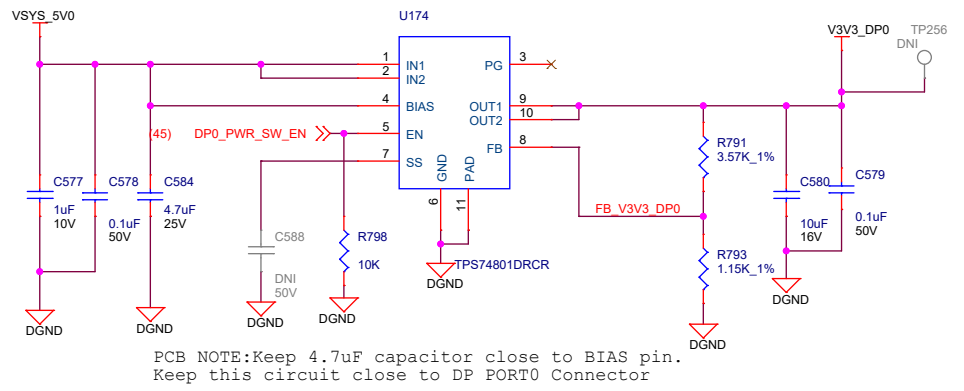


GROUND TEST POINTS

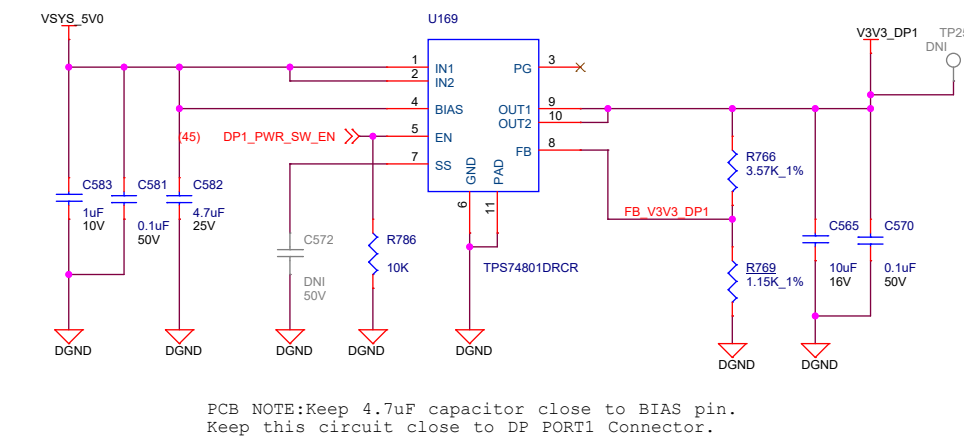


Display Port0

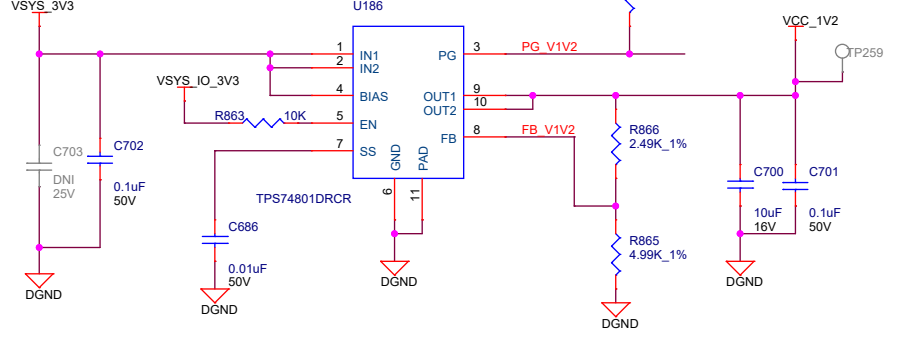
5V to 3.3V LDO



Display Port1
5V to 3.3V LDO

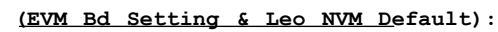


3.3V to 1.2V LDO

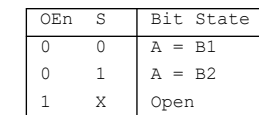


Project : J7 EVM		Title POWER SUPPLY #4	
		Size C	Rev E2
		Date: Thursday, August 22, 2024	
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EVM development & evaluation Test circuitry
(TI EVM Only)

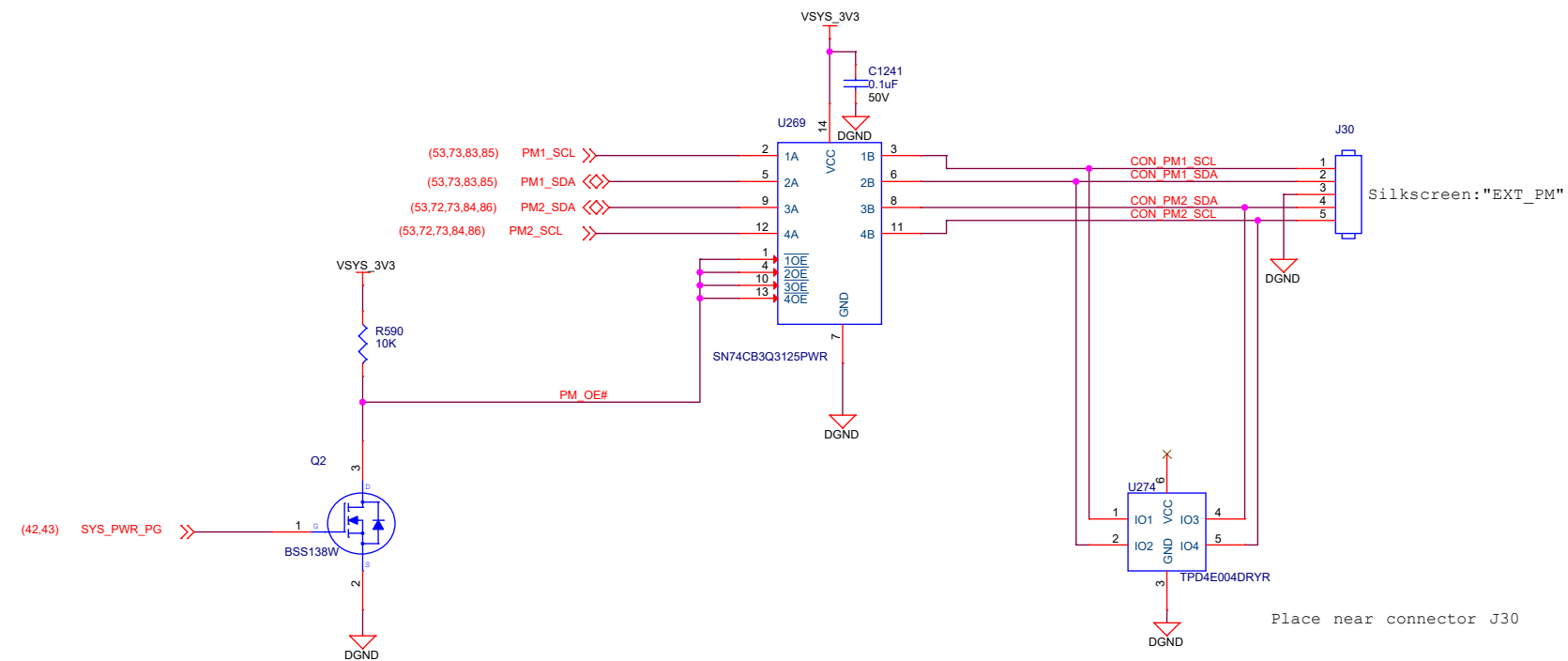


OEn	S	Bit State
0	0	A = B1
0	1	A = B2
1	X	Open



EVM POWER MEASUREMENT I2C BUS ISOLATION

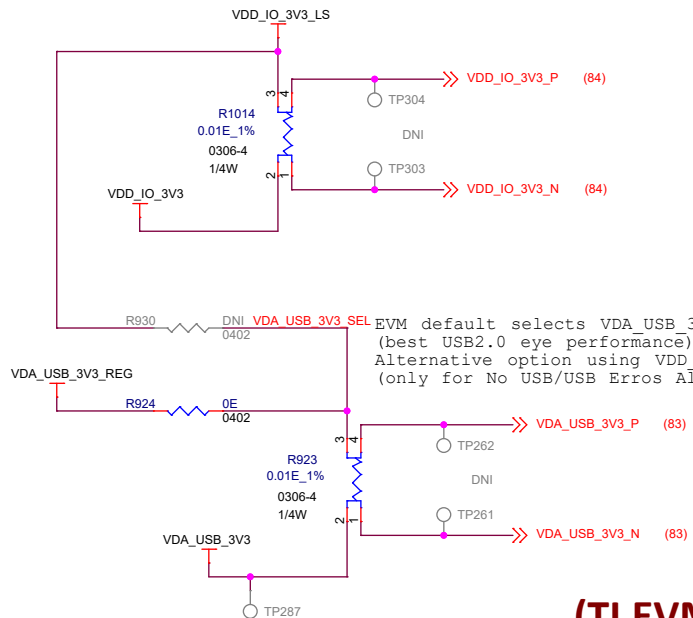
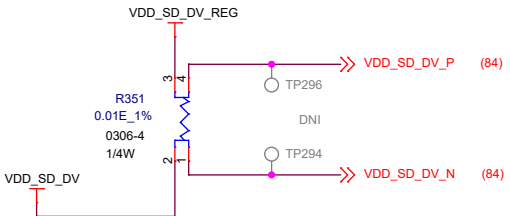
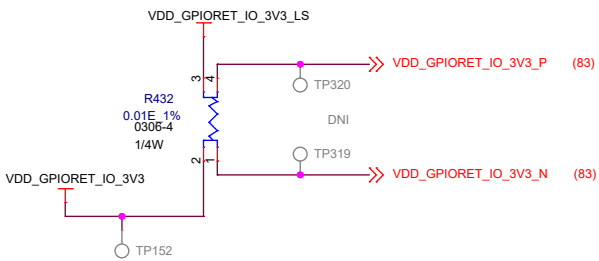
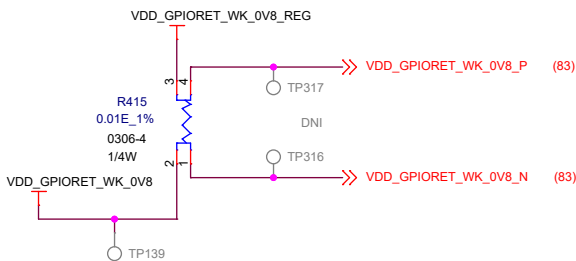
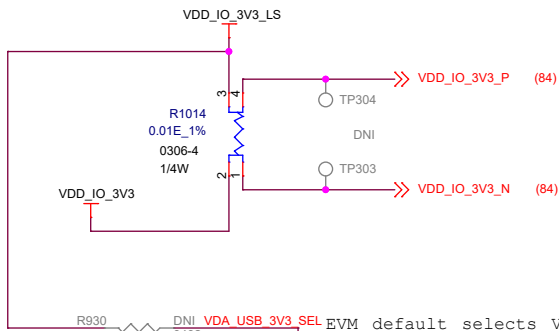
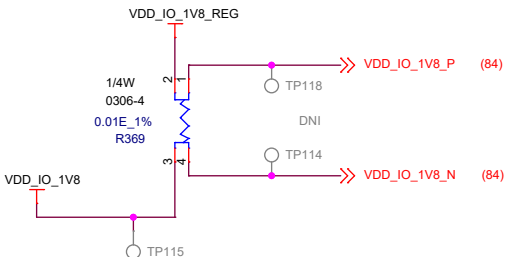
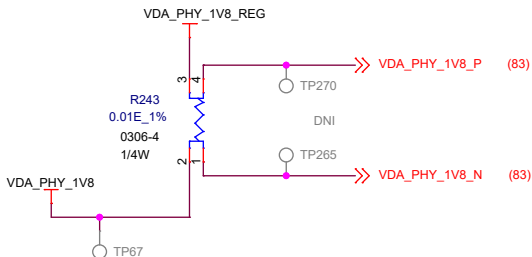
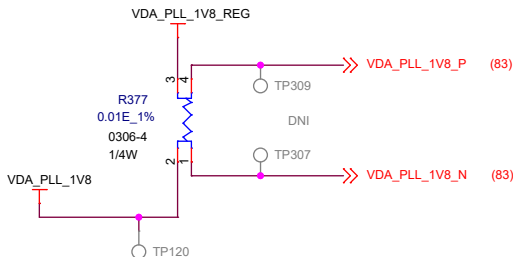
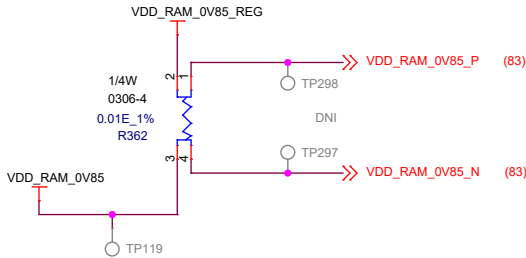
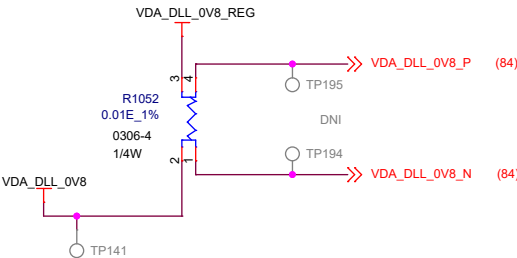
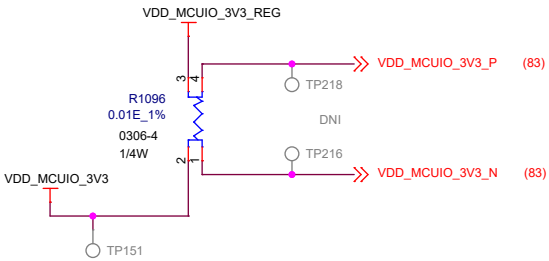
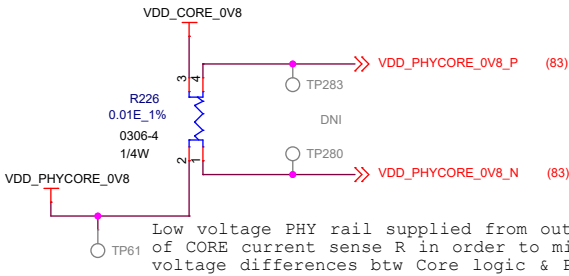
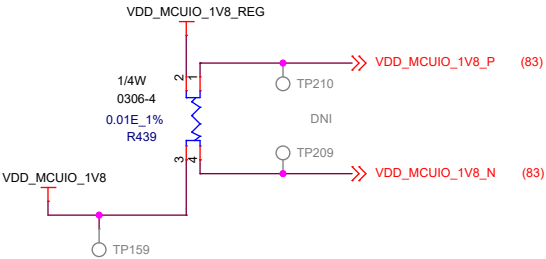
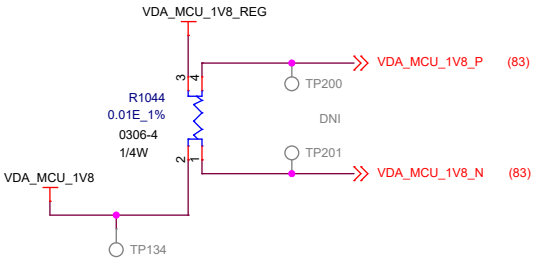
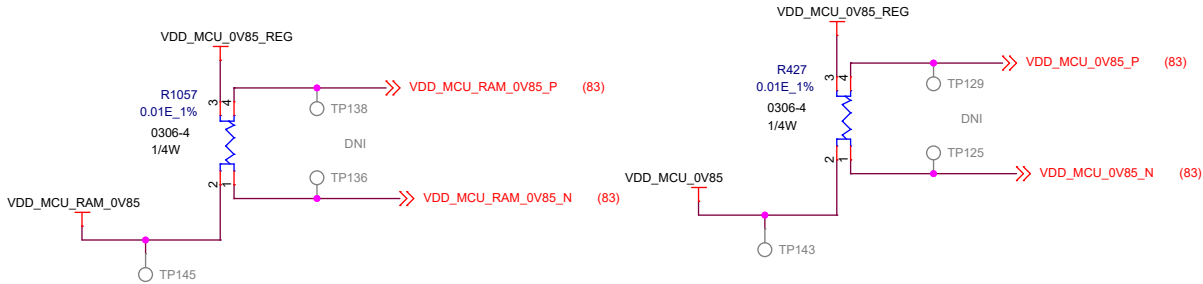
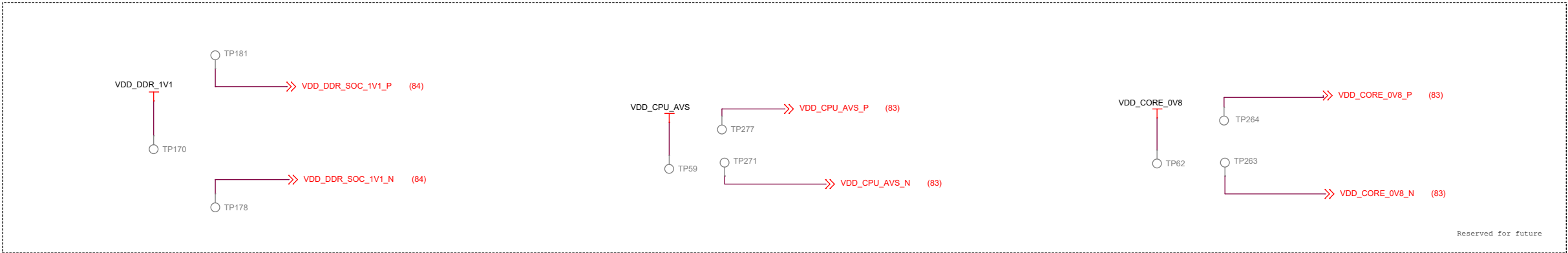
EVM development & evaluation Test circuitry
(TI EVM Only)



(TI EVM Only)

SOC Current Sense Resistors

(TI EVM Only)



(TI EVM Only)

(TI EVM Only)

Project :

J7 EVM



Title
SOC Current Sense Resistors

Size
C
PROC184 002

Rev

E2

Date: Thursday, August 22, 2024

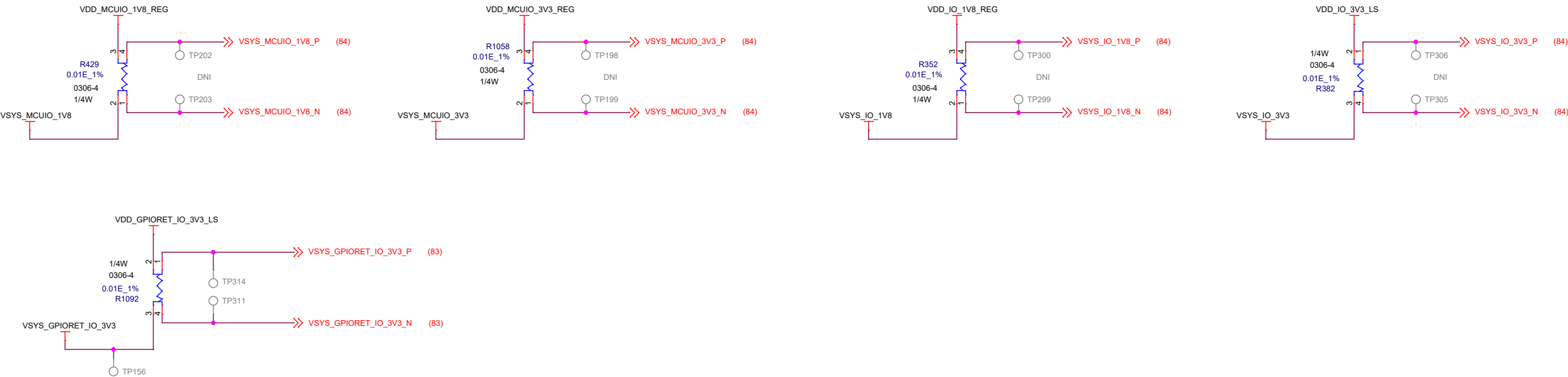
Sheet 79 of 85

EVM development & evaluation test circuitry

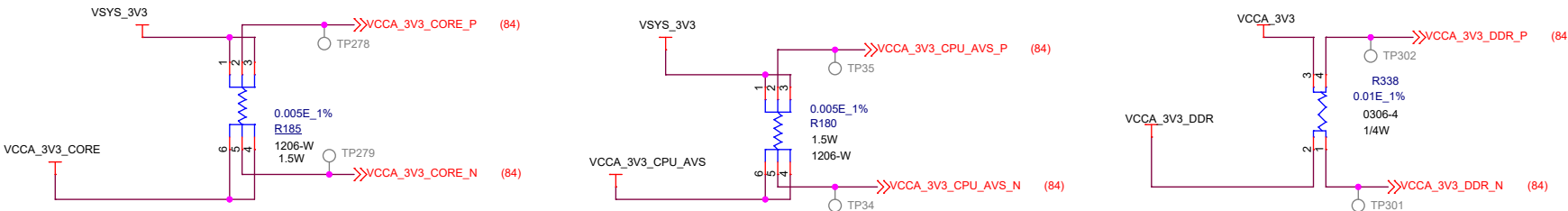
LPDDR4 SDRAM Current Sense Resistors



Peripheral Current Sense Resistors

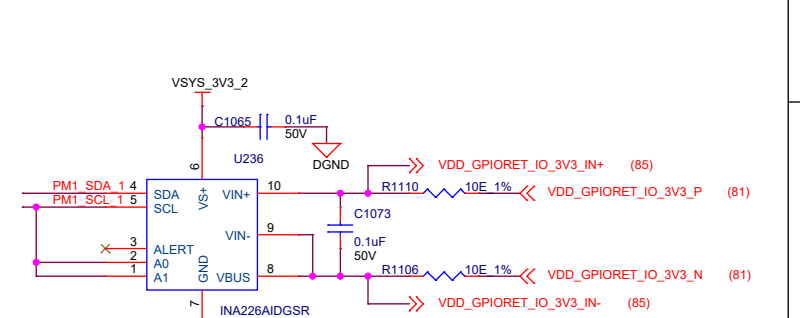
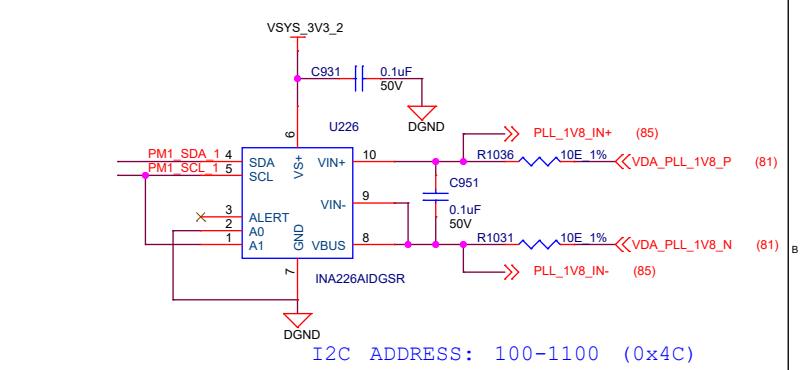
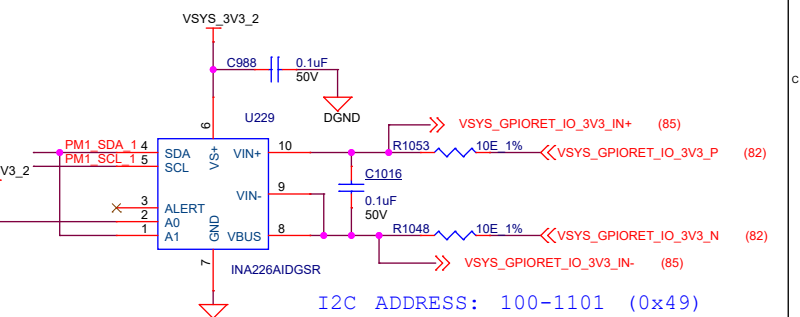
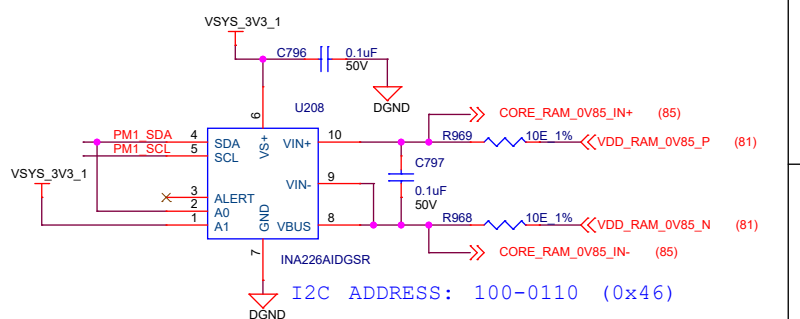
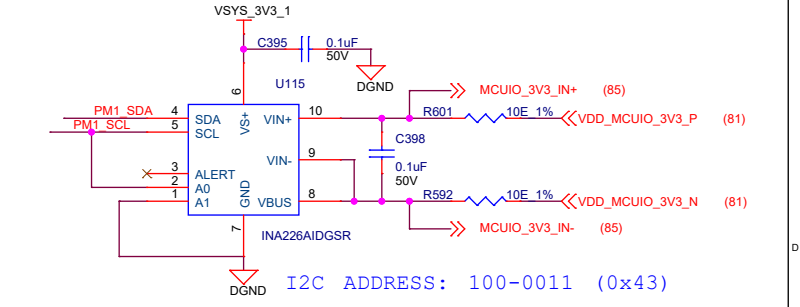
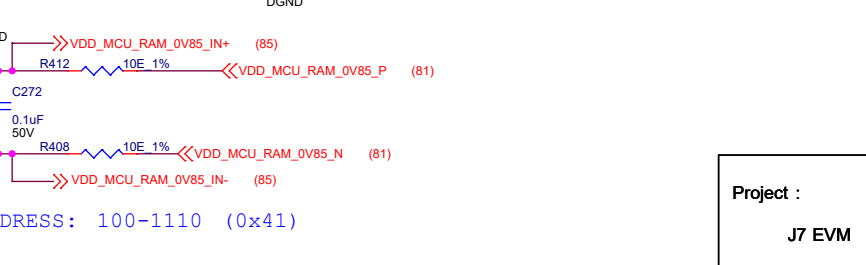
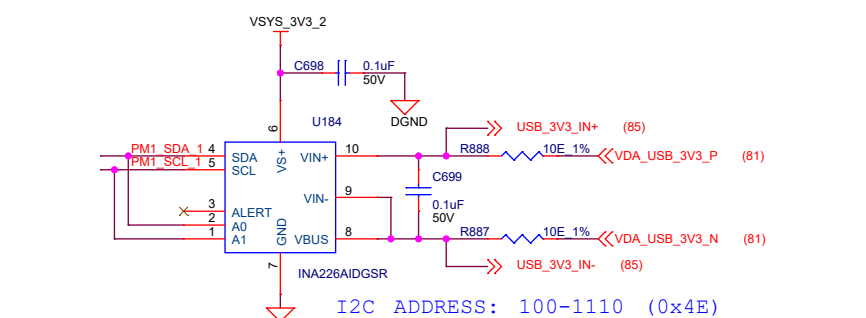
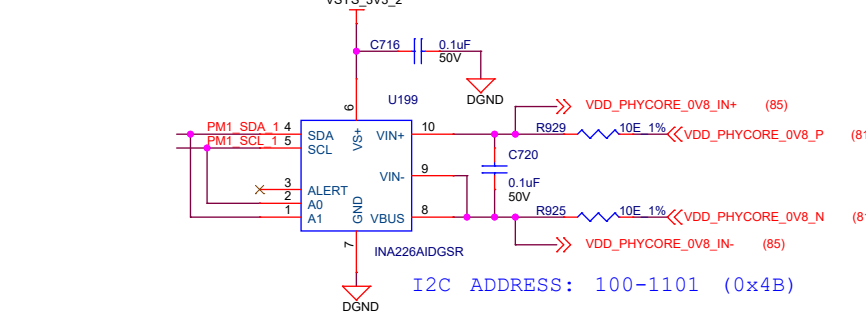
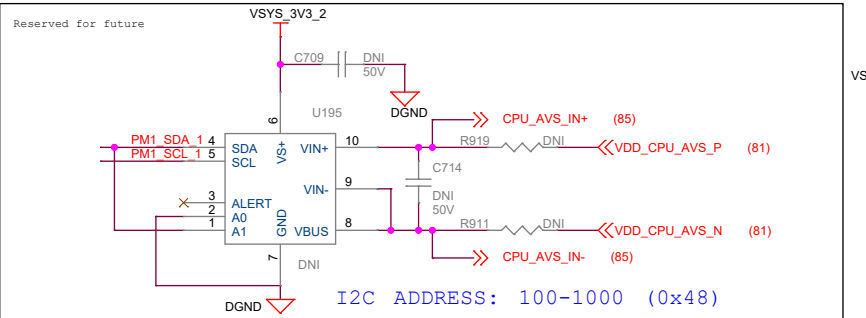
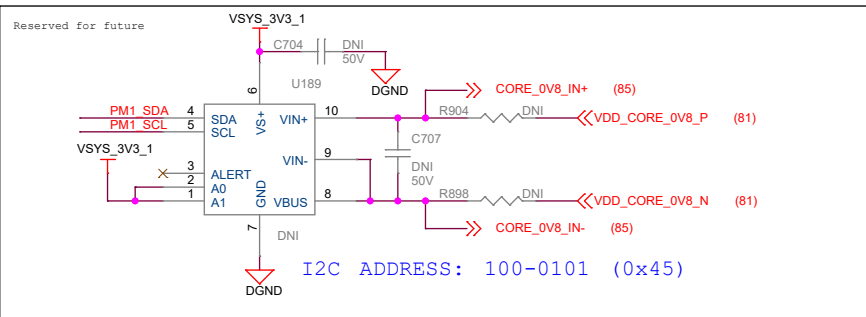
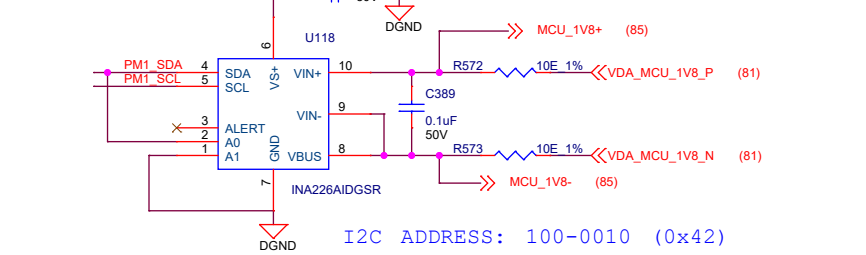
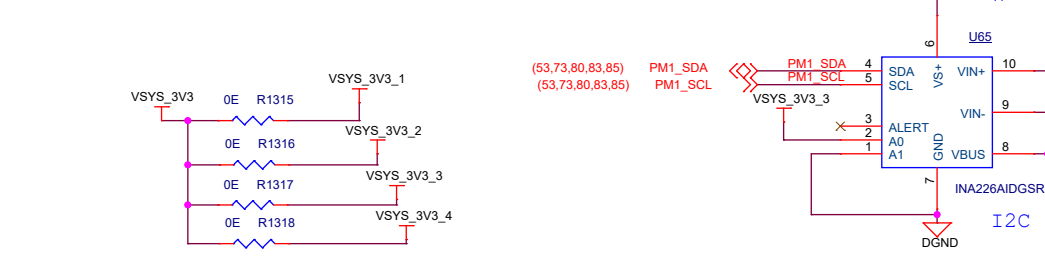
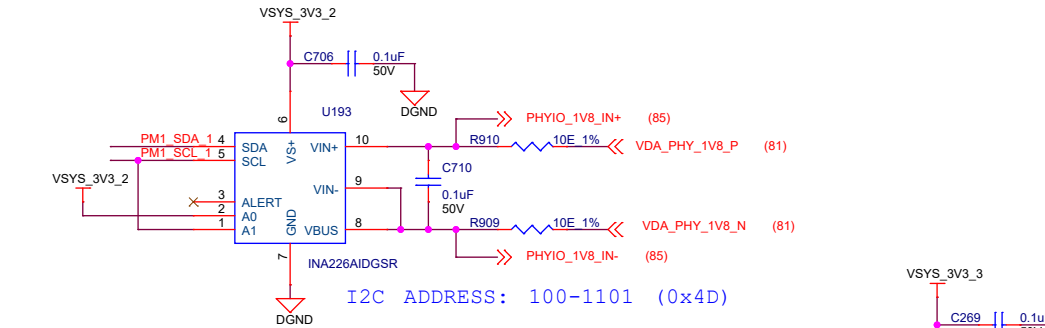
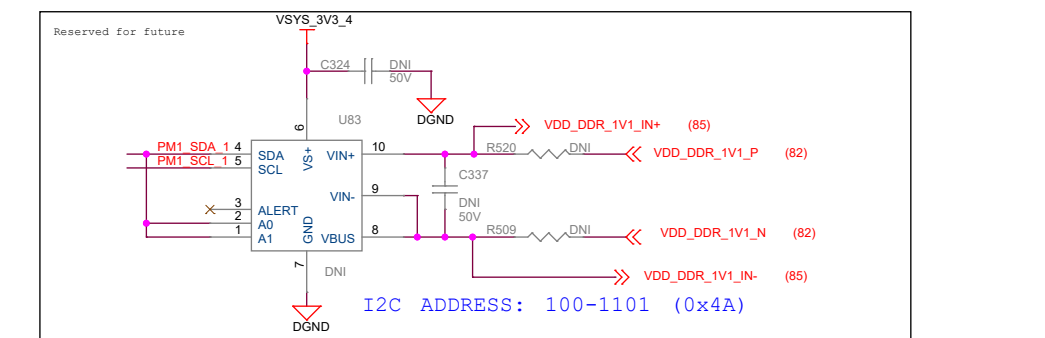
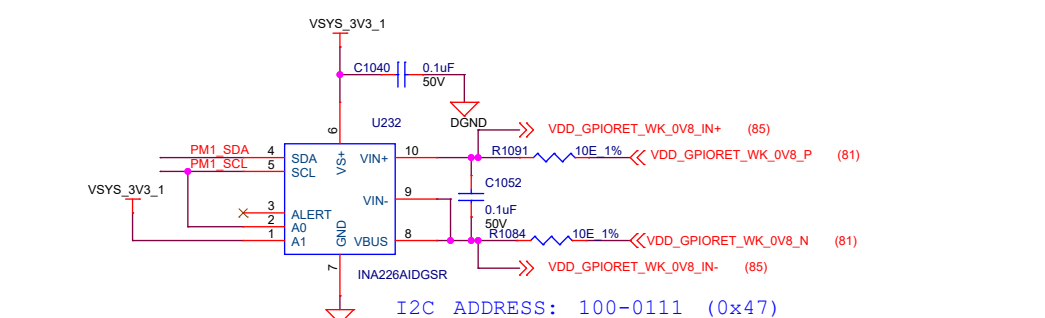
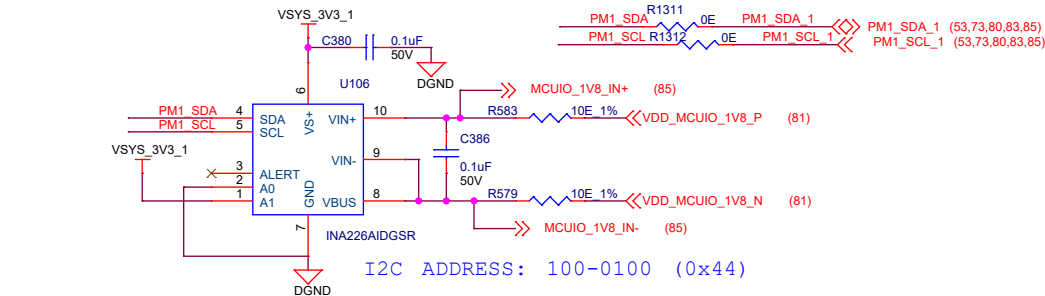
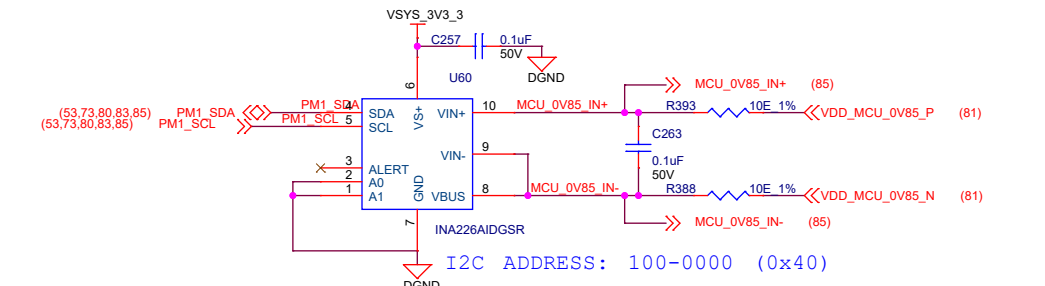


CORE, AVS and DDR input supply sense resistors



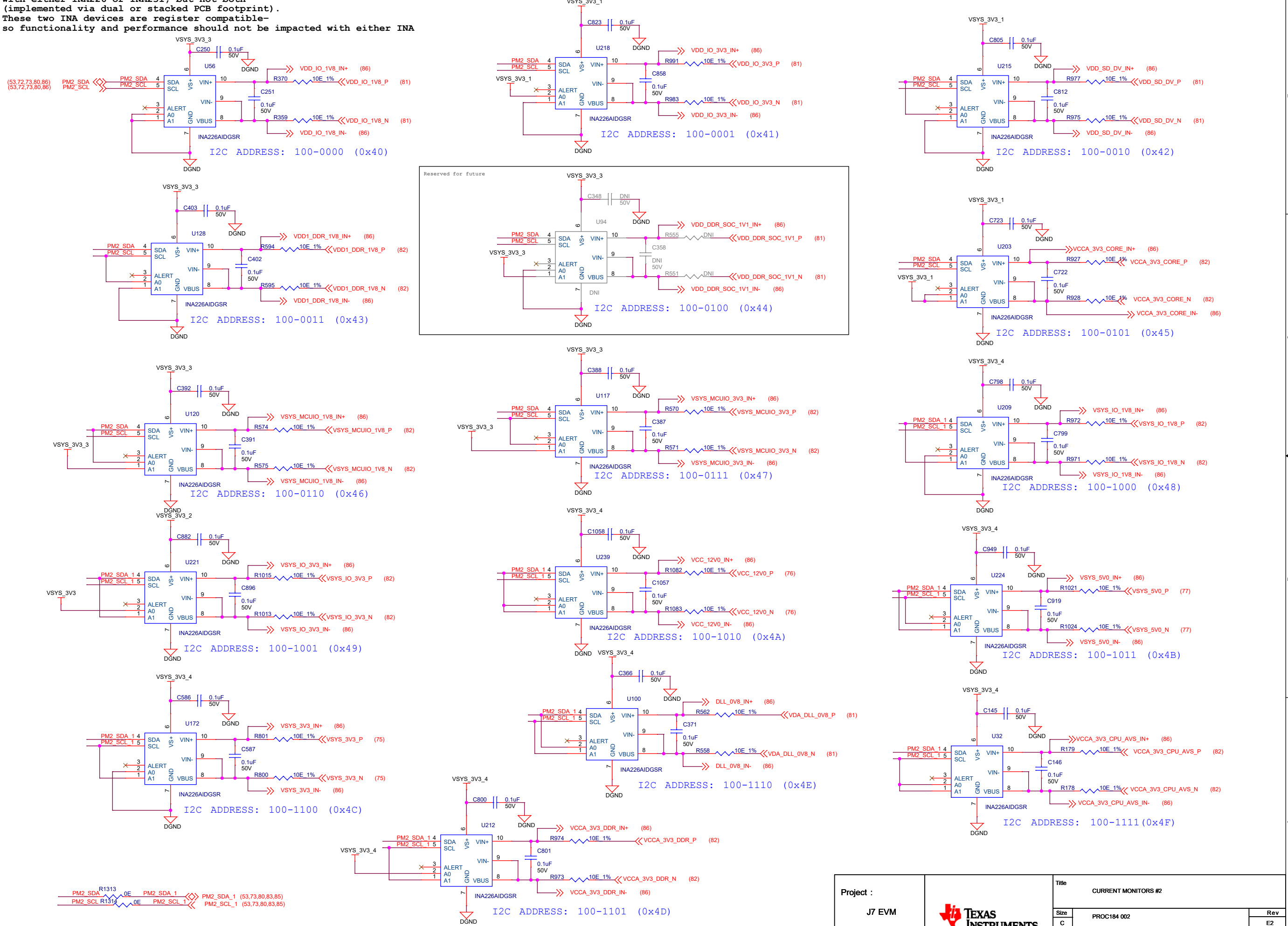
Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible - so functionality and performance should not be impacted with either INA

CURRENT MONITORS #1



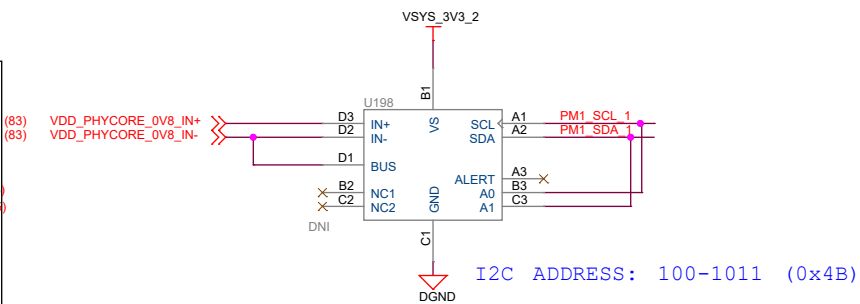
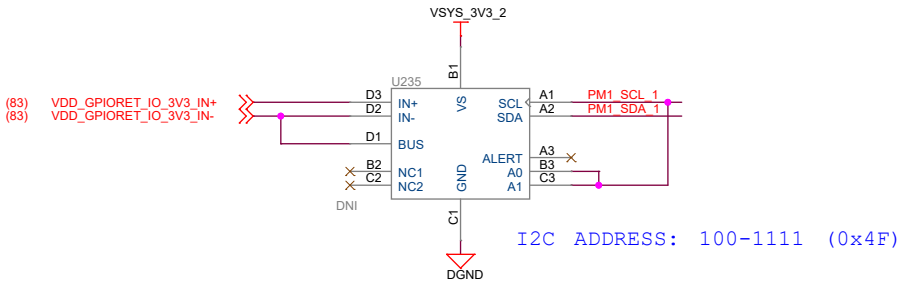
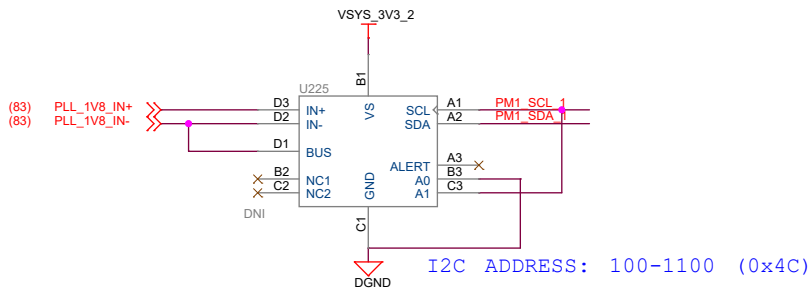
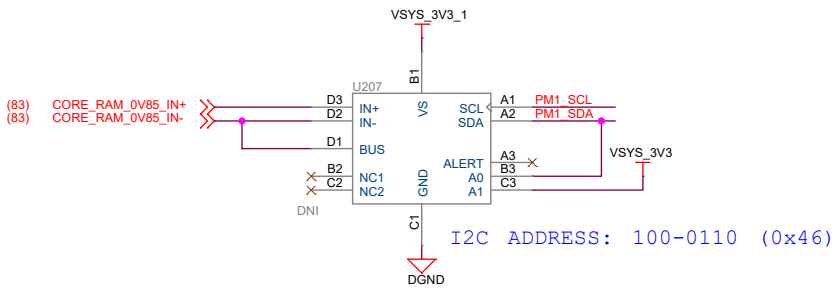
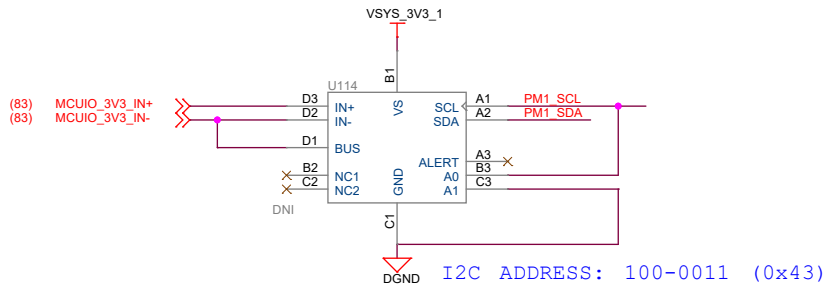
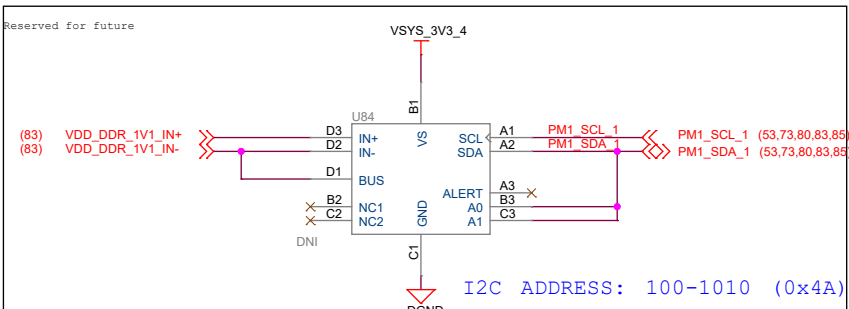
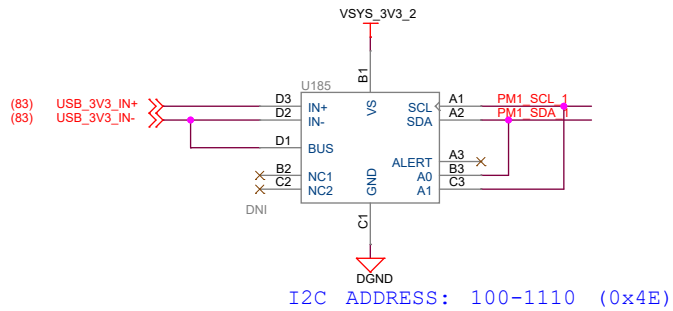
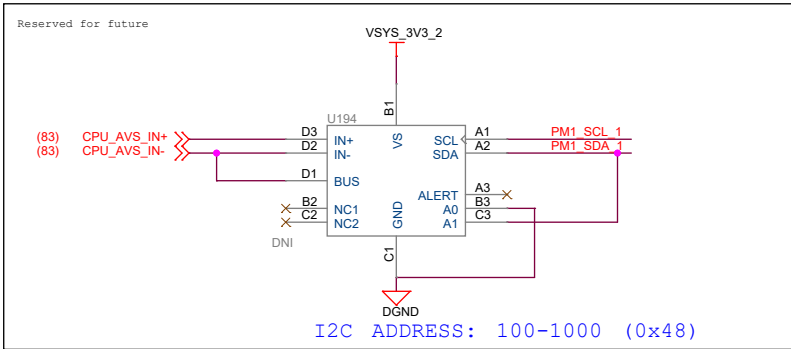
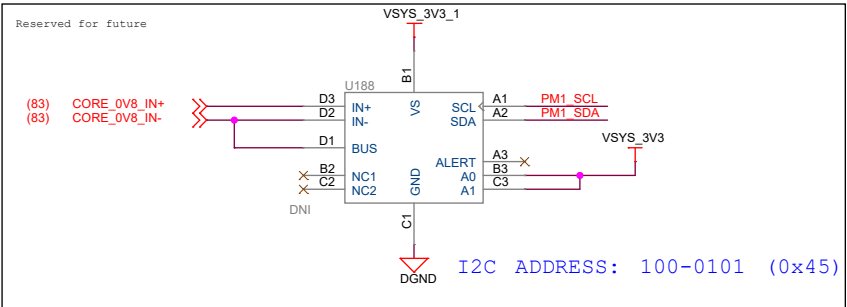
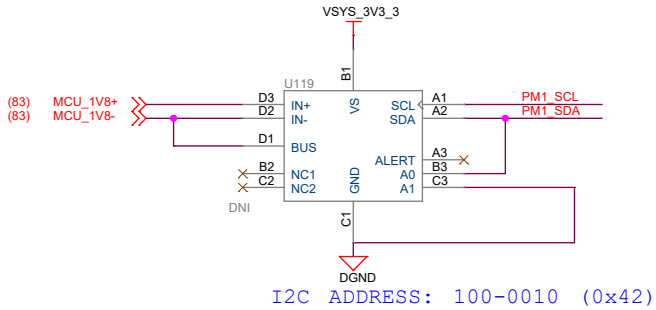
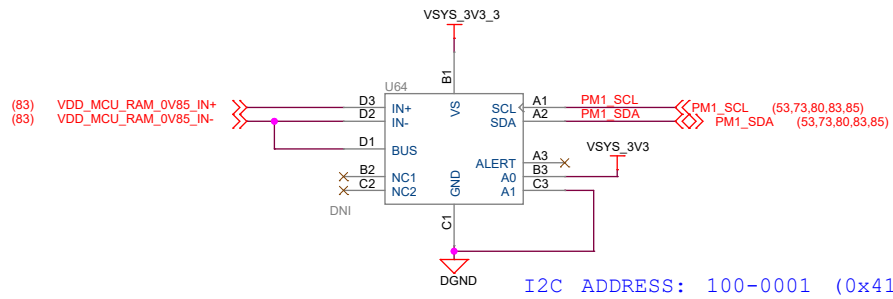
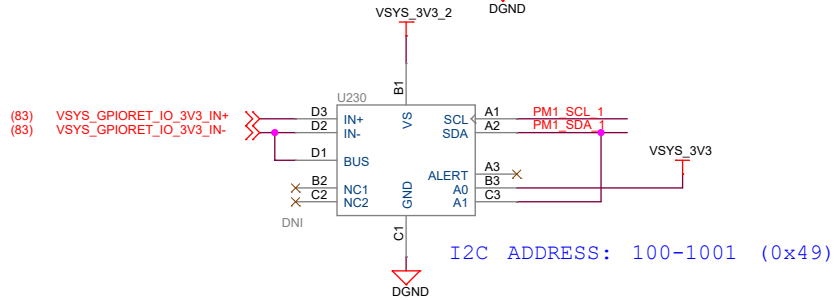
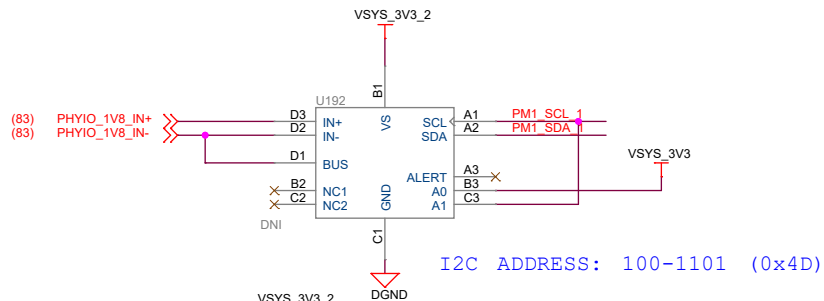
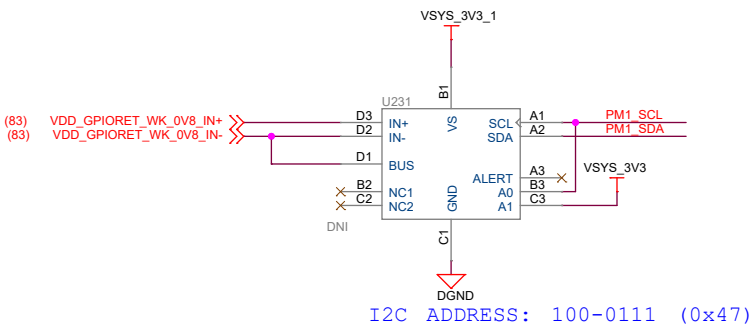
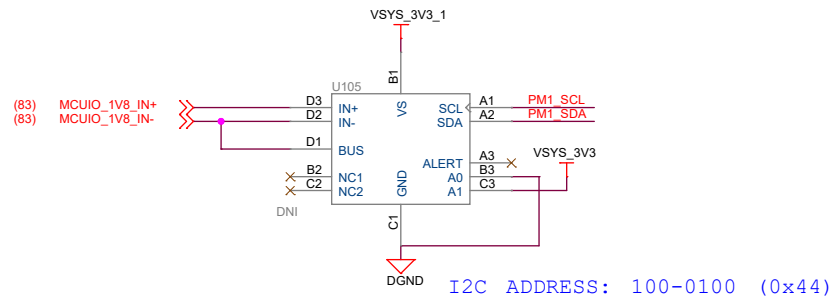
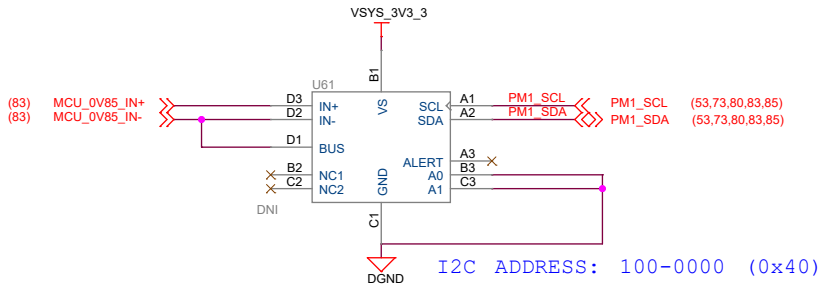
Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

CURRENT MONITORS #2



CURRENT MONITORS - INA231

Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA



Project :

J7 EVM



Title CURRENT MONITORS#1- INA231

Size PROC184 002

Date: Thursday, August 22, 2024

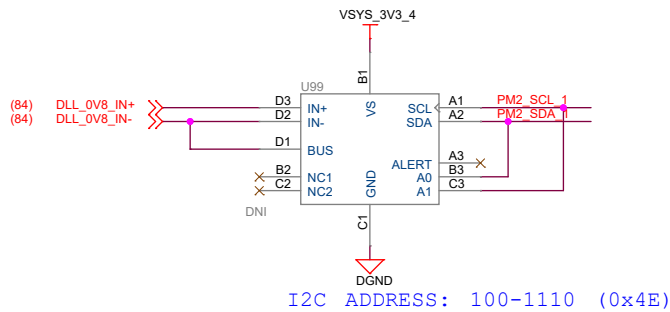
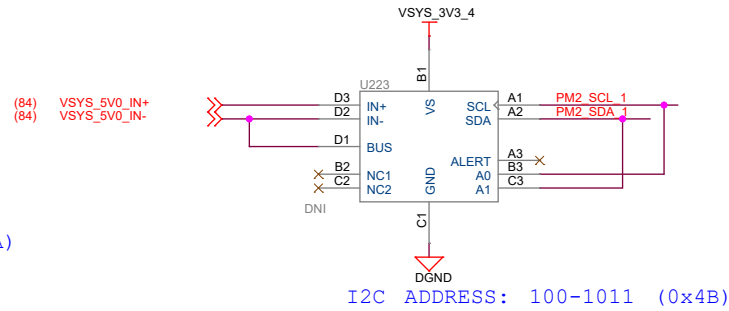
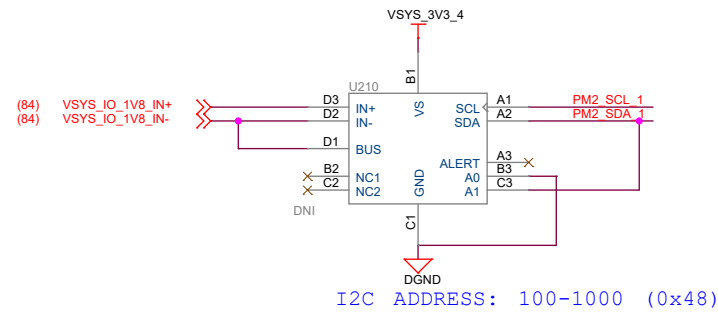
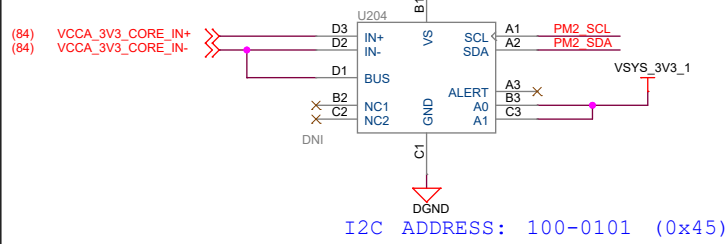
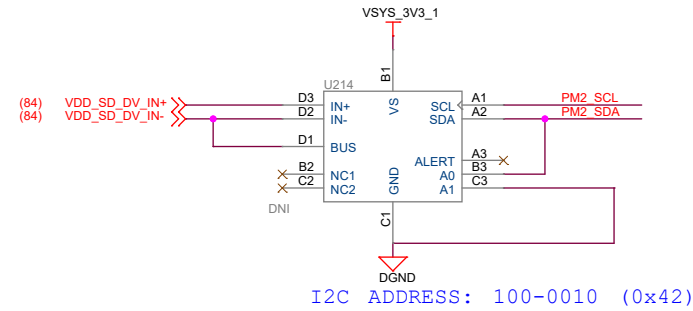
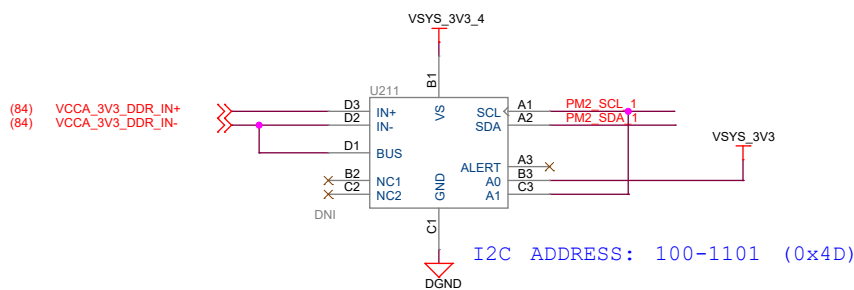
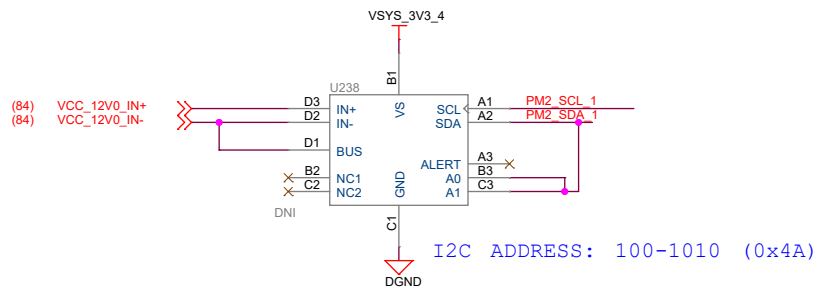
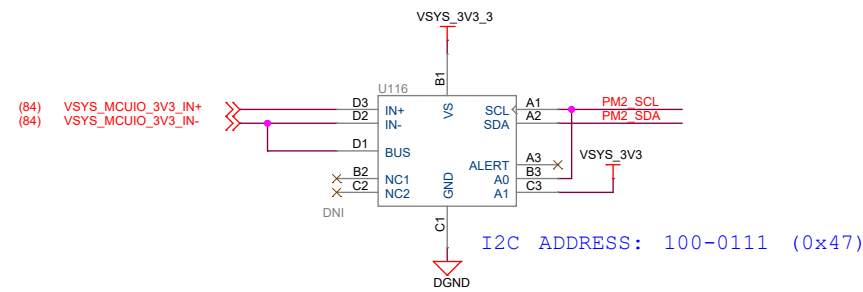
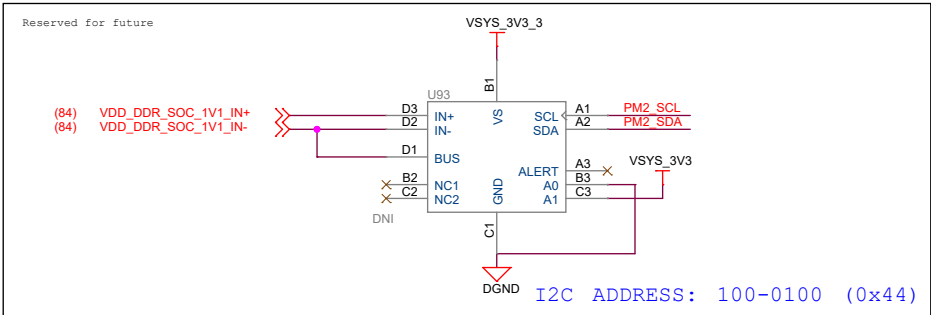
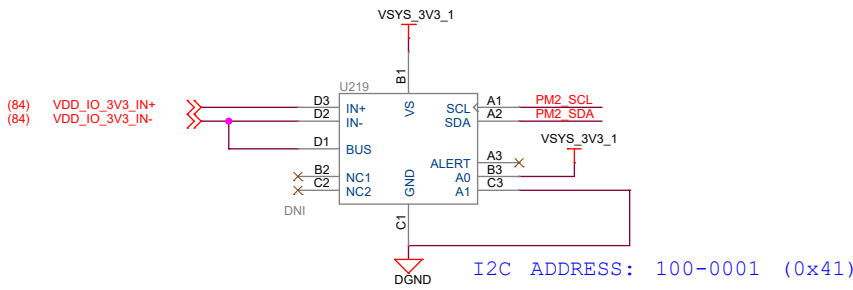
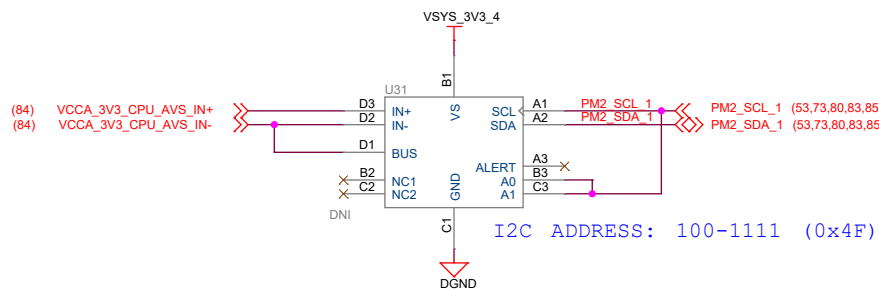
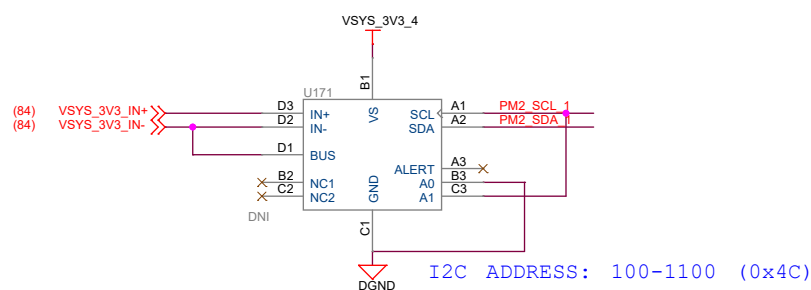
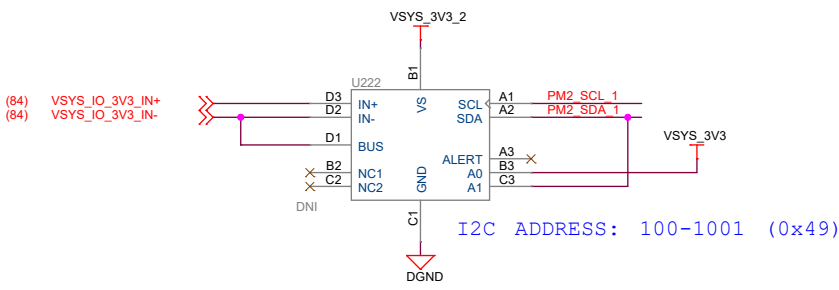
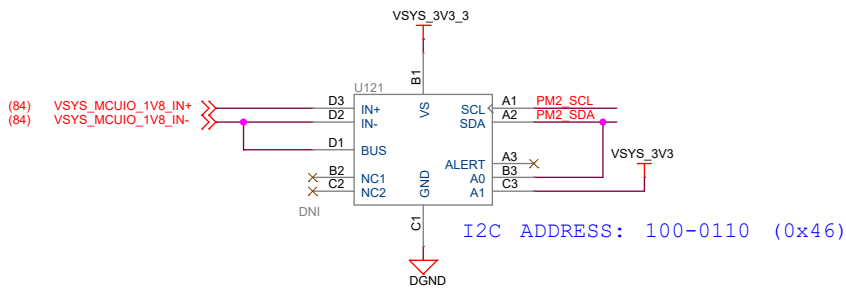
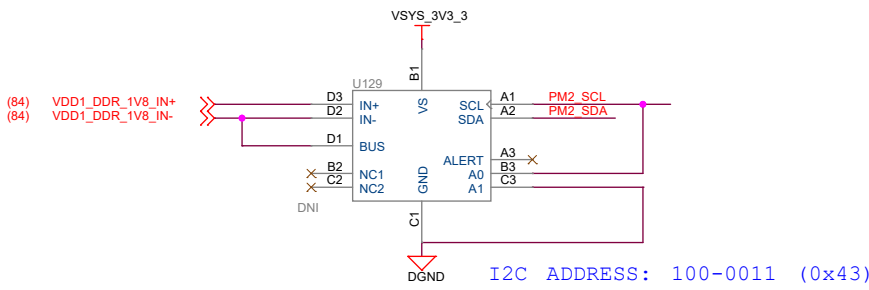
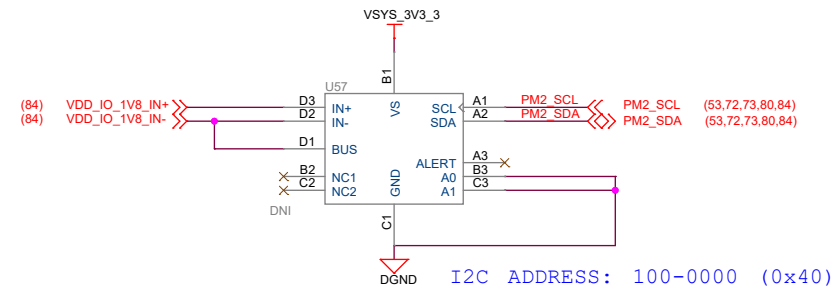
Sheet 83 of 85

Rev

E2

Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

CURRENT MONITORS - INA231

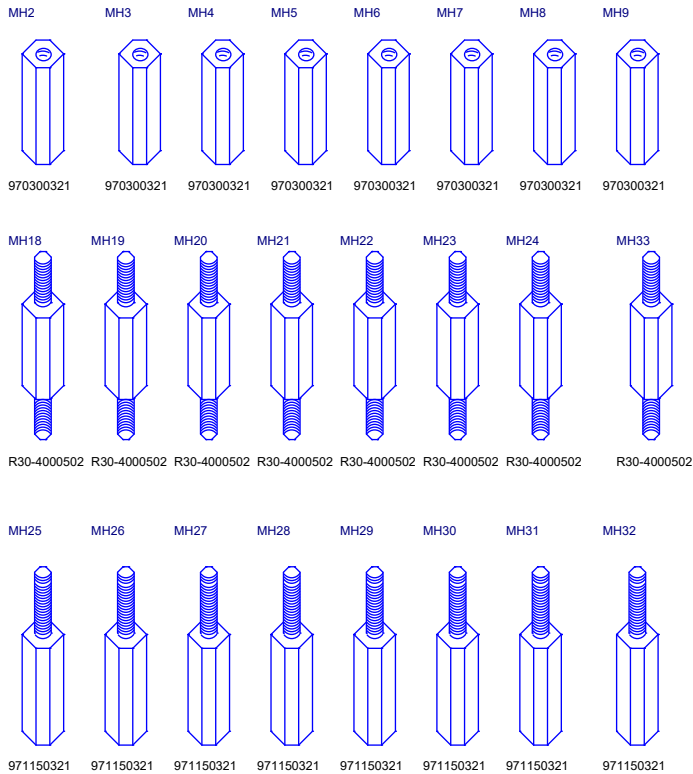


HARDWARE SCHEMATICS

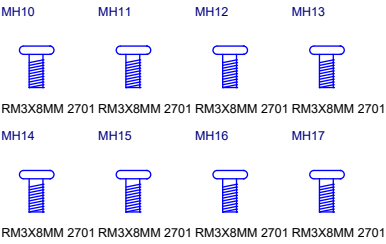
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

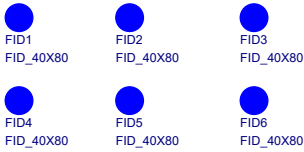
STANDOFFS



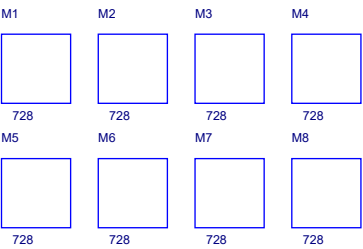
SCREWS



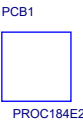
FIDUCIALS



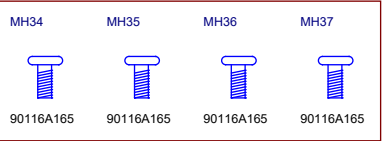
RUBBER FEET



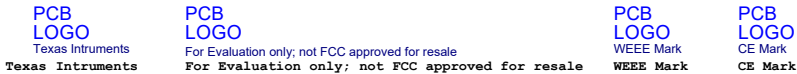
BARE PCB



SCREW FOR FAN ASSEMBLY



LOGOs



LABELS

Board Serial No.



Assembly Revision.



EVM Orderable No.



Orderable Part Numbers

Variant	Label Text
001:Soldered GP SoC	J742S2XG01EVM
002:Soldered HS SoC	J742S2XH01EVM
003:Socketed SoC	J742S2XS01EVM

SOCKET



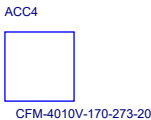
HEAT SINK



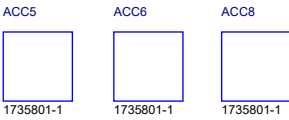
PROCESSOR



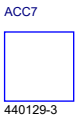
FAN



CRIMP PIN



CONN HOUSING



Project :
J7 EVM



Title		
HARDWARE SCHEMATICS		
Size	Rev	
C	PROC184 002	E2
Date:	Wednesday, September 18, 2024	Sheet 85 of 85