

J742S2/TDA4VPE/TDA4APE Evaluation Module

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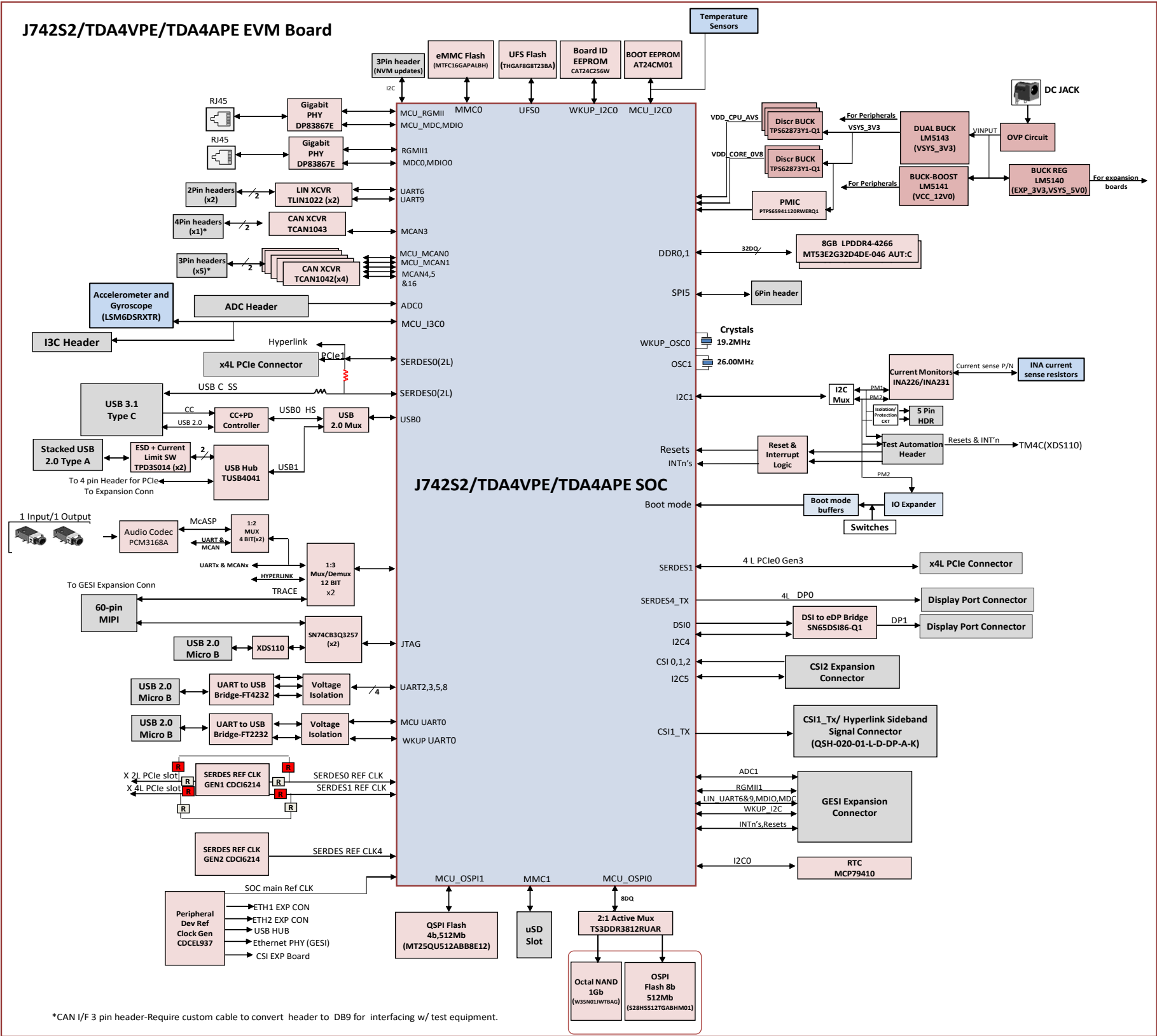
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REVISION HISTORY #1

	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	0.1	14 DEC 2023	Updated SOC Symbol into TI Breakout schematics drafted from PROC141E4A. Deleted unused sections of the schematics; DDR2, DDR3, ENET-EXP-1, ENET-EXP-2, and corresponding SOC power sections	Mistral Design Team		
	0.2	19 DEC 2023	Deleted SERDES4 Rx testponints. Deleted unused 0.1uF caps on: VDD_CORE: C869, C987, C871, C956, C924, C771 VDD_CPU: C964, C961, C903 VDDSHV0_MCU: C1030 VDDSHV0: C945 VDDS_MMC0: C868 VDDSHV5: C975 VDDS_DDR: U50155, U50190, C1013, U50173, U50181, C946, U50182, U50180, C1061 VDDA_0P8_PLL_DDR2: C991, C1076, C1087, FL195	Mistral Design Team		
	0.3	24 JAN 2024	Updated TI review comments: SOC symbol SERDES PCIe clock out section is updated along with removal of symbol documentation	Mistral Design Team		
E1A	0.4	16 MAY 2024	Updated TI comments DNI - U229 and Populated U230	Mistral Design Team		

REVISION HISTORY #2

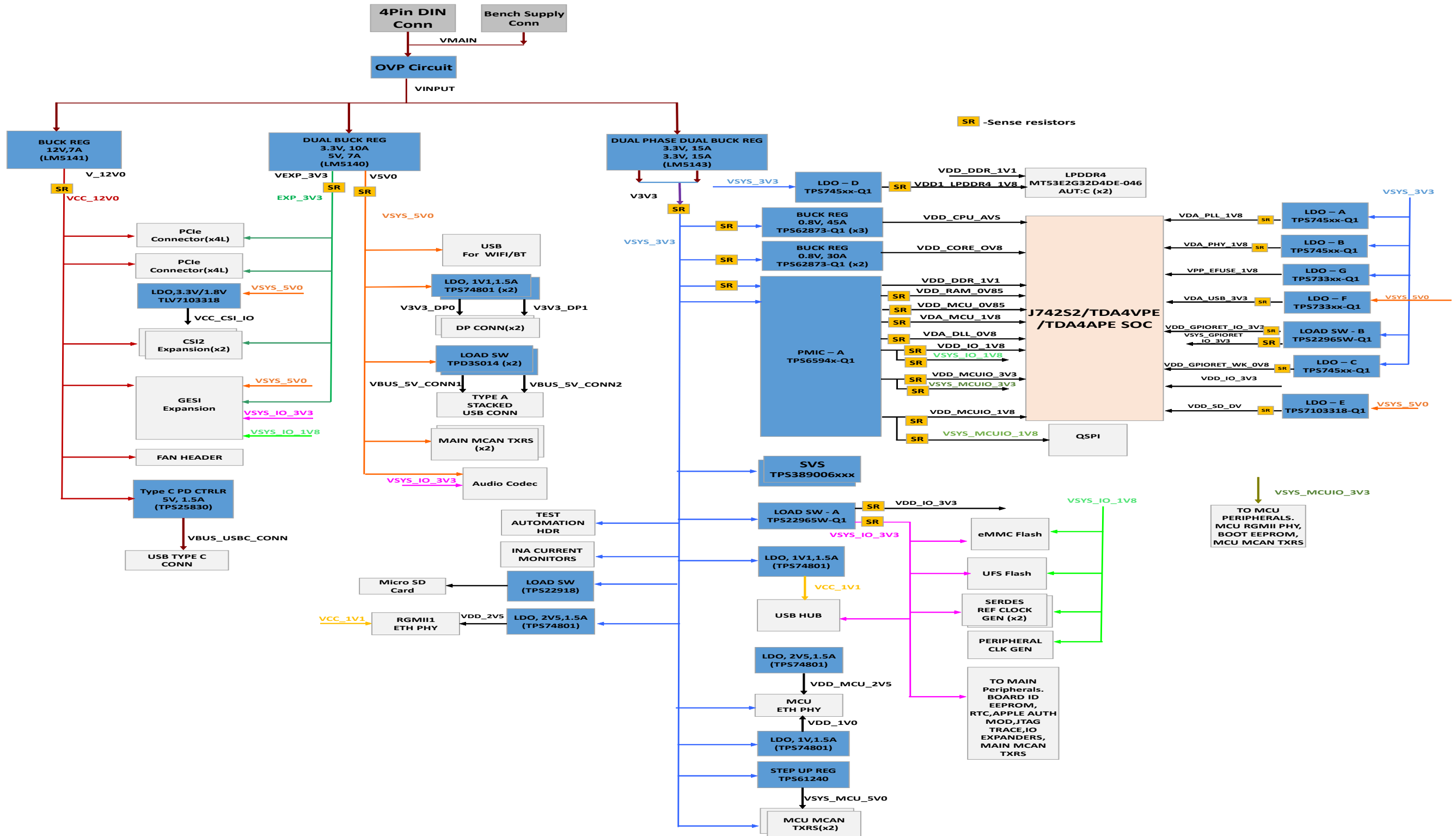
BLOCK DIAGRAM



*CAN I/F 3 pin header-Require custom cable to convert header to DB9 for interfacing w/ test equipment.

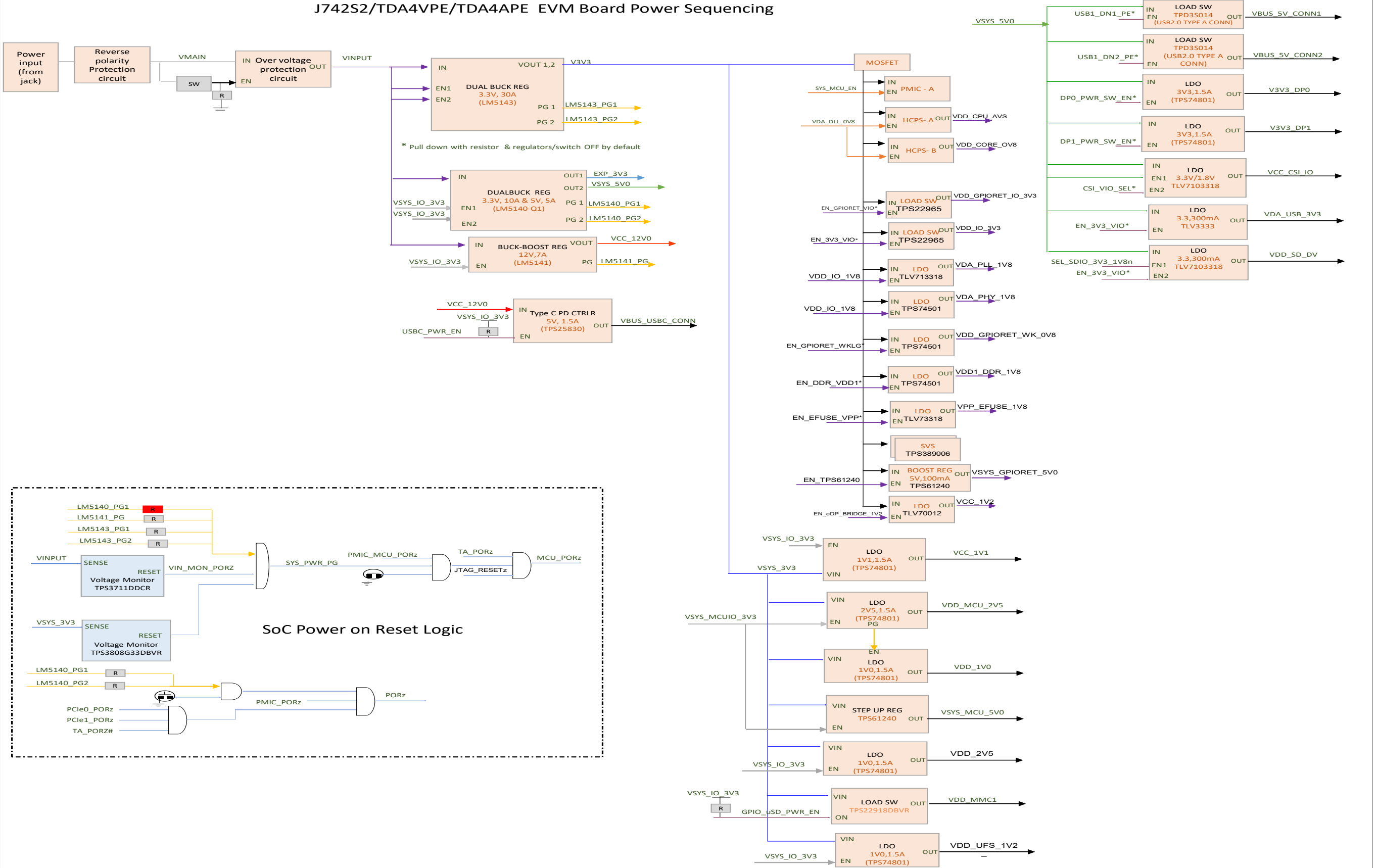
POWER FLOW DIAGRAM

J742S2/TDA4VPE/TDA4APE EVALUATION MODULE POWER Tree




POWER SEQUENCE

J742S2/TDA4VPE/TDA4APE EVM Board Power Sequencing

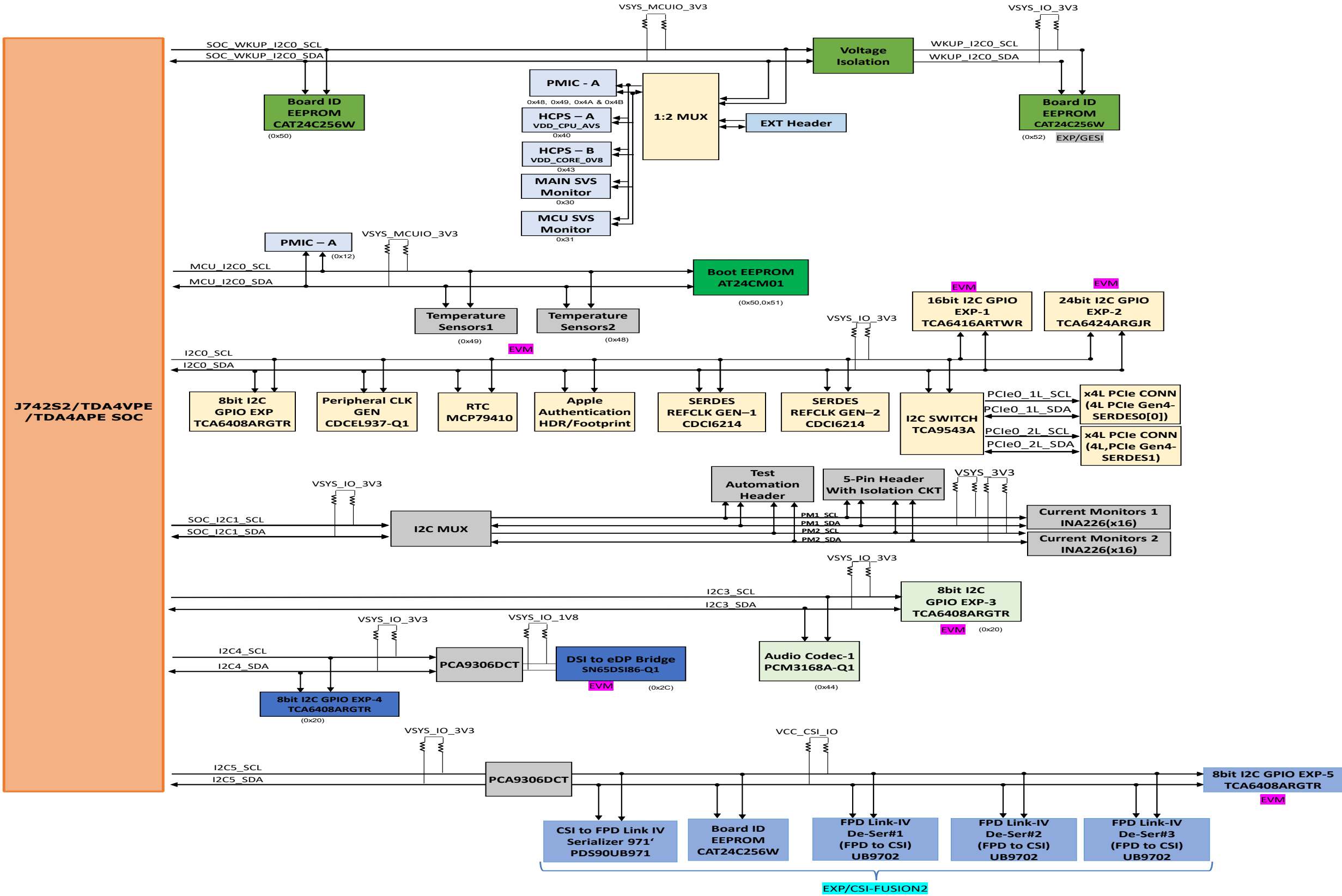


PDN

Please see the PDN file "J742S2 EVM Single Leo Dual HCPS
PDN-3A v0.20.pdf" which is included in the released design files

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I2C TREE



Project :

J7 EVM



Title
I2C TREE

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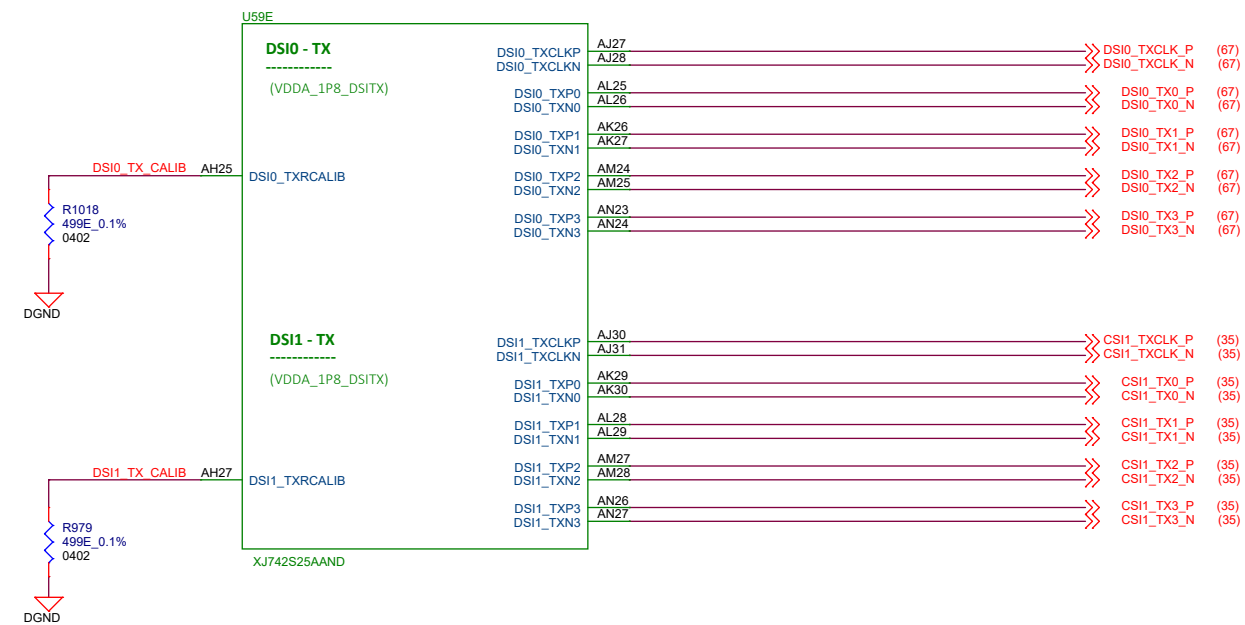
I2C TABLE

Board	Interface name	Part#	Address	J742S2 Port mapping
EVM	Board ID EEPROM	CAV24C256WE-GT3	0x50	WKUP_I2C0
EXP/GESI	Board ID EEPROM	CAT24C256W	0x52	
EVM	PMICs	PMIC A: TPS659413	PMIC A: 0x48, 0x49, 0x4A & 0x4B	
EVM	Tulip - VDD_CPU_AVS Regulator	TPS62873	0x40	
EVM	Tulip - VDD_CORE_OV8 Regulator	TPS62873	0X43	
EVM	MAIN SVS Monitor	PPS38900603NRTERQ1	0X30	
EVM	MCU SVS Monitor	PPS38900603NRTERQ1	0X31	
EVM	Temperature Sensors	TMP100NA/3K	0x48, 0x49	MCU_I2C0
EVM	Boot EEPROM	AT24CM01	0x50, 0x51	
EVM	I2C Switch for PCIe	TCA9543APWR	0x70	Main I2C0
EVM	RTC Clock	MCP79410-I/SN	0x57,0x6F	
EVM	SerDes Clock gen #1 Optional	CDCI6214	Optional	
EVM	SerDes Clock gen #2	CDCI6214	0x77,0x76	
EVM	Pheriphal Clock Gen	CDCEL937-Q1	0x6D	
EVM	16bit I2C GPIO EXPANDER1	TCA6424ARGJR	0x20	
EVM	24bit I2C GPIO EXPANDER2	TCA6424ARGJR	0x22	
EVM	8 bit I2C GPIO Expander4	TCA6408ARGTR	0x20	Main I2C4
EVM	DSI TO eDP BRIDGE	SN65DSI86IPAPQ1	0x2C	
EVM	DSI FPC Connector	<connector interface>		
EVM	I2C Switch for Automation header		0x22	Main I2C1
EVM	Current Monitors and Header		0x40 to 0x4F	
EVM	8bit GPIO Expander3	TCA6408ARGTR	0x20	Main I2C3
EVM	AUDIO IF Codec	PCM3168A-Q1	0x44	
EXP	8bit GPIO Expander5	TCA6408ARGTR	0x20	Main I2C5
EXP/CSI-FUSION2	Board ID EEPROM (Fusion2 Serial Capture)	CAT24C256W	0x52	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #1 (FPD to CSI)	UB9702	0x3D	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #2 (FPD to CSI)	UB9702	0x30	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #2 (FPD to CSI)	UB9702	0x32	
EXP/CSI-FUSION2	CSI to FPD Link IV Serializer 971	UB971	0x18	

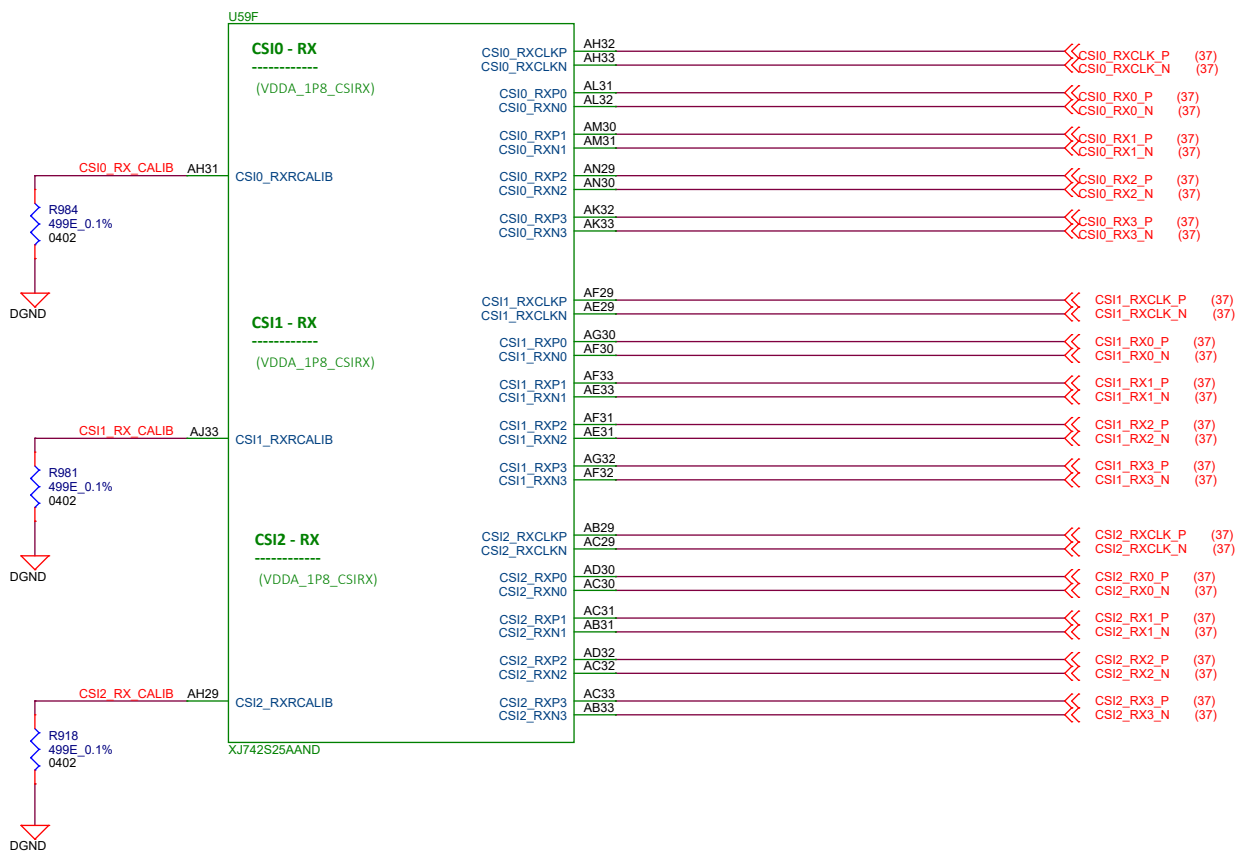
GPIO EXPANDER MAP/TABLE

J742S2 EVM - GPIO Mapping Table						
WKUP Domain						
Net name	J742S2 Mapping					Remarks
	Package	Signal Name	GPIO Number	Input/Output	Default	State
EN_EFUSE_VPP	WKUP_GPIO0_54	WKUP_GPIO0_54	Output	BOOTMODE	Active	High
BOOT_EEPROM_WP	WKUP_GPIO0_1	WKUP_GPIO0_1	Output	BOOTMODE	Active	High
MCU_CAN1_STB	WKUP_GPIO0_2	WKUP_GPIO0_2	Output	BOOTMODE	Active	High
GPIO_MCU_RGMII1_RST#	WKUP_GPIO0_56	WKUP_GPIO0_56	Output	BOOTMODE	Active	low
SYS_IRQz	WKUP_GPIO0_7	WKUP_GPIO0_7	Input	PU	Active	low
OSPI/HYPER_MUX_SEL	WKUP_GPIO0_6	WKUP_GPIO0_6	Output	DIP_SEL	NA	
PMIC_MCU_INT# / H_MCU_INT#	MCU_OSPi1_CSN1	WKUP_GPIO0_39	Input	PU	Active	low
MCU_RGMII1_INT#	WKUP_GPIO0_3	WKUP_GPIO0_3	Input	PU	Active	Low
SYS_MCU_PWRDN	MCU_SPiO_D0	WKUP_GPIO0_55	Output	BOOTMODE	Active	low
MCU_CAN0_STBz	MCU_SPiO_D1	WKUP_GPIO0_69	Output	BOOTMODE	Active	low
LSM6DSOX_INT/LSM6DSRX_INT	WKUP_GPIO0_57	WKUP_GPIO0_57	Input	BOOTMODE	NA	
PM_I2C_SEL	WKUP_GPIO0_66	WKUP_GPIO0_66	Output	BOOTMODE	Active	High
USBC_DIR_SOC	MCU_OSPiO_CSN1	WKUP_GPIO0_28	Input	PU	Active	High
I2C0_IOEXP_INT#	MCU_ADC1_AIN7	WKUP_GPIO0_86	Output	PU	Active	Low
CANiO_RET_WAKE	MCU_SPiO_CS0	WKUP_GPIO0_70	Input	PU	NA	
						Push-button wake signal
Main Domain						
MAIN_RET_WAKE	GPIO0_11	GPIO0_11	Input	PU	NA	
HYP1_RXFLCLK_MUX	MCASP0_AXR2	GPIO0_18	Input	PU	Active	Low
SEL_SDIO_3V3_1V8n	MCAN15_RX	GPIO0_8	Output	NA	Active	low
CSI2_EXP_A_GPIO2(MCASP4_AXR1/T_RC_DATA16_MUX)	MCAN0_RX	GPIO0_26	I/O	NA	NA	
CSI2_EXP_A_GPIO4(MCASP4_AXR3/T_RC_DATA5_MUX)	MCAN1_RX	GPIO0_28	I/O	NA	NA	
TRC_DATA0_MUX	MCAN13_TX	GPIO0_3	Input	PU	NA	
SOC_GPIO0_21_MUX	MCASP2_ACLKX	GPIO0_21	Input	PU	Active	Low
						RGMII1 INT signal
GPIO Expander - 1 Part# TCA6416ARTWR						
I2C0/0x20	P00	PCle1_2L_MODE_SEL	Input	DIP_SEL	NA	PCle1 4-Lane Mode Select ('0' - Root Complex, '1' - End Point)
	P01	PCle1_4L_PERSTz	Input	PD	Active	low
	P02	PCle1_2L_RC_RSTz	Output	PD	Active	low
	P03	PCle1_2L_EP_RST_EN	Output	PD	Active	low
	P04	PCle0_4L_MODE_SEL	Input	DIP_SEL	NA	PCle0 2-Lane Mode Select ('0' - Root Complex, '1' - End Point)
	P05	PCle0_4L_PERSTz	Input	PD	Active	low
	P06	PCle0_4L_RC_RSTz	Output	PD	Active	low
	P07	PCle0_4L_EP_RST_EN	Output	PD	Active	low
	P10	PCle1_4L_PRSNT#	Input	PU	Active	High
	P11	PCle0_4L_PRSNT#	Input	PU	Active	High
	P12	CDCI1_OE1/OE4	Output	PU	Active	High
	P13	CDCI1_OE2/OE3	Output	PU	Active	High
	P14	AUDIO_MUX_SEL	Output	PU	Active	High
	P15	EXP_MUX2	Output	NA	NA	
	P16	EXP_MUX3	Output	NA	NA	
	P17	GESI_EXP_PHY_RSTz	Output	PU	Active	High
						EXP_RSTz - Terminated with Test point
GPIO Expander - 2 Part# TCA6424ARGJR						
I2C0/0x22	P00	R_GPIO_RGMII1_RST	Output	PU	Active	low
	P02	GPIO_USD_PWR_EN	Output	PU	Active	High
	P03	USBC_PWR_EN	Output	PU	Active	High
	P04	USBC_MODE_SEL1	Output	DIP_SEL	NA	
	P05	USBC_MODE_SELO	Output	DIP_SEL	NA	
	P06	GPIO_LiN_EN	Output	PD	Active	High
	P07	R_CAN_STB	Output	PU	Active	High
	P10	CTRL_PM_I2C_OE#	Output	PD	Active	High
	P13	CDCI2_RSTZ	Output	PU	Active	low
	P14	USB2_0_MUX_SEL	Output	PD	Active	High
	P15	CANUART_MUX_SELO	Output	PD	Active	High
	P16	CANUART_MUX2_SEL1	Output	PU	Active	High
	P17	CANUART_MUX1_SEL1	Output	PU	Active	High
	P25	USER_INPUT1	Input	DIP_SEL	NA	
	P26	USER_LED1	Output	PD	Active	High
	P27	USER_LED2	Output	PD	Active	High
						User LED2 Enable ('1' - LED Off, '0' - LED On)
GPIO Expander - 3 Part# TCA6408ARGTR						
I2C3/0x20	P0	CODEC_RSTZ	Output	PD	Active	low
	P1	CODEC_SPARE1	NA	UNUSED	NA	
						Not used (test point)
GPIO Expander - 4 Part# TCA6408ARGTR						
I2C40x20	P0	DP0_PWR_SW_EN	Output	PD	Active	High
	P1	DP1_PWR_SW_EN	Output	PD	Active	High
	P2	GPIO_eDP_ENABLE	Output		Active	High
						DSi to eDP bridge enable
GPIO Expander - 5 Part# TCA6408ARGTR						
I2C5/0x20	P0	CSI2_EXP_RSTZ	Output	PD	Active	low
	P1	CSI2_EXP_A_GPIO0	IO	NA	NA	
	P2	CSI2_EXP_A_GPIO1	IO	NA	NA	
	P3	CSI2_EXP_A_GPIO3	IO	NA	NA	
	P4	CSI2_EXP_B_GPIO1	IO	NA	NA	
	P5	CSI2_EXP_B_GPIO2	IO	NA	NA	
	P6	CSI2_EXP_B_GPIO3	IO	NA	NA	
	P7	CSI2_EXP_B_GPIO4	IO	NA	NA	
						CSI2 Expansion Board Specific.

DSI



CSI



Project :

J7 EVM

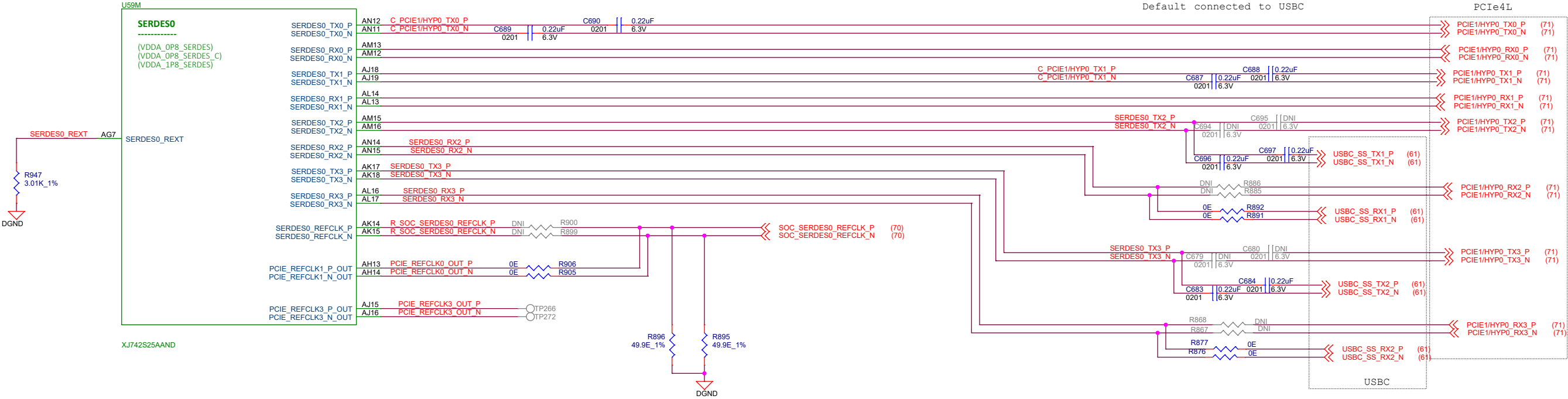


Title	CSI & DSI INTERFACE
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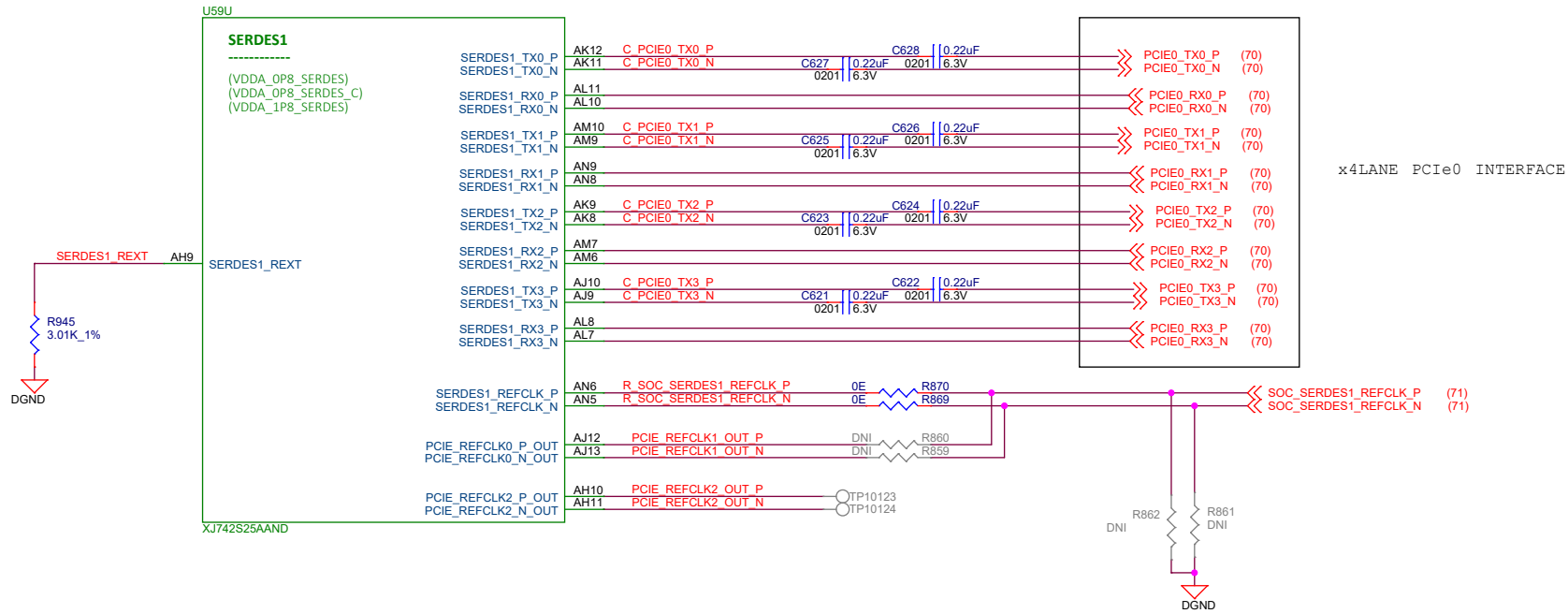
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SERDES0

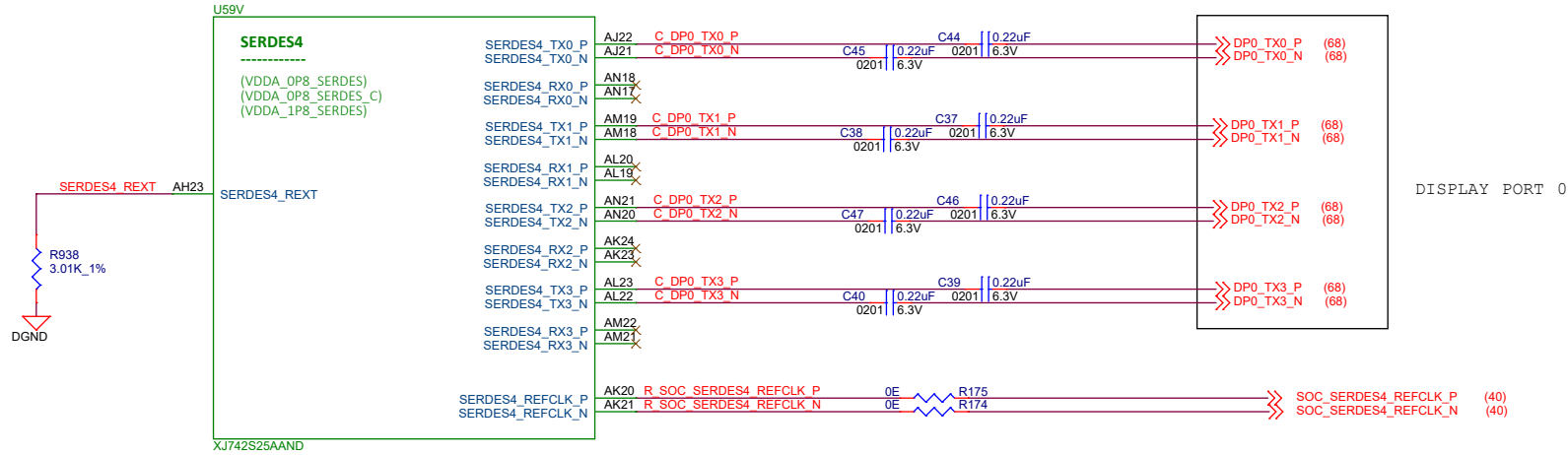
Dedicated 2L to PCIe4L connector, x2L
will be resistor muxed with USBC
Default connected to USBC



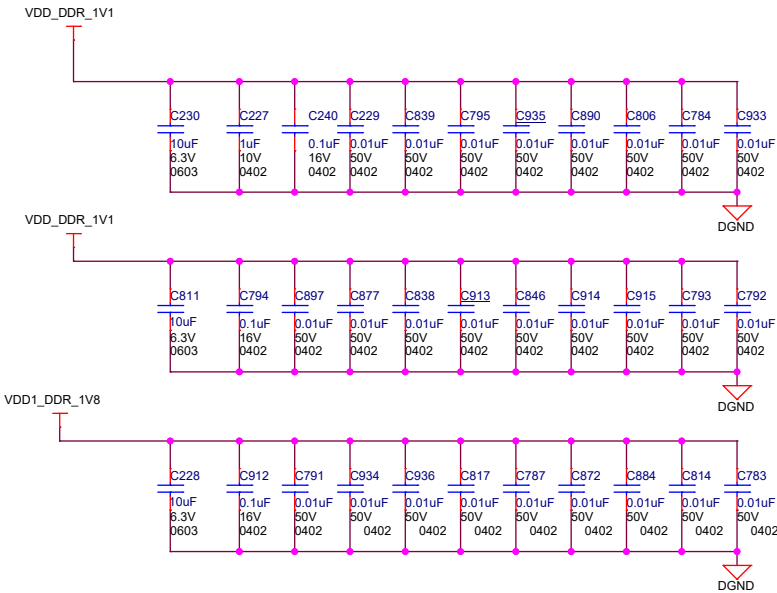
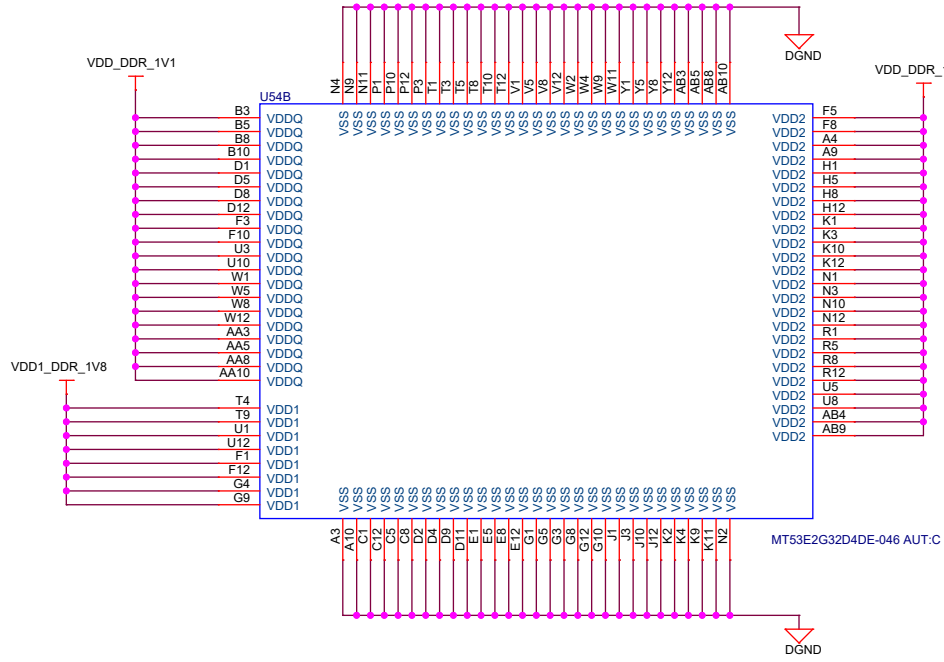
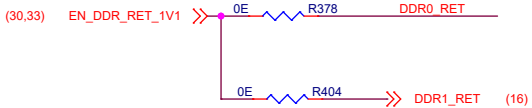
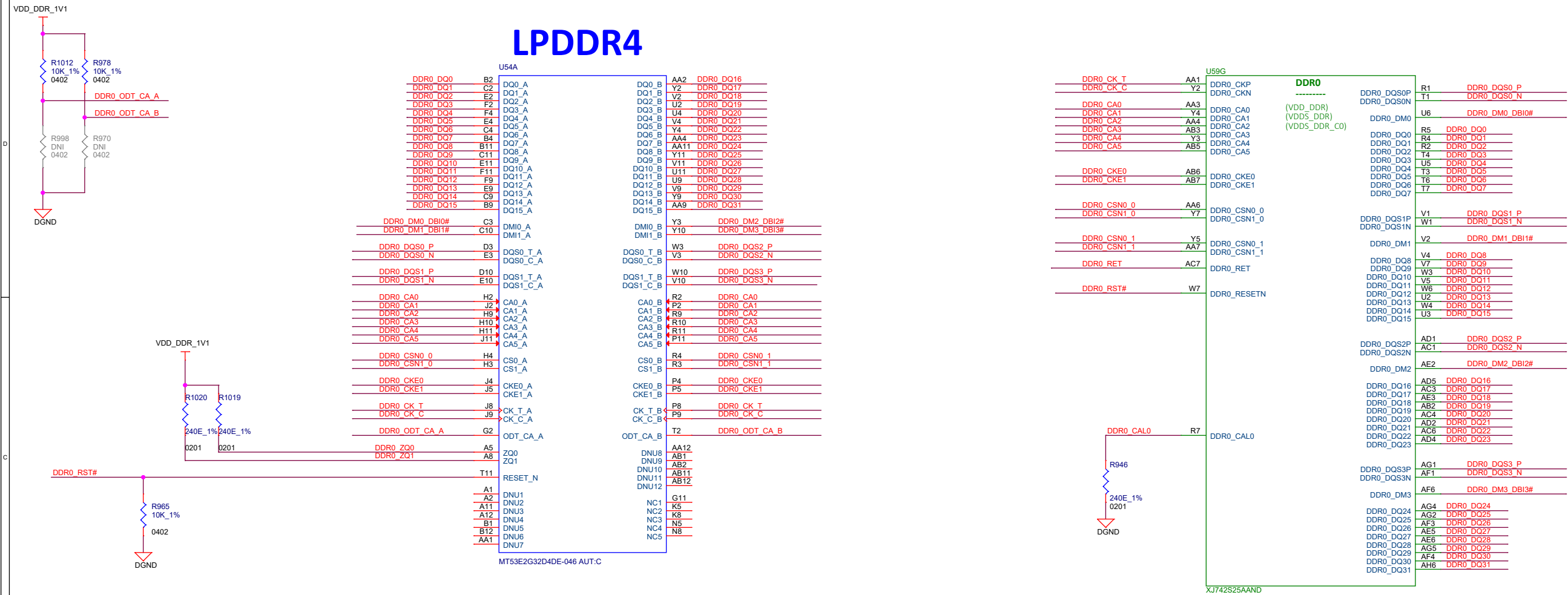
SERDES1

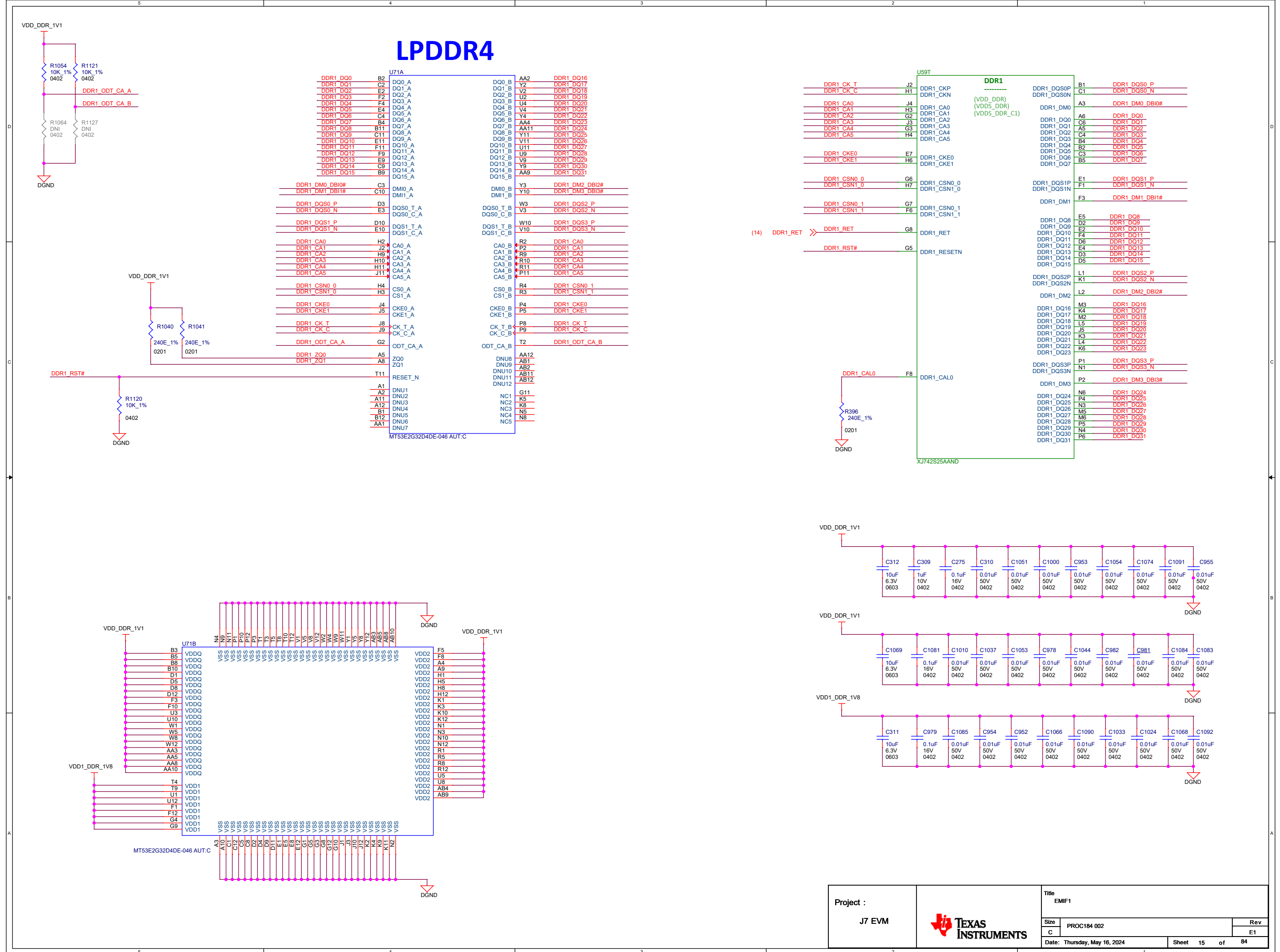


SERDES4

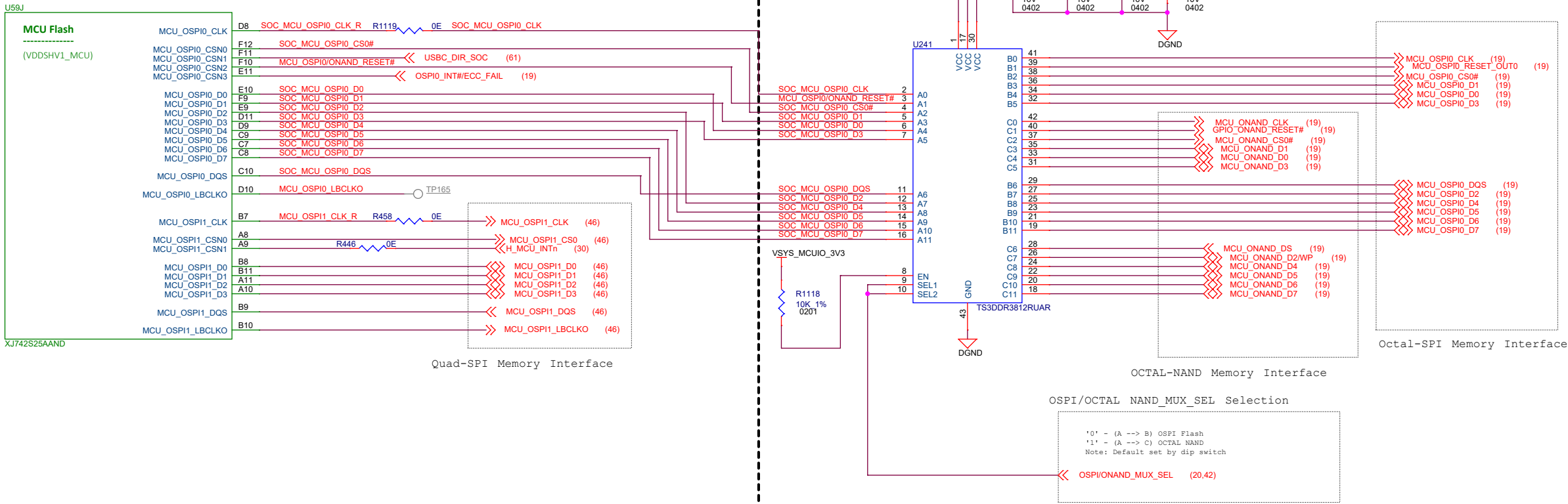


LPDDR4



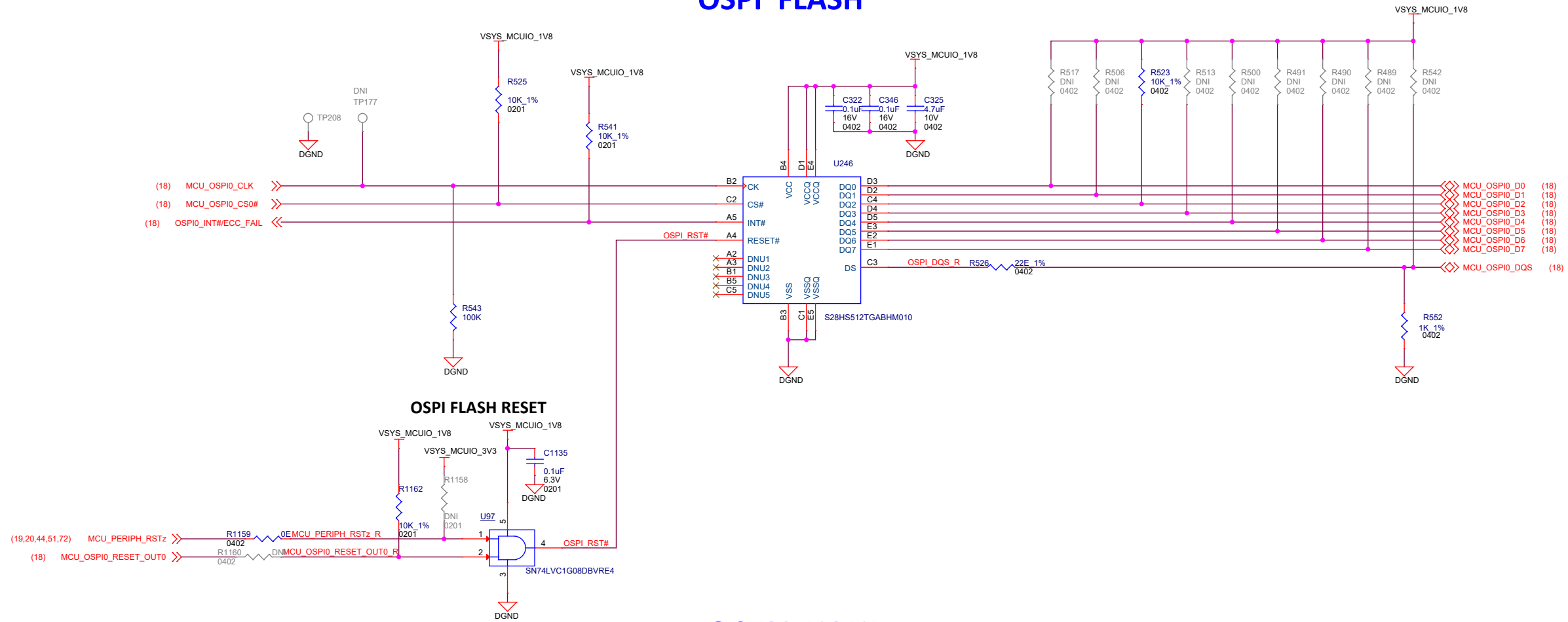


MCU FLASH

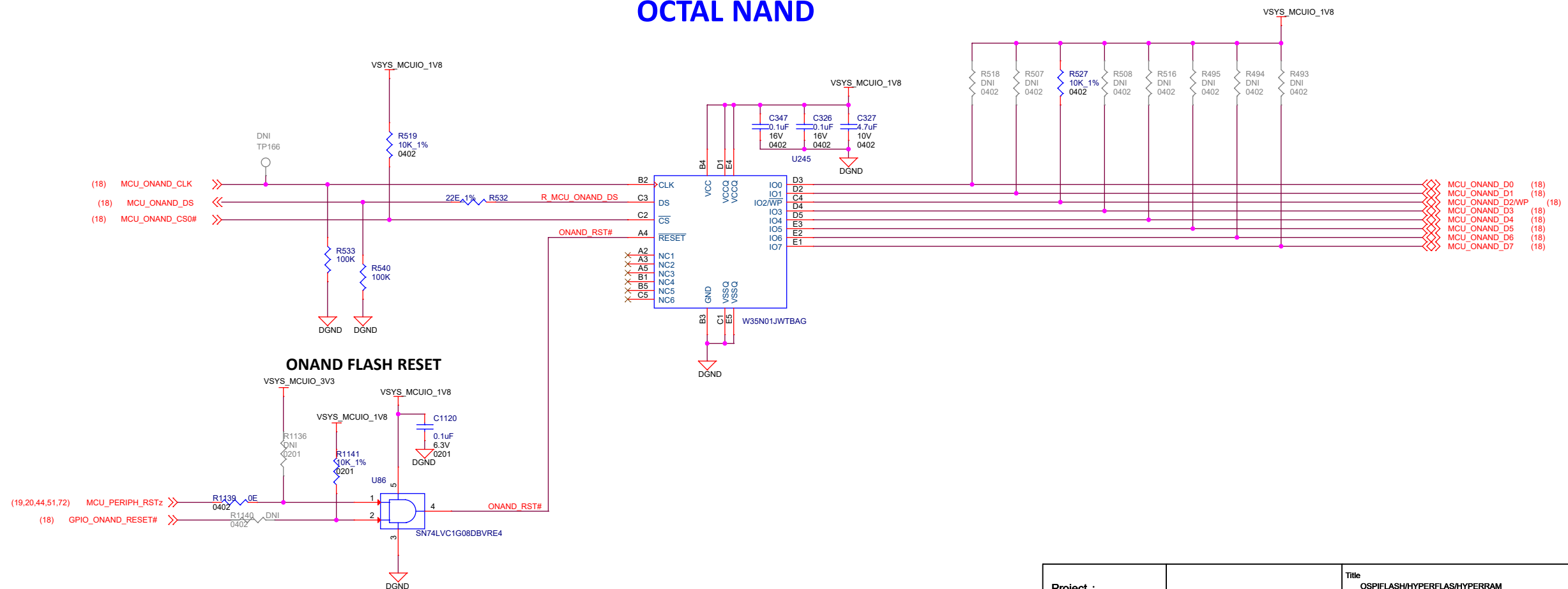


Note: 1K resistors are used to isolate the BOOTMODE control logic after the value is latched.

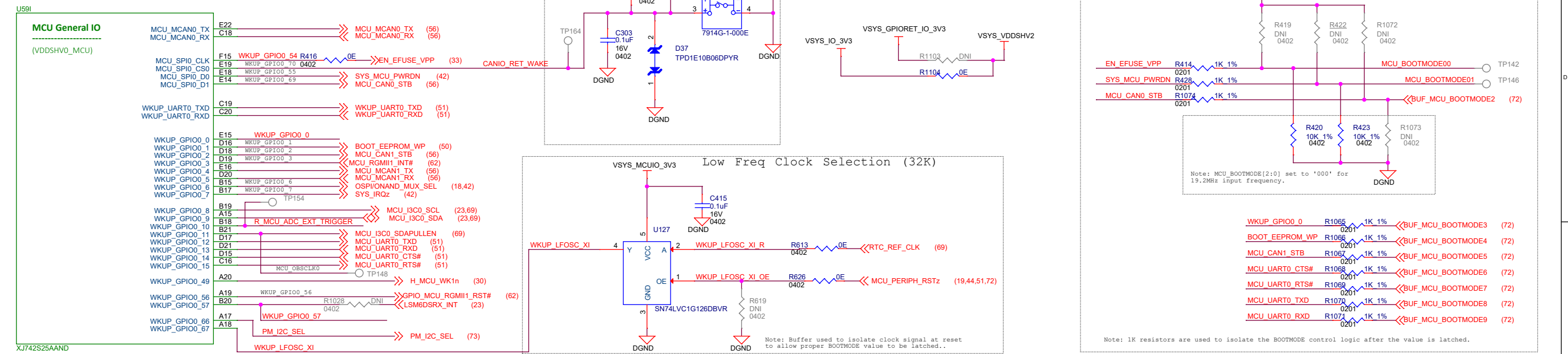
OSPI FLASH



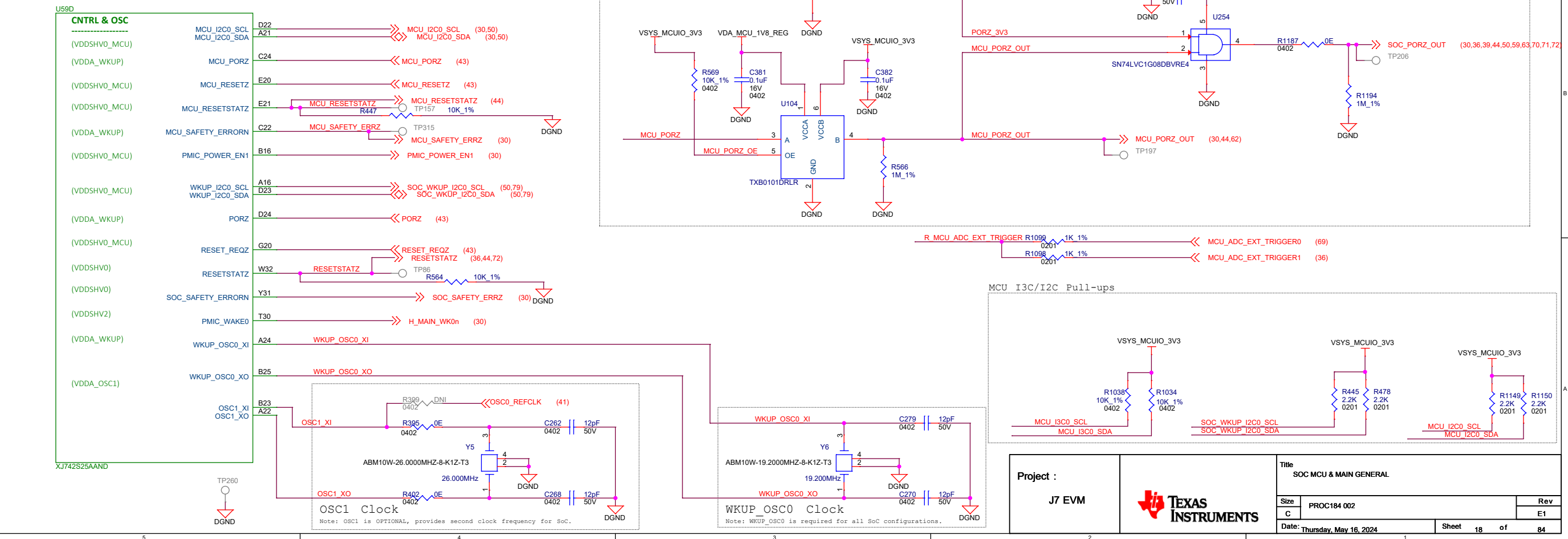
OCTAL NAND



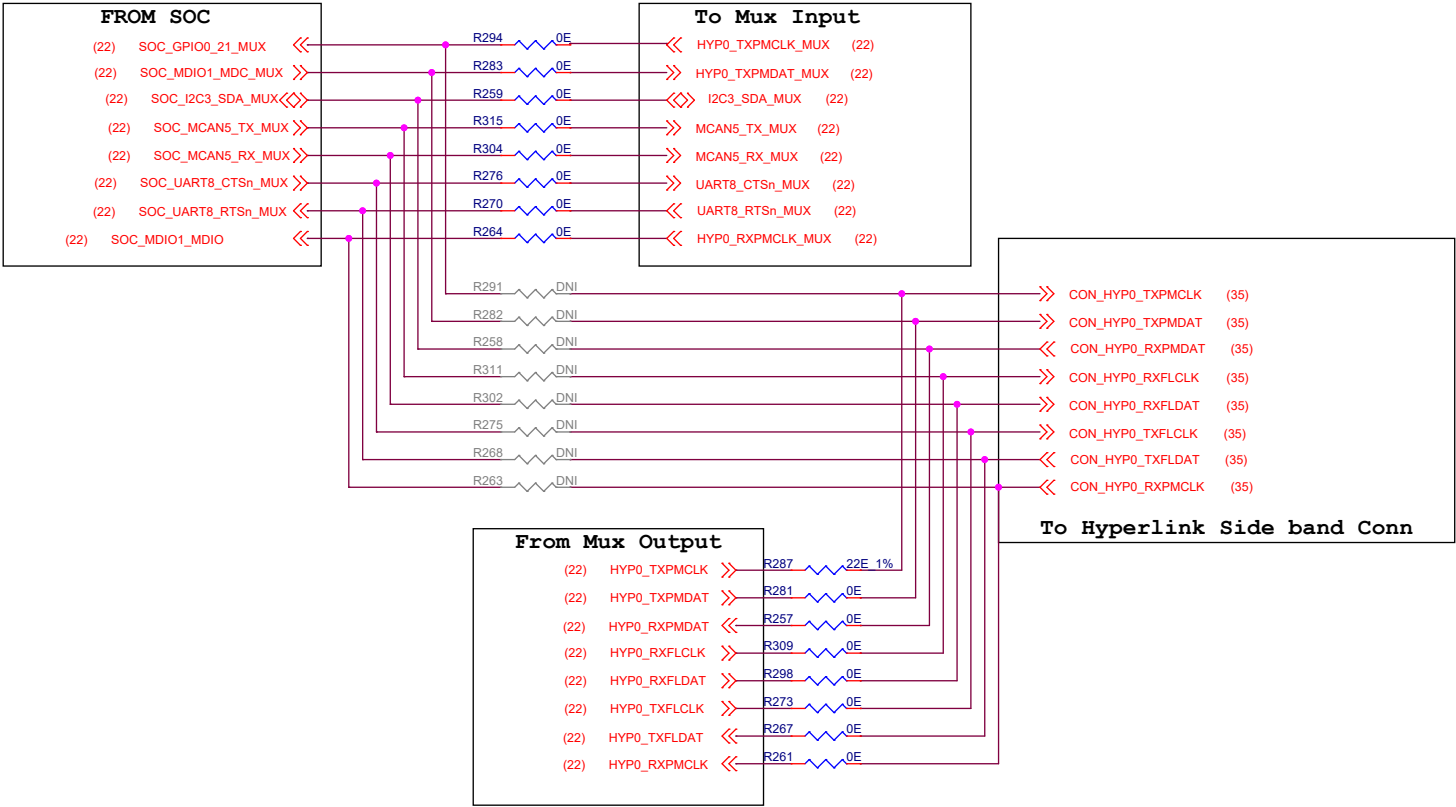
MCU & MAIN GENERAL IO, OSC CLKS



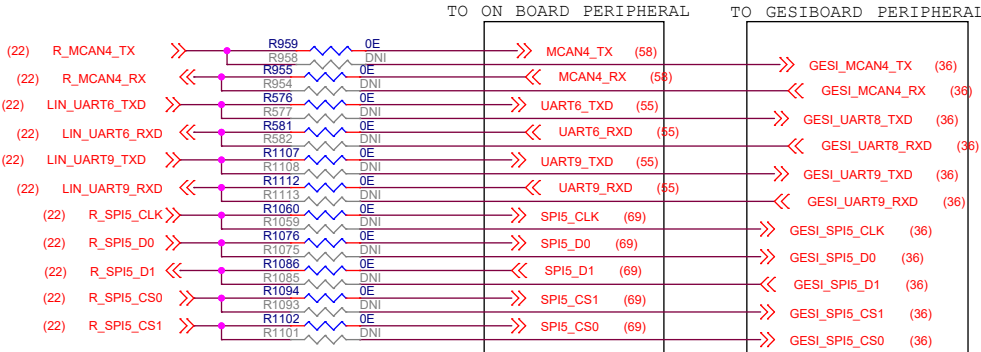
CONTROL & OSC



Resistor Mux option to By-pass MUX for Hyperlink sideband signals



RESISTOR MUX BETWEEN GESI BOARD AND ON BOARD PERIPHERALS



RESISTOR MUX BETWEEN ON BOARD RGMII AND GESI RMII



Project :

J7 EVM



Title
GENERAL IO

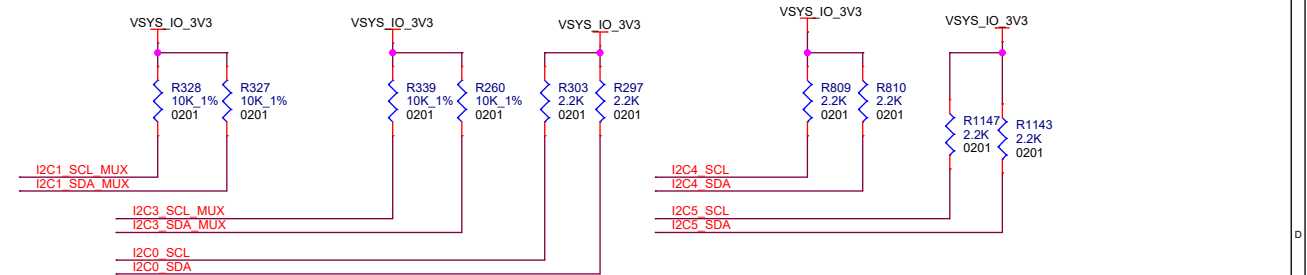
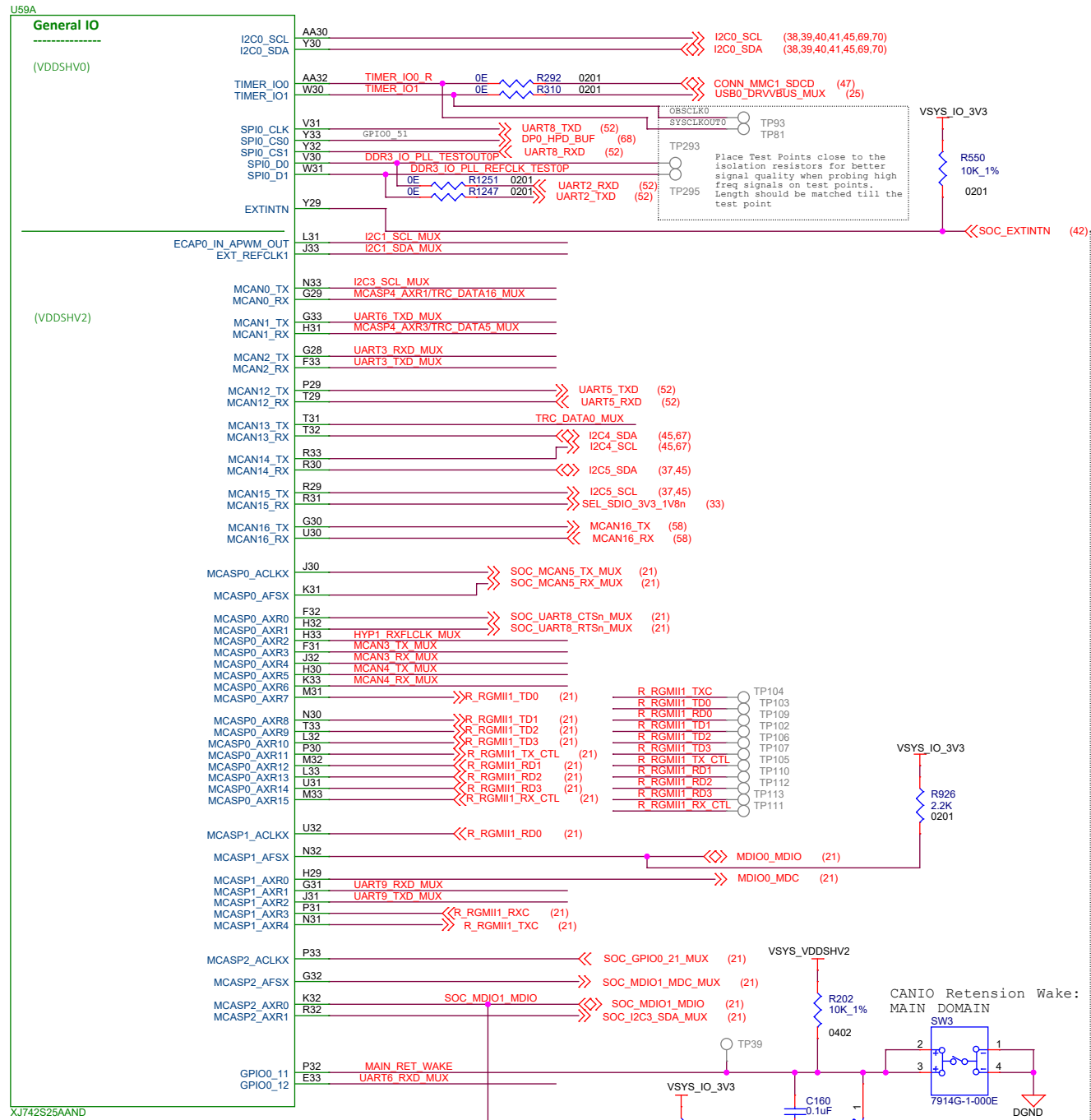
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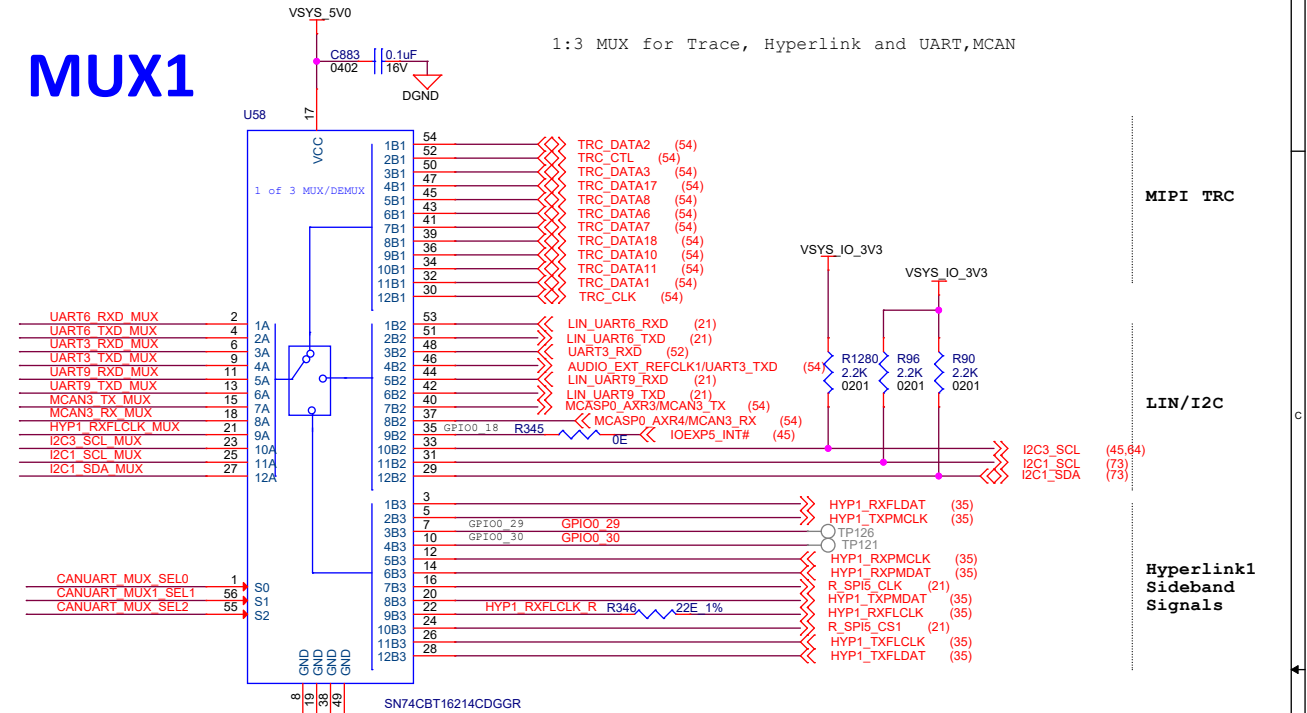
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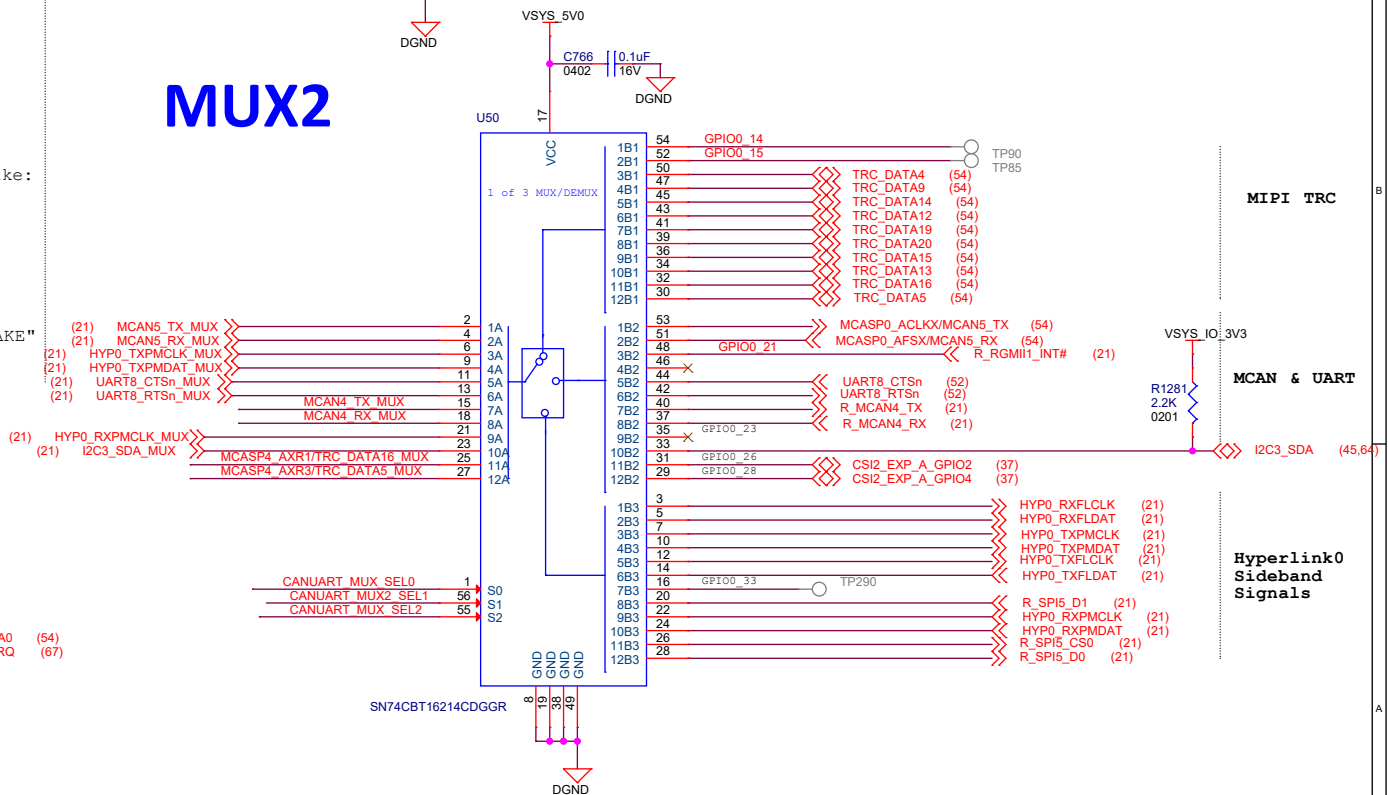
GENERAL IO



MUX1



MUX2

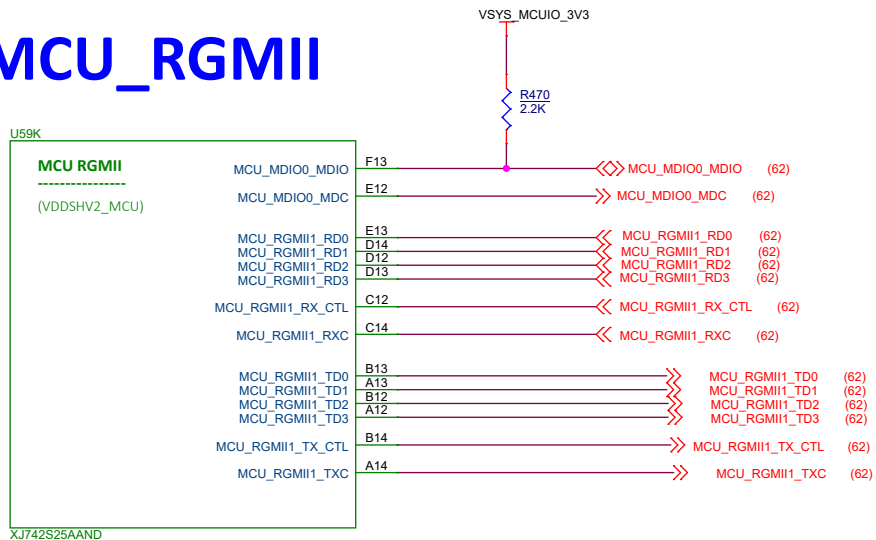


HYPERLINK/TRACE/MCAN/LIN - 1:3 MUX : Truth Table

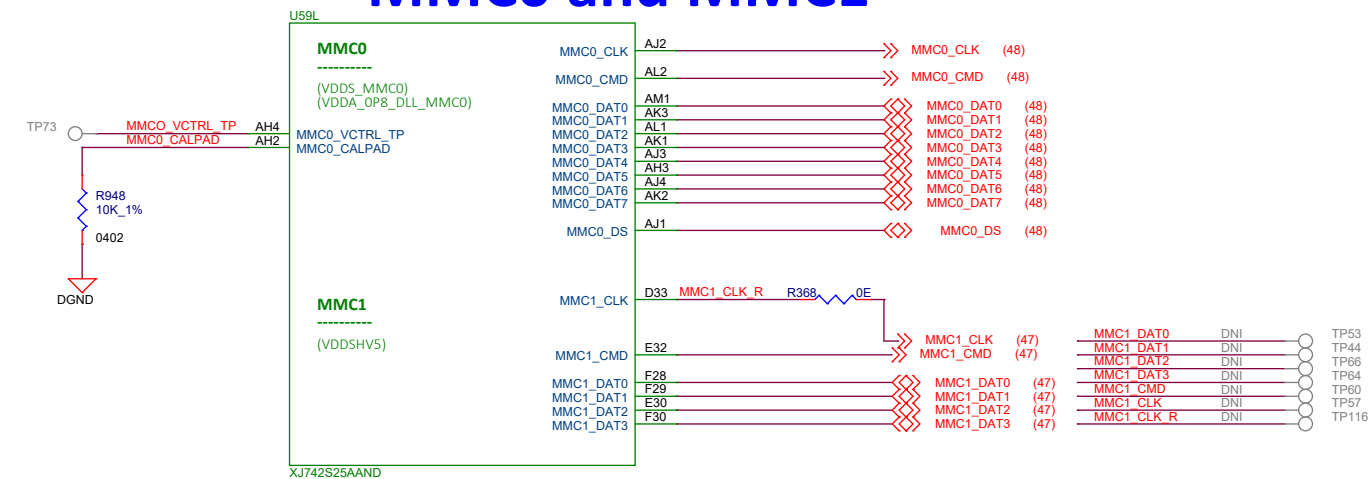
MUX_SEL2	MUX_SEL1	MUX_SEL0	FUNCTION
HIGH	HIGH	LOW	A port = B1 port
HIGH	HIGH	HIGH	A port = B2 port
HIGH	LOW	HIGH	A port = B3 port

(default)

MCU_RGMII



MMC0 and MMC1

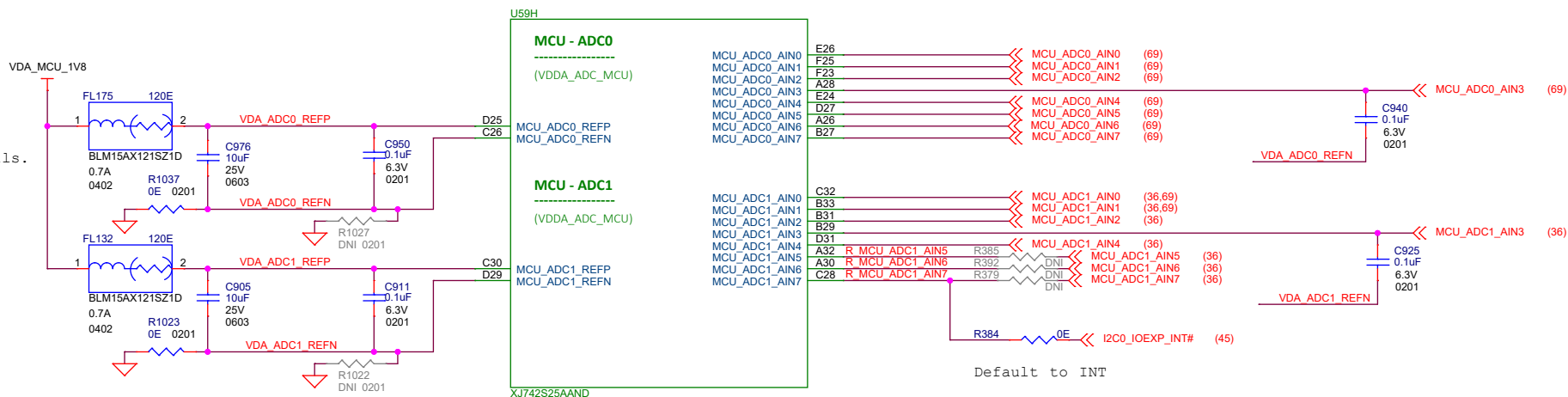


MCU_ADC

Place Beads, 0402 Cs & 0E Rs outside SoC at FP edge
BOM = Install 0E Rs as default

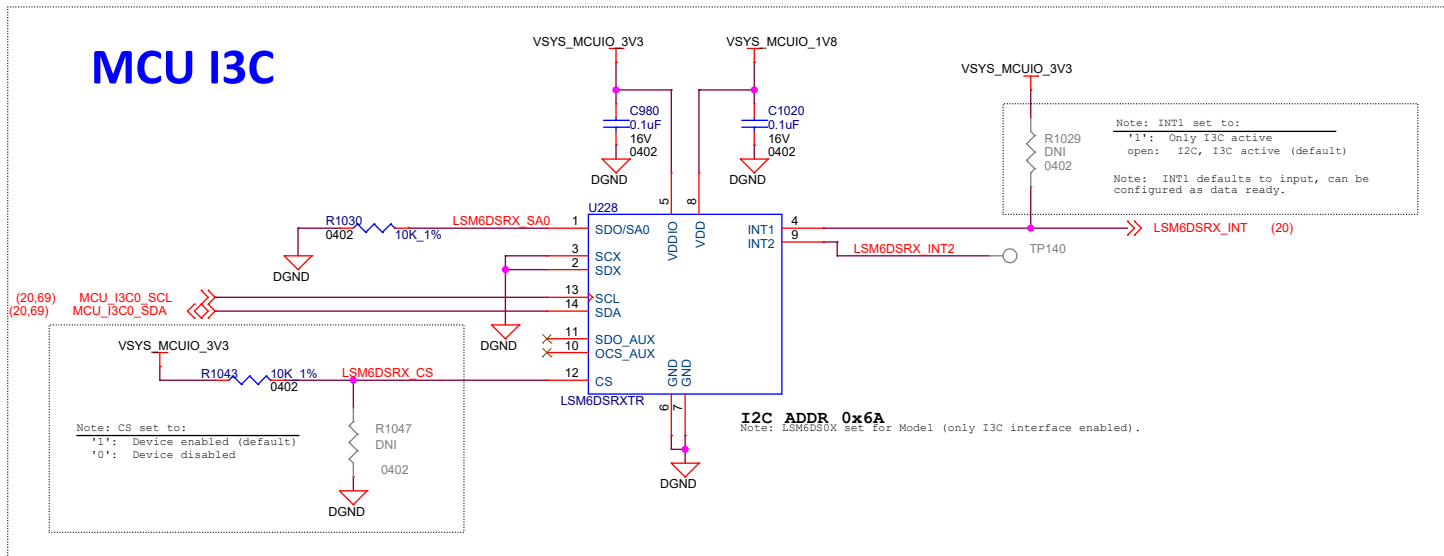
Place 0.1uF Cs across bkout vias & 0E Rs next to Dcaps under SoC
BOM = DNI for 0E Rs (testing option)

ADC 0 & 1 Filtering Scheme:
ADC0/1 VREF_P have 2x independent input balls with same in-line supply filtering as common VDA ADC1V8 pwr rail supplying VDDA_ADC0/1 balls.
(Provisioned supply filtering for PCB layout pending fdbk from TI analog design team.)
-1x Ferrite bead to filter & reduce noise
-1x 0402 (2.2-10uF), SoC perimeter/near end
-1x 0201 for 0.1uF per pwr ball, far end
-1x 0201 0E R to optional short REFN to board GND (as area under SoC allows)



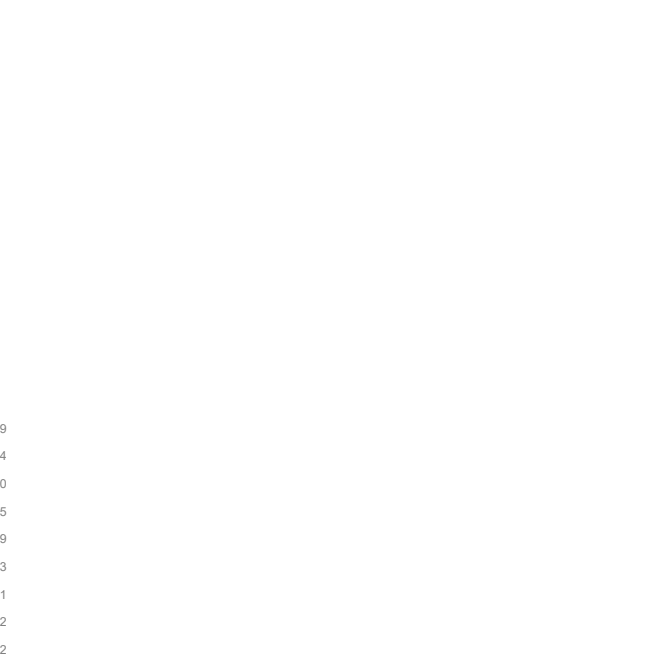
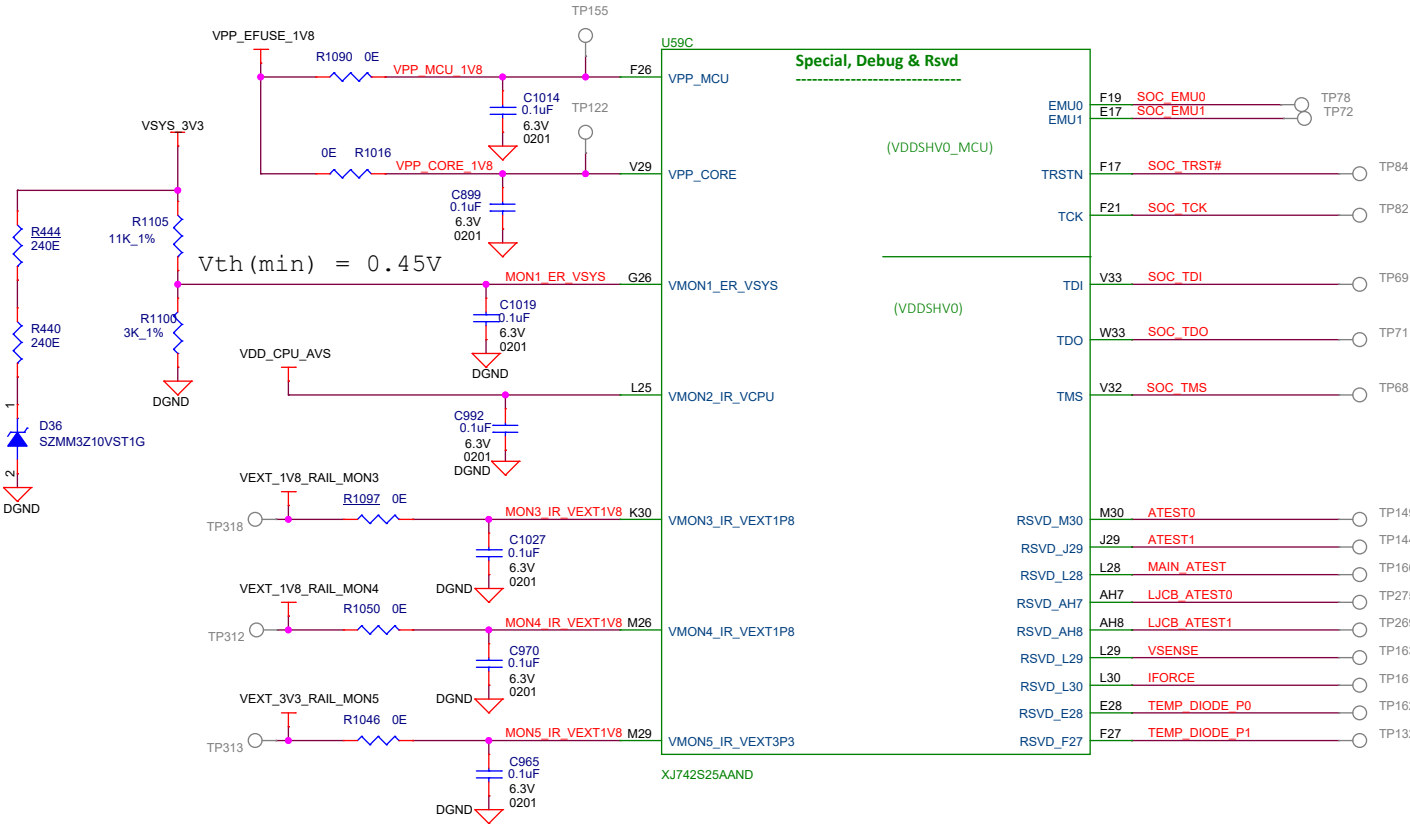
Place 0.1uF Cs across AINx to VREFN nets as close to breakout vias as possible.
BOM = DNI for 0E Rs (testing option)

MCU_I3C

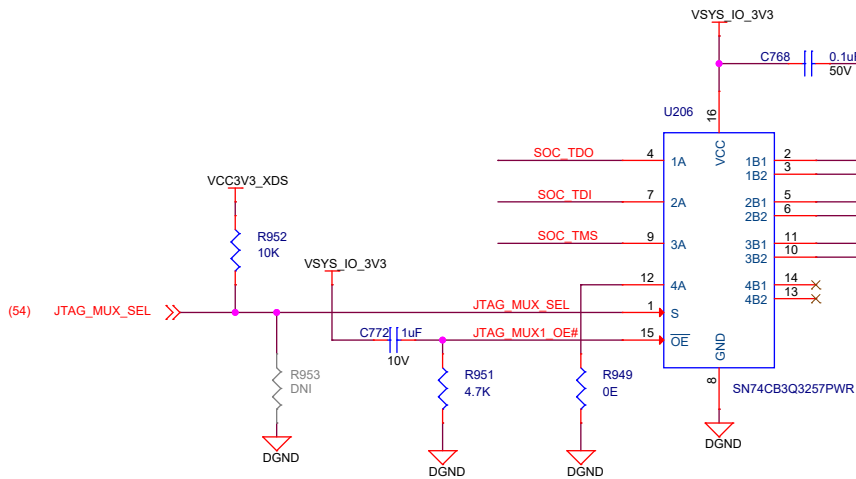


SPECIAL, DEBUG & RSVD

If monitoring VSYS_3V3, protect SoC from 1st stage fault. Alternatively, monitoring protected VCCA_3V3 requires no Zener diode.



JTAG AND TRACE MUX

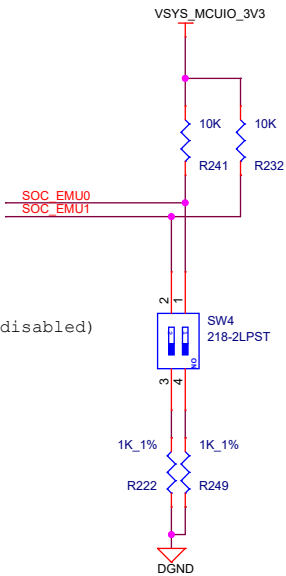


JTAG - 1:2 MUX : Truth Table

MUX_SEL	CONDITION	FUNCTION
LOW	External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]
HIGH	No External Emulator attached & XDS110 Powered via USB	A-->B2 port [ON Board EMU]
LOW	External Emulator attached & XDS110 Powered via USB	A-->B1 port [EXTERNAL EMU]
LOW	No External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]

(default)

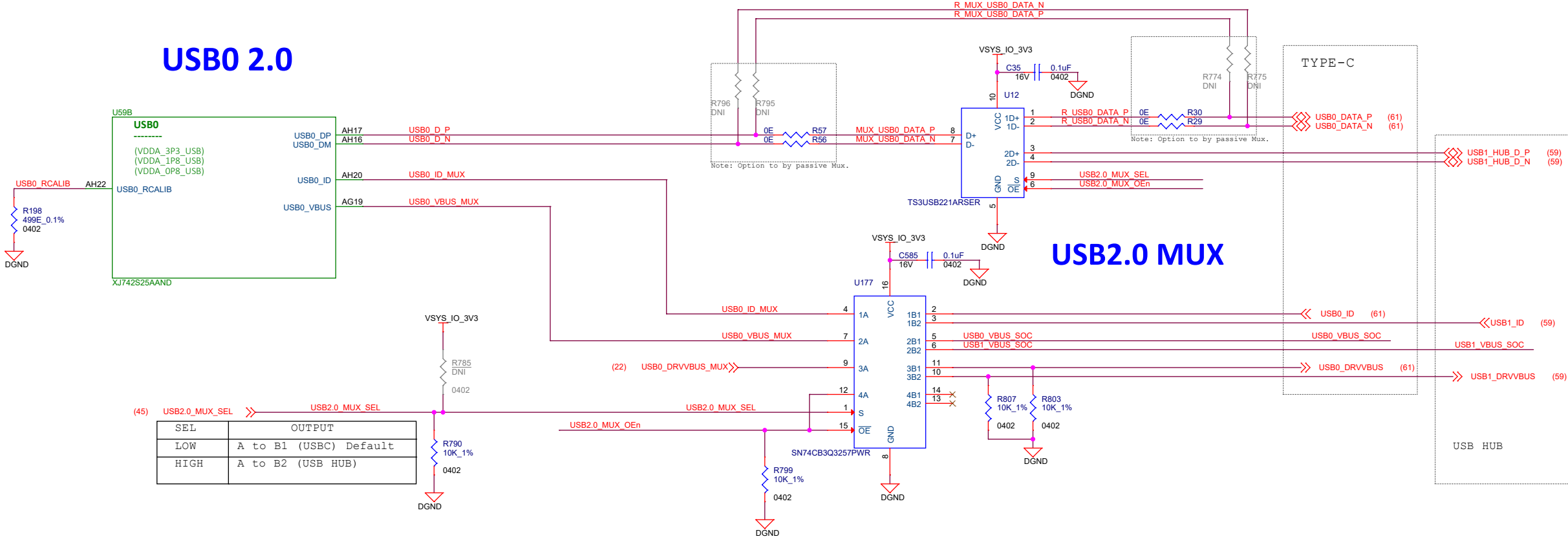
NOTE:SW4.1&2-OFF
(Default wait-in-reset disabled)



USB0 2.0

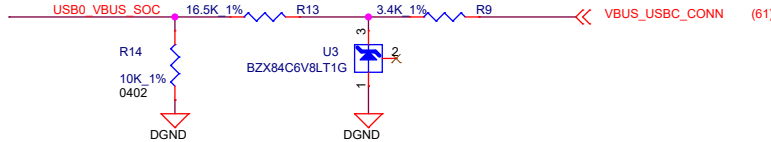
By Pass USB MUX	Mount - R796,R795,R774,R775 DNI -R57,R56,R30,R29
USB MUX (Default)	Mount -R57,R56,R30,R29 DNI - R796,R795,R774,R775

USB0 2.0

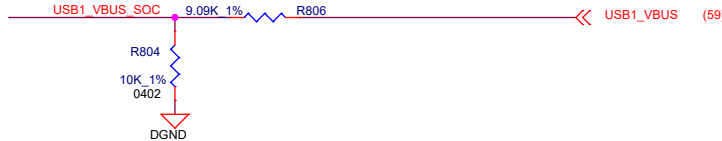


USB VBUS Resistor divider circuit

Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS



Note: Recommended VBUS circuit for embedded Hub



Project :

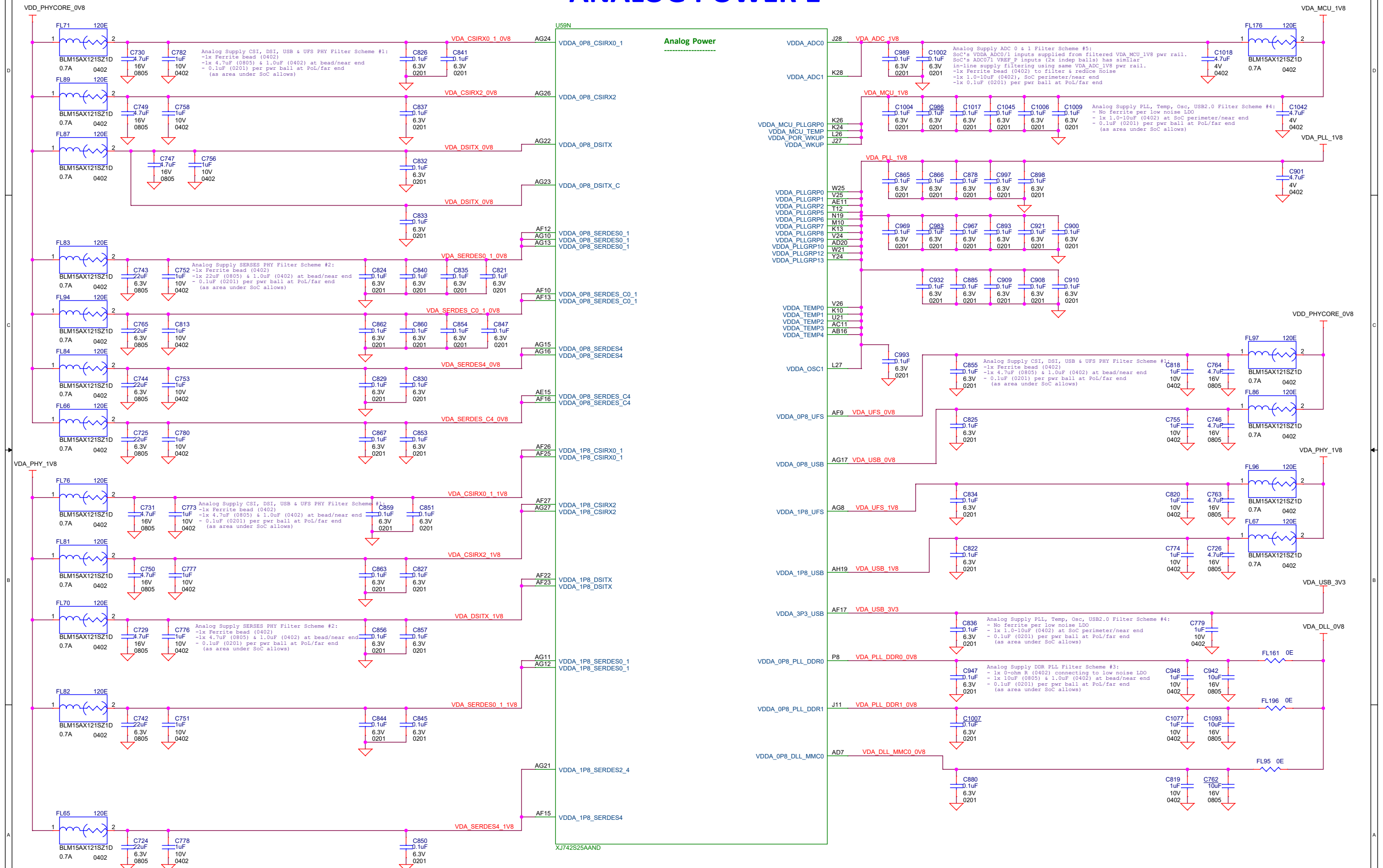
J7 EVM



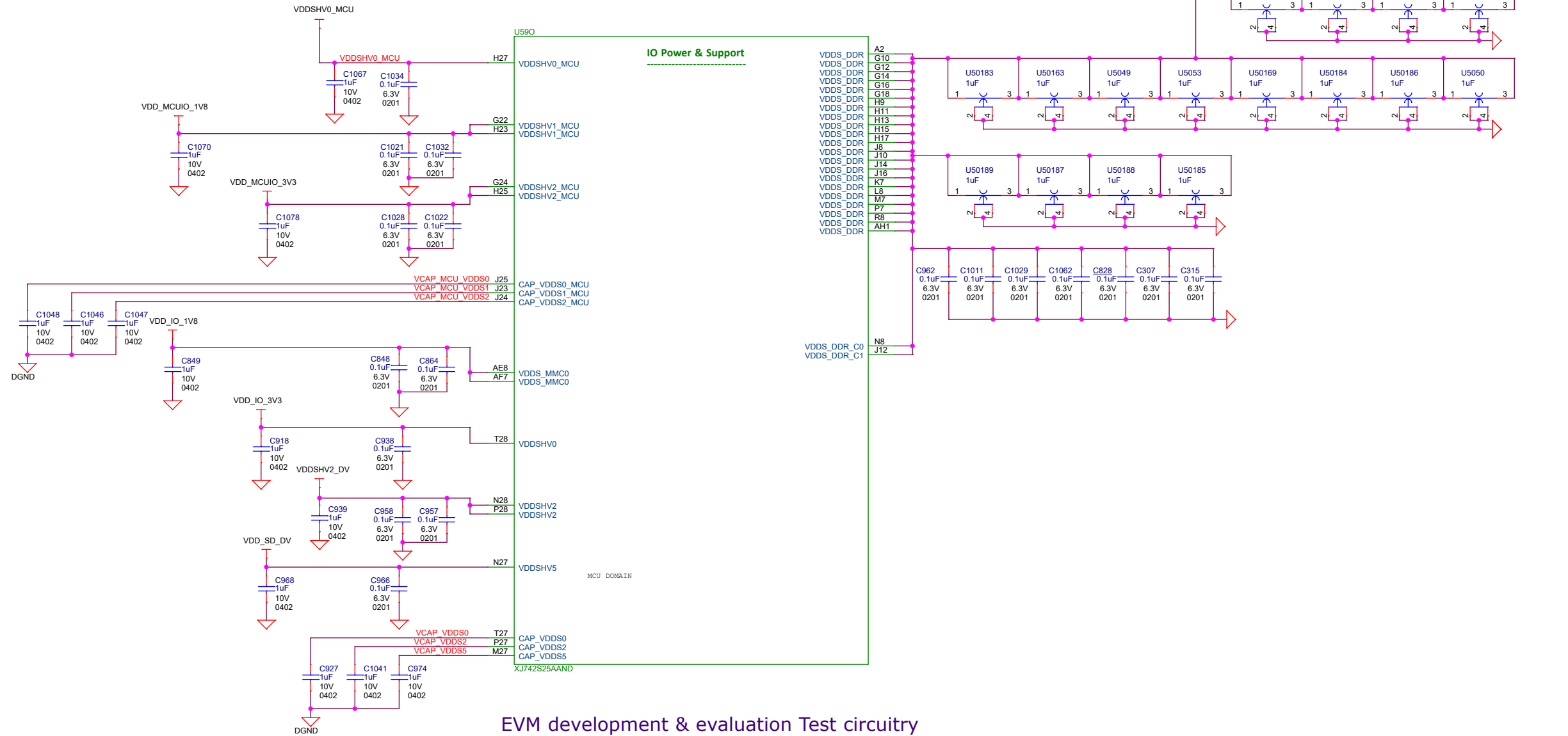
Title	SOC USB 2.0
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Size	PROC184 002	Rev
C		E1
Date:	Thursday, May 16, 2024	Sheet 23 of 84

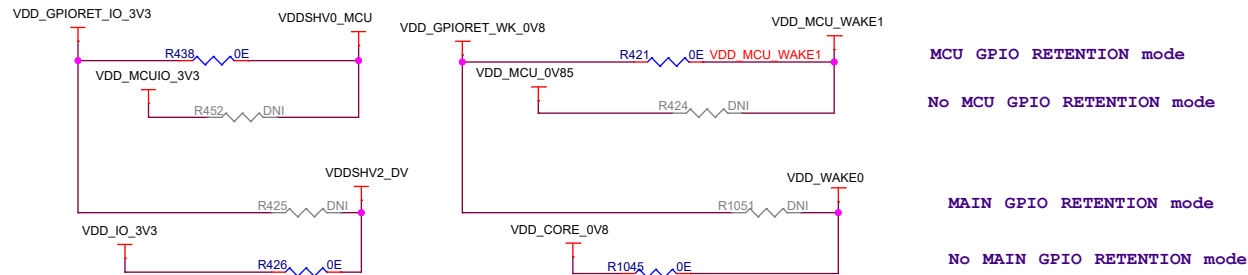
ANALOG POWER 1



IO POWER 2



EVM development & evaluation Test circuitry
EVM GPIO Retention testing option
(TI EVM Only)




Note:
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.
Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Low power modes	Resistors to be Populated	Resistors to be DNI'd
No GPIO RET	R452, R424, R426, R1045	R438, R421, R425, R1051
MCU GPIO RET only	R438, R421, R426, R1045	R452, R424, R425, R1051
MAIN GPIO RET only	R452, R424, R425, R1051	R438, R421, R426, R1045
MCU & MAIN GPIO RET	R438, R421, R425, R1051	R452, R424, R426, R1045

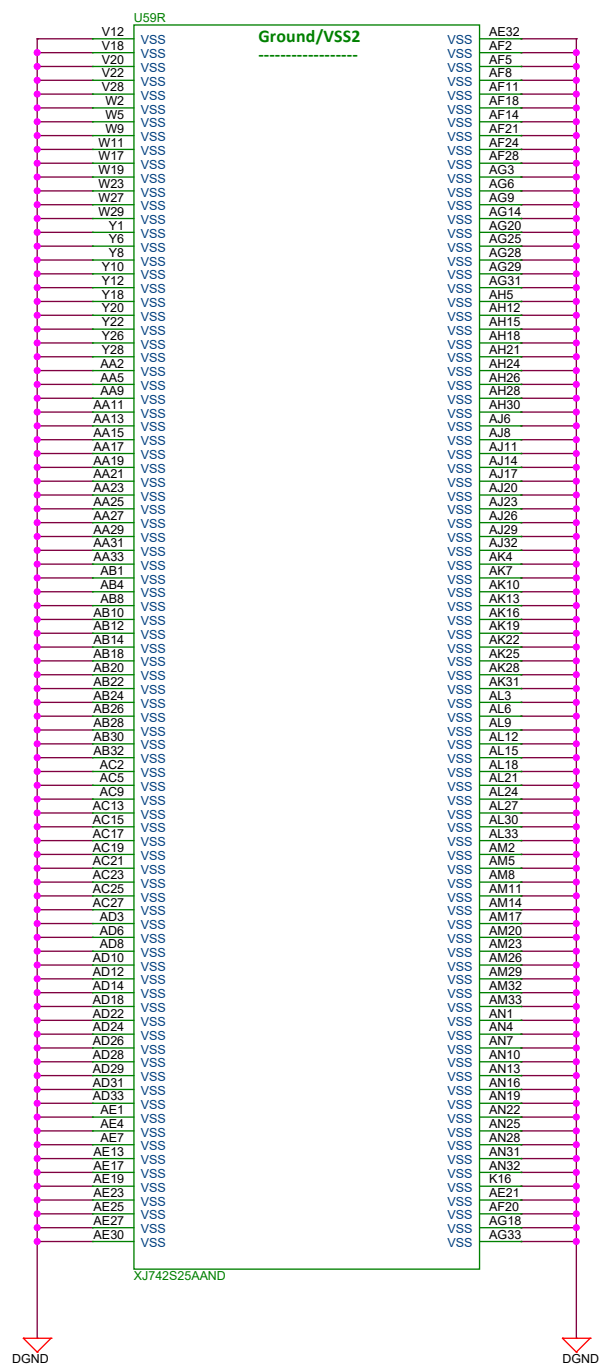
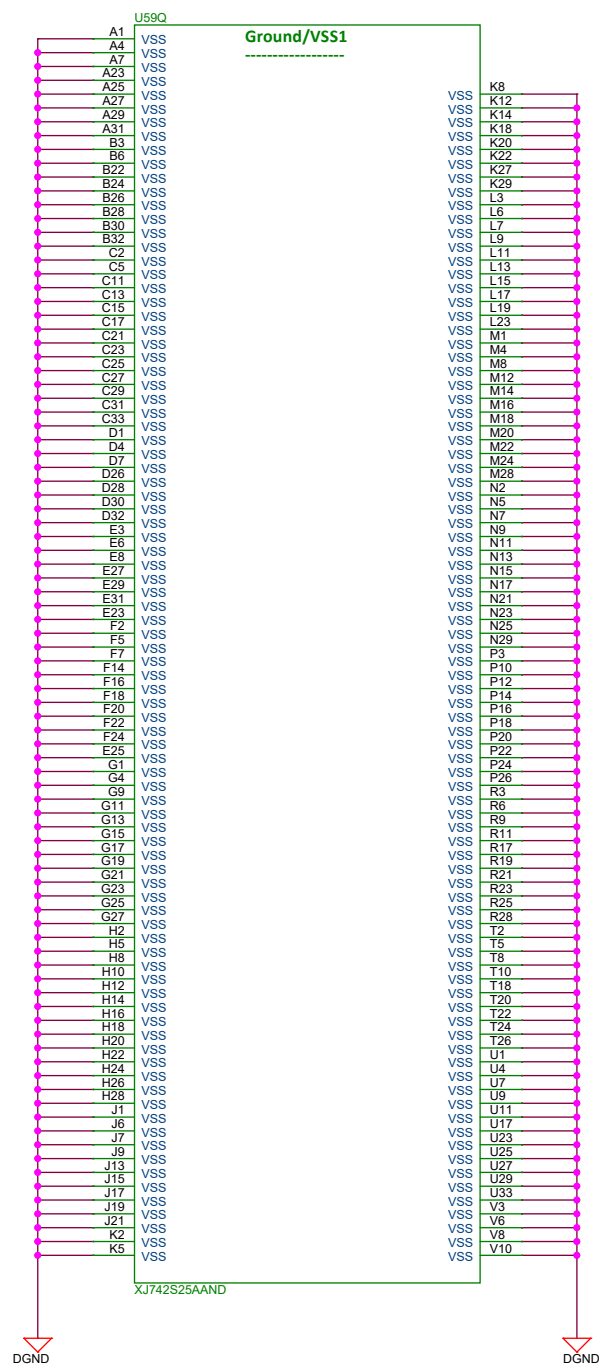
Digital Power



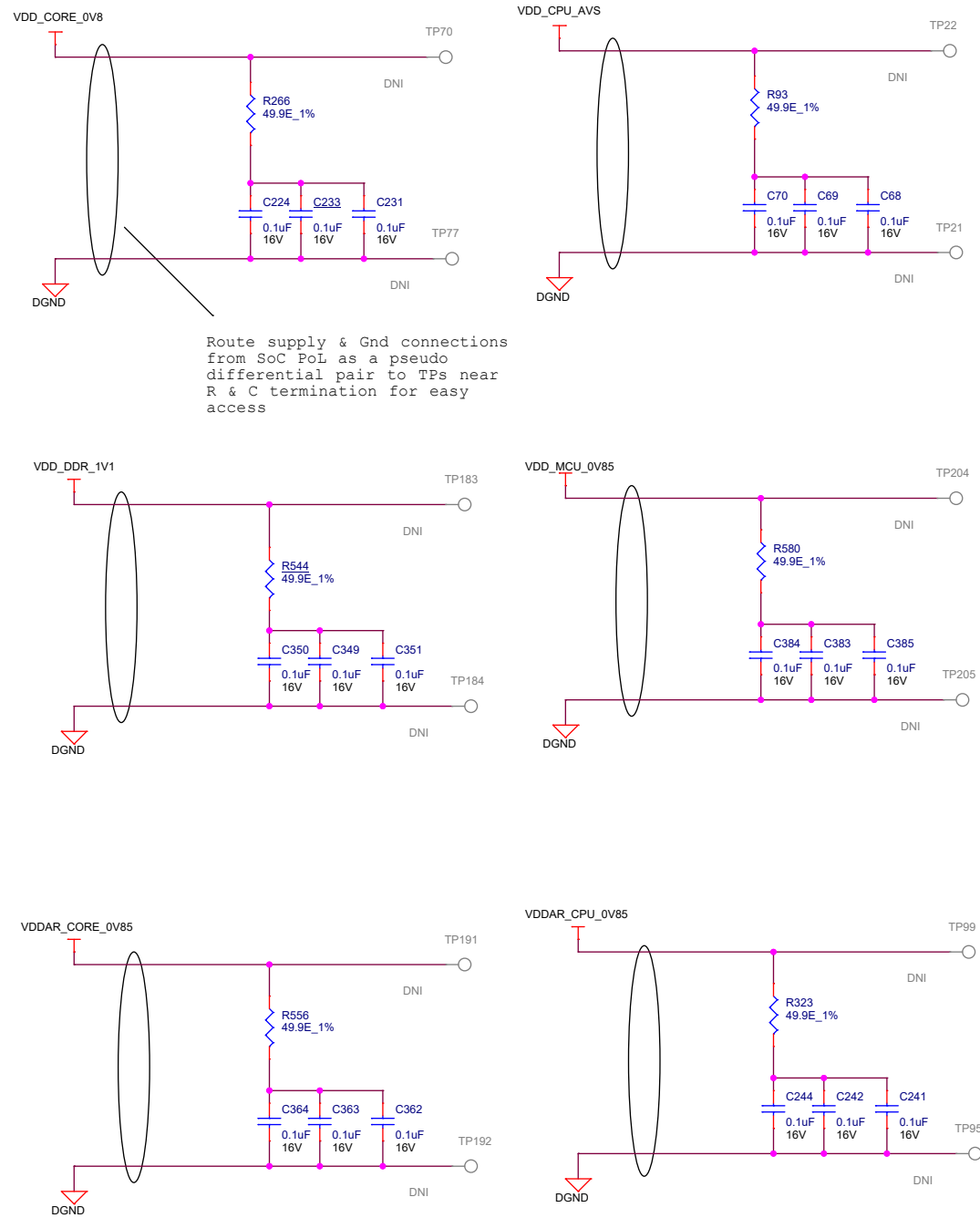
Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Project : J7 EVM		Title SOC DIGITAL POWER 3		
		Size	PROC184 002	Rev
		C		E1
		Date:	Thursday, May 16, 2024	Sheet 26 of 84

SOC GROUND



SoC Supply Noise Kelvin Sensing



PMIC

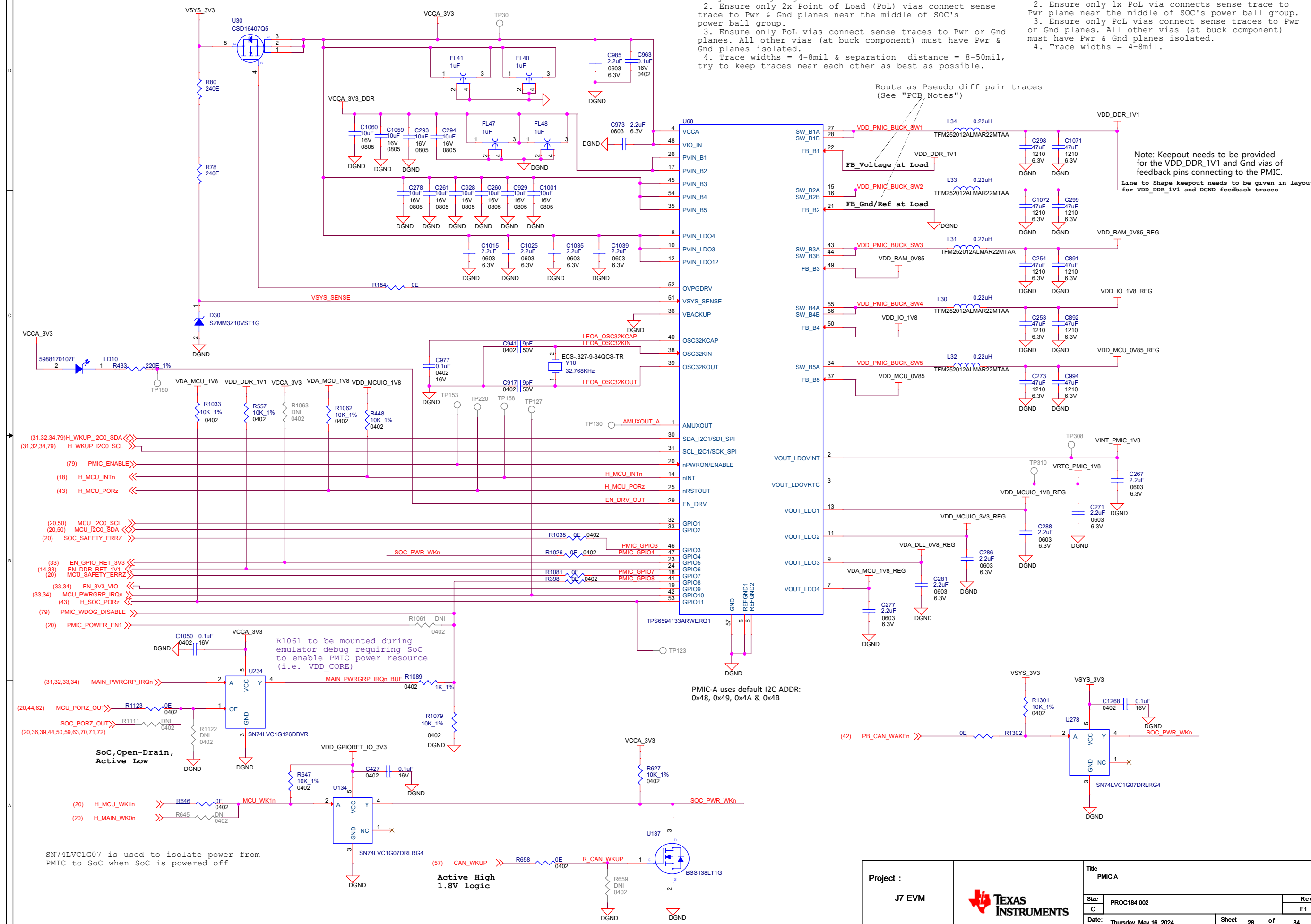
"PCB Notes":


For multi-phase Buck converter configs, route remote sense feedback as follows:

1. Use pseudo differential pair traces on same layer & net to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Ensure only 2x Point of Load (PoL) vias connect sense trace to Pwr & Gnd planes near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
4. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible.

For single-phase Buck converter configs,
route remote sense feedback as follows:

1. Use single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Ensure only 1x PoL via connects sense trace to Pwr plane near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
4. Trace widths = 4-8mil.



Project : J7 EVM		Title PMIC A			
		Size	PROC184 002		Rev
		C			E1
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VDD_CPU_AVS High-Current Power Stage A (HCPS-A)

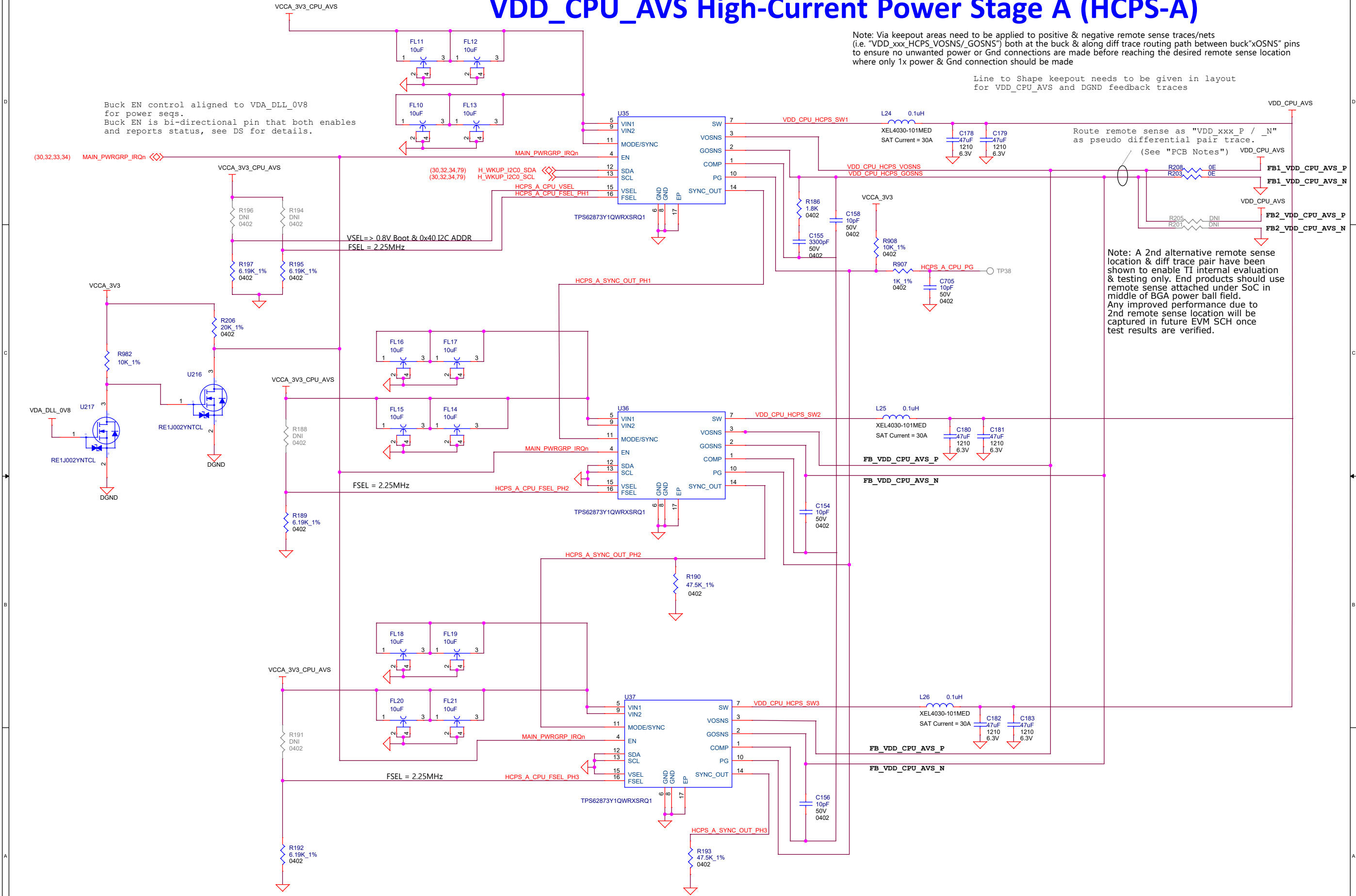
Note: Via keepout areas need to be applied to positive & negative remote sense traces/nets (i.e. "VDD_xxx_HCPS_VOSNS/_GOSNS") both at the buck & along diff trace routing path between buck"xOSNS" pins to ensure no unwanted power or Gnd connections are made before reaching the desired remote sense location where only 1x power & Gnd connection should be made

Line to Shape keepout needs to be given in layout for VDD_CPU_AVS and DGND feedback traces

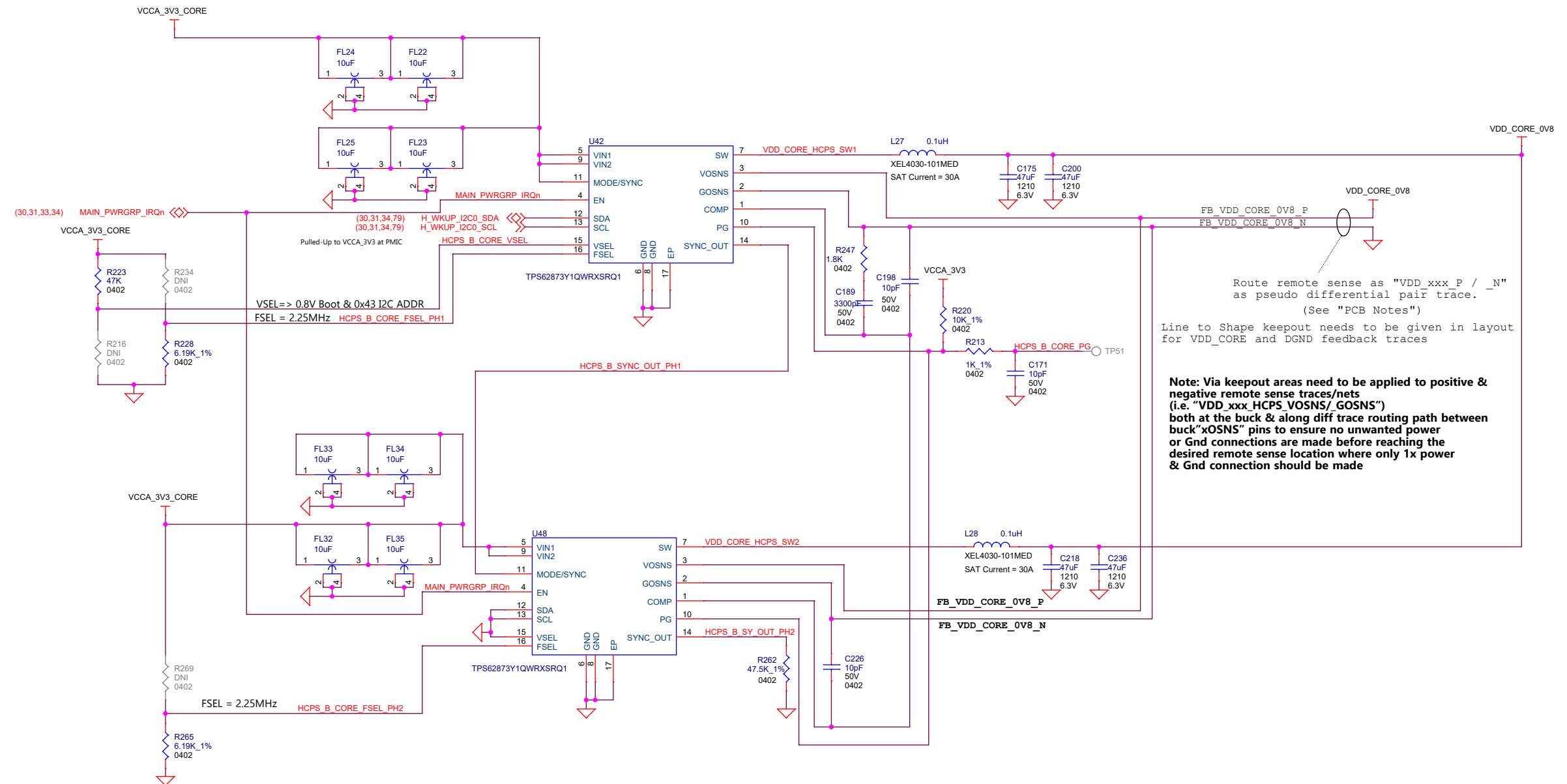
Buck EN control aligned to VDA_DLL_0V8 for power seqs.
Buck EN is bi-directional pin that both enables and reports status, see DS for details.

Route remote sense as "VDD_xxx_P / _N" as pseudo differential pair trace.
(See "PCB Notes")

Note: A 2nd alternative remote sense location & diff trace pair have been shown to enable TI internal evaluation & testing only. End products should use remote sense attached under SoC in middle of BGA power ball field.
Any improved performance due to 2nd remote sense location will be captured in future EVM SCH once test results are verified.

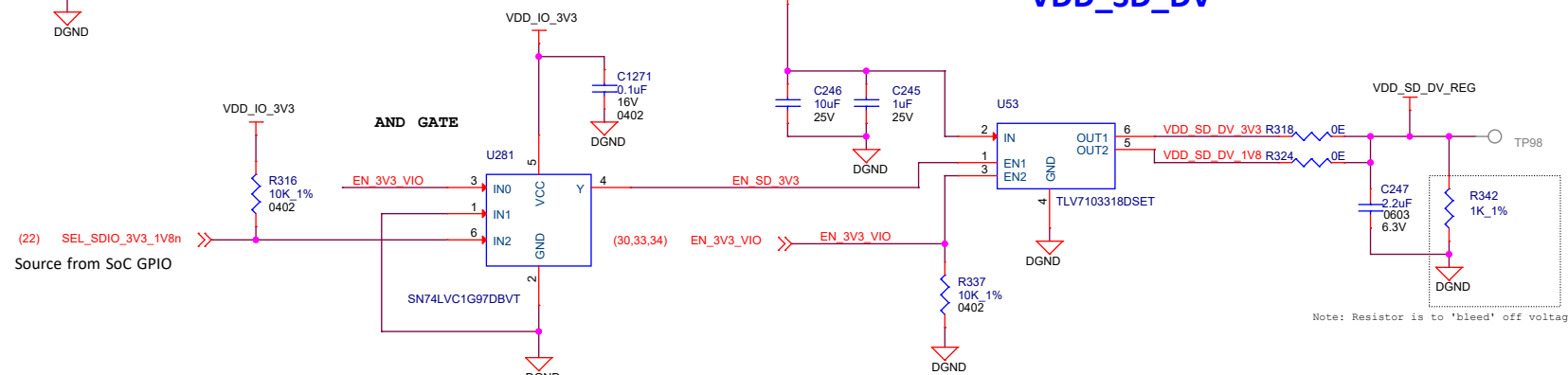
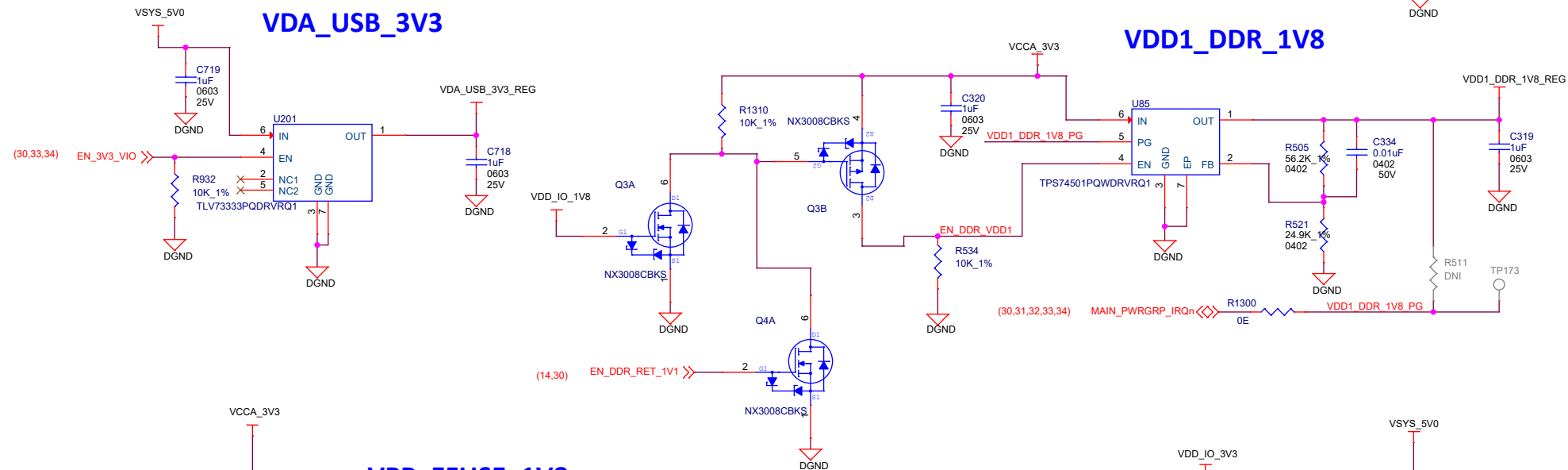
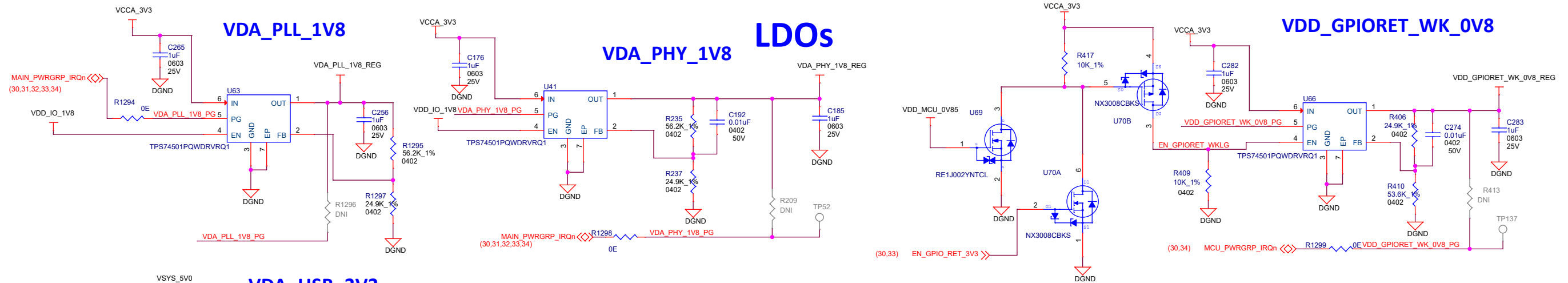
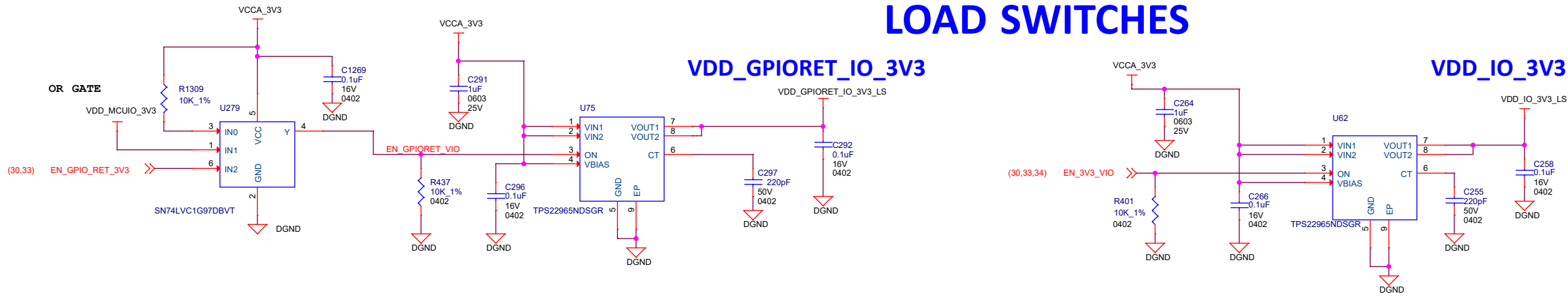


VDD_CORE_0V8 High-Current Power Stage A (HCPS-B)



Note: Via keepout areas need to be applied to positive & negative remote sense traces/nets (i.e. "VDD_XXX_HPCS_VOSNS"/_GOSNS") both at the buck & along diff trace routing path between buck"xOSNS" pins to ensure no unwanted power or Gnd connections are made before reaching the desired remote sense location where only 1x power & Gnd connection should be made

LOAD SWITCHES



EN_GPIORET_VIO & EN_GPIORET_WKLG & EN_DDR_VDD1 Truth table

"OR" Gate Logic			States		
X	Y	OUTPUT	Input - X	Input - Y	Output
0	0	0	OFF	OFF	OFF
0	1	1	OFF	ON	ON
1	0	1	ON	OFF	ON
1	1	1	ON	ON	ON

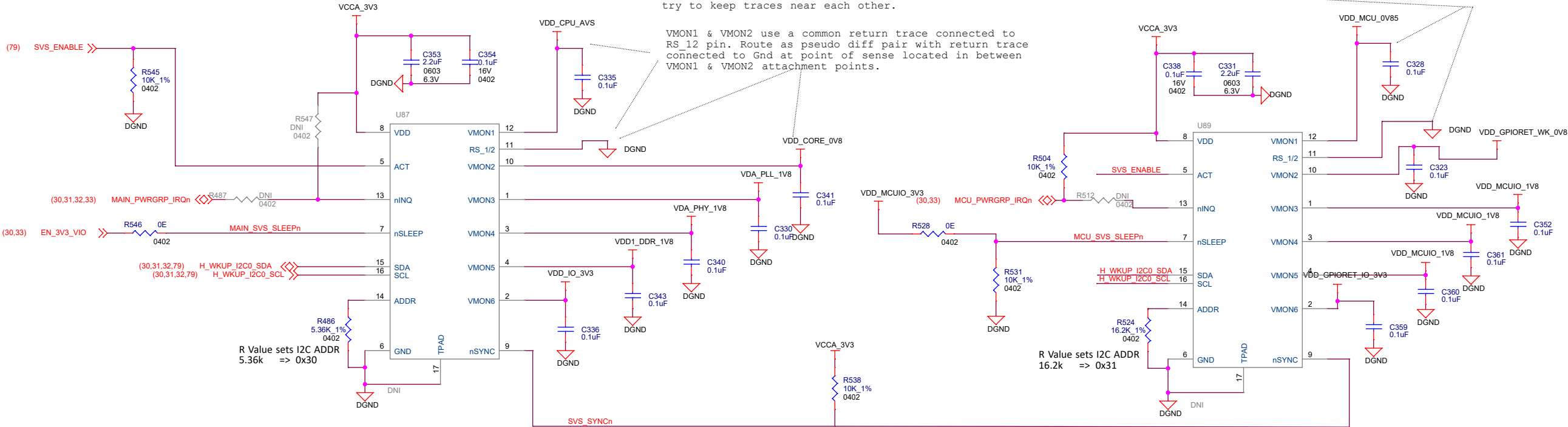
Note: Resistor is to 'bleed' off voltage.

Safety Voltage Supervisors

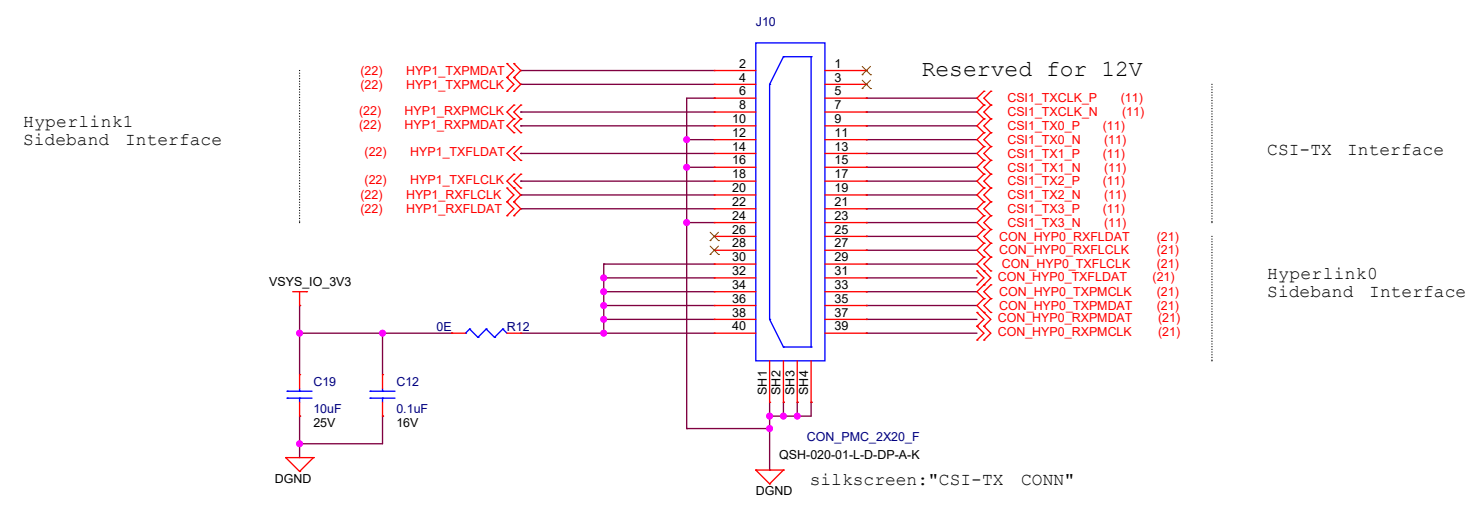
Power rail voltage > 1.0V can connect to VMON3-6 inputs using single-ended traces. Trace widths = 4-8mil, as short as possible & try to avoid routing near HF signals.

Any power rail voltage < 1.0V should connect to VMON1 & VMON2 inputs using "Pseudo Diff Pair Trace" routes. Trace widths = 4-8mil & Separation = 8-50mil, try to keep traces near each other.

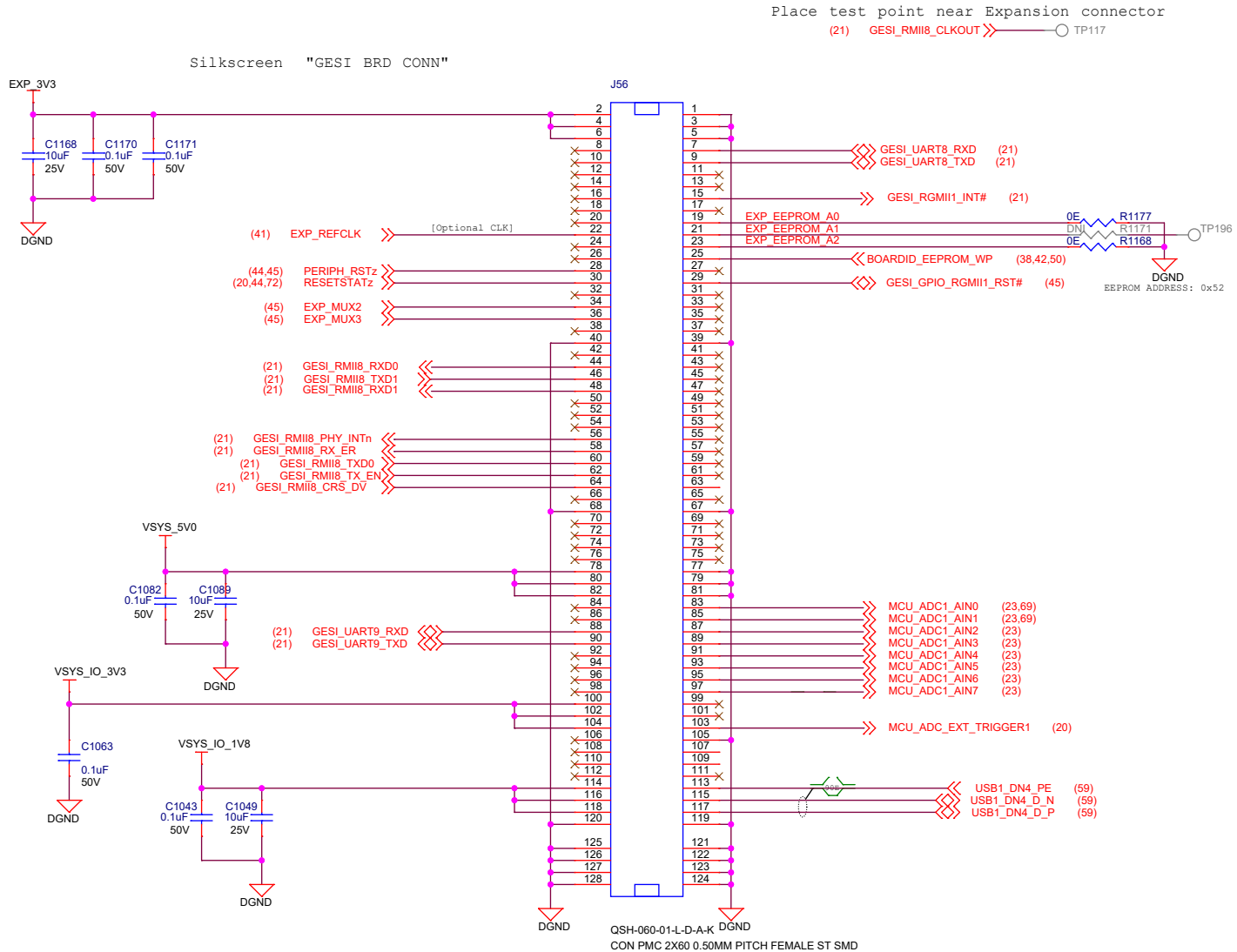
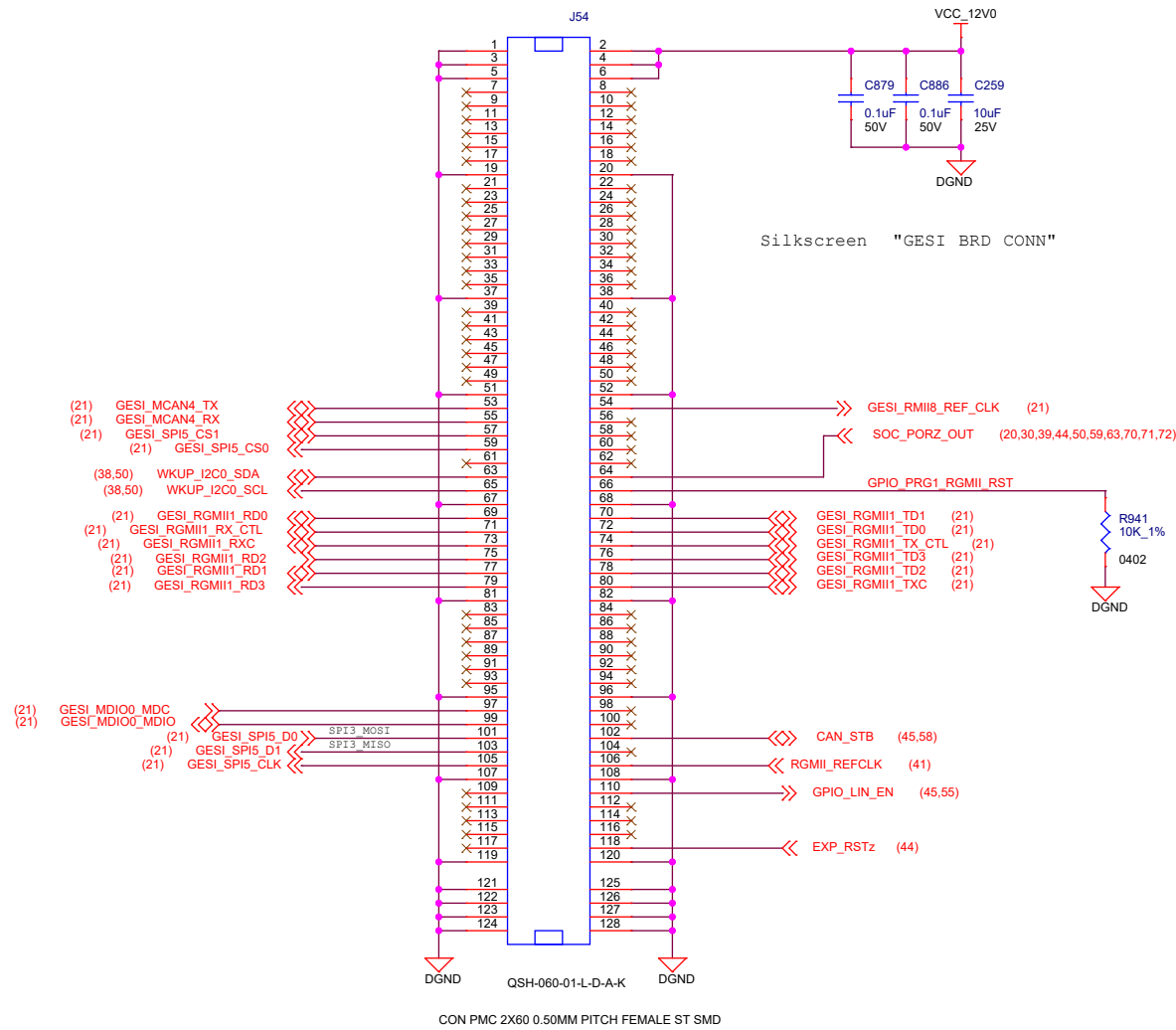
VMON1 & VMON2 use a common return trace connected to RS 12 pin. Route as pseudo diff pair with return trace connected to Gnd at point of sense located in between VMON1 & VMON2 attachment points.



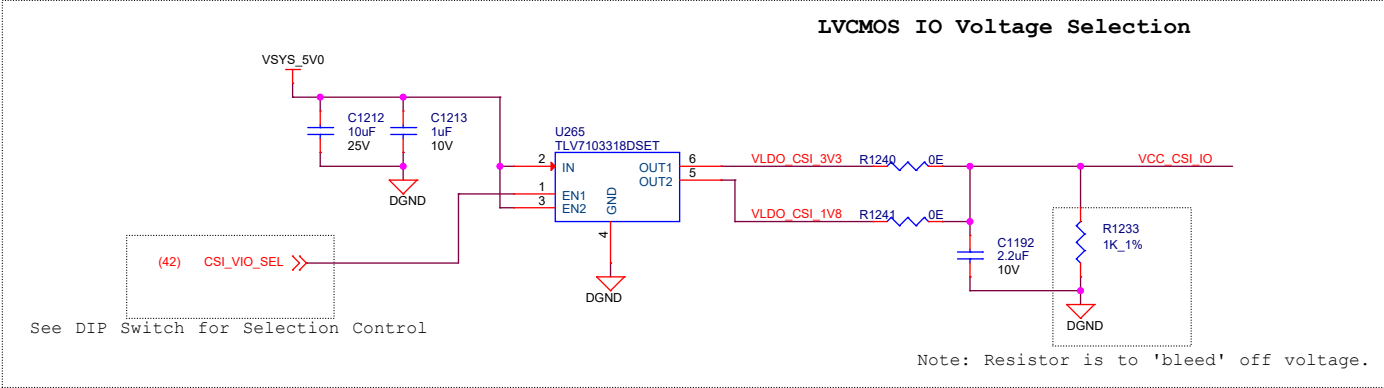
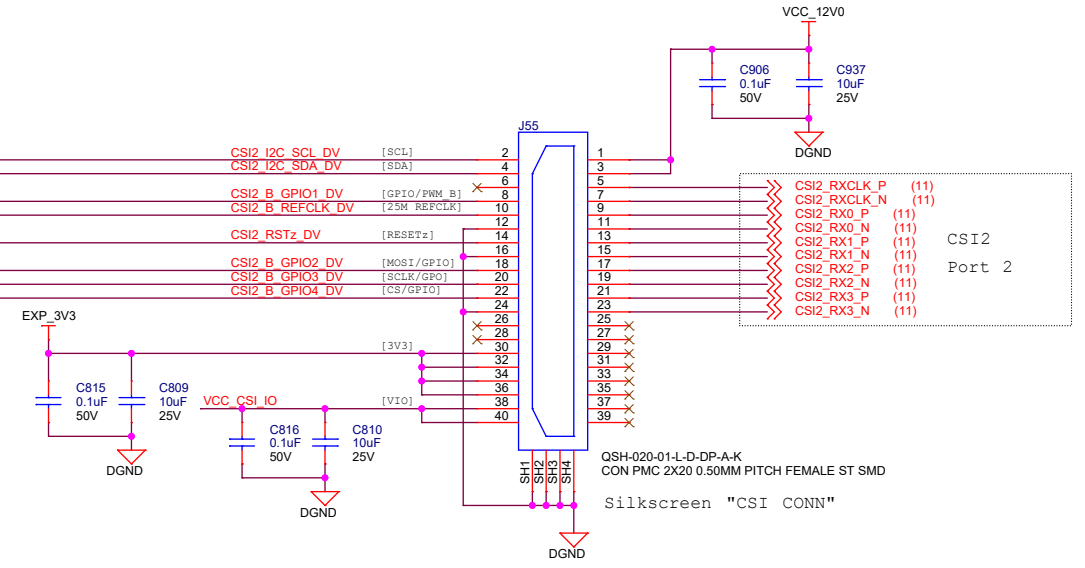
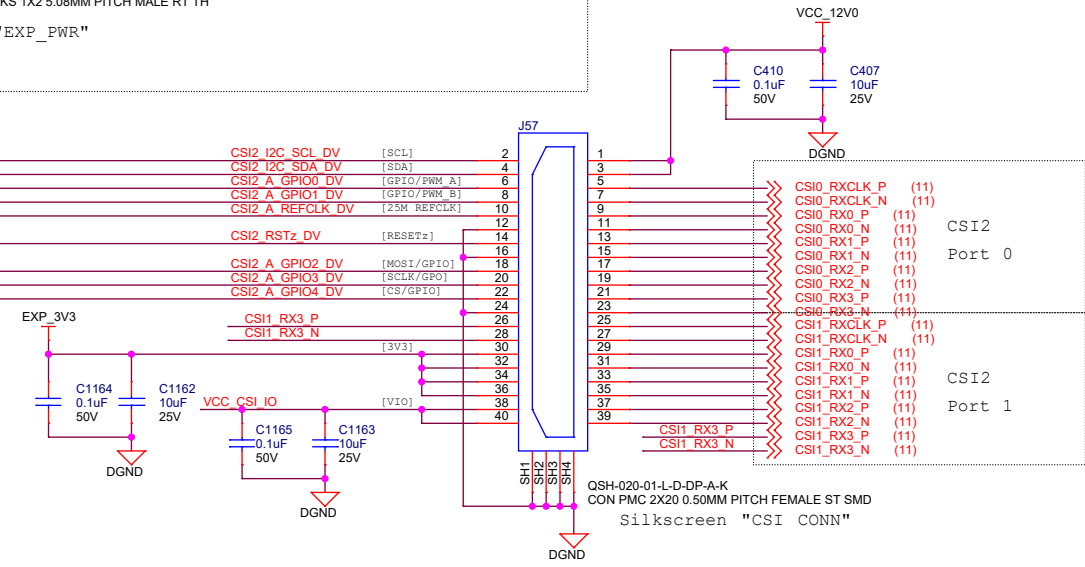
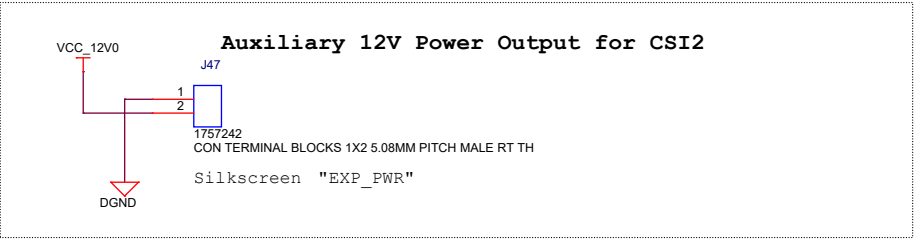
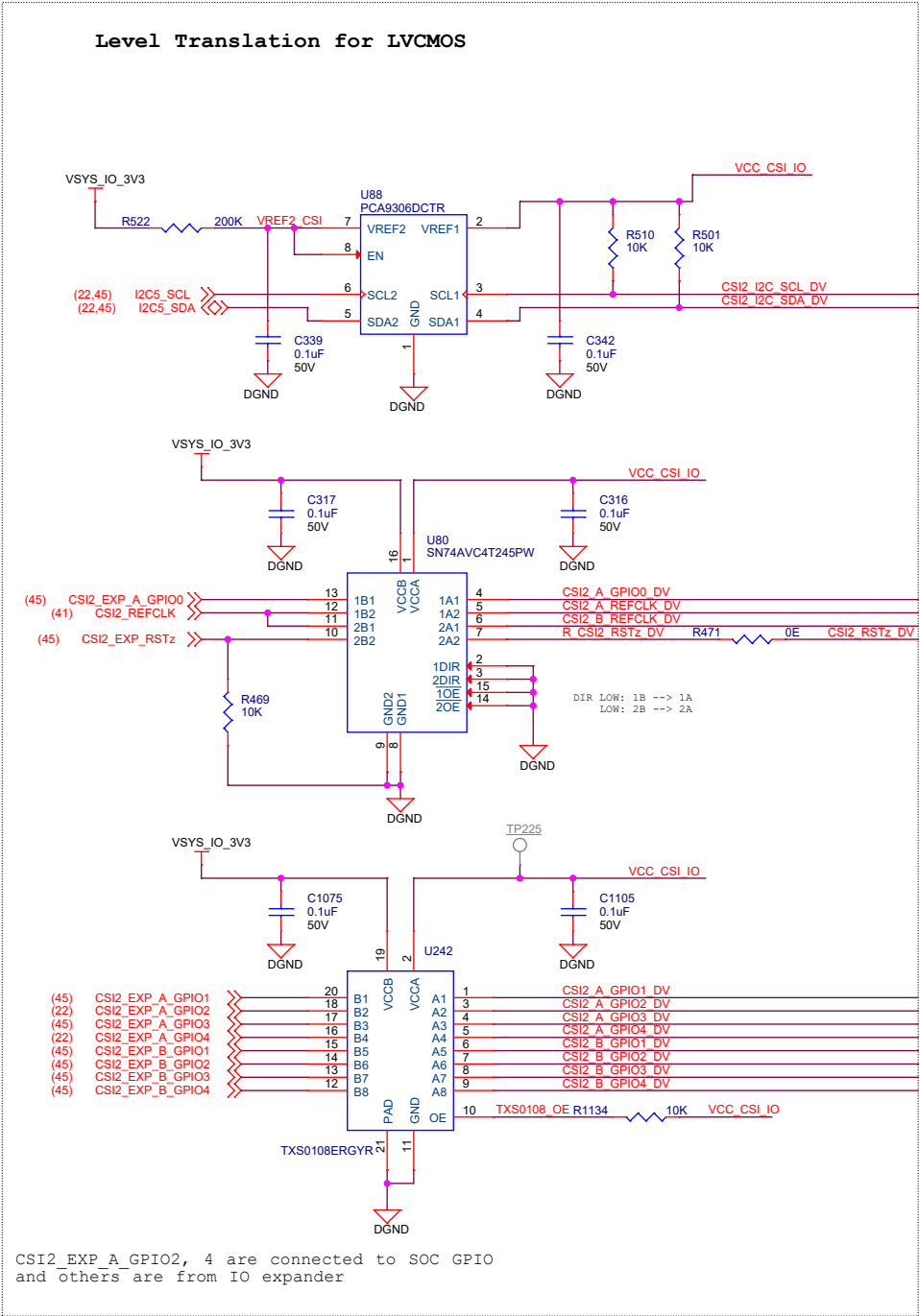
HYPERLINK SIDEBAND CONNECTOR



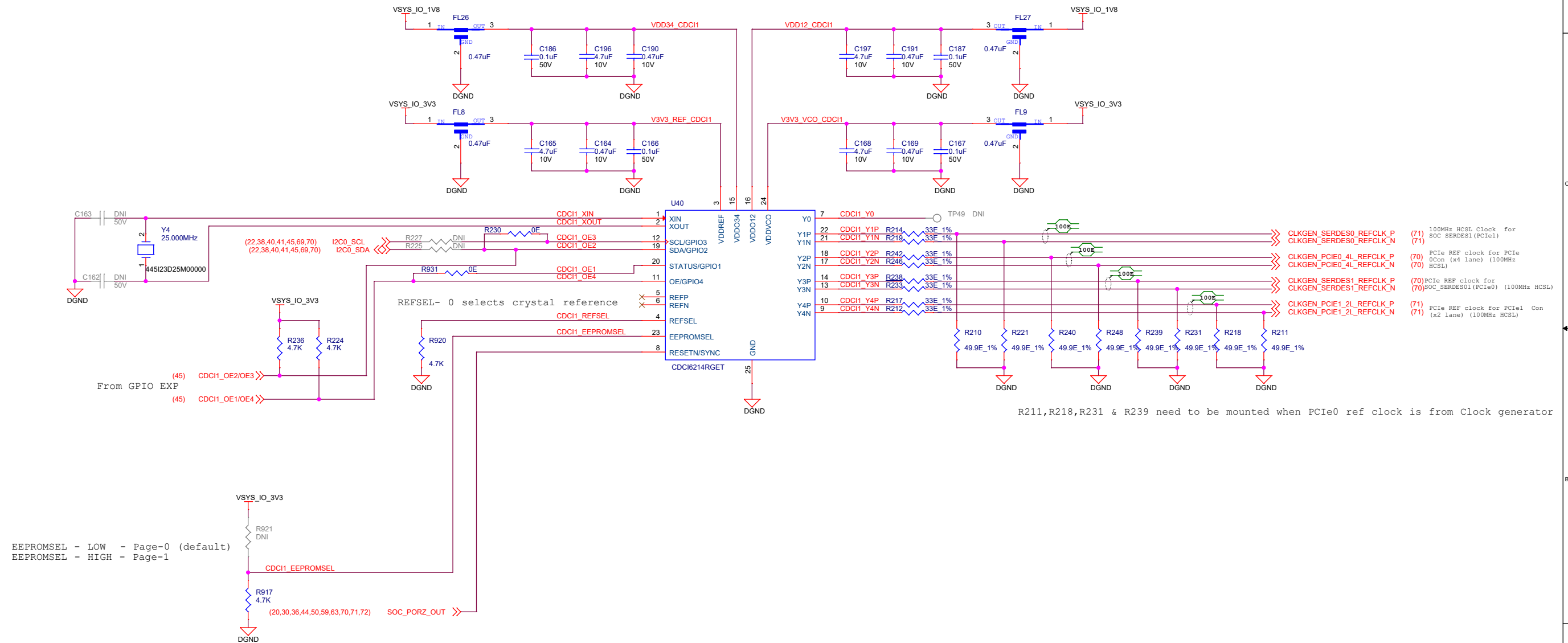
GESI_EXP_CONN



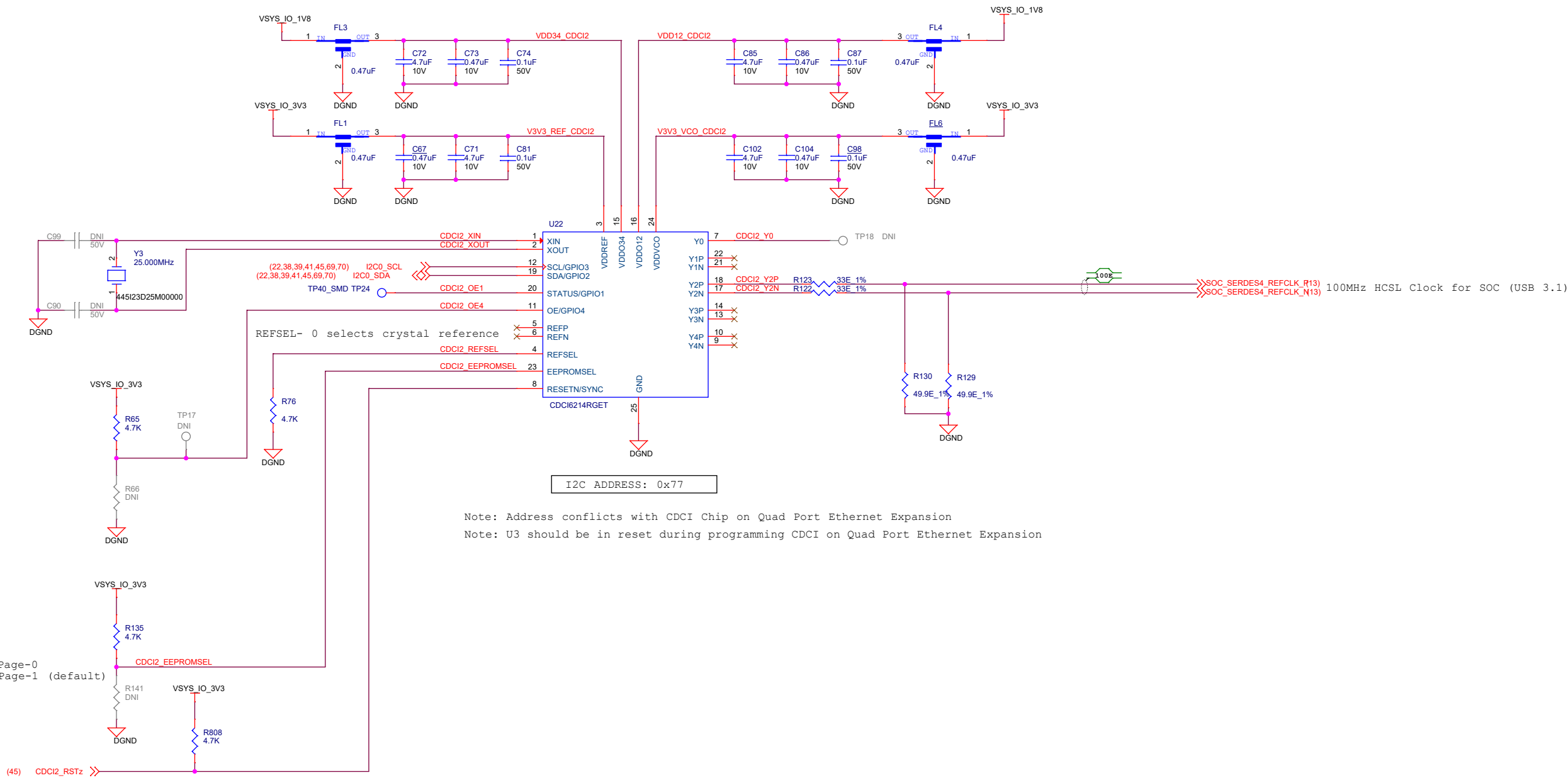
CSI2 EXPANSION CONNECTORS



SERDES CLOCK GENERATOR #1



SERDES CLOCK GENERATOR #2



EEPROMSEL - LOW - Page-0
EEPROMSEL - HIGH - Page-1 (default)

Project :

J7 EVM



Title
SERDES CLOCK GENERATOR #2

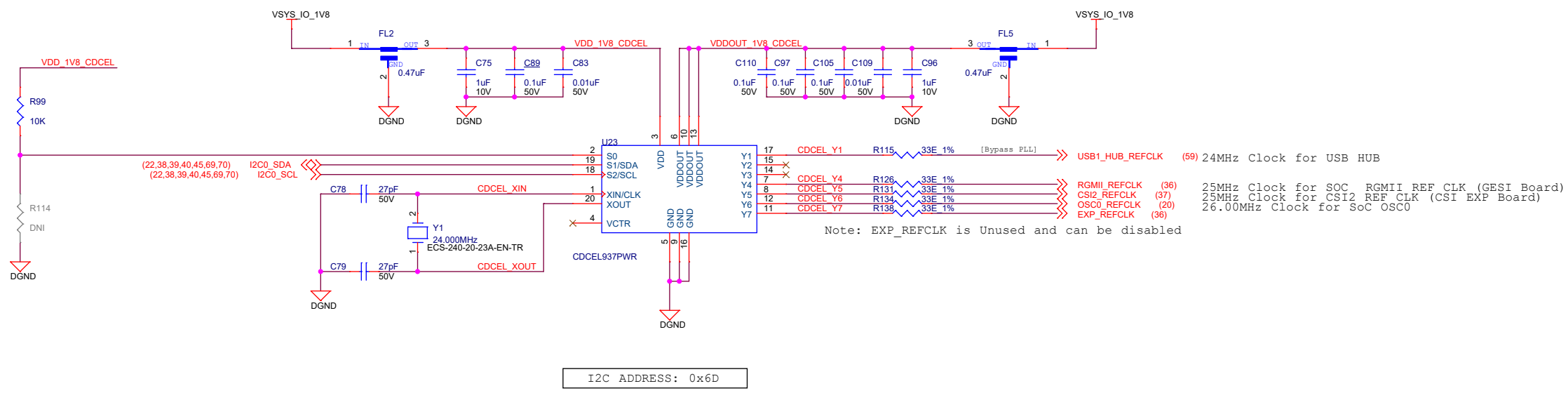
Size
C
PROC184 002

Date: Friday, May 17, 2024

Sheet 37 of 84

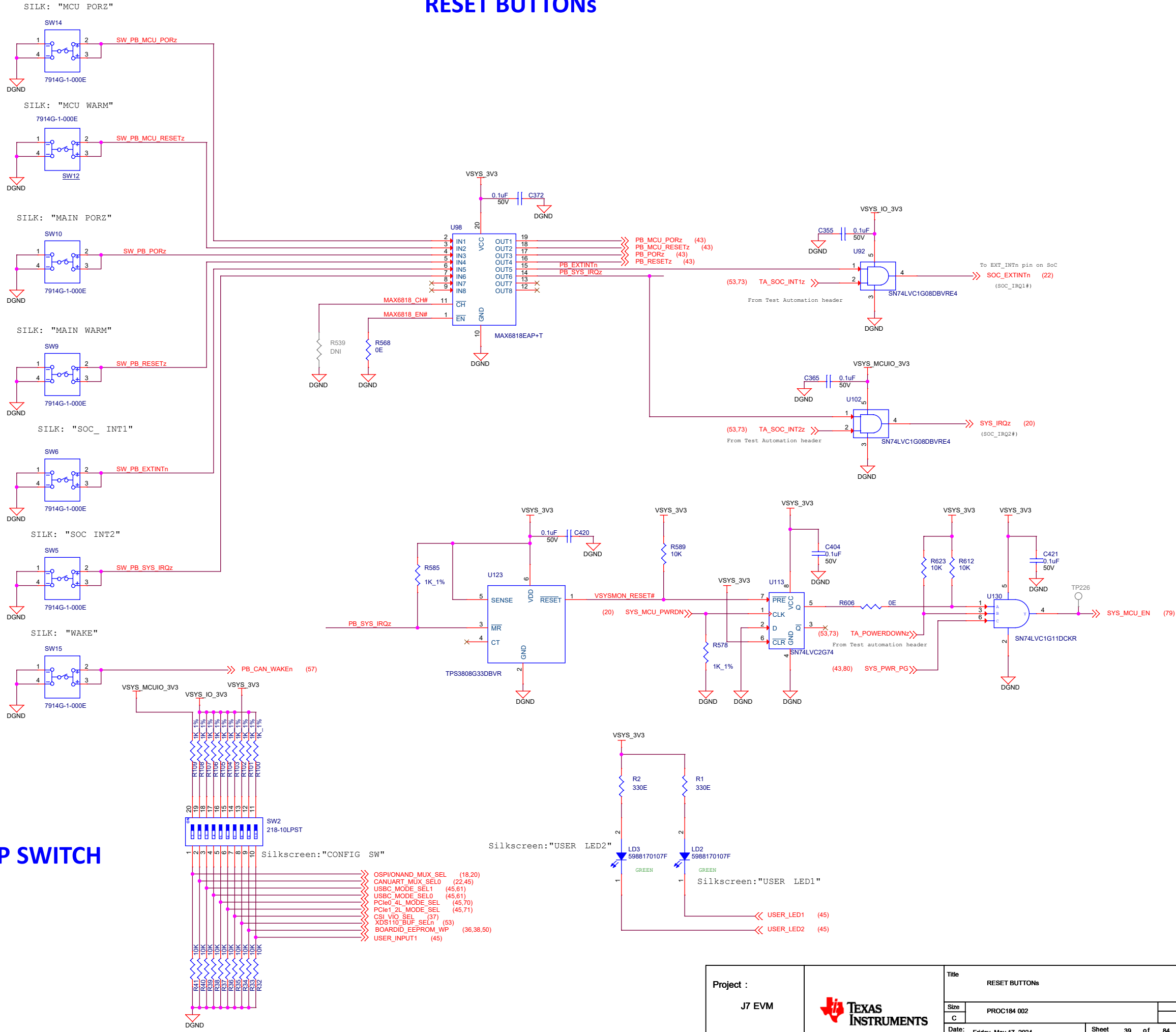
Rev
E1

PERIPHERAL CLOCK GENERATOR



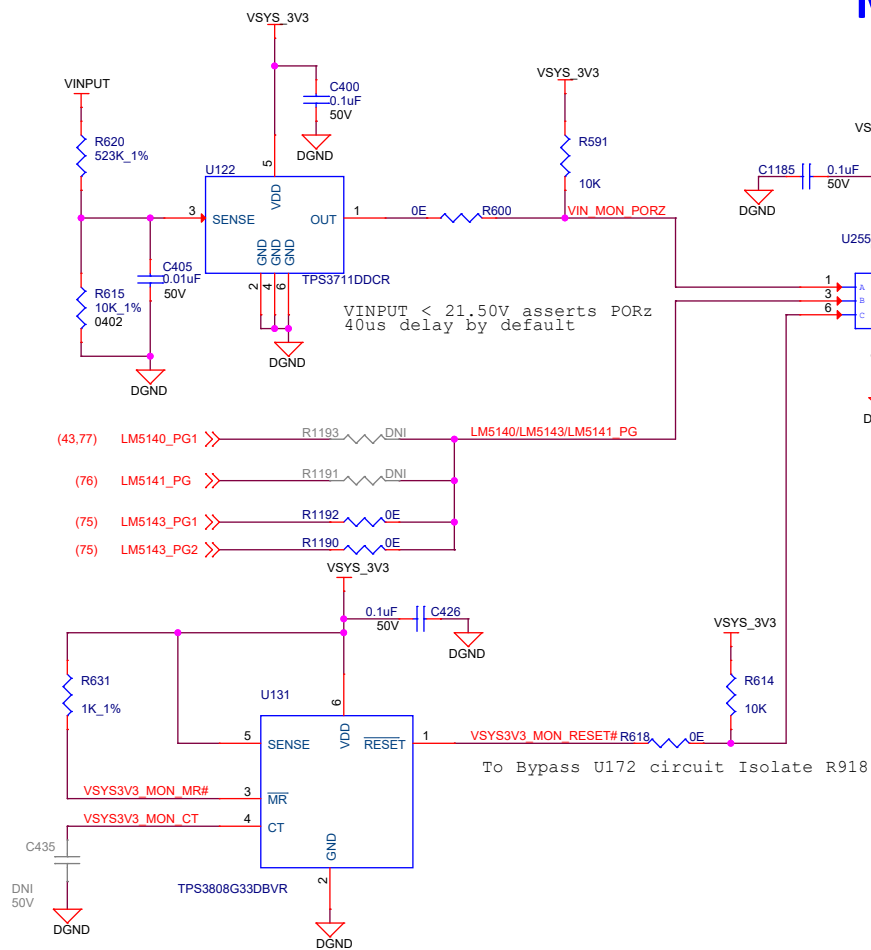
RESET BUTTONs

CONFIG DIP SWITCH

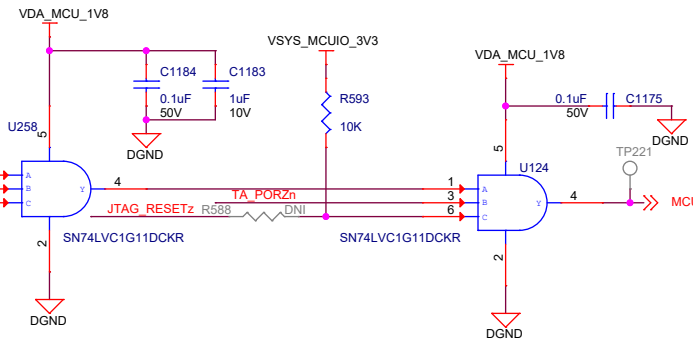
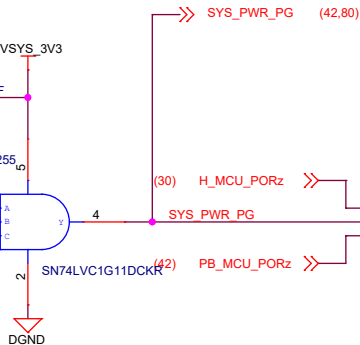


RESET INPUTS

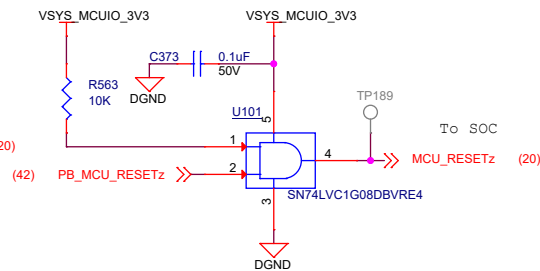
Under Voltage Monitor (VINPUT)



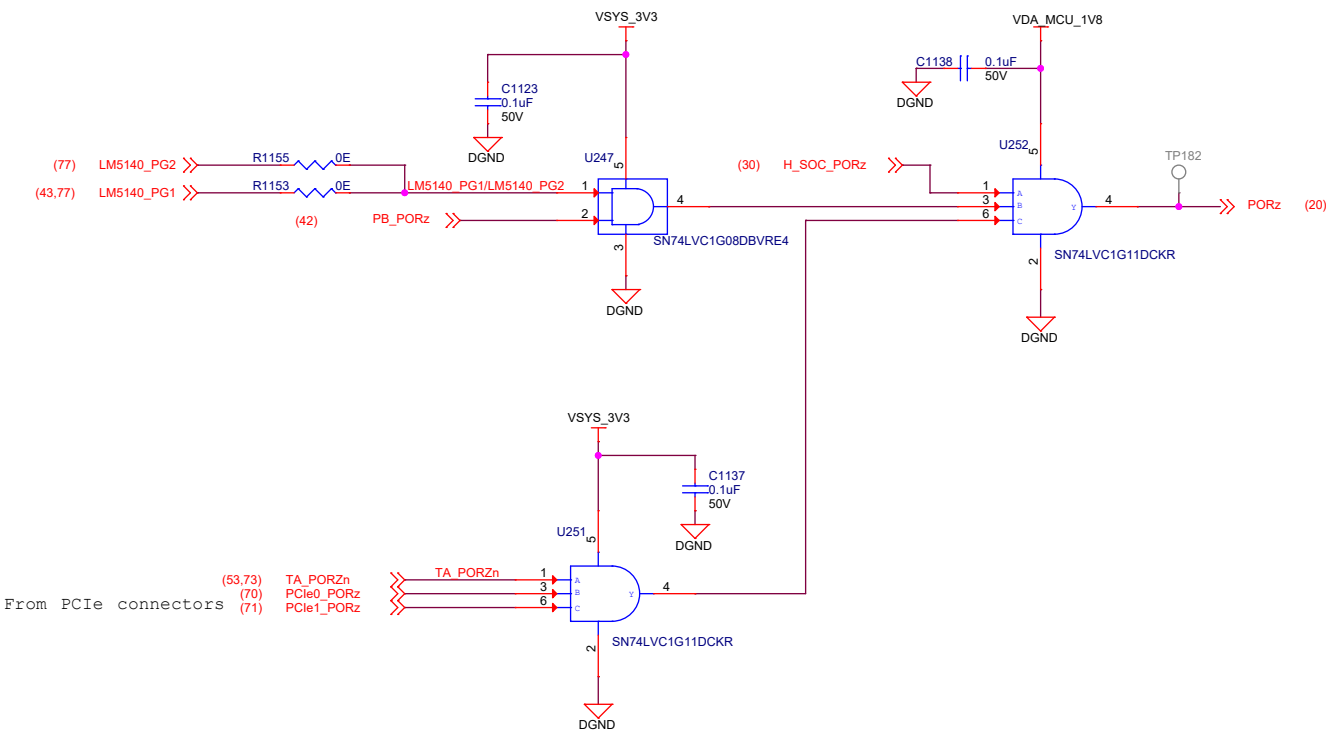
MCU PORz



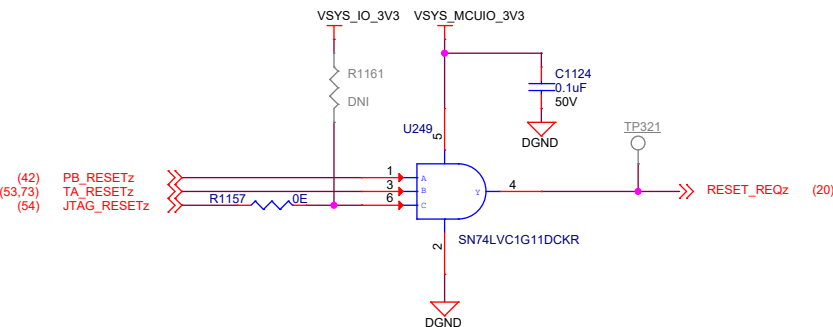
MCU_RESET



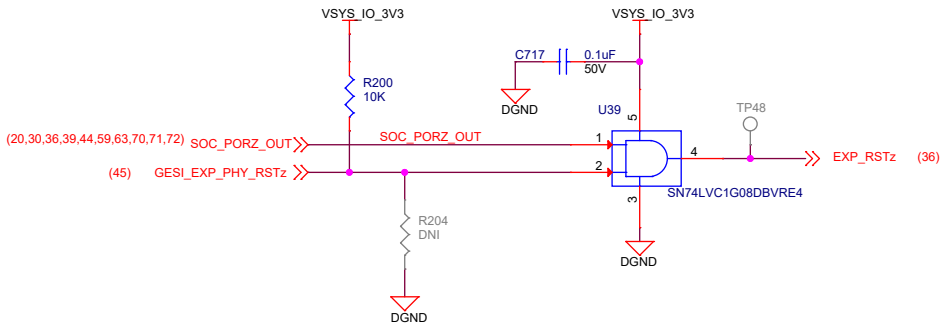
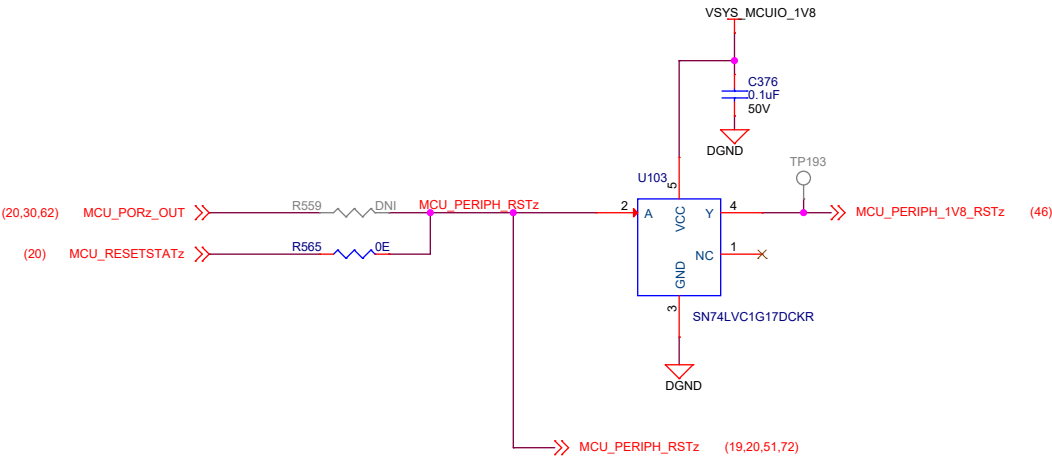
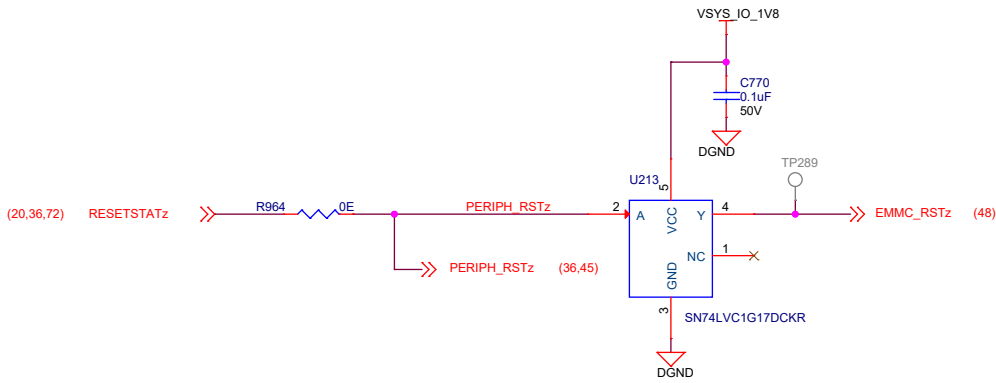
SOC PORz



SOC RESET

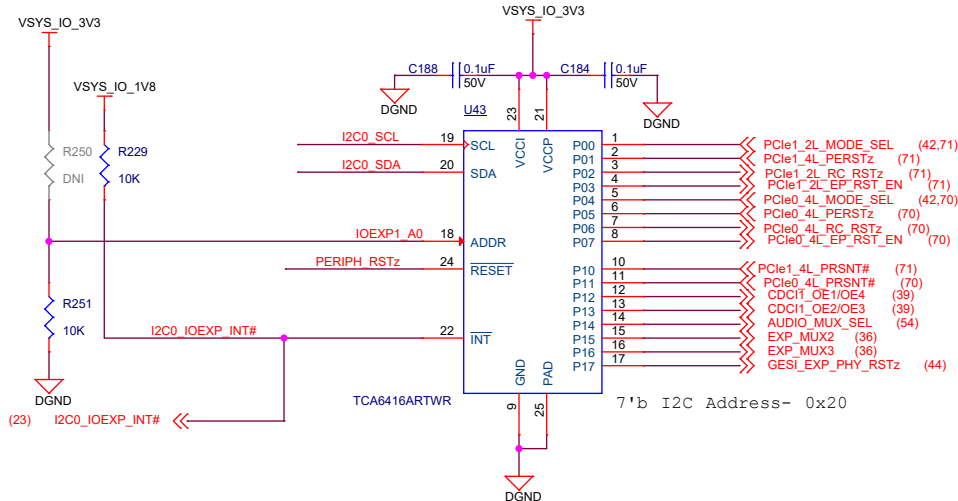


RESET OUTPUTS

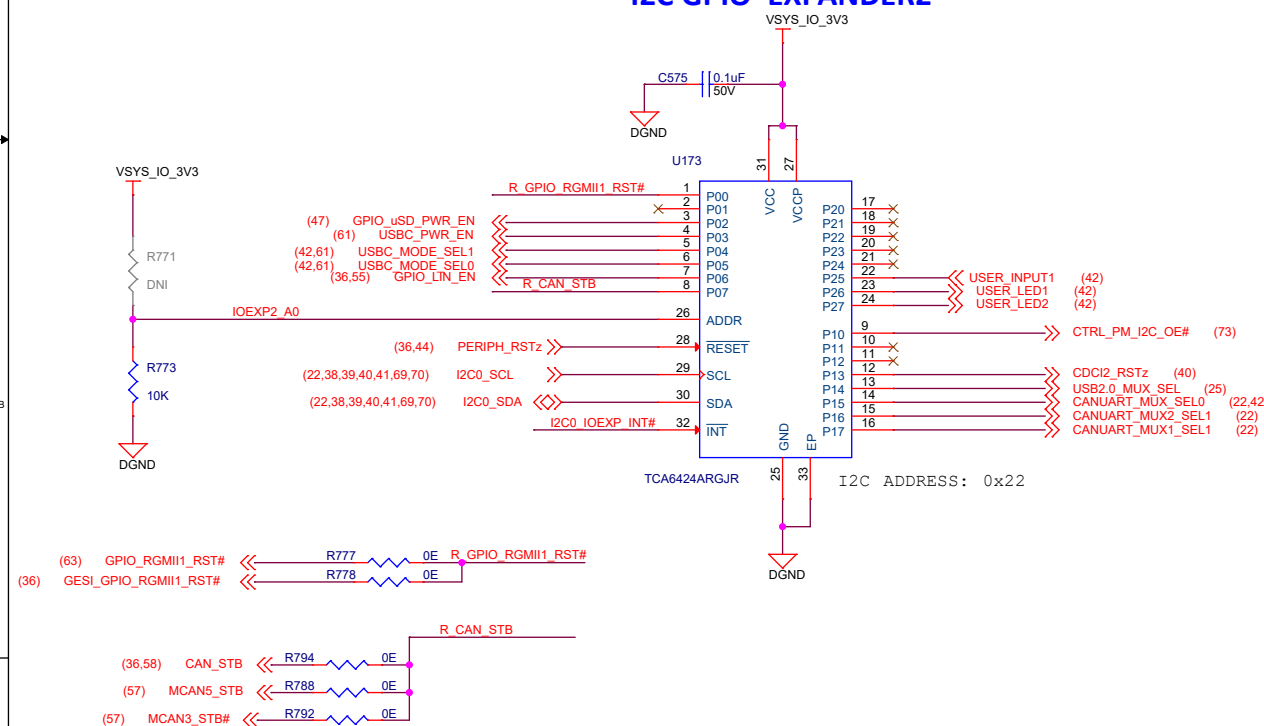


GPIO EXPANDERS

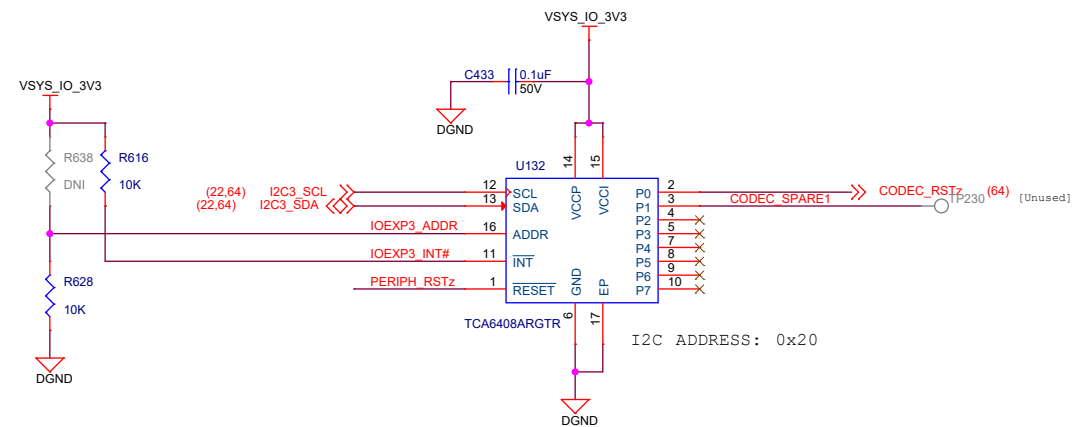
I2C GPIO EXPANDER1



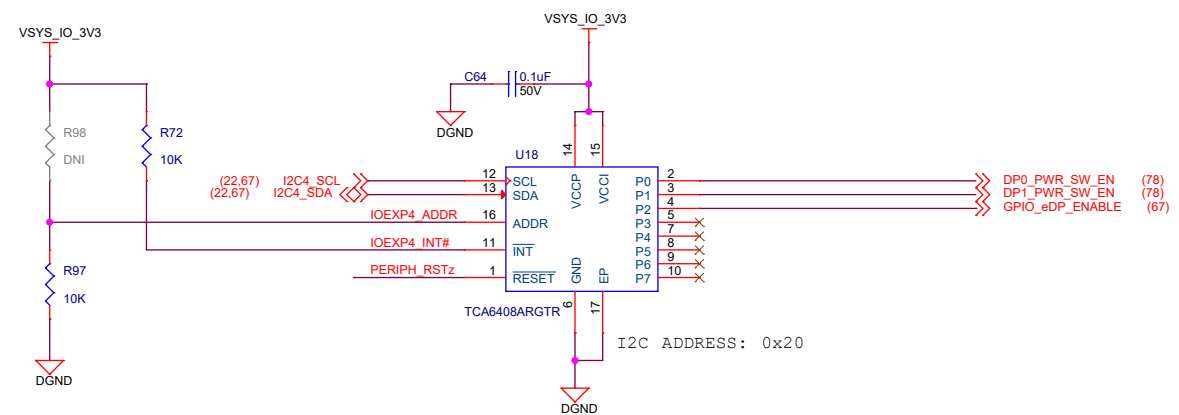
I2C GPIO EXPANDER2



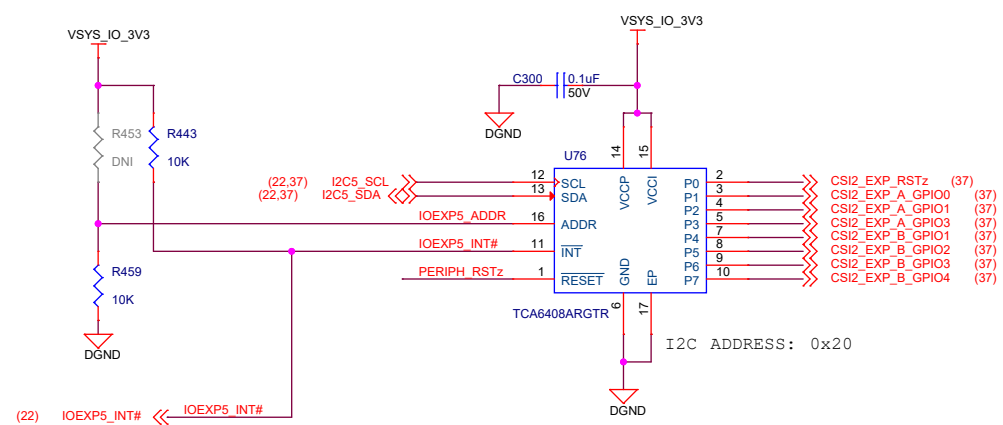
I2C GPIO EXPANDER3



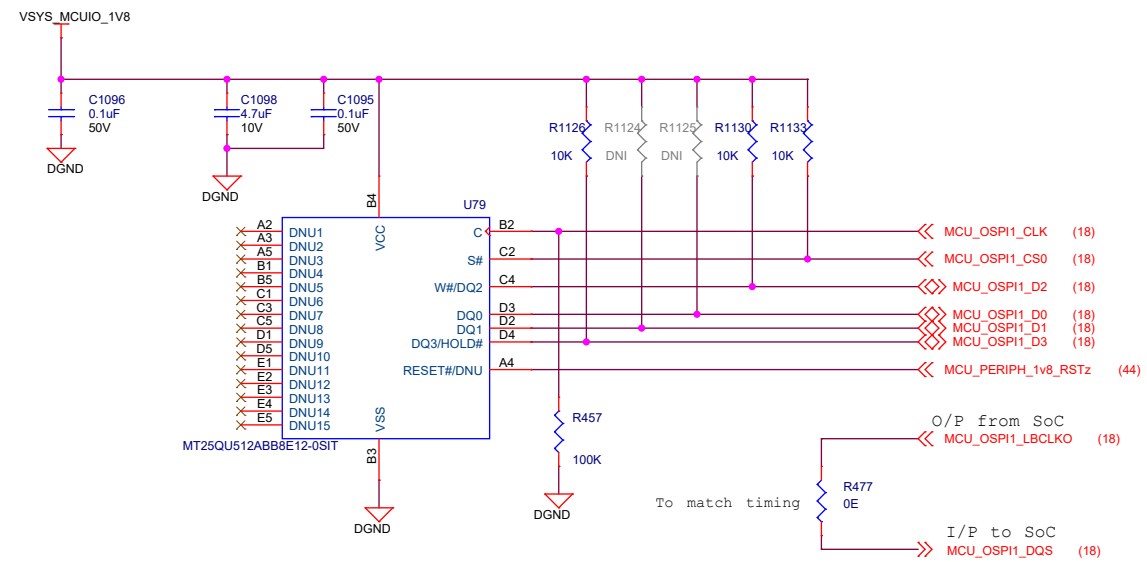
I2C GPIO EXPANDER4



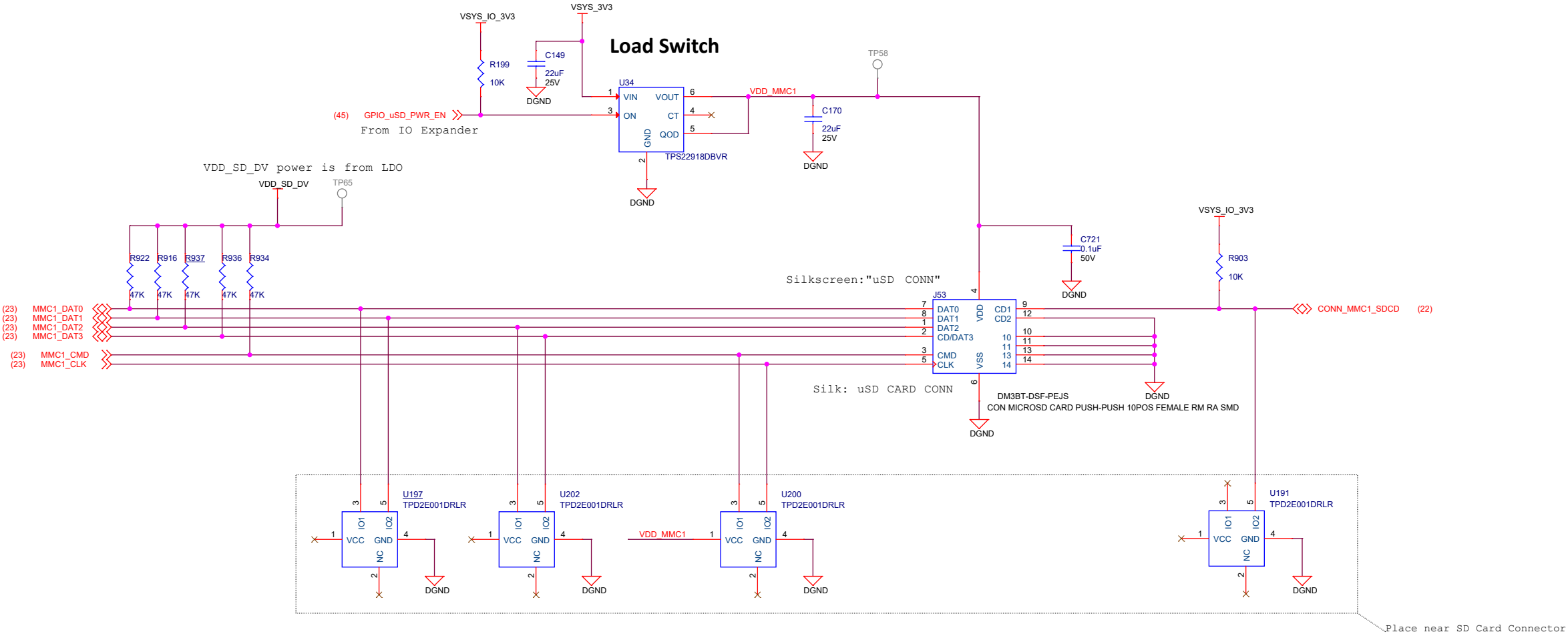
I2C GPIO EXPANDER!



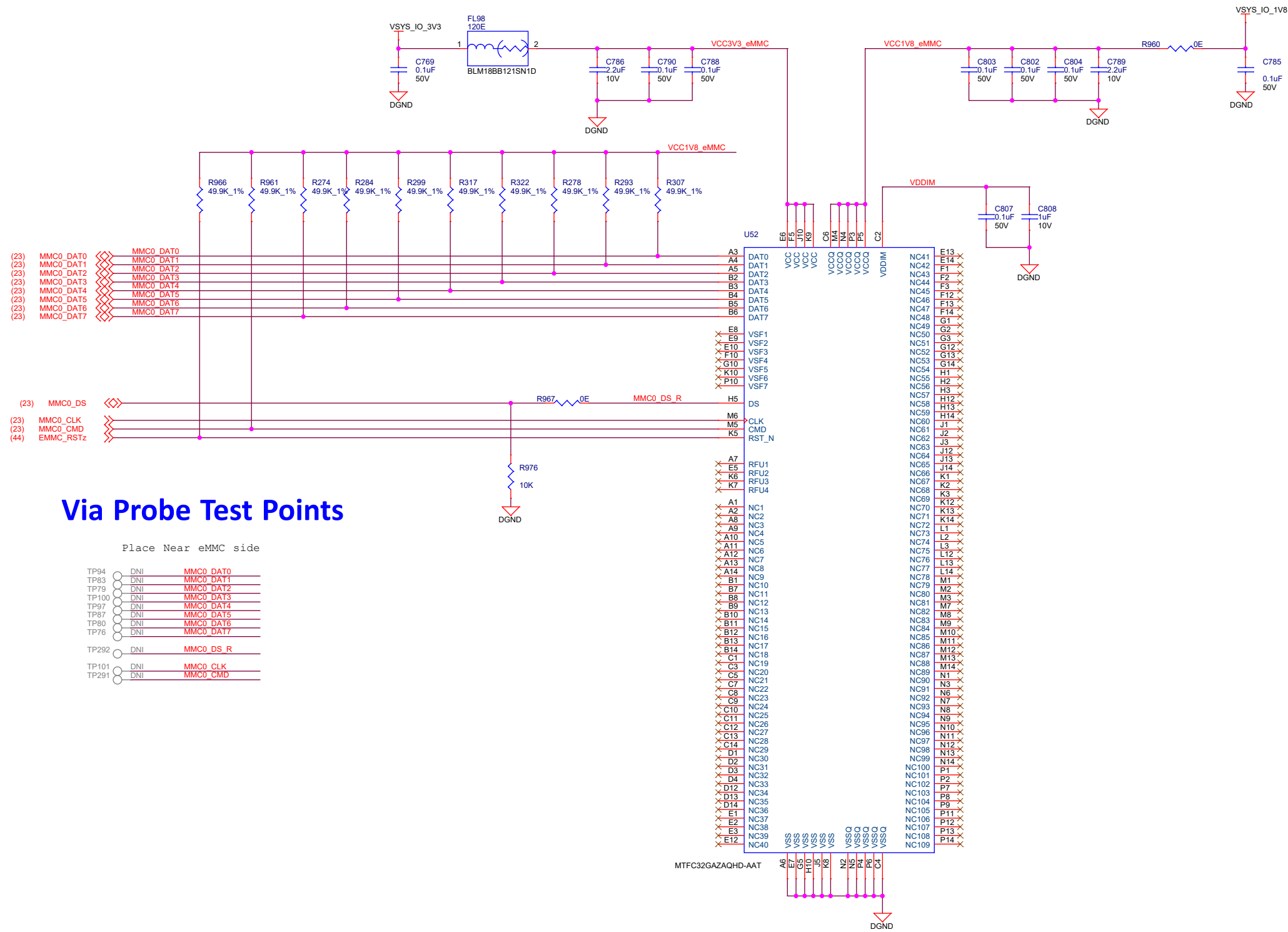
SPI NOR Flash



Micro SD CARD INTERFACE



eMMC FLASH

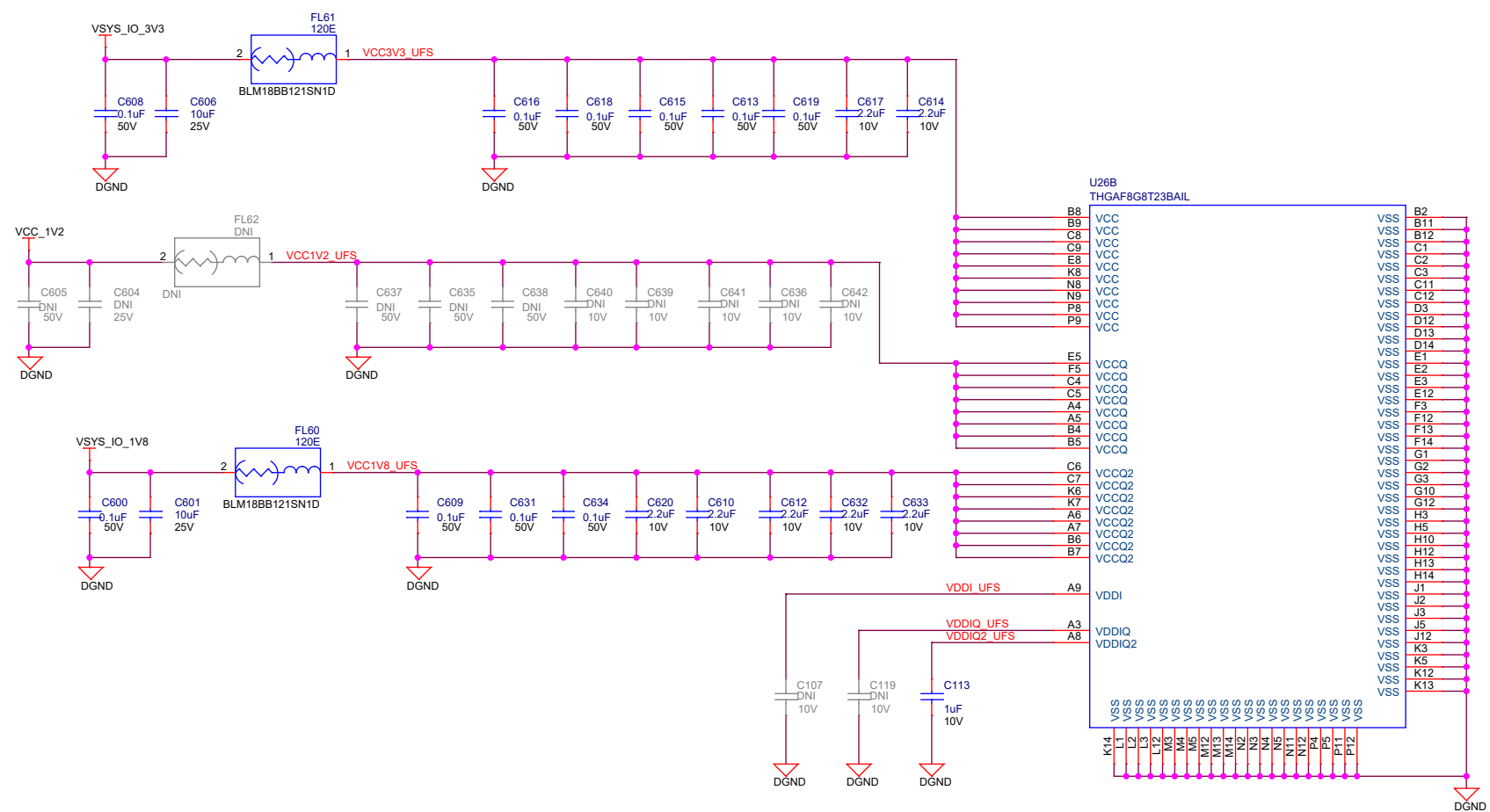
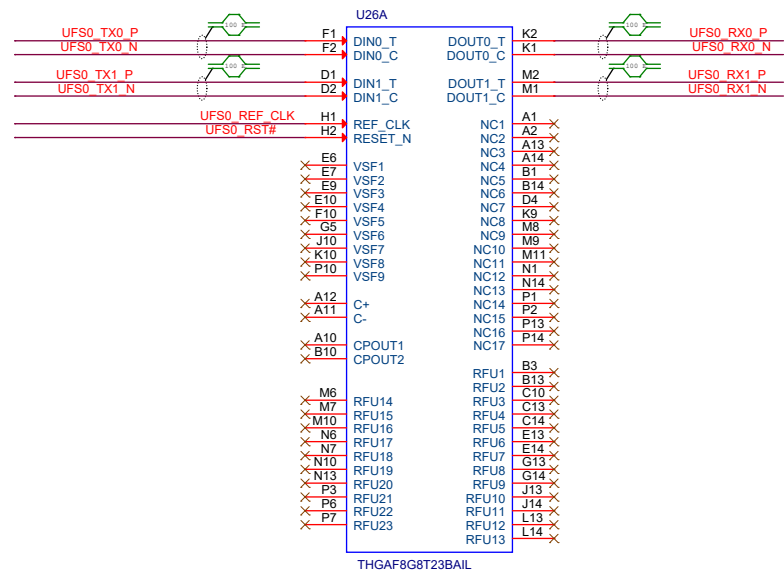
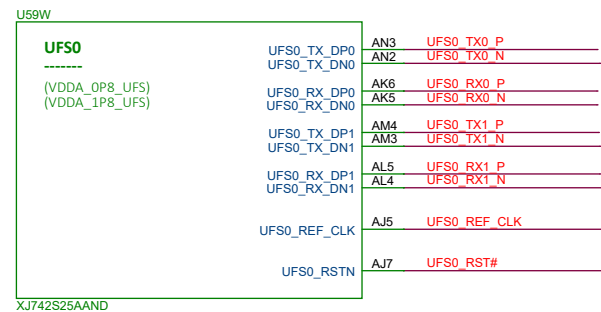


Via Probe Test Points

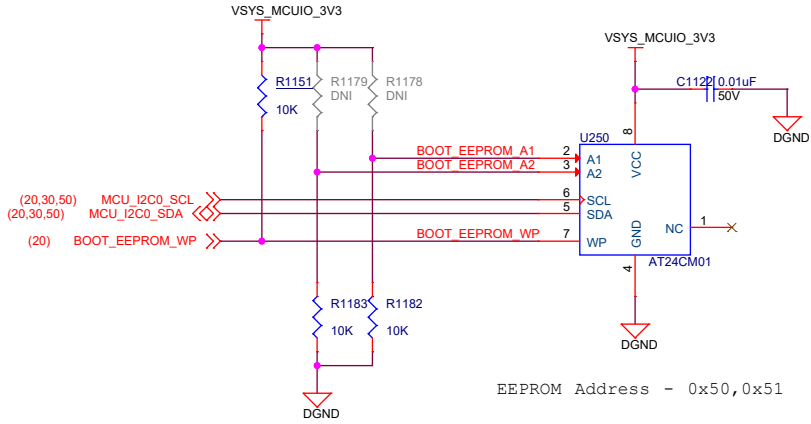
Place Near eMMC side

TP94	DNI	MMC0_DAT0
TP83	DNI	MMC0_DAT1
TP79	DNI	MMC0_DAT2
TP100	DNI	MMC0_DAT3
TP97	DNI	MMC0_DAT4
TP87	DNI	MMC0_DAT5
TP80	DNI	MMC0_DAT6
TP76	DNI	MMC0_DAT7
TP292	DNI	MMC0_DS_R
TP101	DNI	MMC0_CLK
TP291	DNI	MMC0_CMD

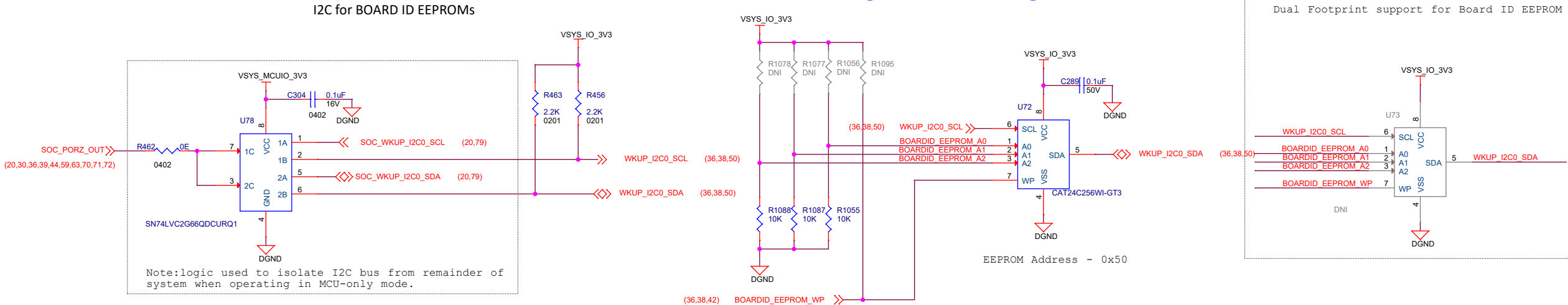
UFS FLASH



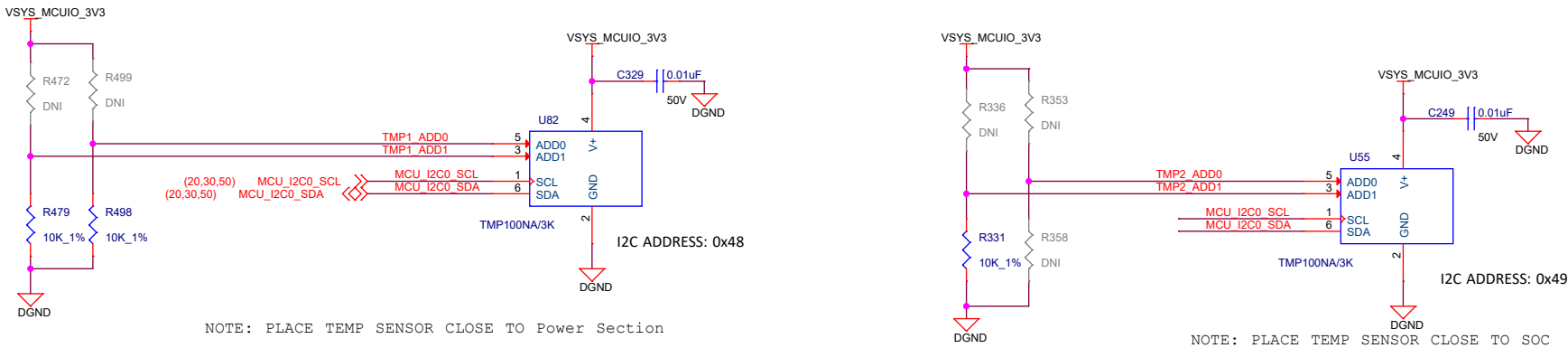
BOOT EEPROM



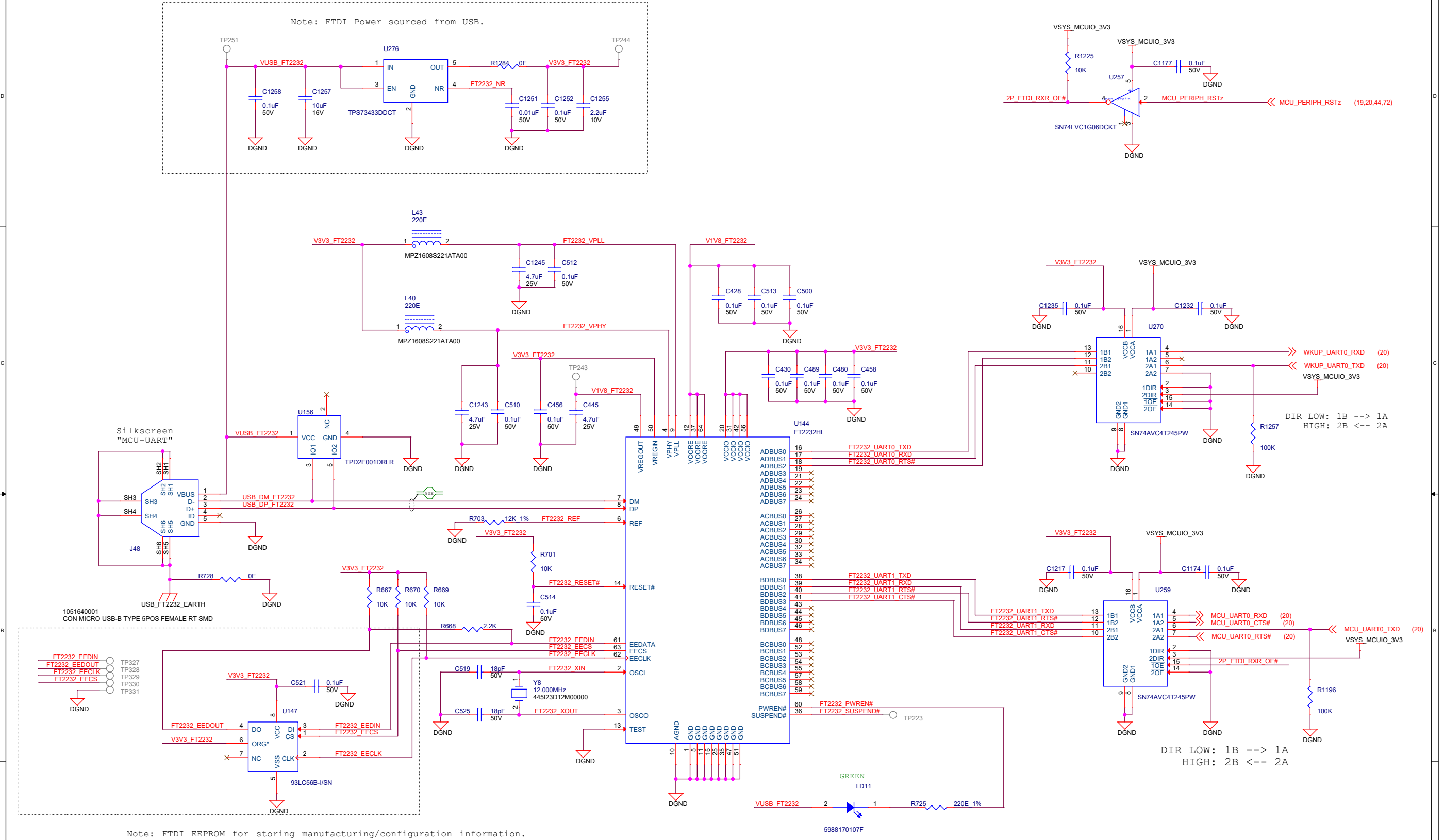
BOARD ID EEPROM



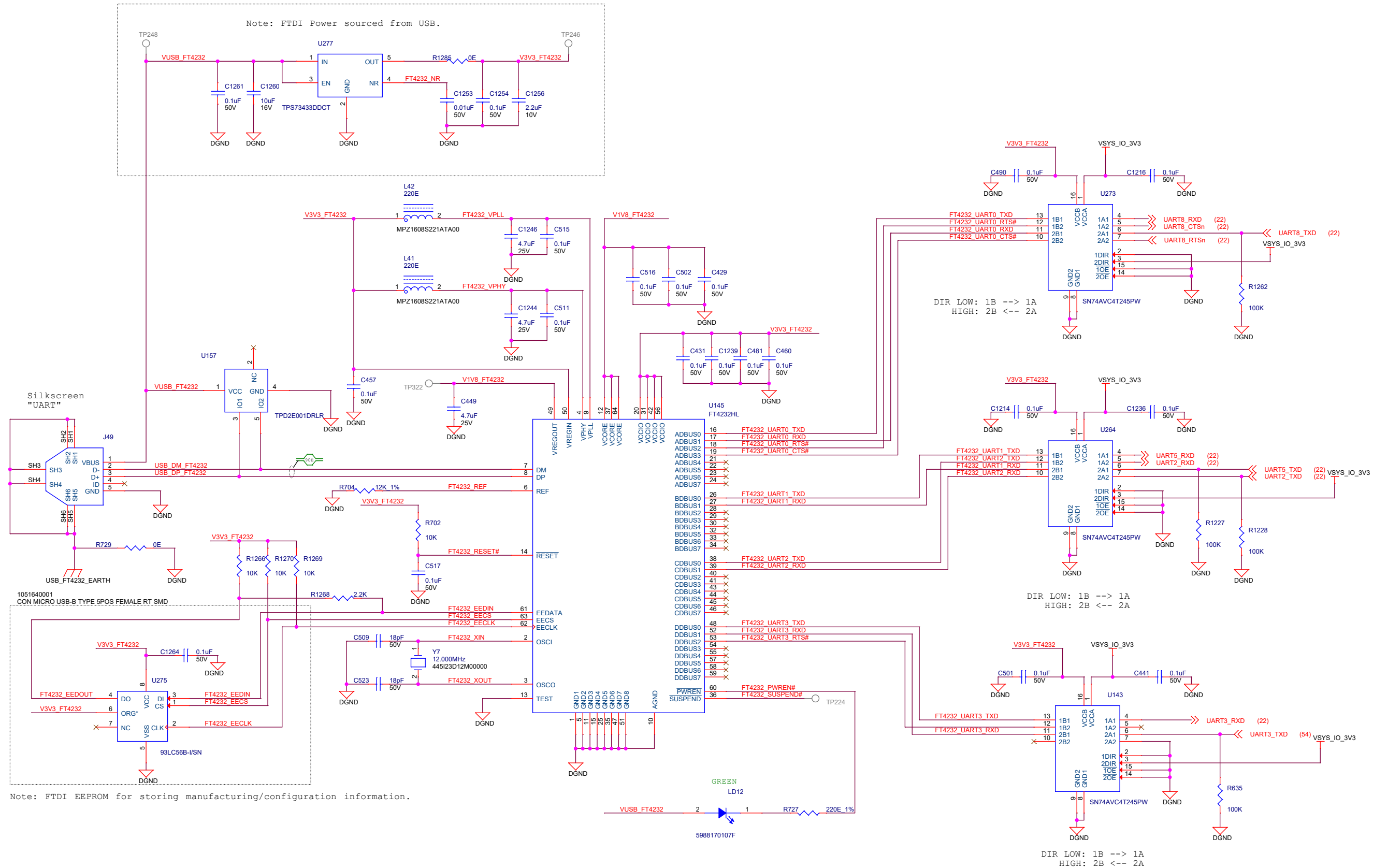
TEMPERATURE SENSORS (TI EVM Only)



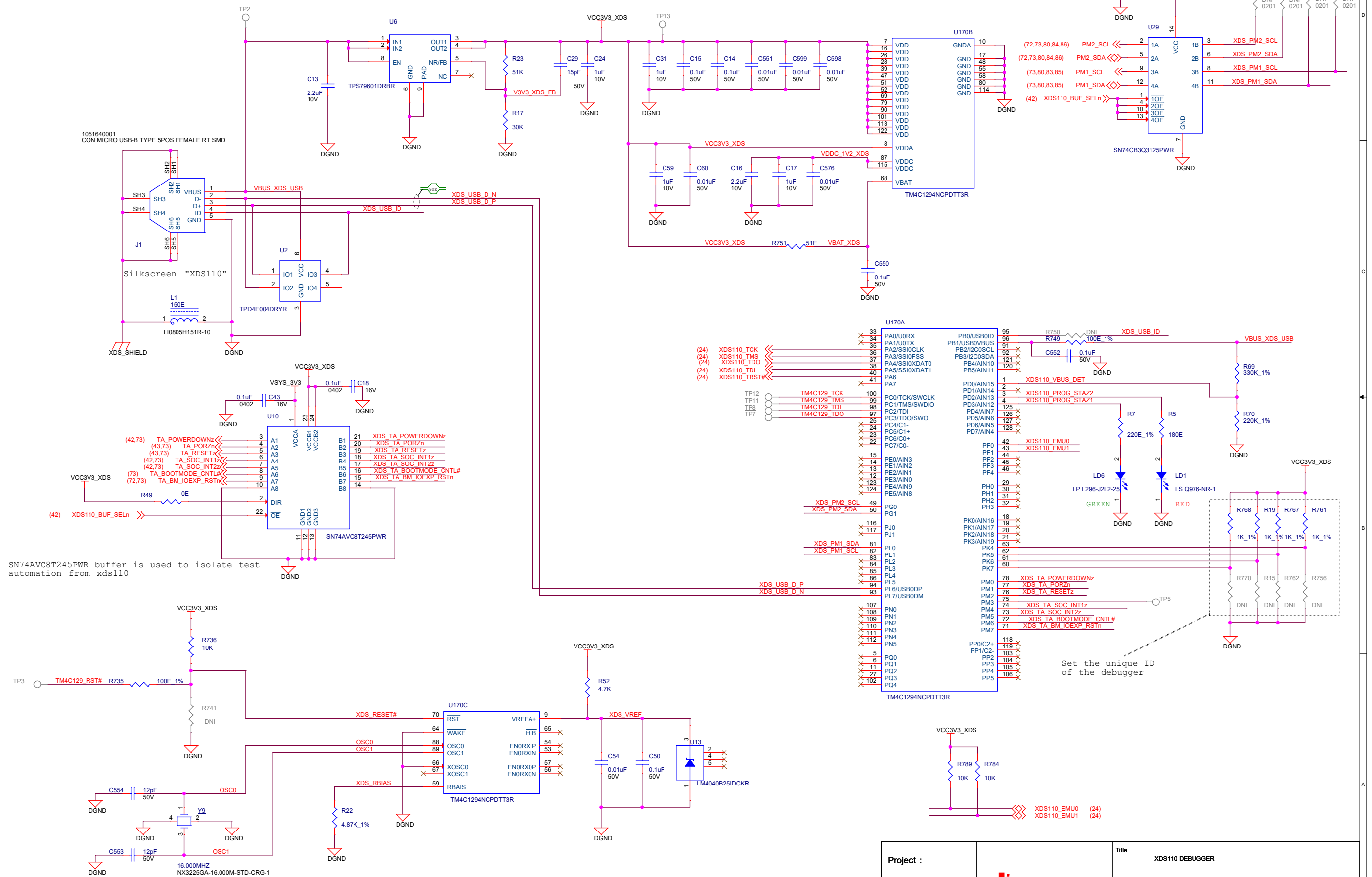
DUAL PORT FTDI



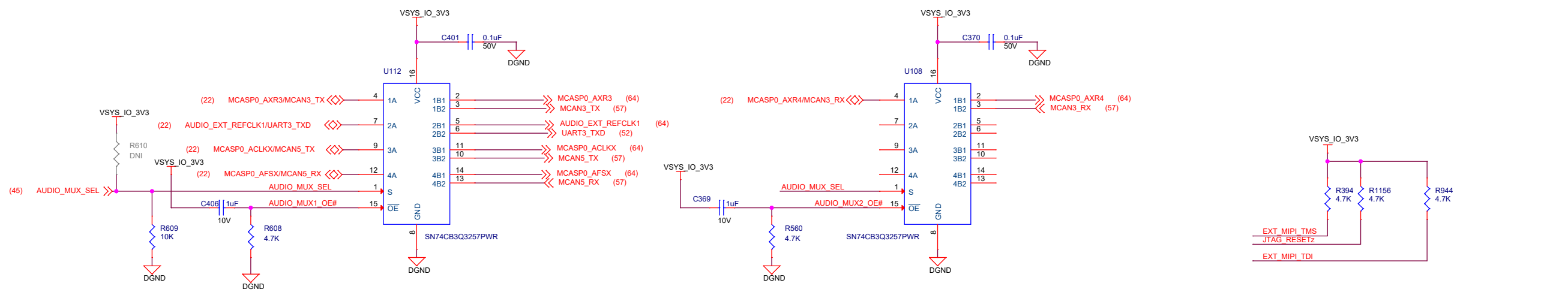
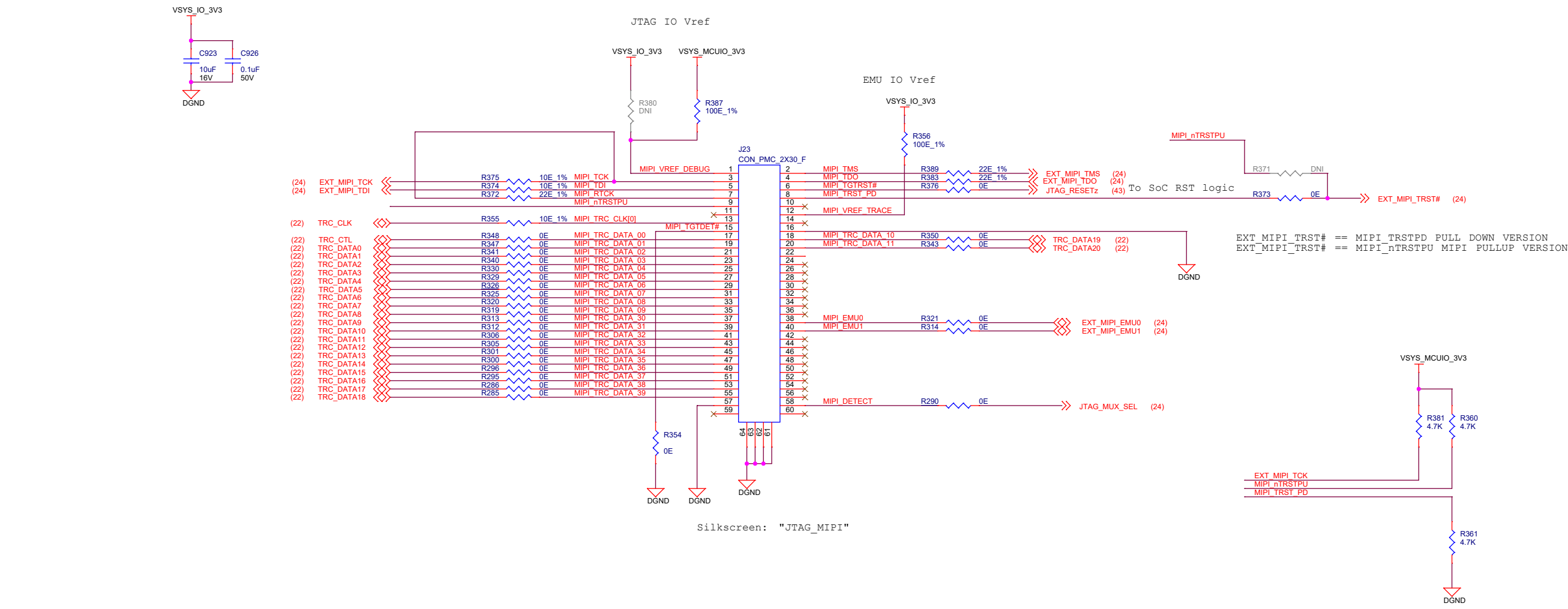
QUAD PORT FTDI



XDS110 DEBUGGER

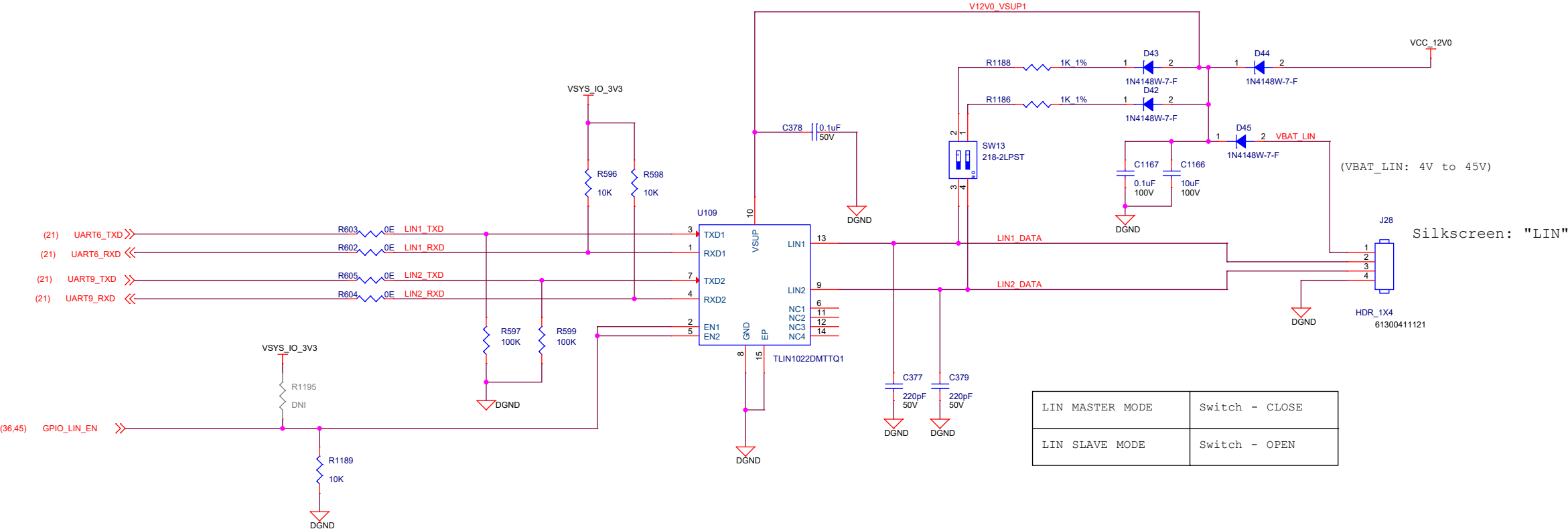


JTAG MIPI60 CONNECTOR



JTAG - 1:2 MUX : Truth Table

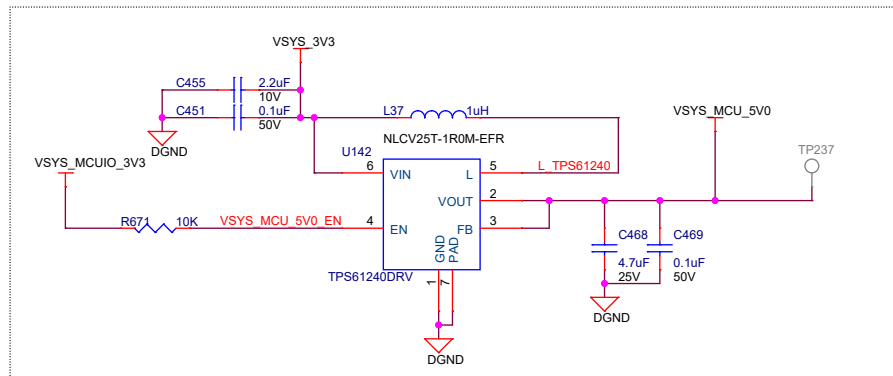
LIN INTERFACE



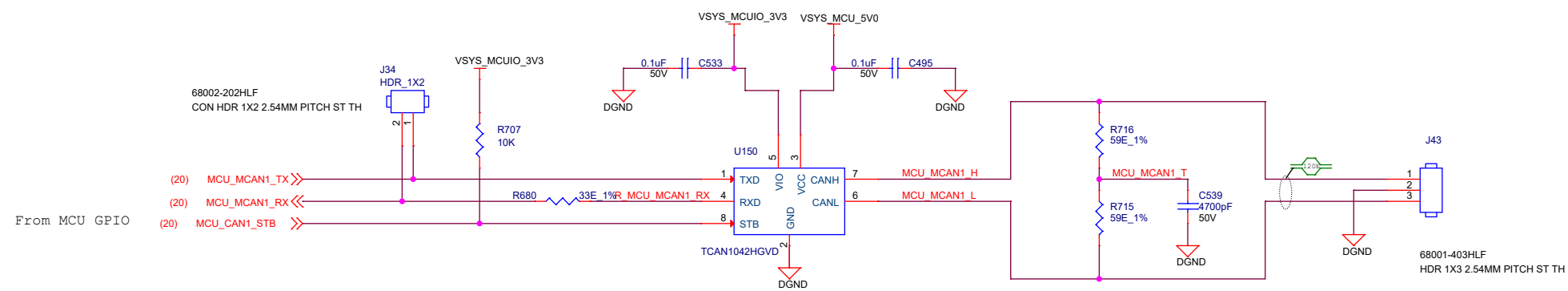
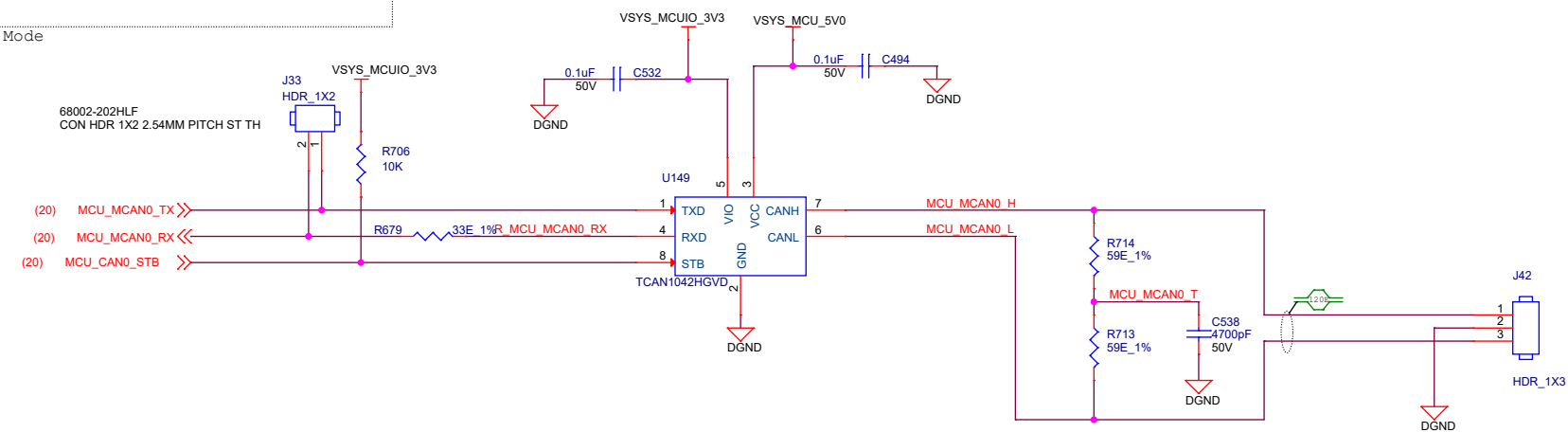
LIN MASTER MODE	Switch - CLOSE
LIN SLAVE MODE	Switch - OPEN

CAN TRANSCEIVERS #1-MCU DOMAIN

VSYS_MCU_5V0 GENERATION



Separate 5V0 supply required for MCU-Only Mode



Project :

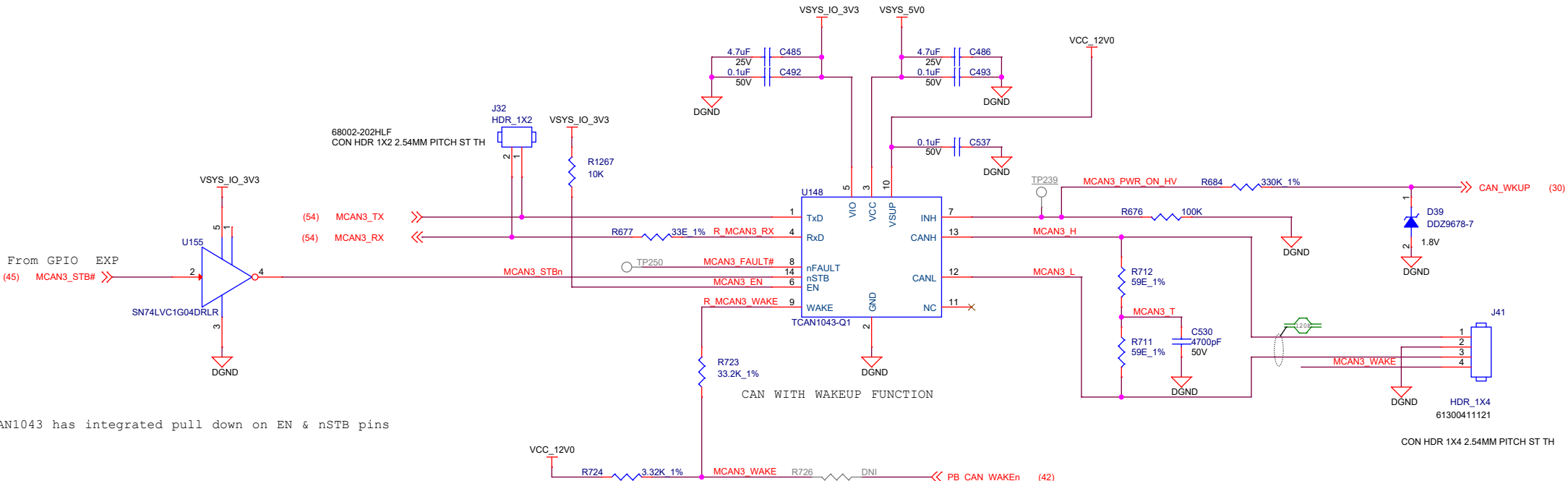
J7 EVM



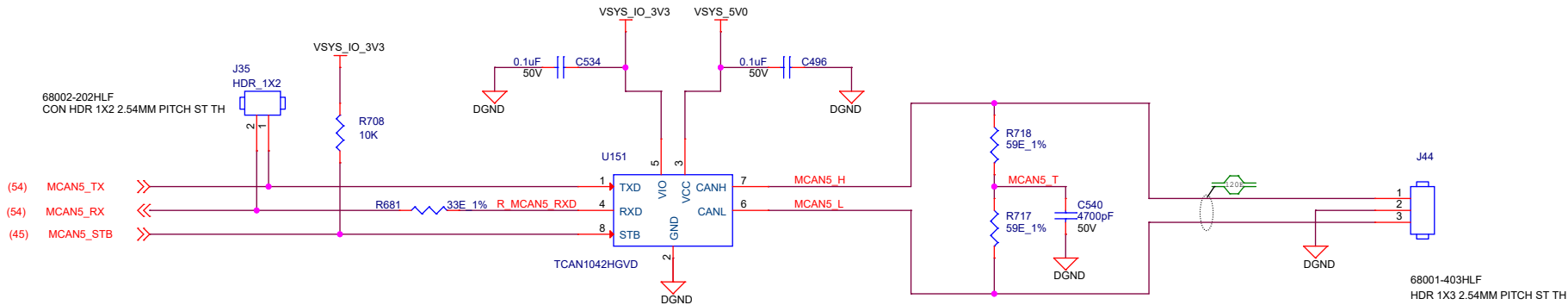
Title	CAN TRANSCEIVERS #1
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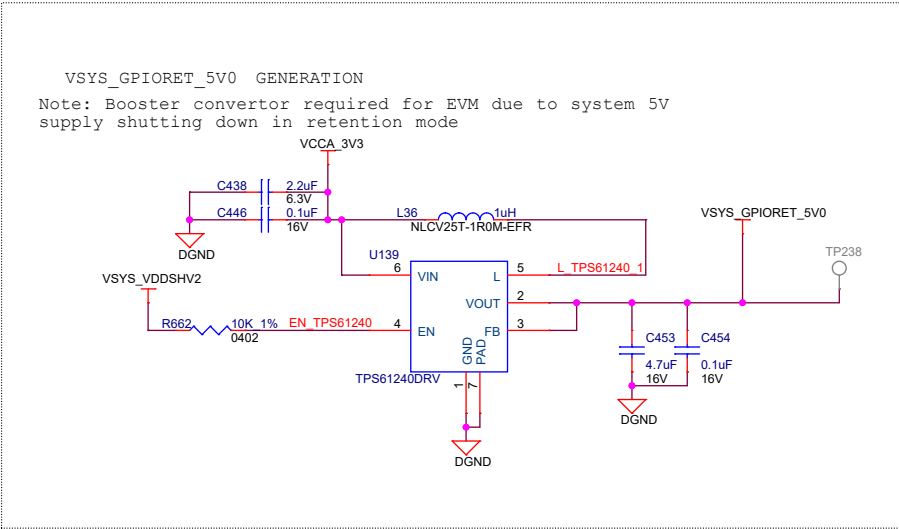
Size	PROC184 002	Rev
C		E1
Date:	Thursday, May 16, 2024	Sheet 53 of 84

CAN TRANSCEIVERS #2-MAIN DOMAIN

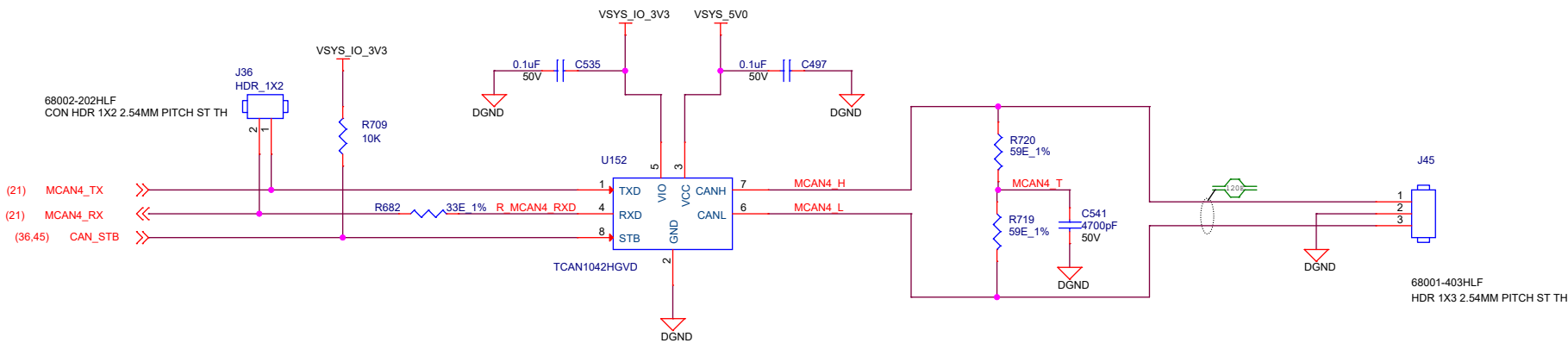
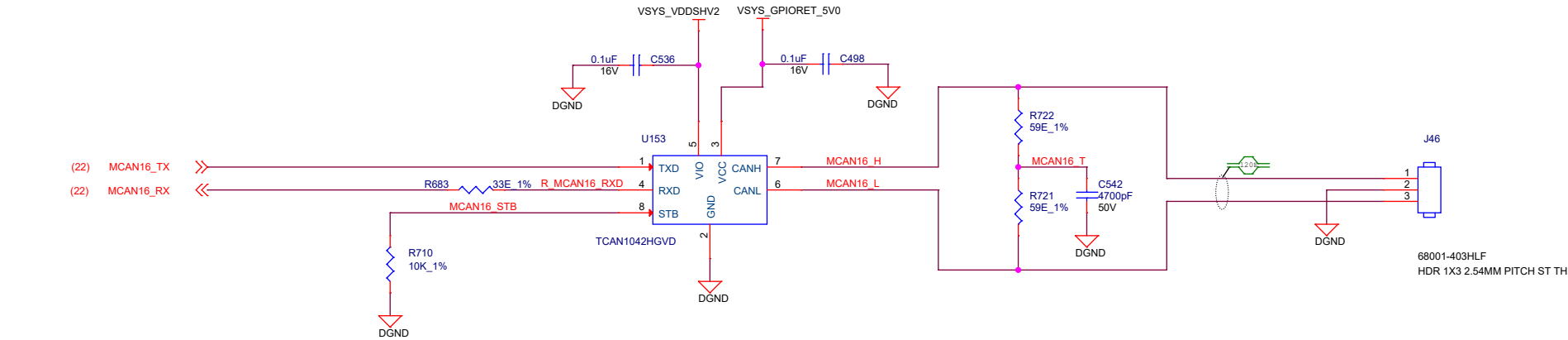


Note:TCAN1043 has integrated pull down on EN & nSTB pins

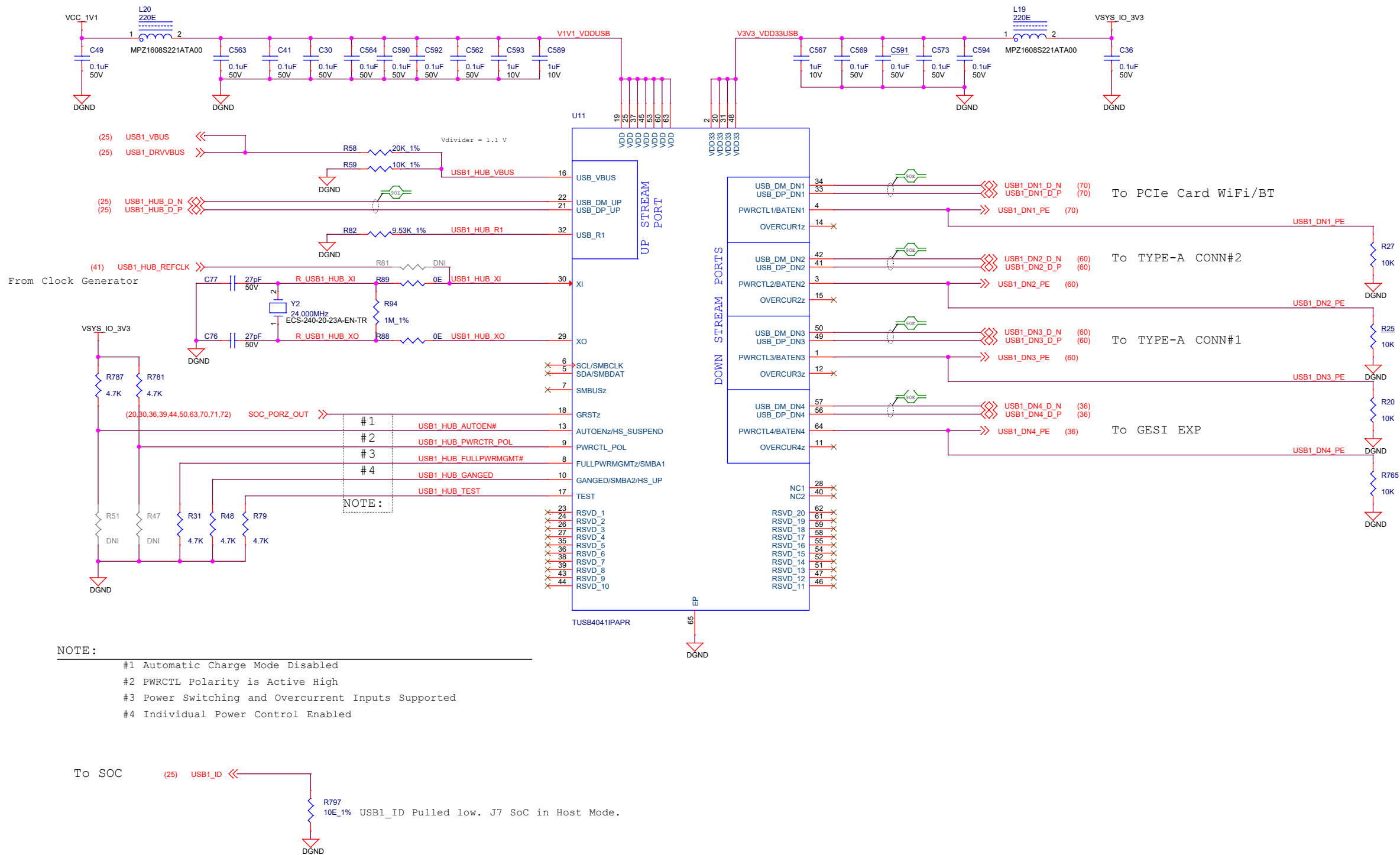




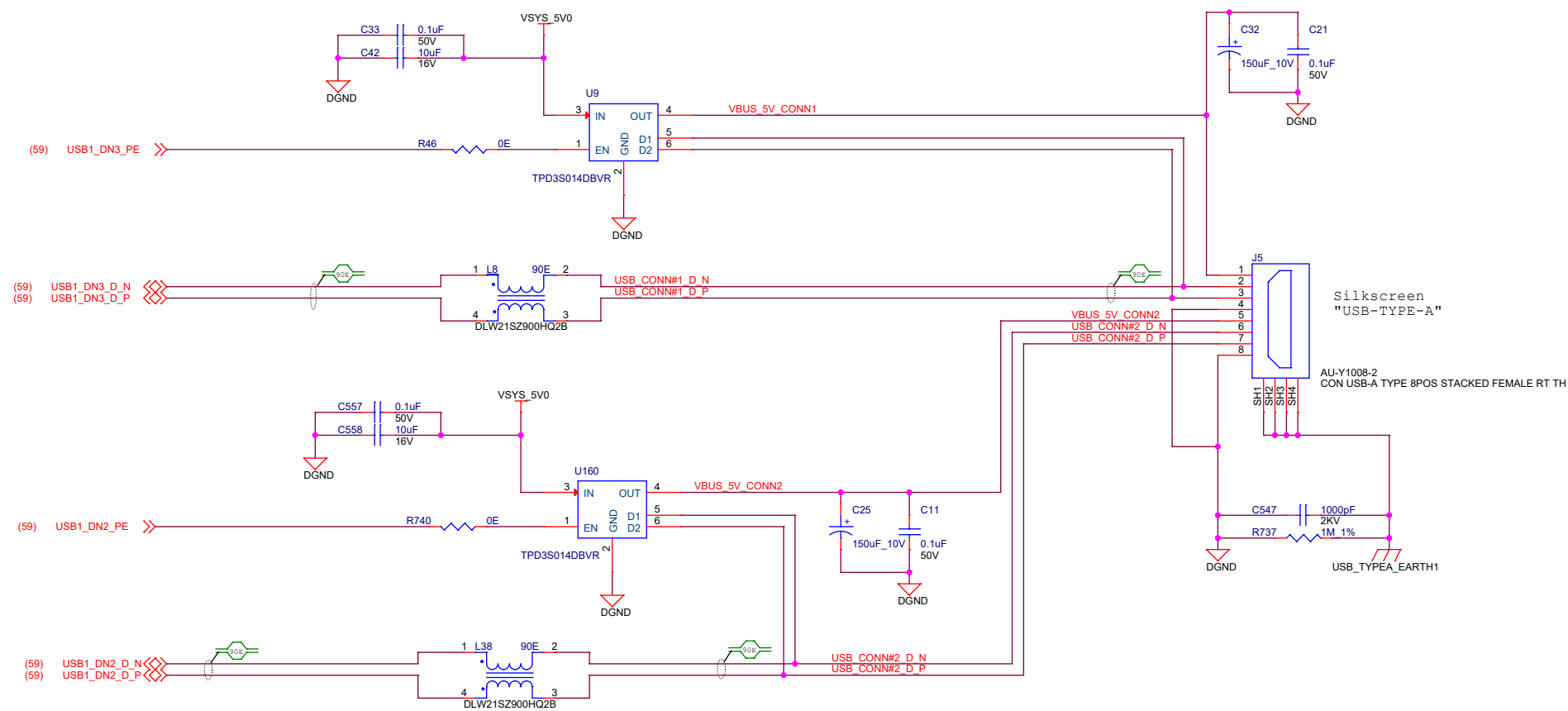
CAN TRANSCEIVER



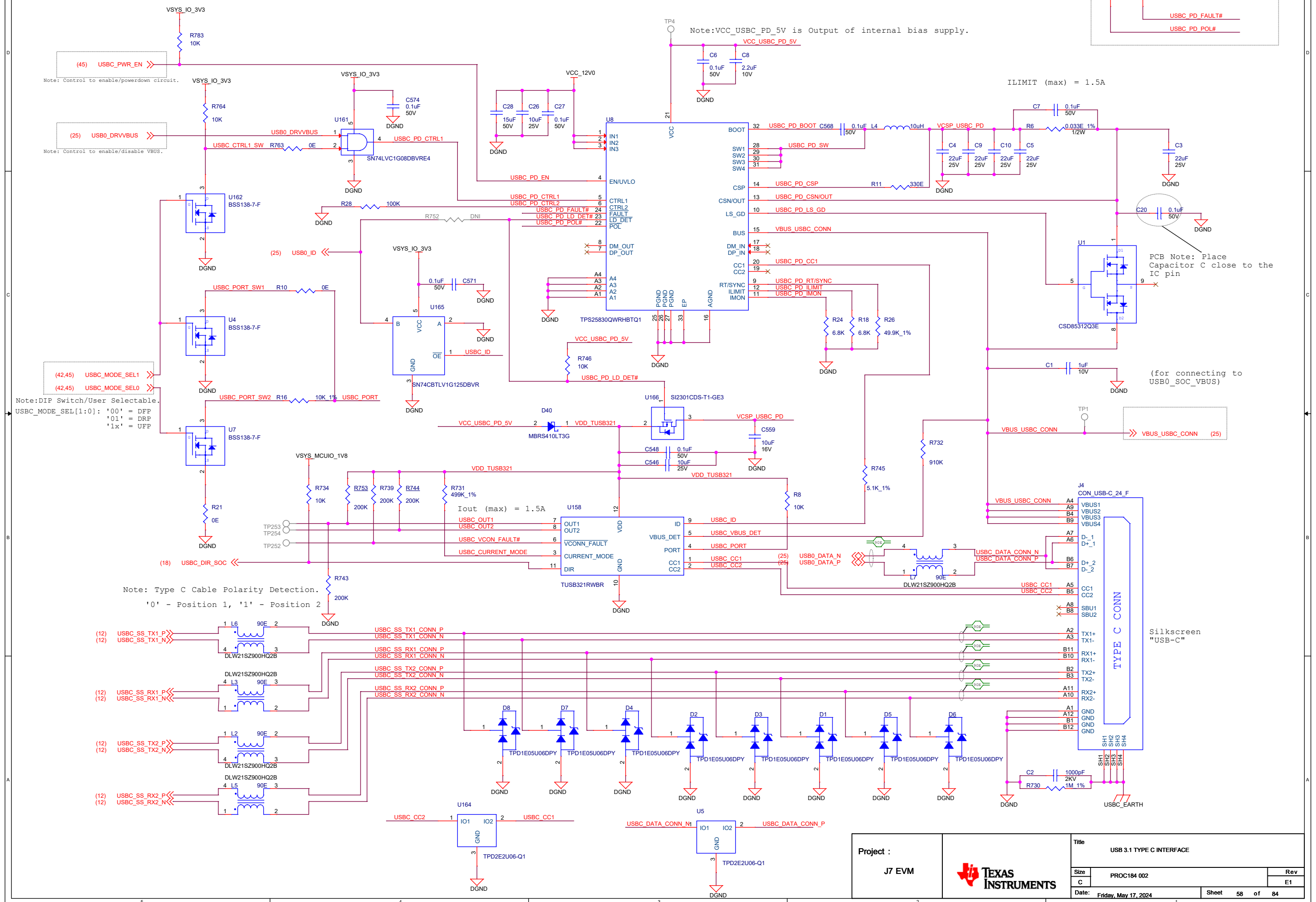
USB HUB



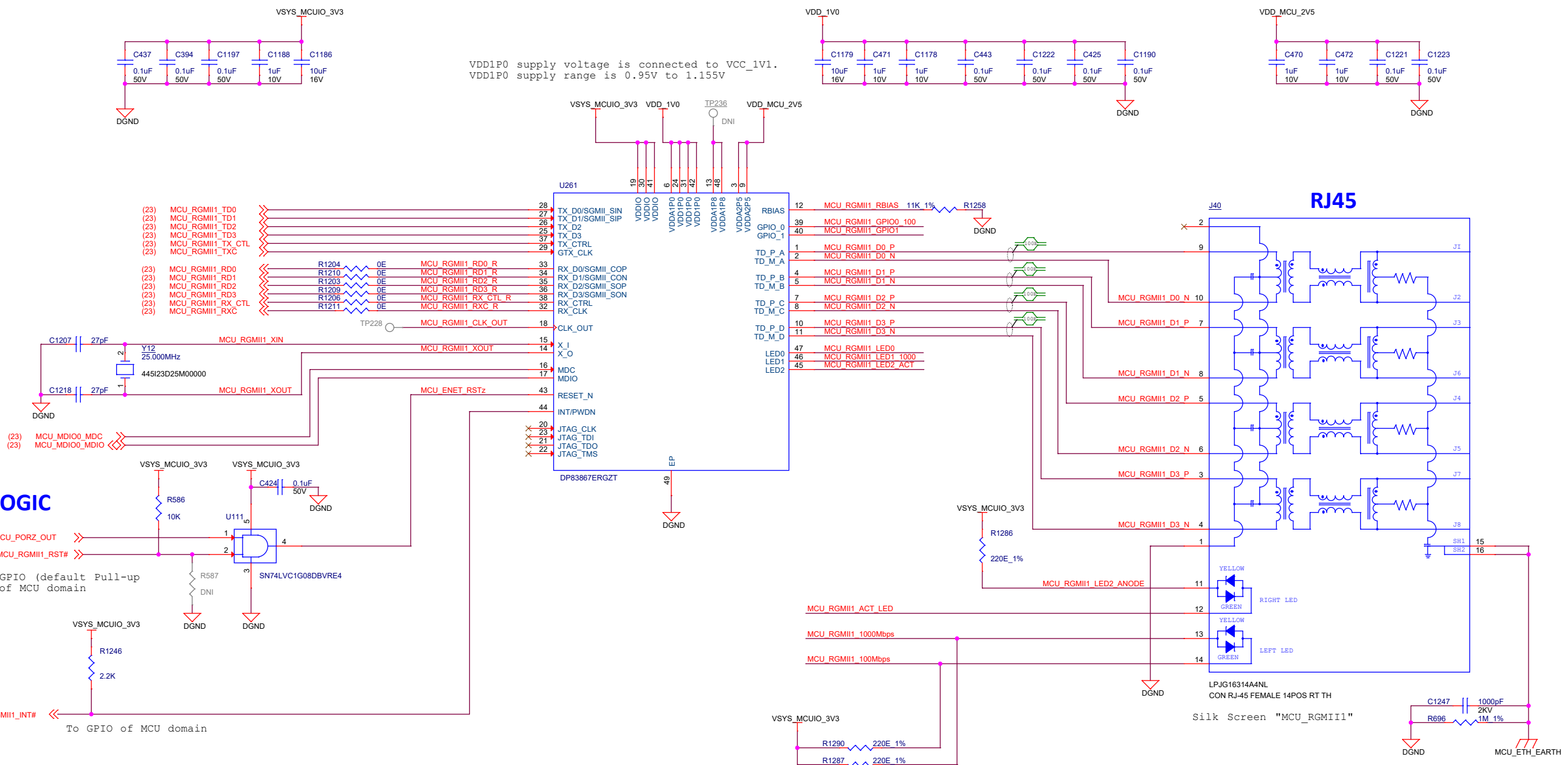
USB 2.0 TYPE-A CONNECTORS



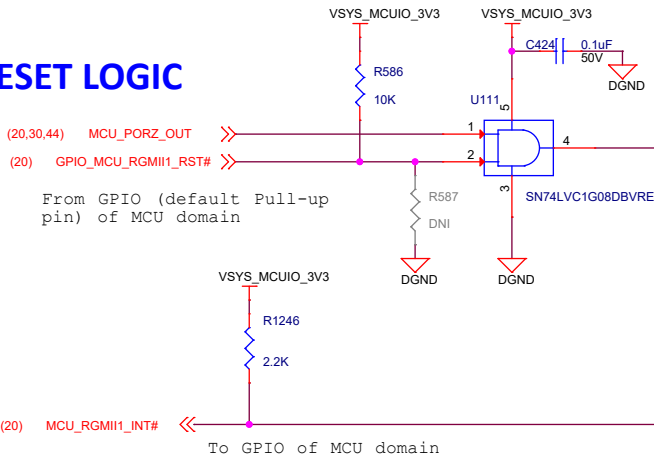
USB 3.1 TYPE C INTERFACE



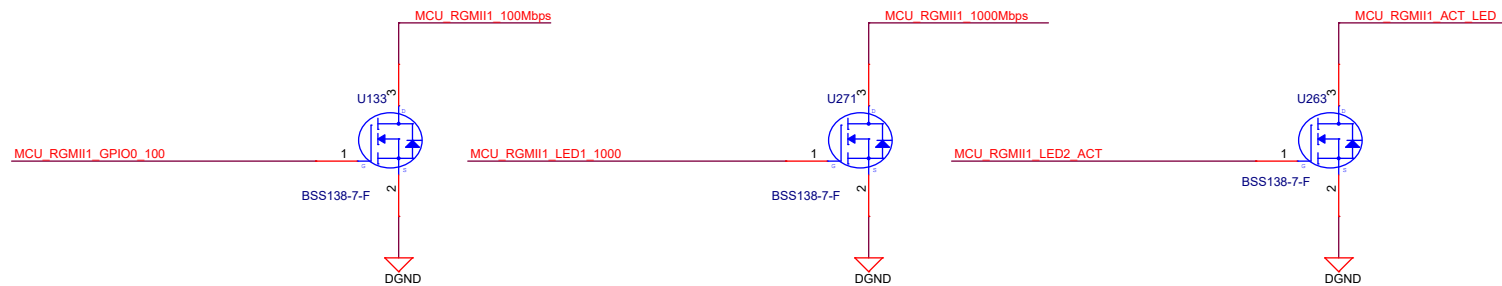
MCU GB ETHERNET



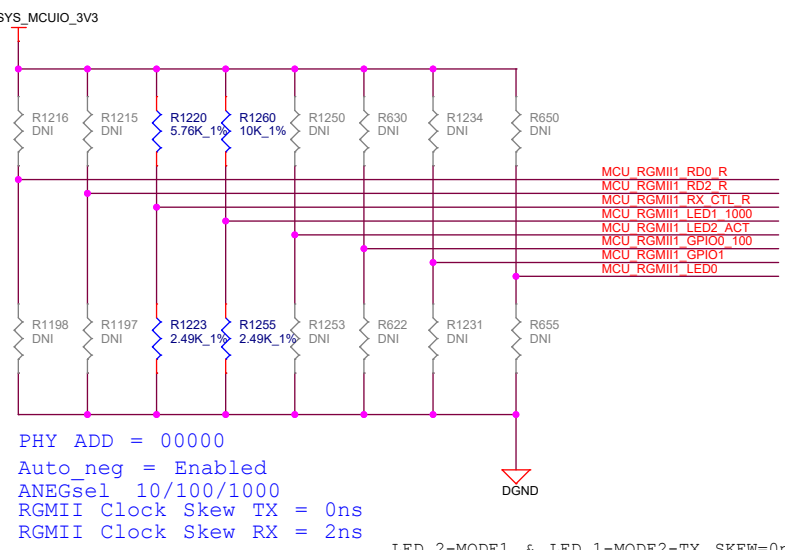
RESET LOGIC



SPEED AND ACTIVITY LED DRIVERS



RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

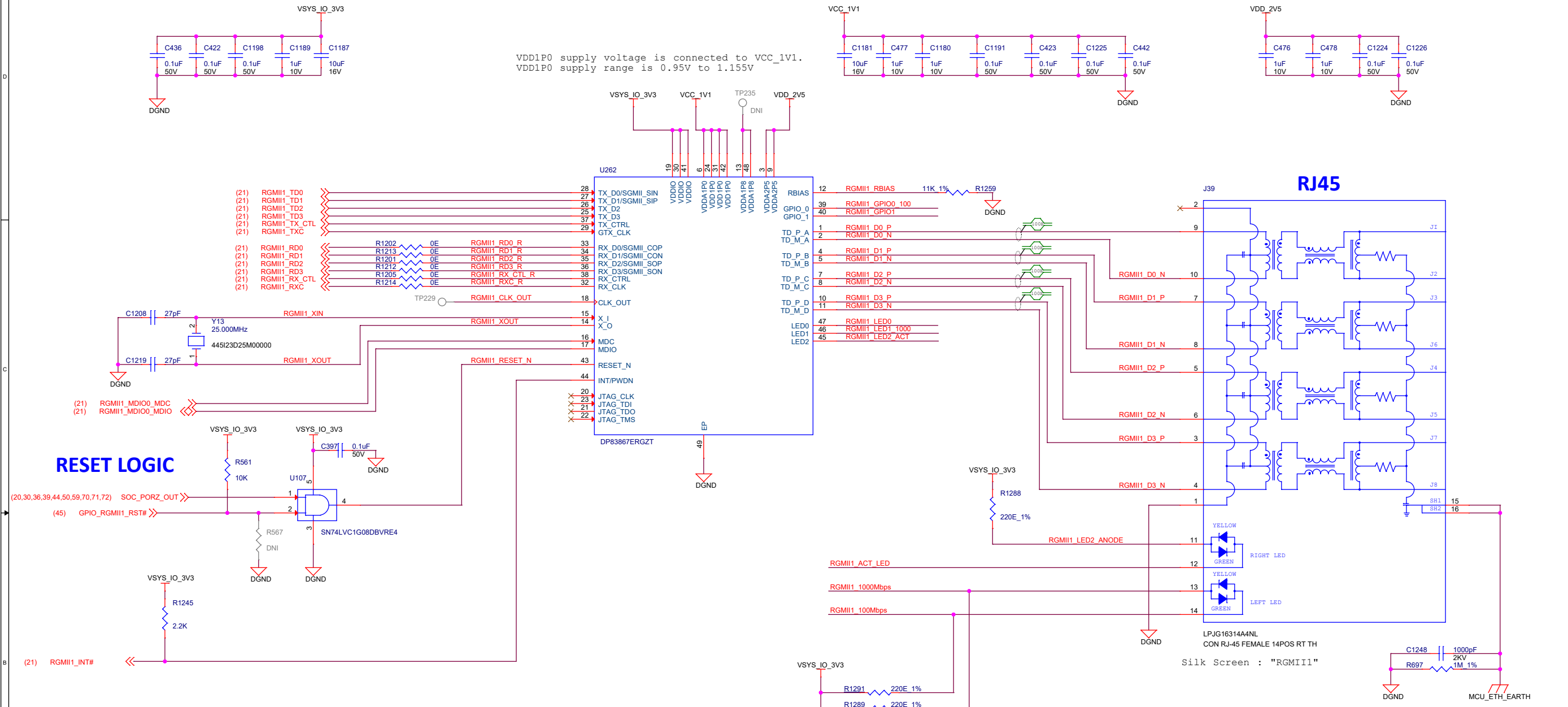


PHY ADD = 00000
Auto_neg = Enabled
ANEGsel 10/100/1000
RGMII Clock Skew TX = 0ns
RGMII Clock Skew RX = 2ns

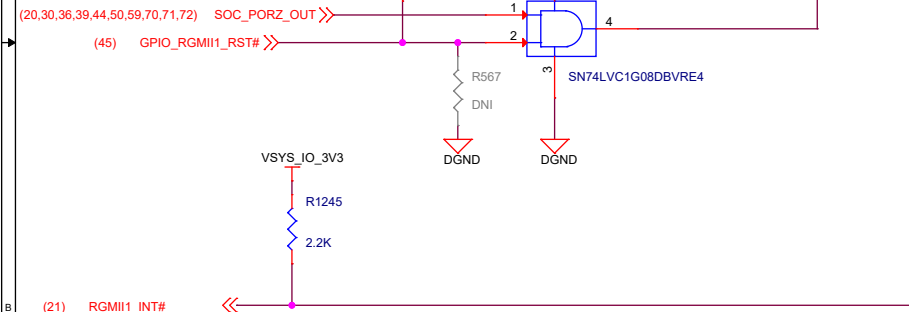
LED_2-MODE1 & LED_1-MODE2-TX SKEW=0ns
GPIO0-MODE1 & GPIO1-MODE1-RX SKEW=2ns

RGMII1

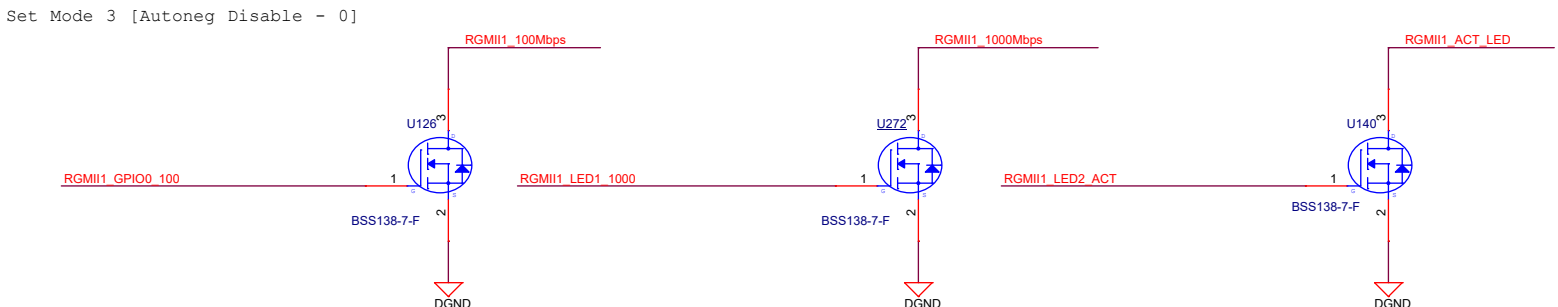
VDD1P0 supply voltage is connected to VCC_1V1.
VDD1P0 supply range is 0.95V to 1.155V



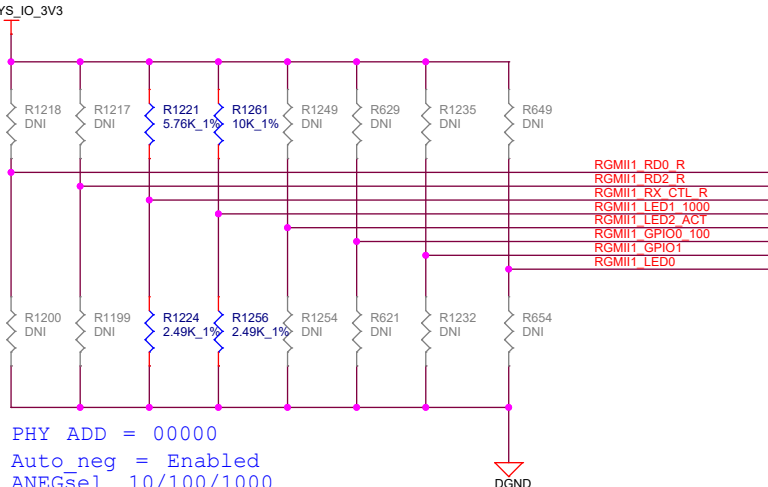
RESET LOGIC



SPEED AND ACTIVITY LED DRIVERS

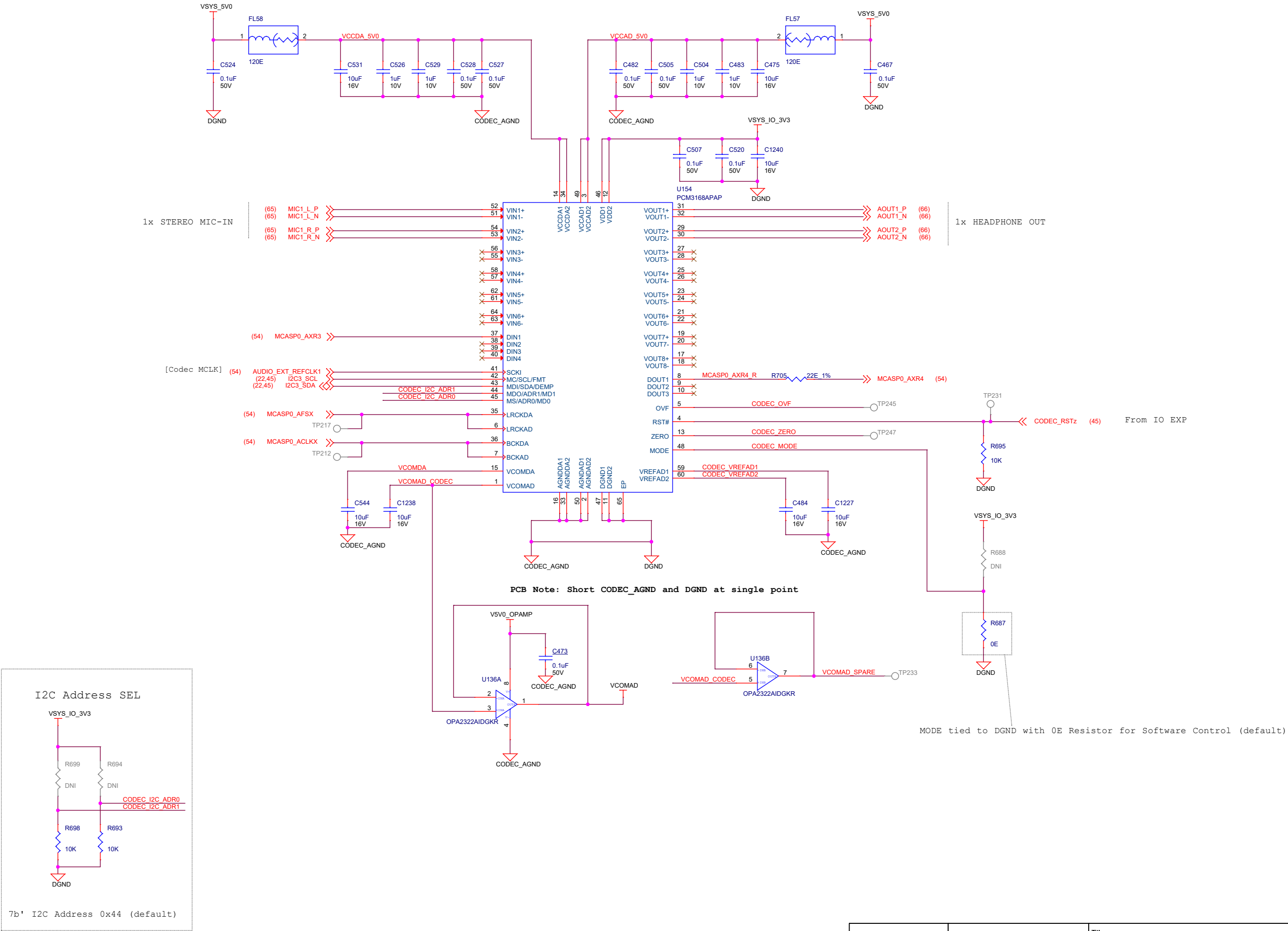


RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

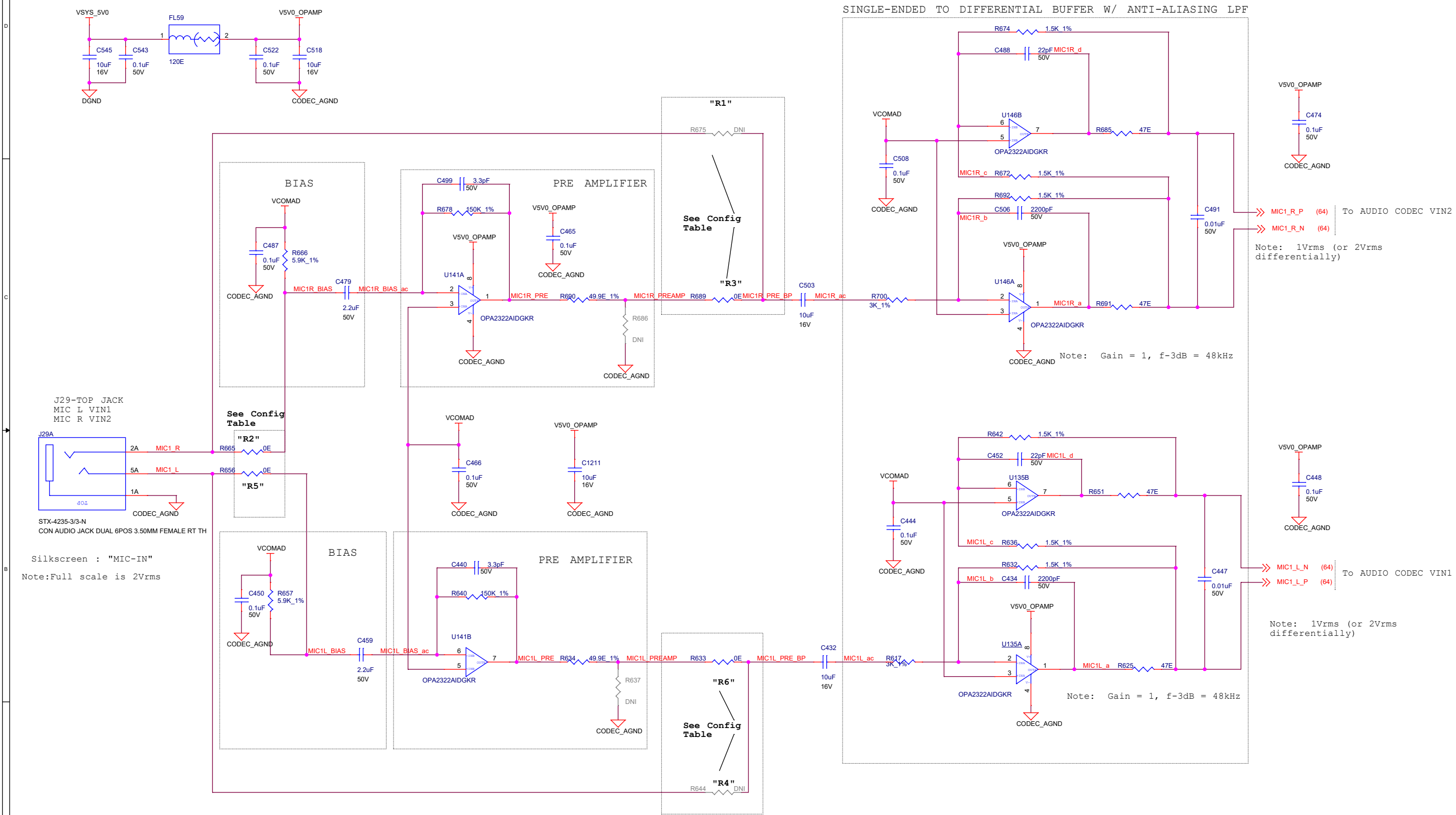


PHY ADD = 00000
Auto_neg = Enabled
ANEGsel 10/100/1000
RGMII Clock Skew TX = 0ns
RGMII Clock Skew RX = 2ns
LED_2-MODE1 & LED_1-MODE2-TX SKEW=0ns
GPIO0-MODE1 & GPIO1-MODE1-RX SKEW=2ns

AUDIO I/F CODEC

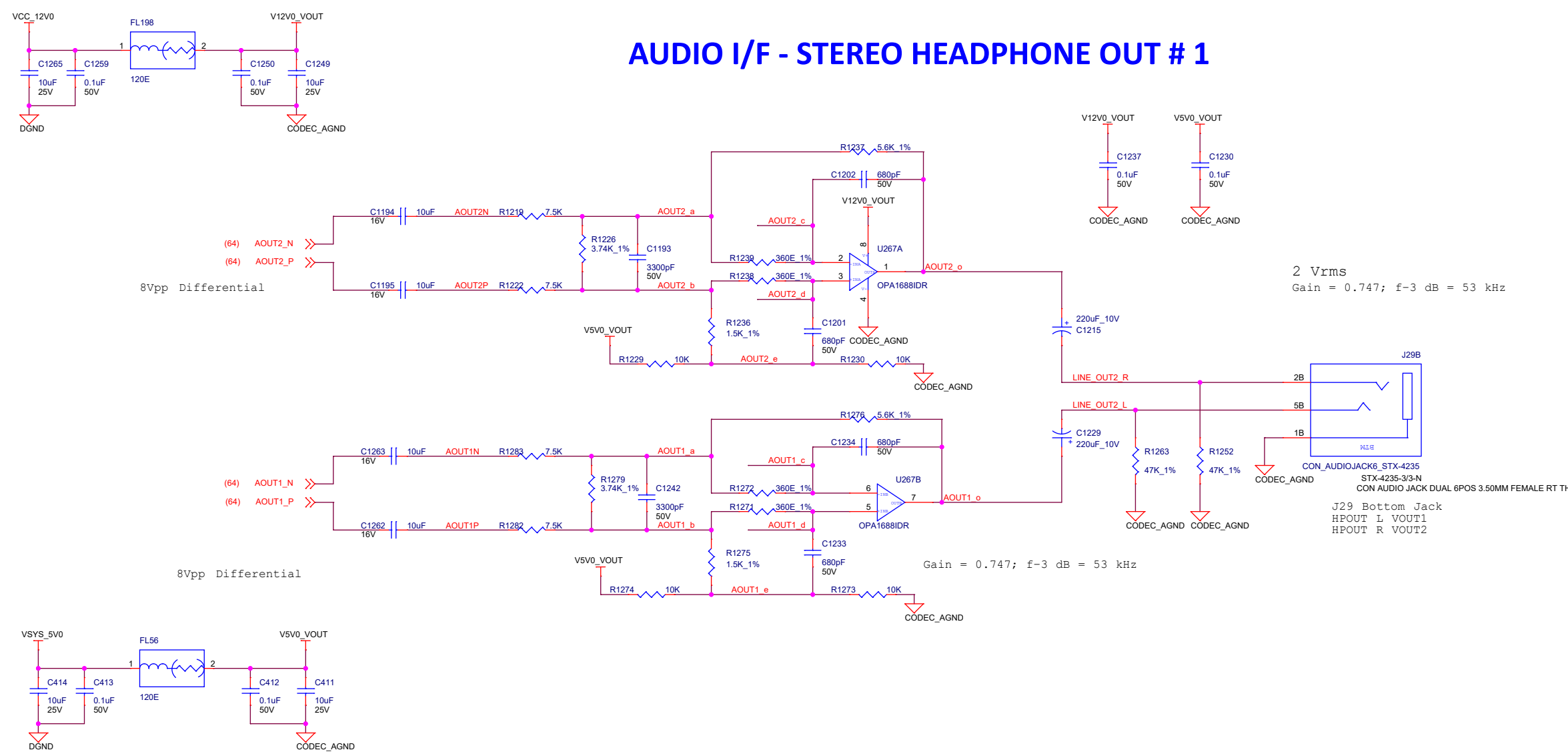


AUDIO I/F - STEREO MIC #1

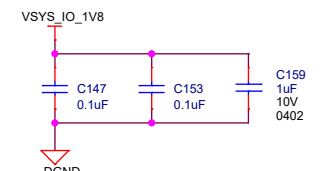
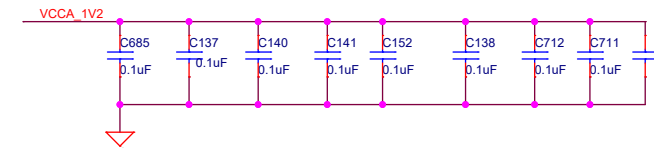
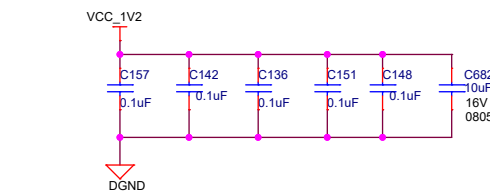
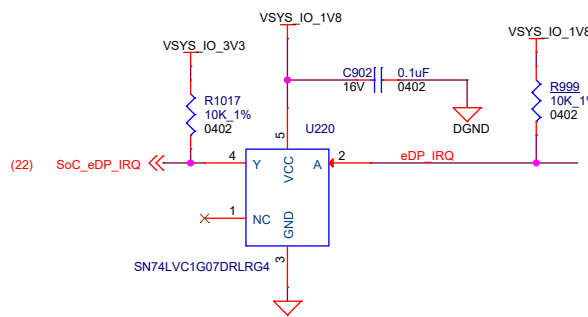
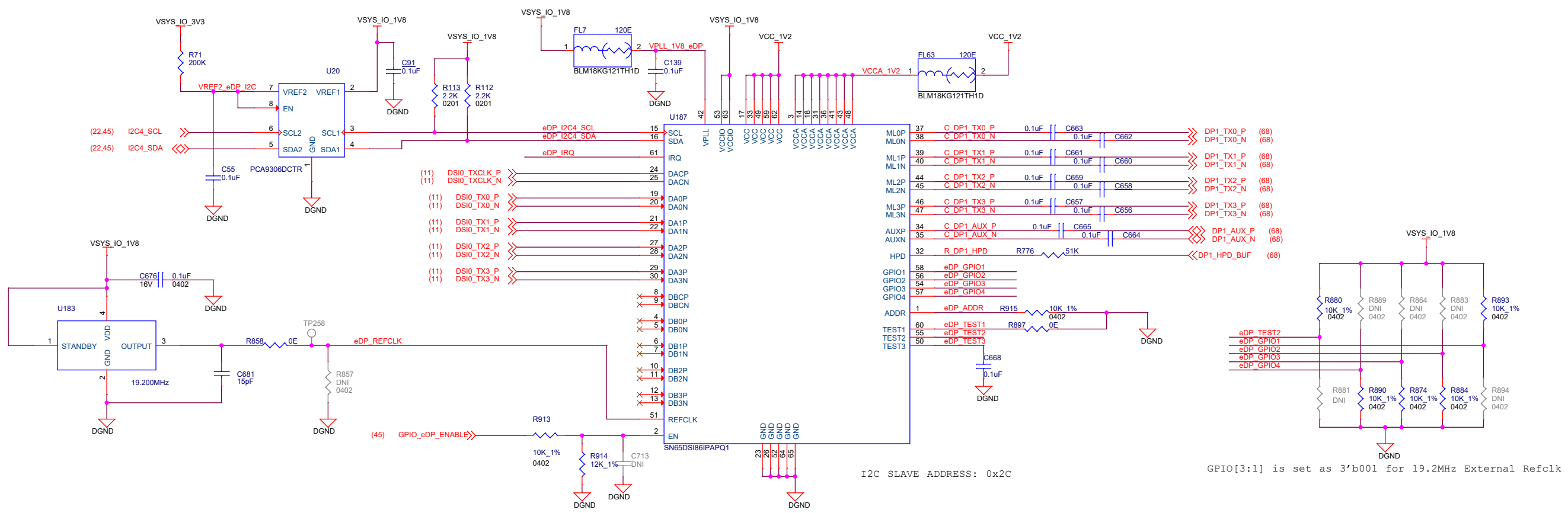


Config Table			
		Install	Remove
PASSIVE-MIC (default)	BIAS + PREAMP	R2,R3,R5,R6	R1,R4
ACTIVE-MIC	BIAS ONLY	R1,R2,R4,R5	R3,R6
LINE-INPUT	NO BIAS/PREAMP	R1,R4	R2,R3,R5,R6

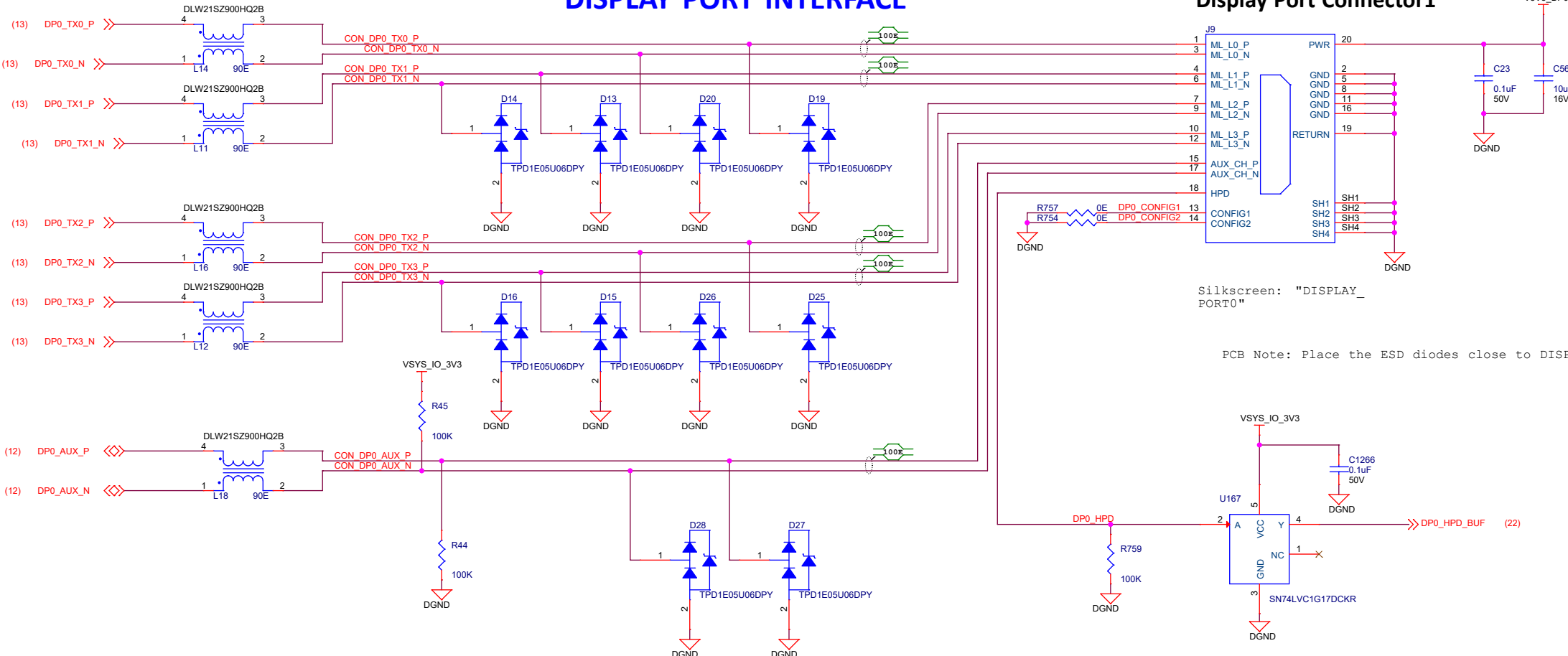
AUDIO I/F - STEREO HEADPHONE OUT # 1



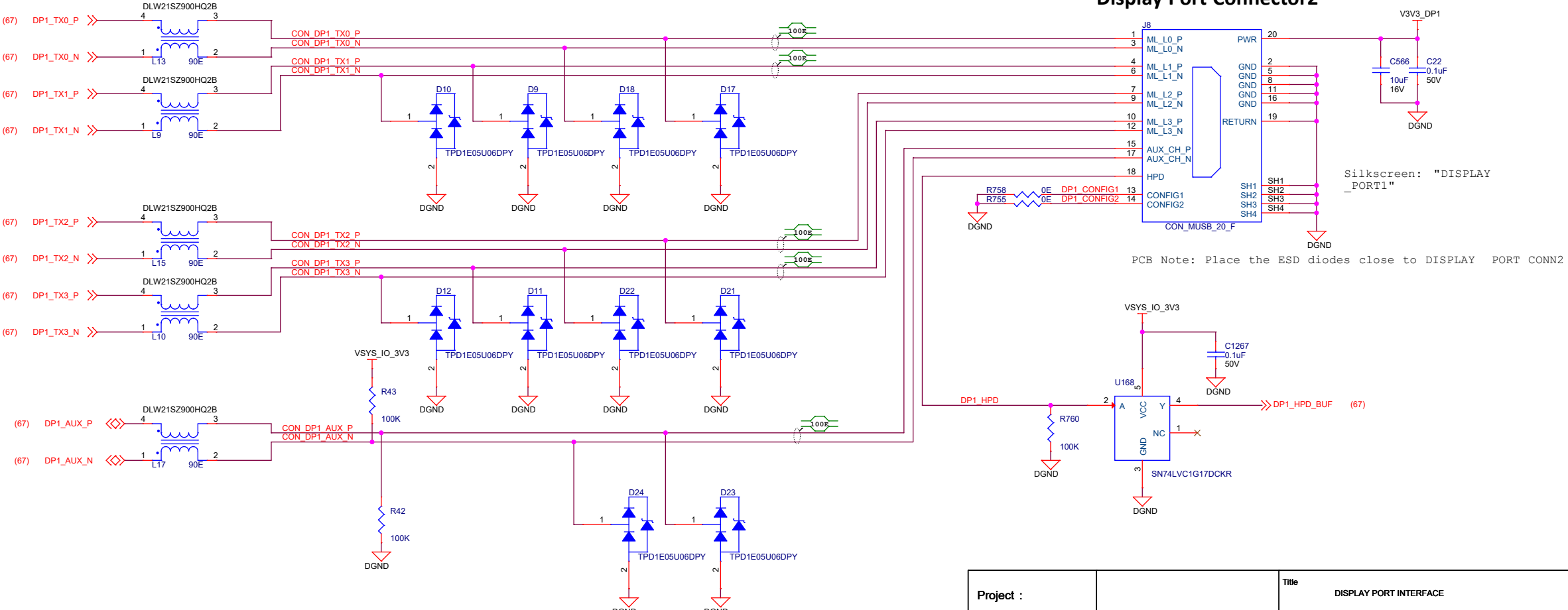
DSI to eDP Bridge



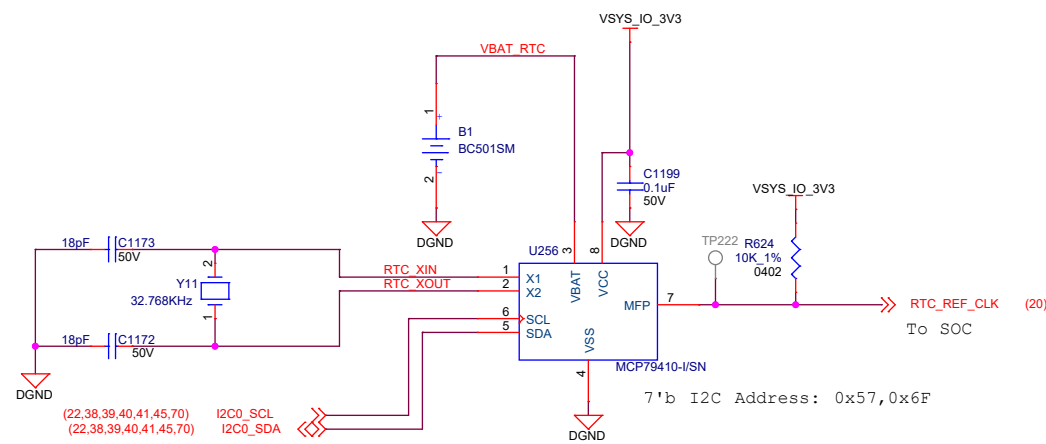
DISPLAY PORT INTERFACE



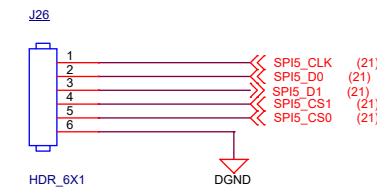
Display Port Connector



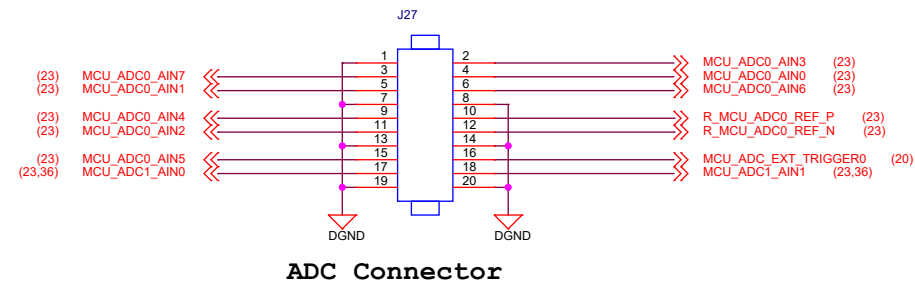
RTC



SPI Header



ADC INTERFACE



I3C Header

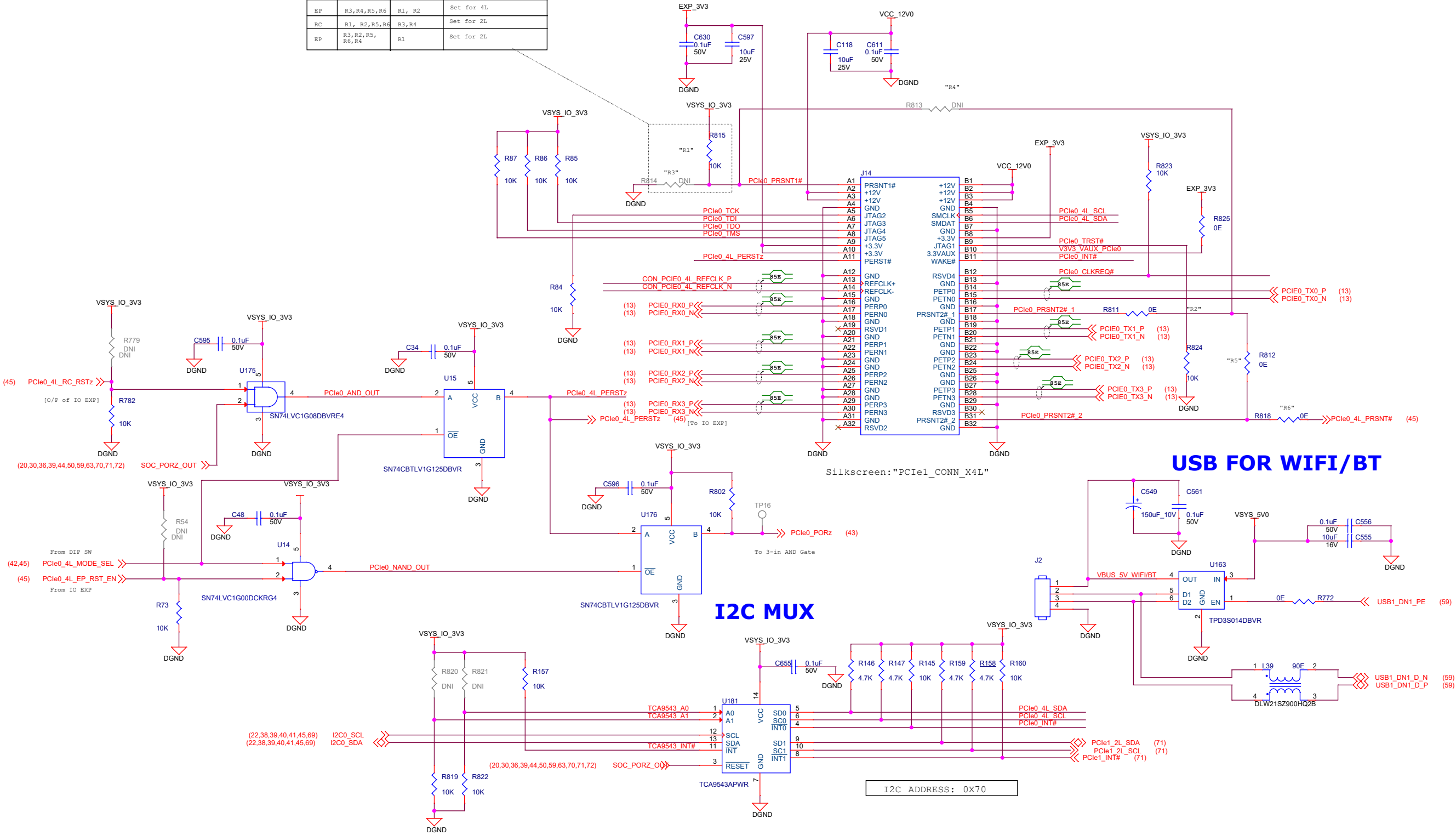


Silk Screen MCU-I3C

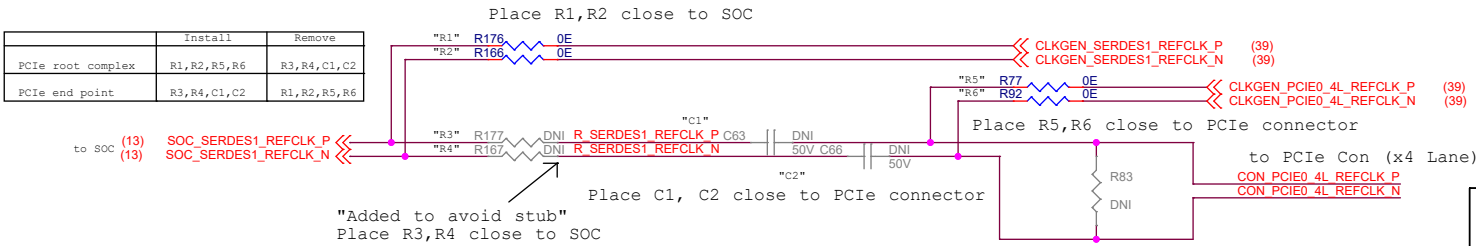
x4LANE PCIe0 Interface

x4 Lane PCIe Connector

MODE	INSTALL	DNI	PCie Lanes	(default)
RC	R1, R6	R3,R4,R2,R5	Set for 4L	
EP	R3,R4,R5,R6	R1, R2	Set for 4L	
RC	R1, R2,R5,R6	R3,R4	Set for 2L	
EP	R3,R2,R5, R6,R4	R1	Set for 2L	



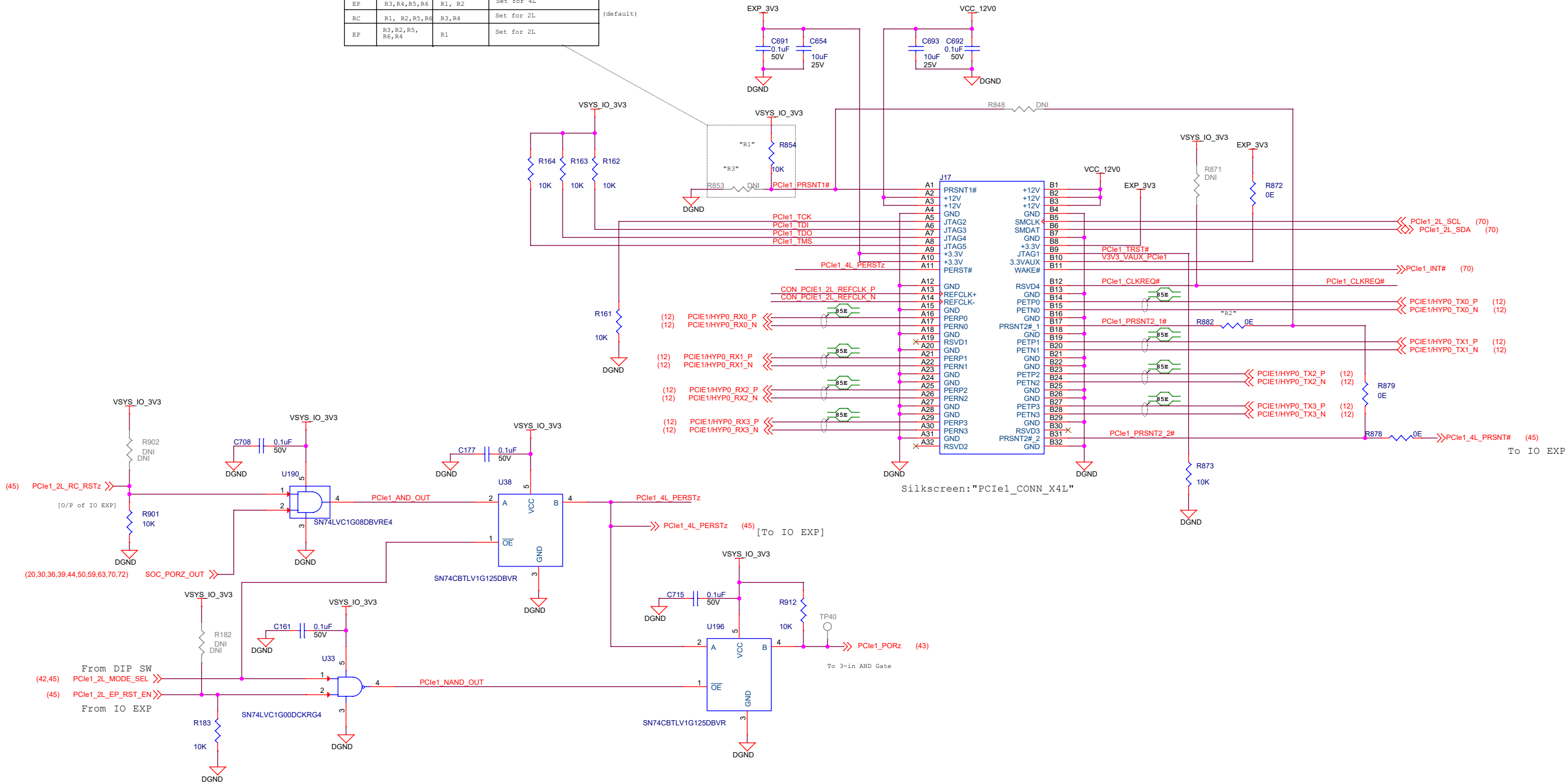
CLOCK ROOT SELECTION



x2LANE PCIe1 Interface(J17)
x4 Lane PCIe Connector

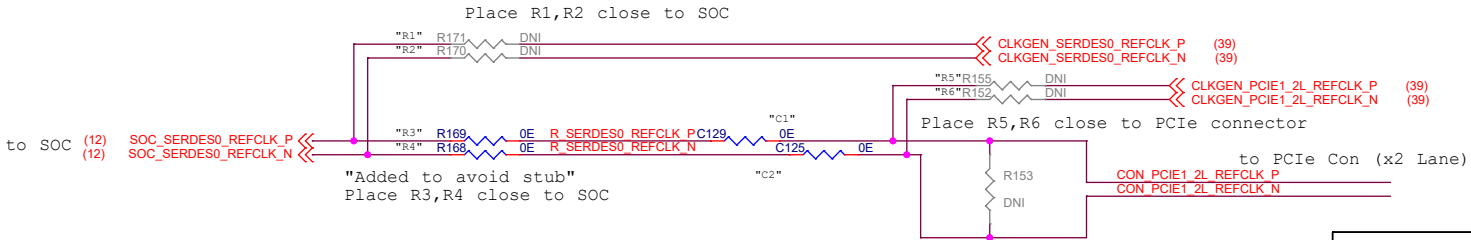
MODE	INSTALL	DNI	PCIe Lanes
RC	R1, R6	R3,R4,R2,R5	Set for 4L
EP	R3,R4,R5,R6	R1, R2	Set for 4L
RC	R1, R2,R5,R6	R3,R4	Set for 2L
EP	R3,R2,R5, R6,R4	R1	Set for 2L

(default)



CLOCK ROOT SELECTION

	Install	Remove
PCIe root complex	R1,R2,R5,R6	R3,R4,C1,C2
PCIe end point	R3,R4,C1,C2	R1,R2,R5,R6

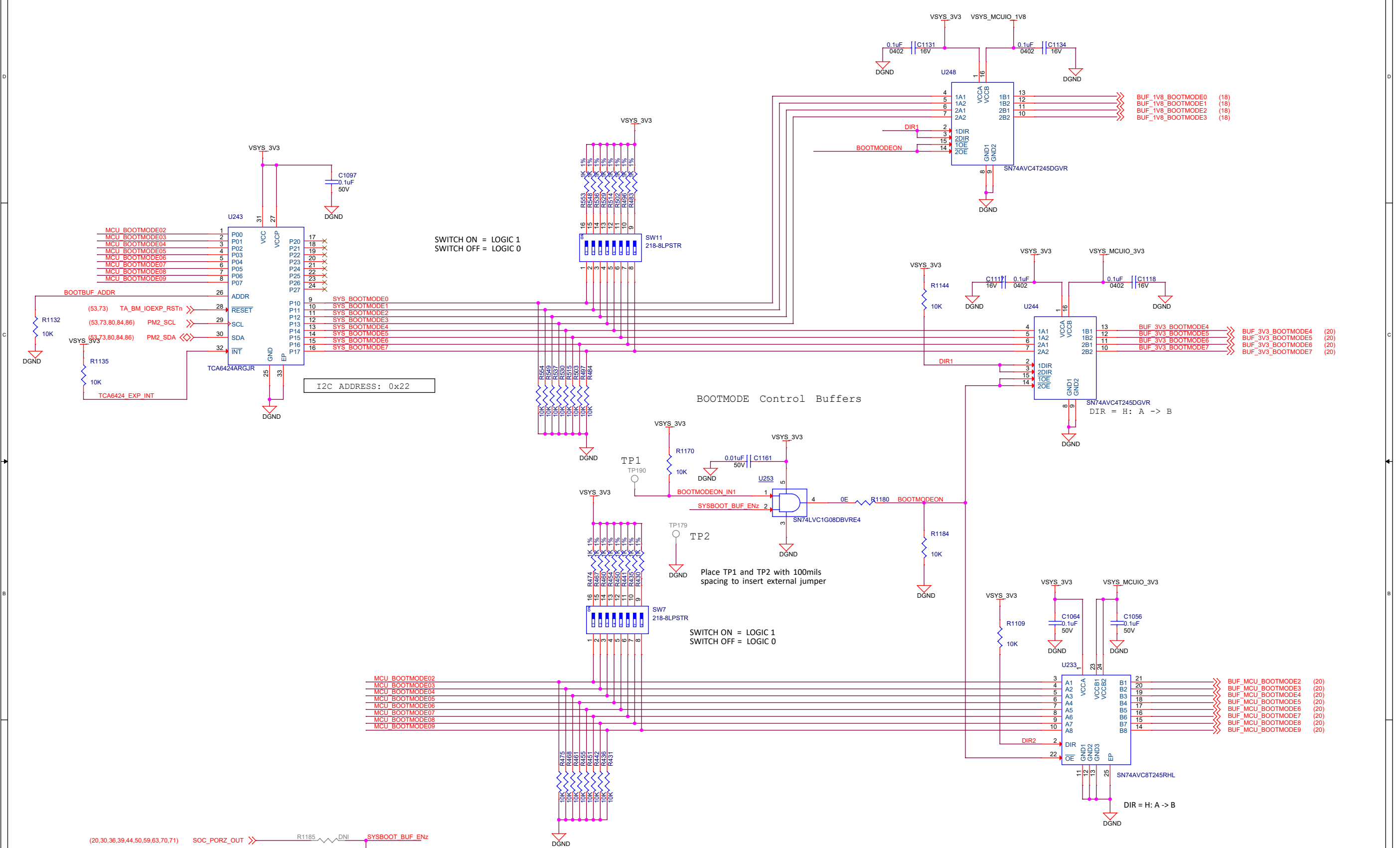


Project :
J7 EVM

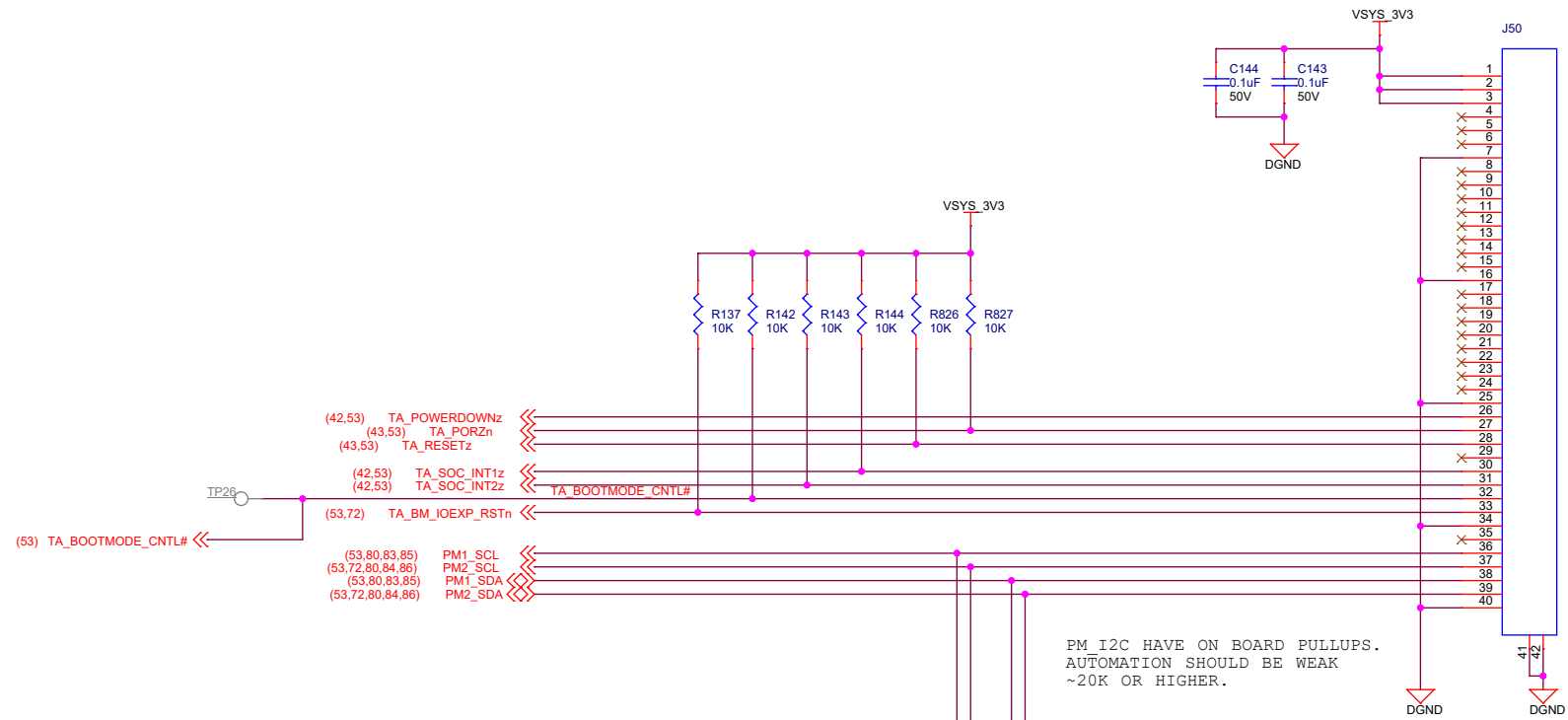


Title x2LANE PCIe Interface		
Size C	PROC184 002	Rev E1
Date: Friday, May 17, 2024	Sheet 68 of 84	

BOOT MODE BUFFER & SWITCHES



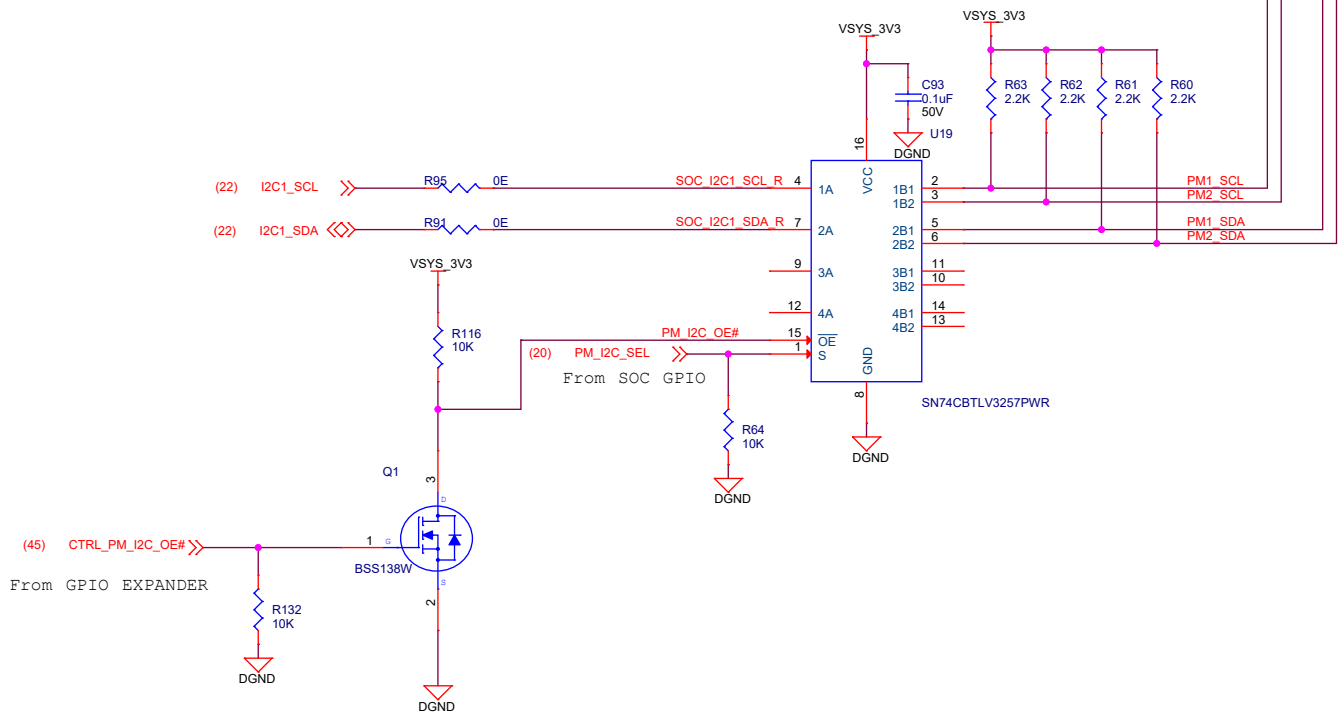
TEST AUTOMATION HEADER



AUTOMATION INTERFACE

ALL SIGNALS SHOULD BE REFERENCED TO EVM_3V3
Cable : Parlex-050R40-76B, .5mm 3"
Silkscreen:"AUTOMATION CONNECTOR"

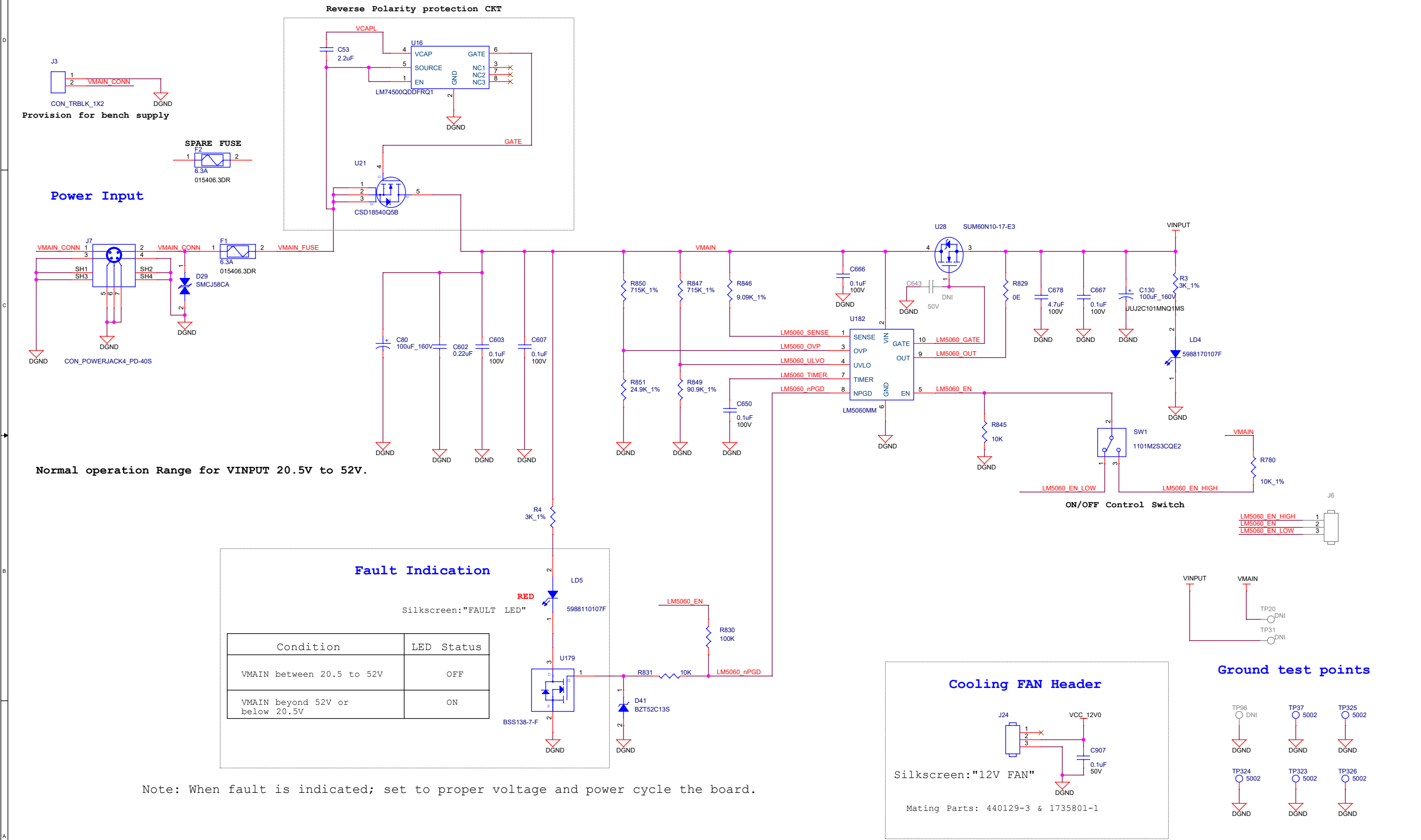
I2C SWITCH



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

OVER VOLTAGE PROTECTION CIRCUIT



Project :

J7 EVM



Title

OVER VOLTAGE PROTECTION CKT

Size

PROC184 002

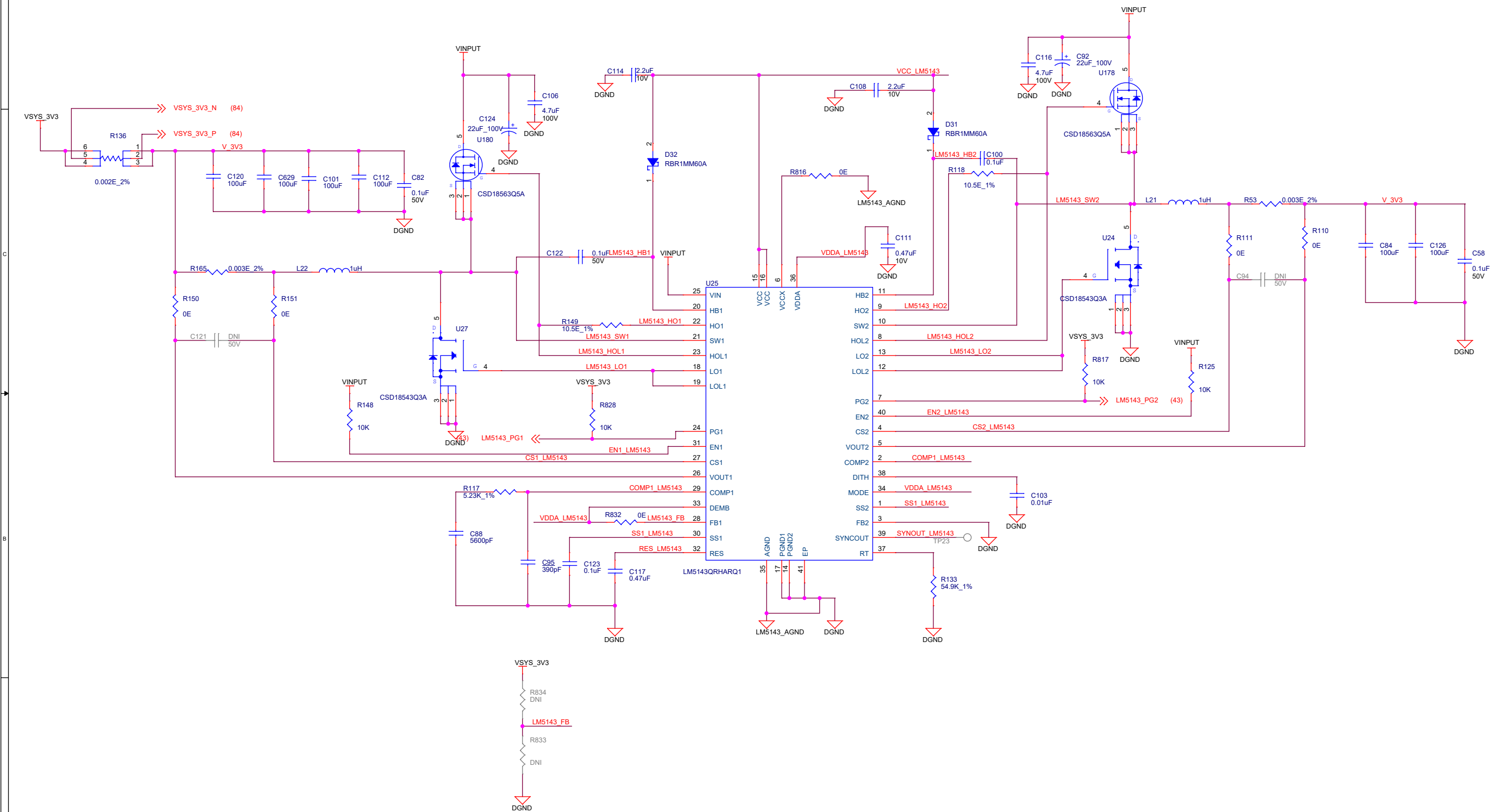
Rev

E1

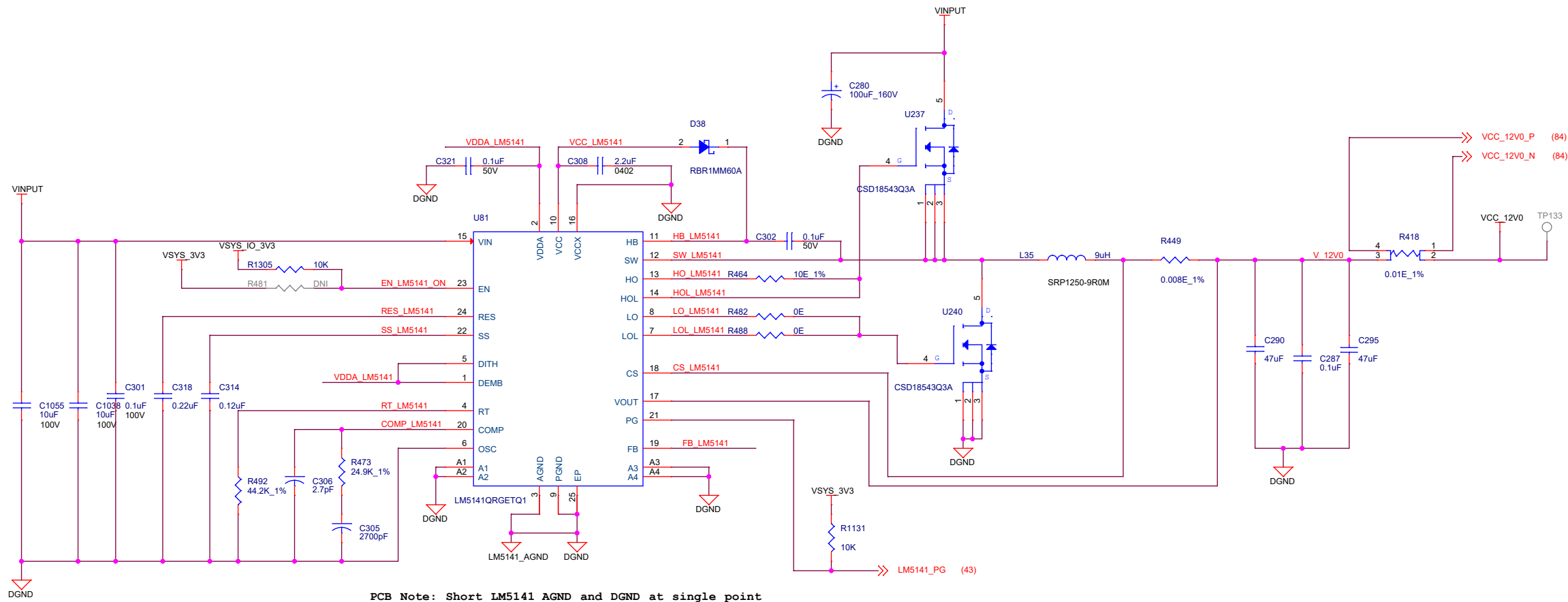
Date: Friday, May 17, 2024

Sheet 71 of 84

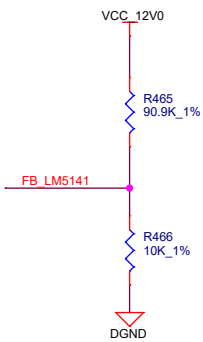
POWER SUPPLY #1



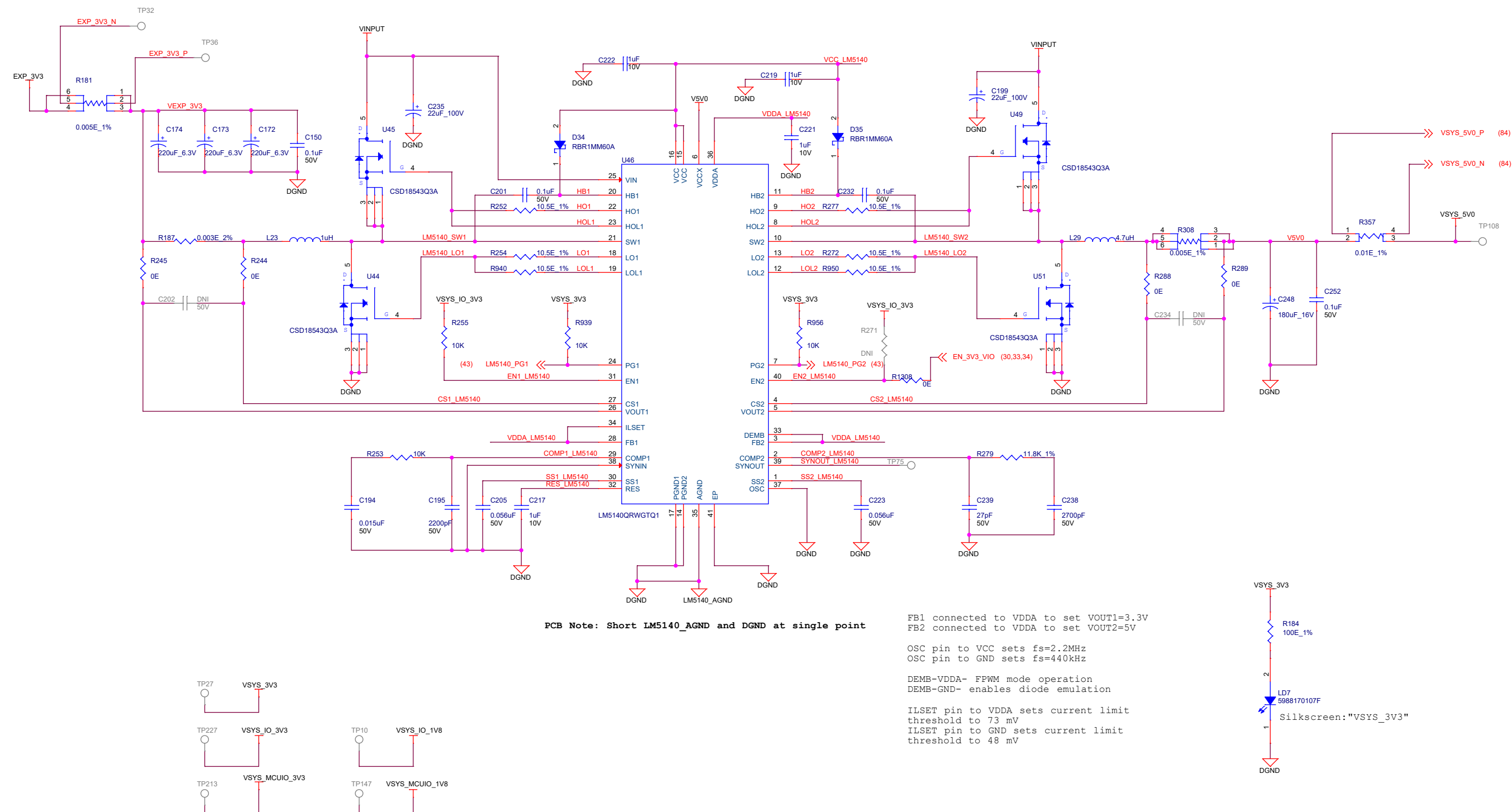
POWER SUPPLY #2



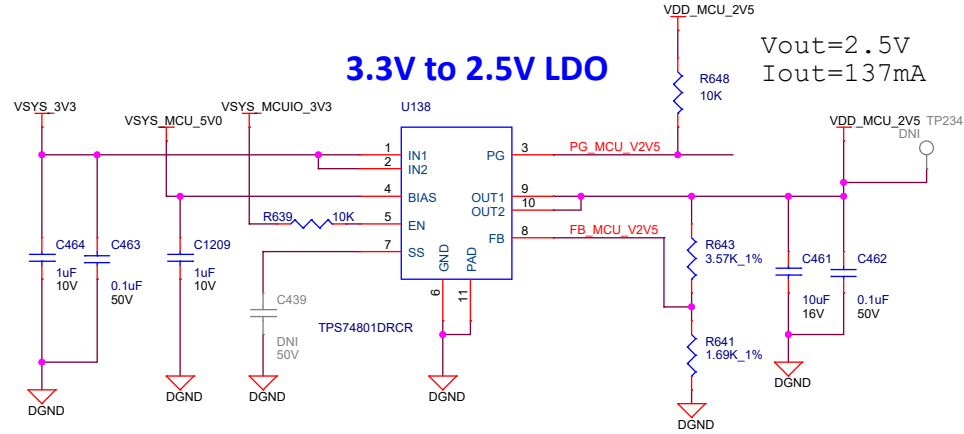
PCB Note: Short LM5141_AGND and DGND at single point



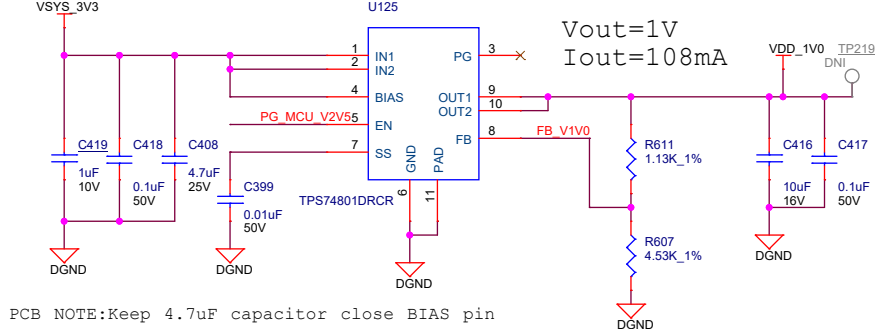
POWER SUPPLY #3
3.3V AND 5V GENERATION



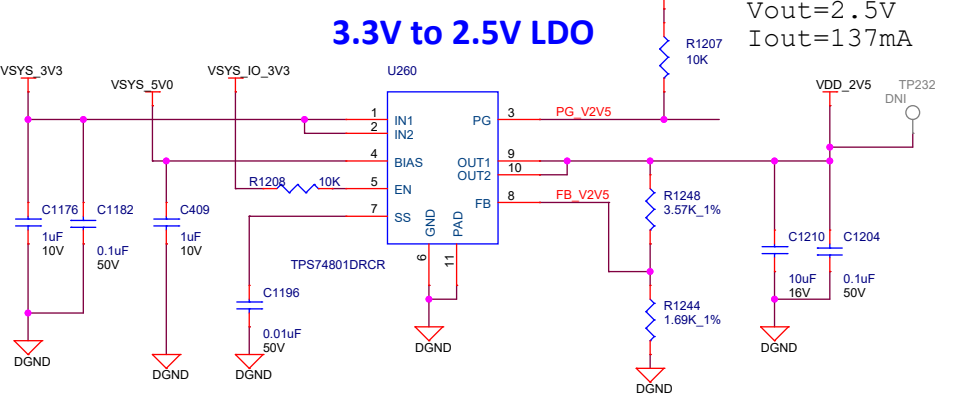
ETHERNET POWER- MCU RGMII



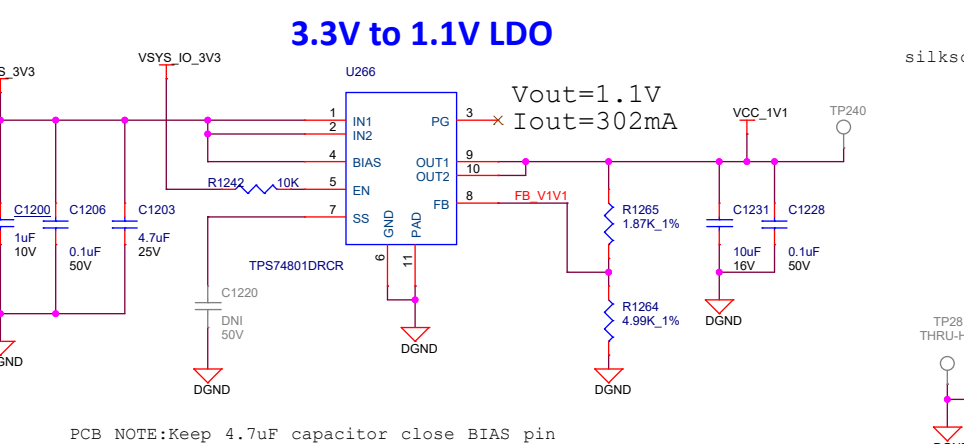
3.3V to 1.0V LDO



ETHERNET POWER- RGMII1

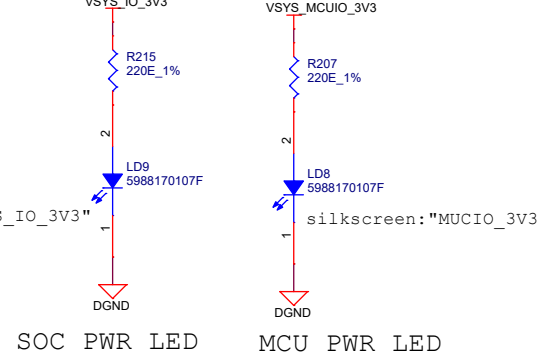


USB HUB POWER & ETHERNET POWER - RGMII1

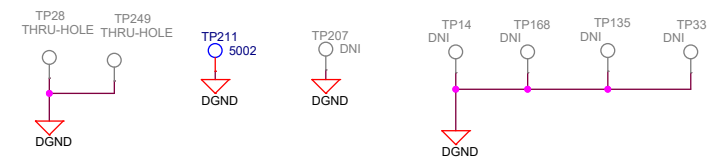


POWER SUPPLY #4

POWER INDICATION LED's

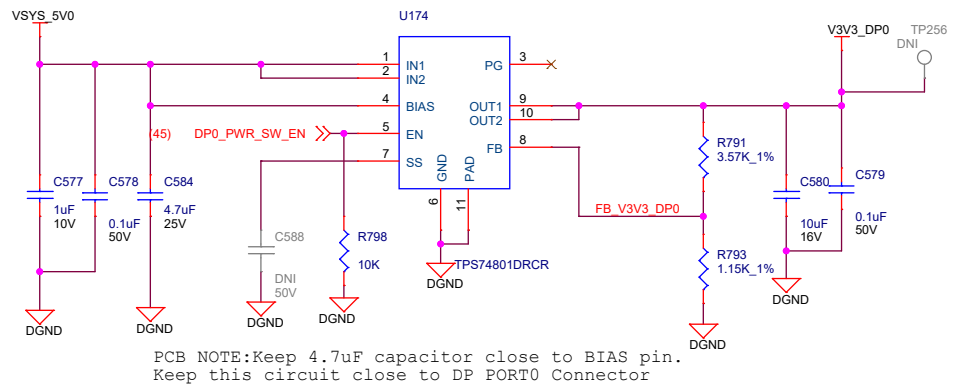


GROUND TEST POINTS

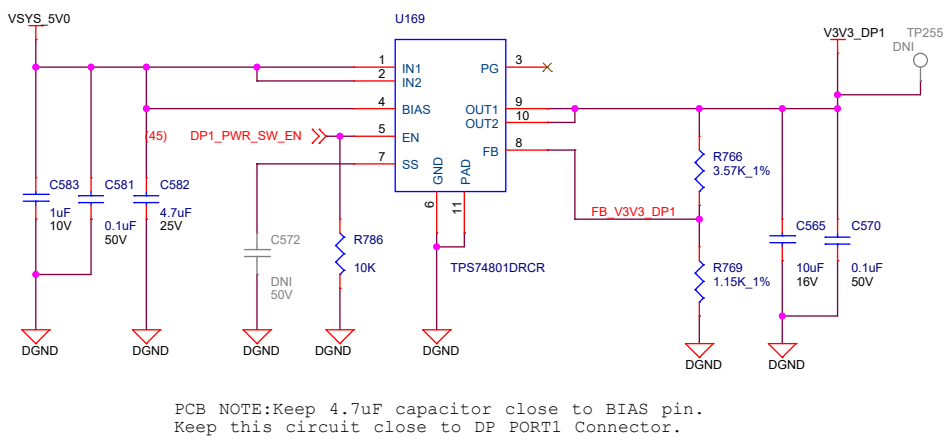


Display Port0

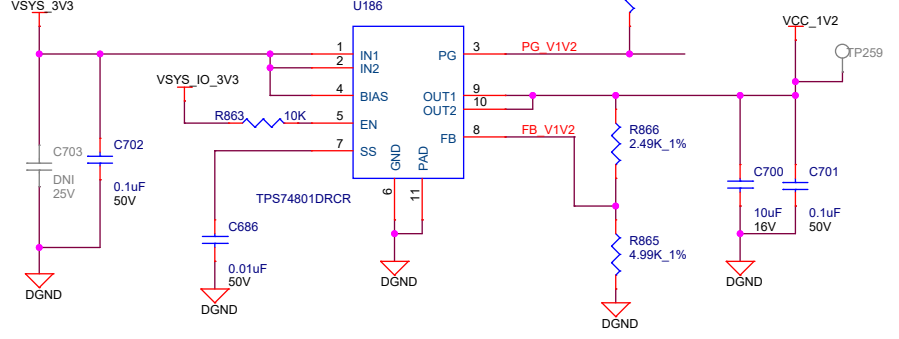
5V to 3.3V LDO



Display Port1
5V to 3.3V LDO

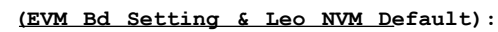


3.3V to 1.2V LDO

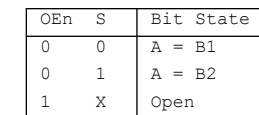


PCB NOTE: Spread the SMD test points Top and Bottom Side of PCB

EVM development & evaluation Test circuitry
(TI EVM Only)

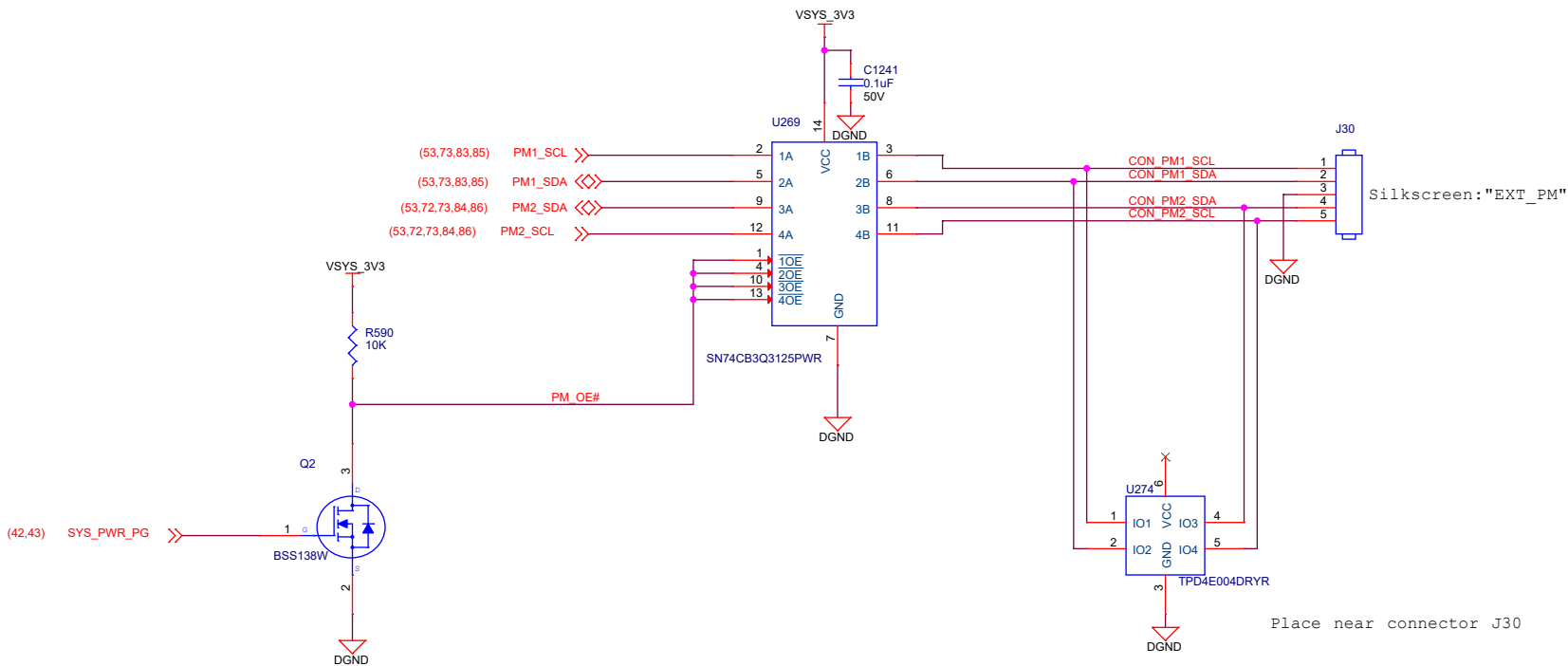


OEn	S	Bit State
0	0	A = B1
0	1	A = B2
1	X	Open



EVM POWER MEASUREMENT I2C BUS ISOLATION

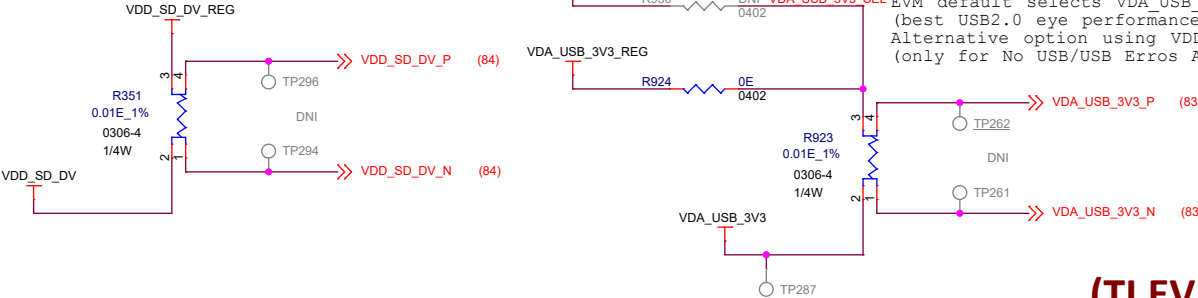
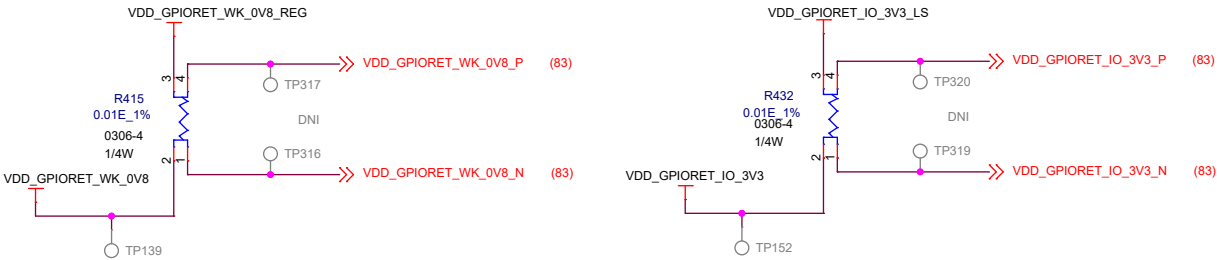
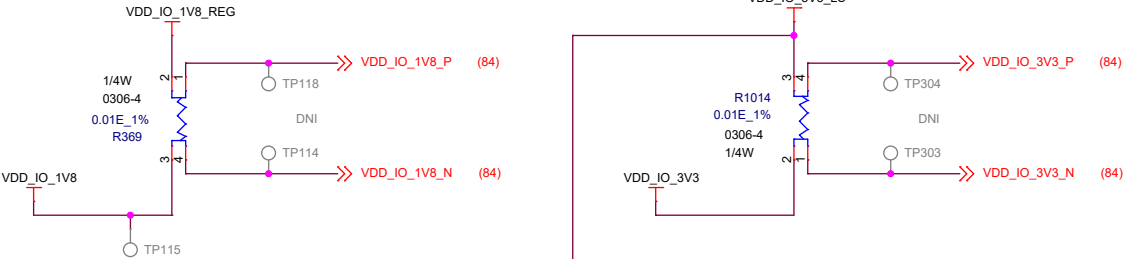
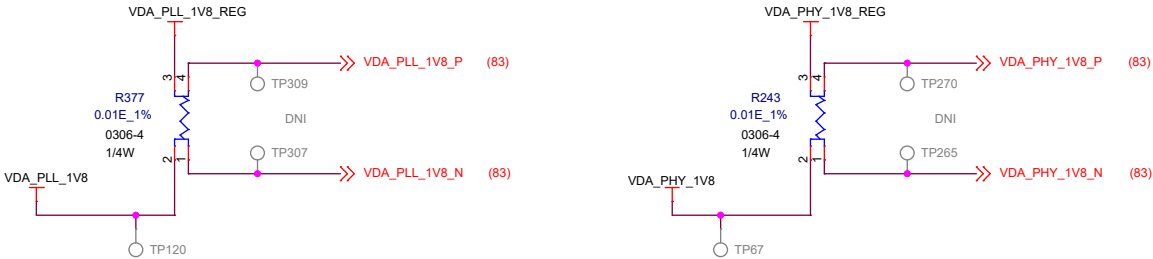
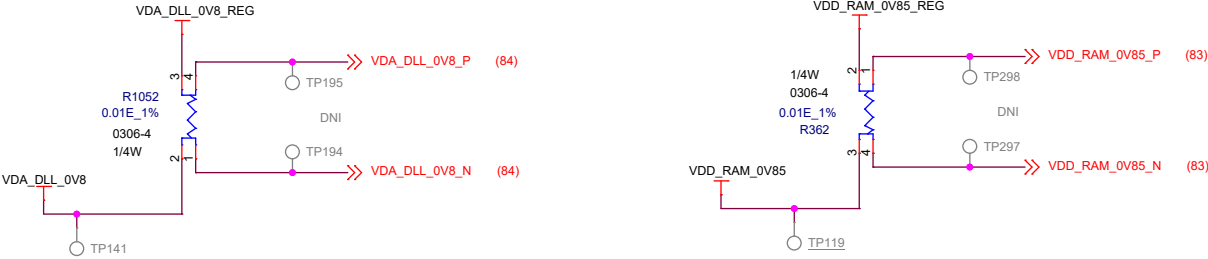
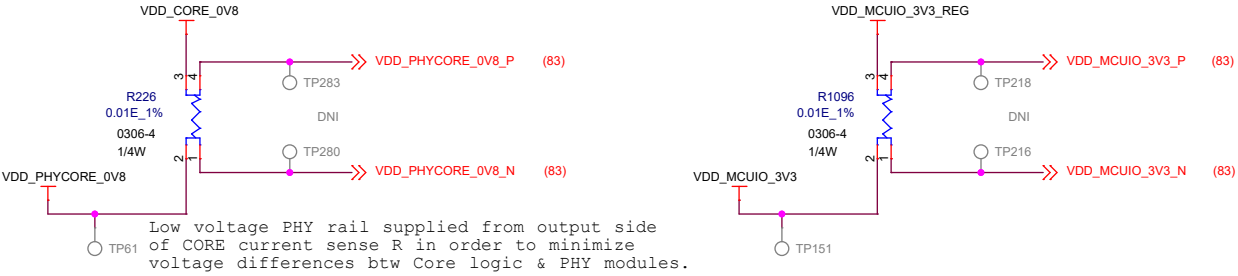
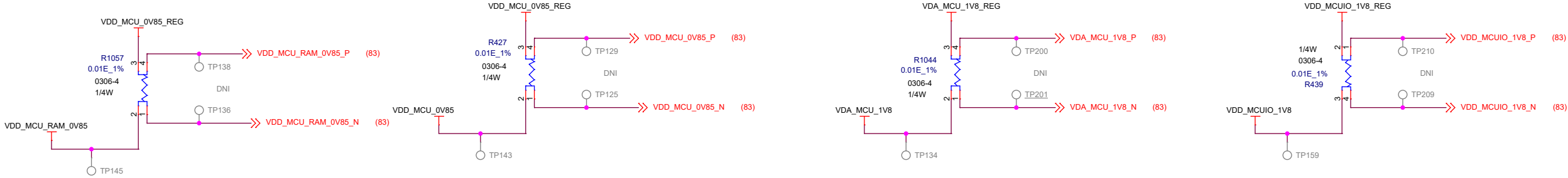
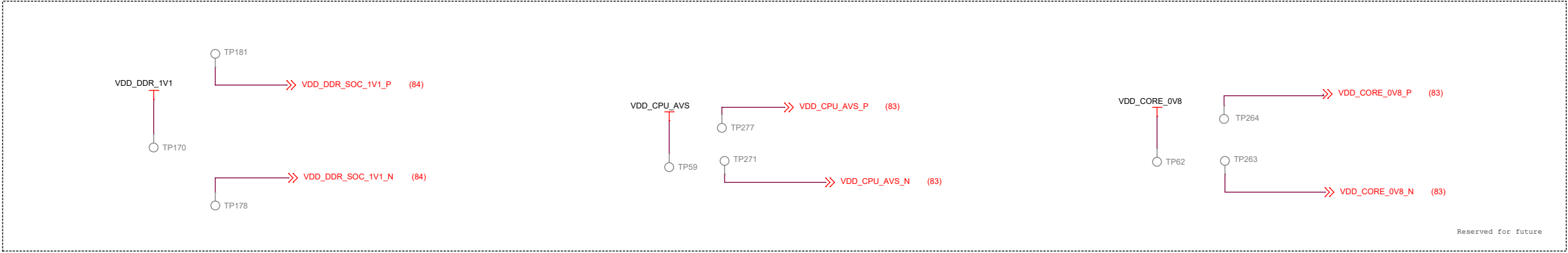
EVM development & evaluation Test circuitry
(TI EVM Only)



(TI EVM Only)

SOC Current Sense Resistors

(TI EVM Only)



(TI EVM Only)

(TI EVM Only)

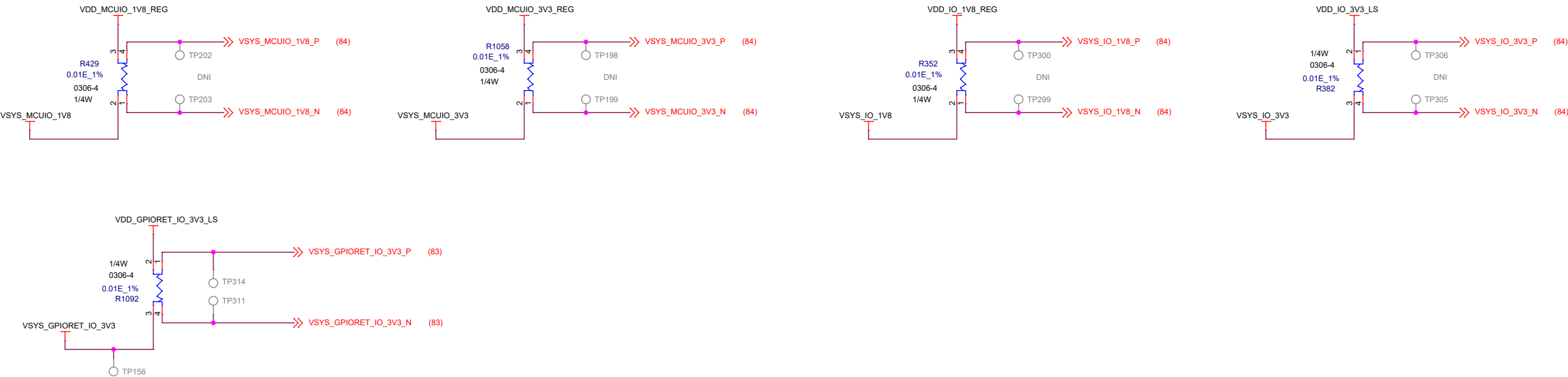
Project : J7 EVM		Title SOC Current Sense Resistors	
Size C		PROC184 002	Rev E1
Date: Wednesday, February 07, 2024		Sheet 78 of 84	

EVM development & evaluation test circuitry

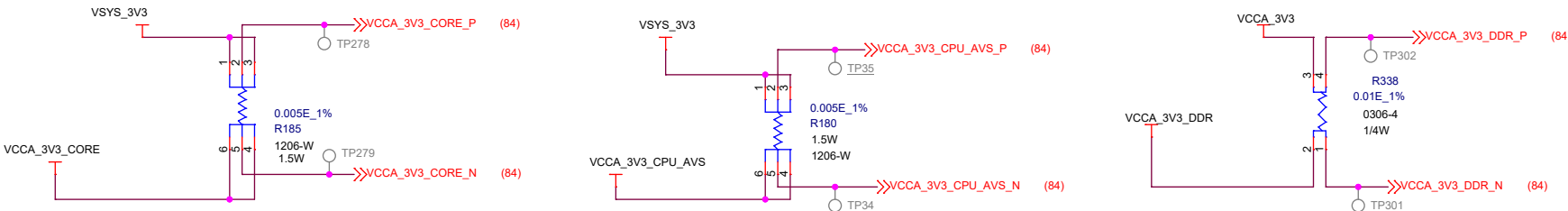
LPDDR4 SDRAM Current Sense Resistors



Peripheral Current Sense Resistors

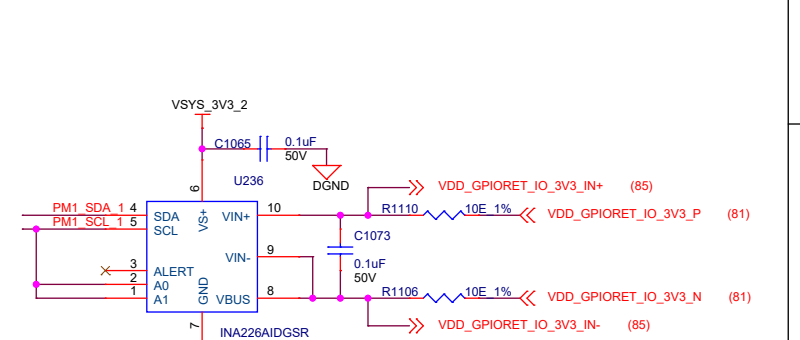
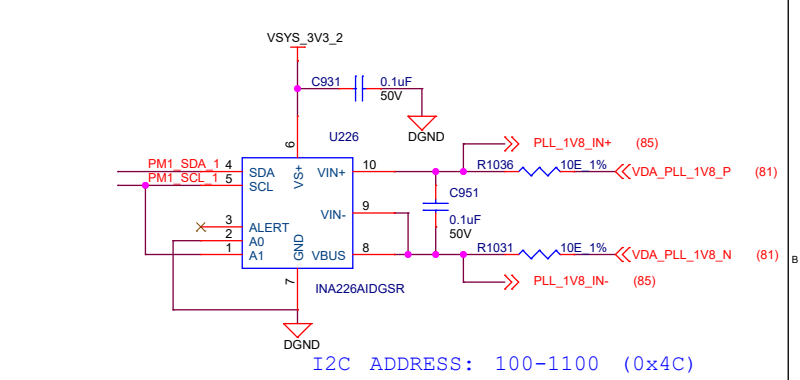
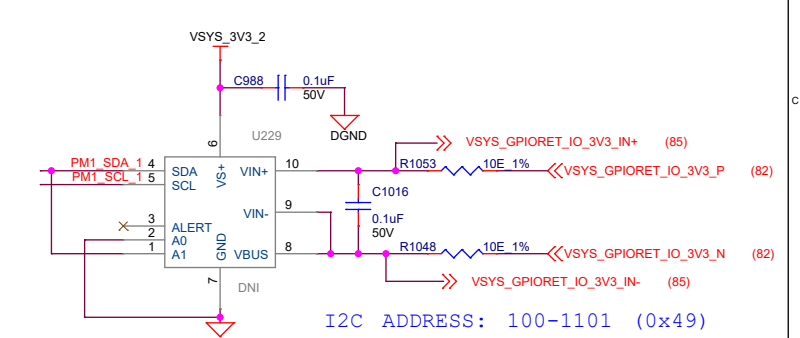
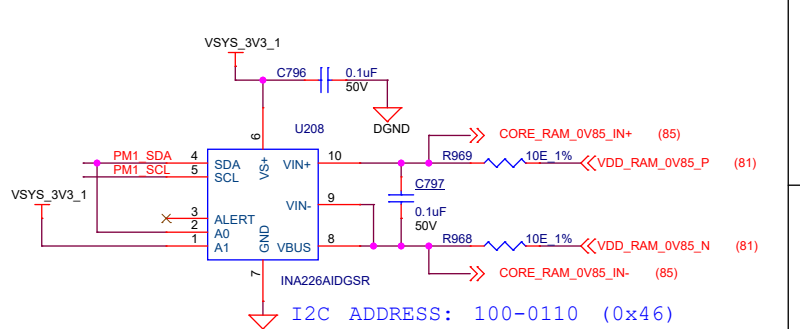
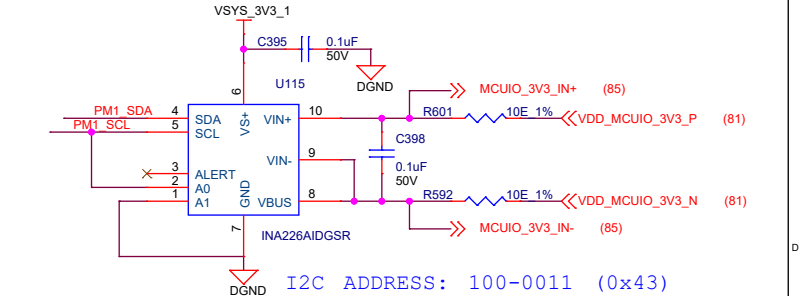
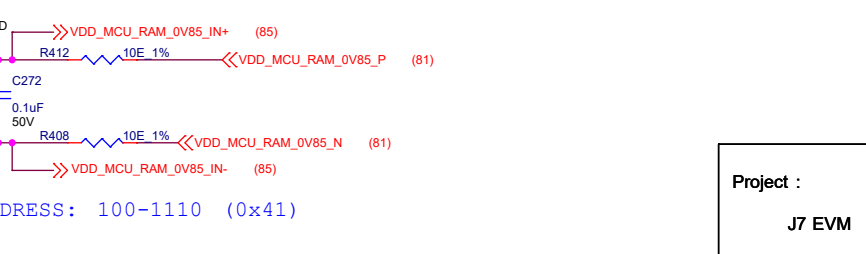
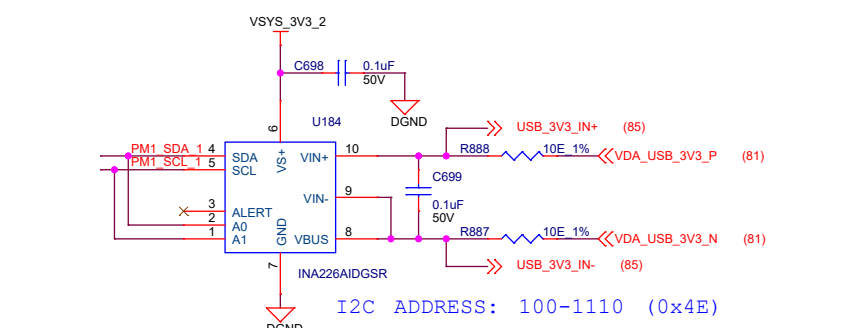
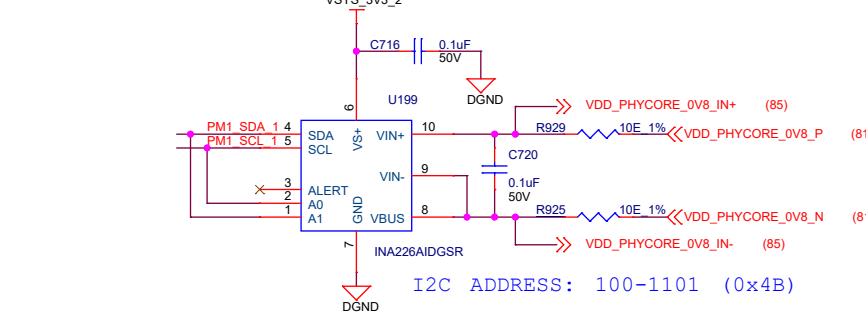
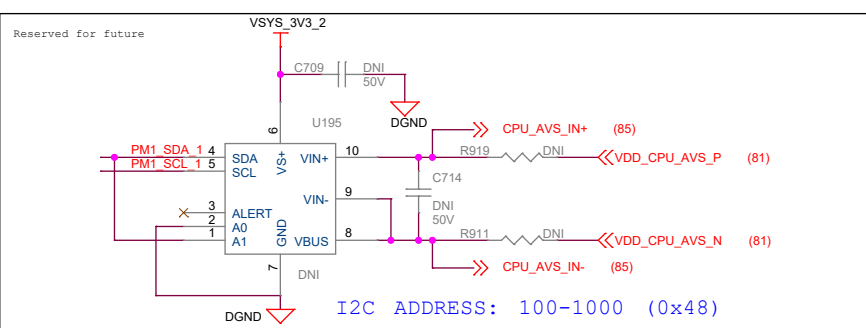
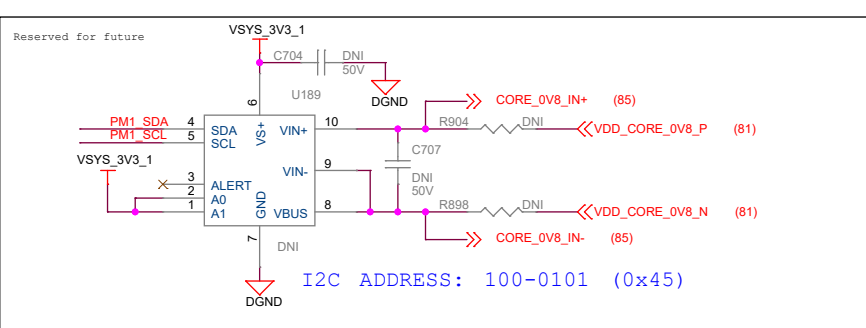
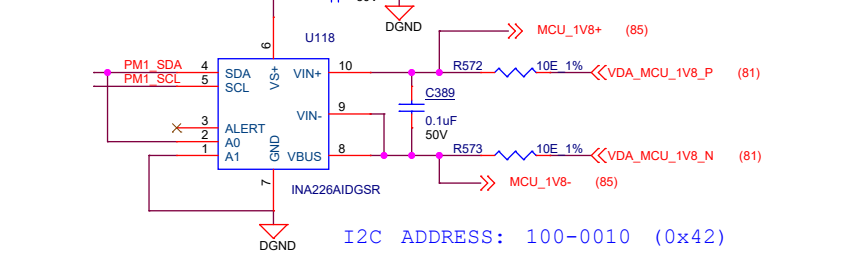
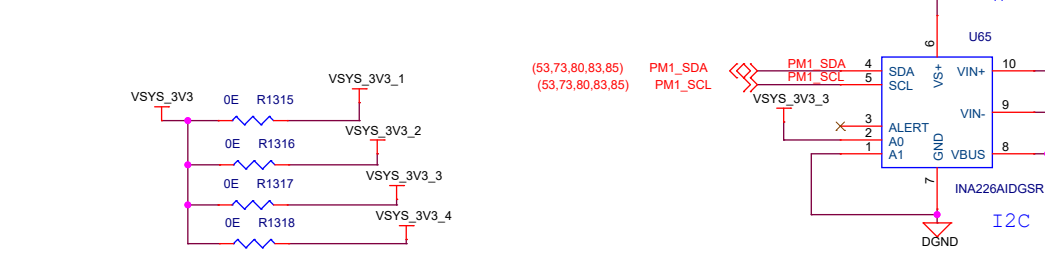
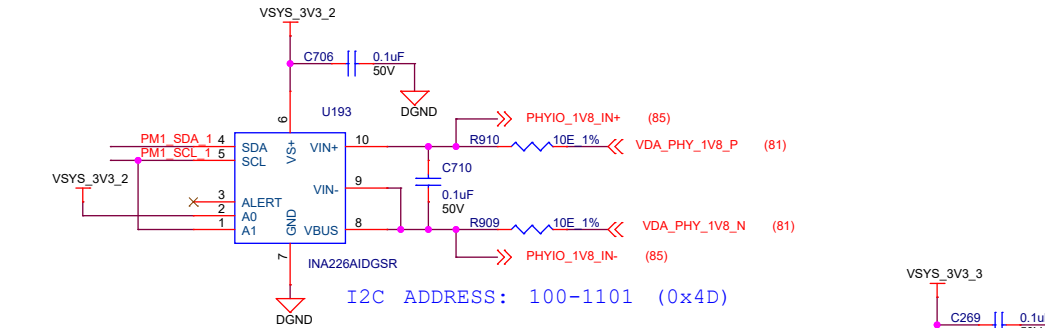
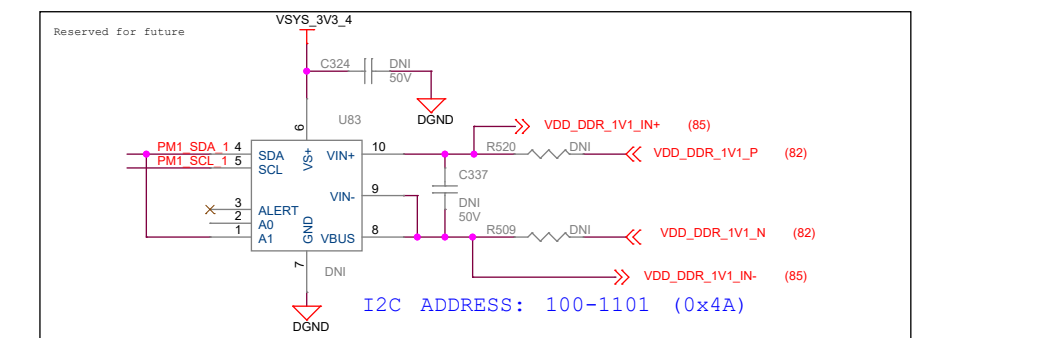
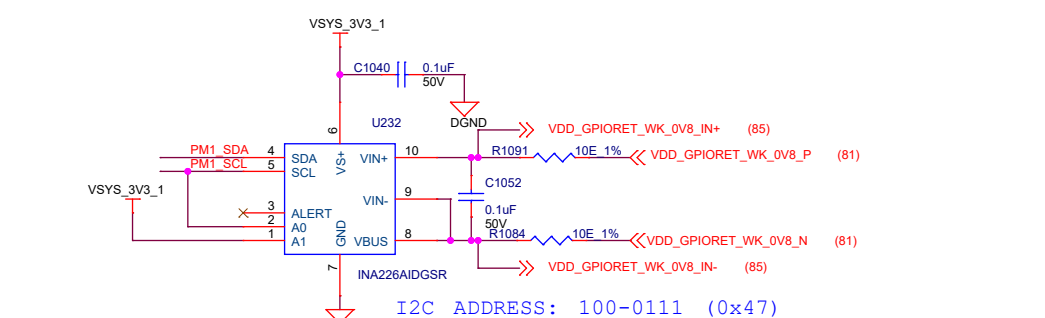
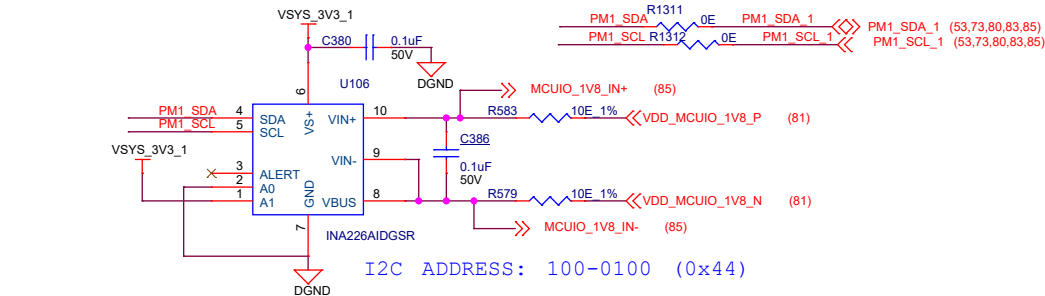
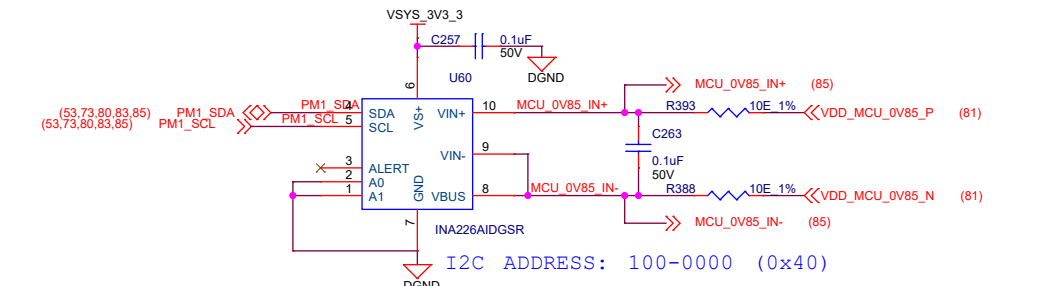


CORE, AVS and DDR input supply sense resistors

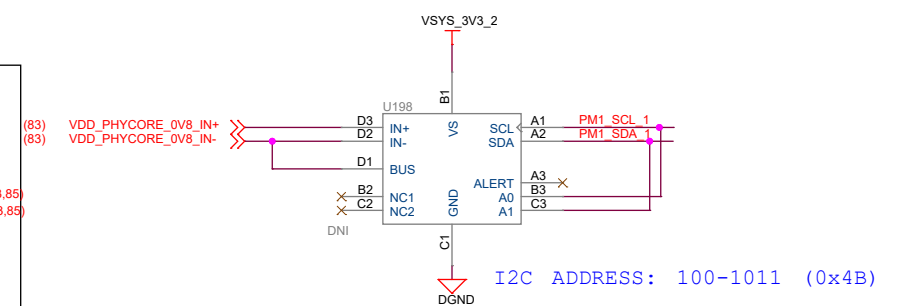
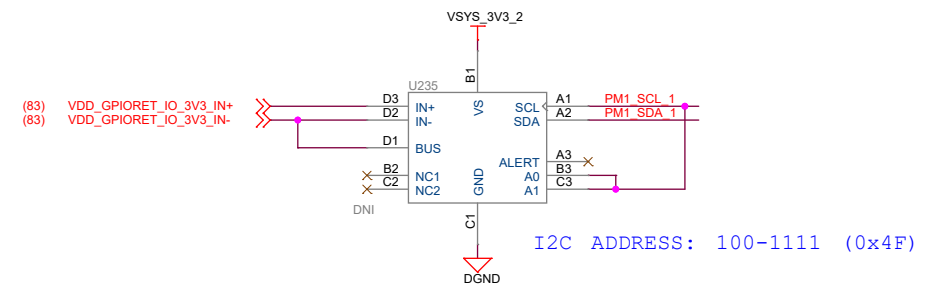
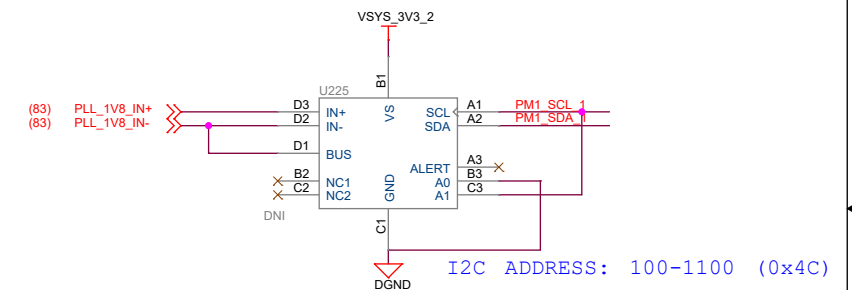
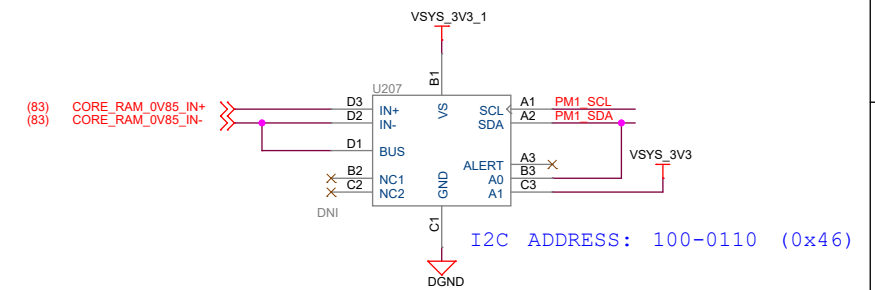
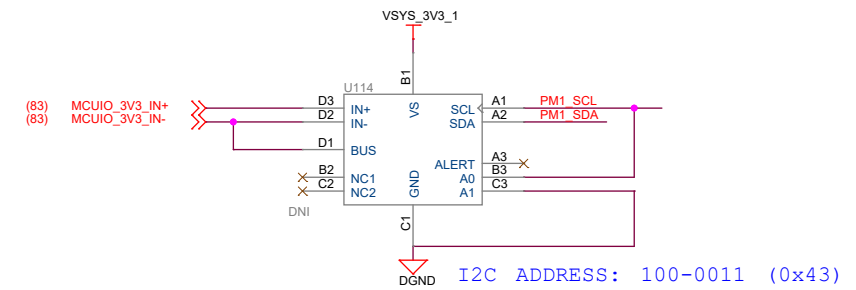


Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible - so functionality and performance should not be impacted with either INA

CURRENT MONITORS #1

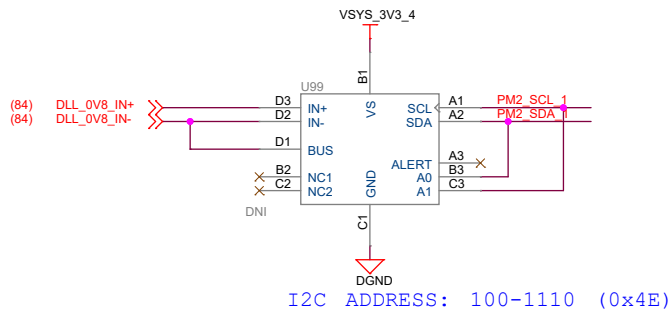
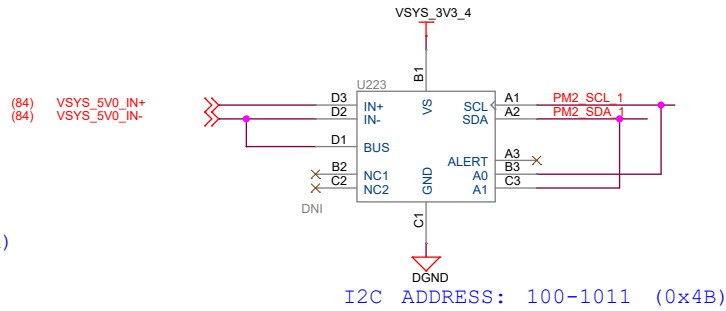
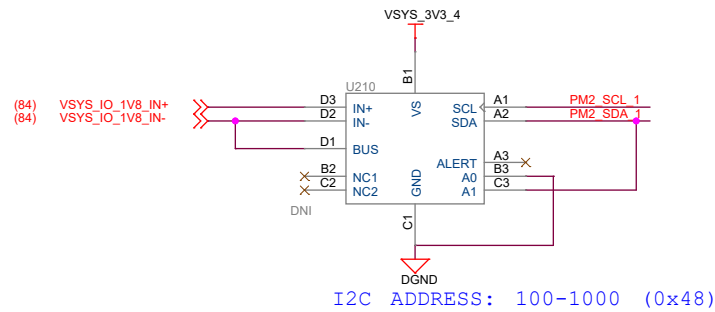
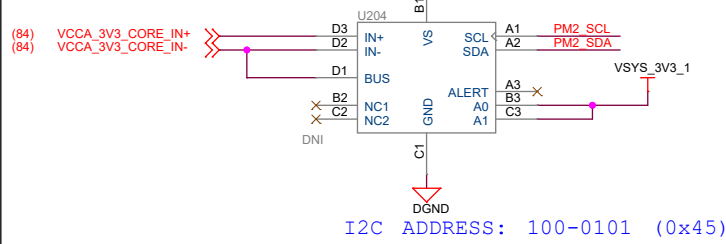
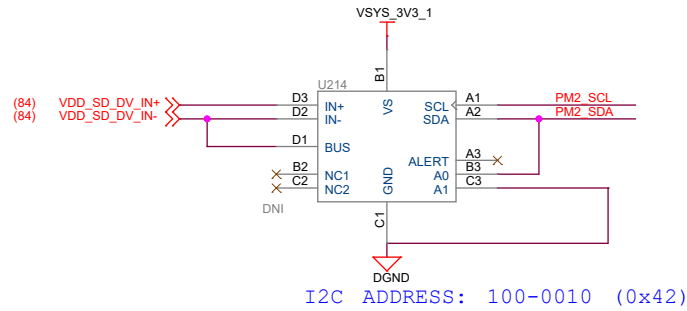
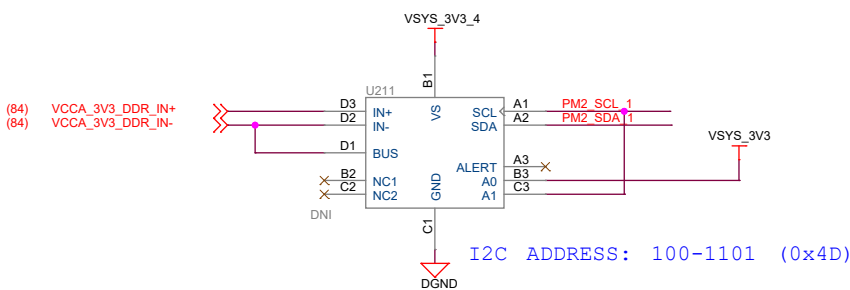
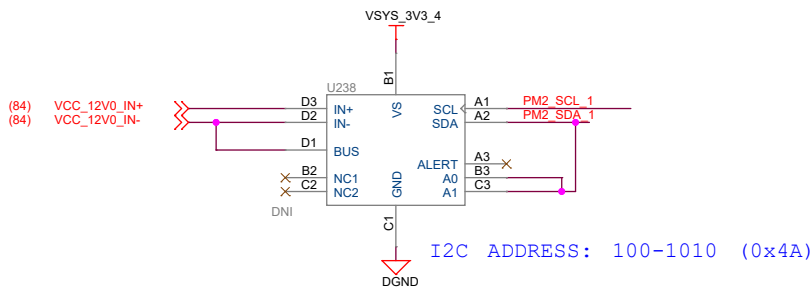
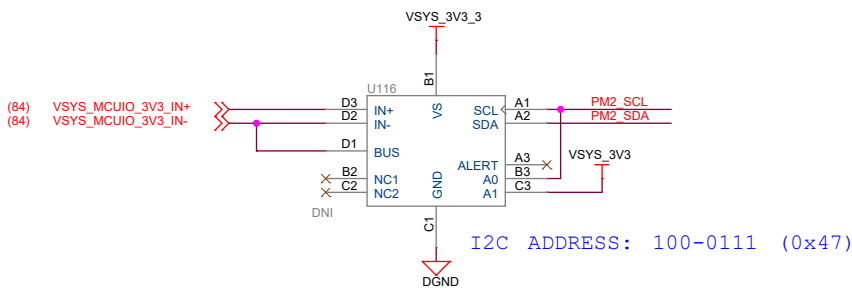
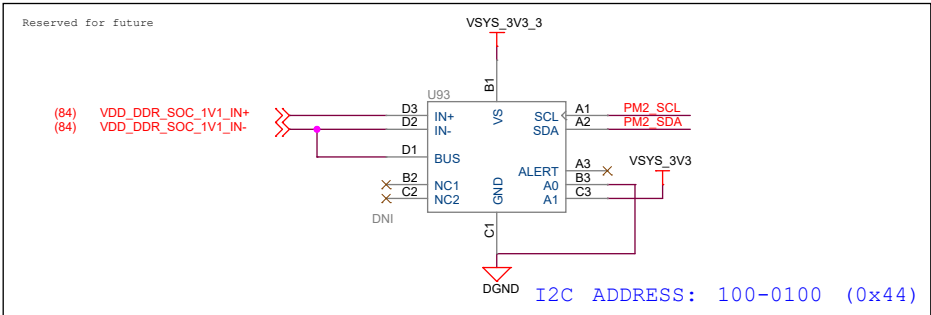
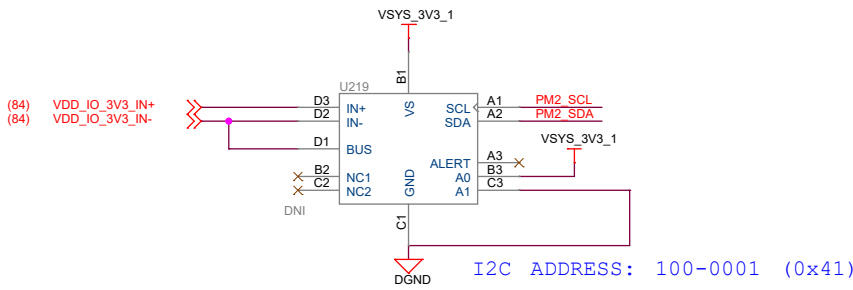
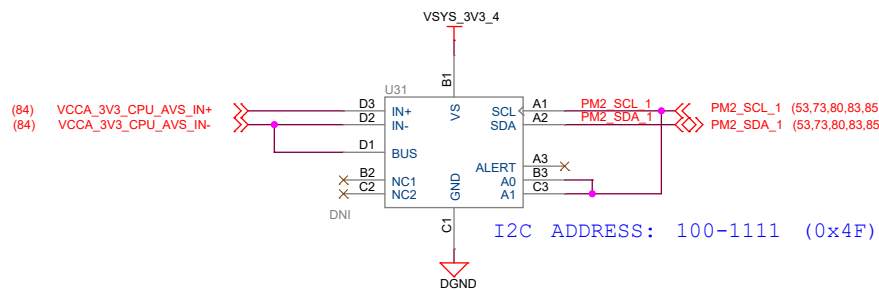
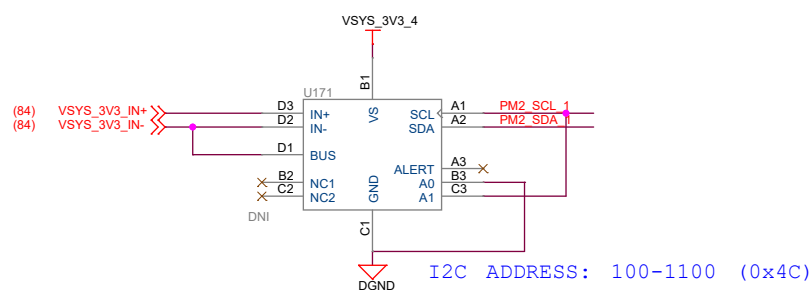
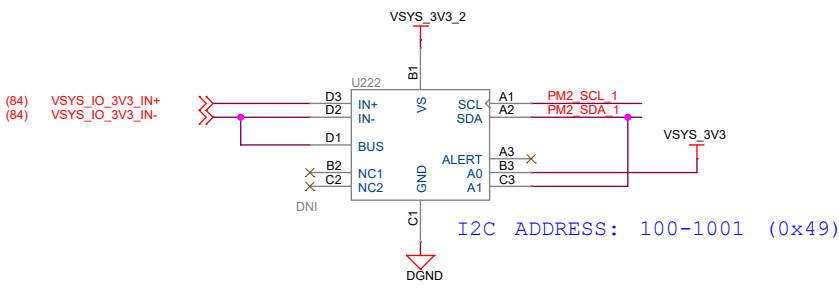
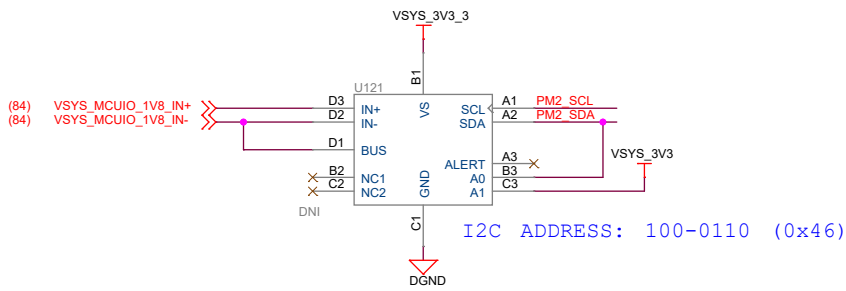
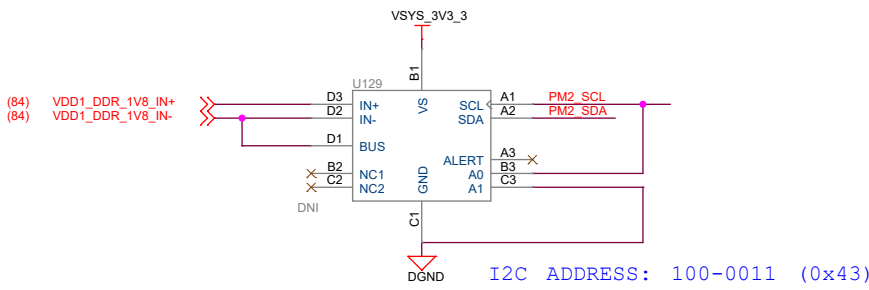
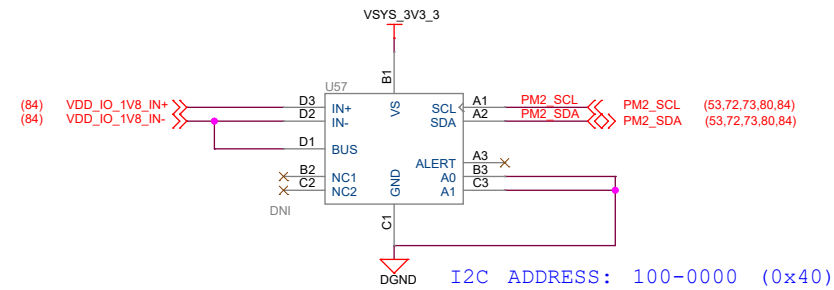


CURRENT MONITORS - INA231



Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

CURRENT MONITORS - INA231

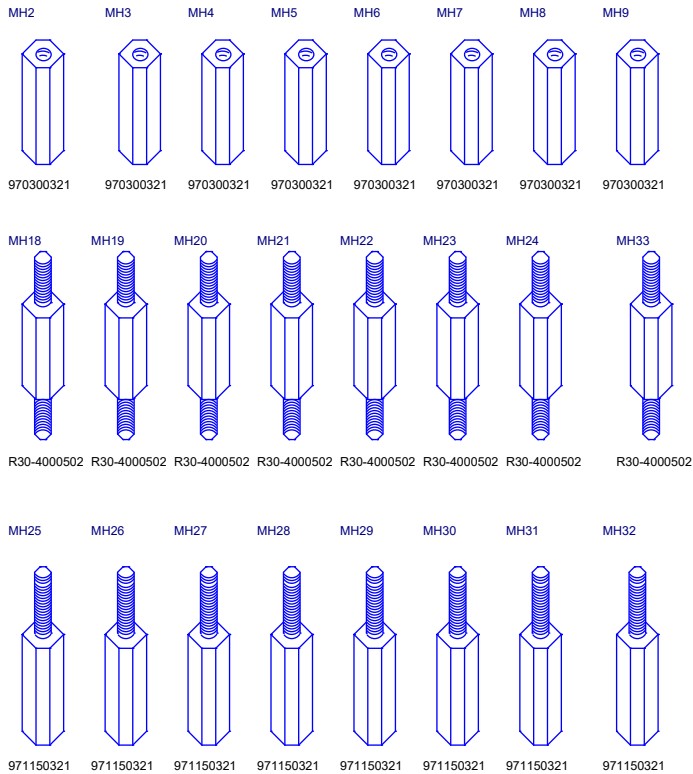


HARDWARE SCHEMATICS

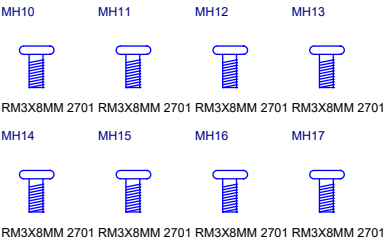
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

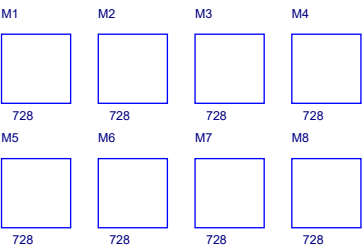
STANDOFFS



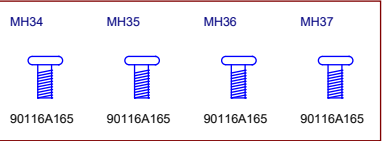
SCREWS



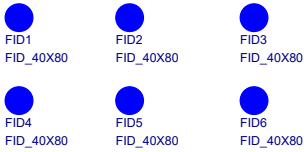
RUBBER FEET



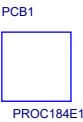
SCREW FOR FAN ASSEMBLY



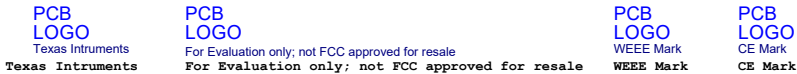
FIDUCIALS



BARE PCB



LOGOs



LABELS

Board Serial No.



Assembly Revision.



EVM Orderable No.



Orderable Part Numbers

Variant	Label Text
001:Soldered GP SoC	J742S2XG01EVM
002:Soldered HS SoC	J742S2XH01EVM
003:Socketed SoC	J742S2XS01EVM

SOCKET



HEAT SINK



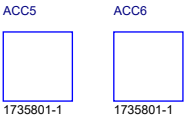
PROCESSOR



FAN



CRIMP PIN



CONN HOUSING

