

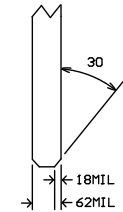
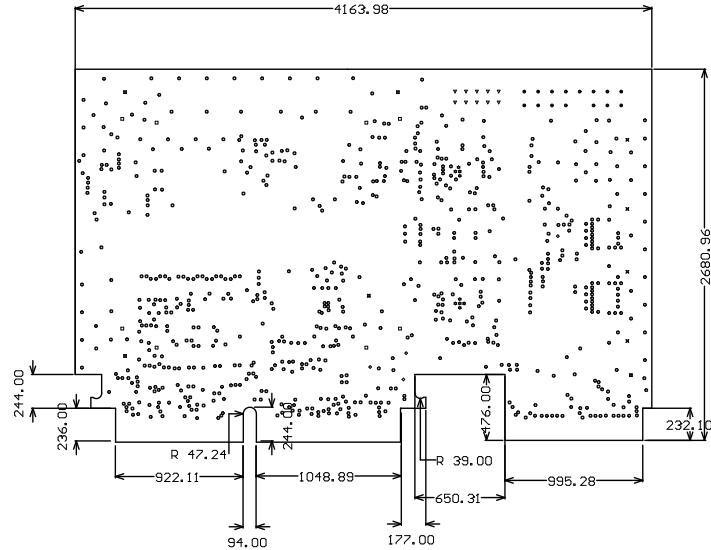
Symbol	Count	Hole Size	Plated	Hole Tolerance (+)	Hole Tolerance (-)	Hole Length	Routed Path Length
☆	9	7.87mil (0.200mm)	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
⊙	761	8.00mil (0.203mm)	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
▽	10	35.04mil (0.890mm)	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
◇	4	37.99mil (0.965mm)	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
●	15	40.16mil (1.020mm)	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
■	1	45.00mil (1.143mm)	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
□	8	45.28mil (1.150mm)	NPTH	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
✕	4	110.24mil (2.800mm)	NPTH	1.97mil (0.050mm)	1.18mil (0.030mm)	-	-
⊗	4	159.00mil (4.039mm)	NPTH	3.00mil (0.076mm)	3.00mil (0.076mm)	-	-
	816 Total						

J5 and J11: NPTH on SMT pads are intentional per manufacturers footprint. SMT pad copper may be pulled back 5-8mil from holes as needed for processing.

### SCALE : NTS

#### NOTES:

- BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
- VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED, PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING/COVERING" REQUIREMENTS.
- MANUFACTURER'S IDENTIFICATION/DATECODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE OF THE BOARD.
- LAYER TO LAYER REGISTRATION SHALL BE WITHIN +/-2 MIL.
- REFER IMPEDANCE TABLE FOR IMPEDANCE CONTROL TRACES ON LAYER 1, 3 & 6.
- ALL VIAS ARE TENTED ON BOTH SIDES UNLESS OTHERWISE SOLDER MASK OPENED IN GERBER.



GOLD FINGER  
SIDE VIEW

### IMPEDANCE TABLE : [6]

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/-10%	REFERENCE LAYER
TOP	5.66 MILS	*	50 OHM	LAYER=2 (GND LAYER)
TOP	4 MILS	7 MILS	100 OHM	LAYER=2 (GND LAYER)
TOP	5 MILS	6.22 MILS	90 OHM	LAYER=2 (GND LAYER)
L3	5.66 MILS	*	50 OHM	LAYER=2 / LAYER=4
L3	4.2 MILS	6 MILS	100 OHM	LAYER=2 / LAYER=4
BOTTOM	5.66 MILS	*	50 OHM	LAYER=5 (GND LAYER)
BOTTOM	4 MILS	7 MILS	100 OHM	LAYER=5 (GND LAYER)
BOTTOM	5 MILS	6.22 MILS	90 OHM	LAYER=5 (GND LAYER)

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	2.00mil	3.6	
1	Top Layer		1.85mil		
	Dielectric 1	FR-4	3.70mil	4.1	
2	GND1		1.26mil		
	Dielectric 2	FR-4	5.00mil	3.7	
3	SIG1		1.26mil		
	Dielectric 3	FR-4	32.00mil	3.7	
4	PWR		1.26mil		
	Dielectric 4	FR-4	5.00mil	3.7	
5	GND2		1.26mil		
	Dielectric 5	FR-4	3.70mil	4.1	
6	Bottom		1.85mil		
	Bottom Solder	Solder Resist	2.00mil	3.6	
	Bottom Overlay				

DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.5 MIL
MIN. VIA PAD SIZE:	18 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408	<input checked="" type="checkbox"/> FR-4 High Tg <input type="checkbox"/> OTHER
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
	<input type="checkbox"/> OTHER +/-
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
	<input type="checkbox"/> OTHER +/-
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER BLUE
	<input type="checkbox"/> MATTE <input checked="" type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input type="checkbox"/> IMMERSION GOLD (ENG)	<input type="checkbox"/> ENEPG
<input type="checkbox"/> MM. TIN/SILVER OR EQUIV	
<input checked="" type="checkbox"/> OTHER	HARD GOLD OVER NICKEL 30u/80u, ON EDGE/FINGERS
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE
	<input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3
	<input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input type="checkbox"/> REQUIRED <input checked="" type="checkbox"/> PER ORDER	
<input type="checkbox"/> OUTER LAYERS 6 MIL WIDE, 6 MIL SPACE	
<input type="checkbox"/> TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	
<input type="checkbox"/> INNER LAYERS 5 MIL WIDE, 7 MIL SPACE	
<input type="checkbox"/> TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	
<input type="checkbox"/> OUTER LAYERS 6.1 MIL WIDE, 6 MIL SPACE	
<input type="checkbox"/> TRACES REQUIRE 90 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE:	
HSEC-180 Adapter Board	
DESIGNED FOR:	
Public Release	
FILE NAME:	
MCU134A.PcbDoc	
ENGINEER:	LAYOUT BY:
Martinez Gustavo	.PCB_Layout
SCALE: 0.72	ALTUM DESIGNER VERSION:
	23.3.1.30

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: MCU134	REV: A	SUN REV: Not in version control
LAYER NAME = HSEC-180 Adapter Board	TID #:		
PLOT NAME = MCU129E1_FAB	GENERATED : 6/12/2024 8:12:38 AM		TEXAS INSTRUMENTS

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ENGINEER:	LAYOUT BY:
Martinez Gustavo	.PCB_Layout
SCALE: 0.72	ALTUM DESIGNER VERSION:
	23.3.1.30