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A

B

C

D

Layer	Name	Material	Thickness
	Top Overlay		
	Top Solder	Solder Resist	0.010mm
1	Top Layer		0.070mm
	Dielectric1	FR-4 High Tg	1.460mm
2	Bottom Layer		0.070mm
	Bottom Solder	Solder Resist	0.010mm
	Bottom Overlay		

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template
D	1	3.200mm (125.98mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c0hn320
◇	1	6.000mm (236.22mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c600hn600m600p-1
I	2	1.016mm (40.00mil)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
✕	2	1.100mm (43.31mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c160h110
✱	2	2.000mm (78.74mil)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
⊕	2	7.000mm (275.59mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c700hn700m700p-1
▽	4	1.000mm (39.37mil)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
⊙	4	1.200mm (47.24mil)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
⊗	4	1.600mm (62.99mil)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
▽	4	2.000mm (78.74mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c200hn200
○	4	3.150mm (124.02mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c315hn315m315p-1
✕	14	1.300mm (51.18mil)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
⊞	17	0.900mm (35.43mil)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
⊗	20	0.300mm (11.81mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v50h30m0mx0
⊕	23	0.750mm (29.53mil)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
□	46	1.020mm (40.16mil)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
✱	167	0.200mm (7.87mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	(Mixed)
	317 Total							

85.00mm

105.00mm

1000.00mil

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: MCU154	REV: E1	SUN REV: Not in version control	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME = 060059-001.dwg	TID #: TIDA-010265			
PLOT NAME = Fabrication Drawing	GENERATED : 9/30/2024 1:34:23 PM		TEXAS INSTRUMENTS	

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Material	Thickness	Constant	Board Layer Stack
Solder Resist	0.010mm	3.5	
	0.070mm		
FR-4 High Tg	1.460mm	4.8	
	0.070mm		
Solder Resist	0.010mm	3.5	

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 8 MIL

MIN. VIA PAD SIZE: 19 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

FR-4

☒ FR-4 High Tg

☐ OTHER

THICKNESS: ☒ 62 MIL (1.6mm) +/-10%

☐ OTHER

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2

☐ OTHER +/-

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2

☐ OTHER +/-

DRILLING:

REFERENCE: ☒ AS SHOWN ☒ NC DRILL FILES

PTH COPPER THICKNESS: ☒ 20-30 um

☐ OTHER

BOARD FINISH:

SILKSCREEN: ☒ TOP ☒ BOTTOM

SILKSCREEN COLOR: ☒ WHITE ☐ OTHER

SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER

☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☐ IMMERSION GOLD (ENIG) ☐ ENEPIG

☐ IMM. TIN/SILVER OR EQUIV ☒ OTHER HASL

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE

☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3

☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: ☐ YES

BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS

INSTRUMENTS

PROJECT TITLE:

TIEUM-MTR-HUINU

DESIGNED FOR:

Public Release

FILE NAME:

MCU154E1\_PCB.PcbDoc

Specification must be met in all applications.

ENGINEER: Jason Osborn

LAYOUT BY:

SCALE: 1.00

ALTUM DESIGNER VERSION: 23.9.2.47

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