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BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.</p> <p>2. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED, PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING/COVERING" REQUIREMENTS.</p> <p>3. MANUFACTURER'S IDENTIFICATION,DATECODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE OF THE BOARD.</p> <p>4. LAYER TO LAYER REGISTRATION SHALL BE WITHIN +/-5 MIL.</p> <p>5. REFER IMPEDANCE TABLE FOR IMPEDANCE CONTROL TRACES ON LAYER 1, 3, 5 , 8 & 10.</p> <p>6. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS OTHERWISE SOLDER MASK OPENED IN GERBER.</p> <div><div><div>2755.90mil</div><div>2276.49mil</div></div><div>LAYER STACK-UP :</div><table><tr><th>Layer</th><th>Name</th><th>Material</th><th>Thickness</th><th>Constant</th><th>Board Layer Stack</th></tr><tr><td></td><td>Top Overlay</td><td></td><td></td><td></td><td></td></tr><tr><td></td><td>Top Solder</td><td>Solder Resist</td><td>0.50mil</td><td>3.5</td><td></td></tr><tr><td>1</td><td>Top Layer</td><td></td><td>1.40mil</td><td></td><td></td></tr><tr><td></td><td>Dielectric 1</td><td>FR-4</td><td>3.70mil</td><td>4</td><td></td></tr><tr><td>2</td><td>L02_GND1</td><td></td><td>1.40mil</td><td></td><td></td></tr><tr><td></td><td>Dielectric 2</td><td>FR-4</td><td>5.00mil</td><td>4</td><td></td></tr><tr><td>3</td><td>L03_SIG1</td><td></td><td>1.40mil</td><td></td><td></td></tr><tr><td></td><td>Dielectric 3</td><td>FR-4</td><td>7.00mil</td><td>4</td><td></td></tr><tr><td>4</td><td>L04_GND2</td><td></td><td>1.40mil</td><td></td><td></td></tr><tr><td></td><td>Dielectric 4</td><td>FR-4</td><td>4.00mil</td><td>4</td><td></td></tr><tr><td>5</td><td>L05_SIG2</td><td></td><td>1.40mil</td><td></td><td></td></tr><tr><td></td><td>Dielectric 5</td><td>FR-4</td><td>7.00mil</td><td>4</td><td></td></tr><tr><td>6</td><td>L06_PWR</td><td></td><td>1.40mil</td><td></td><td></td></tr><tr><td></td><td>Dielectric 6</td><td>FR-4</td><td>4.00mil</td><td>4</td><td></td></tr><tr><td>7</td><td>L07_GND3</td><td></td><td>1.40mil</td><td></td><td></td></tr><tr><td></td><td>Dielectric 7</td><td>FR-4</td><td>7.00mil</td><td>4</td><td></td></tr><tr><td>8</td><td>L08_SIG3</td><td></td><td>1.40mil</td><td></td><td></td></tr><tr><td></td><td>Dielectric 8</td><td>FR-4</td><td>5.00mil</td><td>4</td><td></td></tr><tr><td>9</td><td>L09_GND4</td><td></td><td>1.40mil</td><td></td><td></td></tr><tr><td></td><td>Dielectric 9</td><td>FR-4</td><td>3.70mil</td><td>4</td><td></td></tr><tr><td>10</td><td>Bottom Layer</td><td></td><td>1.40mil</td><td></td><td></td></tr><tr><td></td><td>Bottom Solder</td><td>Solder Resist</td><td>0.50mil</td><td>3.5</td><td></td></tr><tr><td></td><td>Bottom Overlay</td><td></td><td></td><td></td><td></td></tr><tr><td colspan="3">Total board thickness:</td><td colspan="3">61.40mil</td></tr></table></div> <div><div>DESIGN INFORMATION</div><div>MIN. TRACK WIDTH: 3.5MIL MIN. CLEARANCE: 4 MIL MIN. VIA PAD SIZE: 18 MIL MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL</div><div>MATERIAL: <input type="checkbox"/> FR-408 <input checked="" type="checkbox"/> FR-4 High Tg <input type="checkbox"/> OTHER THICKNESS: <input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER TOLERANCE: <input type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/- BOW & TWIST: <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/- DRILLING: REFERENCE: <input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES PTH COPPER THICKNESS: <input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER BOARD FINISH: SILKSCREEN: <input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM SILKSCREEN COLOR: <input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER SOLDER RESIST COLOR: <input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER <input type="checkbox"/> MATTE <input checked="" type="checkbox"/> SEMI-GLOSS SURFACE FINISH: <input checked="" type="checkbox"/> IMMERSION GOLD (ENIG) <input type="checkbox"/> ENEPIG <input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER ARRAY/PANEL: <input checked="" type="checkbox"/> CUT AND TRIM PER M1 BOARD OUTLINE <input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF: <input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3 <input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER ADDITIONAL REQUIREMENTS: BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input type="checkbox"/> REQUIRED <input checked="" type="checkbox"/> PER ORDER <input type="checkbox"/> OUTER LAYERS 6 MIL WIDE, 6 MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE <input type="checkbox"/> INNER LAYERS 5 MIL WIDE, 7 MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE <input type="checkbox"/> OUTER LAYERS 6.1 MIL WIDE, 6 MIL SPACE TRACES REQUIRE 90 OHM DIFFERENTIAL IMPEDANCE</div><div><div>TEXAS INSTRUMENTS</div><div>PROJECT TITLE: F29H85x controlSOM EVM DESIGNED FOR: Public Release FILE NAME: MCU144A.PcbDoc ENGINEER: Gustavo Martinez LAYOUT BY: Krypton Solutions SCALE: 1.00 ALTUM DESIGNER VERSION: 24.3.1.35</div></div></div> <table><tr><td colspan="2">ALL ARTWORK VIEWED FROM TOP SIDE</td><td>BOARD #: MCU144</td><td>REV: A</td><td>SUN REV: Not in version control</td><td rowspan="3">Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. 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