

AM62A7 / AM62A3 LOW POWER STARTER KIT SK (EVM) WITH TPS65931211-Q1 PMIC

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REV	A1
VER	1.2

D-Note :-

SK/EVM is a device evaluation board or platform. The SK/EVM is not a reference design. In some cases the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SOC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata, and TRM when designing their custom board. The information found in the datasheet should always take precedence over the SK/EVM implementation.

R-Note :-

- * Verify the DNI components configuration with respect to the SK schematics (Use PDF) after completion of board design before board assembly
- * A standard 5% tolerance resistor can be used for most of the series and parallel pull resistor
- * Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build. (Refer FAQs listed for additional details)

KEY LINKS TO COLLATERALS

Hardware Design Guide : https://www.ti.com/lit/an/sprad85/sprad85.pdf
Schematic Design and Review Checklist : https://www.ti.com/lit/an/sprad21d/sprad21d.pdf
PMIC Power Solutions Application Note : https://www.ti.com/lit/po/sltv204/sltv204.pdf
DDR Board Design and Layout Guidelines : https://www.ti.com/lit/an/sprad66a/sprad66a.pdf
SKs (Starter Kits) for reference : SK-AM62B, SK-AM62B-P1, SK-AM62-LP, SK-AM62-SIP, SK-AM62A-LP, SK-AM62P-LP

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REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	09 AUG 2023	Drafted from "PROC135E3_SCH" document.	Mistral Design Team	Nishant	Ajit MB
0.2	18 AUG 2023	Updated SoC, eMMC & PMIC Part Number	Mistral Design Team	Nishant	Ajit MB
1.0	21 AUG 2023	Baselined and Released	Mistral Design Team	Nishant	Ajit MB
1.1	11 JUNE 2024	Updated SoC Pin name (VMON_VSYS), Enabled Voltage ratings for all the capacitors and added Design Review notes Moved to DNI : C33, C36, C291, C177, R272, U56, Y1 Moved to Mount : C556, R295, R296, R297, R299, R300, R301, R302, R303, R505, R534 C290 - 1uF changed to 2.2uF; C288,C184,C181,C39 - 1uF changed to 0.1uF; C45,C42 - 9pF changed to 18pF; C182,C179 - 2.2uF changed to 1uF; C40 - 4.7uF changed to 1uF; C38 - 0.1uF changed to 4.7uF R350 - 2.2K changed to 10K; R125,R135 - 3.4K_1% changed to 3.48K_1%; R343 - 22E changed to 0E; R315,R242,R371 - 49.9K_1% changed to 10K; R368 - 10K_1% changed to Std 10K; R311 - 100K changed to Std 10K; R342,R341,R586,R584 - 22E_1% changed to 0E; R331,R344,R328 - 499E_0.1% changed to 499_1%; R451 - 10K changed to 47K; R351,R611 - 11K_1% changed to 10K_1%.	Mistral Design Team	Pandiya Rajan	Ajit MB
1.2	13 FEB 2025	Updated SoC Part Number	Mistral Design Team	Pandiya Rajan	Ajit MB

LINKS TO KEY FAQs

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1203305/faq-am62a7-and-am62a7-q1-custom-board-hardware-design-collaterals-to-get-started>

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1203441/faq-am62a3-and-am62a3-q1-custom-board-hardware-design-collaterals-to-get-started>

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1306030/faq-am62p-am62p-q1-custom-board-hardware-design--faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit>

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1340905/faq-am62a7-am62a7-q1-am62a3-am62a3-q1---custom-board-hardware-design---guidelines-for-reuse-of-sk-am62a-lp-schematics>

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1347063/faq-am62a7-and-am62a7-q1-am62a3-and-am62a3-q1---custom-board-hardware-design---design-and-review-notes-for-reuse-of-sk-am62a-lp-schematics>

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1280753/faq-am62a7-am62a7-q1-am62a3-am62a3-q1-custom-board-hardware-design---faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit>

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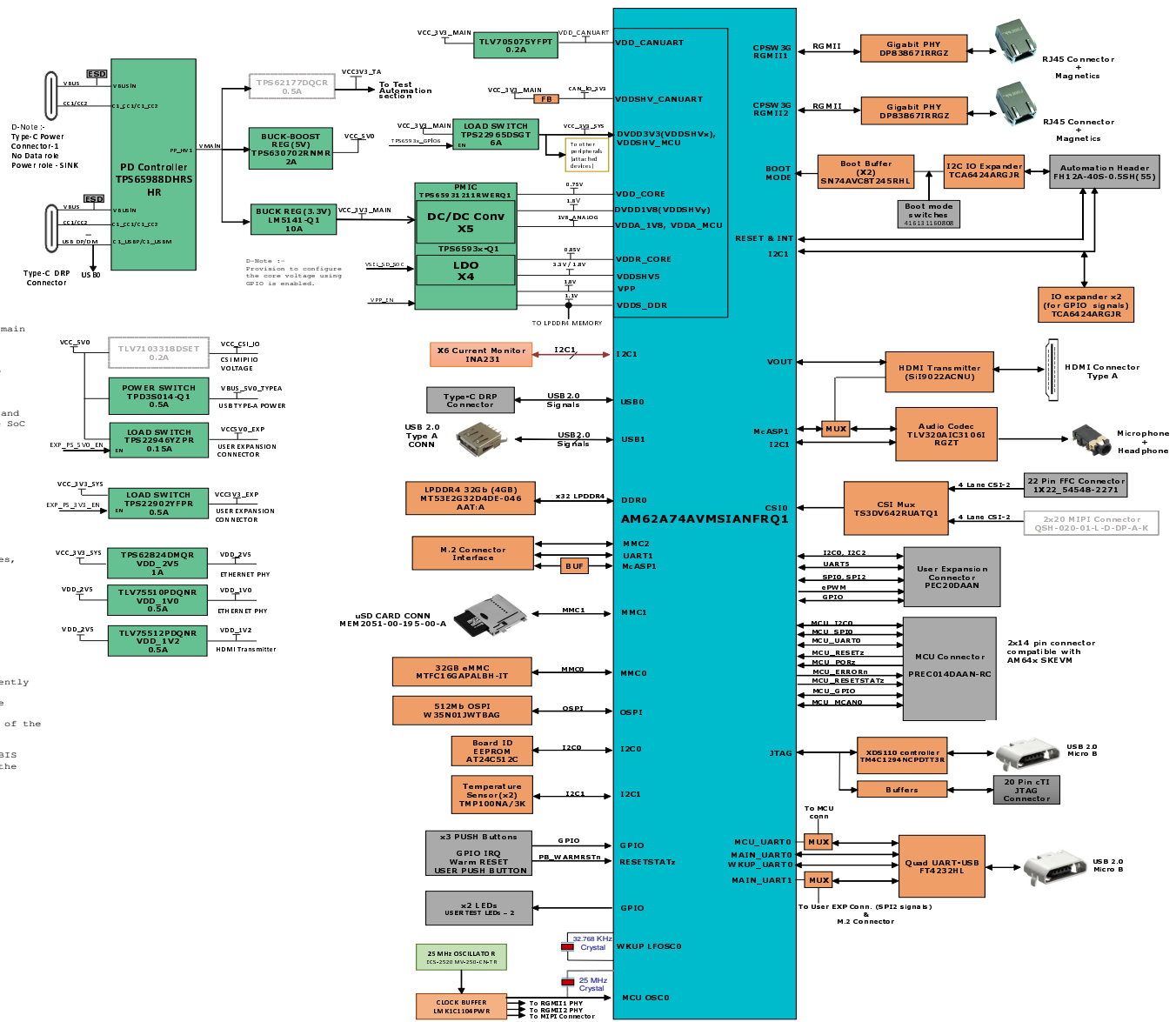
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BLOCK DIAGRAM SK-AM62A-LP

D-Note 1:-
Pins (OBSCLK) D17 and R20 of the SoC are main domain Observation clock output for test and debug purposes only. Add a TP near to the SoC and provision to isolate the signal for testing whenever possible.
Pin (MCU_OBSCLK) C11 of the SoC are MCU Domain Observation clock output for test and debug purposes only. Add a TP near to the SoC and provision to isolate the signal for testing whenever possible.

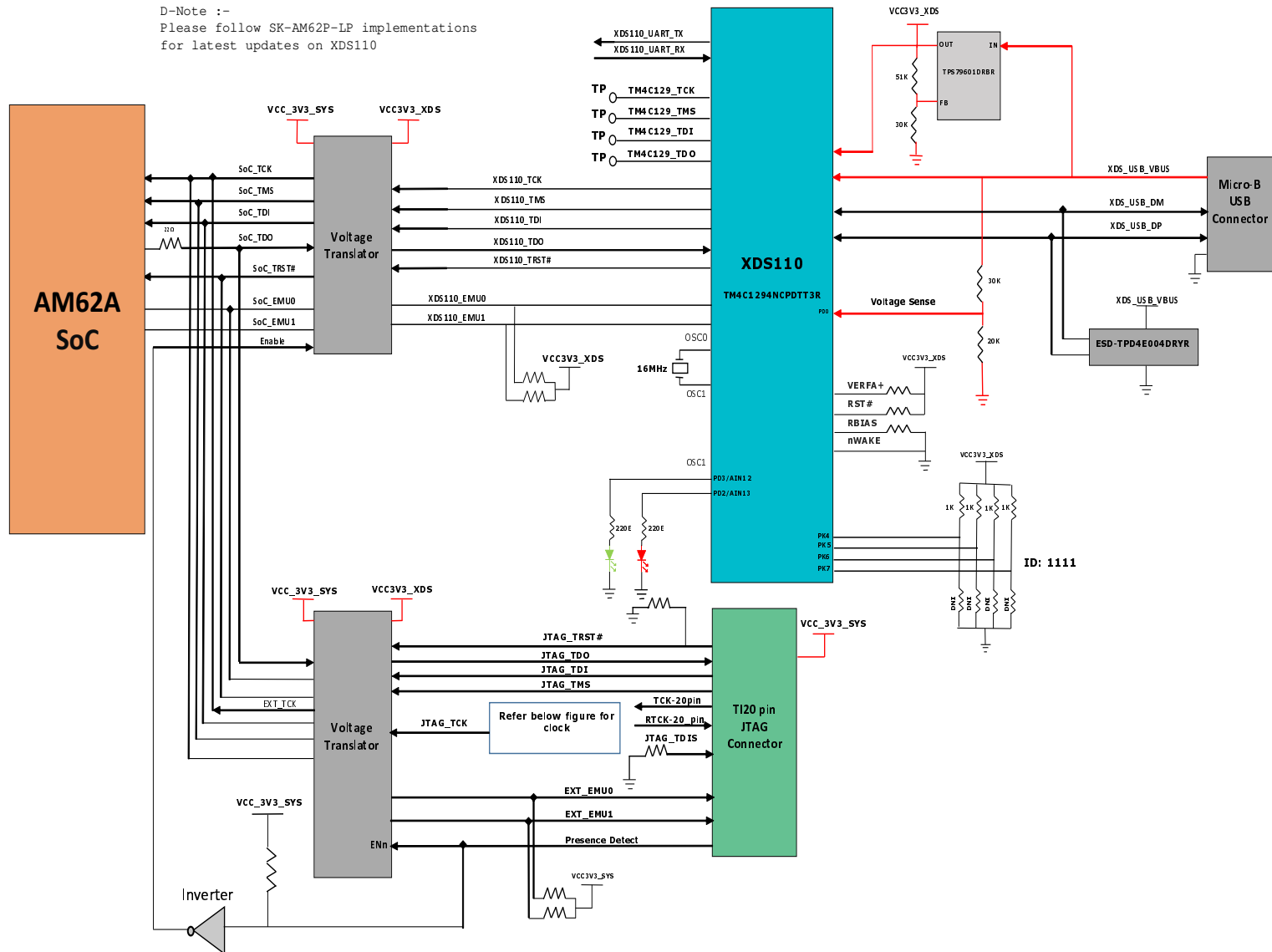
D-Note 1:-
Refer Device Comparison section of the processor data sheet for supported cores, peripherals and memory size

D-Note 1:-
Drive strength configuration is currently not supported. The drive strength must remain in the default state since this is the only condition used during timing closure of the peripherals. The devices are set to maximum drive strength. Please reference to the IBIS model to find the drive strength of the IOs.



BLOCK DIAGRAM_XDS110

D-Note :-
Please follow SK-AM62P-LP implementations
for latest updates on XDS110



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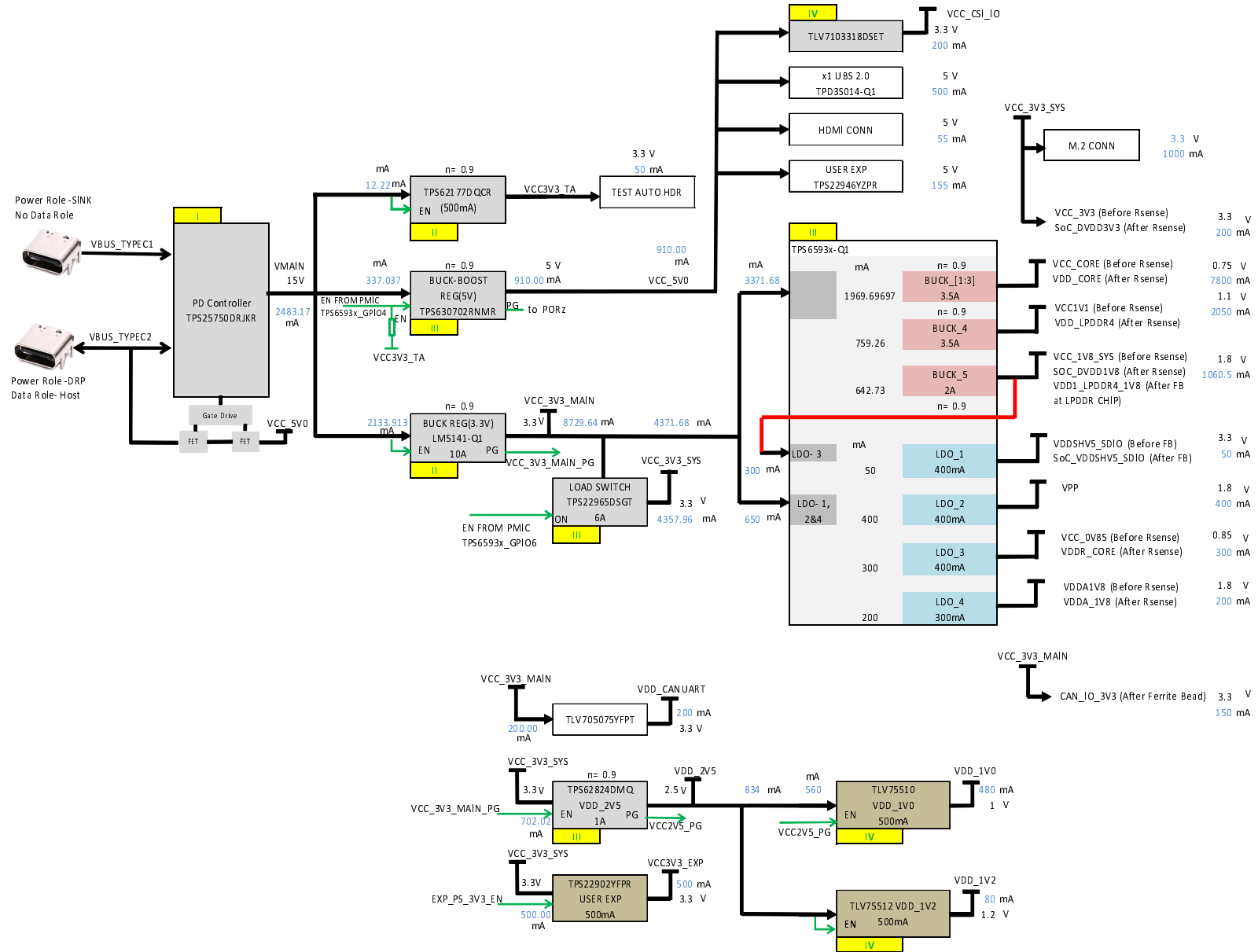


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POWER BLOCK DGM



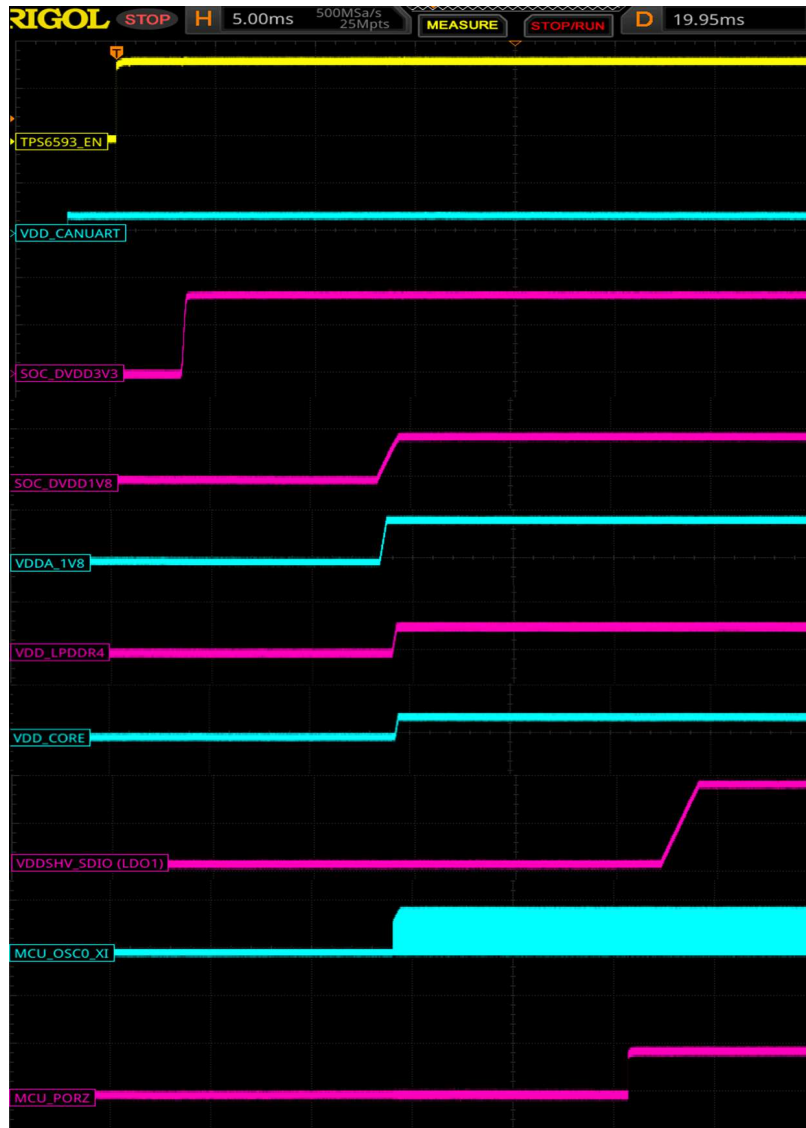
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POWER SEQUENCE



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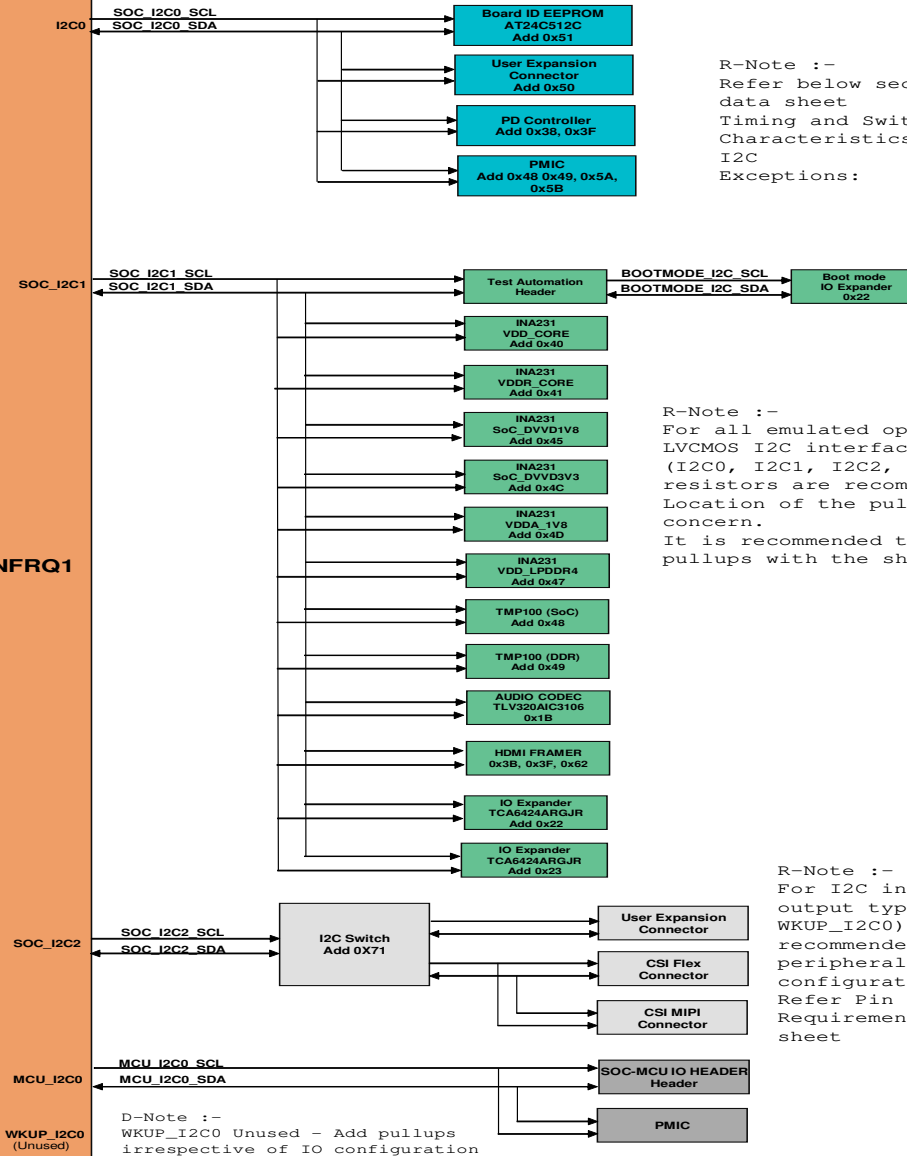
Title POWER SEQUENCE

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I2C TREE

R-Note
Add - Indicates
Address

**AM62A74AVMSIANFRQ1
SoC**



R-Note :-
Refer below section of the SOC
data sheet
Timing and Switching
Characteristics
I2C
Exceptions:

R-Note :-
For all emulated open-drain output
LVCMOS I2C interfaces.
(I2C0, I2C1, I2C2, I2C3) pullup
resistors are recommended
Location of the pullup is not a
concern.
It is recommended to connect the
pullups with the shortest possible stub

R-Note :-
For I2C interfaces with open-drain
output type buffer (MCU_I2C0 and
WKUP_I2C0), an external pullup is
recommended irrespective of
peripheral usage and IO
configuration.
Refer Pin Connectivity
Requirements section of SOC data
sheet

D-Note :-
WKUP_I2C0 Unused - Add pullups
irrespective of IO configuration

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GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE RAIL CONNECTED ON SKEWM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	Soc_DVDD1VB
2	WLAN Interrupt	WLAN_IRQ	INTERUPT	GPIO_72	MMC2_SOWP	INPUT	HIGH	LOW	VDDSHV6	Soc_DVDD1VB
3	Enable for BT Interface	BT_EN_S0C	ENABLE	MCU_SPB0_0	MCU_SPB0_C0	OUTPUT	LOW	HIGH	VDDSHV_MCU	Soc_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_N7n	INTERUPT	GPIO_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	Soc_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_CSPI_RSTn	RESET	GPIO_12	OSPI_CS_n1	OUTPUT	HIGH	LOW	VDDSHV3	Soc_DVDD1VB
6	MCU Header GPIO0_16	MCU_GPIO0_16	GPIO	MCU_GPIO0_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
7	MCU Header GPIO0_15	MCU_GPIO0_15	GPIO	MCU_GPIO0_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
8	PMIC Interrupt	PMIC_INT_8	INTERUPT	GPIO_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV3	Soc_DVDD3V3
9	CAN-FD fast wake up signal from switch	CAN_FD_WAKEUP_SW_INH	INTERUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
10	CAN-FD fast wake up signal from MCU header	CAN_FD_WAKEUP_H0R_INH								
11	Interrupt signal from Automotive Ethernet ADD-ON board	CPSW_ETH2_INH								
12	User test LED control signal	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SOWP	OUTPUT	LOW	HIGH	VDDSHV0	Soc_DVDD3V3
13	Watchdog trigger input signal for Watchdog trigger mode	PMIC_WDOG_TRIGGER	ENABLE	MCU_GPIO19	Wakeup_DCO_SCL	INPUT	LOW	HIGH	VDDSHV_MCU	Soc_DVDD3V3
14	Wakeup signal from RGMII	CPSW_ETH2_WAKE	INTERUPT	MCU_GPIO0_10	Wakeup_DCO_SDA	INPUT	LOW	HIGH	VDDSHV_MCU	Soc_DVDD3V3
15	User EXP Conn GPIO	EXP_GPIO1_22	GPIO	GPIO1_22	UART0_CTSn	NA	NA	NA	VDDSHV0	Soc_DVDD3V3
16	IO Expander Interrupt	GPIO1_23_INTn	INTERUPT	GPIO1_23	UART0_CTSn	INPUT	HIGH	LOW	VDDSHV0	Soc_DVDD3V3
17	User Interrupt									
18	User EXP Conn GPIO	EXP_GPIO0_14_1T	GPIO	GPIO0_14	OSPI_CS_n3	NA	NA	NA	VDDSHV1	Soc_DVDD1VB
19	PMIC Standby Disable	PMIC_P_M_END	ENABLE	MCU_GPIO0_22	PMIC_P_M_END	OUTPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
20	User EXP Conn GPIO	EXP_EXPWM1_8	GPIO	GPIO1_10	MCASP0_AXI0	NA	NA	NA	VDDSHV0	Soc_DVDD3V3
IO EXPANDER - 01										
1	Ethernet Daught Card plug in detect	RGMII_R0D_CONN_DET	DETECTION	IO EXPANDER-P00		INPUT	HIGH	LOW		VCC_3V3_SYS
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P01		OUTPUT	HIGH	LOW		VCC_3V3_SYS
3	M.2 module Bluetooth LDO Enable	BT_EN_S0C	ENABLE	IO EXPANDER-P02		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_S0D_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
5	SOC eFuse Voltage (VPP=1.8V) Regulator Enable	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	NA	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P06		OUTPUT	LOW	HIGH		VCC_3V3_SYS
8	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
9	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	IO EXPANDER-P08		OUTPUT	HIGH	LOW		VCC_3V3_SYS
10	eMMC Reset control GPIO	GPIO_EMMC_RSTn	RESET	IO EXPANDER-P11		OUTPUT	HIGH	LOW		VCC_3V3_SYS
11	SOC UART1 Mux Select	UART1_TET_BUF_EN	ENABLE	IO EXPANDER-P12		OUTPUT	HIGH	LOW		VCC_3V3_SYS
12	BT UART WAKEUP signal	BT_UART_WAKE_S0C_3V3	INTERUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER-P14		OUTPUT	HIGH	LOW		VCC_3V3_SYS
14	Raspberry Pi Camera CSI0 GPIO1	CSI0_GPIO0	INPUT/OUTPUT	IO EXPANDER-P15		NA	NA	NA		VCC_3V3_SYS
15	Raspberry Pi Camera CSI0 GPIO2	CSI0_GPIO1	INPUT/OUTPUT	IO EXPANDER-P16		NA	NA	NA		VCC_3V3_SYS
16	WLAN Alert Interrupt	WLAN_ALERTn	INTERUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	HDMI Interrupt	HDMI_INTn	INTERUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC_3V3_SYS
19	MCASP1 Enable and Direction Control	MCASP1_TET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
20		MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
21		MCASP1_TET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	-		VCC_3V3_SYS
22		UART1_TET_SEL	DIRECTION CONTROL	IO EXPANDER-P25		OUTPUT	HIGH	-		VCC_3V3_SYS
23	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	INTERUPT	IO EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_SYS
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER - 02										
1	Soc SPD MUX Selection	SPD_TET_SEL	CONTROL	IO EXPANDER-P30		OUTPUT	LOW	-		VCC_3V3_SYS
2	Soc SPD MUX Enable	SPD_TET_OE	ENABLE	IO EXPANDER-P31		OUTPUT	LOW	LOW		VCC_3V3_SYS
3	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P32		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	CSI Mux and Mipi MUX Selection	CSI_SEL2	CONTROL	IO EXPANDER-P33		OUTPUT	HIGH	-		VCC_3V3_SYS
5	CSI MUX Enable	CSI_EN	ENABLE	IO EXPANDER-P34		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
6	Auto PHY mode config	AUTO_100M_1000M_CONFIG	CONTROL	IO EXPANDER-P35		OUTPUT	NA	NA		VCC_3V3_SYS
7	CSI I/O Voltage Select (VCC_CSI_I/O)	CSI_VIDD_SEL	CONTROL	IO EXPANDER-P36		OUTPUT	LOW	-		VCC_3V3_SYS
8	WLAN Reset control GPIO	SOC_WLAN_S0D_RST	RESET	IO EXPANDER-P37		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	Wlink Enable	WL_1T_EN	ENABLE	IO EXPANDER-P38		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
10	CSI Reset Control GPIO	CSI_RST2	RESET	IO EXPANDER-P39		OUTPUT	LOW	LOW		VCC_3V3_SYS

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Title GPIO MAPPING TABLE

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USB TYPE-C PD CONTROLLER AND POWER SUPPLY

POWER INDICATION LED: VBUS_TYPEC1

D-Note :-
Ok to use a 1K standard 5% tolerance resistor

R-Note :-
This is a supply negotiation indicator. On indicates success.

TYPE-C DUAL PD CONTROLLER

SPI EEPROM & PROGRAMMING HEADER

EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A

D-Note :-
Refer AM52P implementation for adding the capacitors



MISTRA

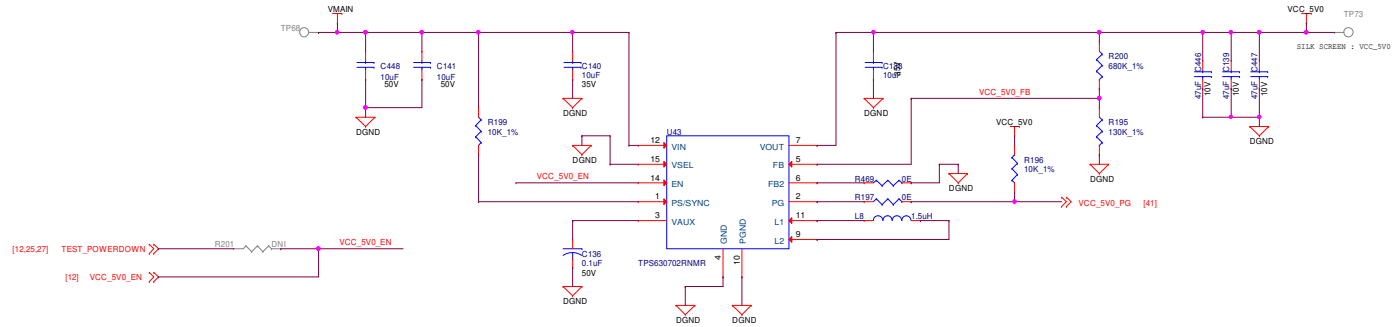
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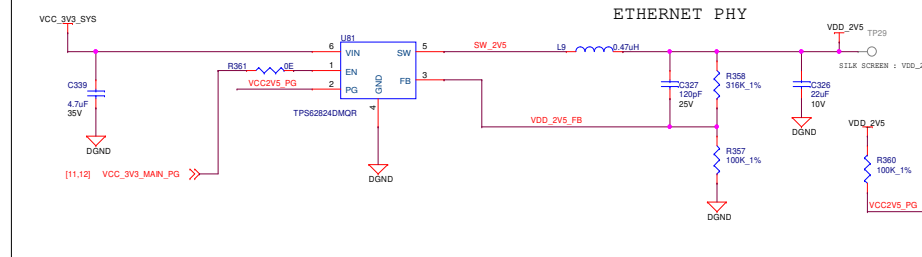
PERIPHERAL POWER SUPPLIES - 1

VinMin = 4.5V
VinMax = 15V
Vout = 5V @ 2A

D-Note :-
Add a Jumper or OR for isolation
or Current measurement for
preproduction board

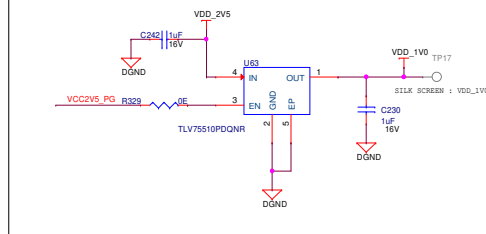


2.5V, 1.0 AMP SUPPLY

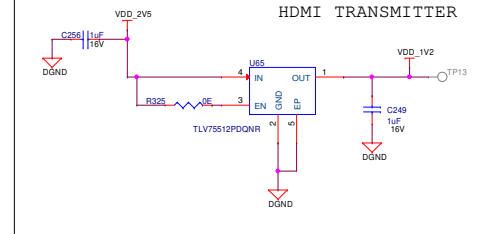


PERIPHERAL SUPPLY - ETHERNET PHY

1.0V, 0.5 AMP SUPPLY



1.2V, 0.5 AMP SUPPLY



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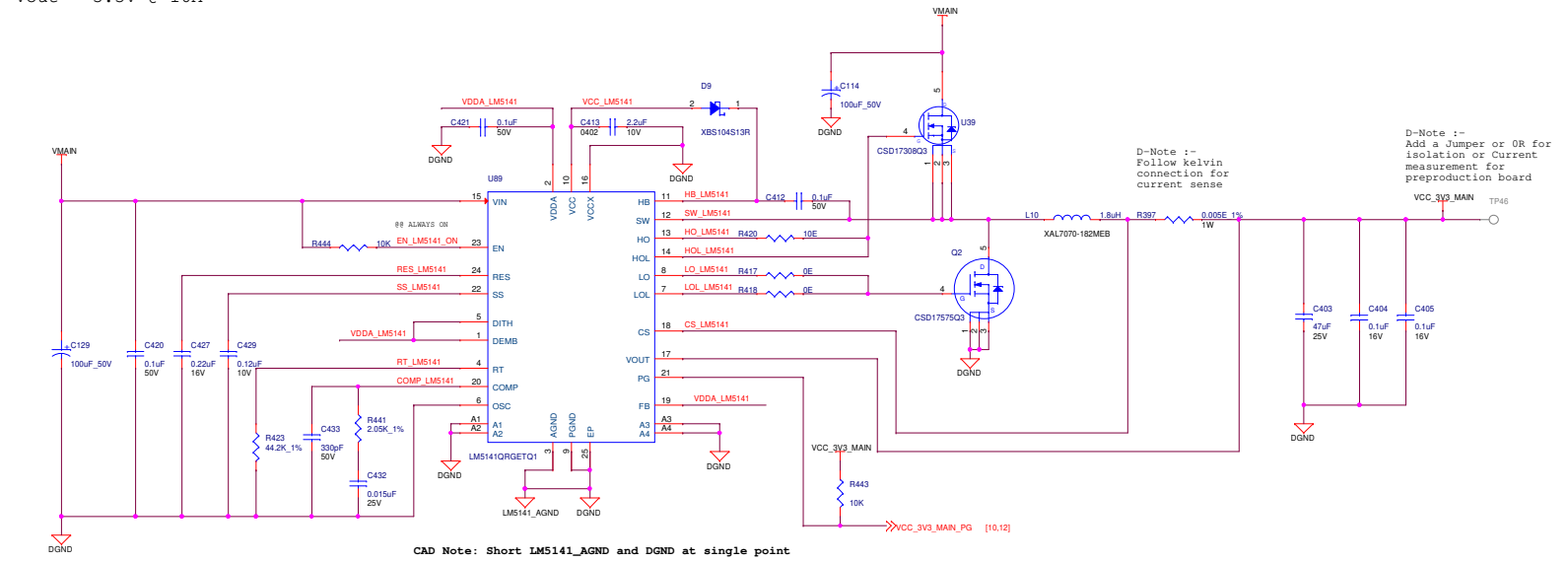
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PERIPHERAL POWER SUPPLIES - 2

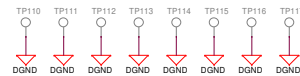
3.3V, 10.0 AMPS SUPPLY

VinMin = 4.5V
VinMax = 15V
Vout = 3.3V @ 10A



[33] ETH_CAN_NH_PRREREG >> EN LM5141 ON

GND TEST POINTS



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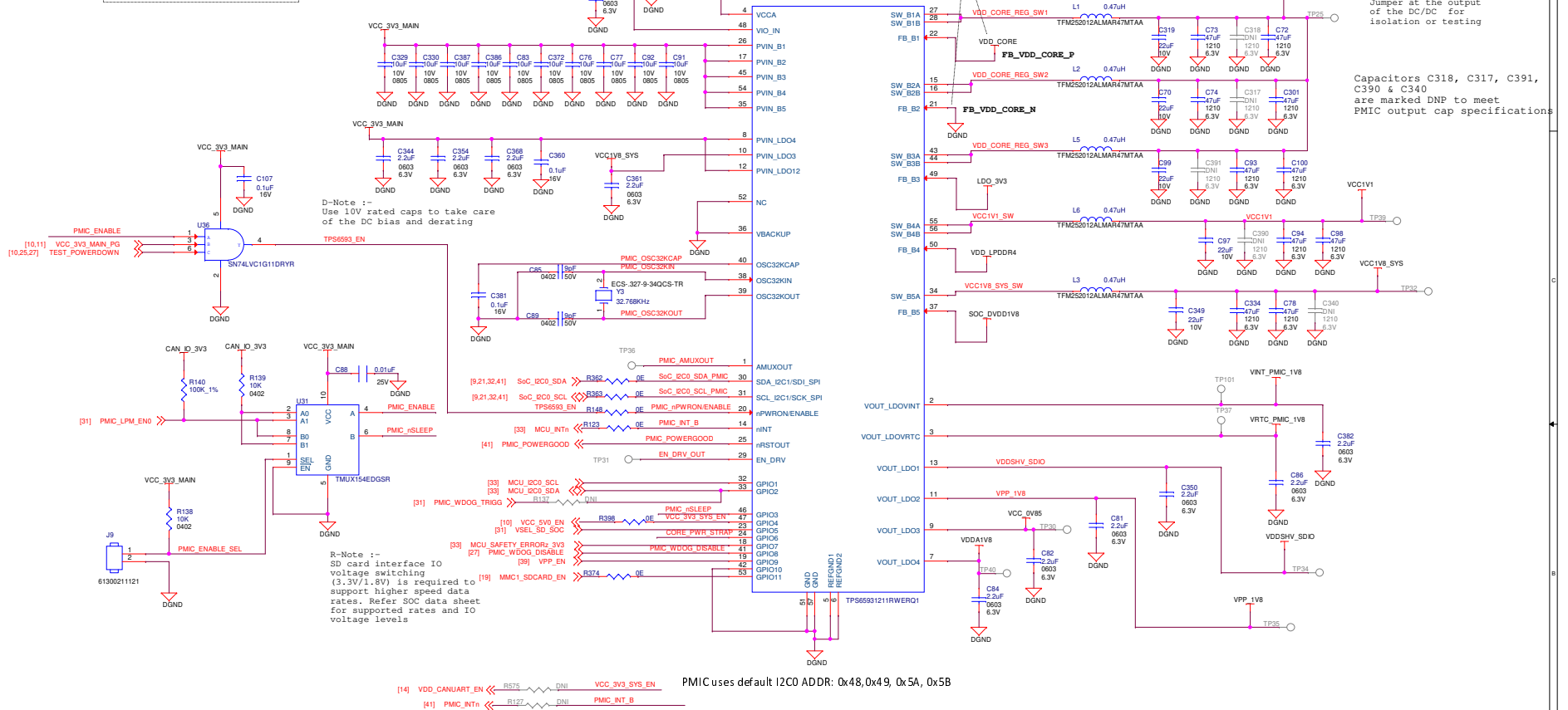
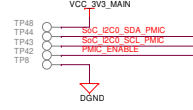


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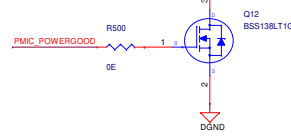
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SOC POWER SUPPLY PMIC

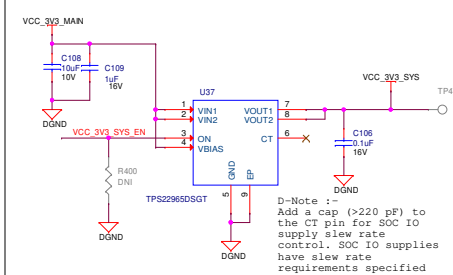
PMIC Config option



POWER INDICATION LED



VCC_3V3_SYS LOAD SWITCH

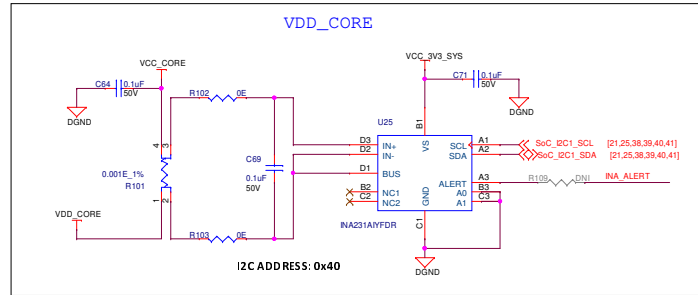


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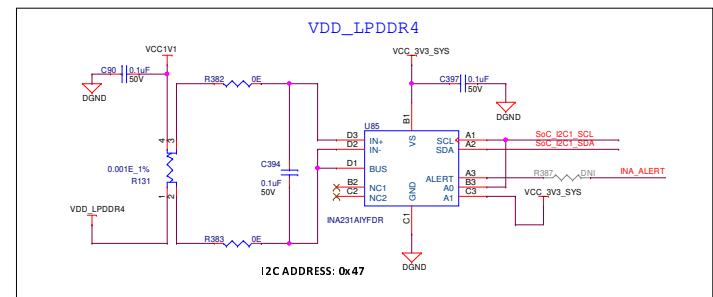
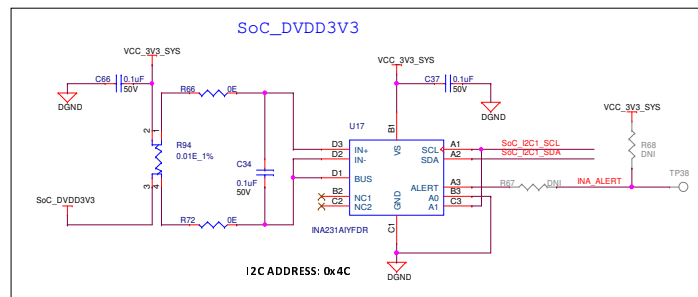
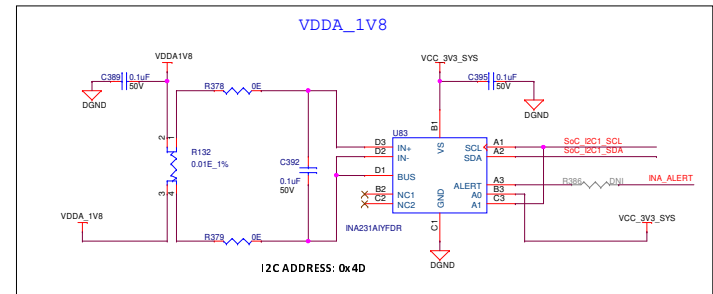
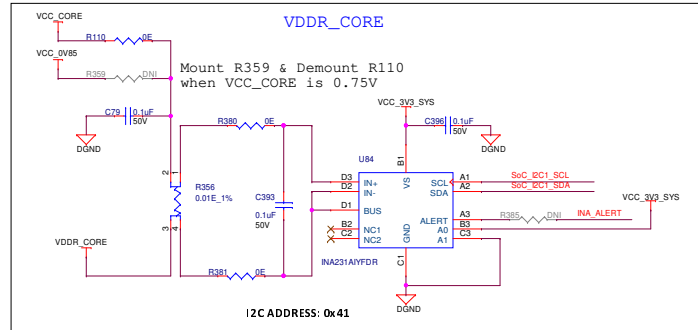
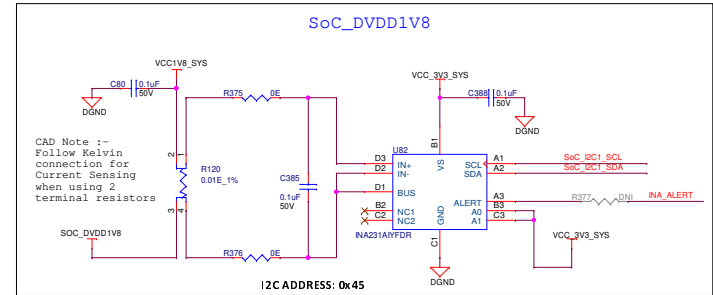


SOC POWER SUPPLY PMIC		
Size	PROC136A1	Rev
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CURRENT MONITORING DEVICES



D-Note :-
Note the supply rail name change across the shunt when optimizing the design (Deleting the current sense resistor)



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (1W_REX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

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Title CURRENT MONITORING DEVICES

Size	Rev
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SOC POWER

D-Note :-
Recommend implementing the voltage monitoring functionality using VMON_VSYS for early detection of supply failure. It is meant to be a power-fail indicator for the main input (higher) voltage rail that enters the PCB. For example, 5, 12, or 24 volts. The error associated with this monitor would require you to set the threshold significantly lower than the nominal to avoid false trigger. Refer System Power Supply Monitor Design Guidelines section of the data sheet

D-Note :-
Changing the core voltage is not allowed after the device has been released from reset. If you turn off the core supply, we expect you to turn off all power rails and ramp them down per the power-down sequence and wait until all supply rails decay below 300mv before turning on power again

D-Note :-
VDD_CORE and VDDR_CORE are recommended to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85V

D-Note :-
Add a filter
cap. Refer SOC
data sheet
section System
Power Supply
Monitor Design
Guidelines

D-Note :- Connecting 1.8V supply source directly to VPP continuously is not allowed

D-Note :-
It is very important to select an LDO with very fast transient response and connect its output to the VPP pin with a low loop inductance path to ensure it is able to source the high transient load, where the VPP pin never drops below the minimum operating voltage.

D-Note :-
Refer Pin connectivity requirements to connect the CSIO supplies (analog and core) when CSIO interface is not used
Ferrite and Bulk Caps are optional when CSIO is not used and Boundary scan functionality is required

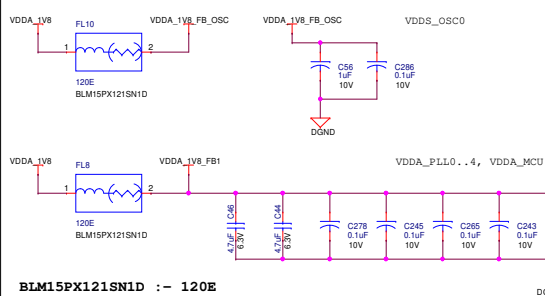
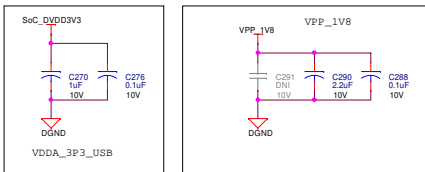
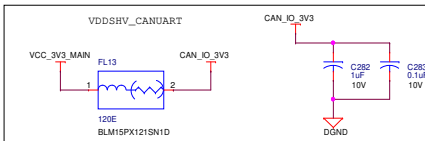
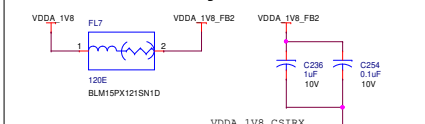
D-Note :-
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialize any time and the USB calibration procedure does not happen. Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

D-Note :-
A Trace connected to SOC is effectively an antenna that will pick up noise. A potential will be generated on the signal when noise couples into the antenna. This potential will be largest on the highest impedance end of the signal. By placing a pull-up or pull-down near the SOC pin, we force the highest potential to the open-circuit end of the signal rather than the SOC end of the signal.

b-Note :- Common SOC LVCMOS I/O interface guidelines
 1. Most of the SOC I/Os are not fail-safe. No input should be applied before supply ramps.
 2. SOC LVCMOS inputs have minimum slew rate requirements specified
 3. SOC I/O buffers are off during Reset. A pull is required near to the attached device being driven by the SOC I/Os
 4. When a trace is not a trace connected and not being actively driven needs a parallel pull.
 When adding pull is not feasible, ensure the traces are routed away from noisy signals

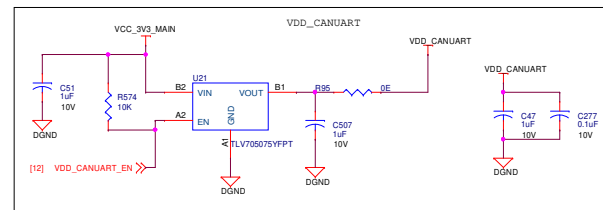
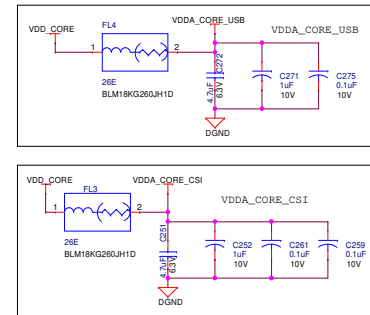
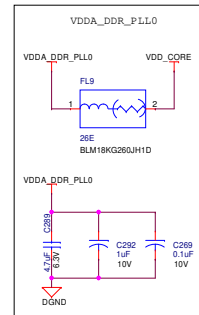
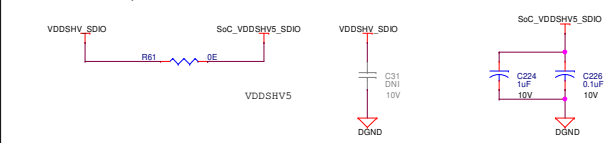
D-Note :-
Select capacitor with ESR < 1 Ω
Ensure the PCB loop inductance is < 2.5 nH
Select 0201 package or smallest possible package
Refer SOC Data sheet

1.8V Analog SUPPLY



BLM15PX121SN1D :- 120E
2A @ 85 deg C
1.1A @ 125 deg C

3.3V/1.8V MMC1 SUPPLY



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Title	SOC POWER
-------	-----------

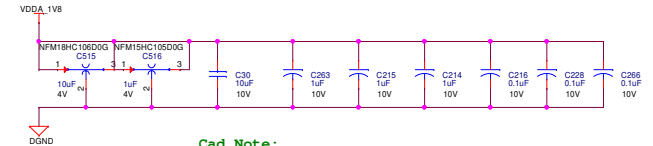
Size	PROC135A1
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Date: Thursday, July 24, 2025

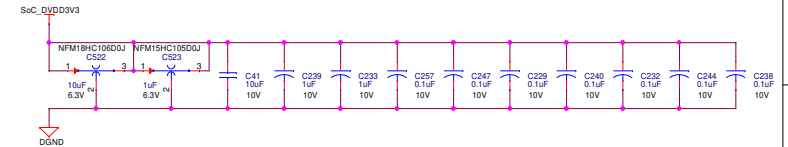
	Rev
	A1

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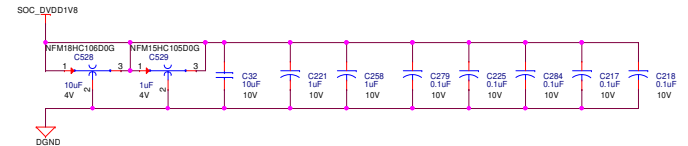
SOC VSS



Cad Note:
Place 0.1 uF caps near to SoC pins



Cad Note:
Place 0.1 uF caps near to SoC pins



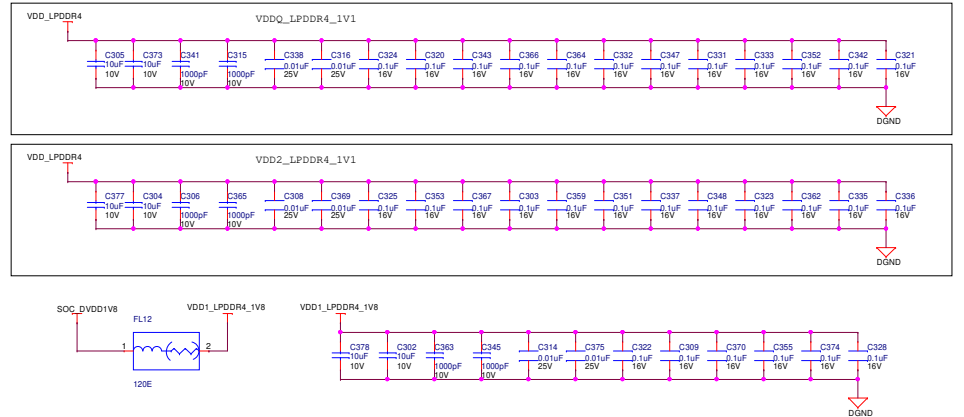
Cad Note:
Place 0.1 uF caps near to SoC pins

U18Q		
A1	VSS	Y9
A10	VSS	Y5
A13	VSS	Y3
A22	VSS	Y15
A27	VSS	Y12
A4	VSS	W5
A6	VSS	W6
AA11	VSS	W2
AA14	VSS	W4
AA2	VSS	W14
AA3	VSS	W11
AA8	VSS	V9
AB1	VSS	V7
AB12	VSS	V5
AB15	VSS	V3
AB18	VSS	V20
AB22	VSS	V1
AB3	VSS	V8
AB5	VSS	V6
AB9	VSS	V4
E3	VSS	U9
B5	VSS	U16
B7	VSS	U7
C4	VSS	U15
D11	VSS	U12
D10	VSS	U10
D2	VSS	U3
D4	VSS	U17
E1	VSS	T15
E5	VSS	T1
F11	VSS	R8
F12	VSS	R4
F16	VSS	R2
F2	VSS	R16
F4	VSS	R14
G12	VSS	R7
G17	VSS	P17
G3	VSS	P20
G5	VSS	P17
G6	VSS	P15
H1	VSS	P13
H11	VSS	P11
H16	VSS	N8
H2	VSS	N16
H4	VSS	N14
J12	VSS	N12
J17	VSS	N10
J3	VSS	M7
K1	VSS	M1
K11	VSS	M4
K4	VSS	M17
K7	VSS	M11
K9	VSS	L3
L12	VSS	L5
L14	VSS	L20

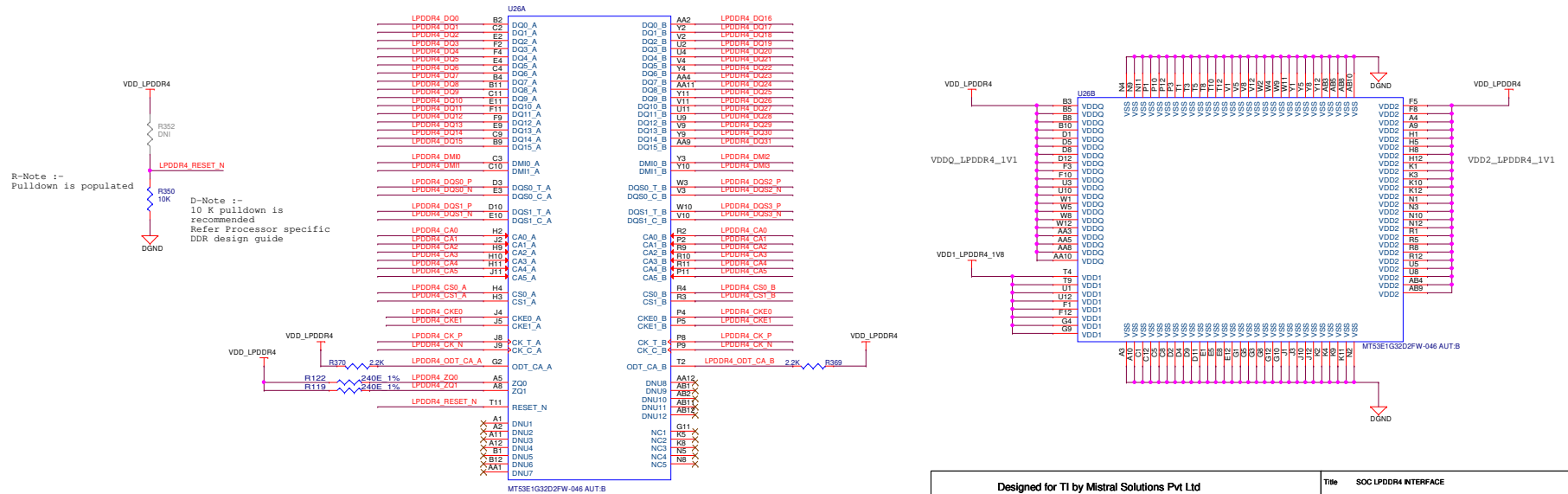
SOC LPDDR4 INTERFACE



LPDDR4 POWER DECAPS



LPDDR4 DEVICE



SOC - MMC Interface

D-Note :-
OE provision on MMC0_CLK
helps improve signal integrity

D-Note :-
MMC0 interface is compliant with the
JEDEC eMMC electrical standard v5.1
(JESD84-B51)

CAD Note :-
Place SOC clock output
pulldown resistor near to
the clock input pin of the
attached (memory) device

```
R-Note :-
What is the reason we selected
pulldown instead of pullup for EMMC,
SD card or other peripherals?
Because there are cases where the
clock is stopped or paused in a low
logic state and the pull-down option
is consistent with this logic state.
```

D-Note :-
The GPIO reset option makes it possible for software to reset the attached device (eMMC or OSPI or SD card or OLDIO or EPHY) without resetting the entire processor if there is a case where the peripheral becomes unresponsive.

D-Note :-
You could eliminate the GPIO option and only use the reset output (Warm or cold), where software forces a warm reset if the peripheral becomes unresponsive. However, this will reset the entire device rather than trying to recover the specific peripheral without resetting the entire device.

D-Note :-
In case ANDING logic is not used and the processor Main Domain warm reset status output (RSETSTATZ) is used to reset the attached device, ensure the IO voltage level of the attached device matches the eMMC/IOVOLTIO voltage level. A level translator is recommended to match the IO voltage level. A resistor divider could be used alternatively, provided optimum impedance value of the resistor divider is used. If too high the rise/fall time of the eMMC reset input could be affected, introducing glitch which is too low it will cause the AM62x to source too much steady-state current during normal operation.

D-Note :-
This family of processor implements a soft PHY for eMMC interface. The pulls required for D0, Clock and other eMMC interface control signals are recommended to be implemented externally.

eMMC FLASH

D-Note :-
Add additional decaps as required
Refer SK-AM62P-LP schematics

D-Note :-
For D7..D1 eMMC device is expected to have the pullups enabled by default. The eMMC host/phy disables the eMMC device pullups and enables SOC internal pullups. Provision for external pullups is optional or the pullups can be deleted

D-Note :-
Ok to use 50K or similar resistor for the parallel

D-Note :-
Ensure eMMC_RSTn Reset input is enabled in the eMMC device (eMMC non-volatile configuration space) for the reset logic to be functional

eMMC FLASH RESET

D-Note :-
Add a series resistor
input for isolation or
SK-AM62P-LP schematics

D-Note :-
Ok to use
standard 47K
or similar
resistor

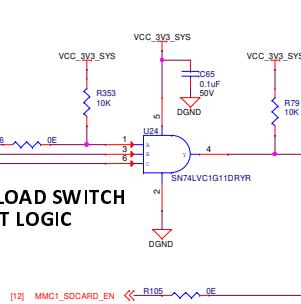
D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before
optimizing the reset ANDing logic. IO level mismatch
could cause supply leakage and affect SOC operation

SD CARD INTERFACE

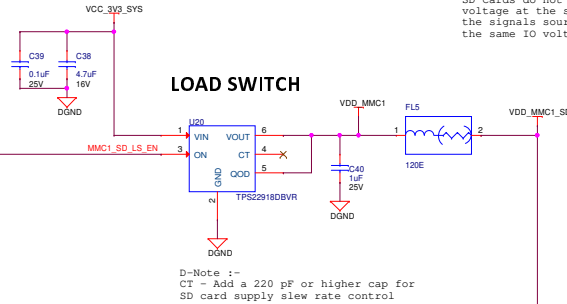
D-Note :-
This power switch, along with the reset logic, and the host IO power supply circuit is required to support UHS-I SD Cards which begins communications using 3.3V signal levels and later change to 1.8V signal levels when changing to one of the faster data transfer speeds. Cycling power to the SD Card is the only way to put it back into 3.3V mode since SD Cards do not have a reset pin. The host IO power supply must power off/on and change voltage at the same time as the SD Card. These circuits and the software driver operating the signals sourcing these circuits ensure both devices are off, or on and operating at the same IO voltage at the same time.

D-Note :-
ANDING logic could be optimized to 2 input AND gate
Use RESETSTATz and the SOC IO as inputs

SD CARD LOAD SWITCH RESET LOGIC



LOAD SWITCH

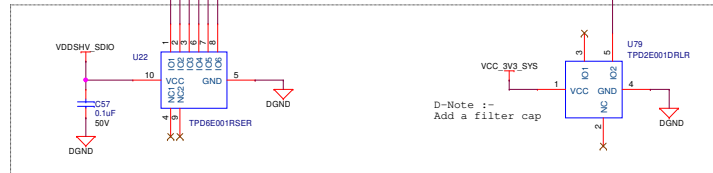
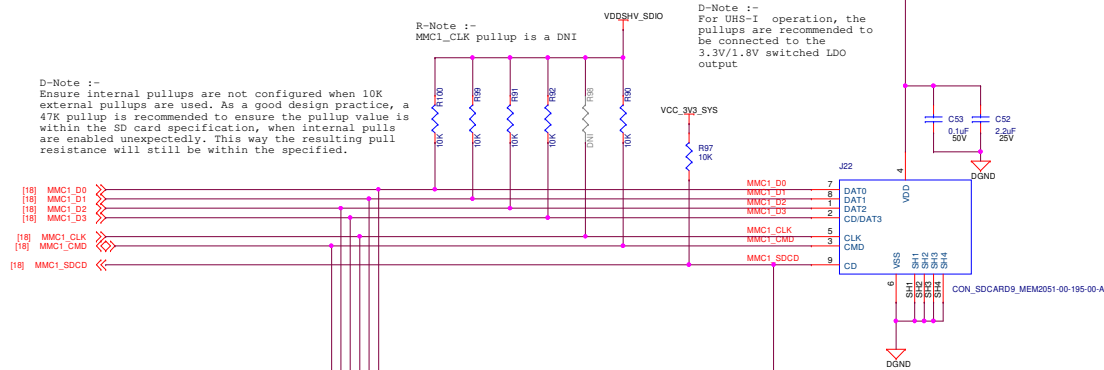


D-Note :-
CT - Add a 220 pF or higher cap for SD card supply slew rate control

D-Note :-
Ensure internal pullups are not configured when 10K external pullups are used. As a good design practice, a 47K pullup is recommended to ensure the pullup value is within the SD card specification, when internal pullups are enabled unexpectedly. This way the resulting pull resistance will still be within the specified.

R-Note :-
MMC1_CLK pullup is a DNI

D-Note :-
For UHS-I operation, the pullups are recommended to be connected to the 3.3V/1.8V switched LDO output



D-Note :-
Add a filter cap

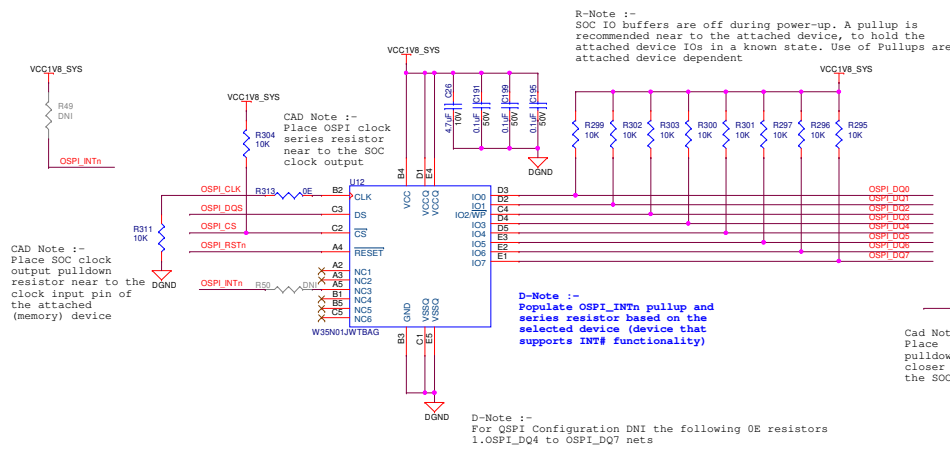
CAD Note :-
Place near SD Card Connector

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Title SD CARD INTERFACE		
Size	PROC135A1	Rev
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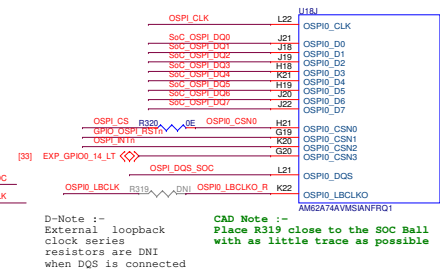
OSPI FLASH



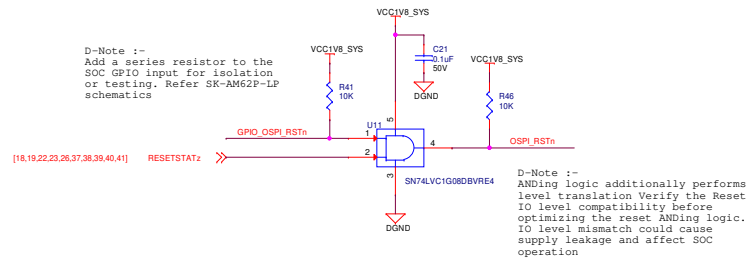
R-Note :-
These 0 0 resistors are used for configuring QSPI and OSPI
This is optional during custom board design

D-Note :-
Connecting OSPI interface to multiple devices is not recommended or supported

SOC OSPI INTERFACE



OSPI FLASH RESET



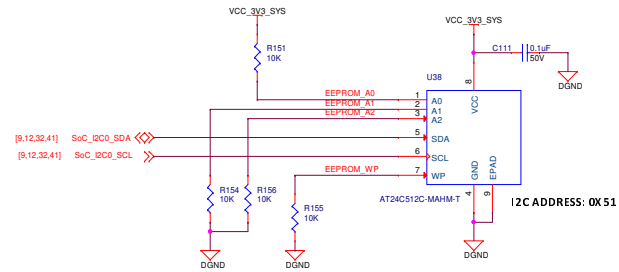
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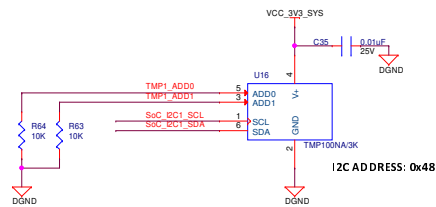
Title OSPI INTERFACE

Size	Rev
C	A1
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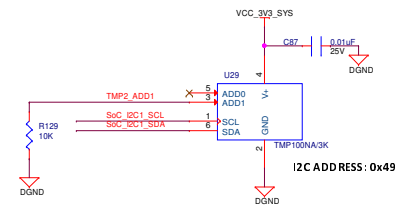
BOARD ID EEPROM



DIGITAL TEMPERATURE SENSORS



CAD NOTE: PLACE TEMP SENSOR CLOSE TO SoC



CAD NOTE: PLACE TEMP SENSOR CLOSE TO LPDDR4

[13,25,38,39,40,41] SoC_I2C1_SCL TP49
[13,25,38,39,40,41] SoC_I2C1_SDA TP50
Silk: SOC_I2C1

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Title BOARD ID EEPROM & TEMPERATURE SENSORS

Size	Rev
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Date: Thursday, July 24, 2025	Sheet 21 of 44

D-Note :-
The caps and values used are as per
the EPHY data sheet recommendations.

R-Note :-
Ferrite is DNI

D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-
Provide provision for series resistor based on EPHY for RX signals near to EPHY

D-Note :-
XI clock Input amplitude allowed
is 1.8V irrespective of the IO
supply. Use a CAP DIVIDER when
the clock amplified is 3.3V

[23]	CPSW_RGMII_INTn	→	R78	0E	CPSW_RGMII_INTn
[41]	CPSW_ETH_INTn	←	R108	0E	CPSW_RGMII_INTn
[23:31]	SoC_RGMII_MDC	→	R108	0E	CPSW_RGMII_MDC
[23:31]	SoC_RGMII_MDIO	↔	R107	0E	CPSW_RGMII_MDIO

D-Note :-
Add a series resistor to the SOC GPIO input for isolation or testing. Refer SK-AM62P-LP schematics

R-Note :-
Pullup is enabled for SOC GPIO input
RESETSTATz series resistor is DNI

D-Note :-
ANDing logic could be optimized to 2 input AND gate Use RESETSTATz (or PORz_OUT) and the SOC IO as inputs

D-Note :-
ANDING logic additionally performs level translation Verify the Reset IO level compatibility before optimizing the reset ANDING logic. IO level mismatch could cause supply leakage and affect SOC operation

```
PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns
```

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TEXAS
INSTRUMENTS



MISTRA

Title	CPSW RGMII_1 ETHERNET PHY
-------	---------------------------

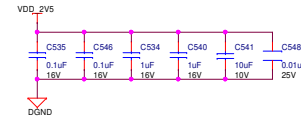
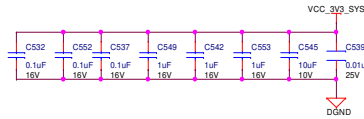
Size	PROC135A1
C	

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	Rev
	A1

CPSW3G RGMII 2 - ETHERNET PHY

D-Note :-
The caps and values used are
as per the EPHY data sheet
recommendations.



D-Note :-
Refer to DP83867ERG2-R-EVM when using LAN
Discrete Transformer Module and RJ45 connector

D-Note :-
Verify the power sequence
requirements for Two-Supply
Configuration and Three-Supply
Configuration

R-Note:-
Ferrite is DNI

RJ45 CONNECTOR WITH INTEGRATED MAGNETICS

D-Note :-
XI clock Input amplitude
allowed is 1.8V
irrespective of the IO
supply. Use a CAP DIVIDER
when the clock amplified
is 3.3V

D-Note :-
Provide provision for
Series resistor based on
EPHY selected for RX
signals near to EPHY

[2,31] SoC_RGMII_MDC

[2,31] SoC_RGMII_MDIO

D-Note :-
Add a series resistor to the
SOC GPIO input for isolation
or testing Refer SK-AM62P-LP
schematics

[39] GPIO_CPSW2_RST
[19,22,26,41] PORz_OUT
[18,19,20,22,26,37,38,39,40,41] RESETSTATz

R-Note :-
Pullup is enabled for SOC GPIO input
RESETSTATz series resistor is DNI

D-Note :-
ANDing logic could be
optimized to 2 input AND
gate. Use RESETSTATz (or
PORz_OUT) and the SOC IO
as inputs

D-Note :-
ANDing logic additionally
performs level translation
Verify the Reset IO level
compatibility before
optimizing the reset ANDing
logic. IO level mismatch could
cause supply leakage and
affect SOC operation

PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

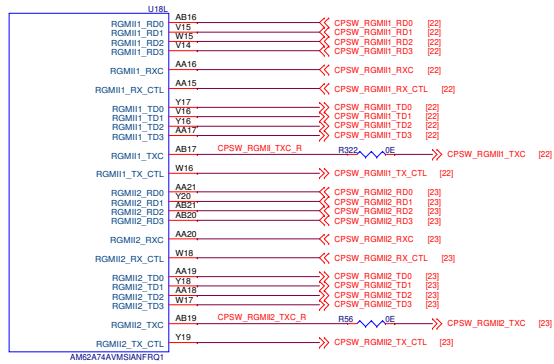
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Title CPSW3G RGMII_2 ETHERNET PHY

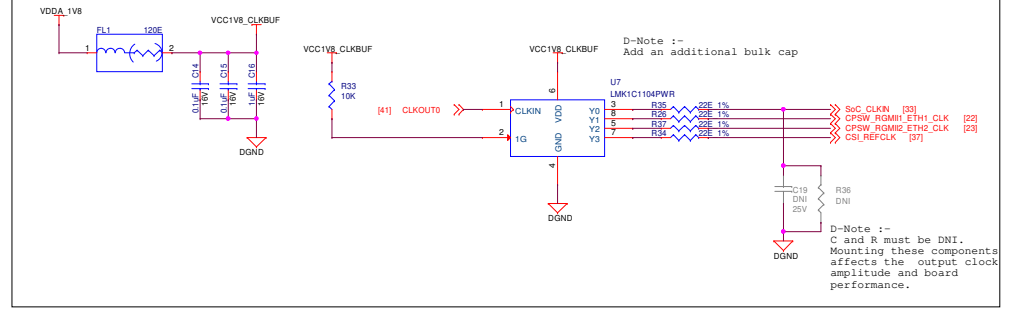
Size	Rev
C	A1
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SOC MAC INTERFACE



D-Note :-
Add series resistors 22.0 on the Ethernet interface TX (TDx) signals near to the SOC

CLOCK BUFFER FOR SOC AND ETHERNET PHYS

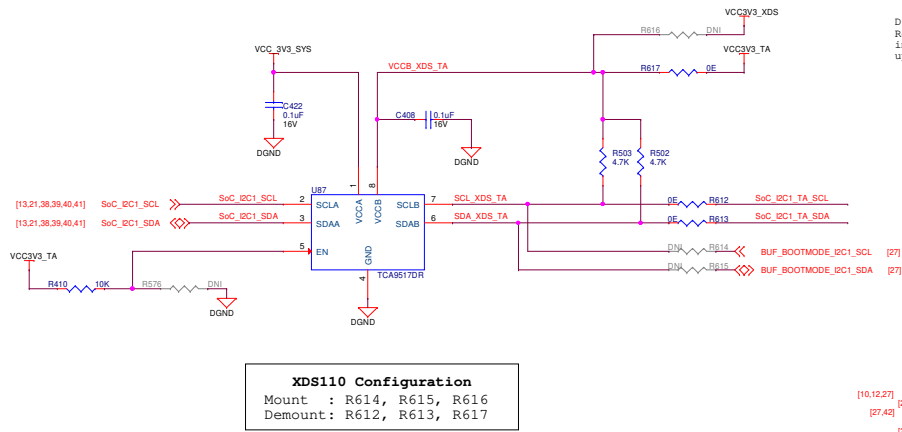


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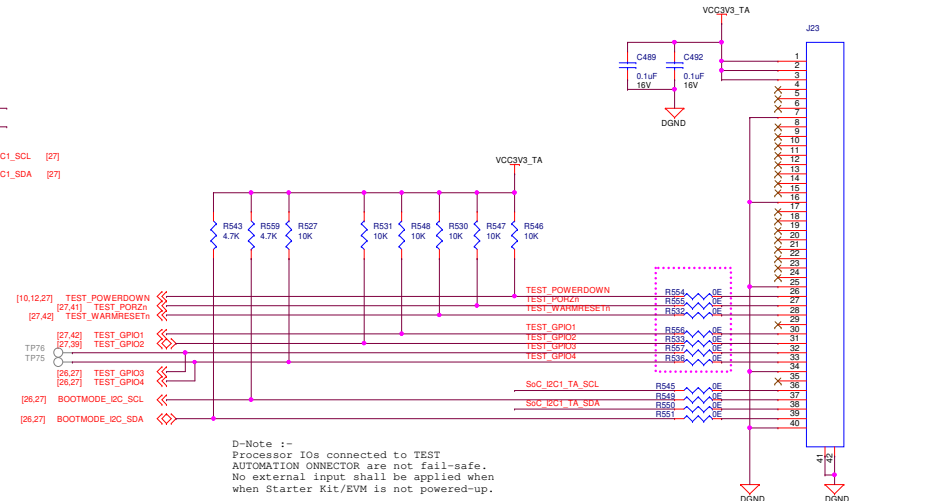
Title		Rev	
SOC MAC INTERFACE, CLOCK BUFFER FOR SOC AND ETHERNET PHYS		A1	
Size	PROC135A1		
C			
Date:	Thursday, July 24, 2025	Sheet	24 of 44

I2C BUS BUFFER



D-Note :-
Refer SK-AM62P-LP
Implementation for the latest
updates

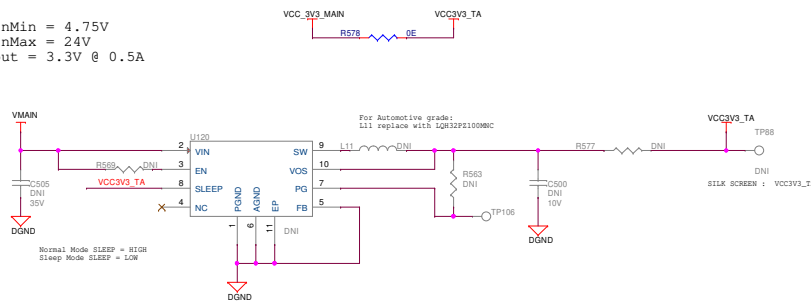
40-PIN TEST AUTOMATION HEADER



CON_FLEX_40X1_FH12A-40S-0.5SH
Silk: AUTOMATION HDR

TEST AUTOMATION BOARD POWER

VinMin = 4.75V
VinMax = 24V
Vout = 3.3V @ 0.5A



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SOC_GPIO1_23 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

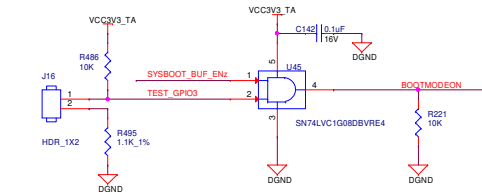
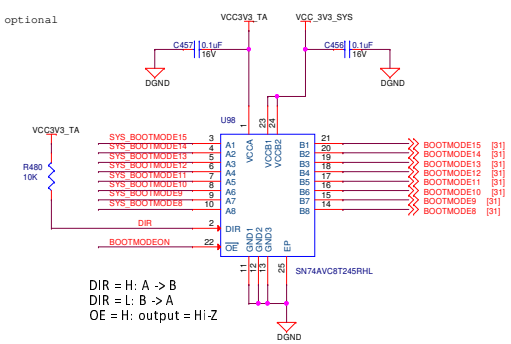
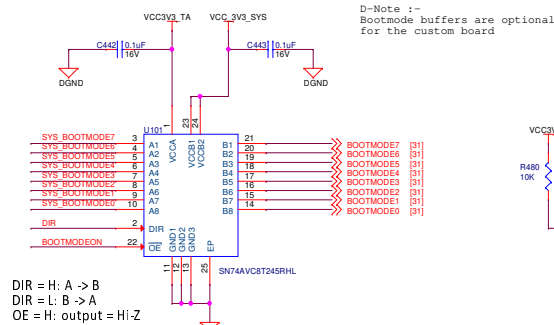
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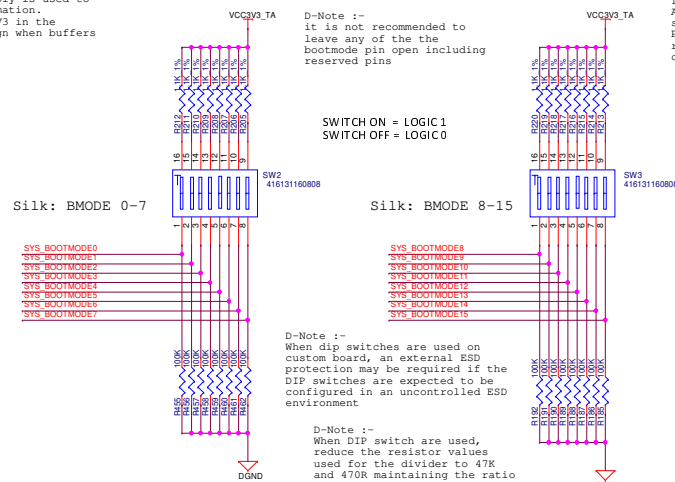
Title TEST AUTOMATION

Size	Rev
C	A1
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BOOT MODE BUFFERS



D-Note :-
VCC3V3_XDS_TA supply is used to support test automation.
Connect SOC_DVDD3V3 in the custom board design when buffers are not used



D-Note :-
Dip switch is optional and used on the SK
for ease of configuration
A pullup or pulldown resistor can be used to
set the BOOTMODE configuration
Provide provision for Pullup and Pulldown
resistors for the bootmode pins that have
configuration capability

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. ETHERNET
6. USB0 DPU
7. USB0 MS

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Title	BOOT MODE BUFFER & SWITCHES
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Size	
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C	PROC135A1
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Date: Thursday, July 24, 2025

	Rev
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A1

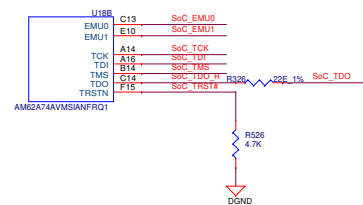
Sheet 26 of 44

D-Note :-
Please follow SK-AM62P-LP
implementations for latest
updates on XDS110

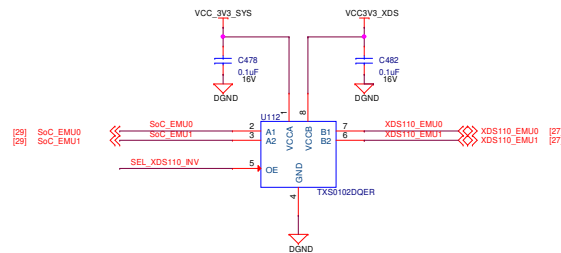
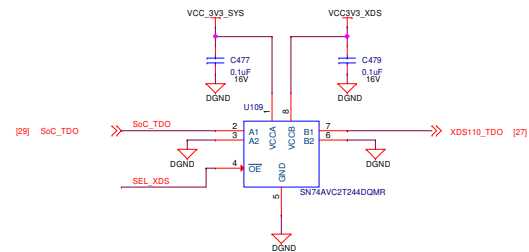
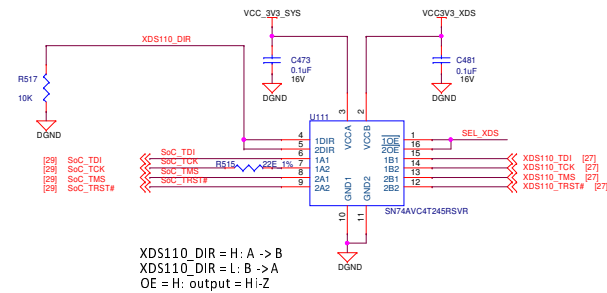
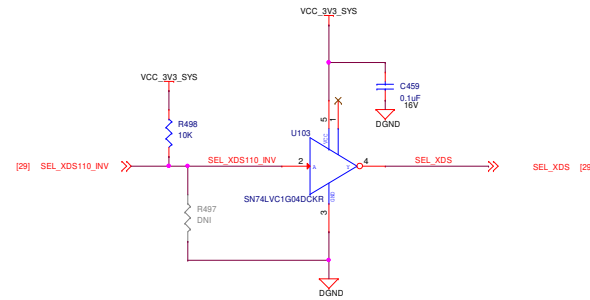


Title				XDS110 DEBUGGER			
Size		PROC135A1				Rev	
C						A1	
Date:			Thursday, July 24, 2025		Sheet		27 of 44

SOC JTAG INTERFACE



BUFFER XDS110



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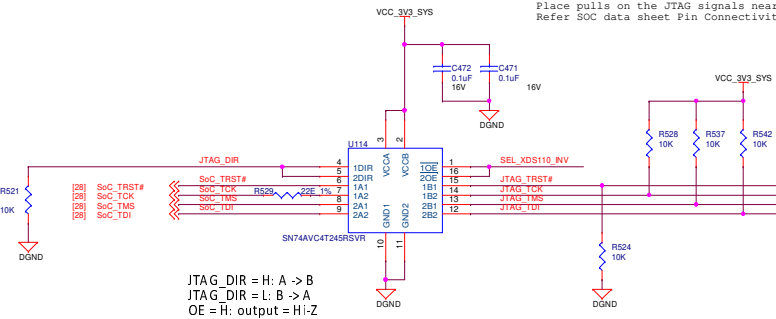


Title JTAG BUFFER

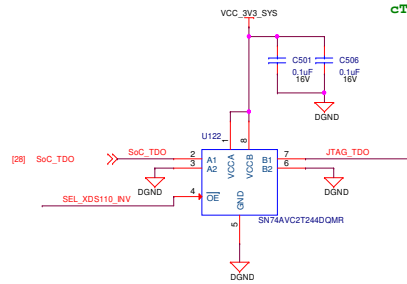
Size	Rev
C	A1
Date: Thursday, July 24, 2025	Sheet 28 of 44

cTI20 JTAG BUFFERS

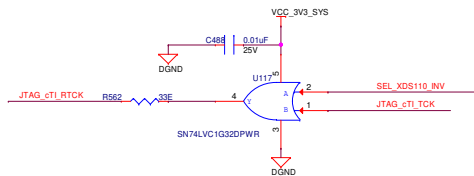
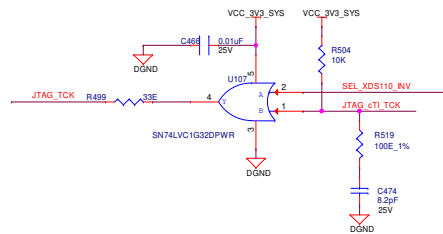
D-Note :-
Place pulls on the JTAG signals near to the SOC
Refer SOC data sheet Pin Connectivity Requirements section



CAD NOTE: Buffers U114 and U122 need to be placed closer to the cTI-20pin connector J19 to reduce Stub length of the JTAG signals.

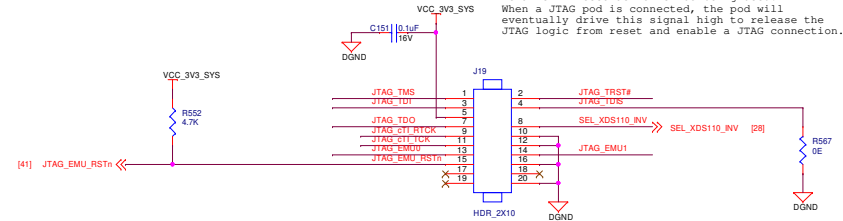


JTAG CLOCK BUFFER

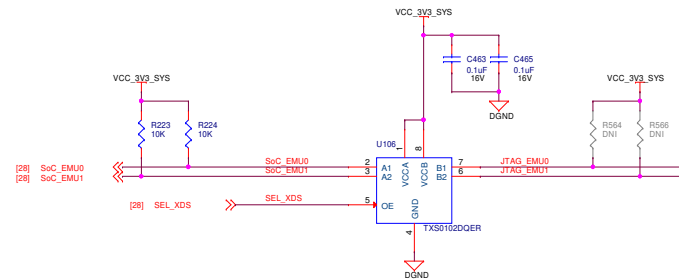


JTAG 20 PIN cTI CONNECTOR

D-Note :-
TRSTn is the reset to the JTAG logic. For normal operation, this is pulled low, and thus the JTAG remains in reset as it is not being used. When a JTAG pod is connected, the pod will eventually drive this signal high to release the JTAG logic from reset and enable a JTAG connection.



Silk: cTI



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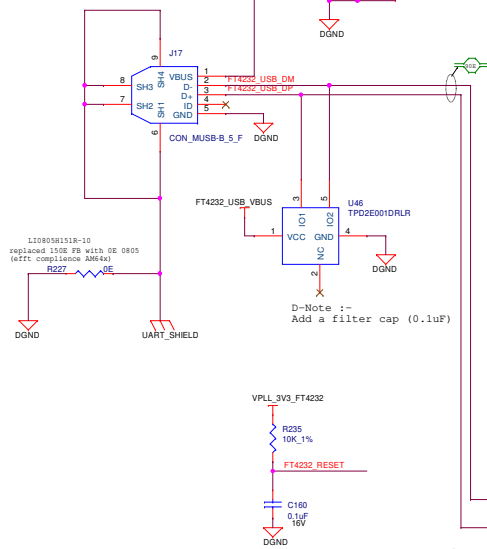


Title JTAG 20 PIN cTI CONNECTOR

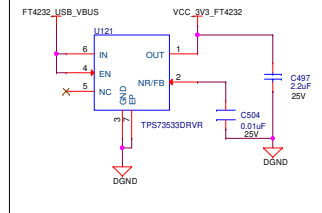
Size	Rev
C	A1
Date: Thursday, July 24, 2025	Sheet 29 of 44

FT4232 UART TO USB BRIDGE

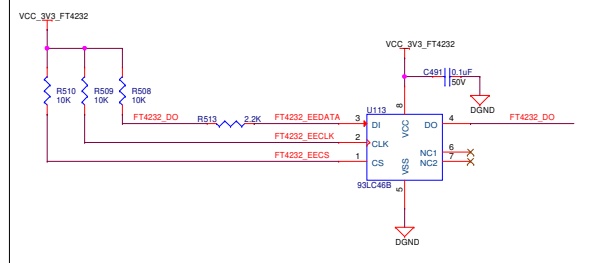
Silk: UART



FT4232: 5V to 3.3V@500mA LDO

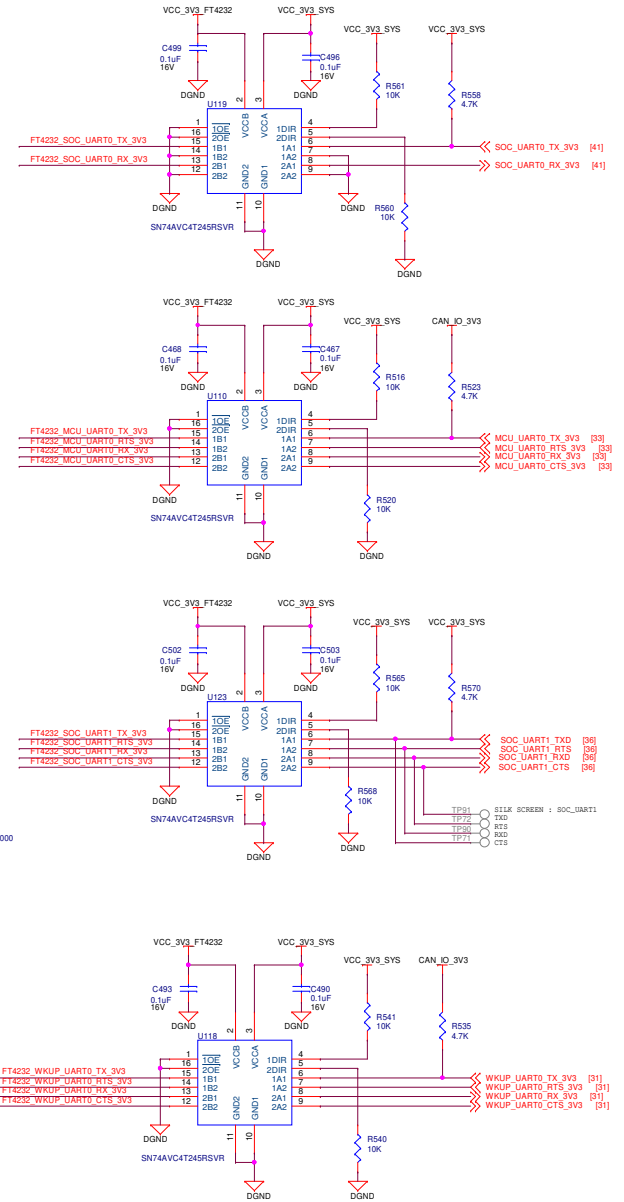


EEPROM



D-Note :-
Follow SK-AM62P-LP for latest
FT4232 implementations

R-Note :-
Verify the implementation with
the device manufacturer



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Title FT4232 UART TO USB BRIDGE

Size PROC135A1

C

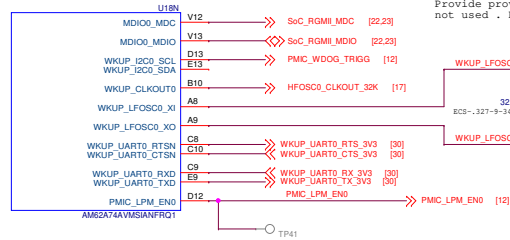
Date: Thursday, July 24, 2025

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Rev

A1

SOC WKUP DOMAIN



D-Note :-
Open-drain output type buffer I2C interfaces A pullup is recommended for Open-drain output type I2C interfaces irrespective of the IO configuration Refer pin connectivity table of SOC data sheet

D-Note :-
WKUP_LFOSCO has limited use case. Provide provision to ground XI when not used . Refer SOC data sheet

D-Note :-
The only LFOSCO register bits that should be changed by the customer are BP_C, PD_C, and CTRLMMR_WKUP_LFXOSC_TRIM[18:16], where PD_C is reset (0) to enable the oscillator and the BP_C bit is only set (1) to place the oscillator in bypass mode when using an LVCMOS clock source. The CTRLMMR_WKUP_LFXOSC_TRIM[18:16] bits are set based on the actual capacitance load applied to the crystal, as defined by the Load Capacitance Equation. The load capacitance range of the crystal will be half of the recommended capacitor value range, since there are connected in series with the crystals resonate circuit.

D-Note :-
Open-drain output type buffer I2C interfaces have slew rate requirement when pulled to 3.3 V. An RC is recommended for slew rate control. Refer SK-AM62P-LP schematics

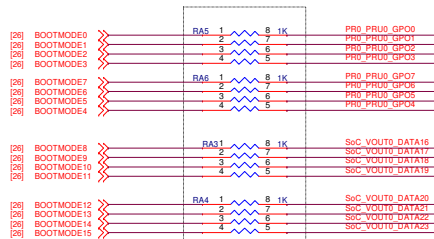
D-Note :-
SOC IO buffers used for GPMC interface signals are disabled during reset. The required pulls for the interfaced signals are provided on the GPMC interface card

D-Note :-
Refer SOC data sheet for the recommended circuit configuration during preproduction PCB and the production PCB

D-Note :-
Shorting of bootmode inputs (IOs) is not recommended or allowed since the IOs have alternate functions that could be configured after boot. Shorting the bootmode pins directly to VCC or ground directly is not recommended. Connect each of the bootmode pins through separate resistor. Choose the bootmode resistor value based on the use case (10K or similar)

D-Note :-
Reduce the series resistor value when buffer is not used to 0R
This resistor is used to isolate the alternate function during testing

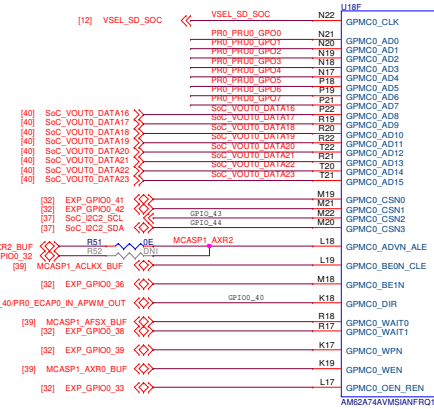
BOOTMODE PINS



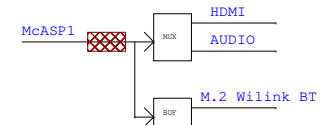
D-Note :-
1K Resistors are used to isolate the BOOTMODE control logic after the value is latched

SOC GPMC INTERFACE

D-Note :-
Add a series resistor 0R when used as GPMC0_CLK



D-Note :-
Add a 22R at the output of MCASP1_ACLKX near to the SOC



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Title SOC WKUP & GPMC

Size PROC135A1

C

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Rev A1

USER EXPANSION CONNECTOR

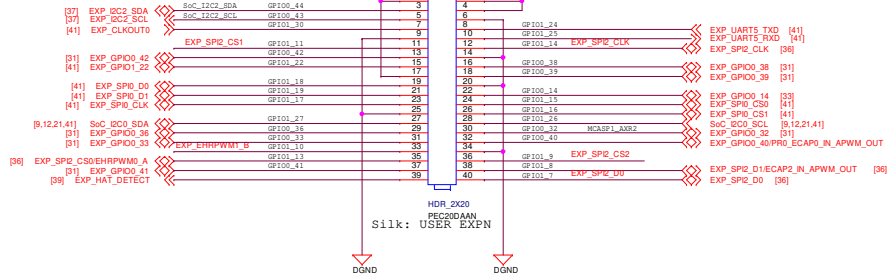
U18E	B30	EXP_EHRPWM1_B	GP101_10
MCASP0_AXR0	B18	EXP_SPI2_CS2	GP101_9
MCASP0_AXR1	B19	SOC_SPI2_OUT	GP101_8
MCASP0_AXR2	C19	SOC_SPI2_D0	GP101_7
MCASP0_AXR3			
MCASP0_ACLKX	A19	EXP_SPI2_CS1	GP101_14
MCASP0_ACLKR	A21	SOC_SPI2_CLK	SOC_SPI2_CLK [36]
MCASP0_AFSX	A20	REFCLK1_B	R55
MCASP0_AFSR	B21	SOC_SPI2_CS0	GP101_13

CAD Note :-
R55 (Series damping resistor) should be placed close to SOC

D-Note :-
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO

D-Note :-
Add a series resistor 22 0 for the SPI2 clock output near to the SOC

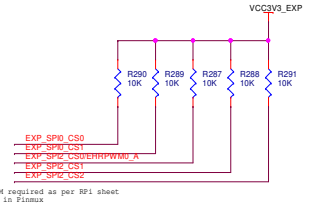
D-Note :-
These supplies are off by default
The supplies are controlled by the below load switches and needs to be enabled



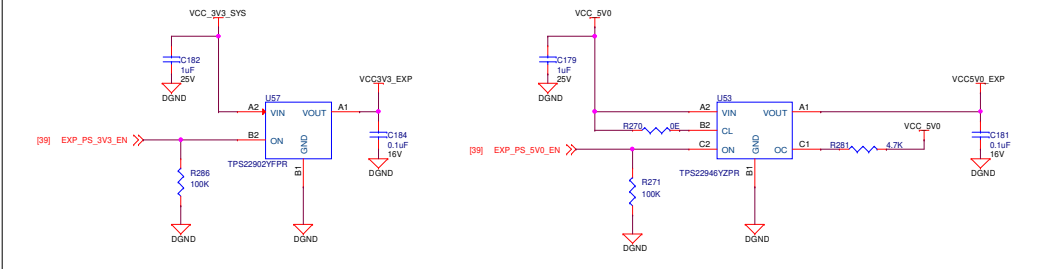
D-Note :-
Any SOC IO that has a trace connected but not being driven actively needs to be connected to an external pull

D-Note :-
Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)

D-Note :-
Processor IOs connected to USER EXPANSION CONNECTOR are not fail-safe.
No external input shall be applied when Starter Kit is not powered-up.



LOAD SWITCHES FOR USER EXPANSION CONNECTOR



R-Note :-

AM62A Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62A Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

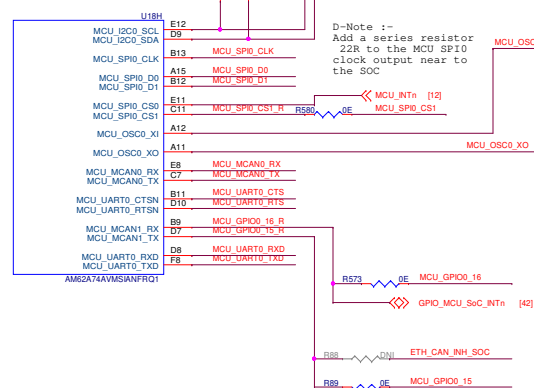
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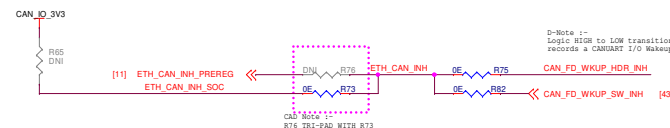
Title USER EXPANSION CONNECTOR

Size	Rev
C	A1
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D-Note :-
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO



D-Note :-
X0 should be grounded when
external oscillator is use
Refer SOC data sheet



D-Note :-
Logic HIGH to LOW transition on this signal
records a CANUART I/O Wakeup Event

D-Note :-
Connect the 25 MHz crystal directly to the SOC Xi and Xo pins (No Series or parallel resistors are recommended). The internal oscillator implements AGC (Automatic Gain Control) for amplitude control. Match the SOC and the EPHY crystal specs

D-Note :-
Refer Applications, Implementation, and Layout section of the data sheet for clock routing guidelines as below:
Clock Routing Guidelines
Oscillator Routing

D-Note :-
No HFOSC0 registers are required to be changed. These registers should remain in their default state.
Select the appropriate crystal circuit components that are compliant to the values defined in the MCU_OSC0 Crystal Circuit Requirements table. Read the Load Capacitance and Shunt Capacitance sections to select the appropriate crystal circuit components.

D-Note :-
MCU_OSQO has been validated only with a 25 Mhz clock source, so that is the only frequency supported. The datasheet shows MCU_OSQO not starting until after the core voltage because there are some cases where the oscillator may not start until VDD_CORE is valid. In most cases it will start as early as VDDOS_OSQO, but this may not always be the case. This diagram in the datasheet is showing the maximum start-up time, which must include the case where the delay is based on VDD_CORE being valid.

SOC-MCU_UART0 MUX

OEn	SEL	INPUT/OUTPUT An	
L	L (DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER

OEn	SEL	INPUT/OUTPUT An	
L	L (DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER

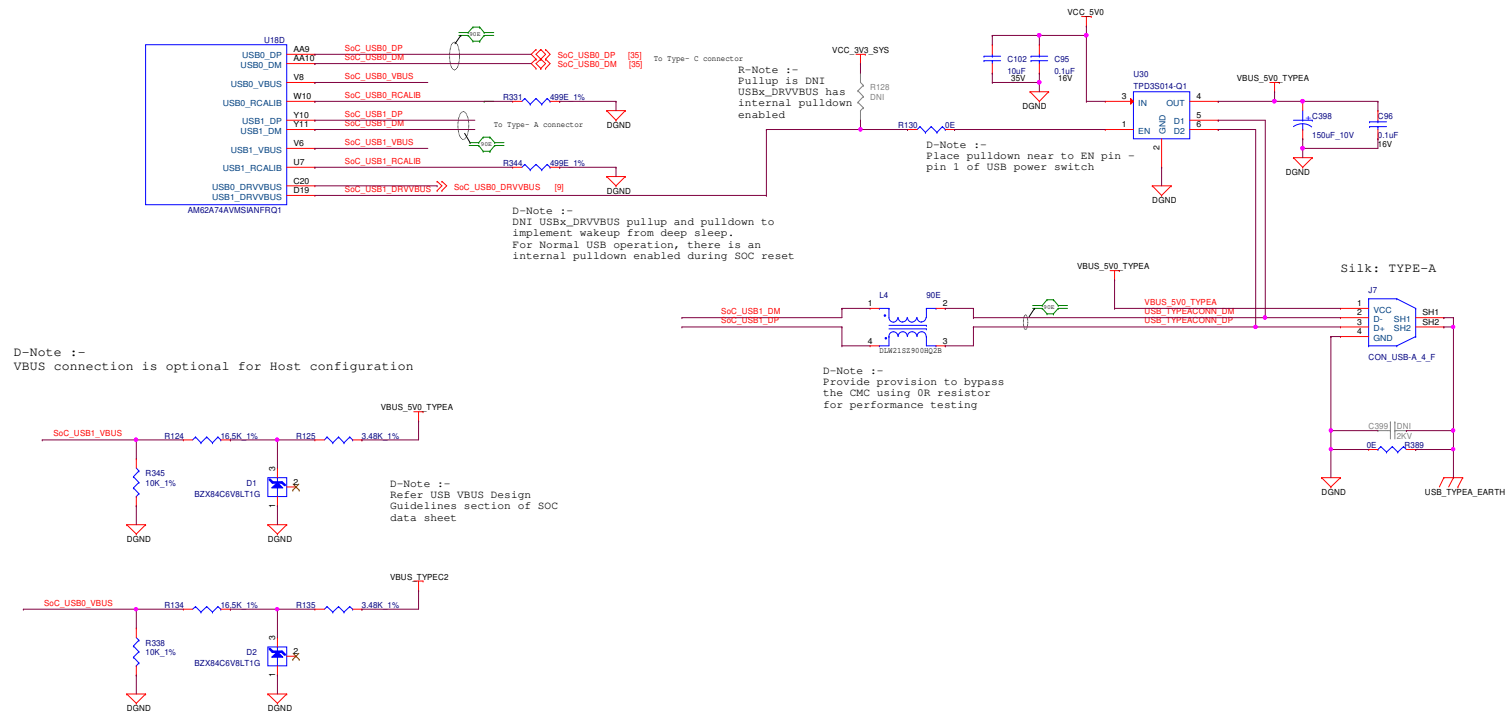
[illegible]

D-Note :-
Any SOC IO that has a trace connected but not being driven actively needs a parallel pull

D-Note :-
Processor I/Os connected to MCU
expansion CONNECTOR are not fail-safe.
No external input shall be applied when
when Starter Kit/EVM is not powered-up.

USB1 - USB 2.0 TYPE-A

D-Note :-
Use power switch with OC indication
Example TPS2051
Connect to a SOC IO for OC detection
Refer SK-AM62P-LP schematics



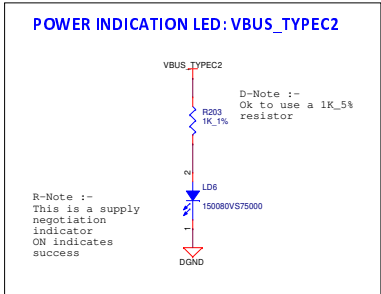
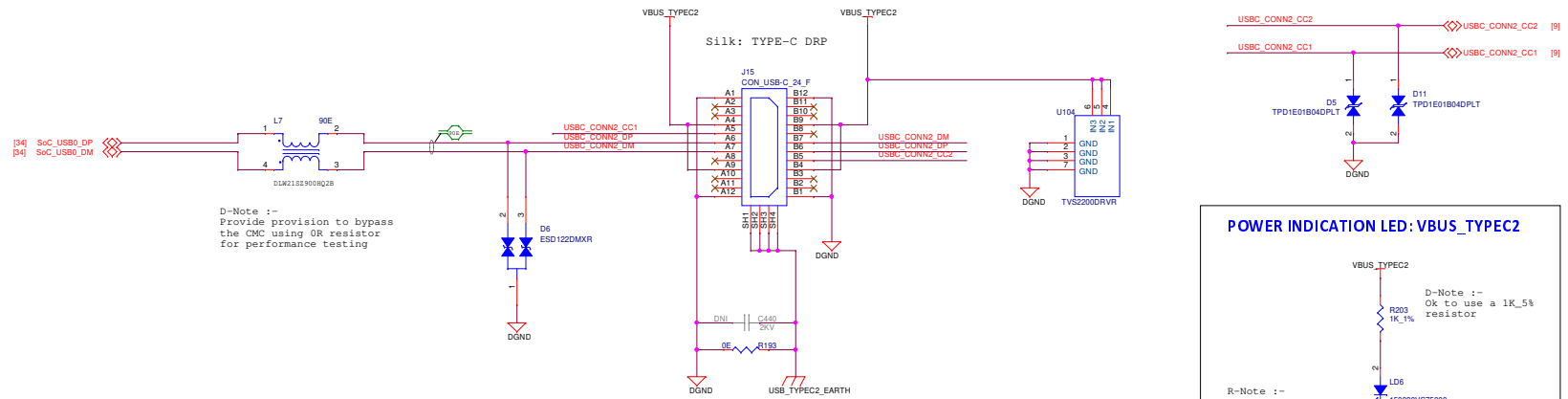
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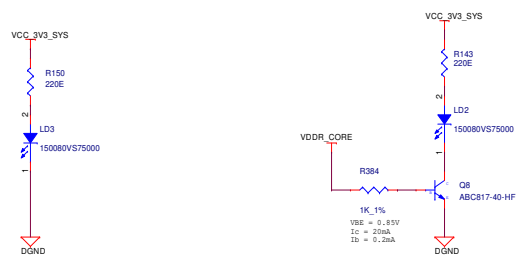
Title	USB1 TYPE-A
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Size	PROC135A1	Rev
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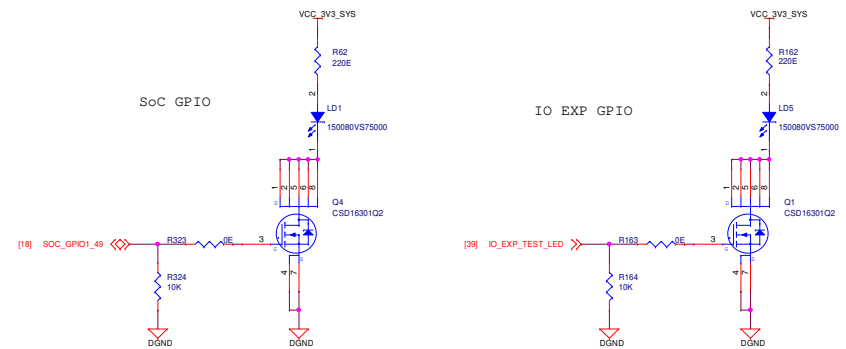
USB0 TYPE-C DRP



POWER RAIL LEDS



USER TEST LEDS

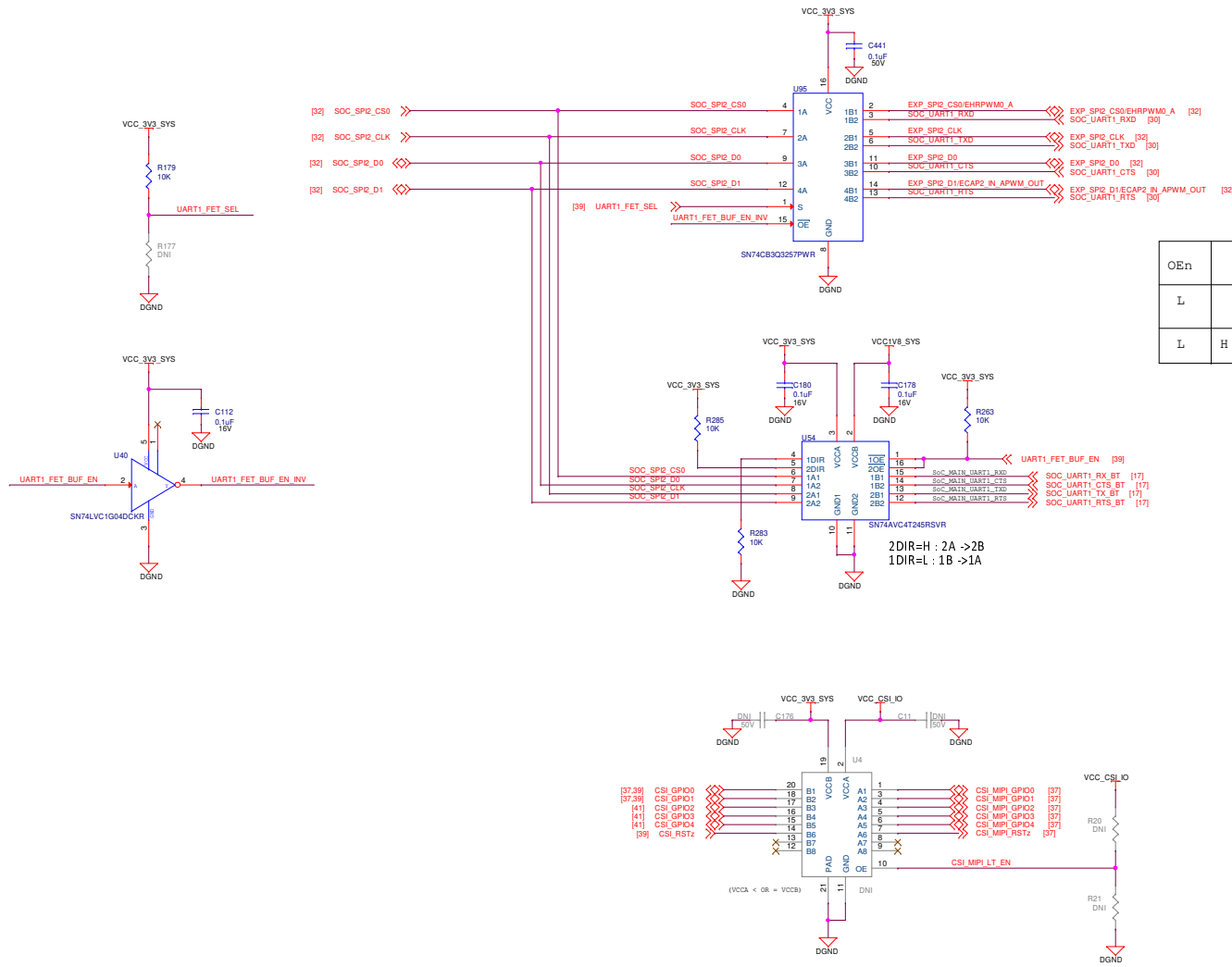


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Title: USB0 TYPE-C DRP & USER TEST LED		
Size	PROC135A1	Rev
C		A1
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SoC UART1 FET SWITCH & BUFFER



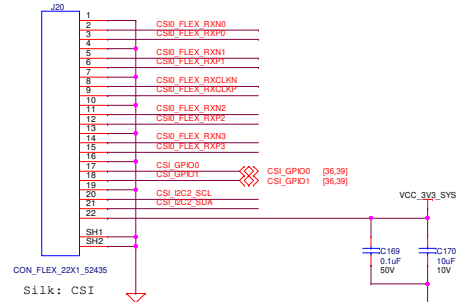
Designed for TI by Mistral Solutions Pvt Ltd



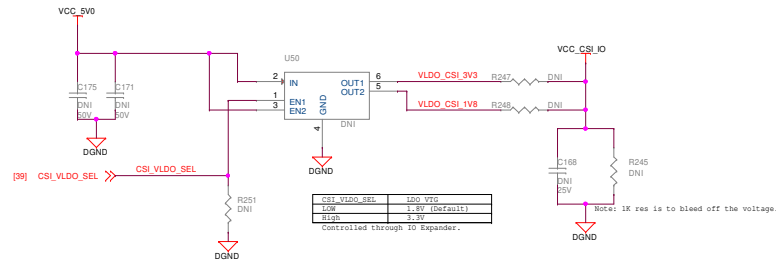
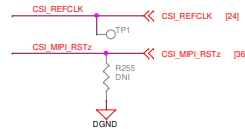
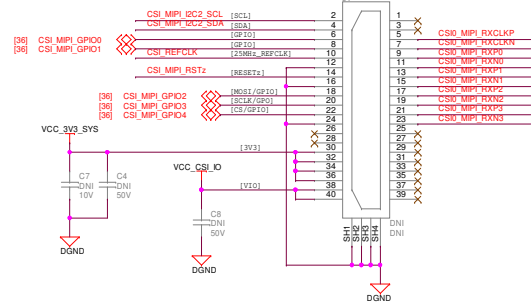
Title SoC UART1 FET SWITCH & BUFFER

Size	Rev
C	A1
Date: Thursday, July 24, 2025	Sheet 36 of 44

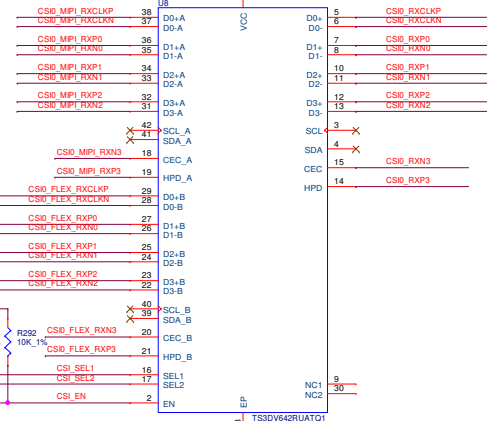
CSI INTERFACE



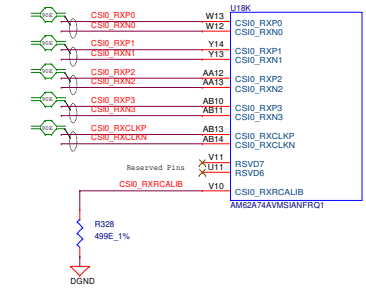
MIPI CONNECTOR



[39] CSI_SEL2
[39] CSI_EN



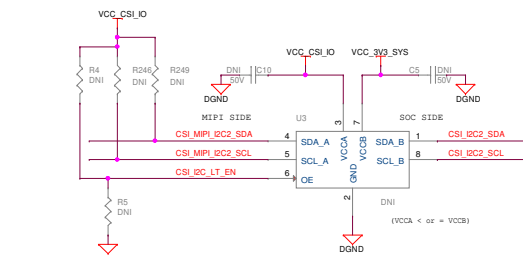
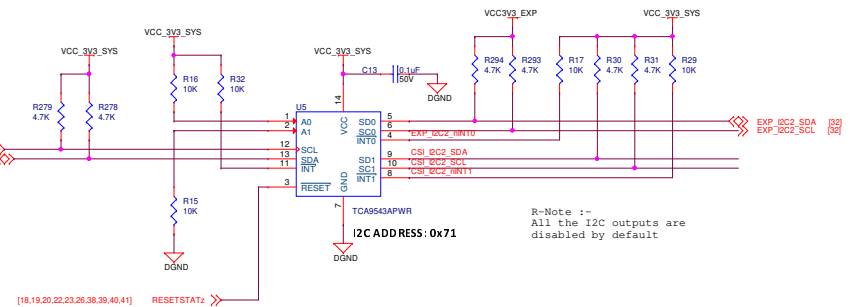
SOC CSI INTERFACE



CSI - 1:2 MUX : Truth Table

MUX_SEL_2	FUNCTION
LOW	INPUT<--A port [CSI-2 Connector - J1]
HIGH	INPUT<--B port [Flex Camera Connector - J20] (default)

I2C SWITCH FOR SoC_I2C2



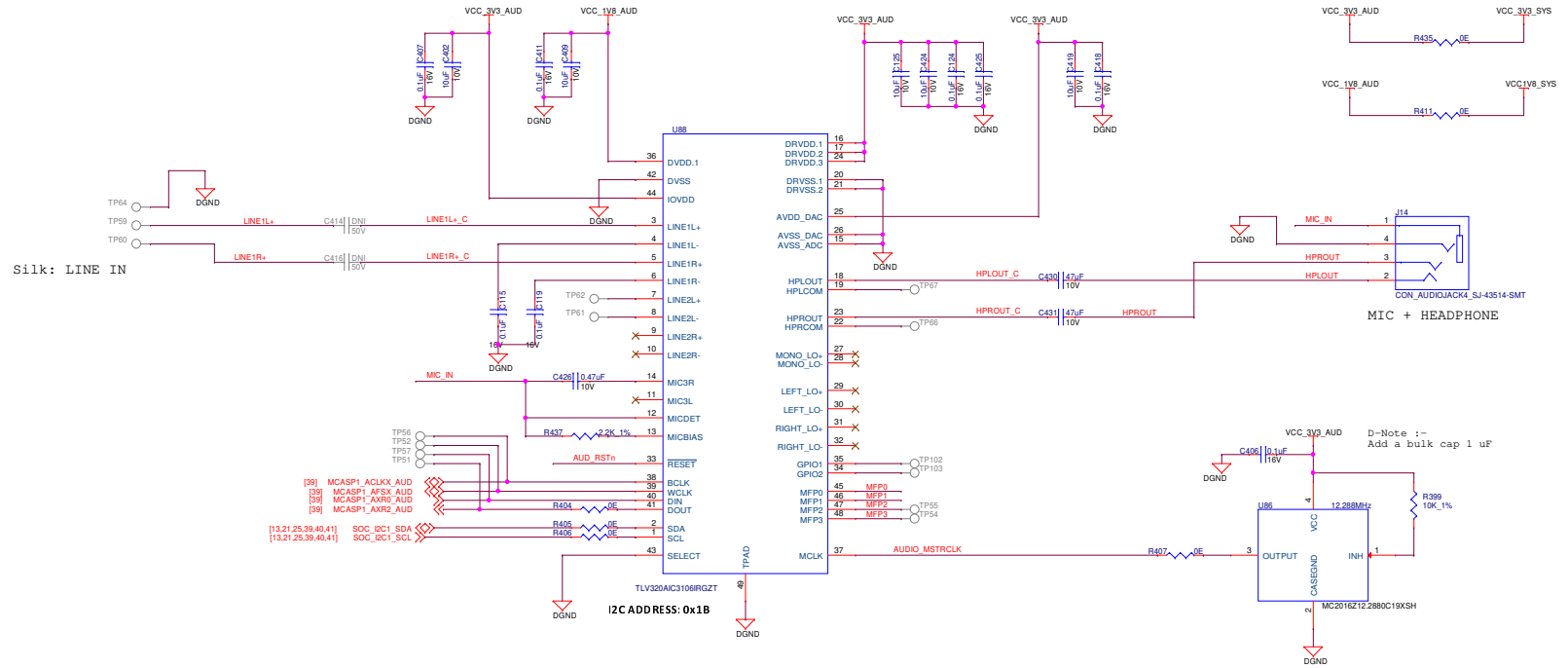
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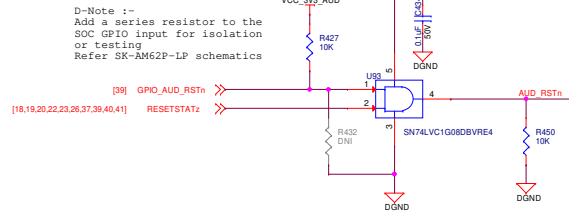
Title CSI INTERFACE

Size	Rev
C	A1
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AUDIO CODEC

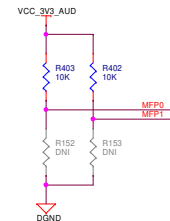


AUDIO CODEC RESET



CODEC I2C ADDRESS SELECTION

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B



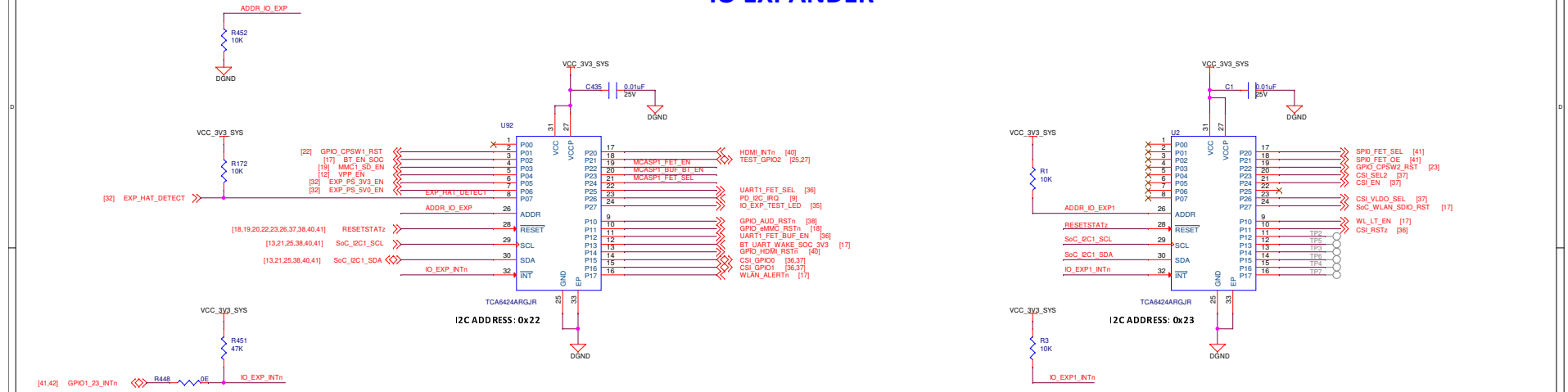
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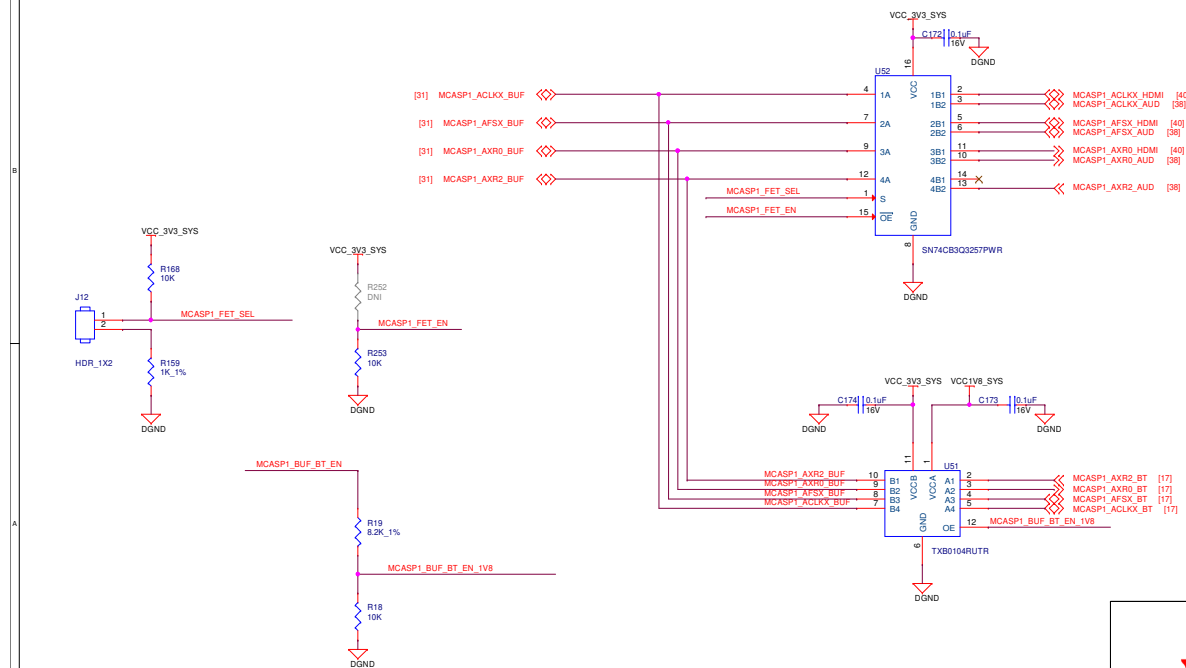
Title AUDIO CODEC

Size	Rev
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IO EXPANDER



McASP1 FET SWITCH & BUFFER



OEn	SEL	INPUT/OUTPUT An	
L	H (DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

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Title IO EXPANDER

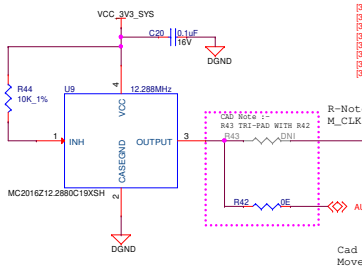
Size	Rev
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HDMI INTERFACE

R-Note :-
Verify the implementation with the device manufacturer

U18M	U22	SOC_VOUT0_DATA0
VOUT0_DATA0	U21	SOC_VOUT0_DATA1
VOUT0_DATA1	U20	SOC_VOUT0_DATA2
VOUT0_DATA2	U19	SOC_VOUT0_DATA3
VOUT0_DATA3	U18	SOC_VOUT0_DATA4
VOUT0_DATA4	U17	SOC_VOUT0_DATA5
VOUT0_DATA5	U16	SOC_VOUT0_DATA6
VOUT0_DATA6	U15	SOC_VOUT0_DATA7
VOUT0_DATA7	U14	SOC_VOUT0_DATA8
VOUT0_DATA8	U13	SOC_VOUT0_DATA9
VOUT0_DATA9	U12	SOC_VOUT0_DATA10
VOUT0_DATA10	U11	SOC_VOUT0_DATA11
VOUT0_DATA11	U10	SOC_VOUT0_DATA12
VOUT0_DATA12	U9	SOC_VOUT0_DATA13
VOUT0_DATA13	U8	SOC_VOUT0_DATA14
VOUT0_DATA14	U7	SOC_VOUT0_DATA15
VOUT0_DATA15	U6	SOC_VOUT0_DATA16
VOUT0_DATA16	U5	SOC_VOUT0_DATA17
VOUT0_DATA17	U4	SOC_VOUT0_DATA18
VOUT0_DATA18	U3	SOC_VOUT0_DATA19
VOUT0_DATA19	U2	SOC_VOUT0_DATA20
VOUT0_DATA20	U1	SOC_VOUT0_DATA21
VOUT0_DATA21	U0	SOC_VOUT0_DATA22
VOUT0_DATA22	U22	SOC_VOUT0_DATA23
VOUT0_DATA23	U21	SOC_VOUT0_DATA24
VOUT0_DATA24	U20	SOC_VOUT0_DATA25
VOUT0_DATA25	U19	SOC_VOUT0_DATA26
VOUT0_DATA26	U18	SOC_VOUT0_DATA27
VOUT0_DATA27	U17	SOC_VOUT0_DATA28
VOUT0_DATA28	U16	SOC_VOUT0_DATA29
VOUT0_DATA29	U15	SOC_VOUT0_DATA30
VOUT0_DATA30	U14	SOC_VOUT0_DATA31
VOUT0_DATA31	U13	SOC_VOUT0_DATA32
VOUT0_DATA32	U12	SOC_VOUT0_DATA33
VOUT0_DATA33	U11	SOC_VOUT0_DATA34
VOUT0_DATA34	U10	SOC_VOUT0_DATA35
VOUT0_DATA35	U9	SOC_VOUT0_DATA36
VOUT0_DATA36	U8	SOC_VOUT0_DATA37
VOUT0_DATA37	U7	SOC_VOUT0_DATA38
VOUT0_DATA38	U6	SOC_VOUT0_DATA39
VOUT0_DATA39	U5	SOC_VOUT0_DATA40
VOUT0_DATA40	U4	SOC_VOUT0_DATA41
VOUT0_DATA41	U3	SOC_VOUT0_DATA42
VOUT0_DATA42	U2	SOC_VOUT0_DATA43
VOUT0_DATA43	U1	SOC_VOUT0_DATA44
VOUT0_DATA44	U0	SOC_VOUT0_DATA45
VOUT0_DATA45	U22	SOC_VOUT0_DATA46
VOUT0_DATA46	U21	SOC_VOUT0_DATA47
VOUT0_DATA47	U20	SOC_VOUT0_DATA48
VOUT0_DATA48	U19	SOC_VOUT0_DATA49
VOUT0_DATA49	U18	SOC_VOUT0_DATA50
VOUT0_DATA50	U17	SOC_VOUT0_DATA51
VOUT0_DATA51	U16	SOC_VOUT0_DATA52
VOUT0_DATA52	U15	SOC_VOUT0_DATA53
VOUT0_DATA53	U14	SOC_VOUT0_DATA54
VOUT0_DATA54	U13	SOC_VOUT0_DATA55
VOUT0_DATA55	U12	SOC_VOUT0_DATA56
VOUT0_DATA56	U11	SOC_VOUT0_DATA57
VOUT0_DATA57	U10	SOC_VOUT0_DATA58
VOUT0_DATA58	U9	SOC_VOUT0_DATA59
VOUT0_DATA59	U8	SOC_VOUT0_DATA60
VOUT0_DATA60	U7	SOC_VOUT0_DATA61
VOUT0_DATA61	U6	SOC_VOUT0_DATA62
VOUT0_DATA62	U5	SOC_VOUT0_DATA63
VOUT0_DATA63	U4	SOC_VOUT0_DATA64
VOUT0_DATA64	U3	SOC_VOUT0_DATA65
VOUT0_DATA65	U2	SOC_VOUT0_DATA66
VOUT0_DATA66	U1	SOC_VOUT0_DATA67
VOUT0_DATA67	U0	SOC_VOUT0_DATA68
VOUT0_DATA68	U22	SOC_VOUT0_DATA69
VOUT0_DATA69	U21	SOC_VOUT0_DATA70
VOUT0_DATA70	U20	SOC_VOUT0_DATA71
VOUT0_DATA71	U19	SOC_VOUT0_DATA72
VOUT0_DATA72	U18	SOC_VOUT0_DATA73
VOUT0_DATA73	U17	SOC_VOUT0_DATA74
VOUT0_DATA74	U16	SOC_VOUT0_DATA75
VOUT0_DATA75	U15	SOC_VOUT0_DATA76
VOUT0_DATA76	U14	SOC_VOUT0_DATA77
VOUT0_DATA77	U13	SOC_VOUT0_DATA78
VOUT0_DATA78	U12	SOC_VOUT0_DATA79
VOUT0_DATA79	U11	SOC_VOUT0_DATA80
VOUT0_DATA80	U10	SOC_VOUT0_DATA81
VOUT0_DATA81	U9	SOC_VOUT0_DATA82
VOUT0_DATA82	U8	SOC_VOUT0_DATA83
VOUT0_DATA83	U7	SOC_VOUT0_DATA84
VOUT0_DATA84	U6	SOC_VOUT0_DATA85
VOUT0_DATA85	U5	SOC_VOUT0_DATA86
VOUT0_DATA86	U4	SOC_VOUT0_DATA87
VOUT0_DATA87	U3	SOC_VOUT0_DATA88
VOUT0_DATA88	U2	SOC_VOUT0_DATA89
VOUT0_DATA89	U1	SOC_VOUT0_DATA90
VOUT0_DATA90	U0	SOC_VOUT0_DATA91
VOUT0_DATA91	U22	SOC_VOUT0_DATA92
VOUT0_DATA92	U21	SOC_VOUT0_DATA93
VOUT0_DATA93	U20	SOC_VOUT0_DATA94
VOUT0_DATA94	U19	SOC_VOUT0_DATA95
VOUT0_DATA95	U18	SOC_VOUT0_DATA96
VOUT0_DATA96	U17	SOC_VOUT0_DATA97
VOUT0_DATA97	U16	SOC_VOUT0_DATA98
VOUT0_DATA98	U15	SOC_VOUT0_DATA99
VOUT0_DATA99	U14	SOC_VOUT0_DATA100

D-Note :-
Add a bulk cap 1uF

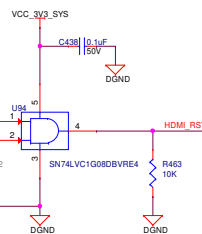


HDMI RESET

D-Note :-
Add a series resistor to the SOC GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

[39] GPIO_HDMI_RST#

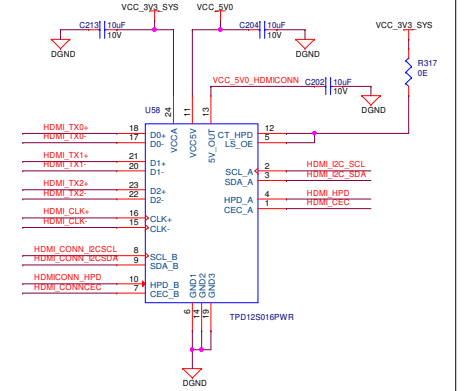
[18,19,20,22,23,26,37,38,39,41] RESETSTAT2



I2C ADDRESS: 0x3B, 0x3F, 0x62

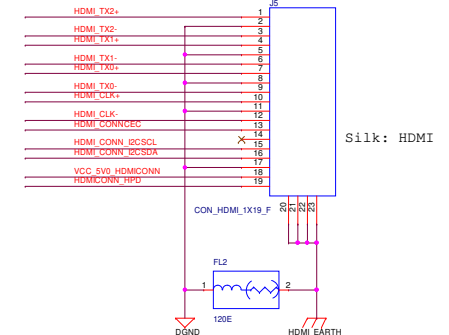
D-Note :-
Add a bulk caps

HDMI ESD DEVICE



R-Note :-
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.

HDMI CONNECTOR



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Title HDMI INTERFACE

Size PROC135A1

C

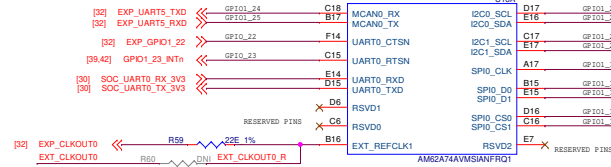
Date: Thursday, July 24, 2025

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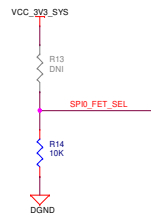
Rev

A1

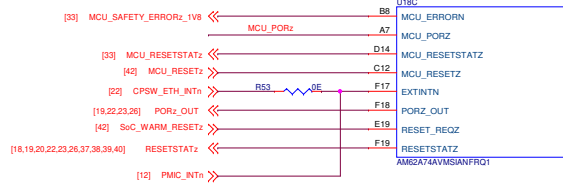
D-Note :-
The TXD and RXD net names for UART are reverse with respect to MCAN (Refer pin attributes section of the data sheet)
Take note while connecting



D-Note :-
Ext_Refclk1 used as Clkout0
A clock signal should always be connected point to point without any branches. When connecting Clkout0 to more than one (multiple) clock inputs, use a buffer with one input and multiple outputs.

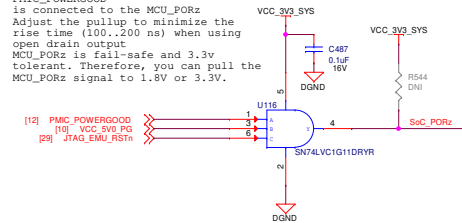


D-Note :-
Provision for a pull-down
Populate when attached device is connected
Refer SOC data sheet pin connectivity requirements



D-Note :-
Open drain output type IO EXTINTn has slew rate limit specified when pulled to 3.3V supply. Add an RC at the input. Refer TMS564EVM.

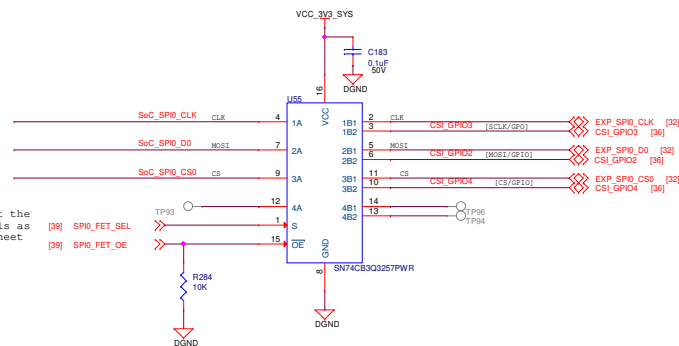
D-Note :-
MCU_PORz input have a maximum rise/fall time requirements when PMIC_POWERGOOD is connected to the MCU_PORz
Adjust the pullup to minimize the rise time (100..200 ns) when using open drain output
MCU_PORz is fail-safe and 3.3v tolerant. Therefore, you can pull the MCU_PORz signal to 1.8V or 3.3V.



SOC - GENERAL

SoC SPI0 FET SWITCH

D-Note :-
Verify and connect the unused data signals as per device data sheet

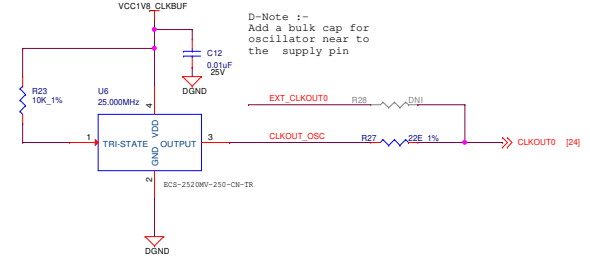


D-Note :-
Add a series resistor 22R for the SPI0 clock output near to the SOC

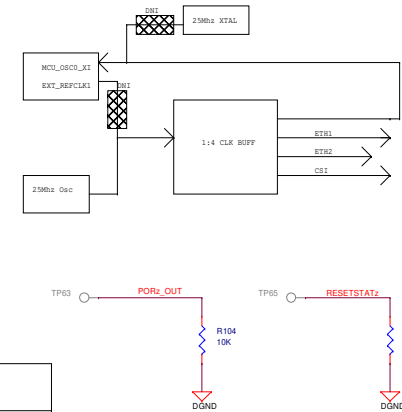
D-Note :-
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO

OSCILLATOR

D-Note :-
Refer SOC data sheet for oscillator specs



D-Note :-
Add a bulk cap for oscillator near to the supply pin

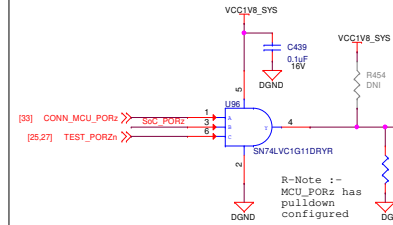


D-Note :-
Pull-down resistor on PORz_OUT and RESETSTATz is provided to hold the attached device in reset condition during SOC reset and power-up

OEn	SEL	INPUT/OUTPUT An	
L	L (DEFAULT)	An=nB1	EXP HDR
L	H	An=nB2	MIPI CSI

MCU POWER ON RESET

D-Note :-
It is recommended to connect the output from logic gate or discrete buffer (with fast rise time) as MCU_PORz input rather than slow rising open drain output.



D-Note :-
Not connecting a valid MCU_PORz could cause unpredictable and probably random behavior, since the device is not getting a valid reset, internal circuits would be in random states. Slow rising reset signal could cause glitches internal to the SOC reset circuit. Use a discrete buffer and have the fast rising output of the buffer drive the MCU_PORz is recommended

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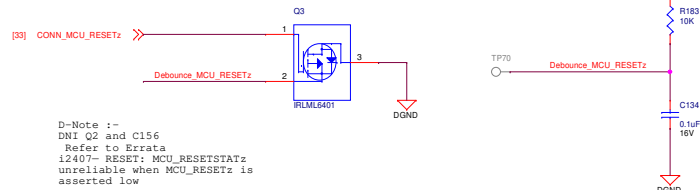


Title OSCILLATOR

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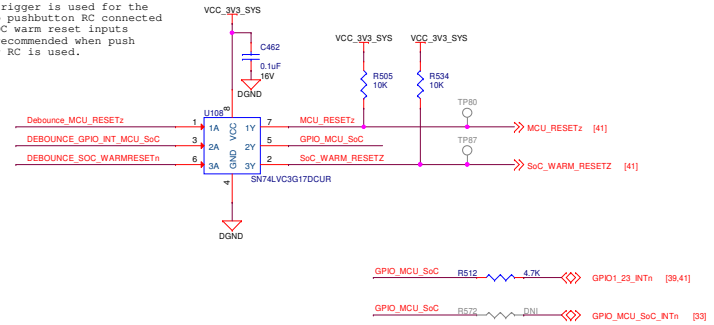
EXTERNAL RESET INPUT AND SCHMITT TRIGGER DEBOUNCE LOGIC

SOC MCU WARM RESET

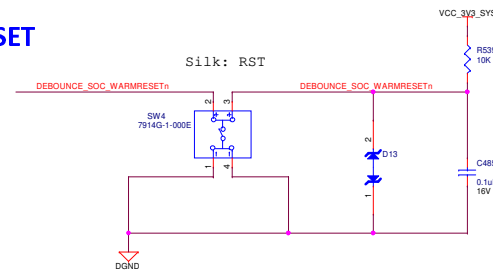
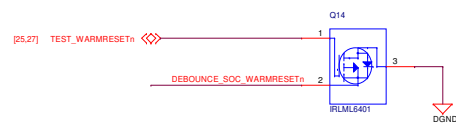


DEBOUNCE CIRCUIT

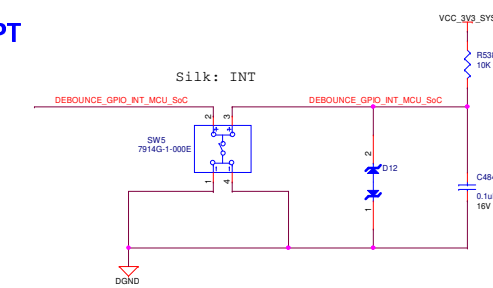
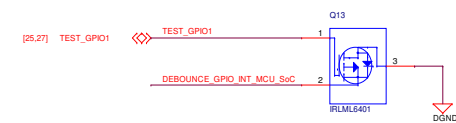
D-Note :-
LVCMOS inputs have slew rate
specifications
Schmitt trigger is used for the
slow ramp pushbutton RC
connected to the SOC warm reset inputs
This is recommended when push
button or RC is used.



SOC WARM RESET



USER INTERRUPT



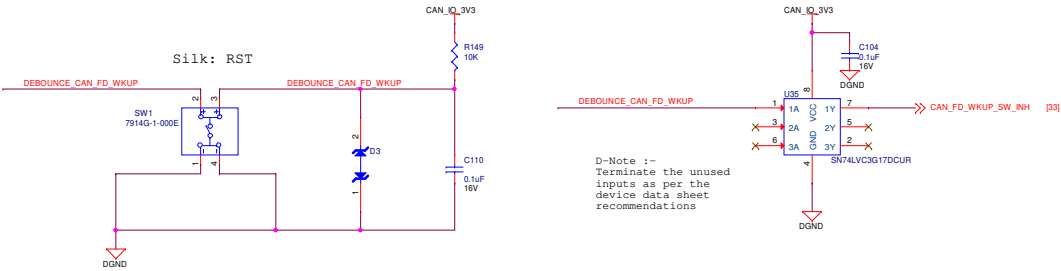
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Title RESET

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CAN-FD FAST WAKE UP SW



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Title CAN FD WKUP SW

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MOUNTING HARDWARE

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

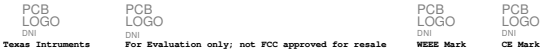
BARE PCB



AM62A SOCKET



LOGOs



JUMPERS



FIDUCIALS



LABELS



SCREW & WASHER FOR PCIe M.2



D-Note :-
Refer STRAP CONFIGURATION OF
ETHERNET PHYS page from
SK-AM64B schematics

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Title HARDWARE SCHEMATICS

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