

AM625 / AM623 Starter Kit SK (EVM) WITH TPS6521904 PMIC

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Revision Number

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REV	B
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D-Note:

SK/EVM is an evaluation board or platform. The SK/EVM is not a reference design. In some cases, the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SoC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata and TRM when designing their custom board. The information found in the datasheet should always take precedence over the SK/EVM implementation.

R-Note:

- * Verify the DNI components configuration with respect to the SK schematics (use PDF) after completion of board design before board assembly.
- * A standard 5% tolerance resistor can be used for most of the series and parallel pull resistors.
- * Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build. (Refer FAQs listed for additional details).



Indicates circuit level change



Indicates that the value of the component has been updated.

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REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	20 Jun 2025	- Drafted from PROC142A1 Schematics - Added optional clock path for EXP_CLKOUT0 signal on the Expansion header to support DANTE	Mistral Design Team	Pandiyarajan	
0.02	26 Jun 2025	Updated TIVA and XDS section as per TI requirement	Mistral Design Team	Pandiyarajan	
0.03	14 July 2025	Implemented the review comments shared by TI	Mistral Design Team	Pandiyarajan	
0.04	21 July 2025	- Replaced U13 with a dual-channel load switch - Changed the implementation of AUDIO_EXT_REFCLK1	Mistral Design Team	Pandiyarajan	
0.05	12 Aug 2025	- Added U113 regulator and corresponding components for VDD_CANUART implementation - Implemented partial IO support for FT4232 UART	Mistral Design Team	Pandiyarajan	
0.06	22 Sept 2025	- TP124 has been added to U12.B7 pin of the SoC - D16 and D17 ESD diodes have been added to J26 and J25 headers respectively - R785, R784 and R786 pulldown resistors have been added to AUDIO_EXT_REFCLK1_R, EXP_CLKOUT0 and AUDIO_EXT_REFCLK1 signals respectively	Mistral Design Team	Pandiyarajan	
0.07	07 Oct 2025	- Changed the supply from VCC3V3_EXP to VCC_3V3_SYS on U111 & R717 - Moved U112 and the corresponding components to the User Expansion Connector section & added the respective D-Notes	Mistral Design Team	Pandiyarajan	
0.08	03 Nov 2025	- R96 has been changed from 10k to 47k - VCCB of U106 has been changed from VCC3V3_TA to VCC_3V3_SYS - Pull-ups R787 & R788 have been added in the FT4232 UART buffers section - Pull-up resistor R789 has been added on TEST_GPIO2_XDS signal	Mistral Design Team	Pandiyarajan	
0.09	04 Nov 2025	- U34 part number has been changed to TPS2051BD and the corresponding circuit has been updated - U114 and the corresponding circuit have been added for ESD protection of USB data lines - Y4 part number has been changed to ABM11W-25.0000MHZ-8-D1X-T3; C303 and C305 have been updated to 13pF	Mistral Design Team	Pandiyarajan	
0.10	11 Nov 2025	Implemented the review comments shared by TI	Mistral Design Team	Pandiyarajan	
0.11	09 Jan 2026	Mounted R6 (The production revision of Wi-Fi+BT module "M.2-CC3351" requires R6 resistor as confirmed by TI)	Mistral Design Team	Pandiyarajan	
0.12	23 March 2026	Below components have been updated based on TI review comments checklist: 1. Value of C232 is changed from 22uF to 4.7uF 2. C491, C534, C535, C536, C537 have been changed from 10pF to 47pF 3. R613, R743, R744, R746, R747 have been changed from 620E to 62E 4. Mounted R363 5. Added D-Notes	Mistral Design Team	Pandiyarajan	
0.13	31 March 2026	- Added D-notes - Added blocks to indicate value/circuit changes form rev A to B	Mistral Design Team	Pandiyarajan	
0.14	14 April 2026	Below components have been updated based on TI review comments checklist: 1. Tolerance of R502, R495, R461, R6, R305, R563, R560, R556, R552, R260, R259, R258, R255, R694, R693 and R400 resistors has been changed from 1% to 5% 2. Value of R304 has been changed from 47K to 10K 3. Value of R330 has been changed from 1.5K to 2.2K 4. Value of R614 & R617 has been changed from 1K to 470E 5. Value of R88 & R188 has been changed from 220E to 470E 6. Added and updated D-Notes	Mistral Design Team	Pandiyarajan	
0.15	23 April 2026	Updated D-Notes	Mistral Design Team	Pandiyarajan	

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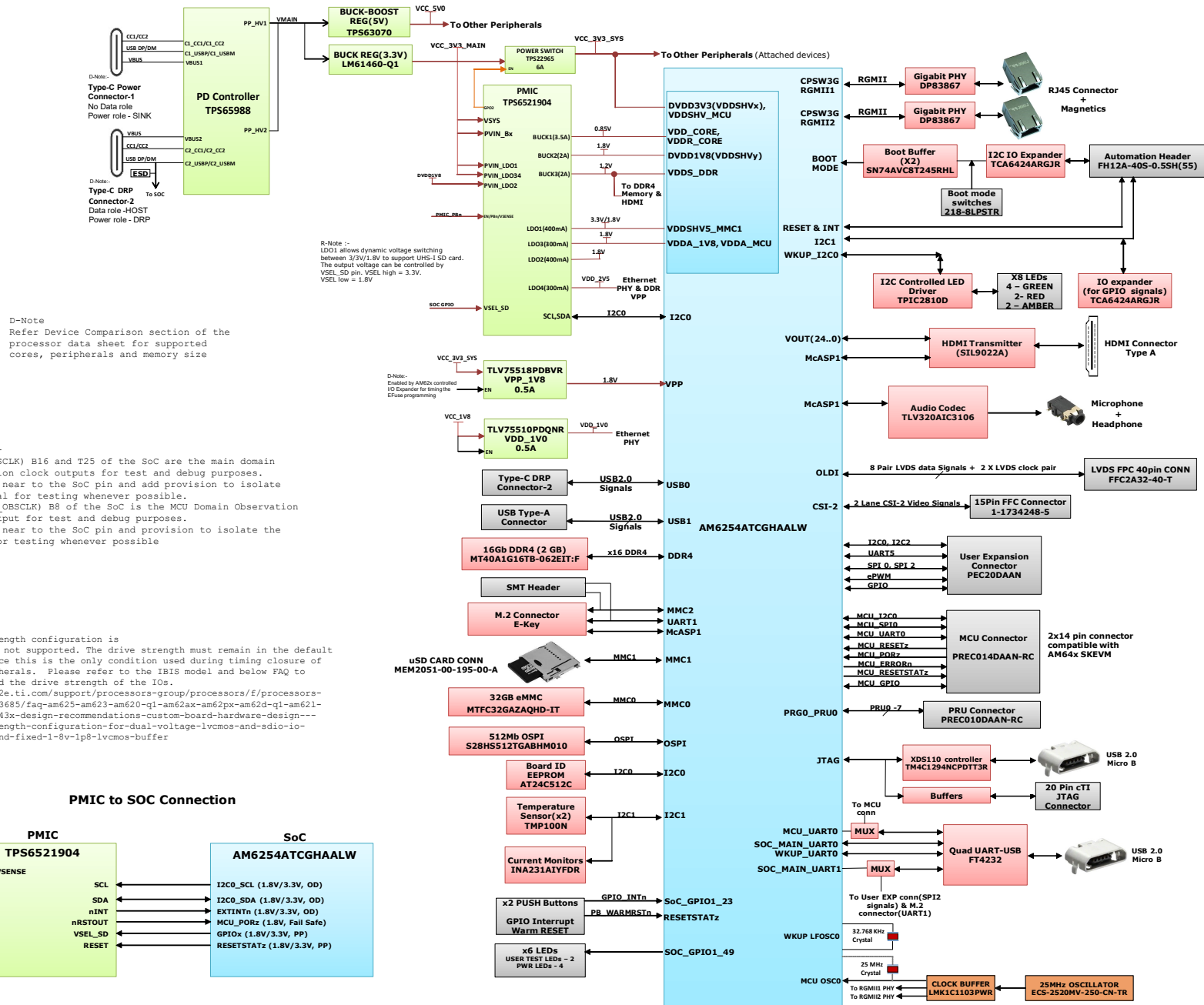
LINKS TO KEY COLLATERALS

Hardware Design Guide: https://www.ti.com/lit/an/sprad05b/sprad05b.pdf
Schematic Design checklist, General guidelines and Review Checklist for AM62x Processor Family: https://www.ti.com/lit/pdf/sprado3
PMIC Power Solutions Application Note: https://www.ti.com/lit/an/slvafd0b/slvafd0b.pdf
DDR Board Design and Layout Guidelines: https://www.ti.com/lit/an/sprad06/sprad06.pdf
SKs (Starter Kits) for Reference: SK-AM62B, SK-AM62B-P1, SK-AM62-LP, SK-AM62-SIP, SK-AM62A-LP, SK-AM62P-LP
Schematic Design guidelines combined for Sitara processor families : https://www.ti.com/lit/pdf/sprad21

LINKS TO KEY FAQs

https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1183910/faq-am625-custom-board-hardware-design-collaterals-to-get-started
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1184006/faq-am623-custom-board-hardware-design-collaterals-to-get-started
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am62x-am62ax-am62px-custom-board-hardware-design-collaterals-for-reference-during-schematic-design-and-schematics-review
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1280721/faq-am625-am623-am625sip-am625-q1-am620-q1-custom-board-hardware-design-faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1332316/faq-am625-am623-custom-board-hardware-design-design-and-review-notes-for-reuse-of-sk-am62b-p1-schematics
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1596731/faq-am625-am623-am620-q1-am625-q1-am625sip-collaterals-for-reference-during-different-phases-of-custom-board-design-self-review-and-bring-up
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1454755/faq-am625-am623-am62aam62p-am62d-q1-am64x-am243x-design-recommendations-custom-board-hardware-design-queries-related-to-soc-data-sheet-pin-attributes
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1457736/faq-am625-am623-am62a-am62p-am62d-q1-am64x-am243x-design-recommendations-custom-board-hardware-design-schematics-review-checklists
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1318441/faq-am625-am623-am62adesign-recommendations-commonly-observed-errors-during-custom-board-hardware-design-sk-schematics-updates-for-design-update-note
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1455706/faq-am625-am623-am620-q1-am625-q1-am625sip-design-recommendations-custom-board-hardware-design-custom-board-schematics-self-review
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1455682/faq-am625-am623-am620-q1-am62l-am62a-am62p-am62d-q1-am64x-am243x-design-recommendations-custom-board-hardware-design-list-of-errors-observed-during-customer-schematics-review

BLOCK DIAGRAM



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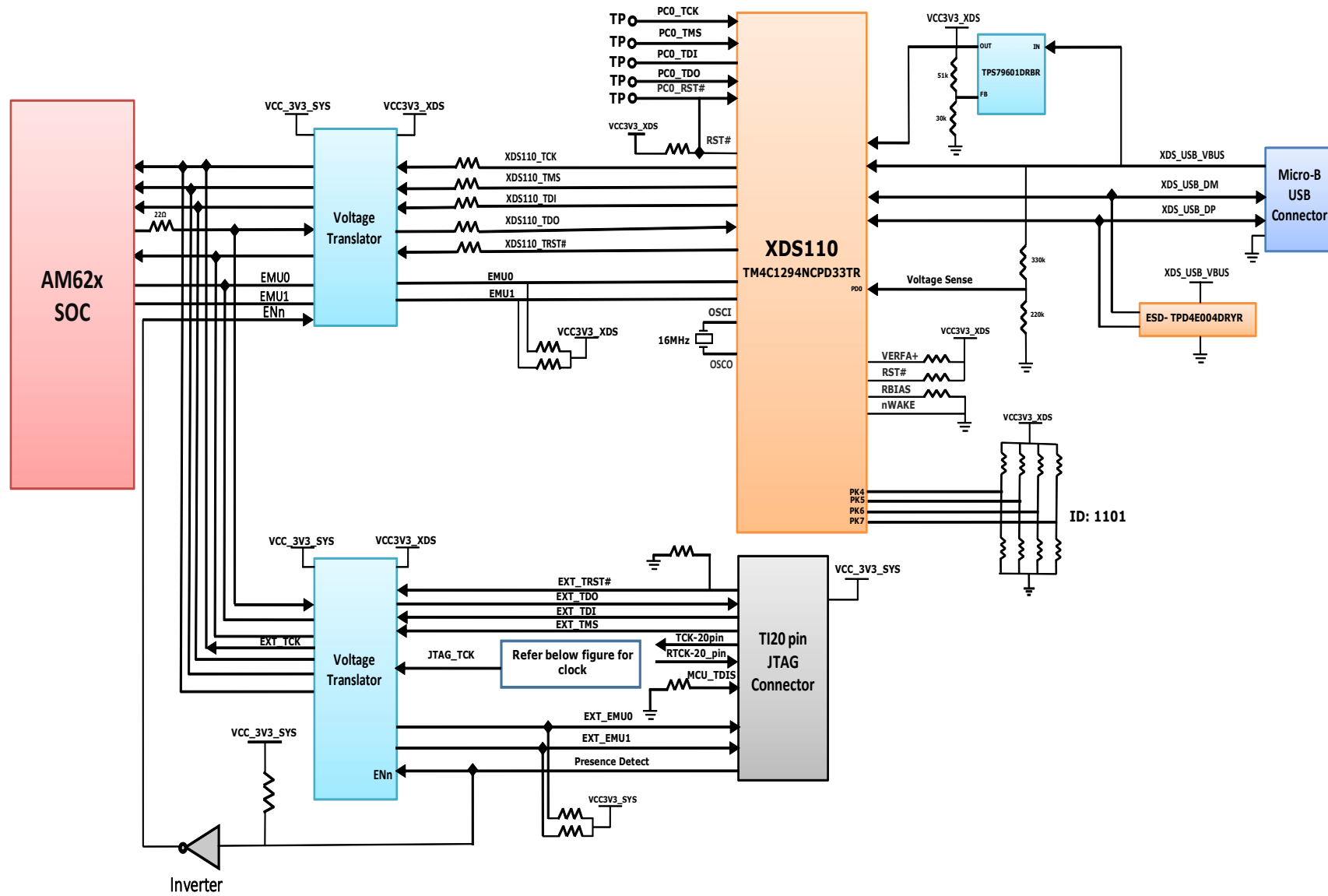
Title	BLOCK DIAGRAM FOR AM625 / AM623 STARTER KIT SK (EVM)
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BLOCK DIAGRAM_XDS110

D-Note:

Please follow SK-AM62P-LP implementations for latest updates on XDS110



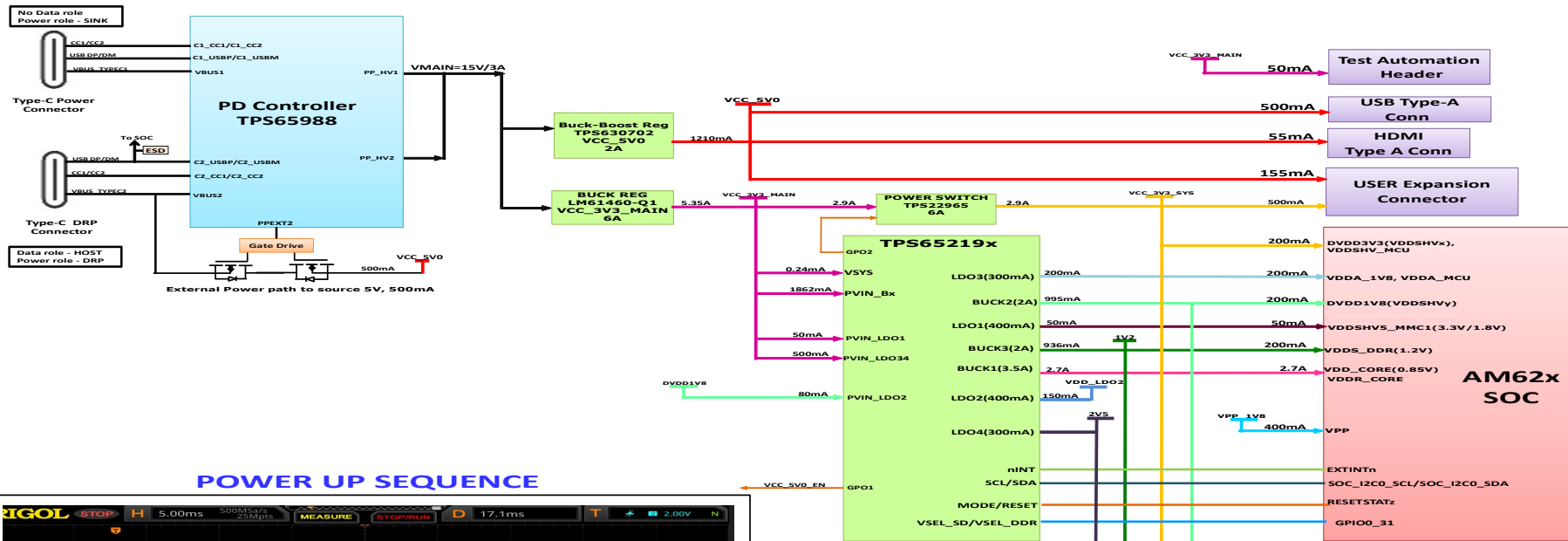
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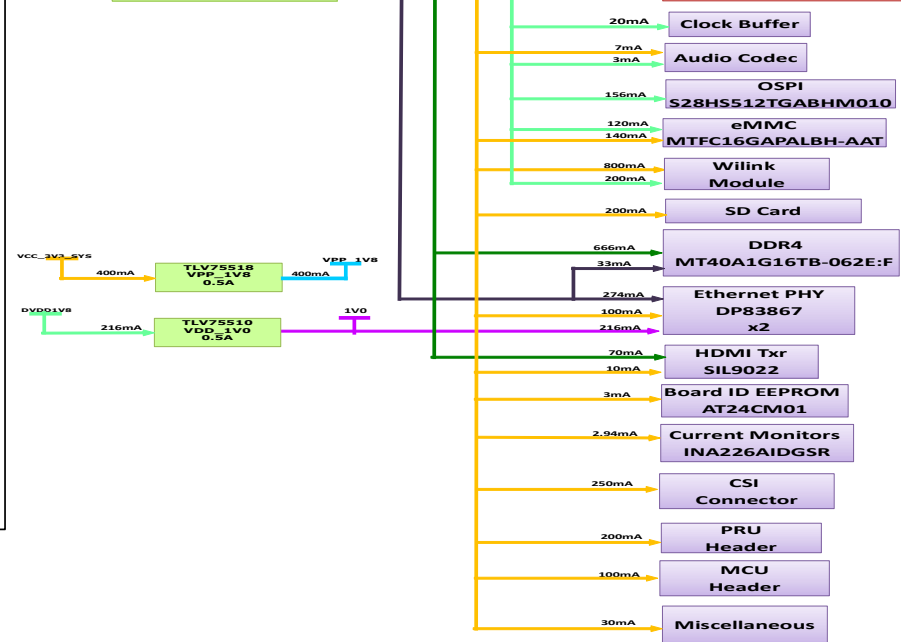
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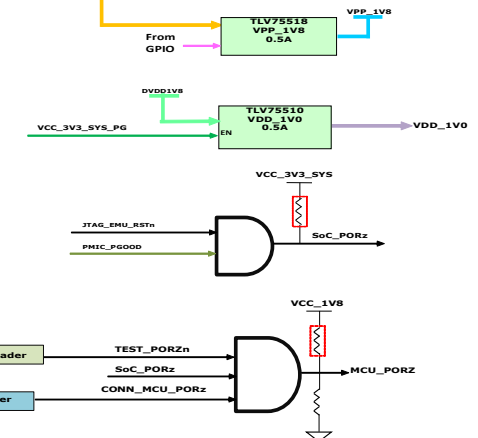
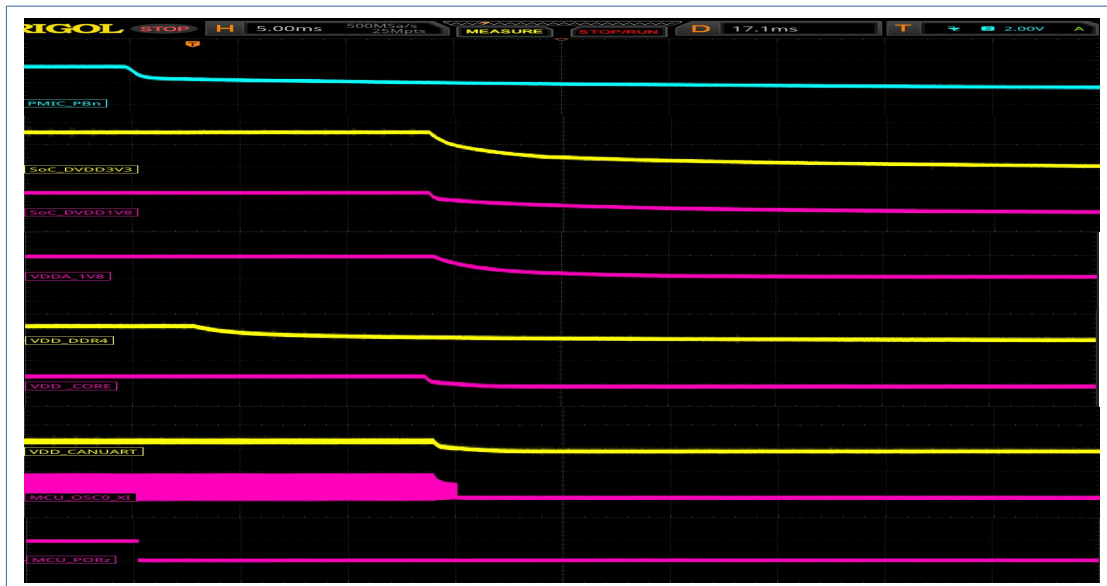
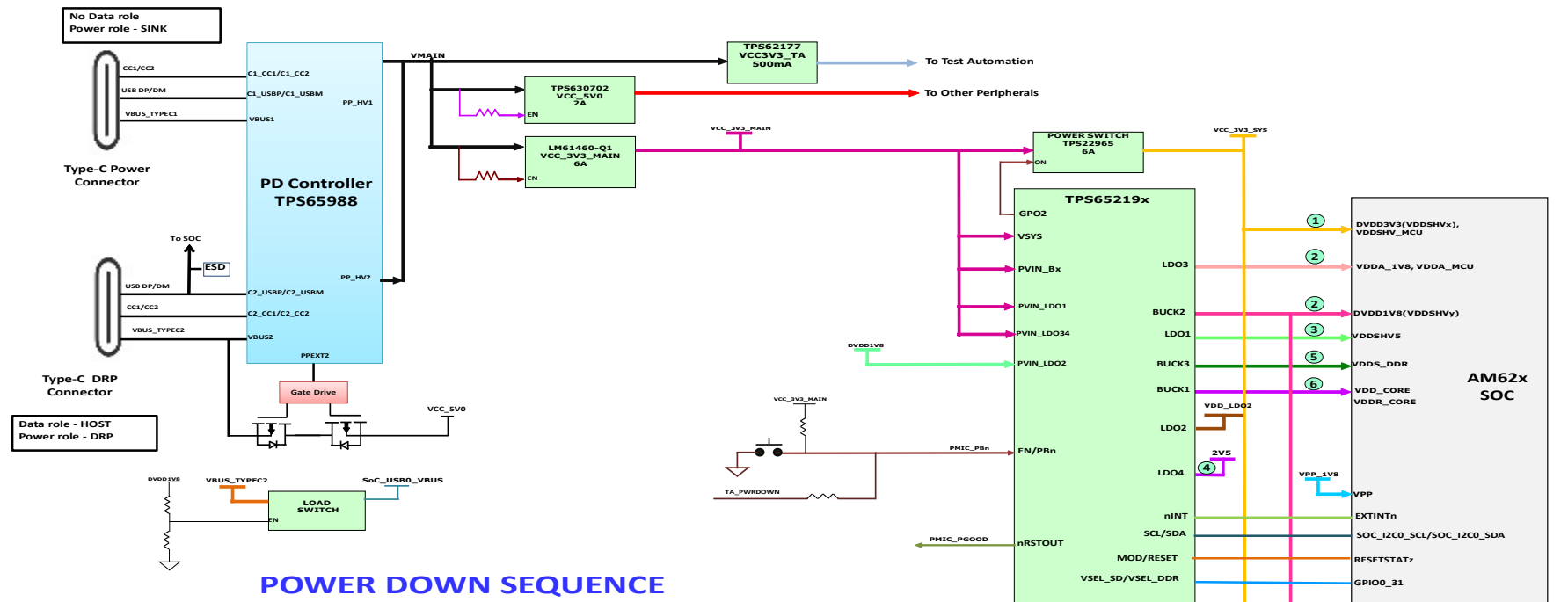
POWER BLOCK DIAGRAM



POWER UP SEQUENCE



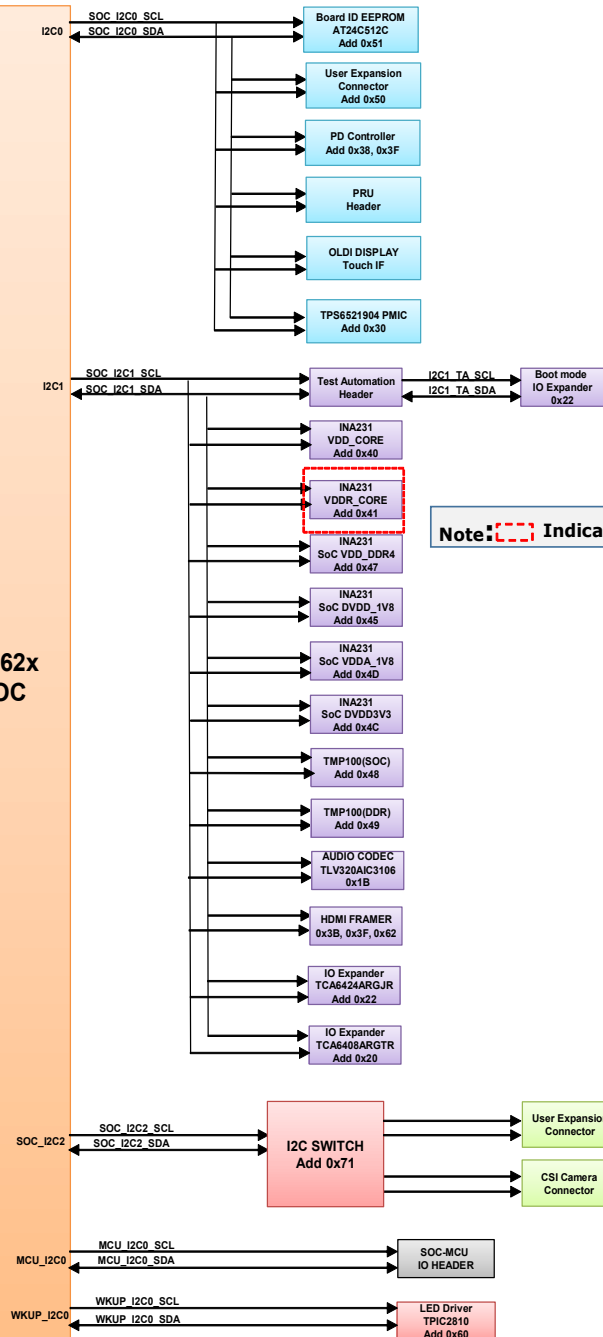
POWER SEQUENCE



I2C TREE

R-Note:
Add -
Indicates
Address

**AM62x
SOC**



Note: [Red dashed box] Indicates DNI

R-Note:

Refer to the following section of the data sheet:
Timing and Switching Characteristics - I2C - Exceptions

R-Note:

For emulated open-drain output type LVCMOS I2C interfaces (I2C0, I2C1, I2C2, I2C3), pull-up resistors are recommended when the IOs are configured for I2C interface. The IOs associated with these I2C interfaces are not compliant to the fall time requirements defined in the I2C specification. A series resistor is used to control the fall time. Location of the pull-up is not critical. The recommendation to connect the pull-ups with the shortest possible stub.

R-Note:

For I2C interfaces with open-drain output type buffer (MCU_I2C0 and WKUP_I2C0), an external pull-up is recommended irrespective of peripheral usage and IO configuration. An RC to limit the slew rate (C placed near to SOC pin) is recommended. Refer to the Pin Connectivity Requirements section of the SoC data sheet.

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GPIO MAPPING TABLE

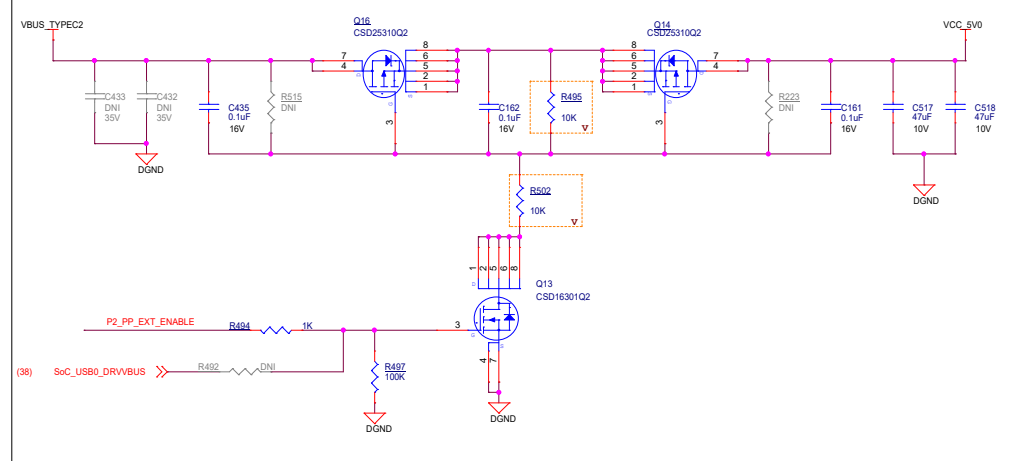
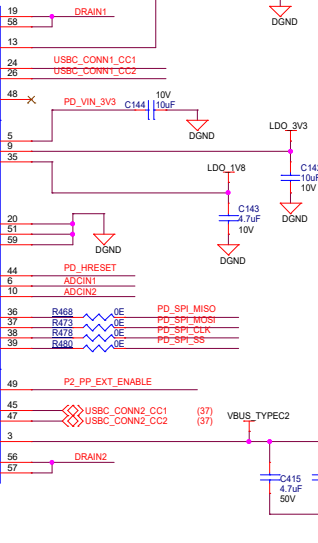
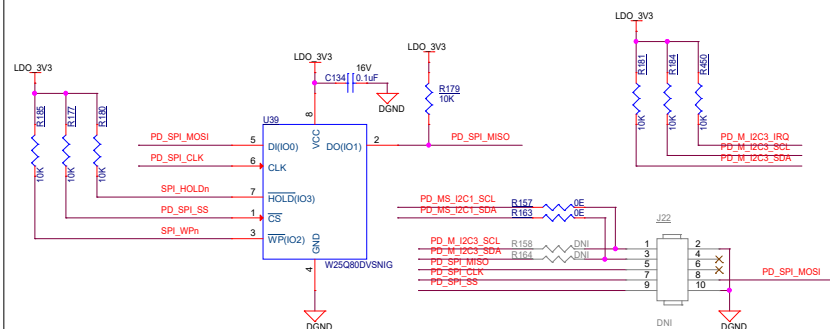
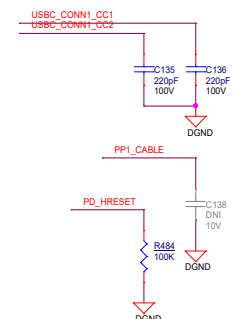
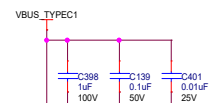
SL NO.	GPIO DESCRIPTION	GPIO NETNAME	Functionality	GPIO USED	SOC MUXED SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE CONNECTED ON SKEVM
1	Enable for WLAN Interface	SoC_WLAN_EN_1V8	ENABLE	GPIO0_71	MMC2_SD CD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	SoC_WLAN_IRQ_1V8	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC_3V3	ENABLE	MCU_GPIO0_1	MCU_SPI0_CS0	OUTPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn/PRU_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
	PRU Connector Interrupt									
	PMIC_INTn									
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	SD Card IO Voltage Select	VSEL_SD	ENABLE	GPIO0_31	GPMC0_CLK	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD3V3
8	IO Expander Interrupt									
9	TEST GPIO1 from Test Automation Connector/ User Interrupt Push Button	MCU_GPIO0_15	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	SoC_DVDD3V3
10	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 01										
1	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER - P02		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER - P03		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER - P04		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER - P05		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER - P06		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
8	EXP CONN HAT Board Detection	RPI_HAT_DETECT	DETECTION	IO EXPANDER - P07		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	M.2 Connector Alert	WLAN_ALERT_3V3	ALERT	IO EXPANDER - P10		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	M.2 Connector WAKEUP	BT_UART_WAKE_SOC_3V3	WAKEUP	IO EXPANDER - P11		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
11	SOC UART1 Mux Select	UART1_MUX_SEL	SELECT	IO EXPANDER - P12		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
12	Enable for Wilink Level Translators	WL_LT_EN	ENABLE	IO EXPANDER - P13		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER - P14		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	Raspberry PI Camera CSI0 GPIO1	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER - P15		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	Raspberry PI Camera CSI0 GPIO2	CSI_GPIO2	INPUT/OUTPUT	IO EXPANDER - P16		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER - P17		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER - P20		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO for communications with AM62x	IO EXPANDER - P21		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
19	MCASP2 Enable and Direction Control	AUD_BUF_EN	ENABLE	IO EXPANDER - P22		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
20		WL_BUF_EN	ENABLE	IO EXPANDER - P23		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
21		AUD_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P24		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
22		WL_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P25		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
23	OLDI Display Touch Interrupt	TS_INT#	INTERRUPT	IO EXPANDER - P26		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER - P27		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 02										
1	M.2 Connector SDIO Reset Control GPIO	WLAN_SDIO_RST_3V3	RESET	IO EXPANDER - P0		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	OLDI Display Reset control	GPIO_TS_RSTn	RESET	IO EXPANDER - P1		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	DETECTION	IO EXPANDER - P2		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	eMMC Reset control GPIO	GPIO_eMMC_RSTn	RESET	IO EXPANDER - P3		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3

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Title GPIO MAPPING TABLE

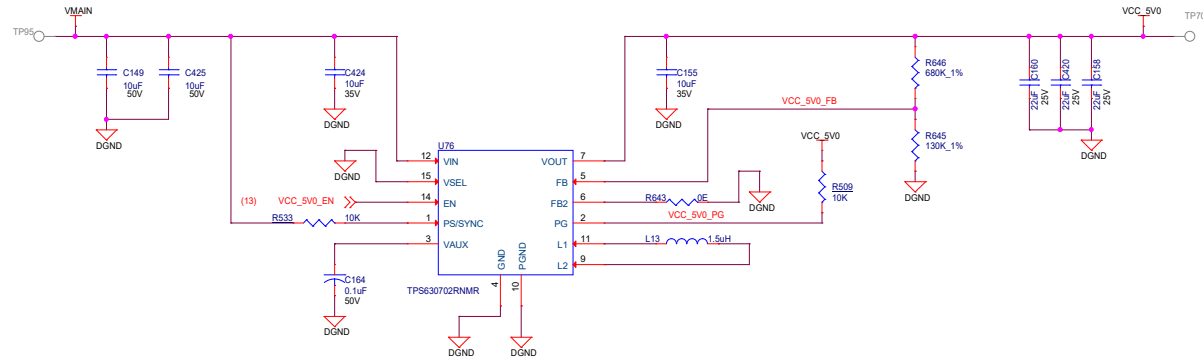
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PERIPHERAL POWER SUPPLIES - 1



D-Note:
Add a jumper or OR for isolation or current measurement
Provision can be provided for pre-production board and can be deleted for production boards as required

GROUND TEST POINTS



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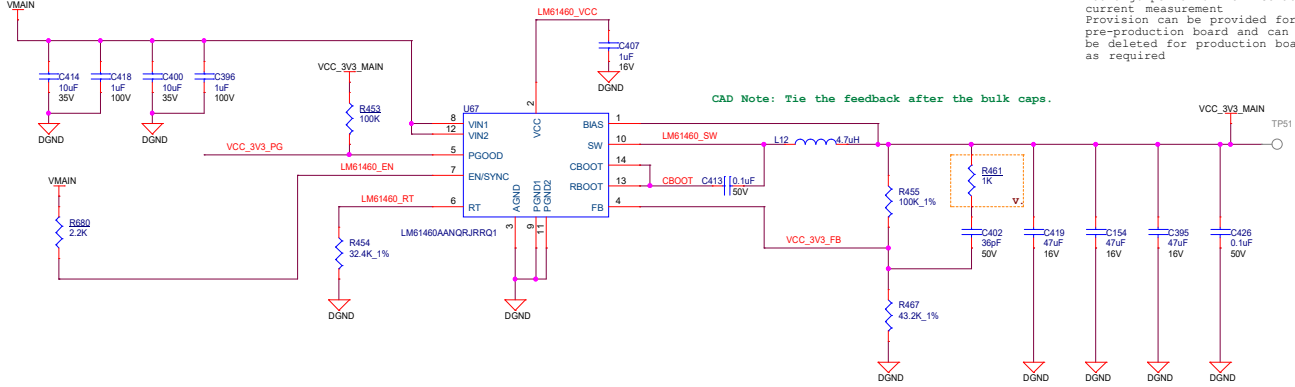
Title PERIPHERAL POWER SUPPLIES-1

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PERIPHERAL POWER SUPPLIES - 2

VinMin = 4.5V
VinMax = 24V
Vout = 3.3V @ 6A

3.3V, 6.0 AMPS SUPPLY

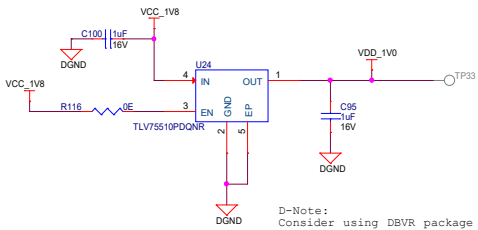


D-Note:
Add a jumper or 0R for isolation or current measurement
Provision can be provided for pre-production board and can be deleted for production boards as required

CAD Note: Tie the feedback after the bulk caps.

PERIPHERAL SUPPLY - ETHERNET PHY

1.0V, 0.5 AMPS

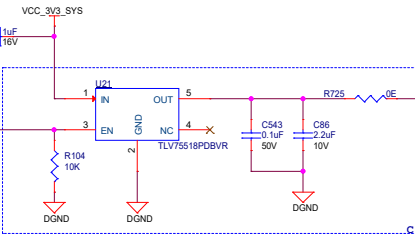


D-Note:
Consider using DBVR package (similar to VPP_1V8 LDO)
LDO package change is due to the manufacturing challenges with QFN package

1.8V VPP, 0.5 AMPS SUPPLY

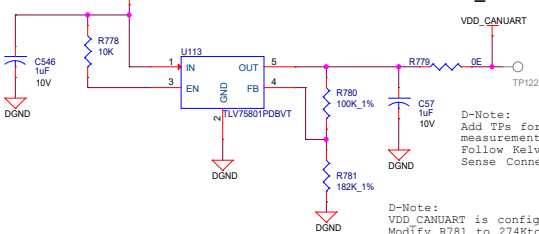
D-Note:
It is important to select an LDO with a fast transient response and connect the LDO output to the VPP pin with a low loop inductance path to ensure that the LDO is able to source the high transient load current, where the VPP pin never drops below the minimum operating voltage.

D-Note:
Alternate part suggestion:
TPS7A21-Q1, Automotive, 500mA, low-noise ultra-low-IQ high-PSRR low-dropout (LDO) voltage regulator



D-Note:
An alternate approach to source the VPP supply is to use an external supply. The required caps and discharge resistor is recommended to be placed near to the SoC VPP pin. The recommendation is to use SoC GPIO to control and time the external power supply output.

CORE SUPPLY FOR CANUART VDD_CANUART



D-Note:
Add TPs for current measurement
Follow Kelvin Current Sense Connection

D-Note:
VDD_CANUART is configured for 0.85V
Modify R781 to 274K to configure VDD_CANUART to 0.75V
Example part number: ERAJ-28RF2743X

D-Note:
Given the transient current requirement during eFuse programming, using a load switch or a FET based switch may not be a recommended approach. It is recommended to use an LDO. A load switch or FET switch is likely to have too much voltage drop that can't be compensated like when using an LDO.

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Title PERIPHERAL POWER SUPPLIES-2

Size	PROC142B(002)	Rev
C		B
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SOC POWER ARCHITECTURE - PMIC

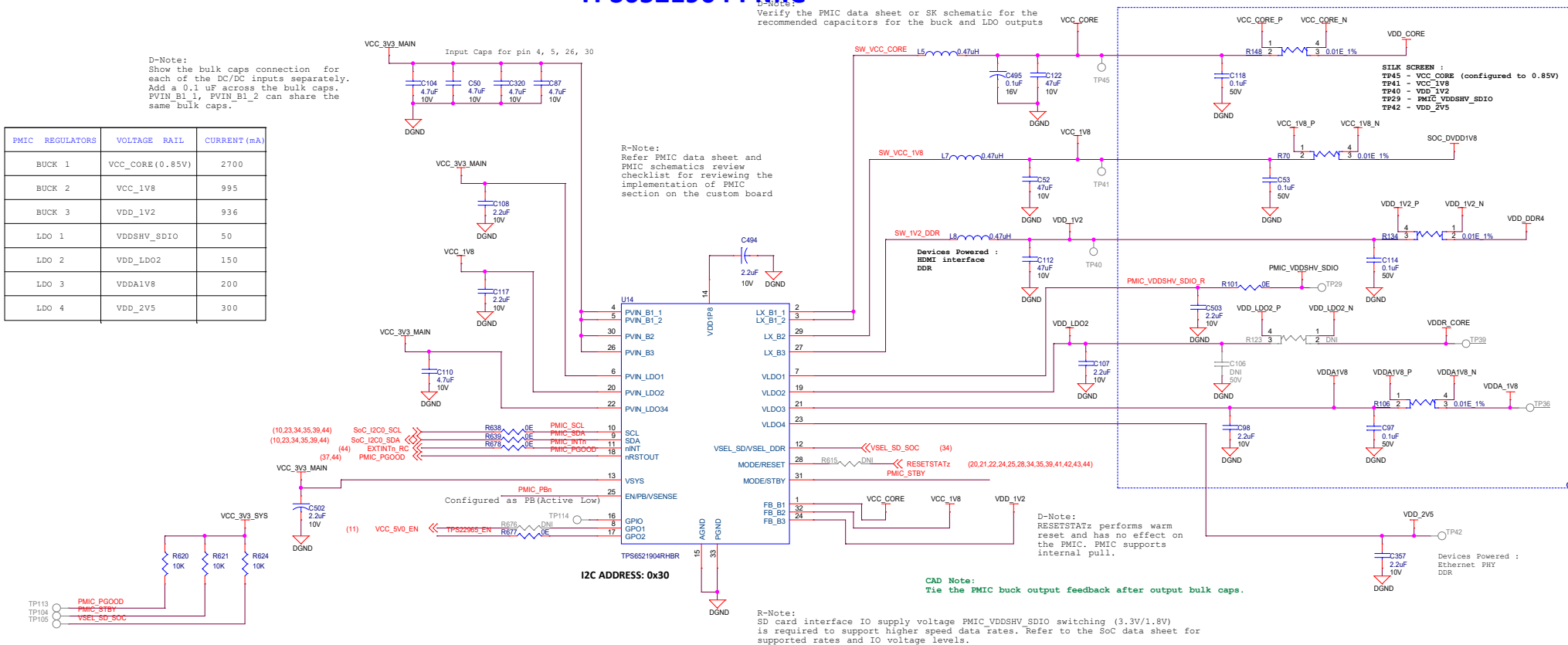
TPS6521904 PMIC

D-Note:
OR resistor or jumper is added at the
PMIC buck output for isolation or testing.

D-Note:
Show the bulk caps connection for
each of the DC/DC inputs separately.
Add a 0.1 uF across the bulk caps.
PVIN_B1_1, PVIN_B1_2 can share the
same bulk caps.

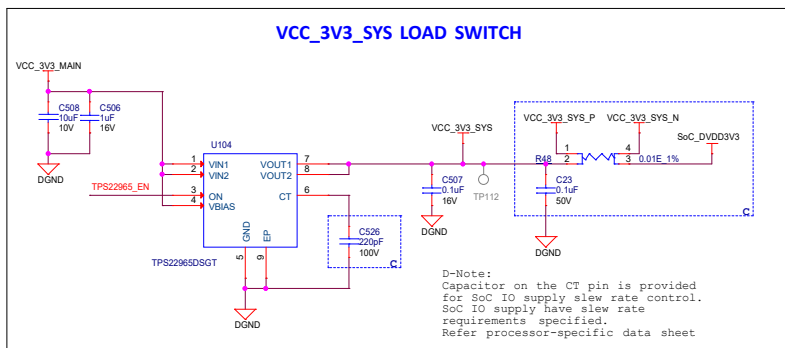
PMIC REGULATORS	VOLTAGE RAIL	CURRENT (mA)
BUCK 1	VCC_CORE(0.85V)	2700
BUCK 2	VCC_1V8	995
BUCK 3	VDD_1V2	936
LDO 1	VDDSHV_SDIO	50
LDO 2	VDD_LDO2	150
LDO 3	VDDA1V8	200
LDO 4	VDD_2V5	300

R-Note:
Refer PMIC data sheet and
PMIC schematics review
checklist for reviewing the
implementation of PMIC
section on the custom board

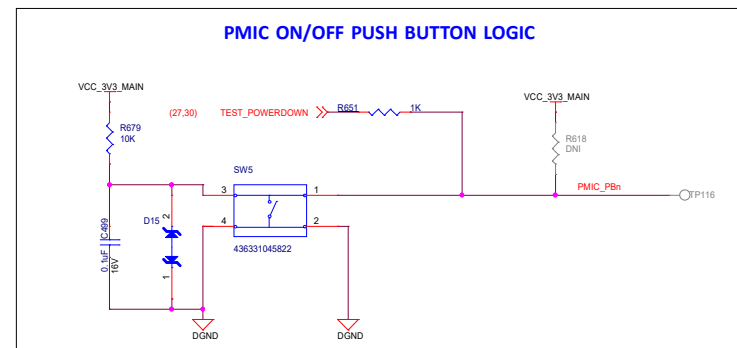


SOC 3.3V IO SUPPLY

VCC_3V3_SYS LOAD SWITCH



PMIC ON/OFF PUSH BUTTON LOGIC



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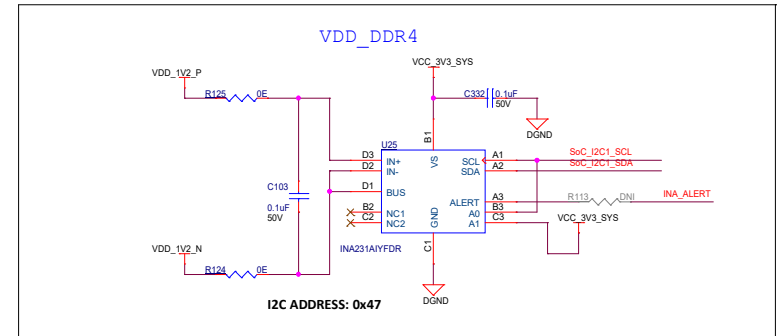
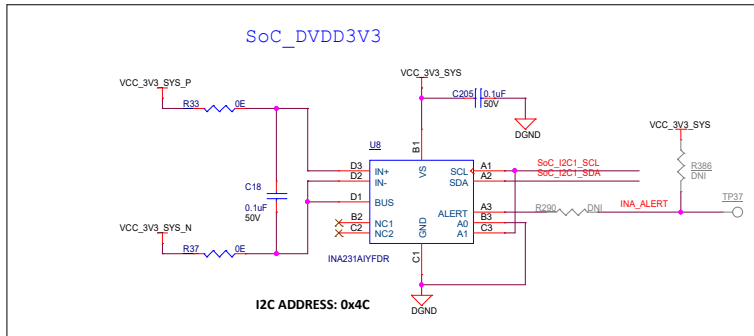
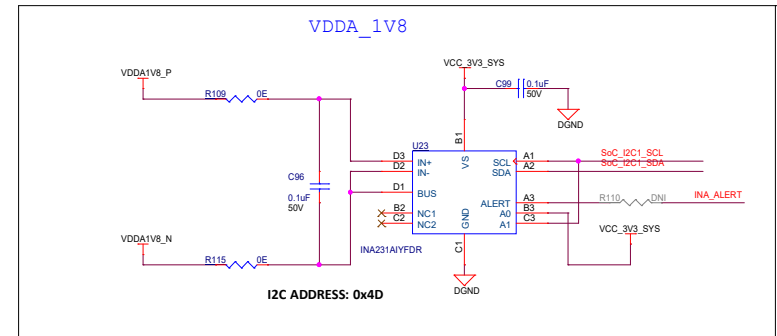
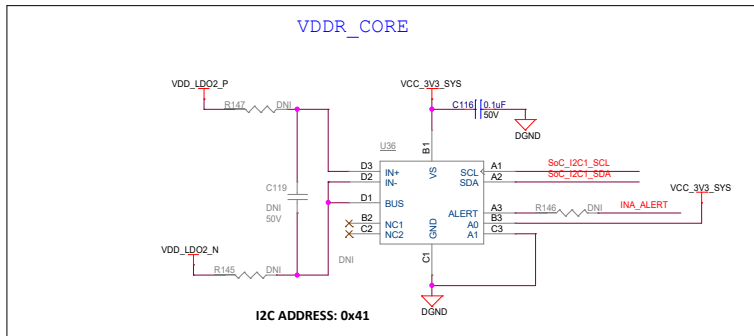
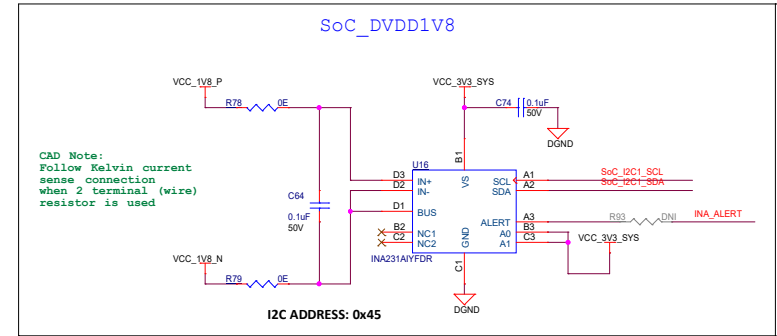
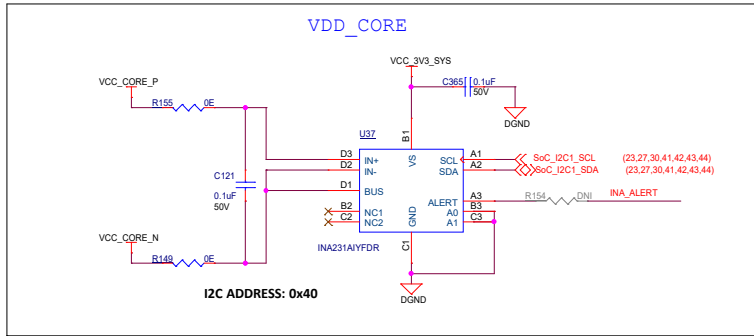
Title
SOC POWER SUPPLIES-PMIC BASED WITH SOC CURRENT MEASUREMENT SHUNTS

Size	PROC142B(002)	Rev	
C		B	
Date:	Friday, May 08, 2026	Sheet	13 of 46

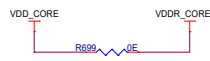
CURRENT MEASUREMENT DEVICES

D-Note: Note the supply rail name change across the shunt when optimizing the design (Deleting the current sense resistor).

D-Note: Provision for 4-wire resistor and current measurement devices have been provided for testing on the EVM board. Implementing current measurement circuit on the custom board is use case and board requirements dependent.



D-Note: OR resistor option to connect VDDR CORE to VDD CORE supply rail. The recommendation is to connect VDD_CORE and VDDR_CORE to the same supply source when VDD_CORE is configured for 0.85V.



CORE_SUPPLY	ARRAY_CORE_SUPPLY	Assembly
0.75 VDD_CORE	0.85 VDDR_CORE	DNI R699 and Mount R123
0.85 VDD_CORE	0.85 VDDR_CORE	DNI R123 and Mount R699

INA I2C SLAVE ADDRESS		
POWER_SOURCE	SUPPLY_NET	SLAVE_ADDRESS (IN_HEX)
VCC_CORE	VDD_CORE	40
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V2_DDR	VDD_DDR4	47

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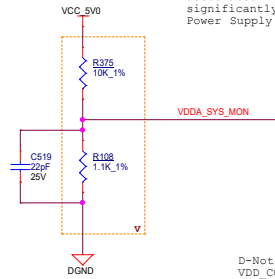


Title SOC SUPPLY RAILS CURRENT MEASUREMENT DEVICES

Size	Rev
C	B
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SOC POWER SUPPLIES AND SUPPLY RAILS

D-Note:
Recommend implementing the voltage monitoring functionality using VMON_VSYS for early detection of supply failure. It is meant to be a power-fail indicator for the main input voltage rail that enters the custom board. For example, a 12, or 24 volts, the error associated with this monitor would require you to set the threshold of the monitored voltage significantly lower than the nominal voltage (ROC) to avoid a false trigger. Refer to System Power Supply Monitor Design Guidelines section of the data sheet.



D-Note:
Changing the core voltage (Dynamically) is not allowed after the SOC has been released from reset. In case the core supply is turned off, the recommendation is to turn off all power rails and ramp them down as per the power-down sequence and wait until all supply rails decay below 300mV before turning on power again.

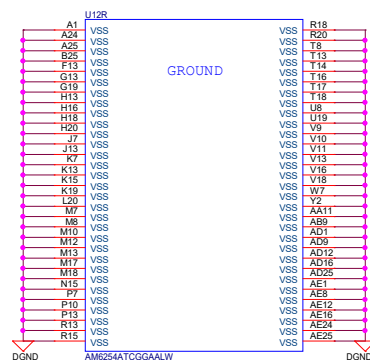
D-Note:
VDD_CORE and VDDR_CORE are recommended to be connected to the same supply source, so they ramp together when VDD_CORE is operating at 0.85 V.

R-Note:
Connecting a 1.8V supply source directly
to VPP pin continuously is not
recommended or allowed.

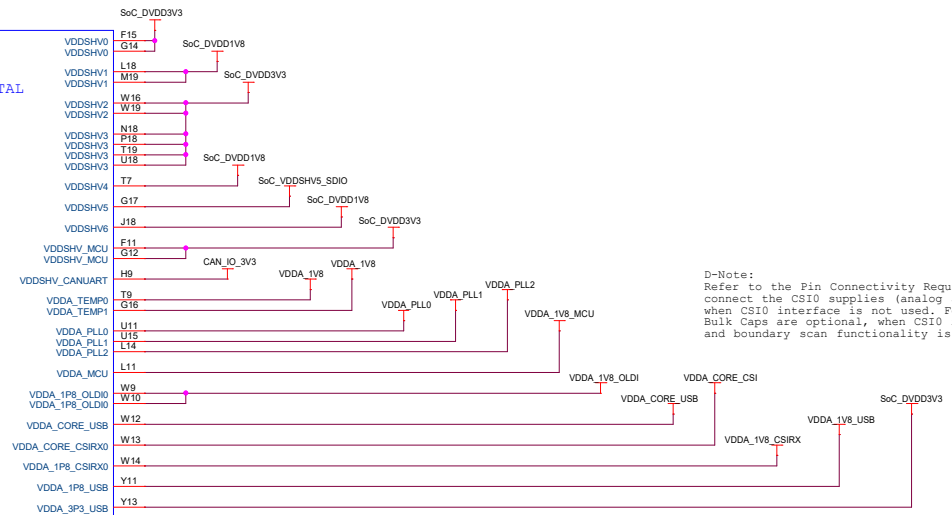
D-Note:
RESERVED PINS
Leave them unconnected

D-Note:
Refer to the pin connectivity requirements section of the SoC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is allowed to have the supplies connected and all the USB pins left unconnected, provided the USB driver is not initialized at any time and the USB allocation procedure does not happen. The recommendation is to connect (Grounding) the USB supplies to the pin connectivity requirements when not used, to optimize power when low power is a critical requirement.

SOC VSS

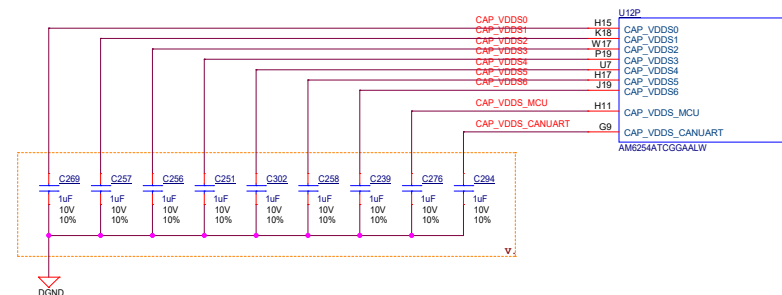


ANALOG AND DIGITAL



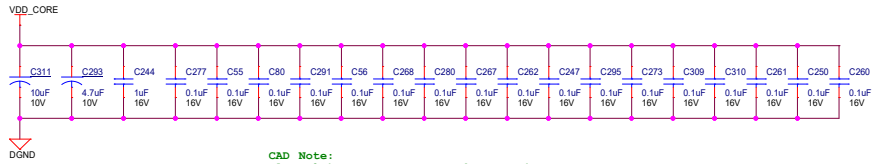
D-Note:
Refer to the Pin Connectivity Requirements to connect the CS10 supplies (analog and core), when CS10 interface is not used. Ferrite and Bulk Caps are optional, when CS10 is not used and boundary scan functionality is required.

D-Note:
A trace connected to SoC is effectively an antenna that will pick up noise. A potential will be generated on the signal when noise couples into the antenna. This potential will be largest on the highest impedance end of the signal. By placing a pull-up (pullup) or pull-down (pulldown) near the SoC pin, we force the highest potential to the open-circuit end of the signal rather than the SoC end of the signal.

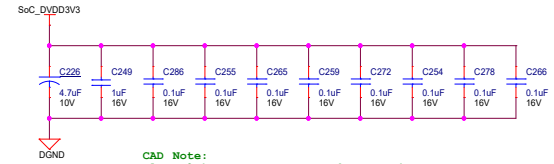


D-Note:
Select capacitors with ESR < 1 ohm. Ensure the PCB loop inductance is < 2.5 nH. Select 0201 package or the smallest possible package.

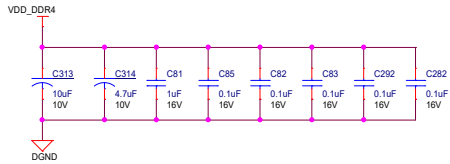
SOC POWER SUPPLIES - DECAPS 1



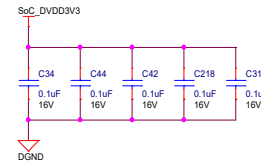
CAD Note:
Place 0.1 uF caps near to the SoC pins.



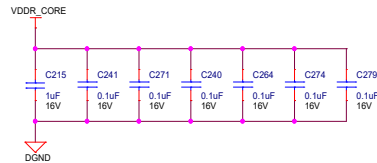
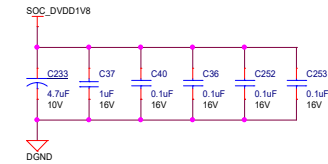
CAD Note:
Place 0.1 uF caps near to the SoC pins.



CAD Note:
Place 0.1 uF caps near to the SoC pins.



CAD Note:
Place 0.1 uF caps near to the SoC pins.



CAD Note:
Place 0.1 uF caps near to the SoC pins.



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Title SOC POWER SUPPLIES - DECAPS 1

Size
C Variant Name = PROC142B(002)

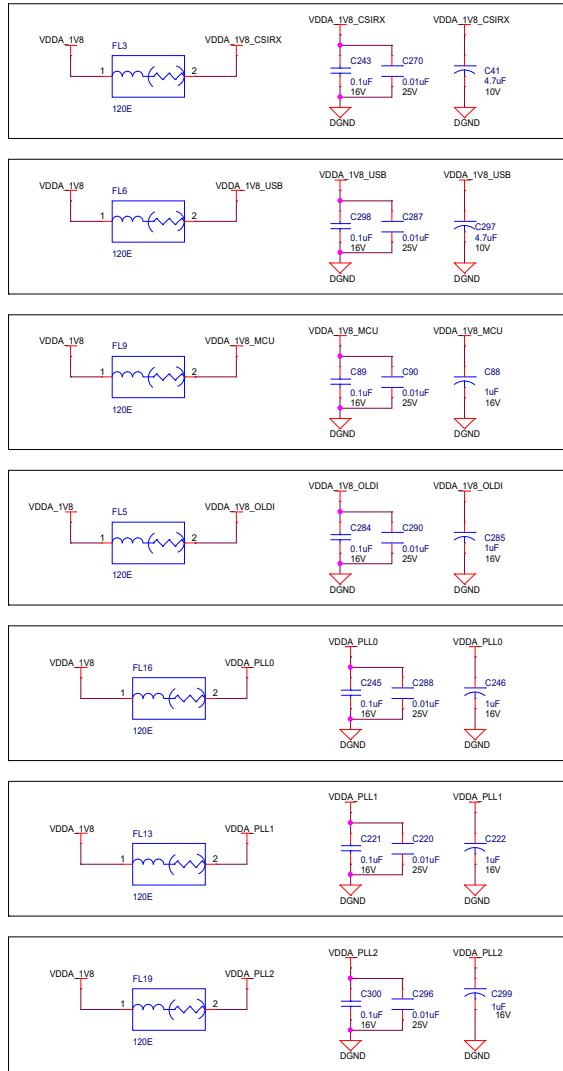
Date: Friday, May 08, 2026

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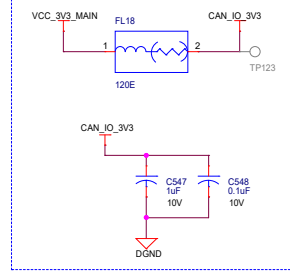
Rev

SOC POWER SUPPLIES - DECAPS 2

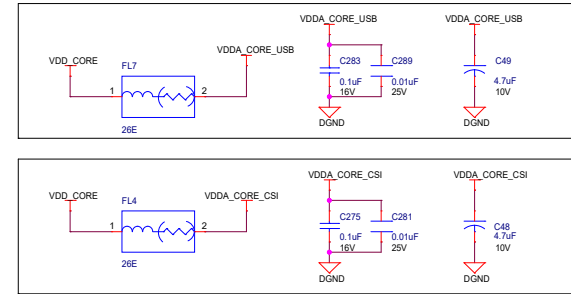
PERIPHERALS - 1.8V ANALOG SUPPLIES



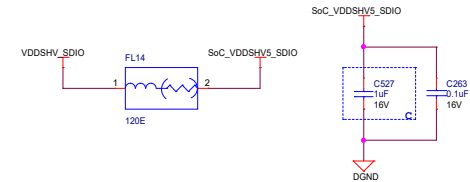
CAN_IO_3V3



PERIPHERALS - CORE SUPPLIES



3.3V/1.8V MMC1 SUPPLY



D-Note:
Common SoC LVCMOS IO Interface Guidelines:
1. Most of the SoC IOs are not fail-safe. No input should be applied before processor supply ramps.
2. SoC LVCMOS inputs have minimum slew rate requirements specified.
3. SoC IO buffers are off during Reset. A pull pull is required near to the attached device input being driven by the SoC IOs (input does not float).
4. Any SoC IO that has a trace connected and not being actively driven needs a parallel pull. When adding a pull is not feasible, ensure the trace is routed away from noisy signals.
5. When the IOs are unused, leave the IOs unconnected and the PADCONFIG setting in the default state.

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Title SOC POWER SUPPLIES - DECAPS 2

Size Variant Name = PROC142B(002)

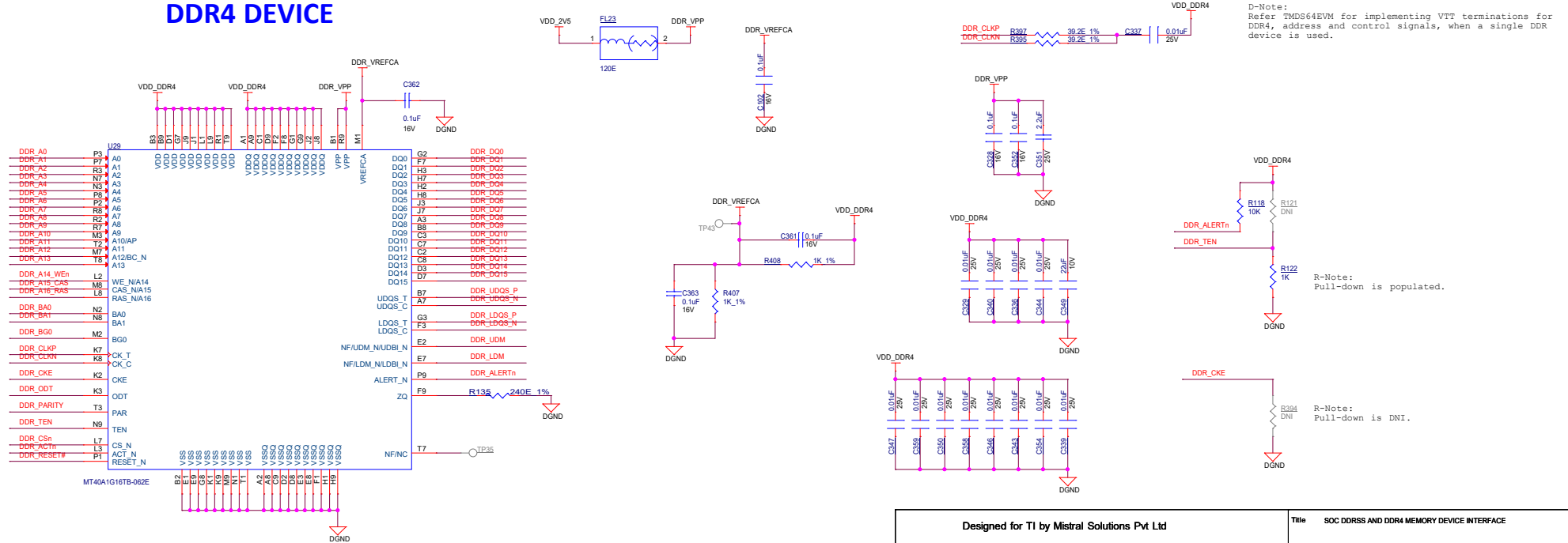
Date: Friday, May 08, 2026

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SOC DDR4 INTERFACE



DDR4 DEVICE



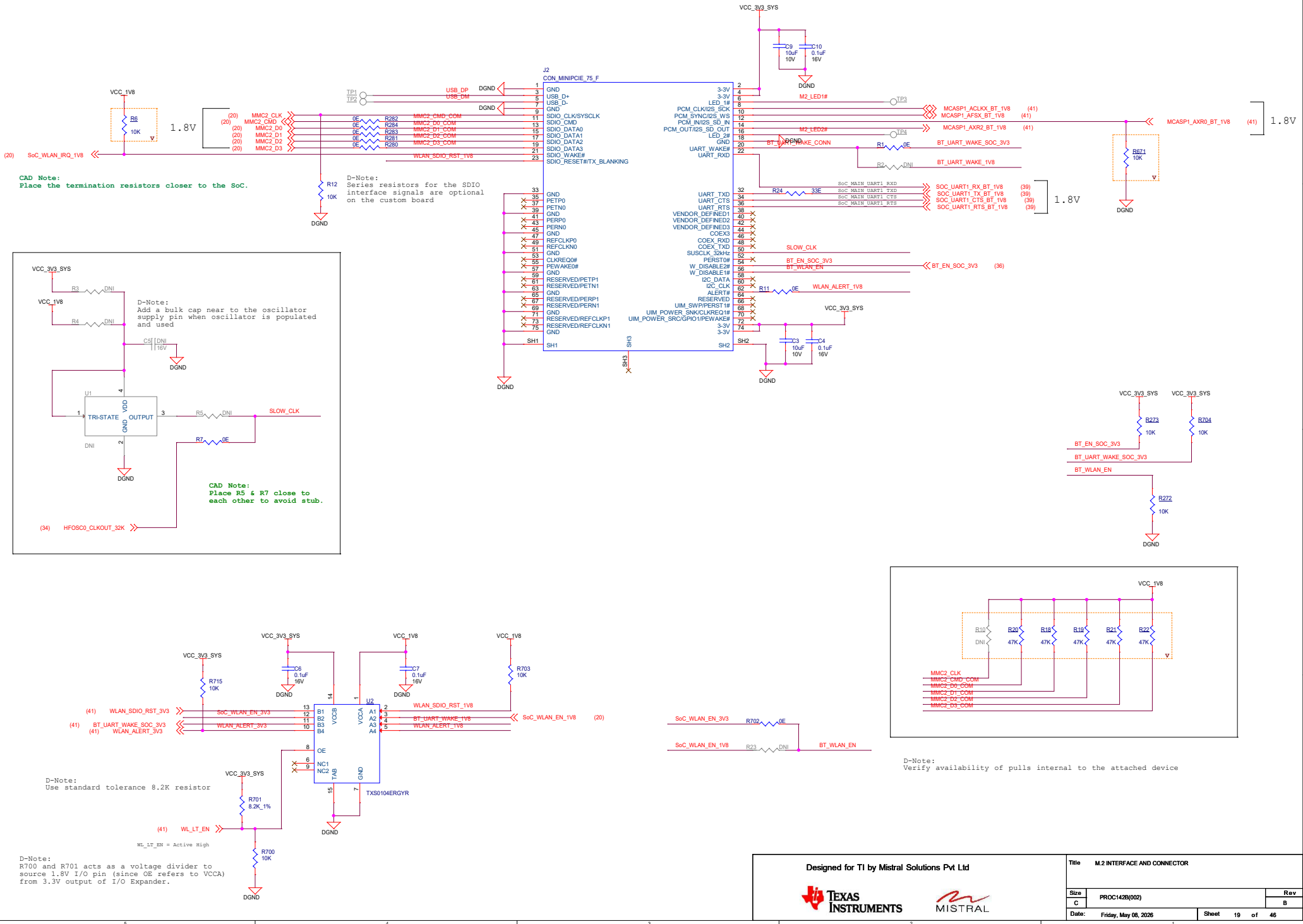
Designed for TI by Mistral Solutions Pvt Ltd



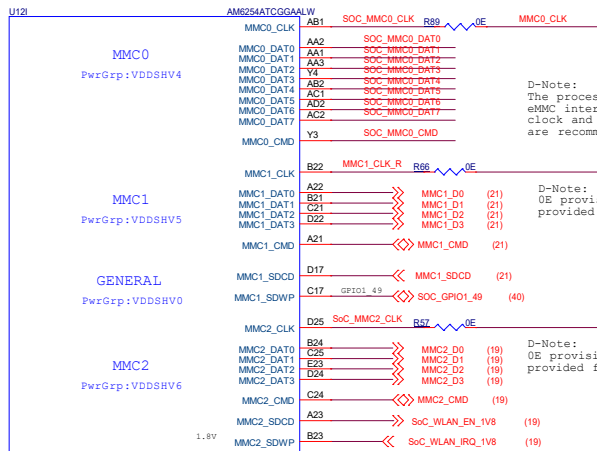
Title	SOC DDRSS AND DDR4 MEMORY DEVICE INTERFACE
-------	--------------------------------------------

Size	Variant Name = PROC142B(002)	Rev
C		B
Date:	Friday, May 08, 2026	Sheet 18 of 46

M.2 INTERFACE



SOC - MMC Interface



D-Note:
OE provision on MMC0_CLK has been provided for control of possible signal reflections

D-Note:
MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51).

D-Note:
The processor family implements a soft PHY for eMMC interface. The pulls required for D0, clock and other eMMC interface control signals are recommended to be implemented externally.

D-Note:
OE provision on MMC1_CLK has been provided for control of possible signal reflections

D-Note:
As a good design practice, a 47K pull-up is recommended to ensure the pull-up value is within the JEDEC specification, when internal pulls are enabled unexpectedly. This way the resulting pull resistance will still be within the specified limits.

D-Note:
OE provision on MMC2_CLK has been provided for control of possible signal reflections

R-Note:
What is the reason pulldown is used for eMMC, SD card or other peripherals clock input? Because, there are cases where the clock is stopped or paused in a LOW logic state, and the pull-down option is consistent with this logic state.

eMMC FLASH RESET

D-Note:
The GPIO reset option makes it possible for the software to reset the attached device (eMMC or OSPI or SD card or OLDI or EPHY) without resetting the entire processor, if there is a case where the peripheral becomes unresponsive.

D-Note:
You could eliminate the GPIO option and only use the reset output (warm or cold), where the software forces a warm reset, if the peripheral becomes unresponsive. However, this will reset the entire device, rather than trying to recover the specific peripheral without resetting the entire device.

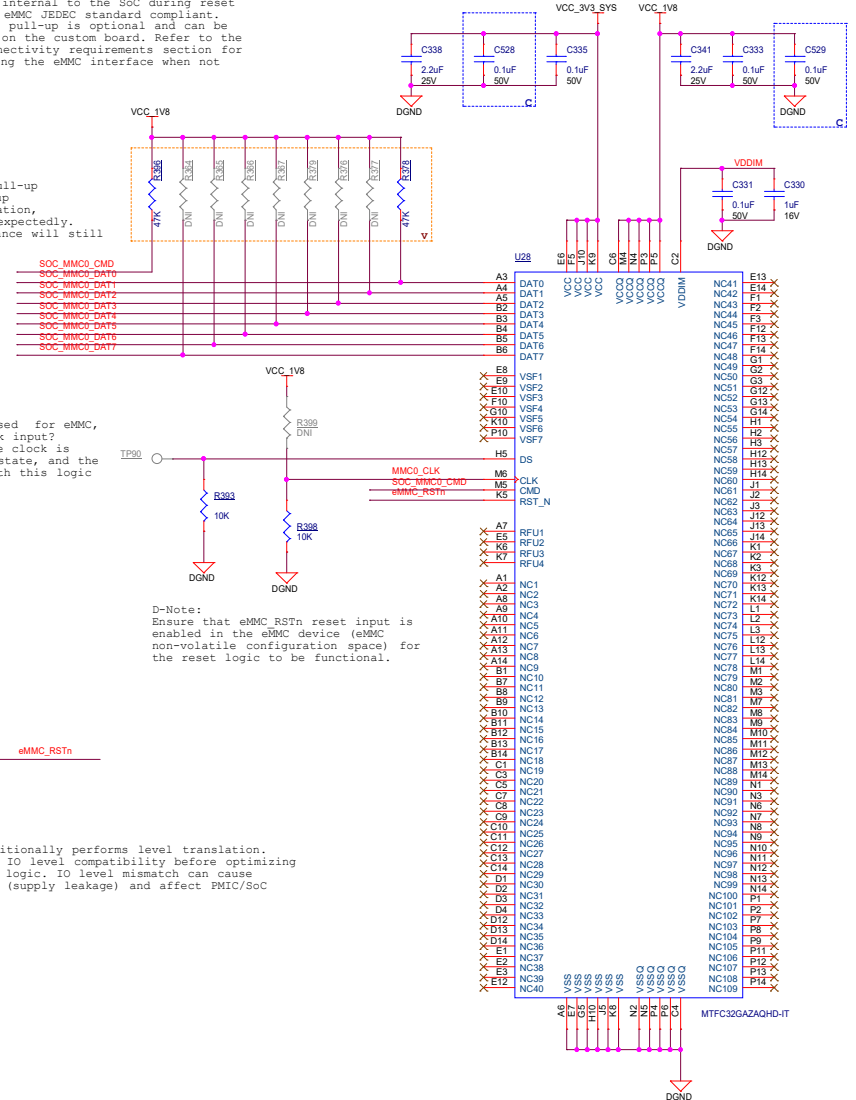
D-Note:
In case ANDING logic is not used and the processor Main domain warm reset status output (RESETSTAT2) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTAT2 IO voltage level. A level translator is recommended to match the IO voltage level. In case the value is too high, the rise/fall time of the eMMC reset input can be slow and introduce too much delay. In case the value is too low, it will cause the AM62x to source too much steady-state current during normal operation.

D-Note:
ANDING logic additionally performs level translation. Verify the reset IO level compatibility before optimizing the reset ANDING logic. IO level mismatch can cause residual voltage (supply leakage) and affect PMIC/SoC operation.

D-Note:
Refer Custom Board Design and Simulation Guidelines for Processor High Speed Parallel Interfaces
<https://www.ti.com/lit/pdf/sdaa087>

D-Note:
The pull-up required for D7-D0, clock and other eMMC interface control signals are enabled internal to the SoC during reset and are eMMC JEDEC standard compliant. External pull-up is optional and can be deleted on the custom board. Refer to the pin connectivity requirements section for connecting the eMMC interface when not used.

eMMC FLASH



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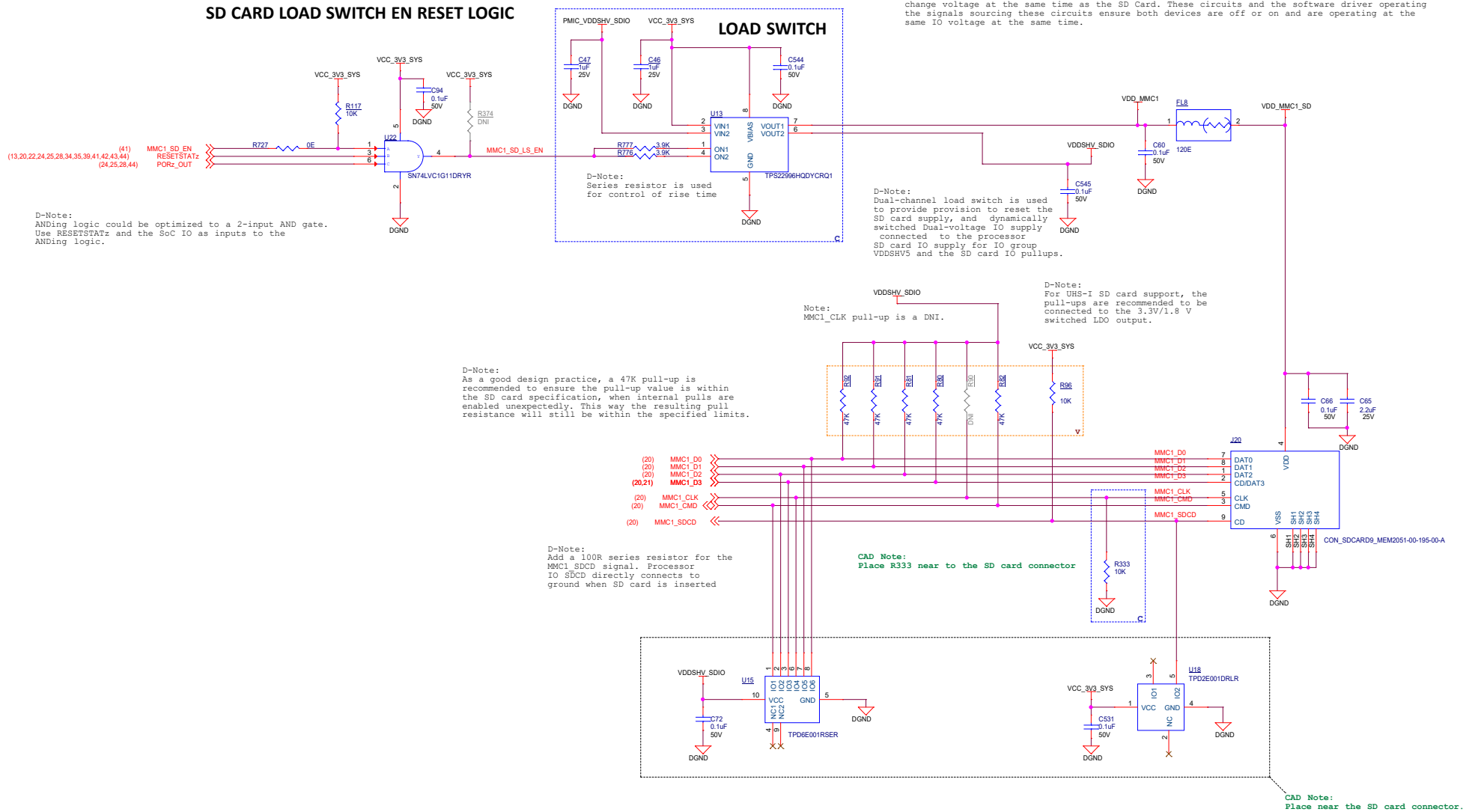
Title SOC MMC0.2 INTERFACE AND eMMC FLASH + RESET

Size	PROC142B(002)	Rev
C		B
Date:	Friday, May 08, 2026	Sheet 20 of 46

SD CARD INTERFACE

D-Note:
Refer Custom Board Design and Simulation Guidelines for
Processor High Speed Parallel Interfaces
<https://www.ti.com/lit/pdf/sdcaa087>

SD CARD LOAD SWITCH EN RESET LOGIC



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Title	SD CARD-LOAD SWITCH, LOAD SWITCH RESET LOGIC AND DATA INTERFACE
-------	-----------------------------------------------------------------

Size	PROC142B(002)	Rev
C		B

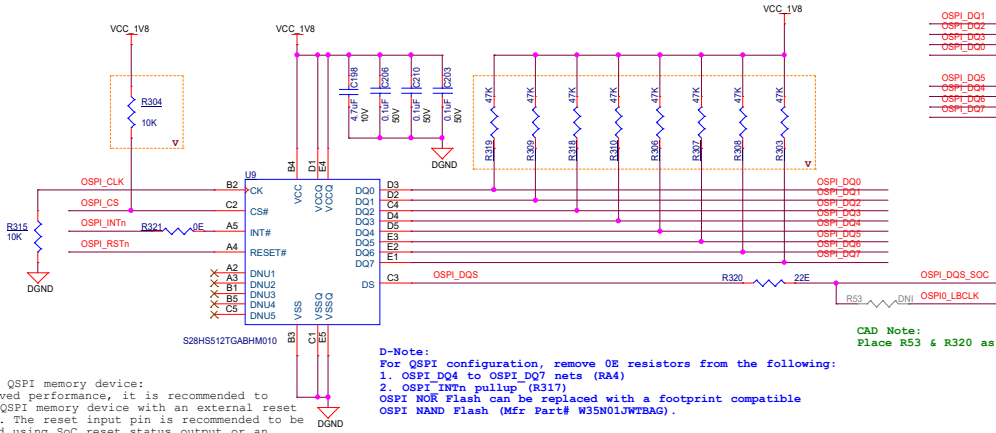
OSPI FLASH

D-Note:
Refer Custom Board Design and Simulation Guidelines for
Processor High Speed Parallel Interfaces
<https://www.ti.com/lit/pdf/sdaa087>

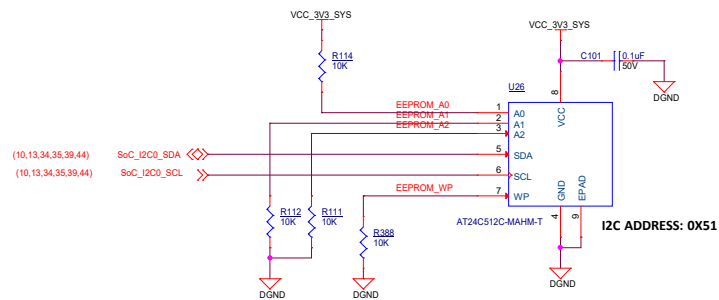
R-Note:
SoC IO buffers are off during reset and after reset.
A pullup is recommended to hold the attached
device IOs in a known state (does not float).
Usage of pullups are attached device dependent.

D-Note:
OR resistors are used for configuring QSPI0 or OSPI0 interface.
This is optional for custom board design.

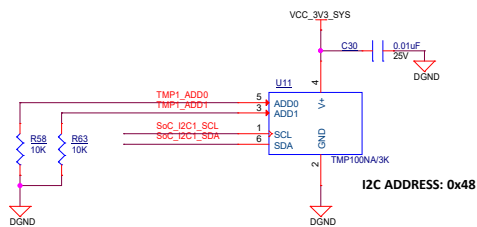
CAD Note:
Place RA3 & RA4 closer to the attached Memory Device



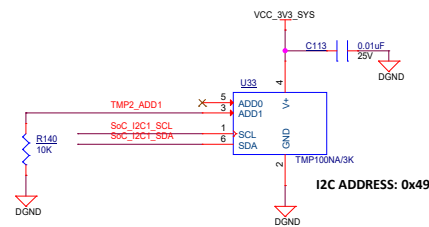
BOARD ID EEPROM



DIGITAL TEMPERATURE SENSORS



CAD Note:
Place the temperature sensor closer to the SoC.



CAD Note:
Place the temperature sensor closer to the SoC.



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Title BOARD ID EEPROM & DIGITAL TEMPERATURE SENSORS

Size PROC142B(002)

C

Date: Friday, May 08, 2026

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Rev B

CPSW3G RGMII 1 - ETHERNET PHY

D-Note:
The caps and values used are as per the EPHY
data sheet recommendations.

D-Note:
Ok to use 0402 package for 1uF cap to
match the 10uF bulk cap package size

D-Note:
Refer to DP83867ERG2-R-EVM when using Discrete LAN
Transformer Module and RJ45 connector.

R-Note:
Ferrite is DNI.

D-Note:
Refer Custom Board Design and Simulation Guidelines for
Processor High Speed Parallel Interfaces
<https://www.ti.com/lit/pdf/sdaa087>

D-Note:
Provide provision for series resistor
based on EPHY for RDX signals near
to the EPHY.

D-Note:
Allowed amplitude for XI clock input
is 1.8V irrespective of the IO supply
used. Use a capacitor divider when
the clock applied is 3.3V.

D-Note:
Refer to the EPHY EVM for JTAG connections.

D-Note:
RBIAS resistor value has
been reduced from 11K
and a parallel capacitor
has been added to improve
Ethernet compliance
testing performance

D-Note:
ANDing logic could be optimized to a 2-input AND gate. Use RESETSTATz (or
PORz_OUT) and the SoC IO as inputs to the ANDing logic.

D-Note:
ANDing logic additionally performs level translation. Verify
the reset IO level compatibility before optimizing the reset
ANDing logic. IO level mismatch can cause residual voltage
(supply leakage) and affect PMIC/SoC operation.

Note:
Full-up is enabled for GPIO input.
RESETSTATz series resistor is DNI.

RJ45 CONNECTOR WITH INTEGRATED MAGNETICS

Silk: CPSW PHY-1

PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

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Title CPSW3G RGMII_1 ETHERNET PHY

Size PROC142B(002)

C

Date: Friday, May 08, 2026

Rev

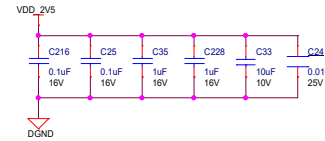
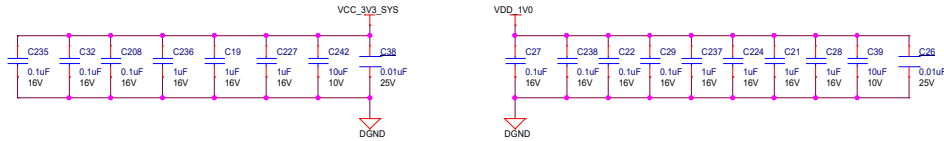
B

Sheet 24 of 46

D-Note:
The caps and values used are as per the
EPHY data sheet recommendations.

D-Note:
Ok to use 0402 package for 1uF cap to
match the 10uF bulk cap package size

CPSW3G RGMII 2 - ETHERNET PHY



D-Note:
Refer to DP83867ERG2-R-EVM when using Discrete LAN
Transformer Module and RJ45 connector.

R-Note:
Ferrite is DNI.

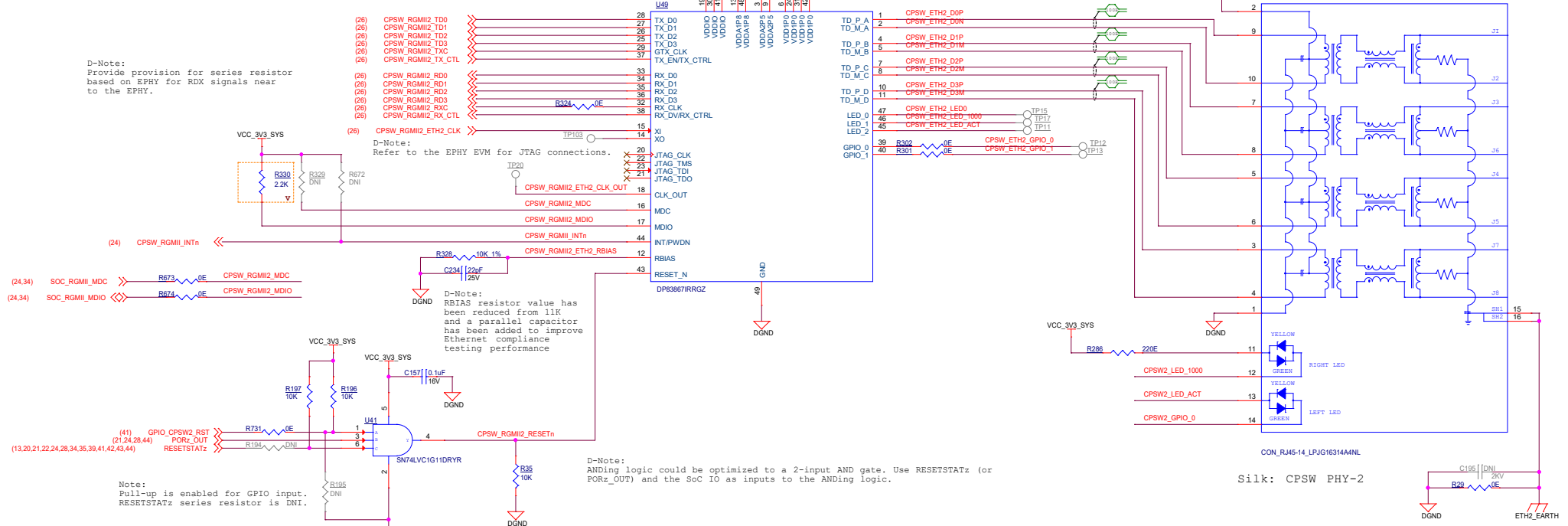
D-Note:
Refer Custom Board Design and Simulation Guidelines for
Processor High Speed Parallel Interfaces
<https://www.ti.com/lit/pdf/sdaa087>

D-Note:
Provide provision for series resistor
based on EPHY for RDX signals near
to the EPHY.

D-Note:
Refer to the EPHY EVM for JTAG connections.

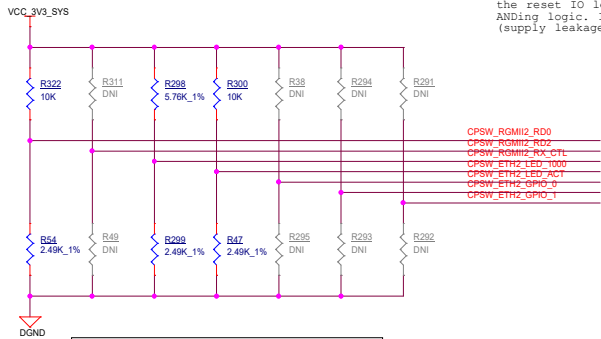
D-Note:
Verify the power sequence requirements
for Two-Supply Configuration and
Three-Supply Configuration.

RJ45 CONNECTOR WITH INTEGRATED MAGNETICS



D-Note:
ANDing logic additionally performs level translation. Verify
the reset IO level compatibility before optimizing the reset
ANDing logic. IO level mismatch can cause residual voltage
(supply leakage) and affect PMIC/SoC operation.

Note:
Pull-up is enabled for GPIO input.
RESETSTATz series resistor is DNI.



PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

Designed for TI by Mistral Solutions Pvt Ltd



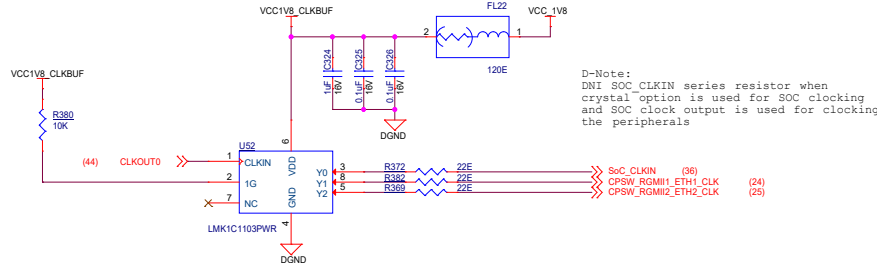
Title CPSW3G RGMII_2 ETHERNET PHY

Size	PROC142B(002)	Rev	B
C		Date	Friday, May 08, 2026
Sheet	25	of	46

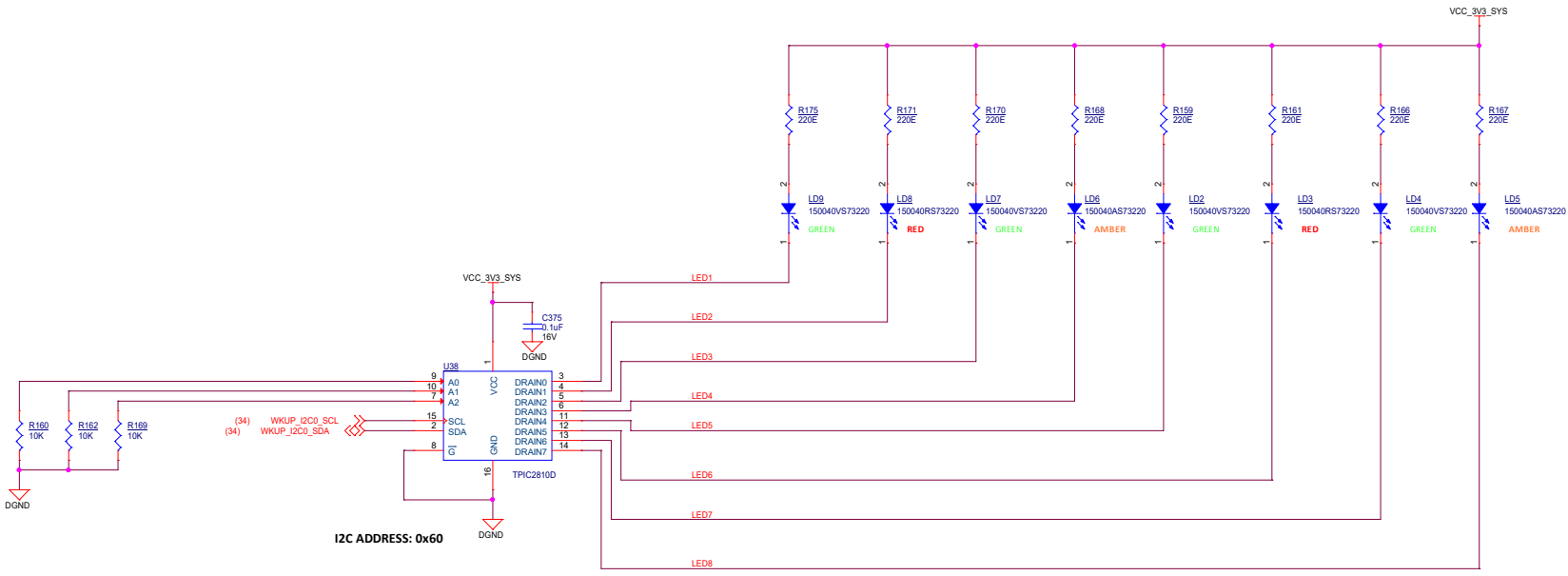
SOC MAC INTERFACE



CLOCK BUFFER FOR SOC AND ETHERNET PHYs



LED DRIVER



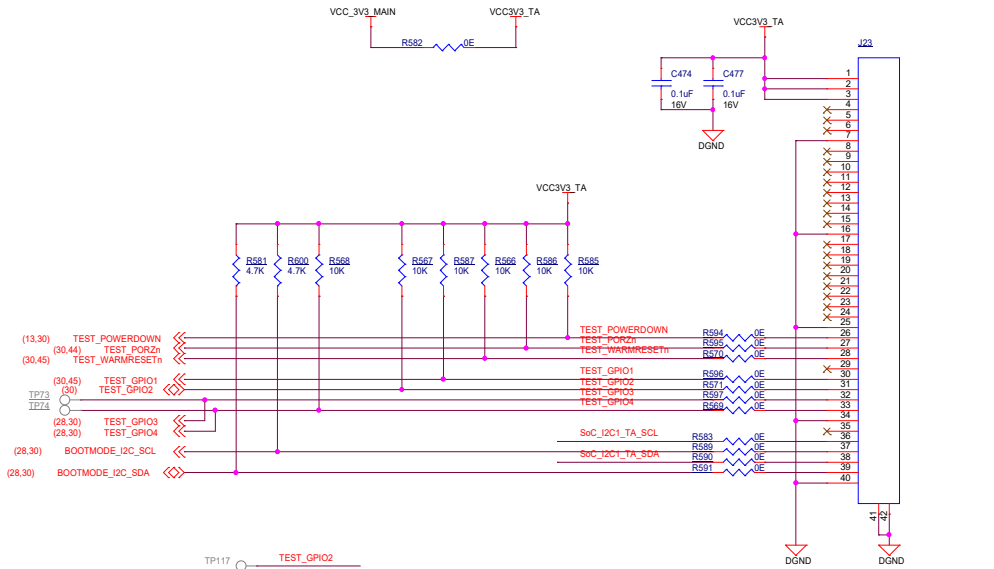
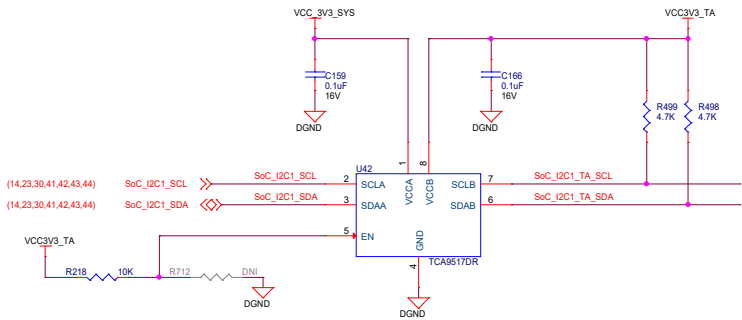
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Title SOC MAC INTRFACE, SOC AND ETHERNET PHYs CLOCK BUFFER, LED DRIVER		
Size	PROC142B(002)	Rev
C		B
Date:	Friday, May 08, 2026	Sheet 26 of 46

40-PIN TEST AUTOMATION HEADER

I2C BUS BUFFER



CON_FLEX_40X1_FH12A-40S-0.5SH
Silk: AUTOMATION HDR

TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on MCU_GPIO0_15 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to a Testpoint	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

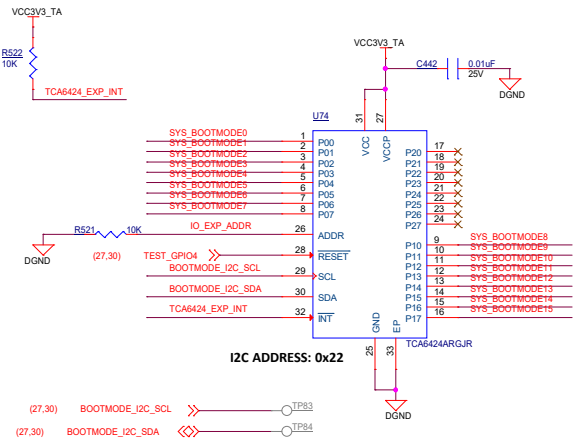
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Title TEST AUTOMATION		Rev
Size	PROC142B(002)	B
C		
Date: Friday, May 08, 2026	Sheet 27 of 46	

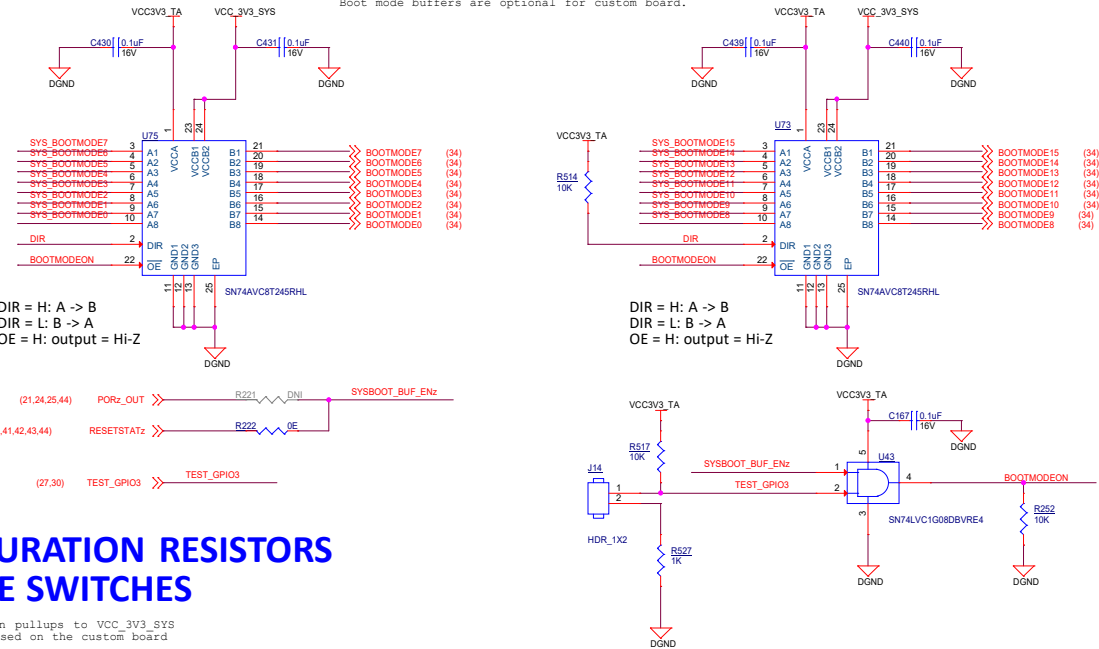
BOOTMODE IO EXPANDER

D-Note:
Add an additional decap.
Verify and terminate unused I/Os.



BOOT MODE BUFFERS

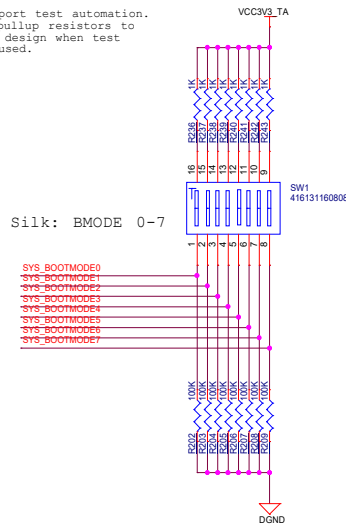
D-Note:
Boot mode buffers are optional for custom board.



BOOTMODE CONFIGURATION RESISTORS AND BOOTMODE SWITCHES

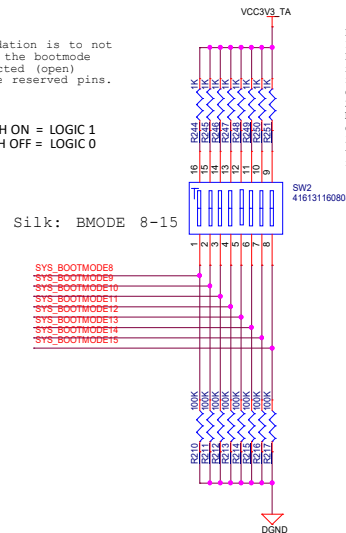
D-Note:
Connect bootmode configuration pullups to VCC3V3_SYS when test automation is not used on the custom board

D-Note:
VCC3V3_TA supply is used to support test automation. Connect bootmode configuration pullup resistors to SoC DVDD3V3 on the custom board design when test automation and buffers are not used.



D-Note:
The recommendation is to not leave any of the bootmode pins unconnected (open) including the reserved pins.

SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0



D-Note:
1. Dip switches are used on the SK for ease of configuration. DIP switches are optional on the custom board. A pull-up or pull-down resistor can be used to set the bootmode configuration. Provide provisions for pull-up and pull-down resistors for the bootmode pins that have configuration capability.
2. When DIP switches are used on the custom board, provision for an external ESD protection may be required if the DIP switches are expected to be configured in an uncontrolled ESD environment.
3. When DIP switches are used, reduce the resistor values used for the divider to 47k and 2K (1K) ohms to optimize the current draw in case the I/Os are used for alternate functions (output).

BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. USB0 DFU
6. BACKUP BOOT OPTION

FAQs FOR REFERENCE TO IMPLEMENT BOOTMODE CONFIGURATION (WITH BUFFER OR WITHOUT BUFFER):

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1391522/faq-am625-am623-am644x-am243x-am62a-am62p-am62d-q1-am62l---bootmode-implementation-without-buffers>

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1414148/faq-am625-am623-am644x-am243x-am62a-am62p-am62d-q1-am62l---bootmode-implementation-with-buffers>

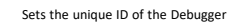
Designed for TI by Mistral Solutions Pvt Ltd



Title BOOT MODE CONFIGURATION BUFFERS & DIP SWITCHES

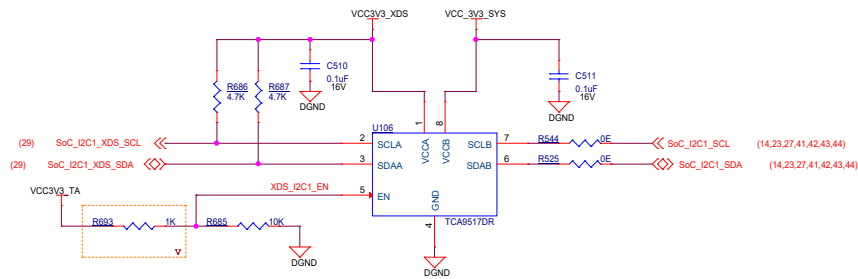
Size	PROC142B(002)	Rev	
C		B	
Date:	Friday, May 08, 2026	Sheet	28 of 46

D-Note:
Please follow SK-AM62P-LP EVM implementations for the latest updates on XDS110.

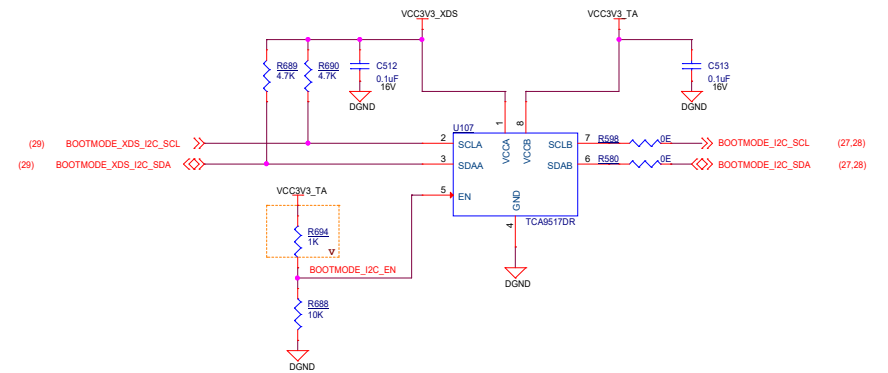


Title		XDS110 DEBUGGER	
Size	PROC142B(002)	Rev	
C		B	
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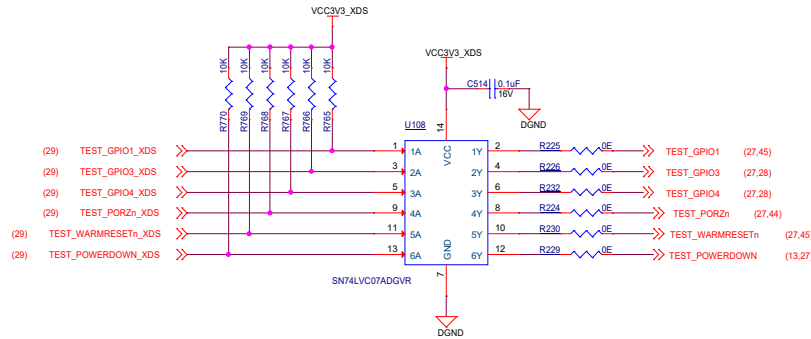
SOC I2C BUS BUFFER



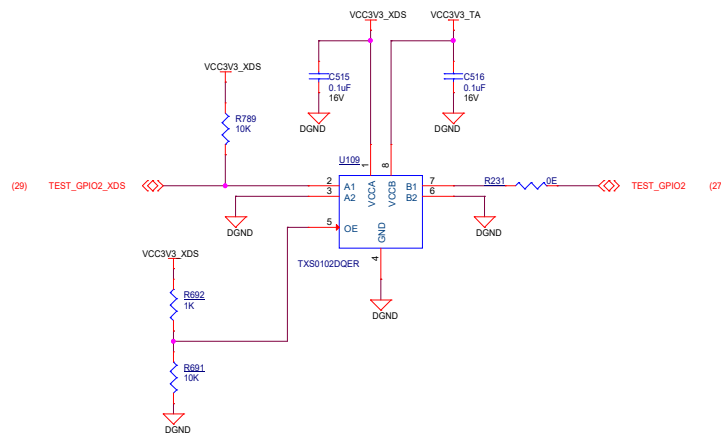
BOOTMODE_I2C_TA BUFFER



ISOLATION BUFFERS FOR TA SIGNALS



D-Note:
Pull-ups (R587, R517, R568, R586, R566, R565 & R567) referenced to VCC3V3_TA are added near to the test automation header



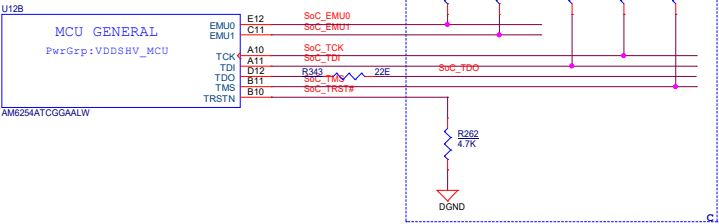
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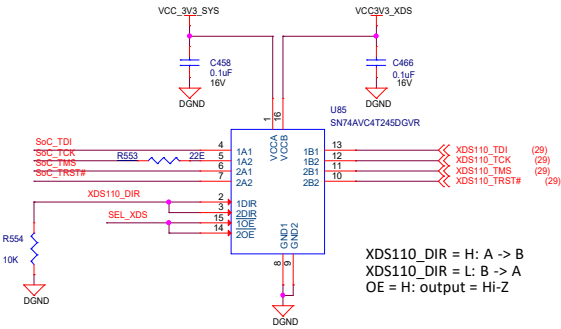
Title AUTOMATION SIGNALS BUFFER

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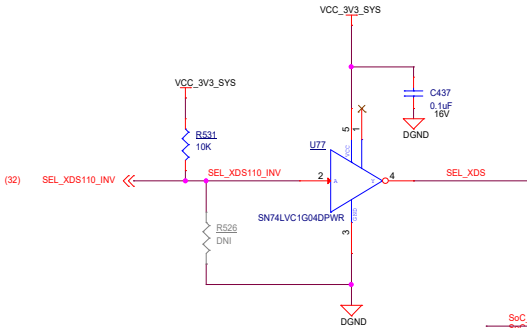
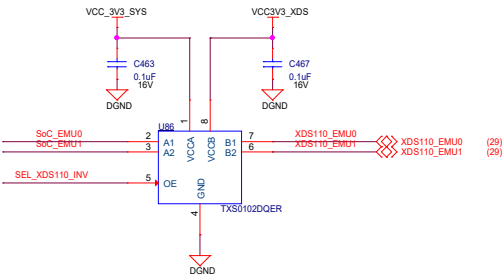
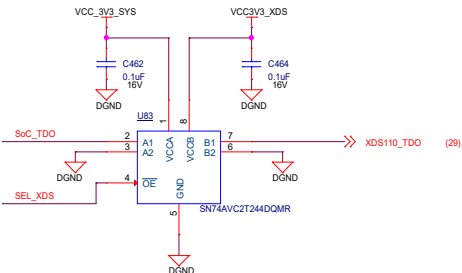
JTAG SOC SECTION



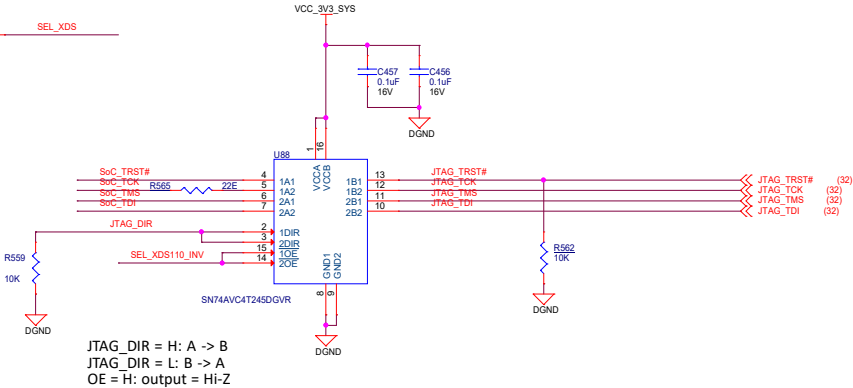
BUFFER XDS110



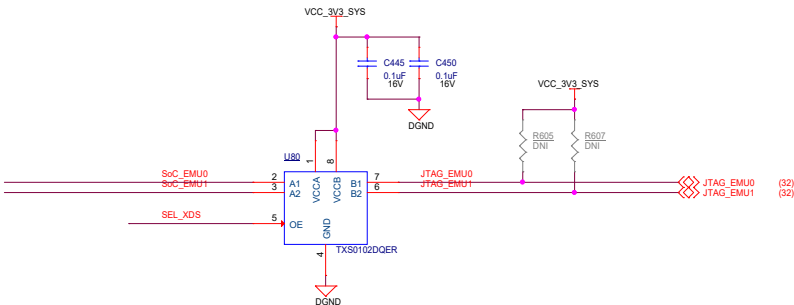
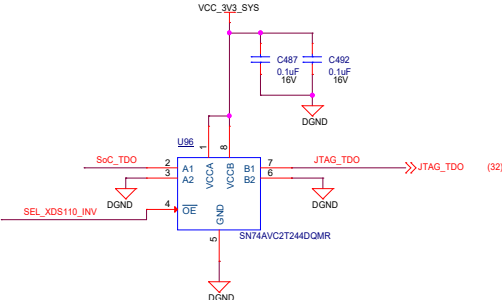
XDS110_DIR = H: A -> B
XDS110_DIR = L: B -> A
OE = H: output = Hi-Z



cTI20 JTAG BUFFERS



JTAG_DIR = H: A -> B
JTAG_DIR = L: B -> A
OE = H: output = Hi-Z



CAD Note:
Buffers U88 and U96 need to be placed closer to the cTI - 20 pin connector J17 to reduce the stub length of the JTAG signals.

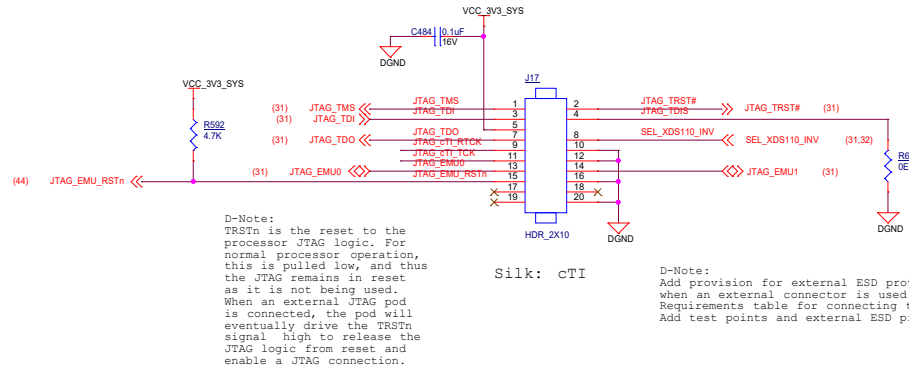
Designed for TI by Mistral Solutions Pvt Ltd



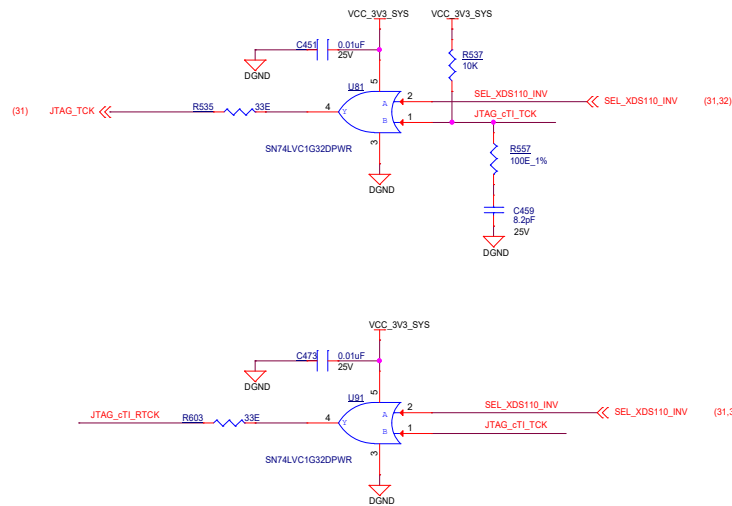
Title SOC JTAG INTERFACE AND JTAG BUFFERS

Size	PROC142B(002)	Rev	
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JTAG 20 PIN cTI CONNECTOR



JTAG CLOCK BUFFER



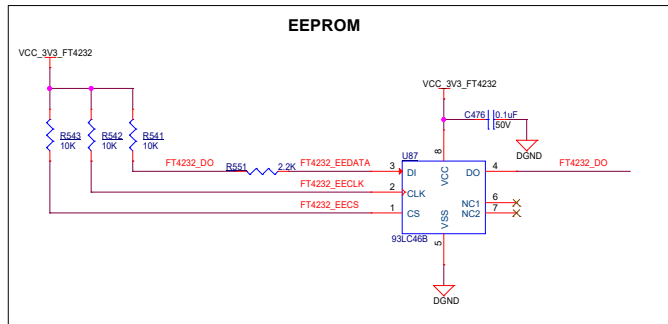
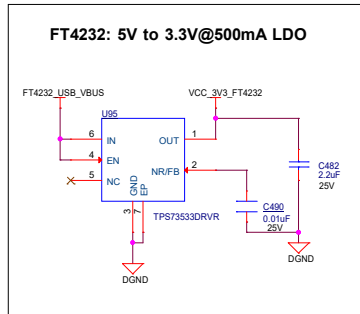
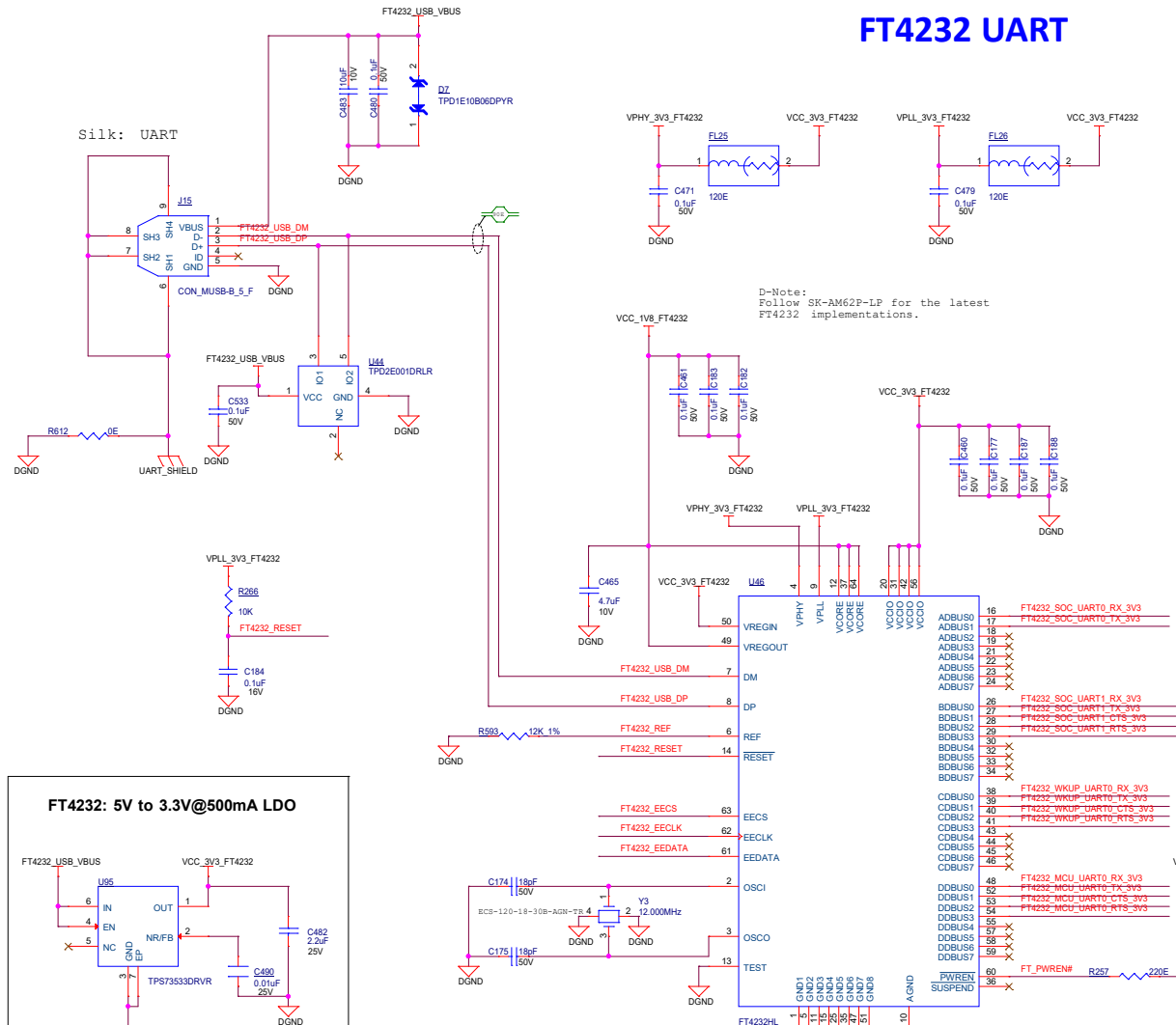
Designed for TI by Mistral Solutions Pvt Ltd



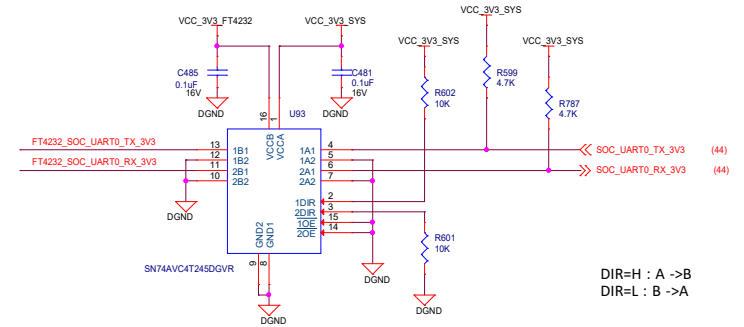
Title JTAG 20 PIN cTI CONNECTOR AND BUFFERS

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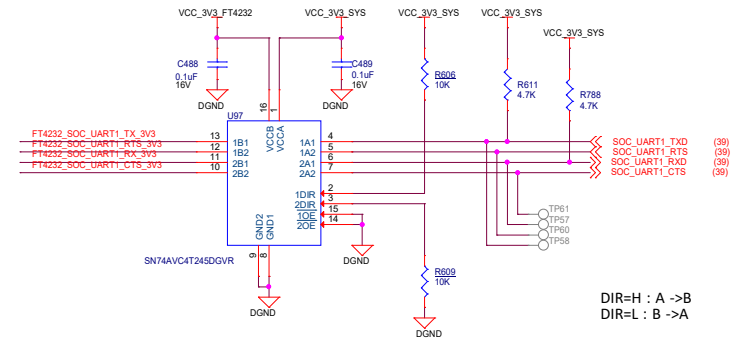
FT4232 UART



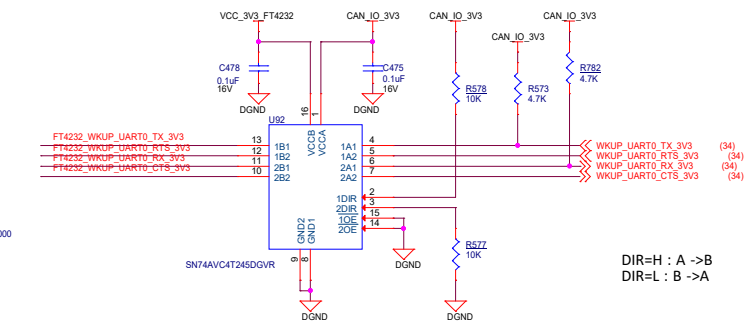
R-Note:
Verify the implementation with
the device manufacturer.



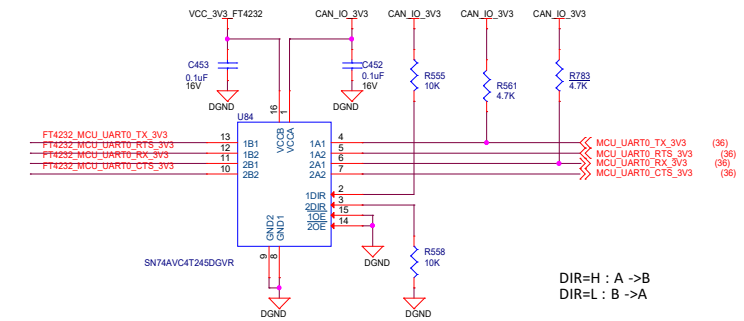
DIR=H : A ->B
DIR=L : B ->A



DIR=H : A → B
DIR=L : B → A



DIR=H : A \rightarrow B
DIR=L : B \rightarrow A



DIR=H : A → B
DIR=L : B → A

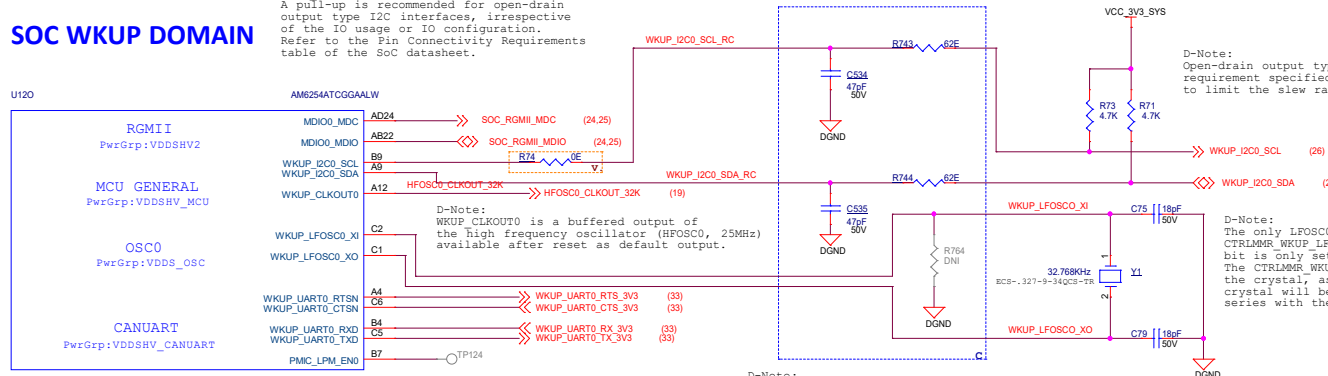


Title				FT4232 UART to USB BRIDGE			
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U120
```

	RGMII PwrGrp:VDDSHV2
	MCU_GENERAL PwrGrp:VDDSHV_MCU
	OSC0 PwrGrp:VDDS_OSC
	CANUART PwrGrp:VDDSHV_CANUART

D-Note:
WKUP_I2C0
A pull-up is recommended for open-drain output type I2C interfaces, irrespective of the IO usage or IO configuration. Refer to the Pin Connectivity Requirements table of the SoC datasheet.

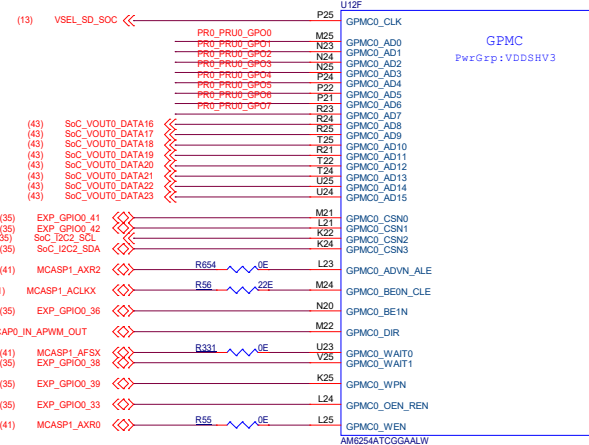


D-Note:
Delete or reduce the series resistor value to 0R when buffers are not used. The series resistors can be used to isolate the alternative function for testing the bootmode configuration.

D-Note:
Addition of Series and Parallel resistors.
Refer to the SoC data sheet for the recommended circuit
configuration for pre-production boards and production
boards.

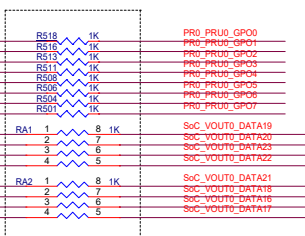
D-Note:
The only LFOSC0 register bits that should be changed by the customer are BP_C, PD_C, and CTRIMMR WKUP LFOSC0 TRIM[18:16] where PD_C is reset (0) to enable the oscillator and the BP_C bit is only set (1) to place the oscillator in bypass mode when using an LVCMOS clock source. The CTRIMMR WKUP LFOSC0 TRIM[18:16] bits are set based on the actual capacitance load applied to the crystal, as defined by the Load Capacitance Equation. The load capacitance range of the crystal will be half of the recommended capacitor value range, since they are connected in series with the resonant circuit of the crystal.

D-Note:
Add a series resistor OR when used as GPMC0 CLK.



Signals from Bootmode buffer

(28)	BOOTMODE0	»	_____
(28)	BOOTMODE1	»	_____
(28)	BOOTMODE2	»	_____
(28)	BOOTMODE3	»	_____
(28)	BOOTMODE4	»	_____
(28)	BOOTMODE5	»	_____
(28)	BOOTMODE6	»	_____
(28)	BOOTMODE7	»	_____
(28)	BOOTMODE11	»	_____
(28)	BOOTMODE12	»	_____
(28)	BOOTMODE15	»	_____
(28)	BOOTMODE14	»	_____
(28)	BOOTMODE13	»	_____
(28)	BOOTMODE10	»	_____
(28)	BOOTMODE8	»	_____
(28)	BOOTMODE9	»	_____



D-Note:
Shorting of multiple boot mode inputs (IOs) together is not recommended or allowed since the IOs have alternative functions that could be configured after booting.
Shorting the boot mode pins directly to VCC or ground is not recommended.
Connect each of the boot mode pins through separate resistors. Choose the boot mode resistor value based on the use case (10K or similar).

D-Note:
LVCMS IO buffers used to implement GPMC interface are off during reset and after reset until the host configures the interface. The recommendation is to add pulls for memory interface signals that can float. The required pulls for the GPMC interface signals are added on the GPMC interface add-on card.

D-Note:
Connect SYS_BOOTMODE signals (output) from
BOOTMODE configuration resistors and switches
when bootmode buffers are not used

R-Note:
Series resistors are used to isolate the SoC BOOTMODE input control logic after the BOOTMODE inputs value is latched.

D-Note:

1. 1k resistor at the output of the buffer is recommended when the bootmode pins are used for alternate functions to limit the buffer current
2. When bootmode isolation buffers are not used, connect the bootmode configuration resistors directly to the SOC bootmode input pins. Connect the SOC bootmode signal used for alternate function to the attached device through OR for isolation or testing.

D-Note:
When the boot mode isolation buffers are not used, connect the boot mode configuration resistors directly to the SoC boot mode input pins. Connect the SoC bootmode signal used for alternative function to the attached device through OR for isolation or testing.

Silk: PRU HDR

D-Note:
Any SoC IO that has a trace connected but not being driven actively needs to be connected to an external pull. When adding pull is not feasible, ensure that the traces are routed away from noisy signals.

D-Note:
Processor I/Os connected to the PRU Header are not fail-safe.
No external input shall be driven when the starter kit is not
powered-up.

D-Note:
LDO can source up to
500mA current



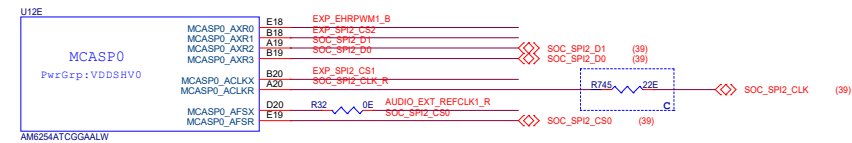
Title	SOC LFOSC0 AND SOC BOOTMODE INPUT PINS, PRU HEADER
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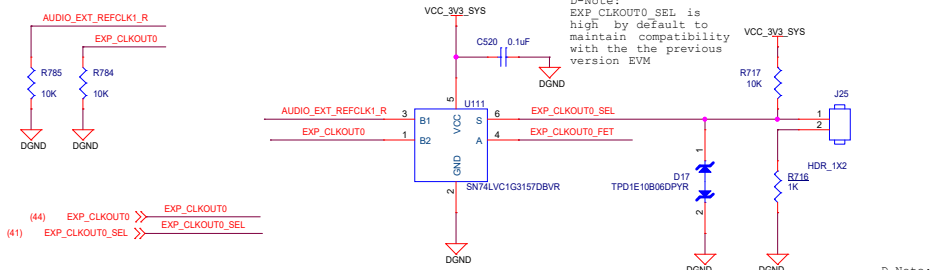
USER EXPANSION CONNECTOR

D-Note:
SoC IO buffers are off during reset. A parallel pull is recommended near to the attached device input that is being driven by the SoC IO (input does not float).

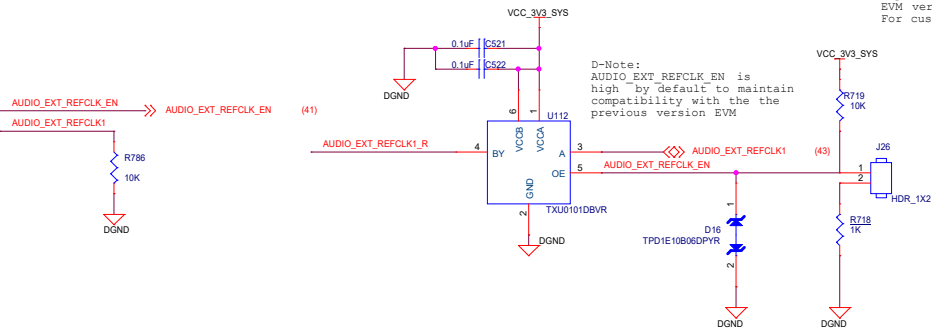
R-Note:
These supplies are off by default. The supplies are controlled by the below load switches and need to be enabled.



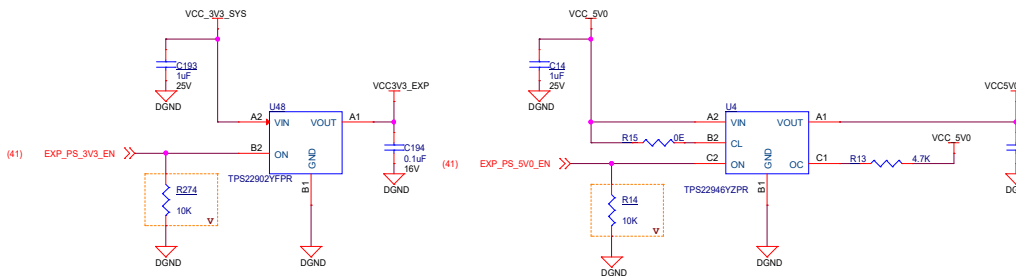
CAD Note:
R32 (Series damping resistor) should be placed closer to the SoC.



D-Note:
U111 & U112 are added to provide support for connecting DANTE daughter card on the User Expansion Connector (without affecting the connection compatibility with the previous EVM version).
For custom board designs, U111 & U112 can be deleted (based on the architecture).



LOAD SWITCHES FOR USER EXPANSION CONNECTOR



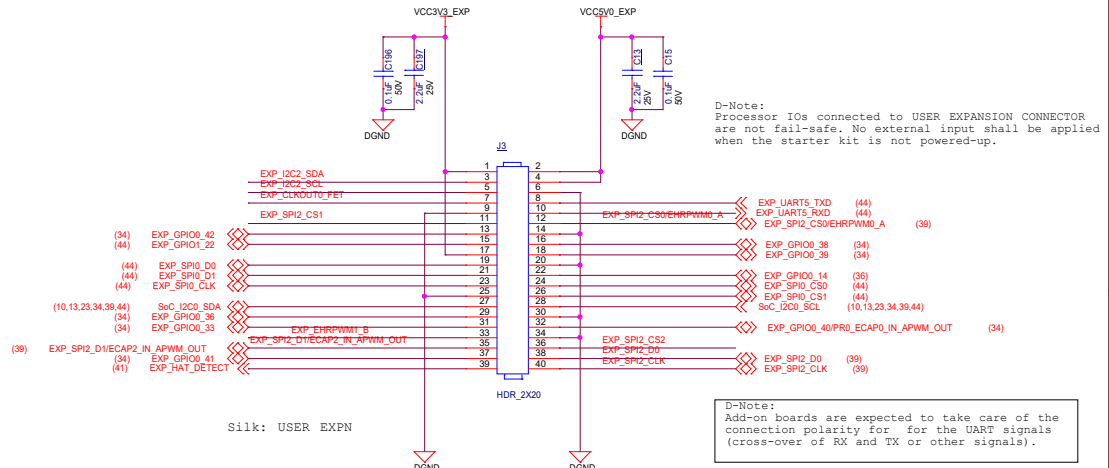
R-Note:

The Starter Kit shall not be powered through the 5V0 or 3V3 supply pins on the 40-pin User Expansion Connector (the pins are output supply).

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62P Starter Kit is not powered.

5V supply on User Expansion Connector can source 150mA max.

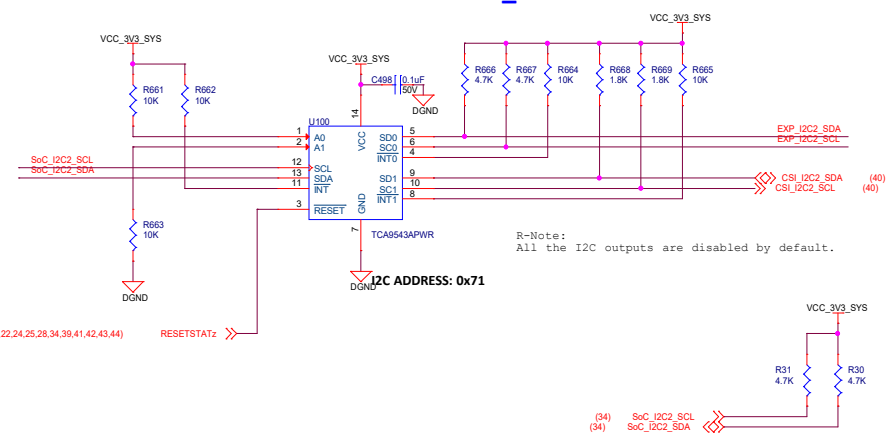
3V3 supply on User Expansion Connector can source 500mA max.



D-Note:
Add-on boards are expected to take care of the connection polarity for the UART signals (cross-over of RX and TX or other signals).

Silk: USER EXPN

I2C SWITCH FOR SoC_I2C2



R-Note:
All the I2C outputs are disabled by default.

I2C ADDRESS: 0x71

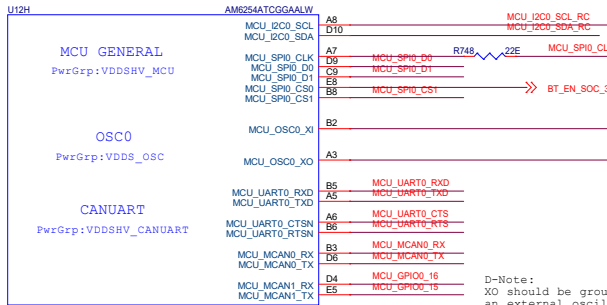
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Title			USER EXPANSION CONNECTOR
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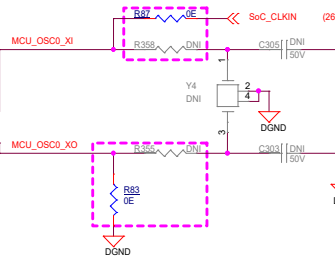
D-Note:
MCU_I2C0
A pull-up is recommended for open-drain output type I2C interfaces, irrespective of the IO usage or IO configuration. Refer to the Pin Connectivity Requirements table of the SoC datasheet.

SOC - MCU DOMAIN



D-Note:
SoC IO buffers are off during reset. A parallel pull is recommended near to the attached device input that is being driven by the SoC IO (input does not float).

D-Note:
Y2 recommended crystal part number:
Change the part number of Y4 to ABM11W-25.000MHZ-8-D1X-T3
Update DNI1 caps C305 and C303 to 12 pF



D-Note:
No HF08C0 registers are required to be changed. These registers should remain in their default state. Select the appropriate crystal circuit components that are compliant to the values defined in the MCU_OSC0 Crystal Circuit Requirements table. Read the Load Capacitance and Shunt Capacitance sections to select the appropriate crystal circuit components.

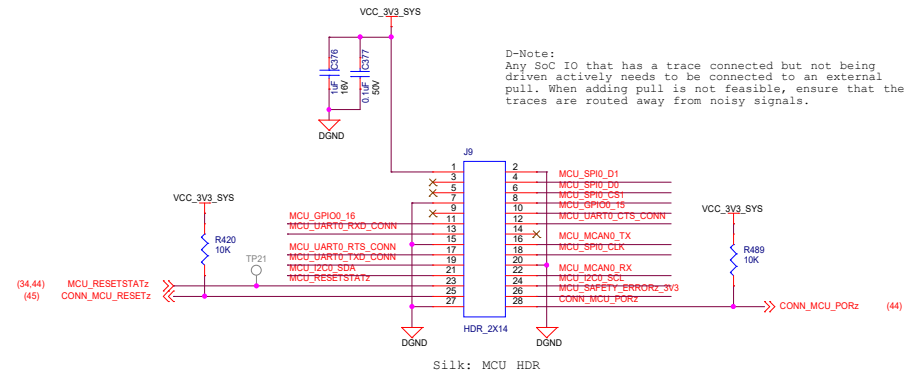
D-Note:
Refer to Applications, Implementation, and Layout section of the data sheet for clock routing guidelines as below:
Clock Routing Guidelines - Oscillator Routing

D-Note:
MCU_OSC0 has been validated only with a 25 MHz clock source, so that is the only frequency supported. The datasheet shows MCU_OSC0 not starting until after the core voltage, because there are some cases where the oscillator may not start until VDD_CORE is valid. In most cases it will start as early as VDD_OSC0, but this may not always be the case. This diagram in the datasheet is showing the maximum start-up time, which must include the case where the delay is based on VDD_CORE being valid.

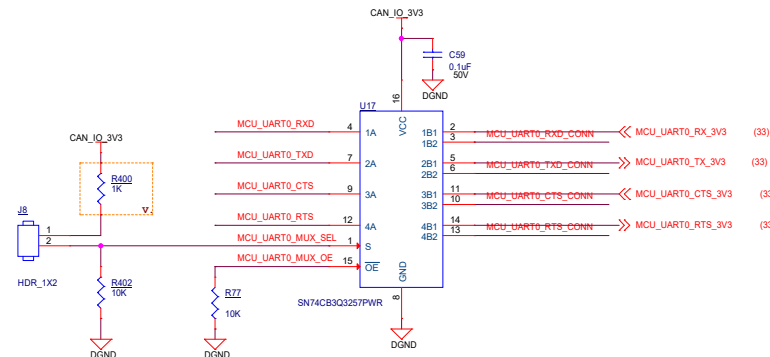
D-Note:
Connect the 25 MHz crystal directly to the SoC XI and XO pins (no series or parallel resistors are recommended). The internal oscillator implements AGC (Automatic Gain Control) for amplitude control. Match the SoC and the EPHY crystal specs.

SOC-MCU HEADER

D-Note:
Any SoC IO that has a trace connected but not being driven actively needs to be connected to an external pull. When adding pull is not feasible, ensure that the traces are routed away from noisy signals.



SOC - MCU_UART0 MUX



OEn	SEL	INPUT/OUTPUT An	
L	L (DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER

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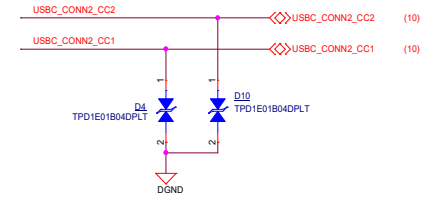
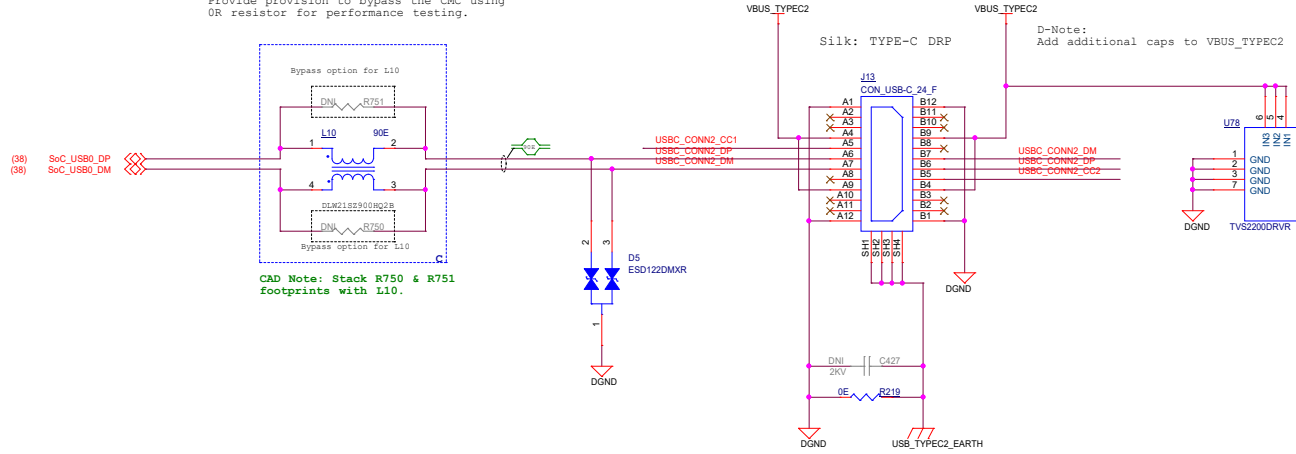
Title SOC-MCU DOMAIN IO, OSC0 and SOC-MCU IO HEADER

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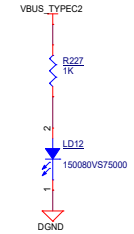
USB0 TYPE-C DRP

D-Note:
Refer to the SK/EVM user's guide for the recommended power adapters.
Using the recommended adapter is recommended for proper functioning of SK/EVM
Reference Document:
EVM User's Guide : <https://www.ti.com/lit/pdf/SPRUJ40>
Reference section : Power Requirement

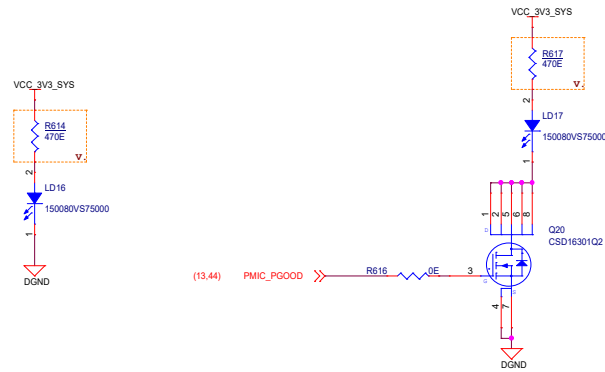
D-Note:
Provide provision to bypass the CMC using
OR resistor for performance testing.



POWER INDICATION LED: VBUS_TYPEC2



POWER RAIL LEDS



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Title USB0 TYPE-C DRP

Size PROC142B(002)

C

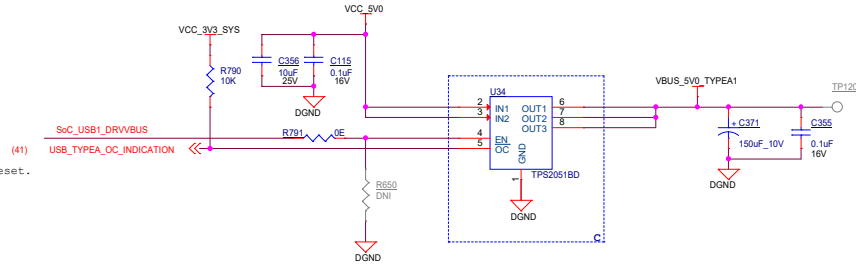
Date: Friday, May 08, 2026

Rev B

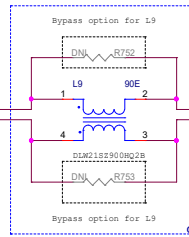
Sheet 37 of 46

USB1 - USB 2.0 TYPE-A

D-Note:
USBx_DRVVBUS Pull-down is a DNI to implement wake-up from deep sleep. For Normal USB operation, there is an internal pull-down enabled during SoC reset. USBx_DRVVBUS external pulldown can be populated when wake-up from deep sleep is not implemented.

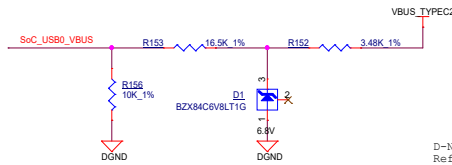


D-Note:
Provision to bypass the CMC using 0R resistor provided for testing the USB interface performance

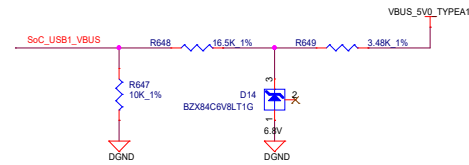


CAD Note:
Stack R752 & R753 footprints with L9.

D-Note:
VBUS divider and VBUS supply connection to processor
Connection of supply to USBx_VBUS pin is optional when USB interface is configured as Host



D-Note:
Refer to the USB VBUS Design Guidelines section of the SoC data sheet for implementing the VBUS voltage divider



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Title SOC USB INTERFACE, USB1 TYPE-A CONNECTOR, POWER SWITCH

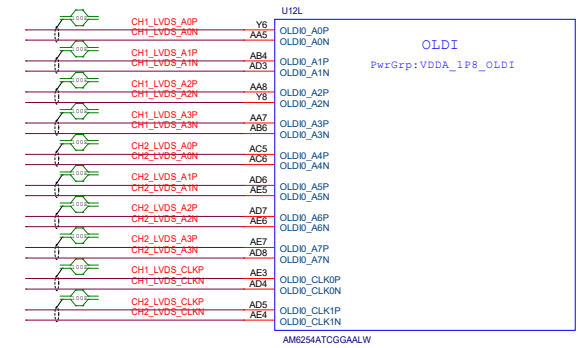
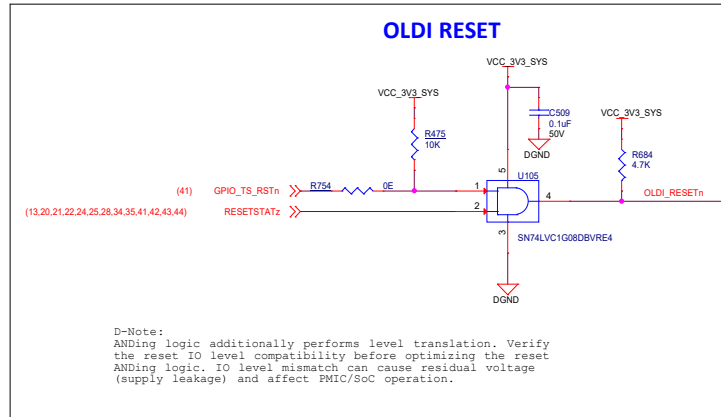
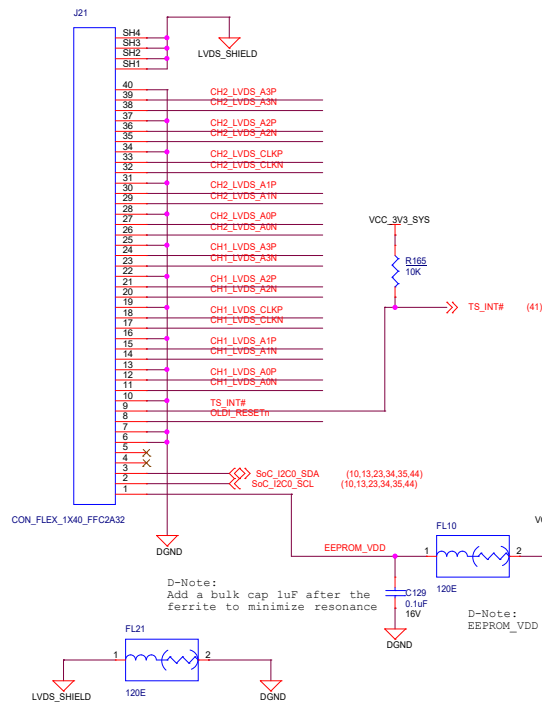
Size PROC142B(002)

C Date: Friday, May 08, 2026

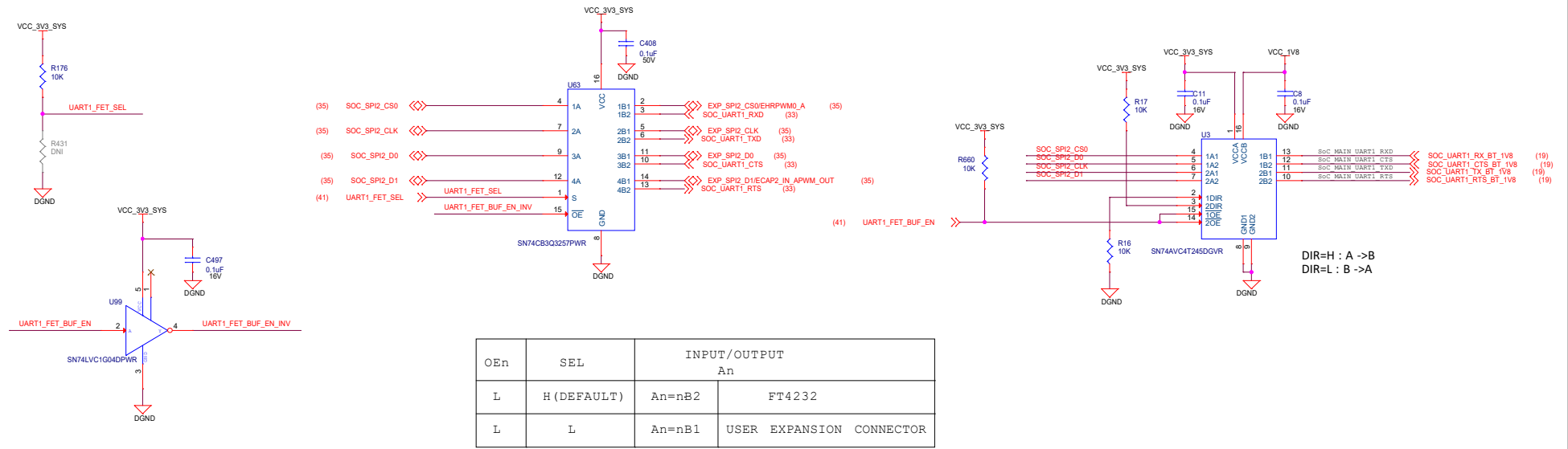
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Rev B

OLDI DISPLAY INTERFACE



SoC UART1 FET SWITCH & BUFFER



OEn	SEL	INPUT/OUTPUT An	
L	H (DEFAULT)	An=nB2	FT4232
L	L	An=nB1	USER EXPANSION CONNECTOR

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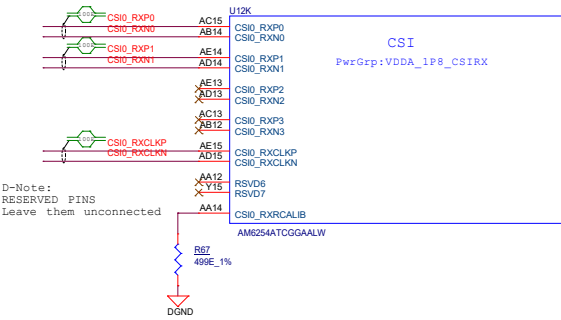
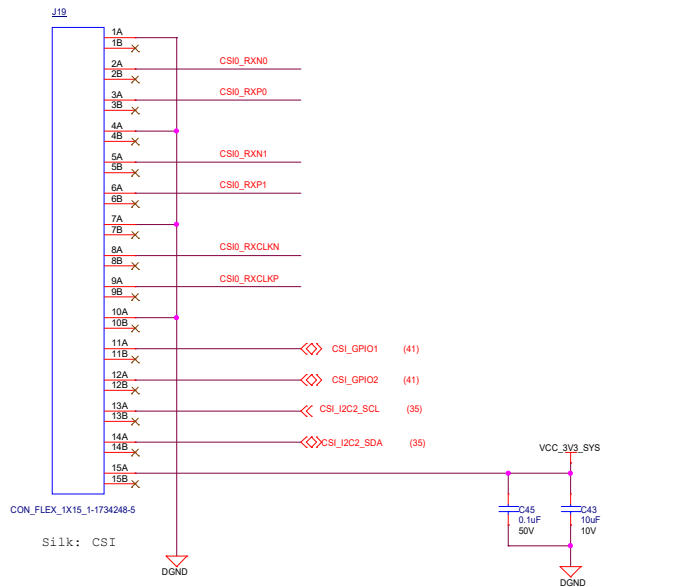


Title		SOC OLDI INTERFACE, LCD CONNECTOR & SOC UART1 FET SWITCH & BUFFER	
Size	PROC142B(002)	Rev	B
C		Date	Friday, May 08, 2026
Date	Friday, May 08, 2026	Sheet	39 of 46

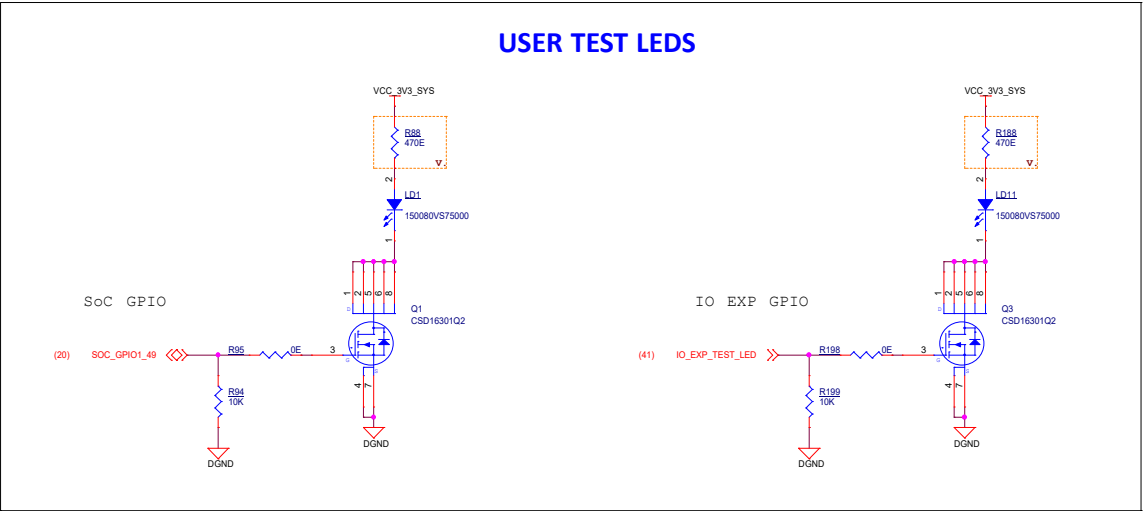
CSI INTERFACE

R-Note:
Based on the end product requirement, interface the CSI signals to the respective attached devices.

CSI CAMERA HEADER



USER TEST LEDS



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Title SOC CSI INTERFACE AND CAMERA CONNECTOR

Size PROC1428(002)

C

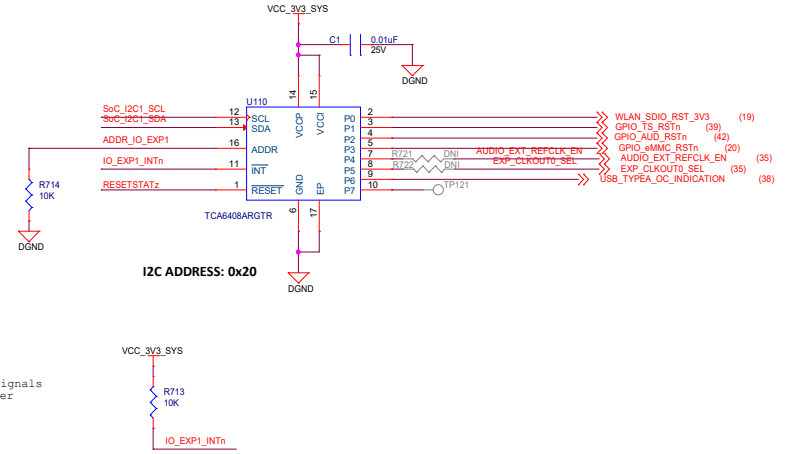
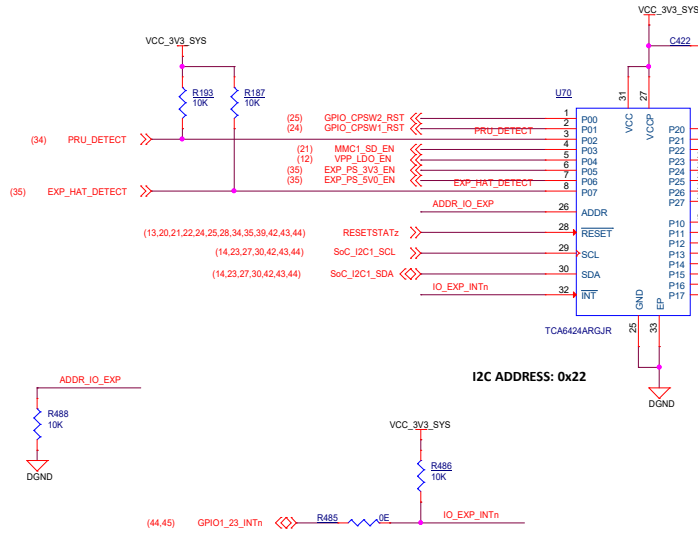
Date: Friday, May 08, 2026

Rev

B

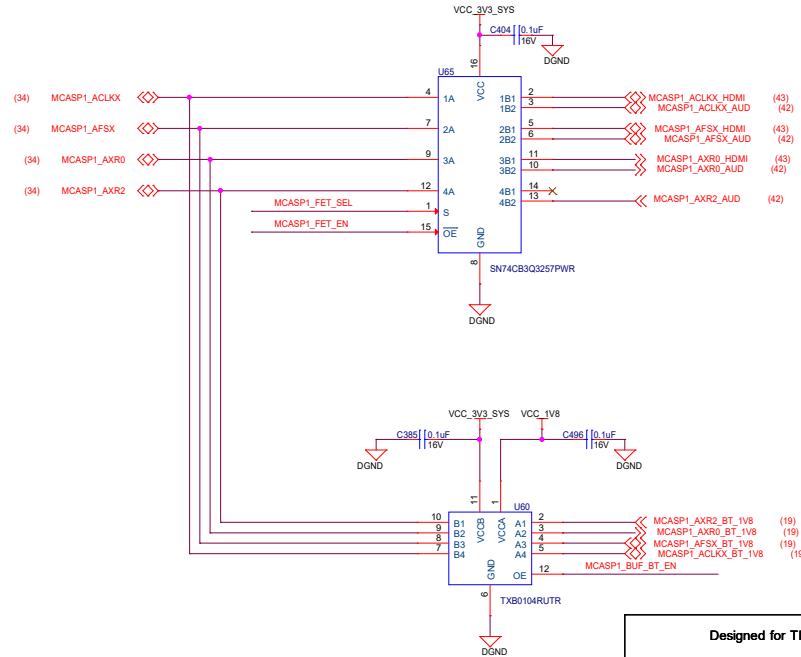
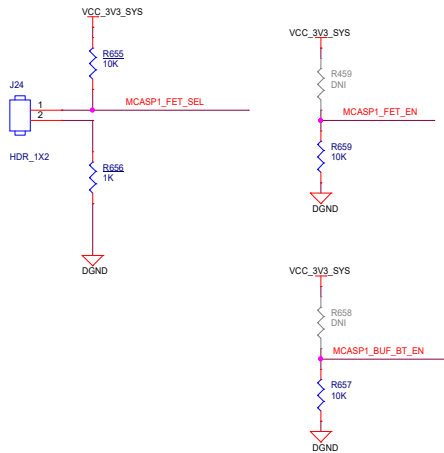
Sheet 40 of 46

IO EXPANDERS



D-Note:
When use of IO expanders are optimized, verify the signals used and assign the signals to processor IOs for proper functioning of the board.

MCASP1 FET SWITCH & BUFFER



OEn	SEL	INPUT/OUTPUT An	
L	H (DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

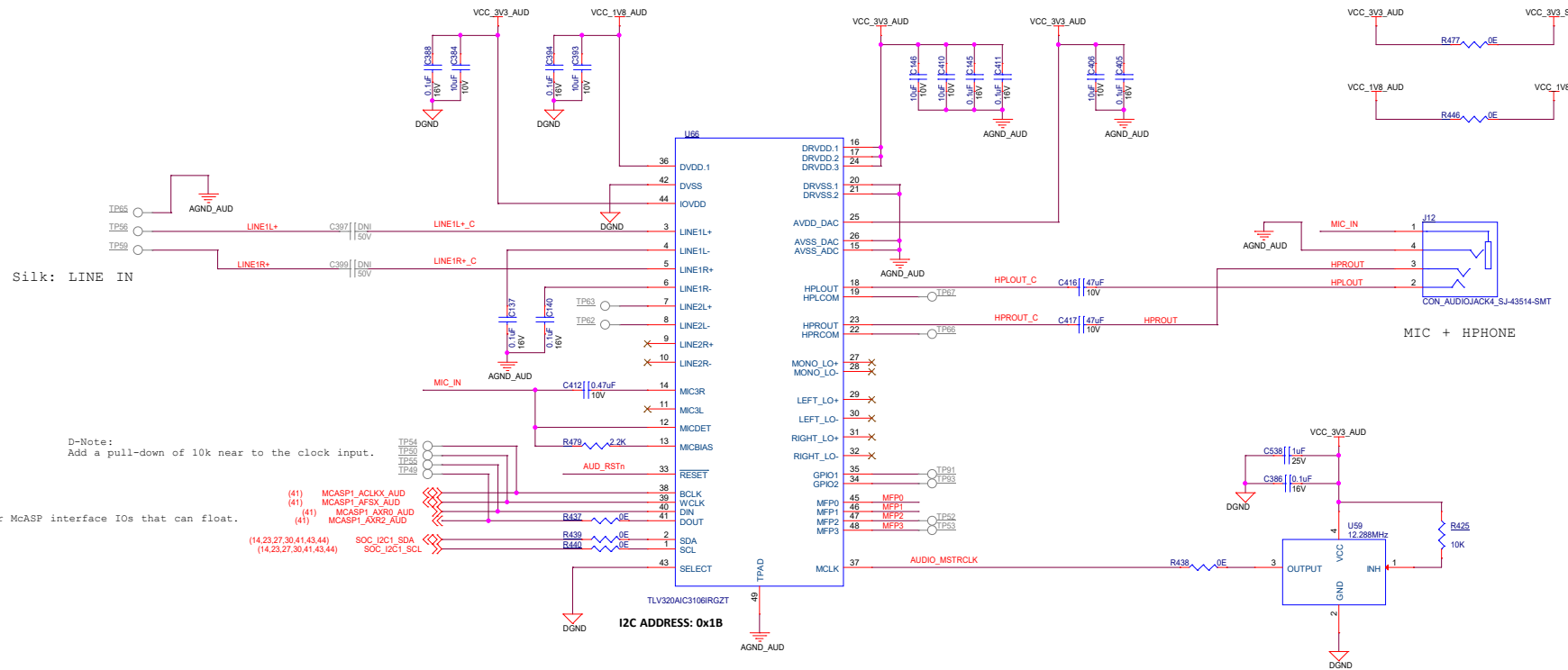
Designed for T1 by Mistral Solutions Pvt Ltd



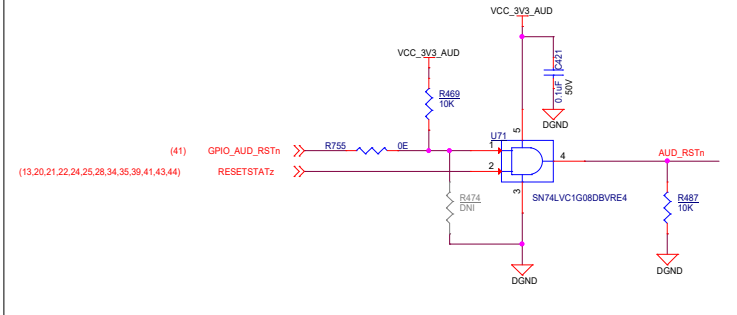
Title IO EXPANDER AND MCASP1 FET SWITCH & BUFFER

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AUDIO CODEC

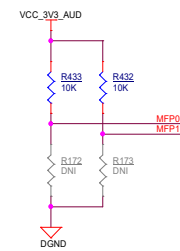


AUDIO CODEC RESET



CODEC I2C ADDRESS SELECTION

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B



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Title AUDIO CODEC

Size PROC1428(002)

C

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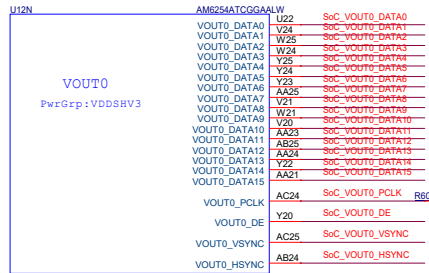
Rev B

SOC - VIDEO OUTPUT INTERFACE

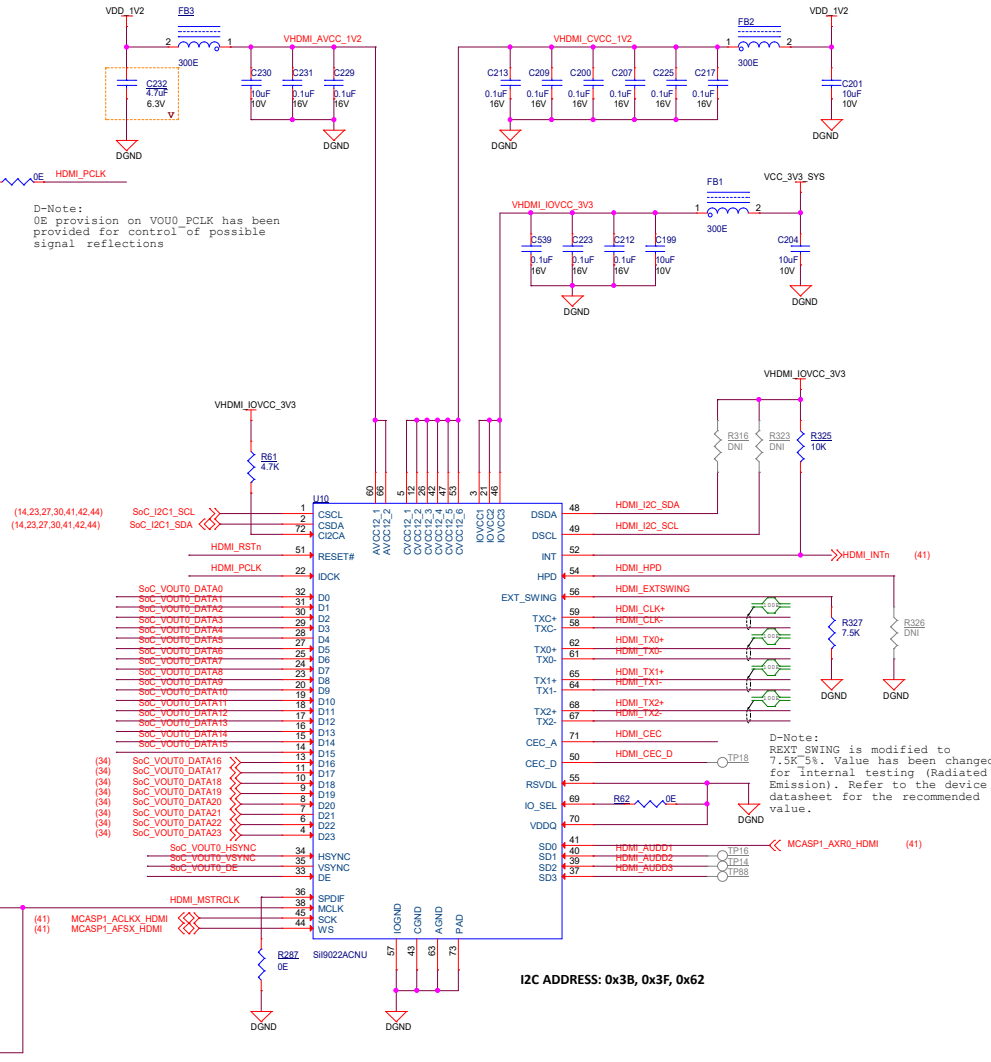
R-Note:
Verify the implementation with
the device manufacturer.

HDMI INTERFACE

D-Note:
Refer Custom Board Design and Simulation Guidelines for
Processor High Speed Parallel Interfaces
<https://www.ti.com/lit/pdf/sdaa087>

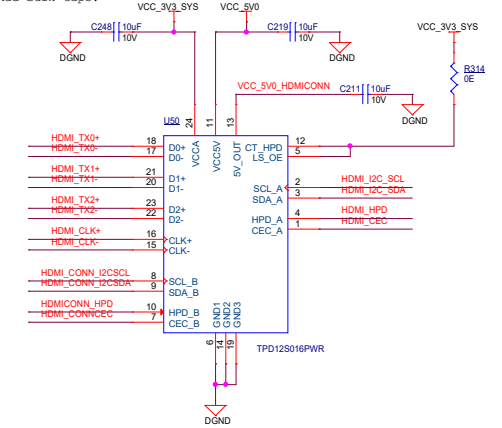


D-Note:
OE provision on VOU0 PCLK has been
provided for control of possible
signal reflections



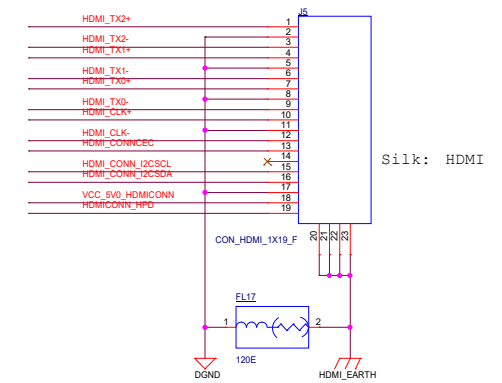
HDMI ESD DEVICE

D-Note:
Add bulk caps.

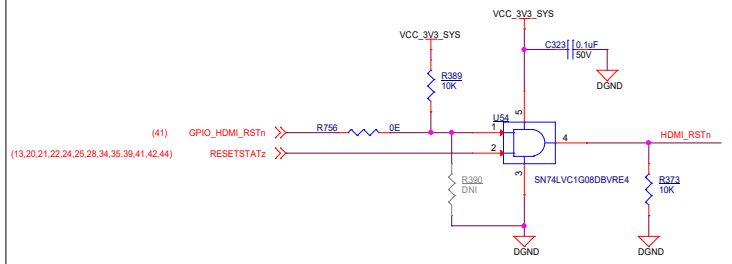


D-Note:
TPD12S016PWR has integrated pull-up or pull-down resistors on the I2C and HPD lines. Hence no external pull-up or pull-down is required.

HDMI CONNECTOR



HDMI RESET

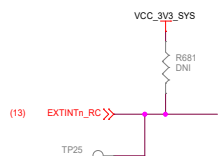
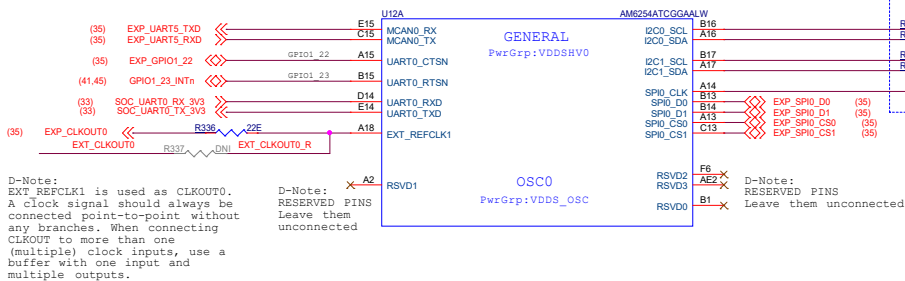


Designed for TI by Mistral Solutions Pvt Ltd



Title				SOC DPI INTERFACE, DPI TO HDMI TRANSMITTER INTERFACE			
Size		PROC142B(002)				Rev	
C						B	
Date:		Friday, May 06, 2026		Sheet		43 of 46	

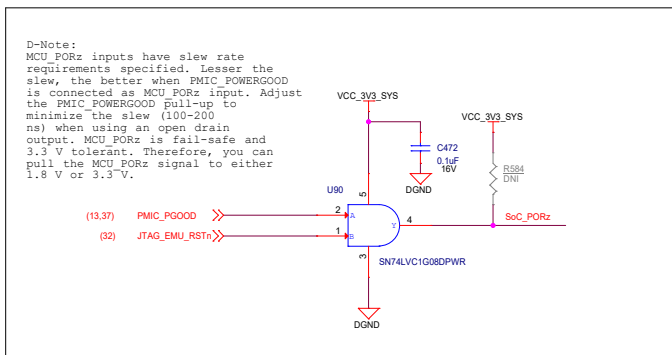
12A		AM25ATCGGAALW	
MCANO_RX	GENERAL PwrGrp: VDDSHV0	IC20_SCL	B16
MCANO_TX		IC20_SDA	A16
UART0_CTSN		IC21_SCL	B17
UART0_RTSN		IC21_SDA	A17
UART0_RXD		SP10_CLK	A14
UART0_TXD		B13	EXP SPI0_D0 (35)
EXT_REFCLK1		B14	EXP SPI0_D1 (35)
		A13	EXP SPI0_CS0 (35)
		C13	EXP SPI0_CS1 (35)
	OSC0 PwrGrp: VDDSD_OSC	RSVD0	F6
RSVD1		A2	D-NOTED: RESERVED PINS
		B1	RESERVED: Pins not connected



D-Note:
Provide provision for a pull-down. Populate when an attached device is connected. Refer to the SoC datasheet for Pin Connectivity Requirements.

[illegible]

D-Note:
Open-drain output type IO EXTINTn has slew rate limit specified,
when pulled to a 3.3 V supply. An RC is added to limit the slew rate



VCC1V8_CLKBUF

10K

U53
25.000MHz

0.01uF
25V

1uF
25V

DQND

EXT_CLKOUT0

R385

DNI

R384

22E

CLKOUT0

26

TRI-STATE

OUTPUT

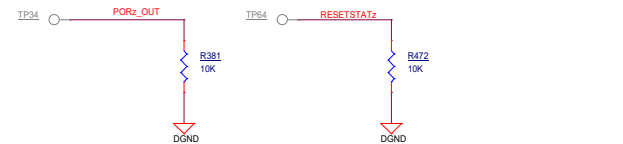
CLKOUT0_OSC

EC6-2520M0-250-CN-TR

D-Note:
Add 10K pulldown
when EXT_CLKOUT0
is configured as
peripheral clock

D-Note:
Recommended
oscillator
part number
LMK6CE0250DDLEF

D-Note:
Refer to the SoC data sheet for oscillator
specifications when the oscillator is used
along with clock buffer and also when
the oscillator is directly connected as
SoC clock input.



D-Note:
Pull-down resistor on PORz_OUT and RESETSTATz is provided to hold the attached device in reset condition during SoC reset and power-up.

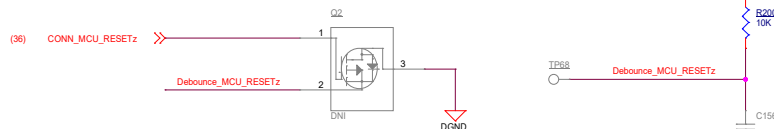


MISTRA

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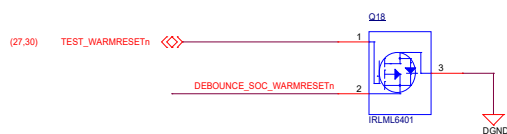
EXTERNAL RESET INPUT AND SCHMITT TRIGGER DEBOUNCE LOGIC

MCU WARM RESET

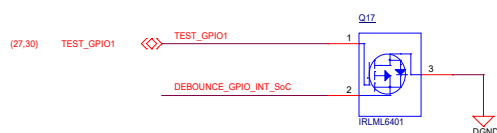


D-Note:
DNI: Q2 and C156.
Refer to errata:
i2407- RESET: MCU_RESETSTATz unreliable when MCU_RESETz is asserted low.

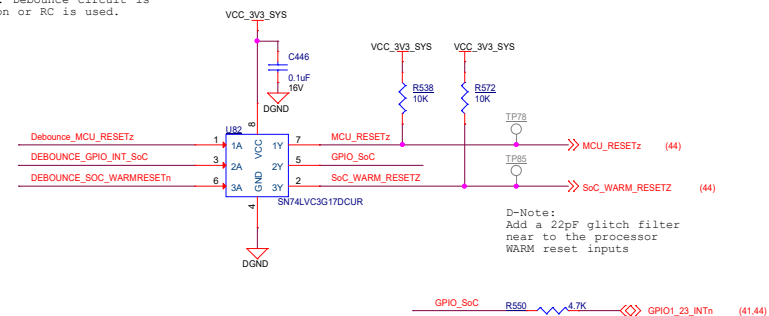
SOC WARM RESET



USER INTERRUPT



DEBOUNCE CIRCUIT



D-Note:
Add a 22pF glitch filter
near to the processor
WARM reset inputs

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Title: SOC PUSH BUTTON RESET INPUTS, DEBOUNCE LOGIC FOR RC RESET

Size: PROC142B(002) Rev: B

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MOUNTING HARDWARE

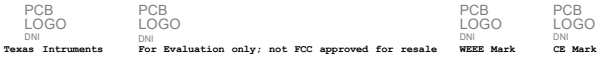
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB



LOGOs



LABELS

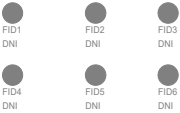
Board Serial No. Assembly Revision



STANDOFF,SCREW & WASHER FOR PCIe M.2



FIDUCIALS



ORDERABLE PART NO



Oderable Part Number	
Variant	Label Text
001	SK-AM62-P1
002	SK-AM62B-P1

R-Note:
Refer to STRAP CONFIGURATION OF ETHERNET PHYS
page from SK-AM64B schematics.

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Title		ASSEMBLY NOTES AND MOUNTING HARDWARE	
Size	PROC142B(002)	Rev	
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