

J721E SOM - DUAL TPS65941x PMICs

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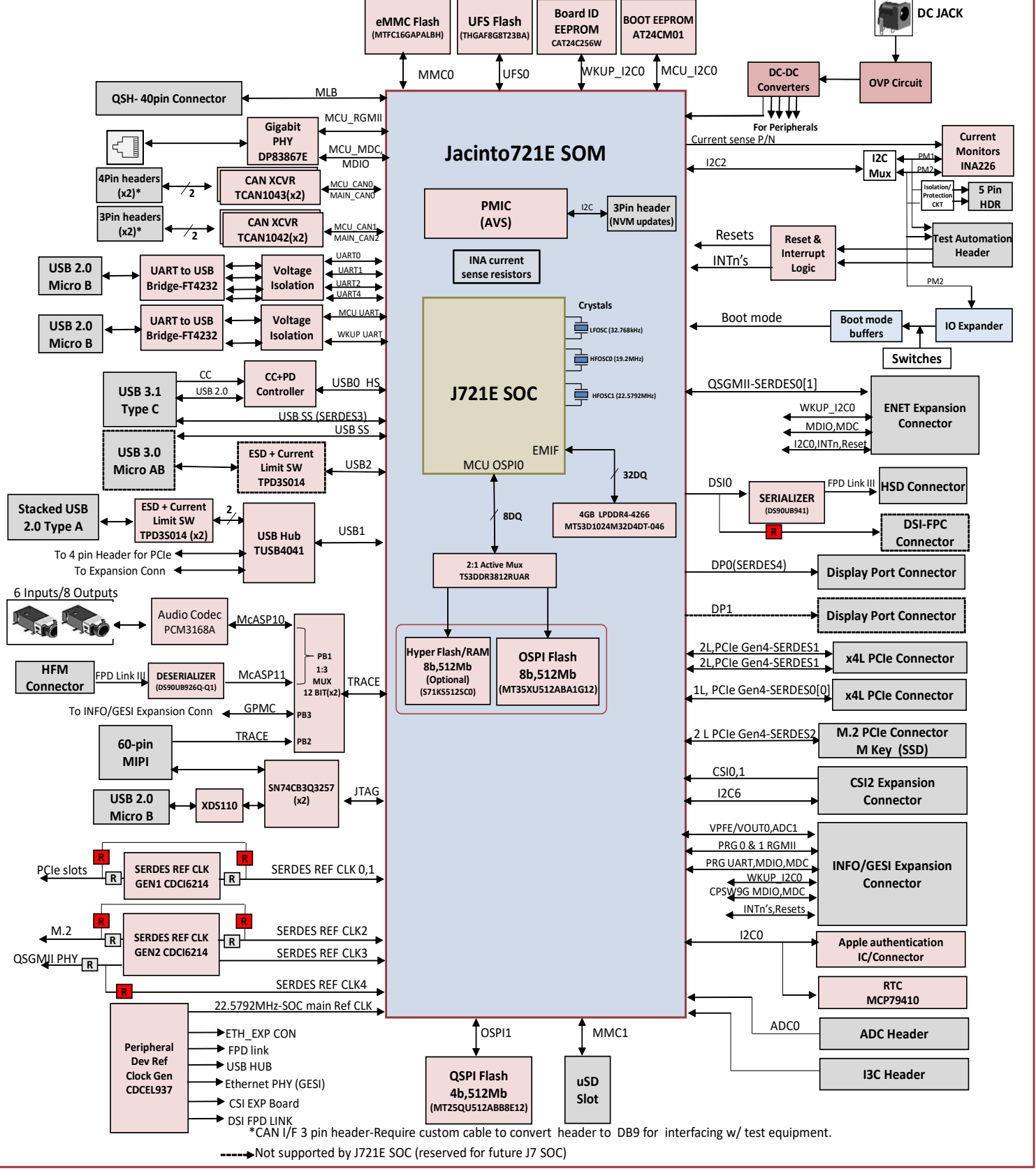
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REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E8A	18 FEB 2021	Drafted from PROC078E8 SCH Released on 23 NOV 2020 Updated PMIC - A(U27) , PMIC - B(U29) and SoC(U9) part numbers for the Silicon Revision changes U9 - J7ES SoC SR1.1: XJ721EGBALF U27 - Leo PMIC A 2.0: PTPS65941310RWERQ1 U29 - Leo PMIC B 2.0: PTPS65941111RWERQ1	Mistral Design Team		

Common Processor Board



2-Phase VDD_CPU PDNs
Not Recommended for New Designs
ALL New Designs should use
3-Phase Buck supplying VDD_CPU
(see SCH's last page)

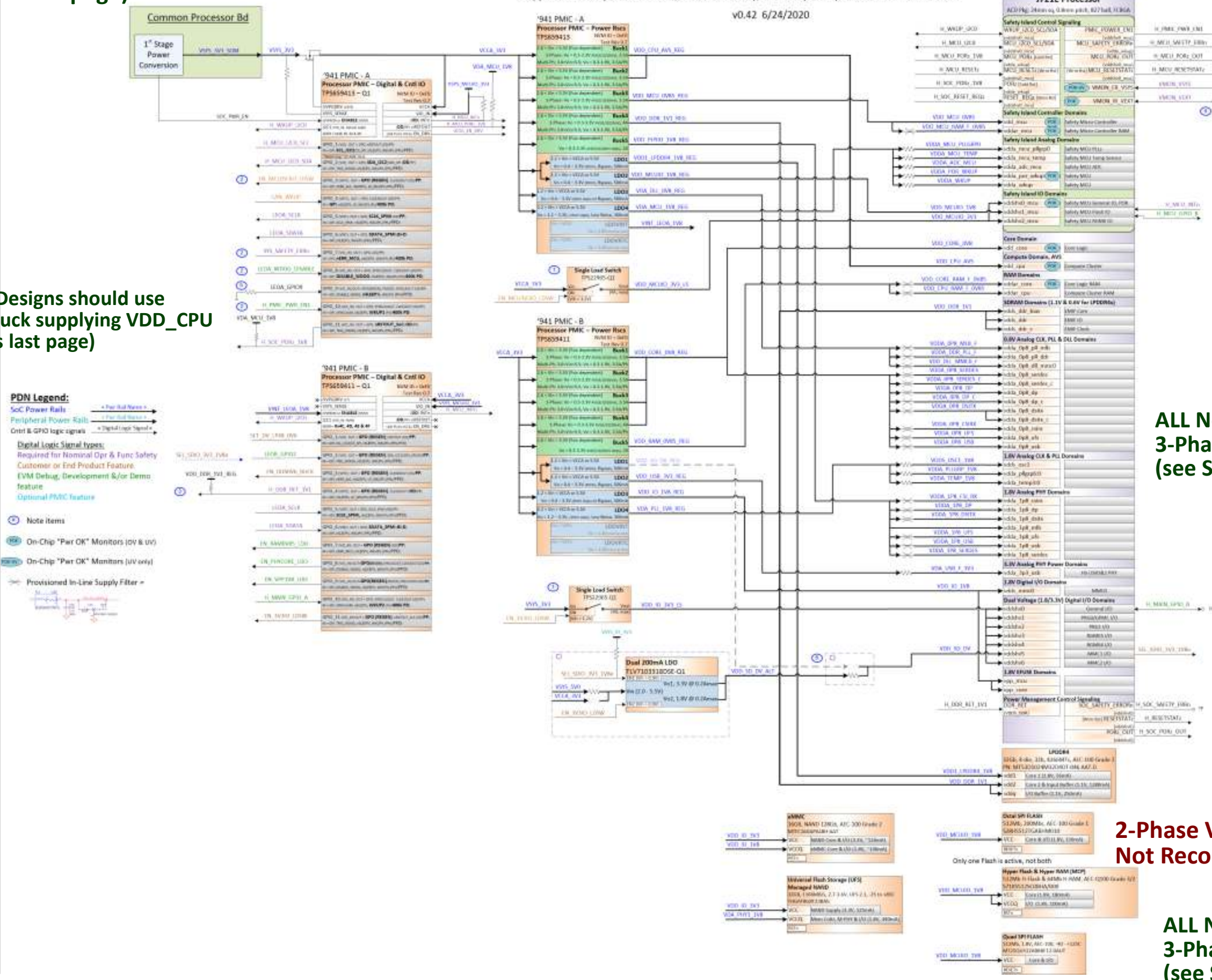
EVM's 2-Phase DUAL PMIC Power Distribution Network (PDN)
(2-Phase Buck supplying VDD_CPU)

2-Phase VDD_CPU PDNs
Not Recommended for New Designs
ALL New Designs should use
3-Phase Buck supplying VDD_CPU
(see SCH's last page)

J721E EVM Dual TPS65941 SoC PDN Overview
(Power Rail & GPIO Mapping Overview)

Supports J721E Superset Use Case, Functional Safety, MCU Only & Suspend-to-RAM with LPDDR4

v0.42 6/24/2020



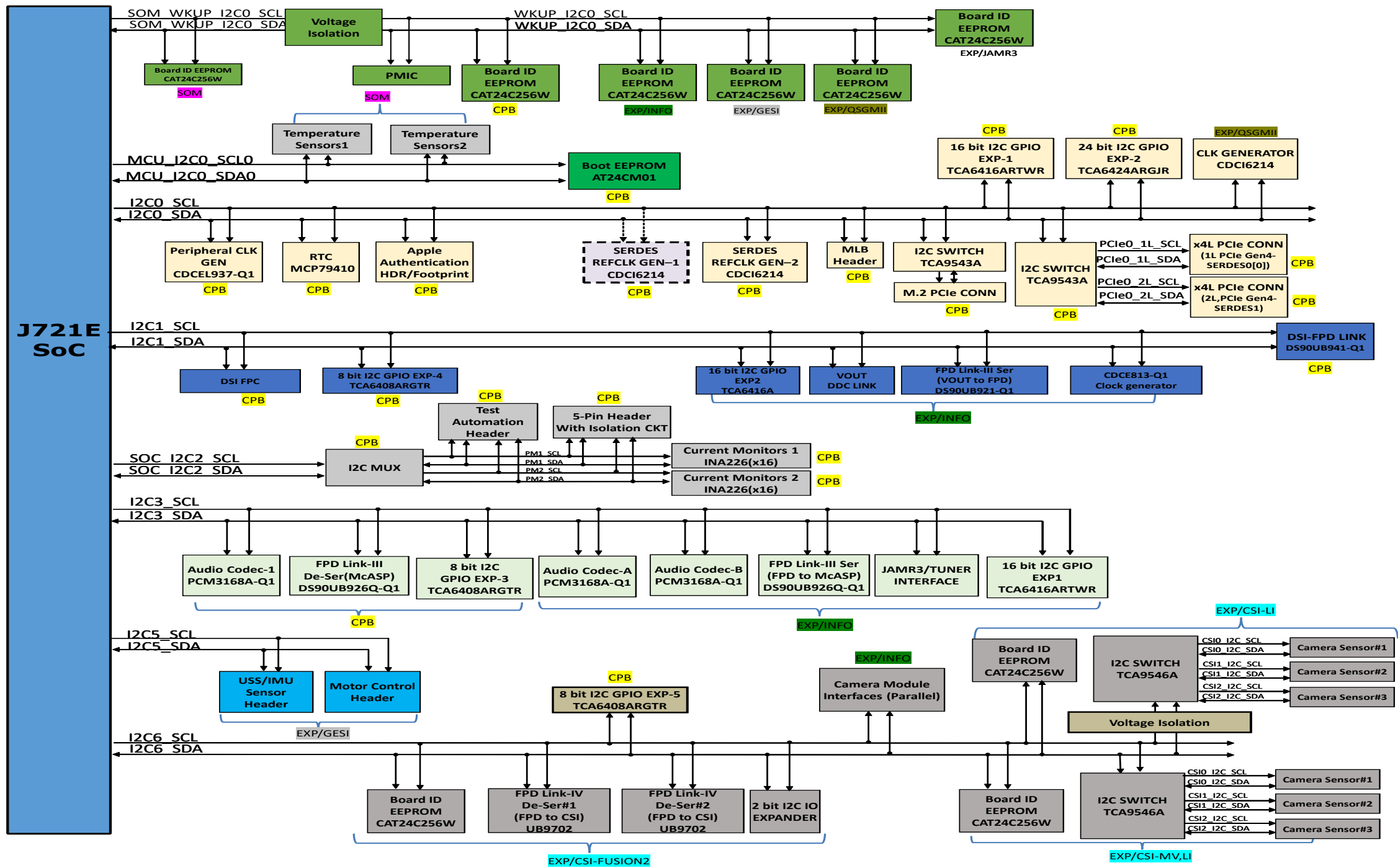
ALL New Designs should use
3-Phase Buck supplying VDD_CPU
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ALL New Designs should use
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(see SCH's last page)

2-Phase VDD_CPU PDNs
Not Recommended for New Designs

ALL New Designs should use
3-Phase Buck supplying VDD_CPU
(see SCH's last page)

SoM I2C TREE DIAGRAM



SoM I2C ADDRESS TABLE

J7ES EVM I2C Table				
Board	I2C Port	Device/Function	Part#	I2C Address
EVM/SoM	WKUP_I2C0	PMIC-A	TPS659413	0x48, 0x49, 0x4A & 0x4B
EVM/SoM	WKUP_I2C0	PMIC-B	TPS659411	0x4C, 0x4D, 0x4E & 0x4F
EVM/SoM	WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x50
EVM/CPB	WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x53
EXP/INFO	WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x52
EXP/GESI	WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x52
EXP/QSGMII	WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x54
EXP/JAMR3	WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x51
EVM/CPB	MCU_I2C0	BOOT EEPROM	AT24CM01	0x50,51
EVM/SoM	MCU_I2C0	Temperature Sensors 1	TMP100NA/3K	0x48
EVM/SoM	MCU_I2C0	Temperature Sensors 2	TMP100NA/3K	0x49
EVM/CPB	SoC_I2C0	Peripheral Clock Generator	CDCEL937-Q1	0x6D
EVM/CPB	SoC_I2C0	RTC Module	MCP79410	0x57,6F
EVM/CPB	SoC_I2C0	Apple Authentication Header/Footprint	2214BR-10G	0x10, 0x11
EVM/CPB	SoC_I2C0	SERDES REF CLK GEN - 2	CDCI6214	0x76
EVM/CPB	SoC_I2C0	16 bit I2C GPIO Expander-1	TCA6416ARTWR	0x20
EVM/CPB	SoC_I2C0	24 bit I2C GPIO Expander-2	TCA6424ARGJR	0x21
EVM/CPB	SoC_I2C0	I2C MUX for both x2LANE and x1LANE PCIe Interface	TCA9543APWR	0x70
EVM/CPB	SoC_I2C0	I2C MUX for M.2 PCIe Connector (2 L PCIe Gen4-SERDES2)	TCA9543APWR	0x71
EVM/CPB	SoC_I2C0	MLB Physical Interface Board	<connector interface>	
EXP/QSGMII	SoC_I2C0	Clock Generator on Quad ENET Board	CDCI6214	TBD
EVM/CPB	SoC_I2C1	8 bit I2C GPIO Expander-4	TCA6408ARGTR	0x20
EVM/CPB	SoC_I2C1	FPD Link-IV Serializer (DSI)	DS90UH981-Q1	0x0E
EXP/INFO	SoC_I2C1	Vout DDC link	CONNECTOR INTERFACE	
EXP/INFO	SoC_I2C1	I2C GPIO Expander(Video)	TCA6416ARTWR	0x21
EXP/INFO	SoC_I2C1	FPD Link-III Serializer (VOUT to FPD)	DS90UB921-Q1	0x1A
EXP/INFO	SoC_I2C1	CDCI (clock generator)	CDCE813-Q1	0x65
EVM/CPB	SoC_I2C1	DSI FPC	CONNECTOR INTERFACE	TBD
EVM/CPB	SoC_I2C2	Current Monitors 1(PM1_I2C)	INA226	0x40-0x4F
EVM/CPB	SoC_I2C2	Current Monitors 2(PM2_I2C)	INA226	0x40-0x4F
EVM/CPB	SoC_I2C2	Test Automation Header	<connector interface>	

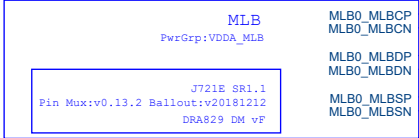
J7ES EVM I2C Table				
Board	I2C Port	Device/Function	Part#	I2C Address
EVM/CPB	SoC_I2C3	8 bit I2C GPIO Expander-3	TCA6408ARGTR	0x20
EVM/CPB	SoC_I2C3	Audio Codec - 1	PCM3168A-Q1	0x44
EVM/CPB	SoC_I2C3	FPD Link-III De-serializer (McASP)	DS90UB926Q-Q1	0x2C
EXP/INFO	SoC_I2C3	Audio Codec - A	PCM3168A-Q1	0x47
EXP/INFO	SoC_I2C3	Audio Codec - B	PCM3168A-Q1	0x46
EXP/INFO	SoC_I2C3	FPD Link-III De-Serializer (FPD to McASP)	DS90UB926Q-Q1	0x3B
EXP/INFO	SoC_I2C3	I2C GPIO Expander (Audio)	TCA6416ARTWR	0x21
EXP/GESI	SoC_I2C3	I2C GPIO Expander1	TCA6416ARTWR	0x21
EXP/GESI	SoC_I2C5	I2C GPIO Expander2	TCA6416ARTWR	0x21
EXP/GESI	SoC_I2C5	USS/IMU Sensor control Header		TBD
EXP/GESI	SoC_I2C5	Booster Pack Header		TBD
EVM/CPB	SoC_I2C6	8 bit I2C GPIO Expander-5	TCA6408ARGTR	0x20
EXP/CSI-FUSION2	SoC_I2C6	I2C IO Expander	PCA9536DGKR	0X41
EXP/CSI-FUSION2	SoC_I2C6	Board ID EEPROM (Fusion2 Serial Capture)	CAT24C256W	0x52
EXP/CSI-FUSION2	SoC_I2C6	FPD-Link IV De-Serializer #1 (FPD to CSI)	UB9702	TBD
EXP/CSI-FUSION2	SoC_I2C6	FPD-Link IV De-Serializer #2 (FPD to CSI)	UB9702	TBD
EXP/CSI-LI	SoC_I2C6	Board ID EEPROM (Leopard Imaging Adapter)	CAT24C256W	0x52
EXP/CSI-LI	SoC_I2C6	I2C MUX Camera sensors	TCA9543APWR	0x70
EXP/CSI-MV	SoC_I2C6	Board ID EEPROM (Machine Vision Application)	CAT24C256W	0x52
EXP/CSI-MV	SoC_I2C6	I2C MUX Camera sensors	TCA9543APWR	0x70
EXP/CSI-MV	SoC_I2C6	Camera Sensor #1, #2 & #3	IMX264LQR-C	TBD
EXP/INFO	SoC_I2C6	Camera Sensor, Parallel	<connector interface>	TBD

GPIO MAPPING TABLE

J721E SoM - GPIO Mapping Table						
Package Signal Name	GPIO	Net name	Input/Output	Default	State	Remarks
WKUP Domain						
WKUP_GPIO0_0	WKUP_GPIO0_0	MCU_MCAN0_EN	Output	BOOTMODE	Active High	MCU CAN0 Enable
WKUP_GPIO0_1	WKUP_GPIO0_1	BOOT_EEPROM_WP	Output	BOOTMODE	Active High	Boot EEPROM Write protect
WKUP_GPIO0_2	WKUP_GPIO0_2	MCU_CAN1_STB	Output	BOOTMODE	Active High	MCU CAN1 Standby
WKUP_GPIO0_3	WKUP_GPIO0_3	GPIO_MCU_RGMII1_RST#	Output	PU	Active low	MCU_RGMII1_Reset
WKUP_GPIO0_6	WKUP_GPIO0_6	WKUP_GPIO0_6	I/O	Test Point	NA	Terminated with Test point
WKUP_GPIO0_7	WKUP_GPIO0_7	SYS_IRQz	Input	PU	Active low	Push-button Interrupt, User Defined/Wake S2R ('0>1' - interrupt pending, '1' - normal operation)
WKUP_GPIO0_8	WKUP_GPIO0_8	OSPI/HYPER_MUX_SEL	Output	DIP_SEL	NA	Flash Memory Selection ('0' - OSPI0, '1' - Hyperflash + HyperRam)
WKUP_GPIO0_9	WKUP_GPIO0_9	PMIC_MCU_INT#	Input	PU	Active low	Interrupt from PMIC
WKUP_GPIO0_17	WKUP_GPIO0_17	MCU_OSPI0_ECC_FAIL	Output	NA	Active High	OSPI_ECC_FAIL (Mux option w/ HYPERBUS_CKn), MCU_OSPI0_ECC_FAIL is DNI resistor option.
MCU_SPI0_CLK	WKUP_GPIO0_52	WKUP_GPIO0_52	I/O	BOOTMODE	NA	Terminated with Test point
MCU_SPI0_CS0	WKUP_GPIO0_55	MCU_RGMII1_INT#	Input	PU	Active Low	MCU Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
MCU_SPI0_D0	WKUP_GPIO0_53	SYS_MCU_PWRDN	Output	PD	Active low	System Power Down ('0' - normal operation, '1' - system power down)
MCU_SPI0_D1	WKUP_GPIO0_54	MCU_CAN0_STBz	Output	PD	Active low	MCU CAN0 Standby
Main Domain						
EXTINTN	GPIO0_0	SOC_EXTINTN	Input	PU	Active low	Push-button Interrupt, User Defined
PRG0_PRU0_GPO5	GPIO0_48	IMU_GPIO1	I/O	NA	NA	Used as GPIO1 for IMU Sensor
PRG0_PRU0_GPO17	GPIO0_60	CAN_STB	Output	PD	Active High	Standby signals for CAN Transceivers
PRG0_PRU0_GPO18	GPIO0_61	GPIO0_61	I/O	NA	NA	Routed to INFO/GES1 expansion connector.
PRG0_PRU0_GPO19	GPIO0_62	GPIO_PRG1_RGMII_RST	Output	PU	Active low	Used as a reset signal for PRG1 Ethernet PHY Chips
PRG0_PRU1_GPO5	GPIO0_68	GPIO_LIN_EN	Output	PD	Active High	LIN transceiver enable
RGMII5_RD0	GPIO0_96	RMII8_PHY_RESET	Output	PU	Active low	Used as a reset signal for RMII8 PHY Chip
RGMII6_TX_CTL	GPIO0_97	C_MCASP10_ACLKR	Input	PU	Active low	CSI2 IO expander Interrupt.('0' -
RGMII6_RX_CTL	GPIO0_98	C_MCASP10_AFSR	NA	PU	Active low	I2C0 IO expander interrupt. ('0' - interrupt pending, '1' - no interrupt)(I2C0_IOEXP_INT#) Note: GPIO only available from Trace/GPMC Mux
RGMII6_RXC	GPIO0_104	RMII8_PHY_INTn	Input	PU	Active Low	RMII8 PHY Interrupt
RGMII6_RD3	GPIO0_105	IMU_GPIO0	I/O	NA	NA	Used as GPIO0 for IMU Sensor
SPI1_CS1	GPIO0_117	SEL_SDIO_3V3_1V8n	Output	PU	Active low	SW controls & transition Sd card to high speed 1.8V signaling if card type supports
UART0_CTSN	GPIO0_123	BP_GPIO3	I/O	NA	NA	Boosterpack_GPIO3
UART0_RTSN	GPIO0_124	BP_GPIO4	I/O	NA	NA	Boosterpack_GPIO4
UART1_CTSN	GPIO0_127	GPIO0_127/EQEPO_S/MLB0_MLBCLK	Output	PU	Active High	CP Board - MCAN2_STB; GES1 - Boosterpack_GPIO2
UART1_RTSN	GPIO1_0	GPIO1_0/EQEPO_I/MLB0_MLBDAT	Output	PD	NA	CP Board - PM I2C Mux seletion. ('0' - SOC_I2C2_SCL/SDA -> PM1_SCL/SDA, '1' -
MCAN1_RX	GPIO1_3	USBC_DIR	Input	PU	NA	USB Type C Cable Orientation. Type-C plug
ECAP0_IN_APWM_OUT	GPIO1_11	GPIO1_11/MAIN_I3C0_SDAPULLEN	Input	PU	Active High	Display IO expander Interrupt. ('0' - interrupt pending, '1' - no interrupt) (IOEXP4_INT#)
EXT_REFCLK1	GPIO1_12	GPIO1_12/MLB0_REFCLK	Input	PD	NA	CP Board Audio De-serializer UB926_GPIO1 (Tuner Unused GPIO)
TIMER_IO1	GPIO1_14	DSI_UB981_INTB	Input	PU	Active low	DSI FPD Link Serializer/Panel Interrupt.
MMC1_SDWP	GPIO1_22	ENET_EXP_INTB	Input	PU	Active low	Ethernet Expansion Interrupt. ('0' - interrupt pending, '1' - no interrupt)
MMC2_DAT3	GPIO1_23	GPIO1_23/UART9_RXD	Input	PU	Active low	Interrupt function. ('0' - interrupt pending, '1' - no interrupt)
MMC2_DAT2	GPIO1_24	GPIO1_24/UART9_TXD	Input	PU	Active low	Interrupt function. ('0' - interrupt pending, '1' - no interrupt)
MMC2_DAT1	GPIO1_25	CSI2_EXP_A_GPIO2	I/O	NA	NA	CSI2 Expansion Board Specific.
MMC2_DAT0	GPIO1_26	CSI2_EXP_A_GPIO4	I/O	NA	NA	CSI2 Expansion Board Specific.
I3C0_SCL	GPIO1_5	H_I3C0_SCL	I/O	NA	NA	CP Board Audio De-serializer UB926_GPIO2
I3C0_SDA	GPIO1_6	H_I3C0_SDA	I/O	NA	NA	CP Board Audio De-serializer UB926_GPIO3
PRG1_PRU0_GPO10	GPIO0_11	PRG1_UART0_RTS#	I/O	PD	NA	INFO Expansion Audio De-serializer UB926_GPIO1 (Tuner Unused GPIO)
PRG0_PRU0_GPO2	GPIO0_45	PRG0_RGMII1_RD2	I/O	NA	NA	INFO Expansion Audio De-serializer UB926_GPIO2
PRG0_PRU0_GPO3	GPIO0_46	PRG0_RGMII1_RD3	I/O	NA	NA	INFO Expansion Audio De-serializer UB926_GPIO3
PRG0_PRU1_GPO2	GPIO0_65	PRG0_RGMII2_RD2	I/O	NA	NA	INFO Expansion JAMR3_GPIO0 (Function to be determined)
PRG0_PRU1_GPO3	GPIO0_66	PRG0_RGMII2_RD3	I/O	NA	NA	INFO Expansion JAMR3_GPIO1 (Function to be determined)
PRG0_PRU1_GPO13	GPIO0_76	PRG0_RGMII2_TD2	I/O	NA	NA	INFO Expansion JAMR3_GPIO2 (Function to be determined)
PRG0_PRU1_GPO16	GPIO0_79	GPIO0_79/PRG0_RGMII2_TXC	Input	NA	NA	INFO Expansion FPD Link3 Display Serializer interrrupt (CON_UB921_INTB)

MLB

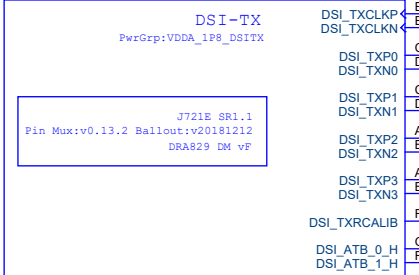
U9L



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DSI

U9E

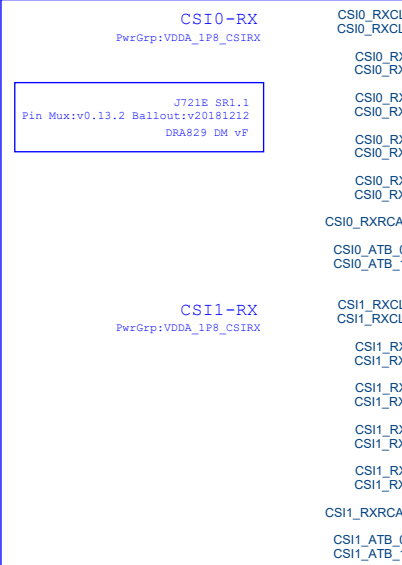


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Note: ATB pins to be left unconnected

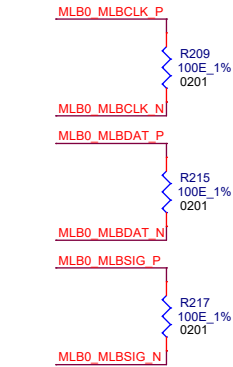
CSI Interface

U9F



J721E_181212

Note: ATB pins to be left unconnected



Note: ATB pins to be left unconnected



Project :

J7 EVM



Title
MLB,CSI&DSI_INTERFACE

Size
C PROC078 001 J721EXSOMG01EVM

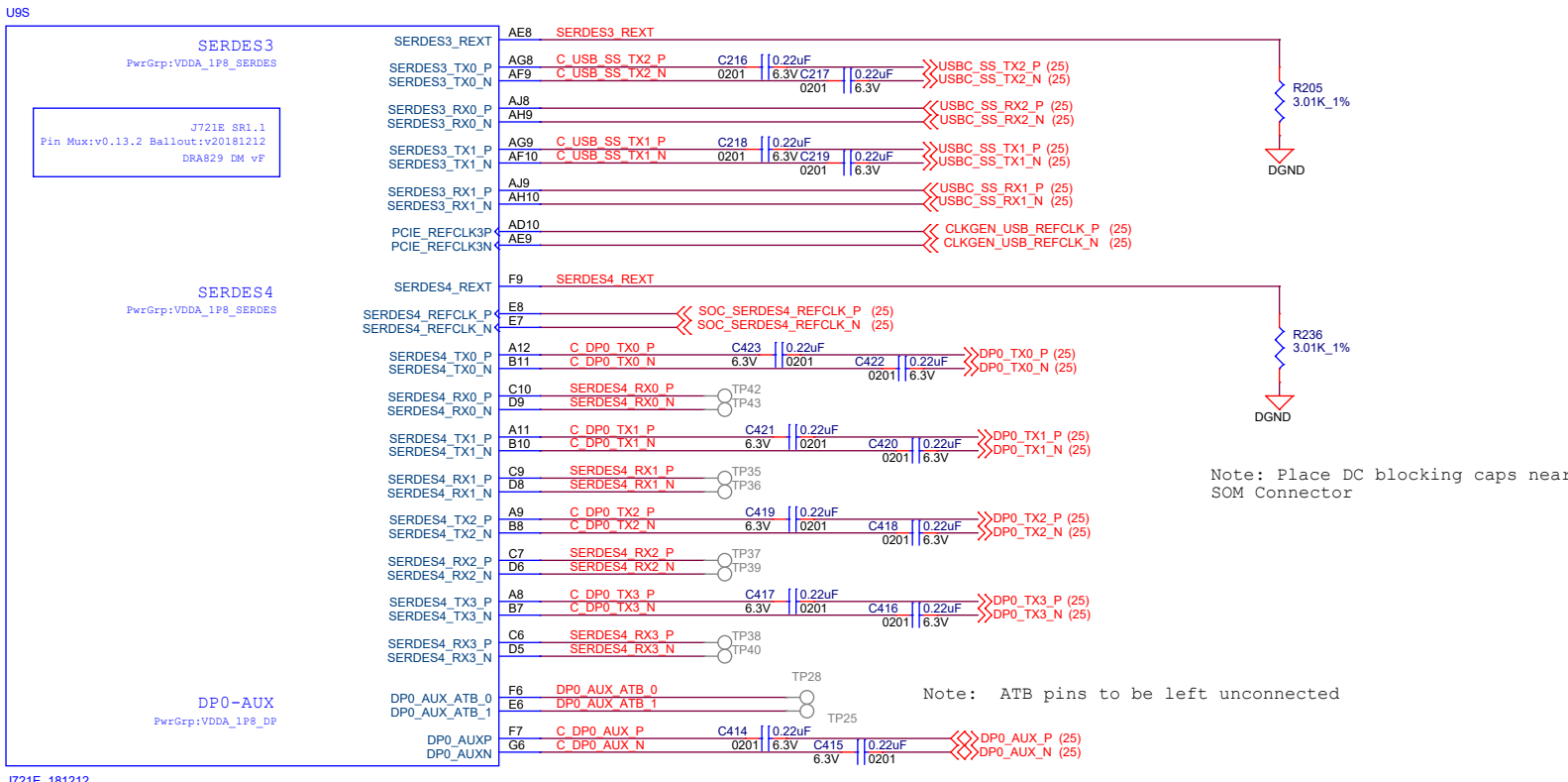
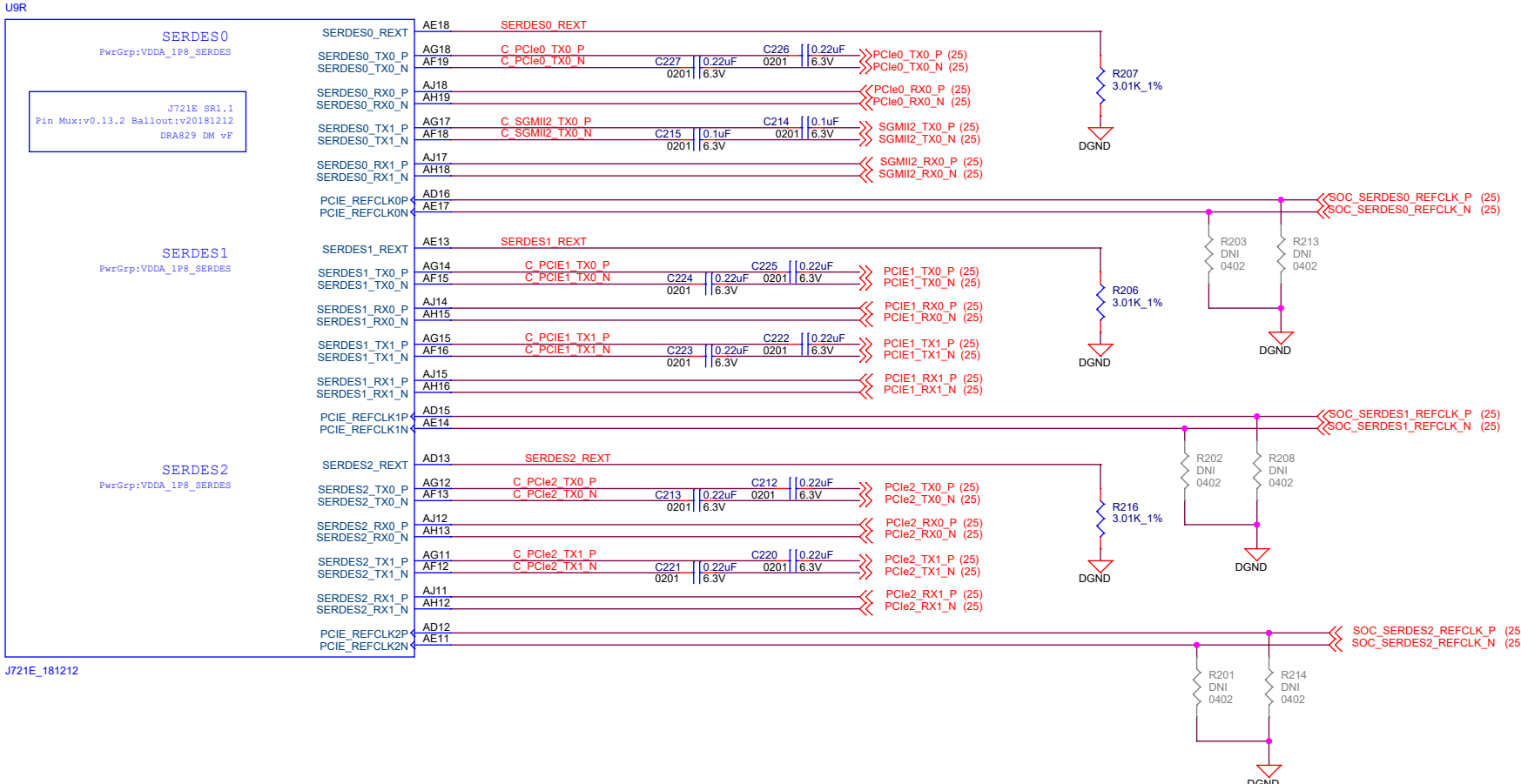
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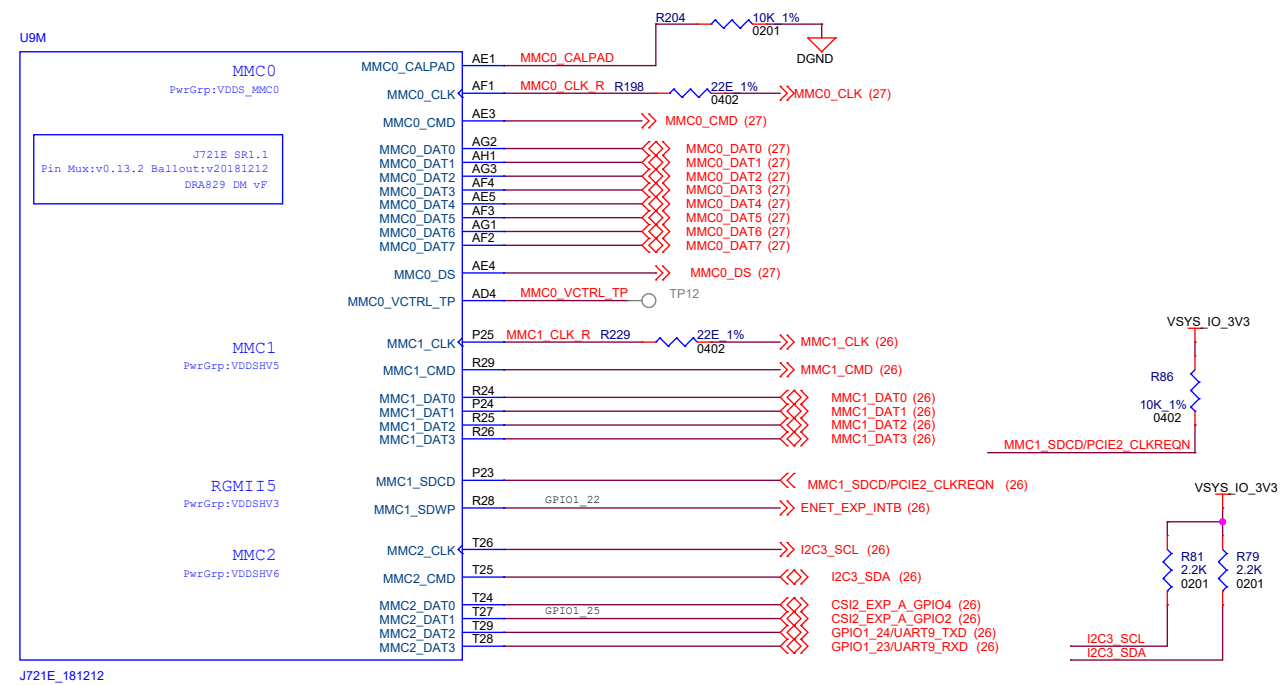
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SERDES



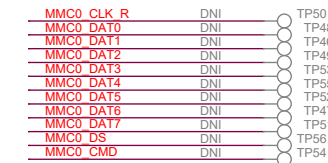
MMC Interface



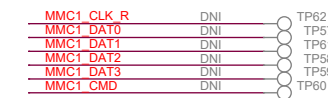
Via Probe Test Points

Place Near SOC

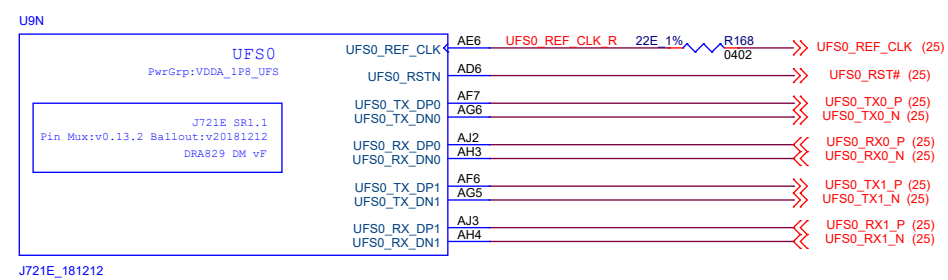
MMC0 :

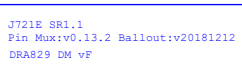


MMC1:

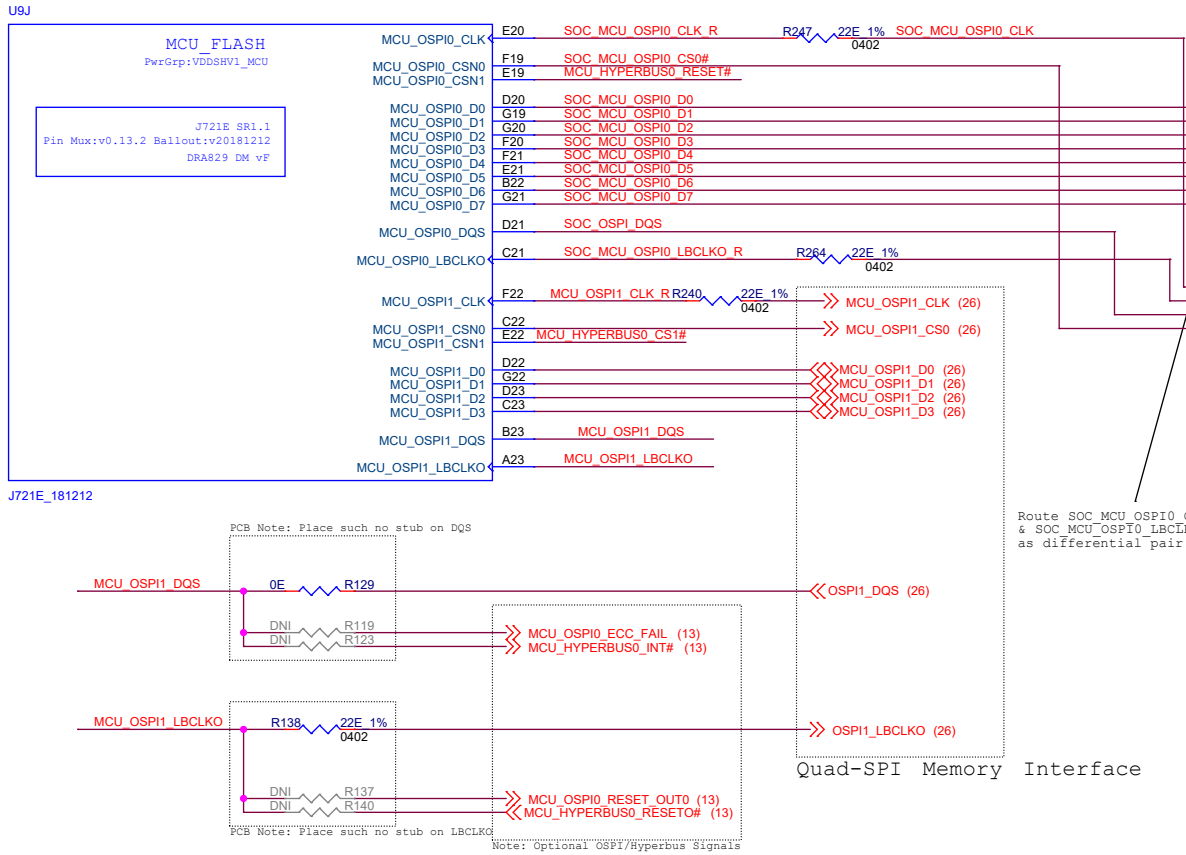


UFS Interface



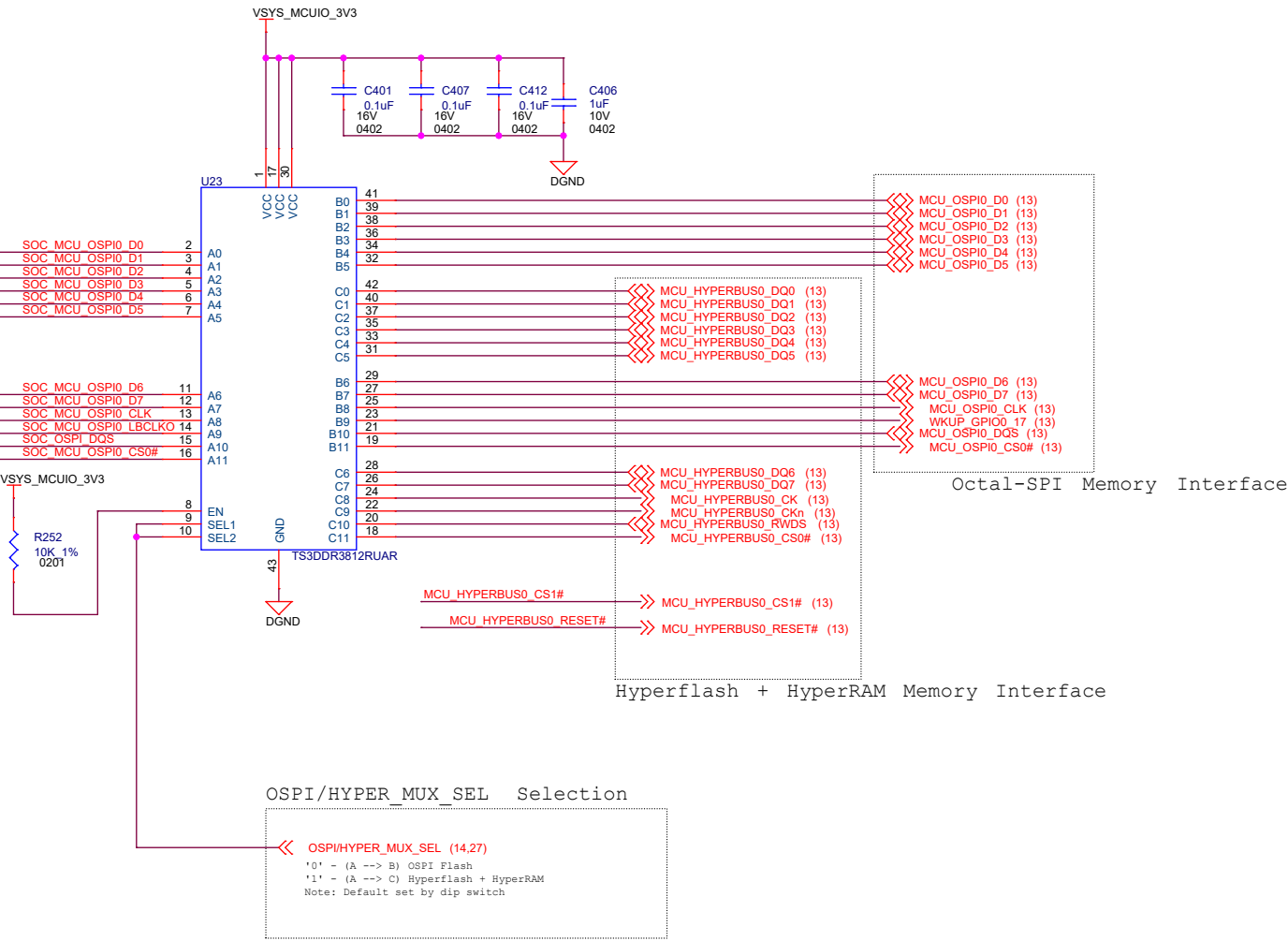


MCU FLASH

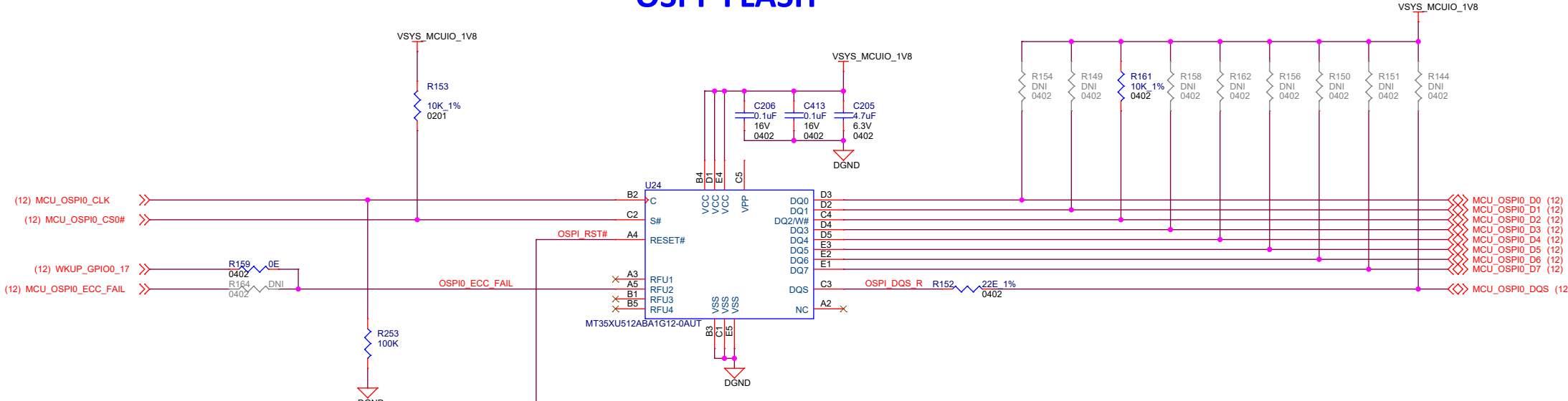


EVM development & evaluation test circuitry
(TI EVM Only)

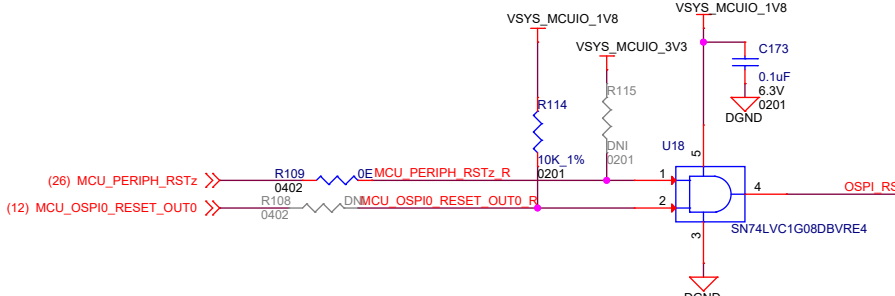
2:1 Mux for OSPI/HYBERBUS



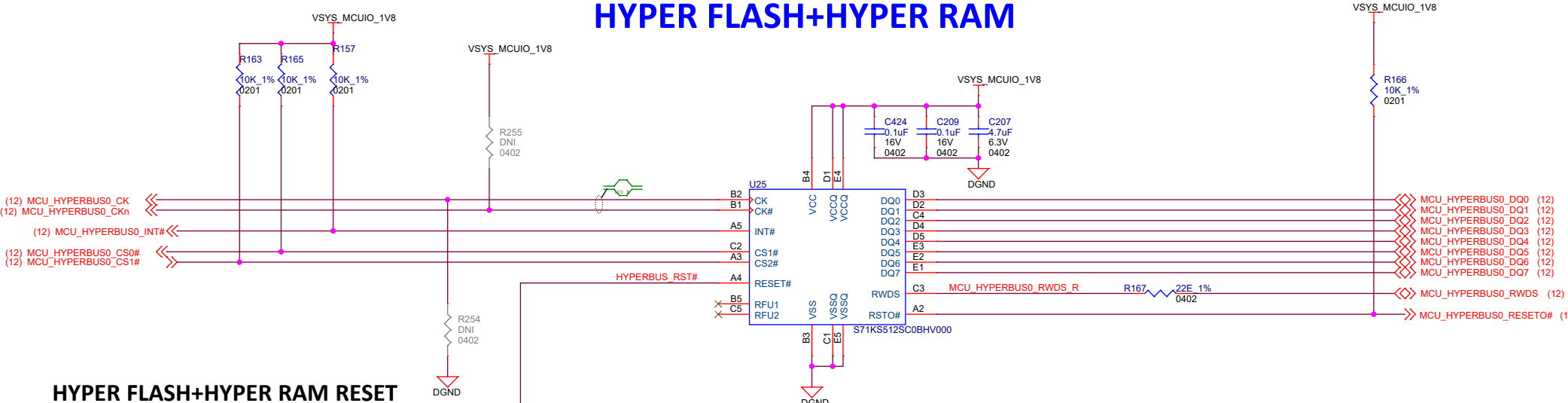
OSPI FLASH



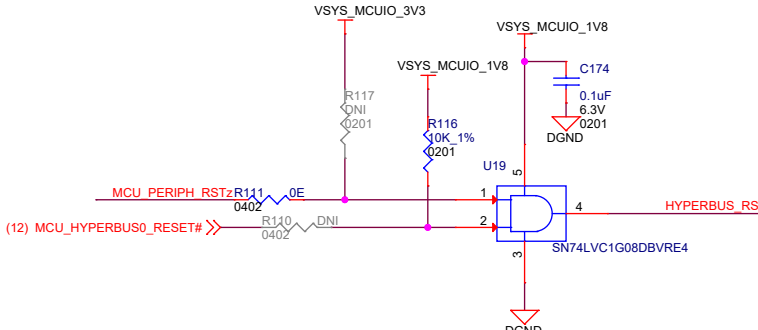
OSPI FLASH RESET



HYPER FLASH+HYPER RAM



HYPER FLASH+HYPER RAM RESET



Project

J7 EVI



Title
OSPIFLASH/HYPERFLAS/HYPERRAI

Size	PROC078 001 J721EXSOMG01EVM
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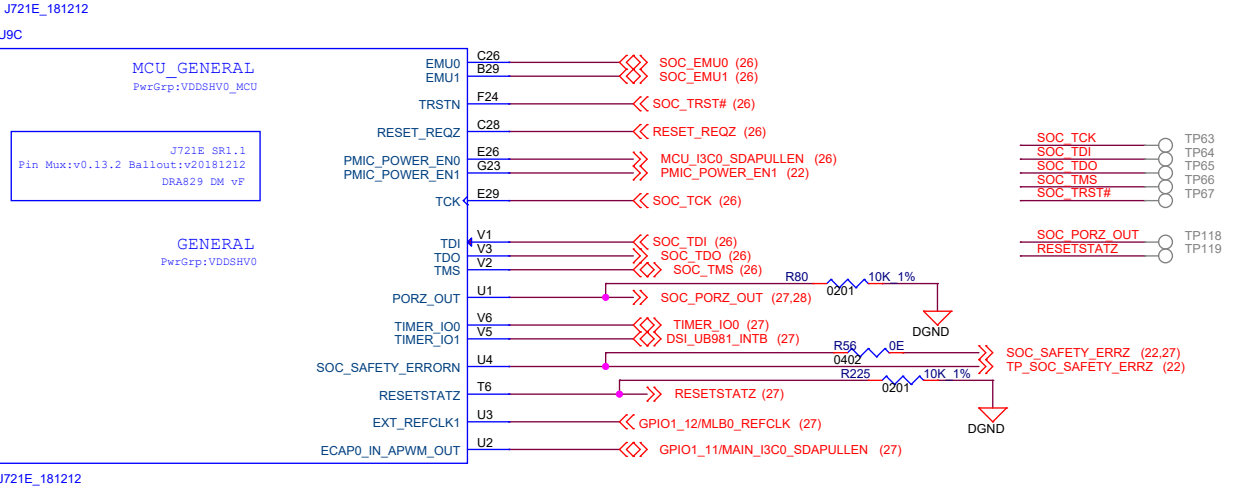
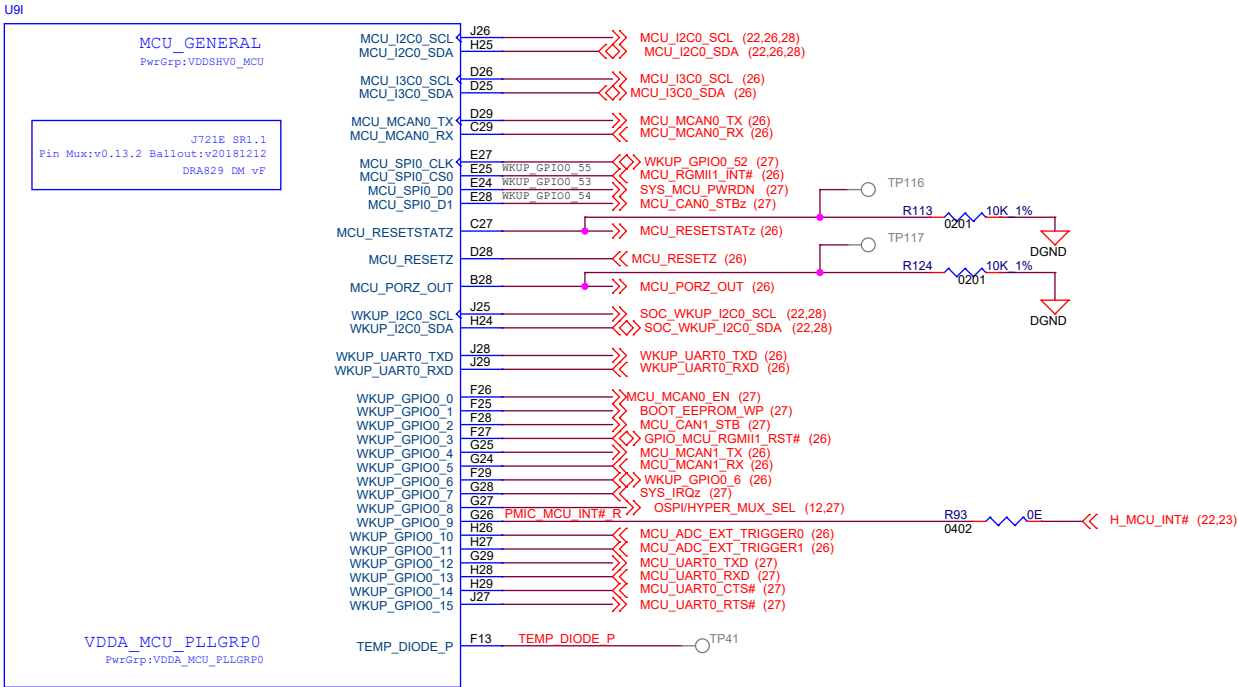
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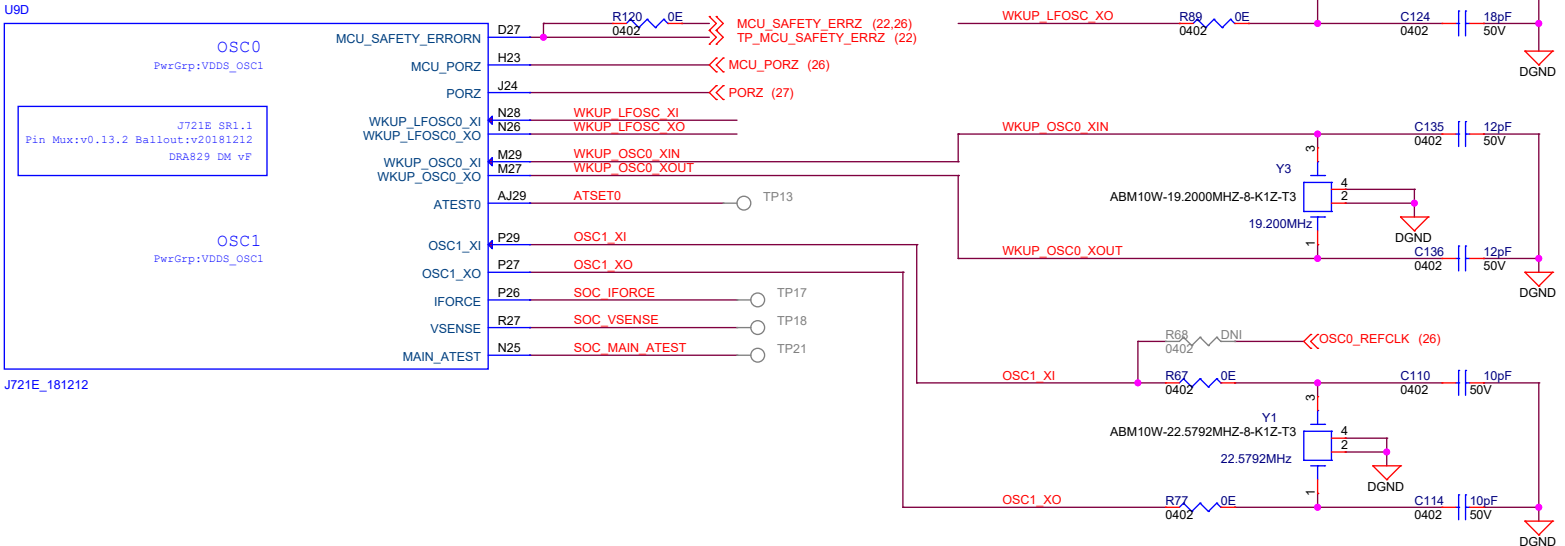
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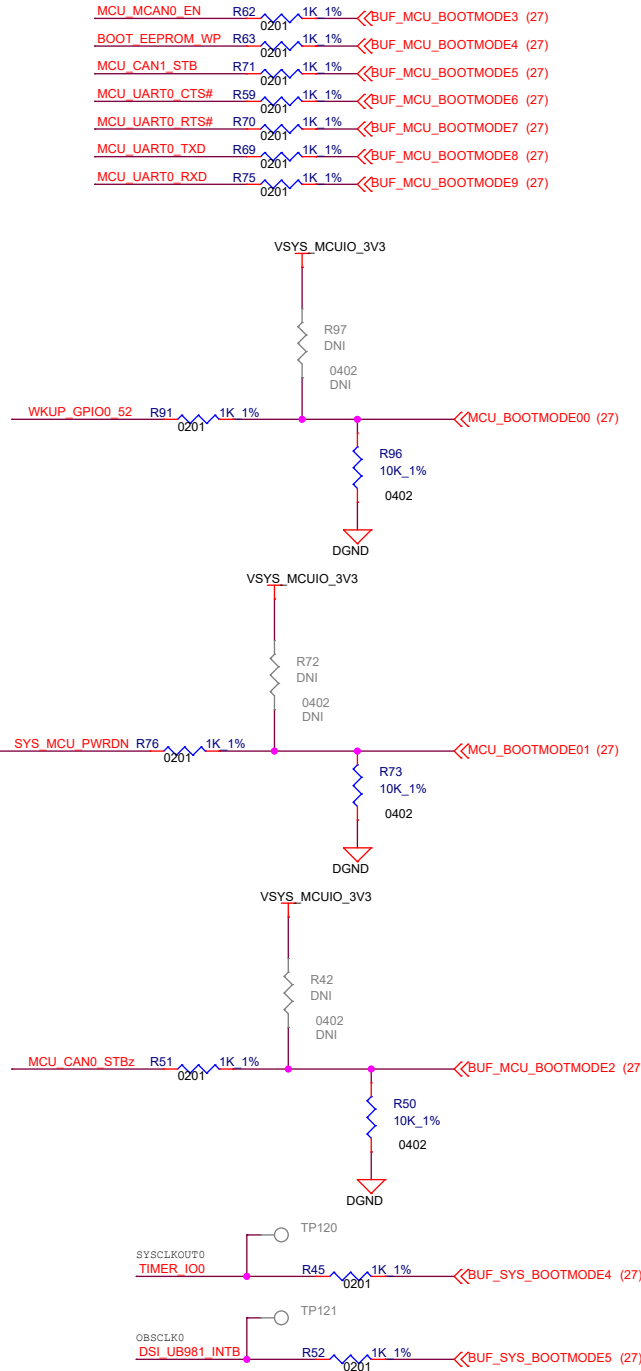
MCU & MAIN GENERAL IO, OSC CLKS



OSC

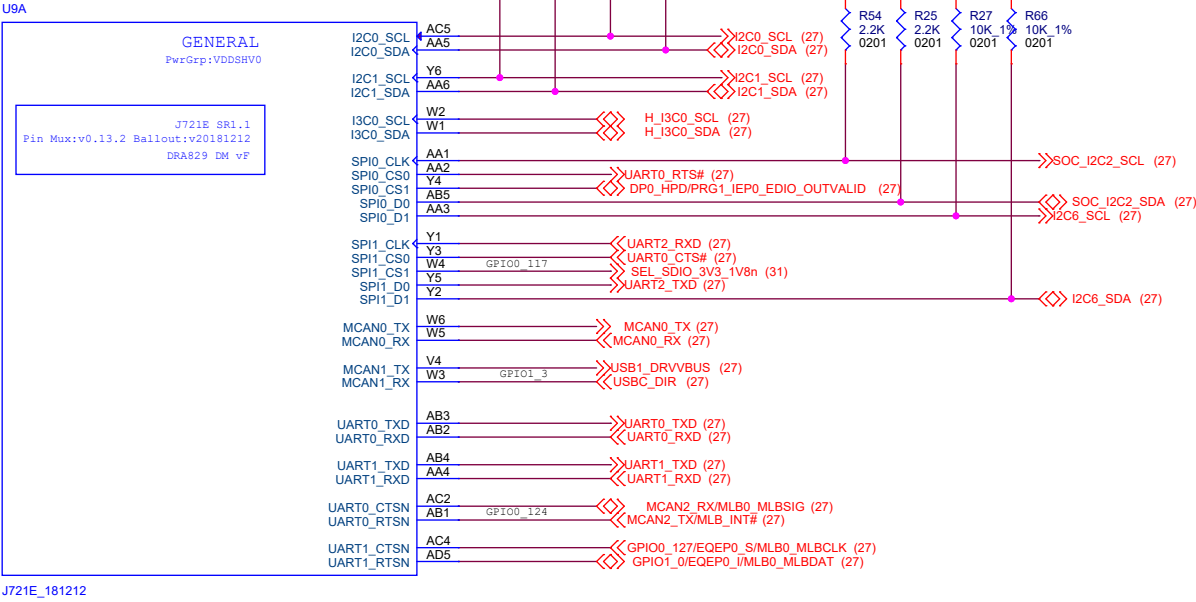


CLKS

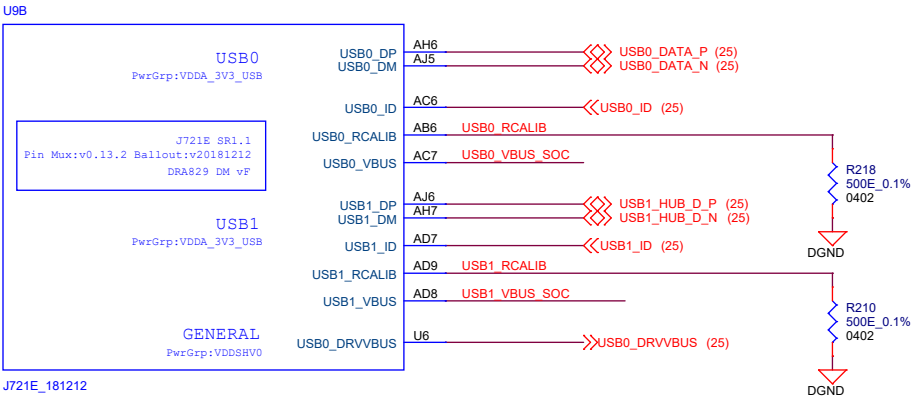


Project : J7 EVM		Title SOC_GENERAL&MCU_GENERAL	
Size C		PROC078 001 J721EXSOMG01EVM	Rev E8A
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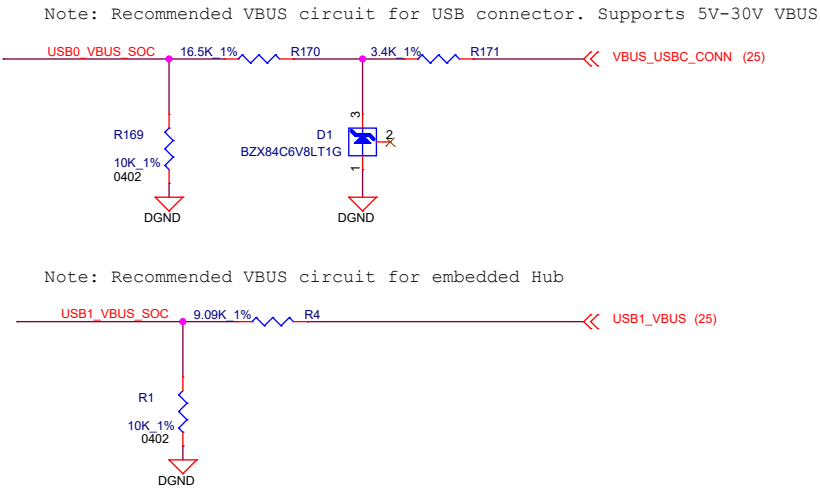
GENERAL



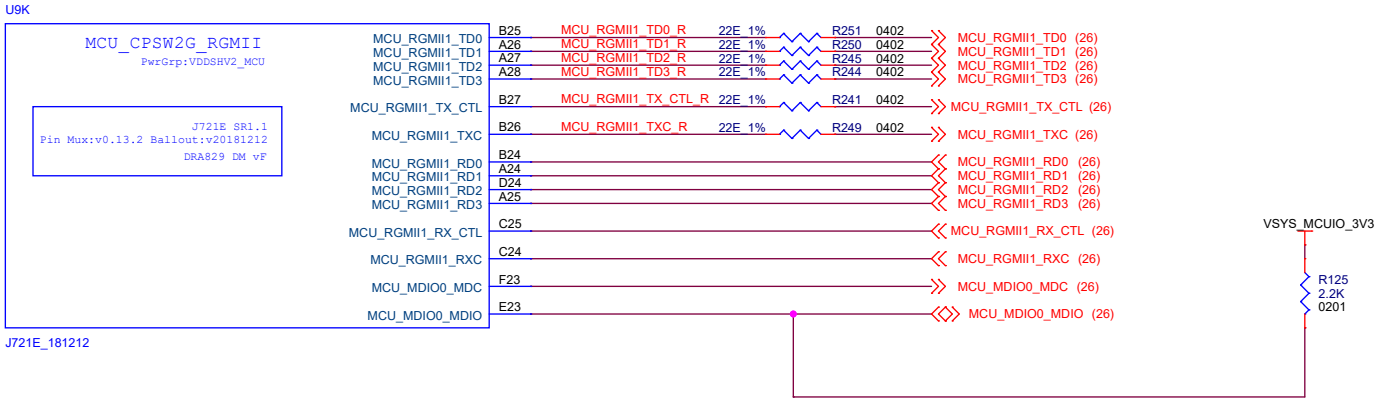
USB



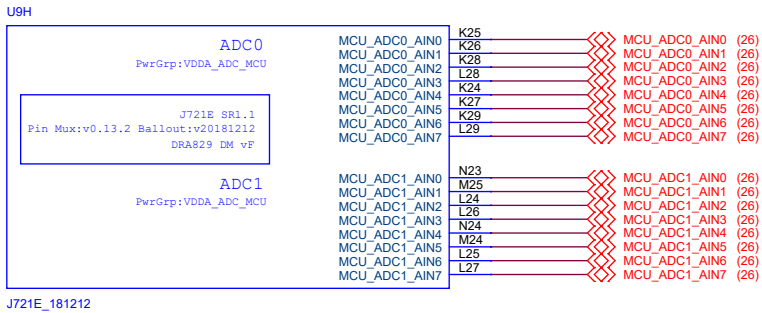
USB VBUS Resistor divider circuit



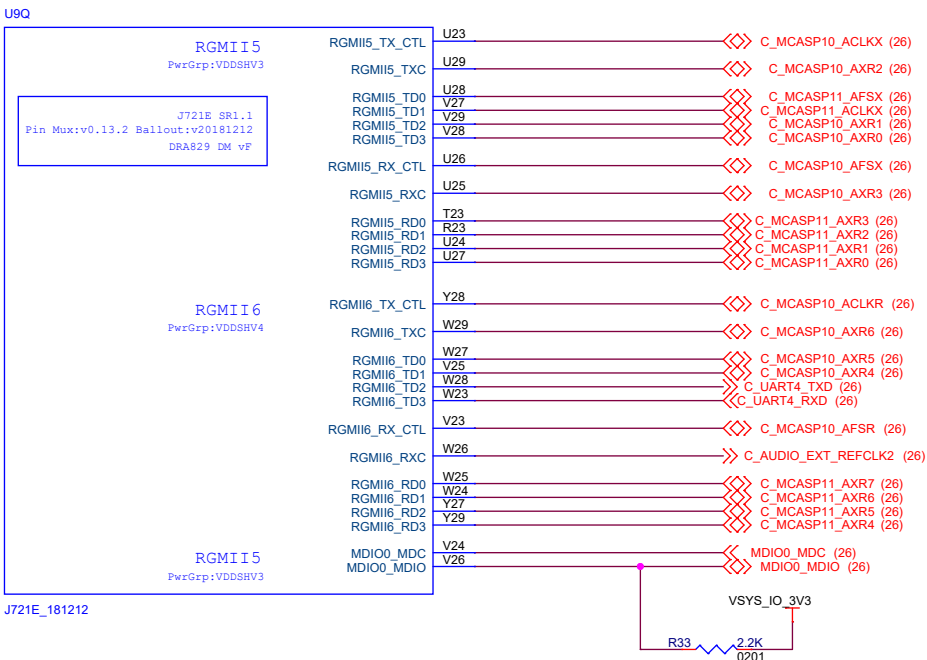
MCU_RGMII



MCU ADCs



MAIN RGMII



Project :

J7 EVM



Title
MCU_RGMII&MCU_ADC

Size
C PROC078 001 J721EXSOMG01EVM

Rev

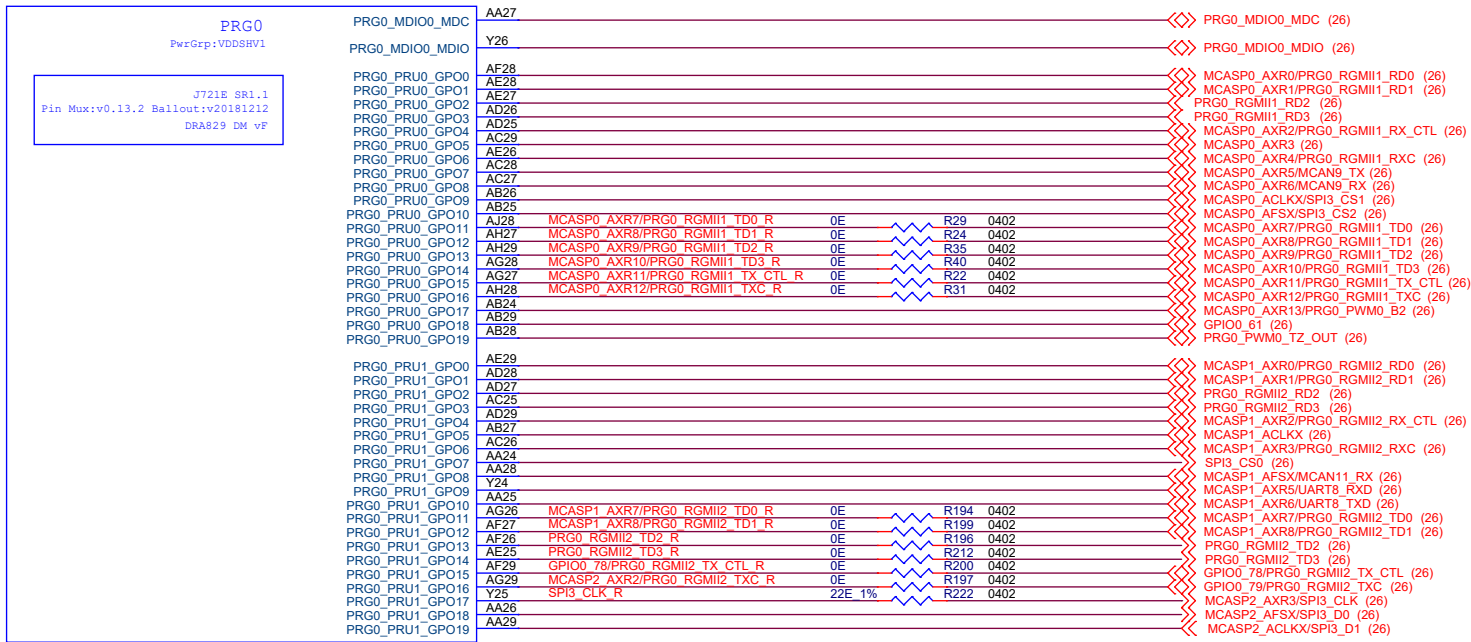
E8A

Date: Thursday, February 18, 2021

Sheet 16 of 34

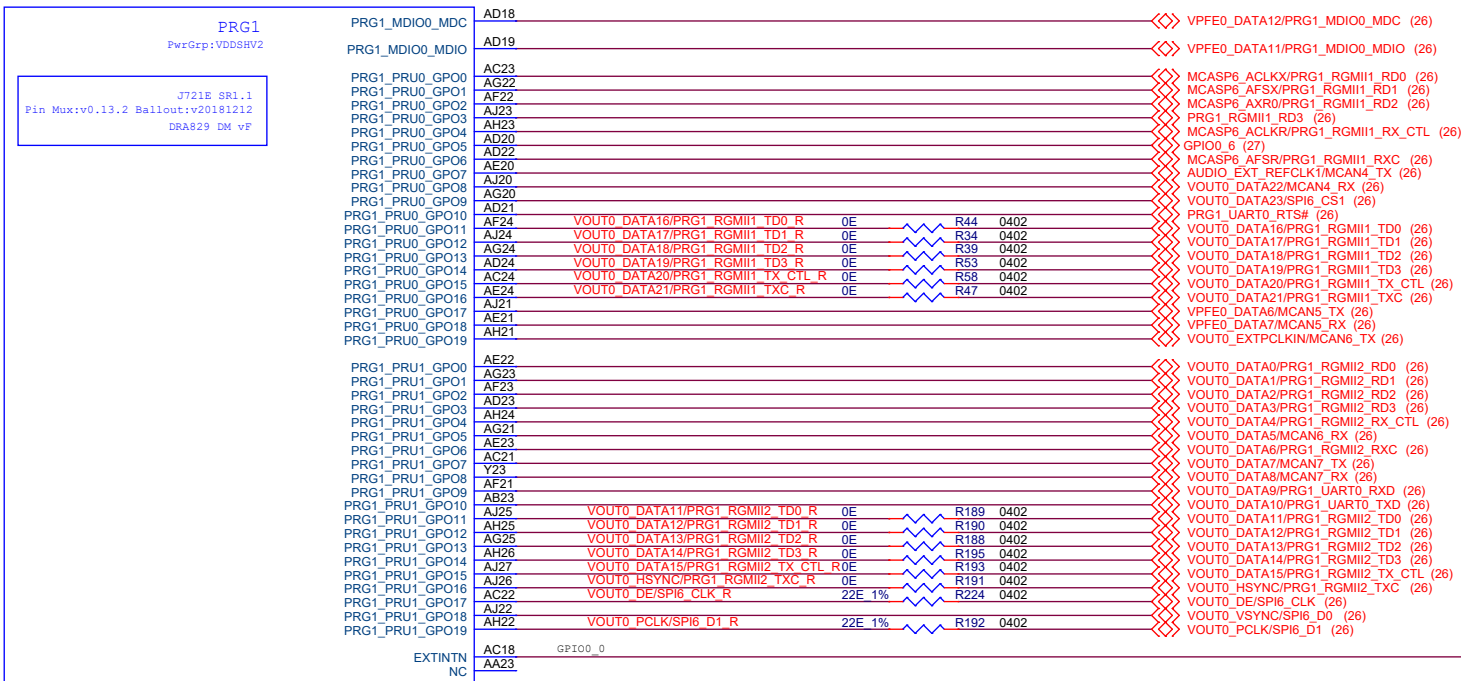
PRG0 & PRG1

U90

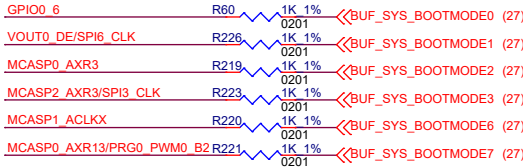


J721E_181212

U9P



J721E_181212



Project :

J7 EVM



Title

PRG

Size

PROC078 001 J721EXSOMG01EVM

Rev

E8A

Date:

Thursday, February 18, 2021

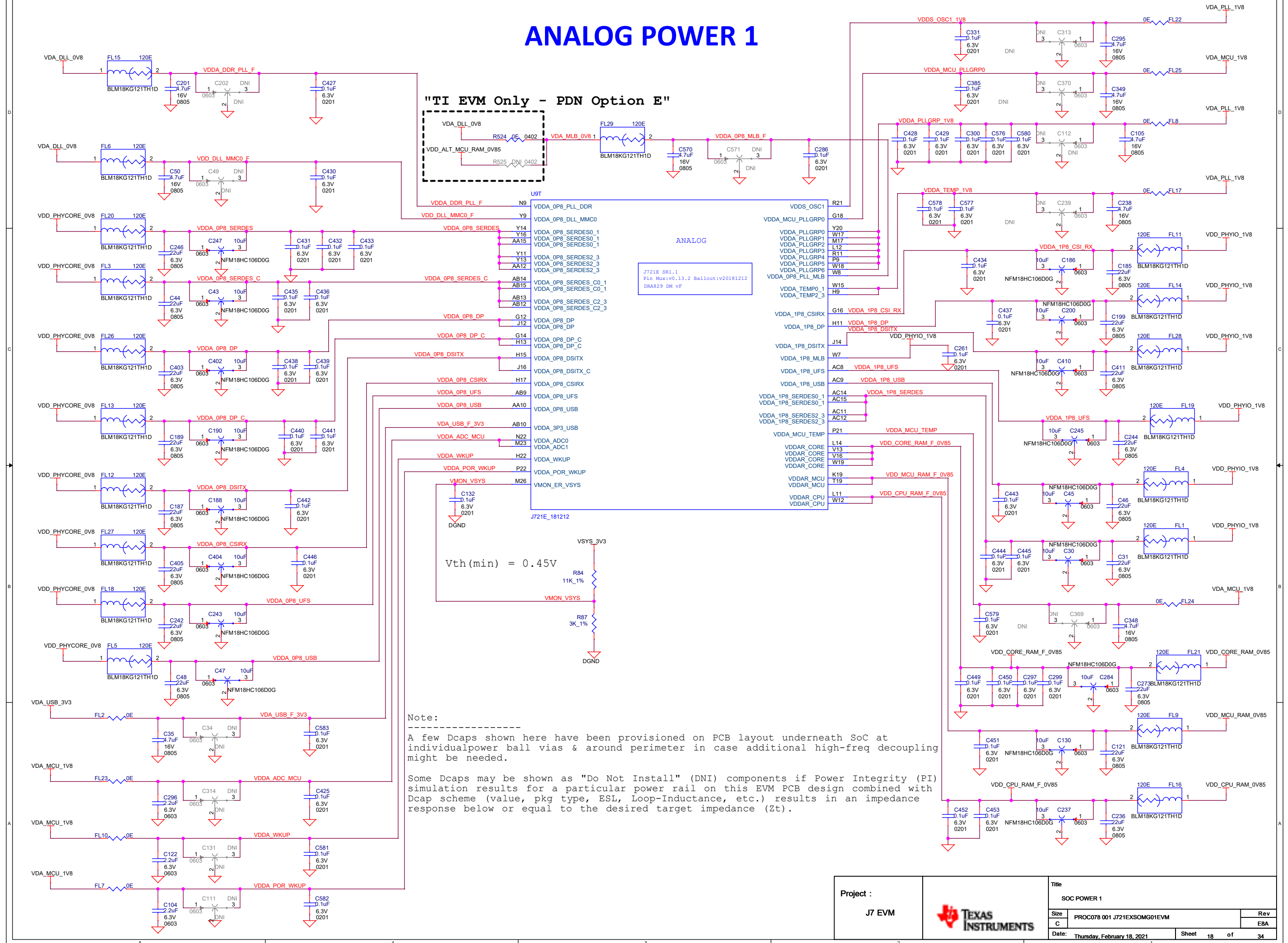
Sheet

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of

34

ANALOG POWER 1

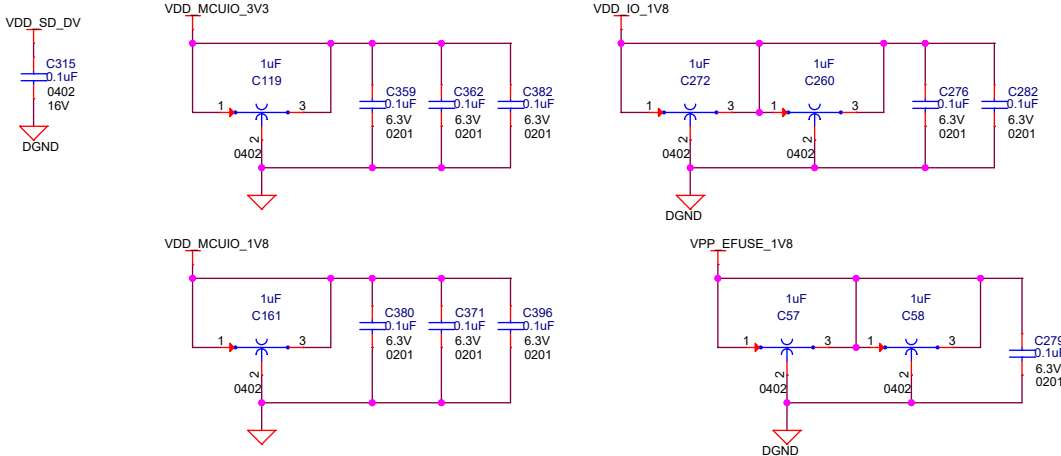
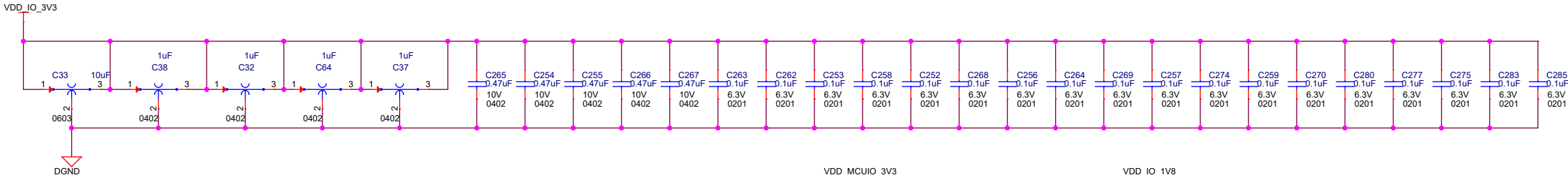
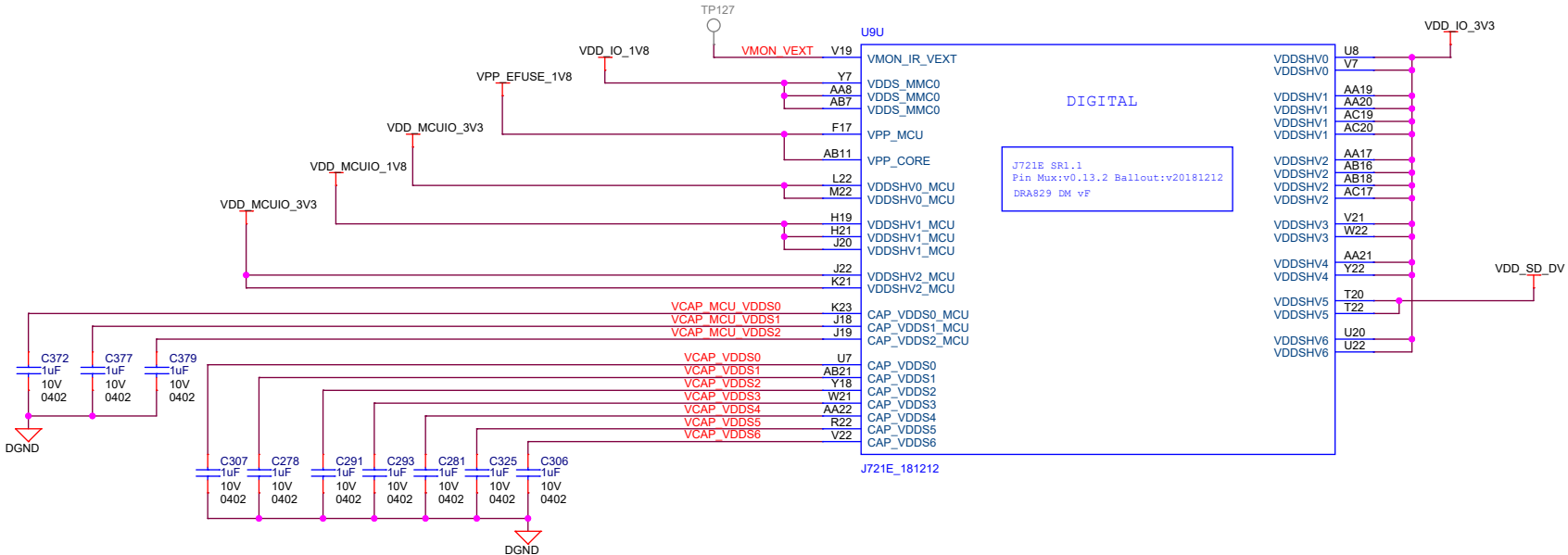


Note:

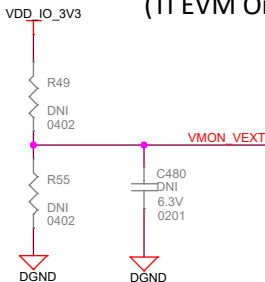
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

DIGITAL POWER 2



EVM development & evaluation test circuitry
(TI EVM Only)



Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Z_t).

Project :

J7 EVM



Title
SOC POWER

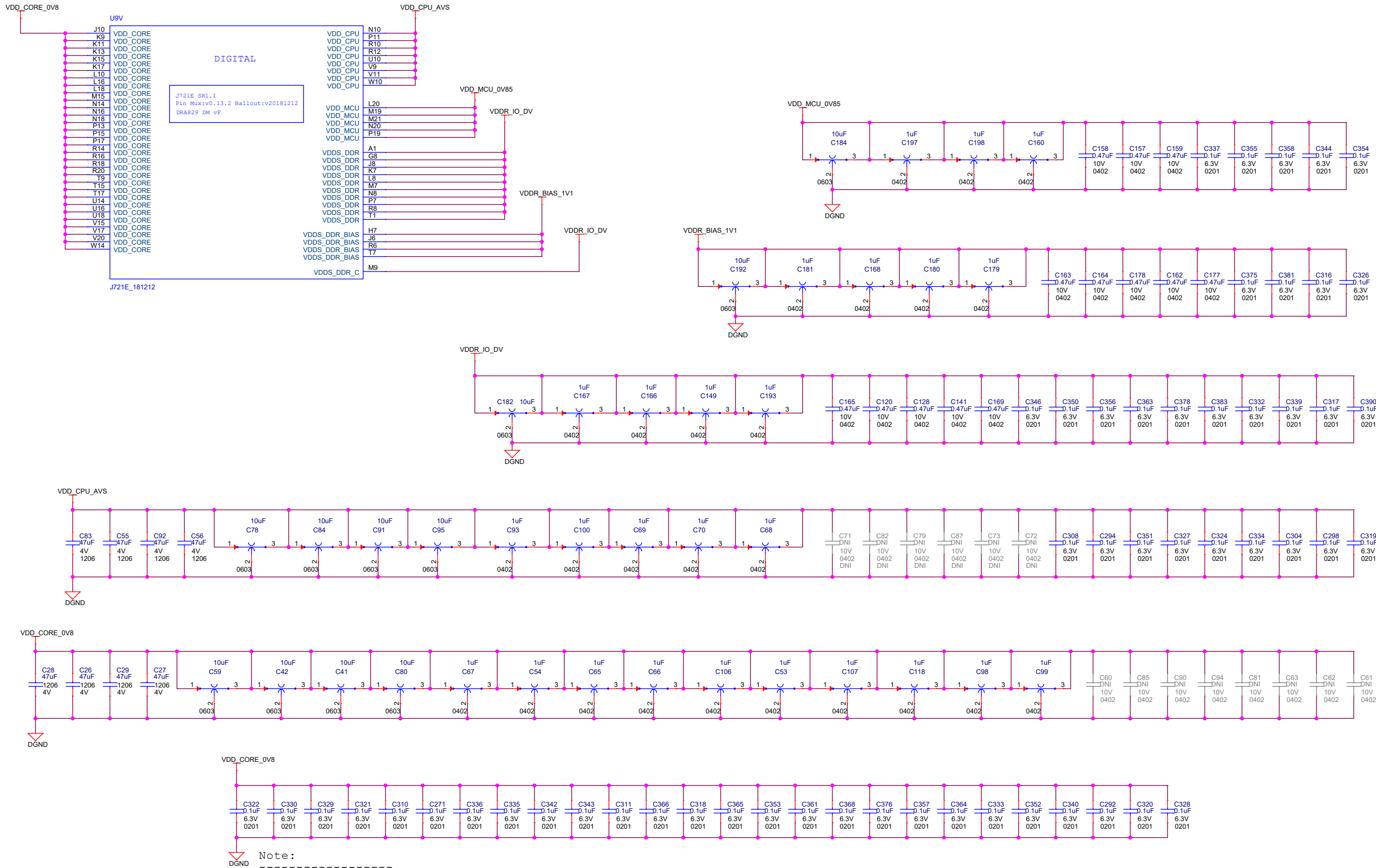
Size	PROC078 001 J721EXSOMG01EVM
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Date: Thursday, February 18, 2021

Rev
E8A

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DIGITAL POWER 3

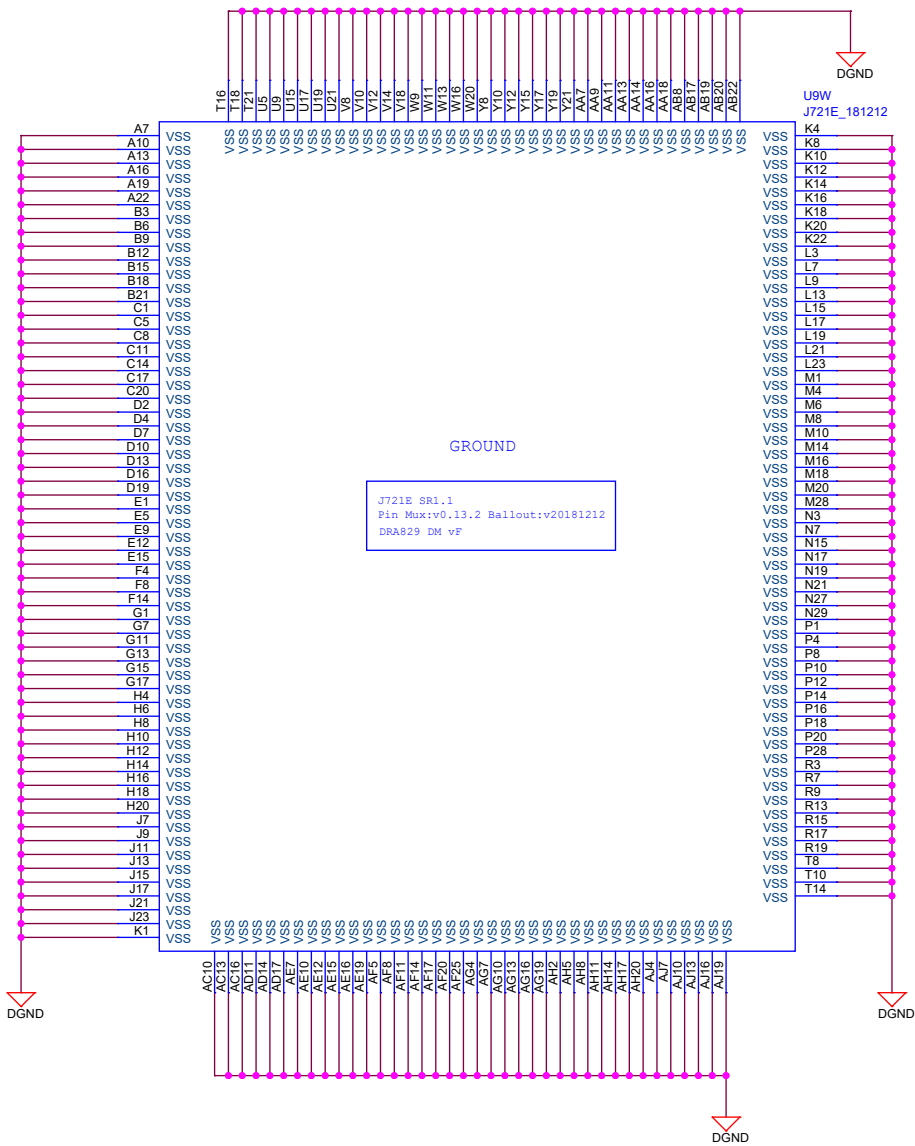


Note:
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Z_t).

Project : J7 EVM		Title SOC POWER 3	
Size C		PROC078 001 J721EXSOMG01EVM	Rev E8A
Date: Thursday, February 18, 2021		Sheet 20 of 34	

SOC GROUND

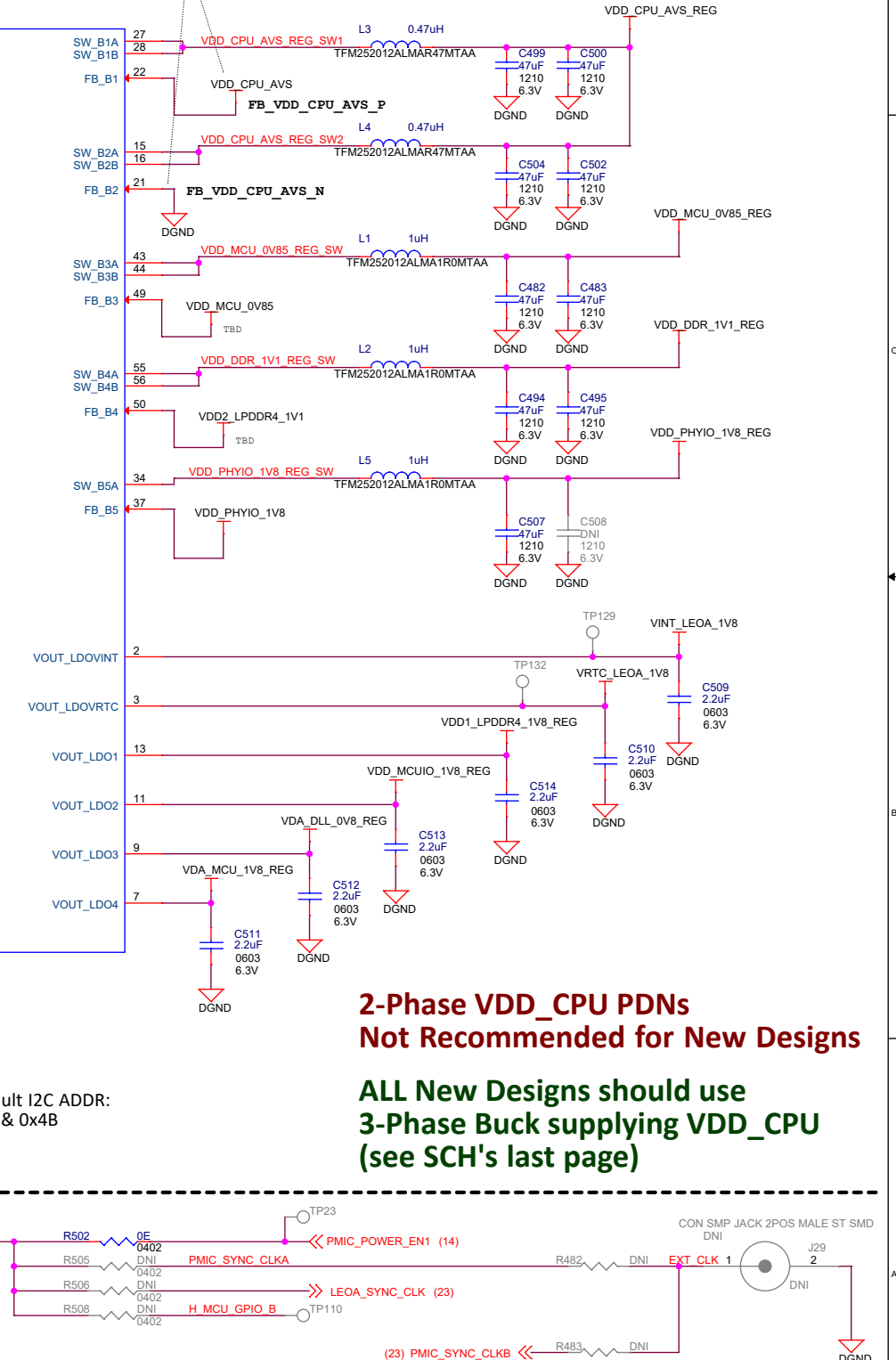
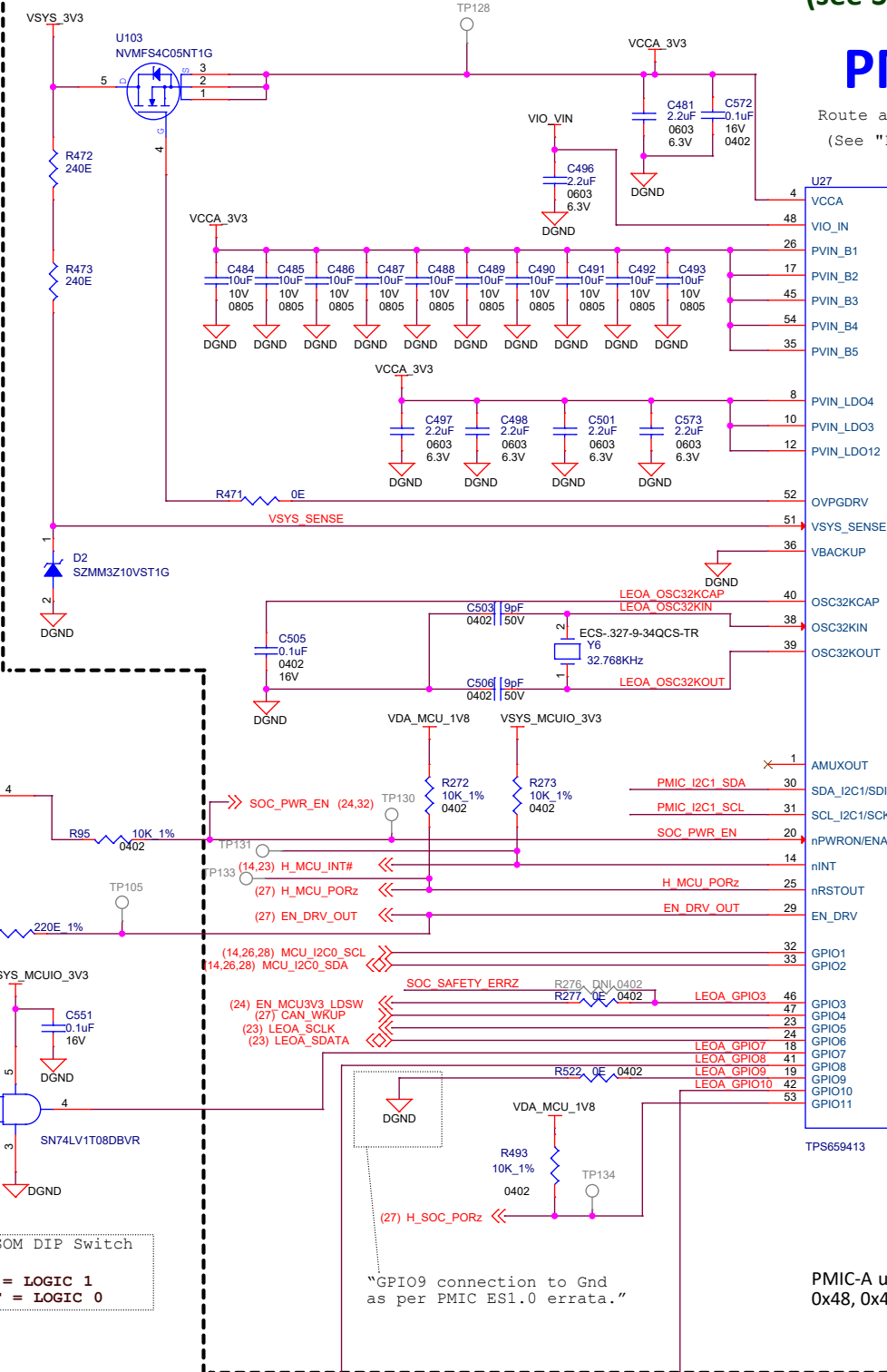


"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:

1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

Route as Pseudo differential pair trace
(See "PCB Notes")




**ALL New Designs should use
3-Phase Buck supplying VDD_CPU
(see SCH's last page)**

PMIC-A uses default I2C ADDR:
0x48, 0x49, 0x4A & 0x4B

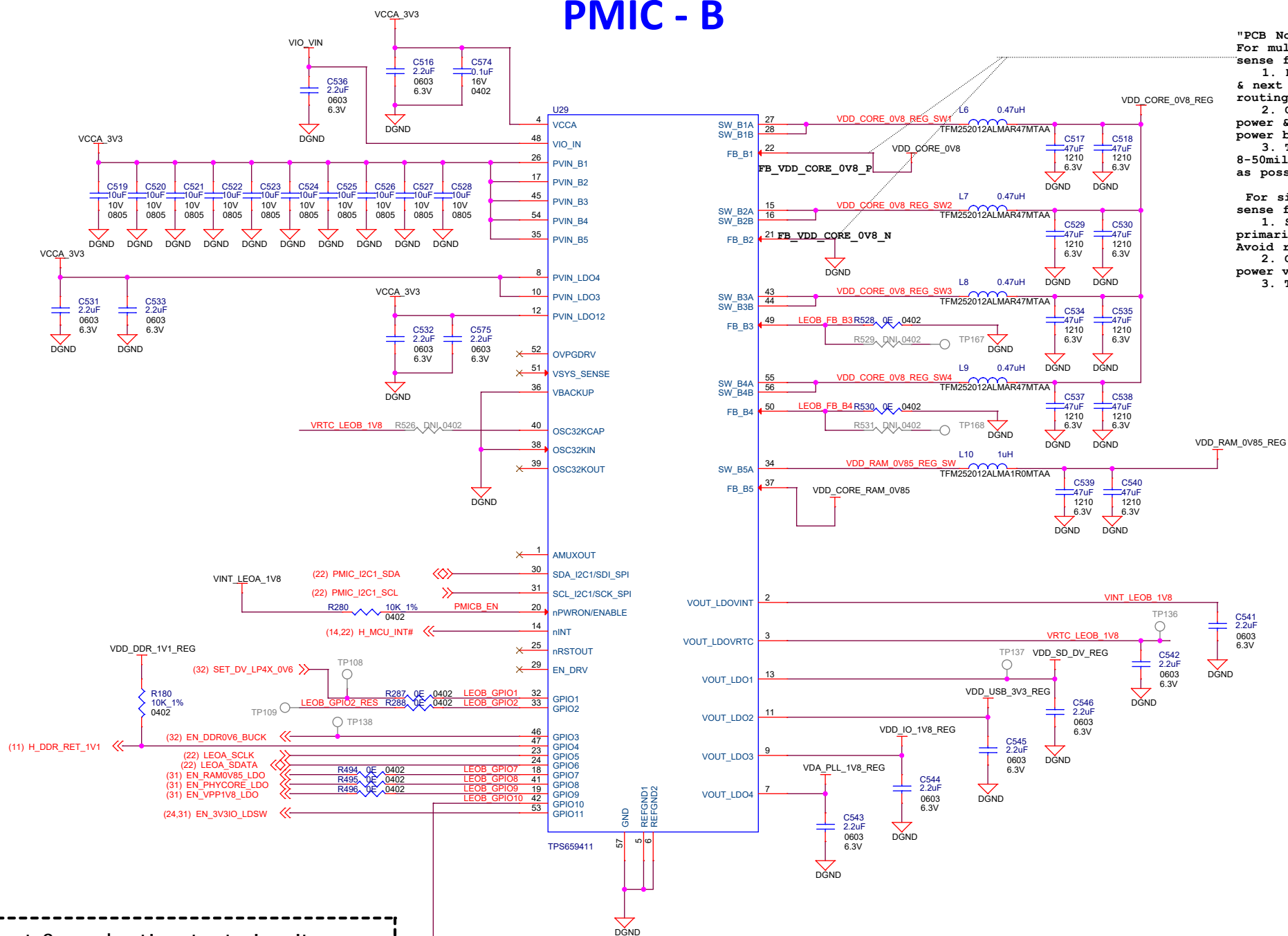
(27) H_SOC_PORz <<—

"GPIO9 connection to Gnd
as per PMIC ES1.0 errata."

SW2	COM	GPIO: Type	NVM Funtion
-1 = Open (Low) = Closed(High)	LEOA_WDOG_DISABLE Alt GPIO	In In/Out	Disable WDOG Alt NVM
-2 = Open (Low) = Closed(High)	Enable WDOG Timer Disable WDOG Timer	In In	Enable WDOG Disable WDOG

Project : J7 EVM		Title POWER SUPPLY 1			
		Size	PROC078 001 J721EXSOMG01EVM	Rev	
		C		E8A	
		Date:	Thursday, February 18, 2021	Sheet	22

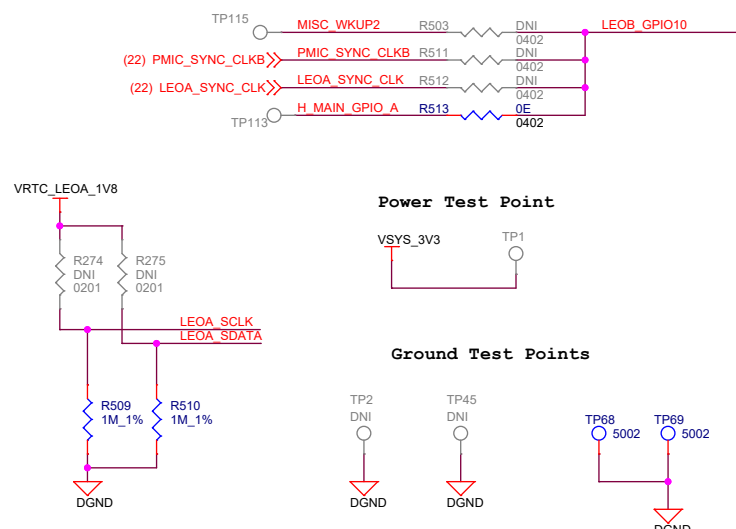
PMIC - B



"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

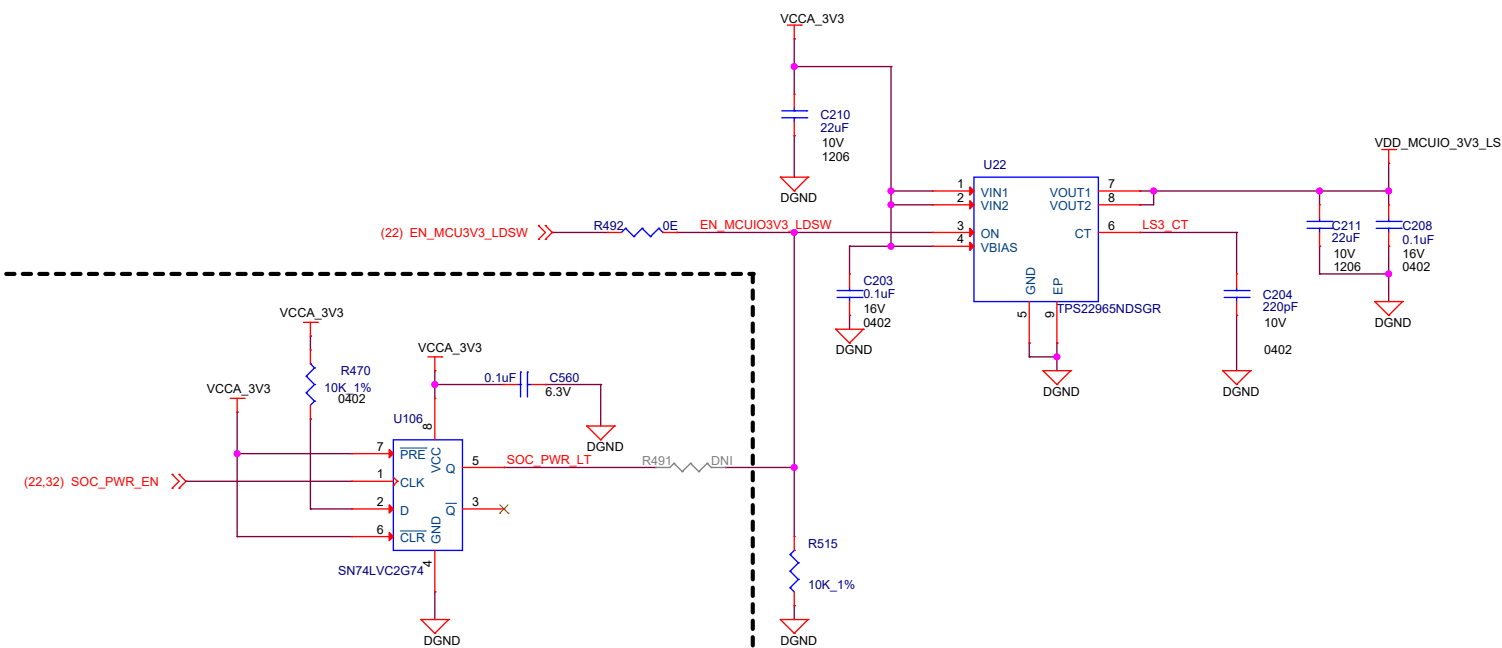
For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

EVM development & evaluation test circuitry
(TI EVM Only)

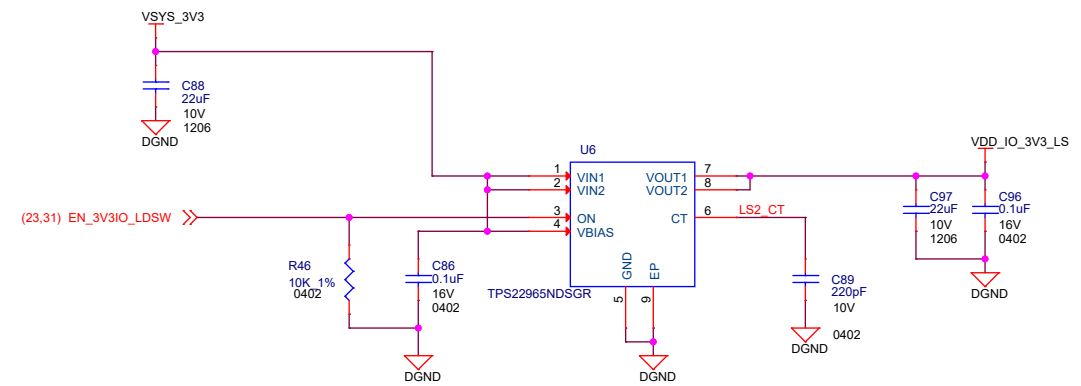


PMIC-B uses NVM to set I2C ADDR:
0x4C, 0x4D, 0x4E & 0x4F

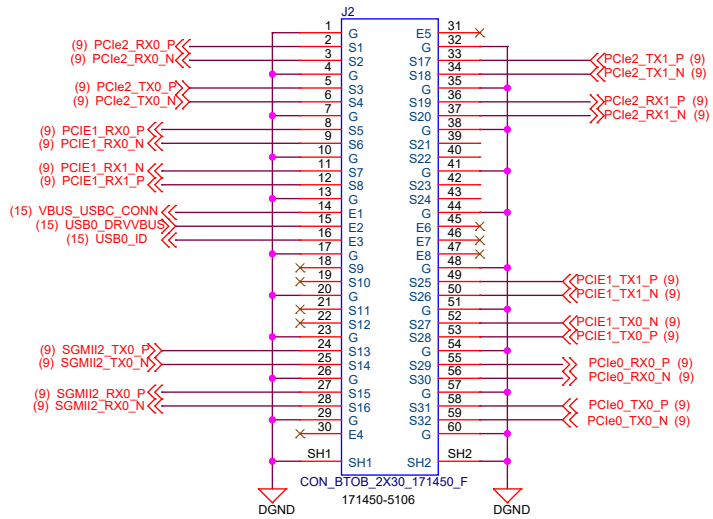
LOAD SWITCHES



EVM development & evaluation test circuitry (TI EVM Only)



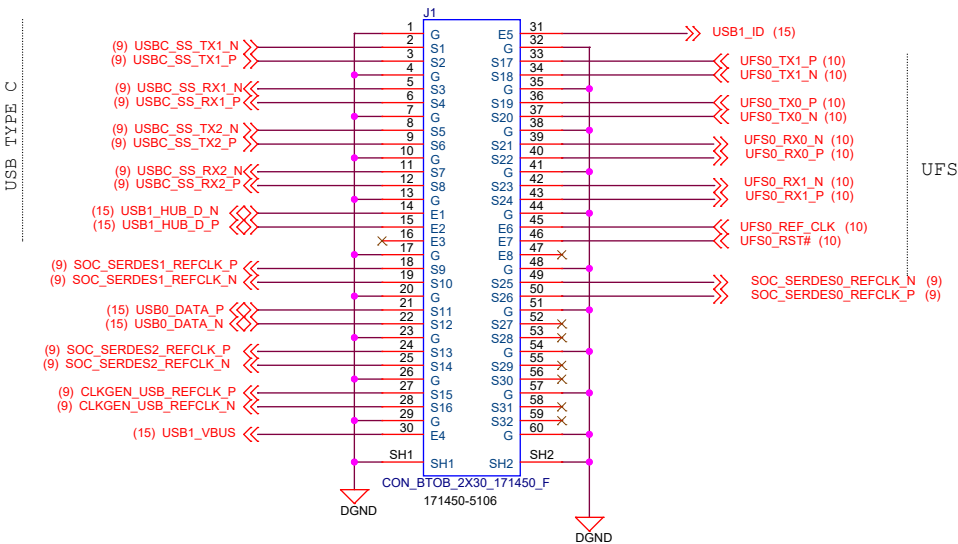
SOM to COMM PROC SERDES CONNECTORS



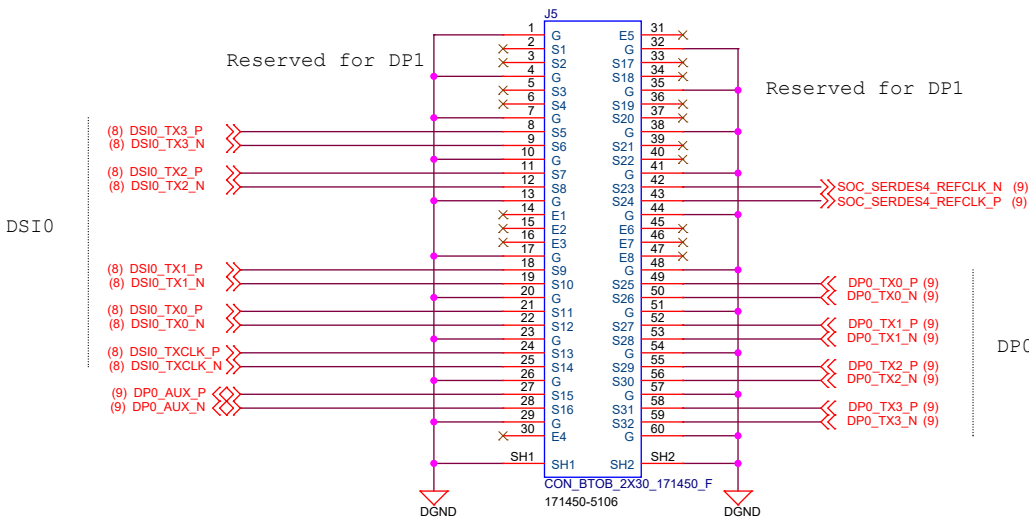
PCIE0-PCIe x1 Lane

PCIE1-PCIe x2 Lane

PCIE2-PCIe M.2



UFS



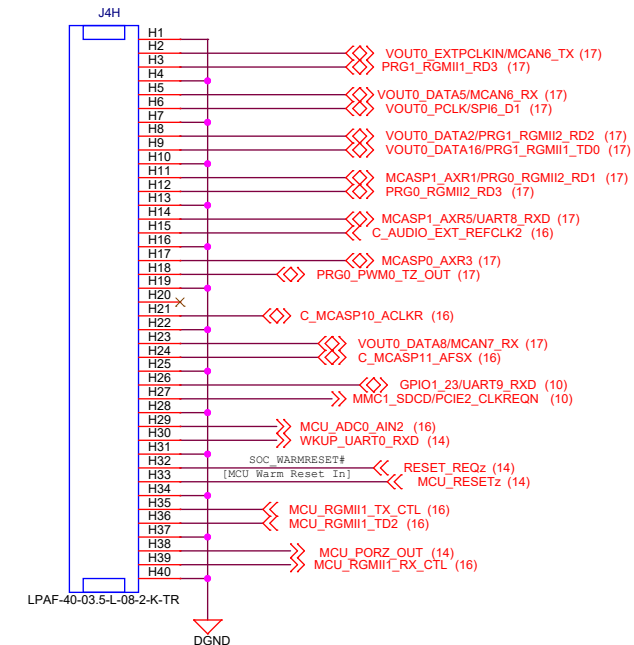
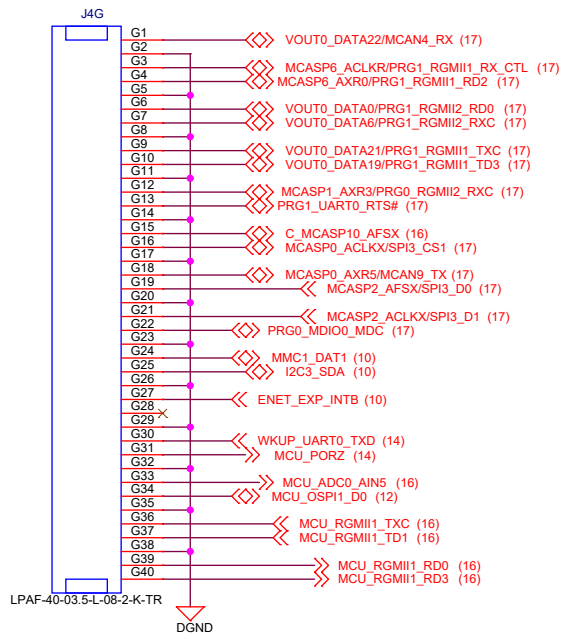
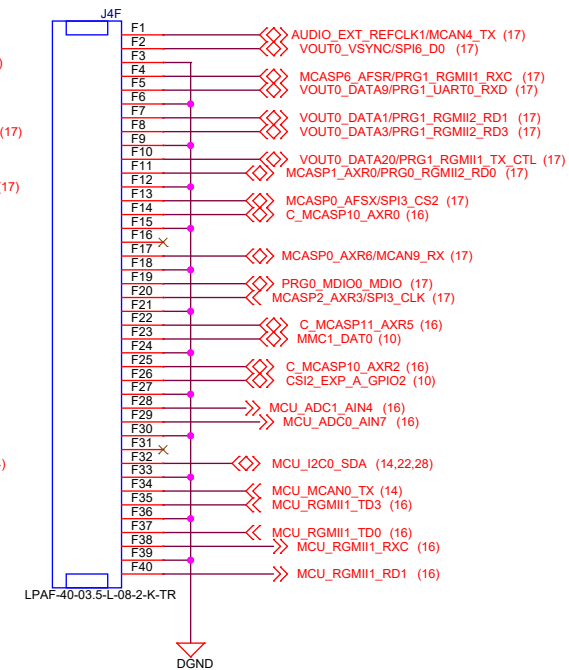
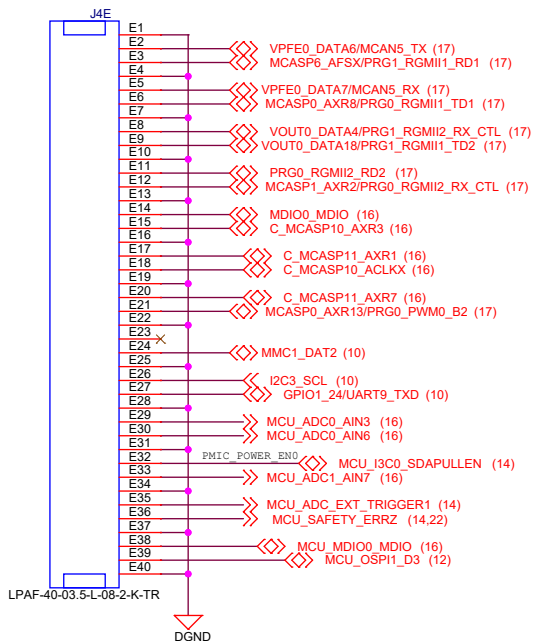
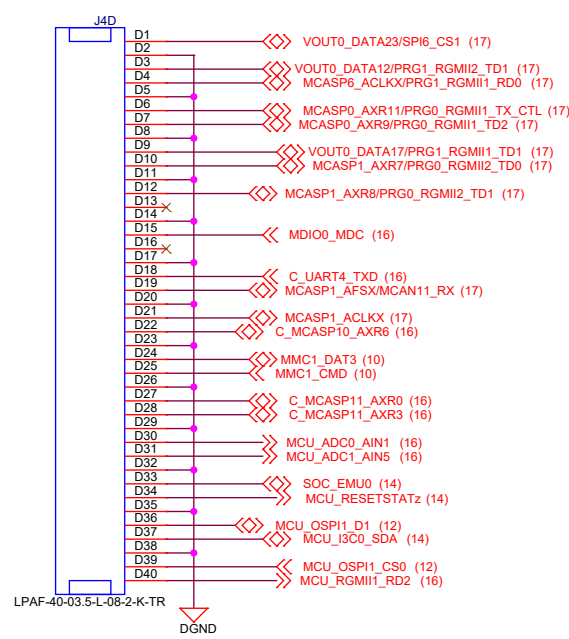
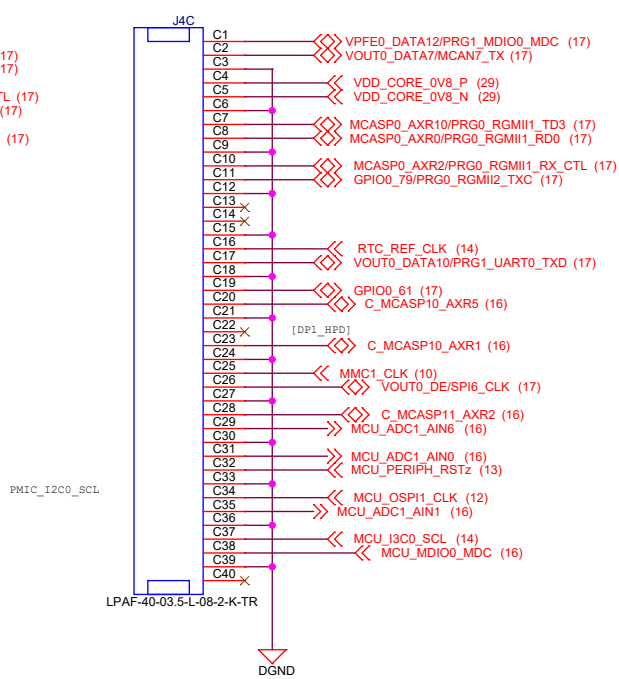
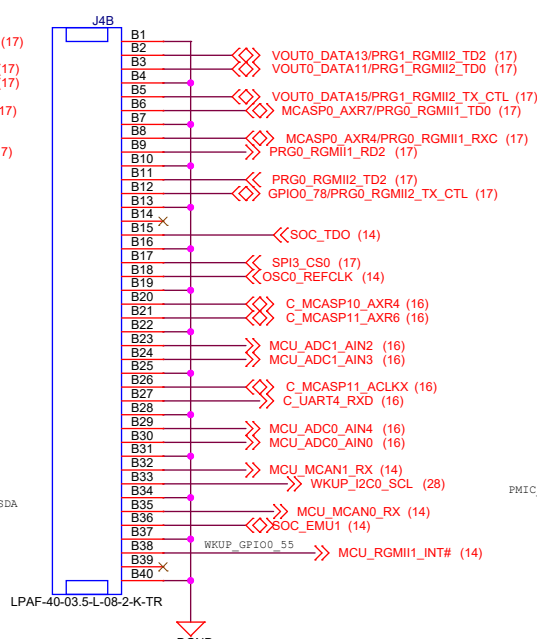
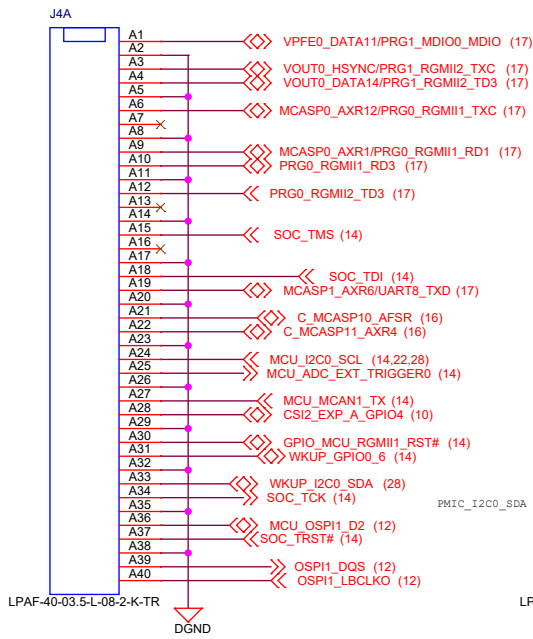
DP0

Project :
J7 EVM



Title SOM B-B MOLEX CONNECTORS		
Size	PROC078 001 J721EXSOMG01EVM	Rev
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Date:	Thursday, February 18, 2021	Sheet 25 of 34

SOM to COMM PROC PRIMARY CONN #1



Project :

J7 EVM



Title
SOM B-B SAMTEC CONN#1

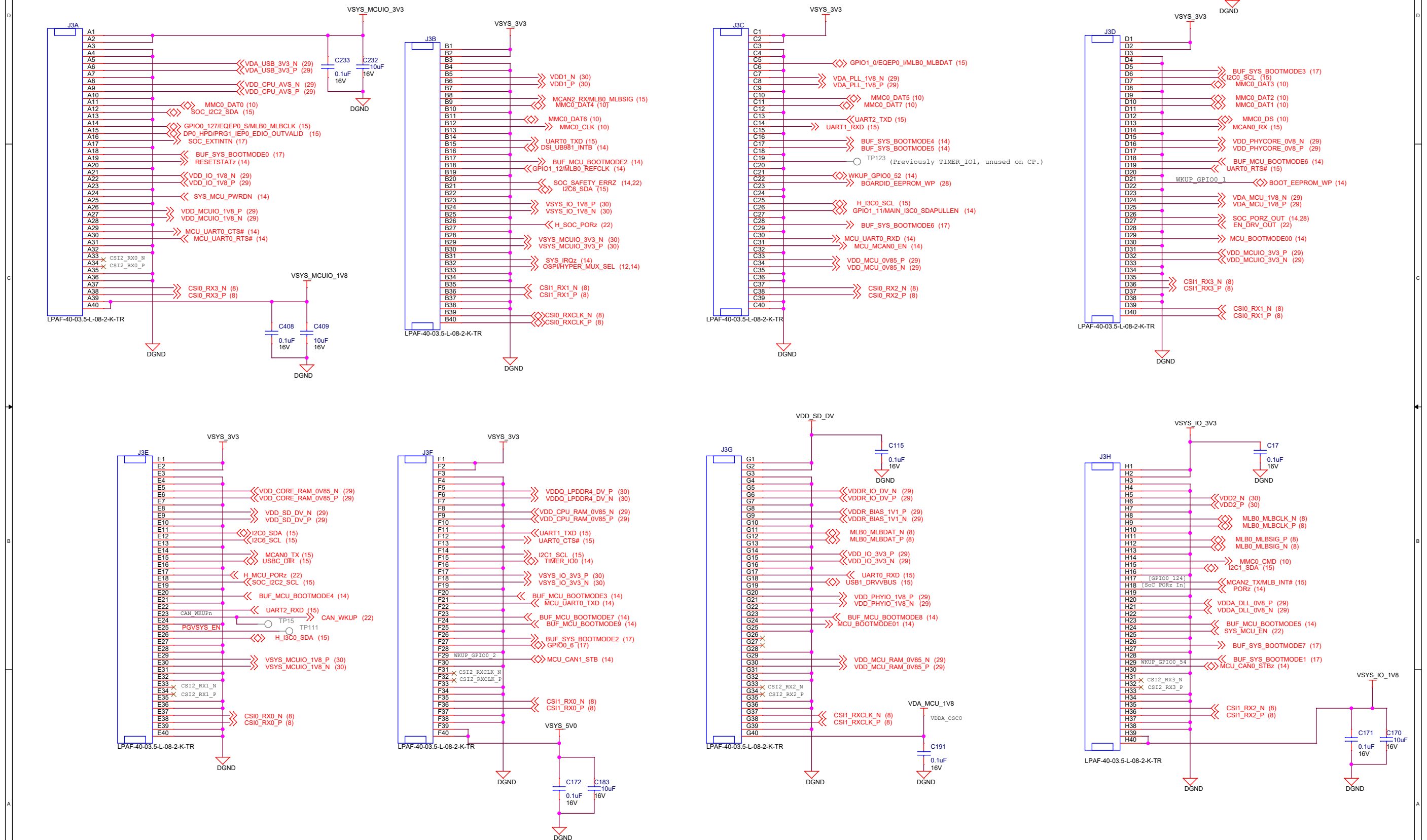
Size
C PROC078 001 J721EXSOMG01EVM

Date: Thursday, February 18, 2021

Rev
E8A

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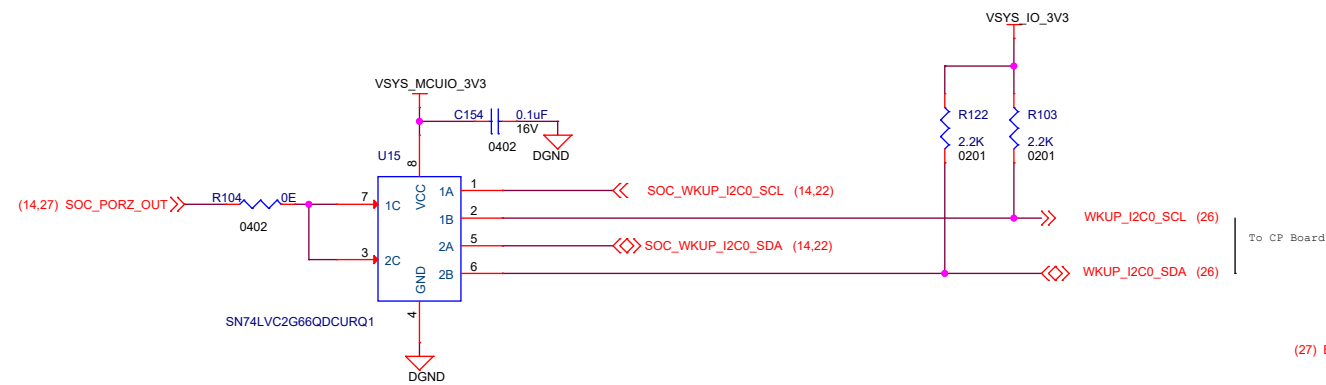
SOM to COMM PROC PRIMARY CONN #2



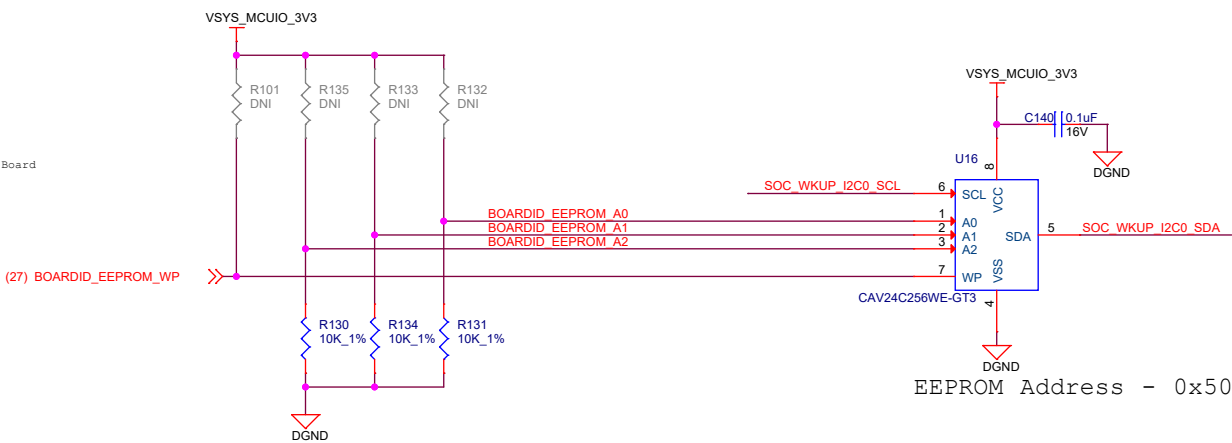
EVM development & evaluation test circuitry

(TI EVM Only)

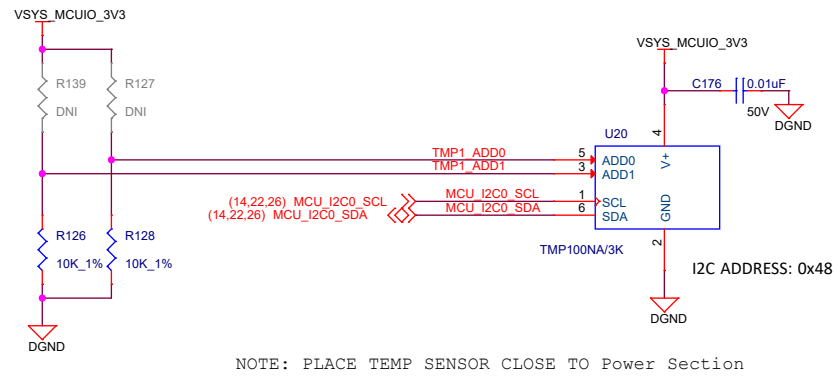
I2C for BOARD ID EEPROMs



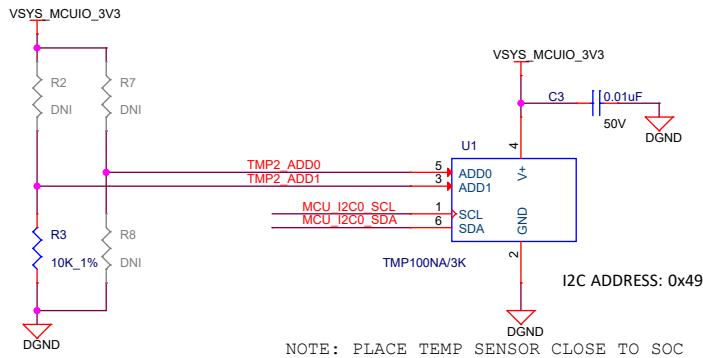
BOARD ID EEPROM (TI EVM Only)



TEMPERATURE SENSORS (TI EVM Only)

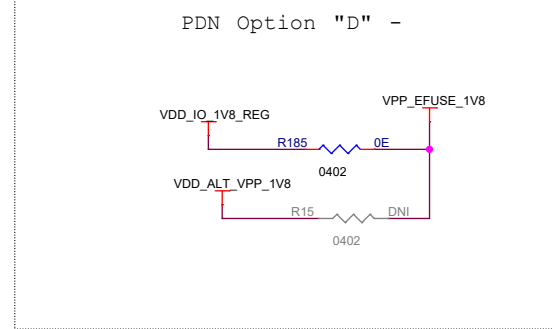
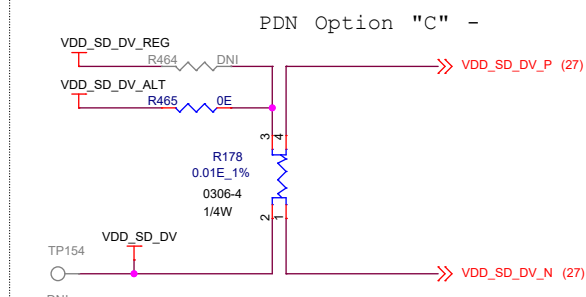
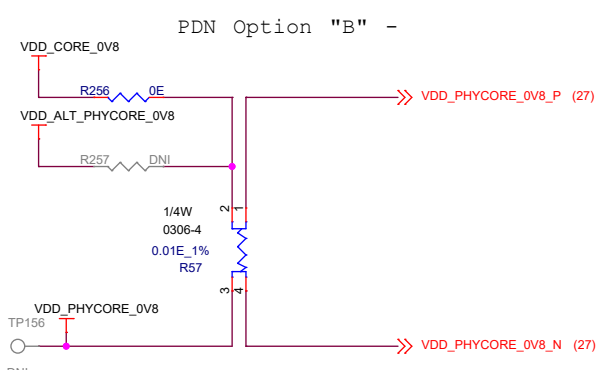
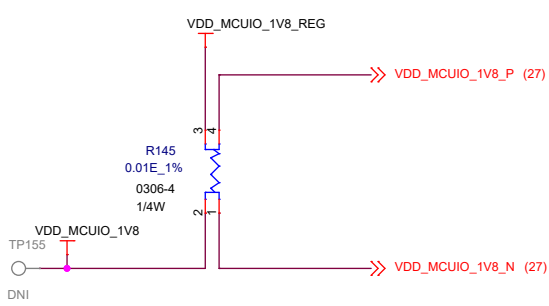
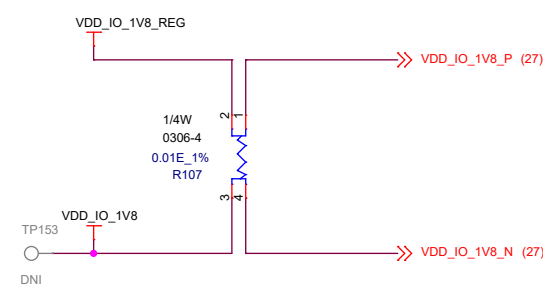
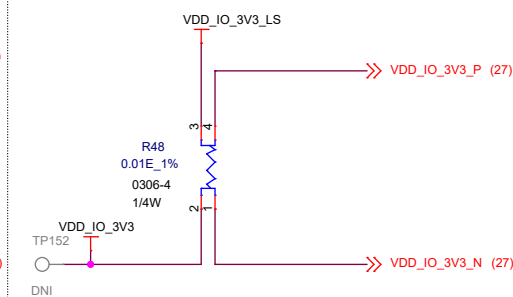
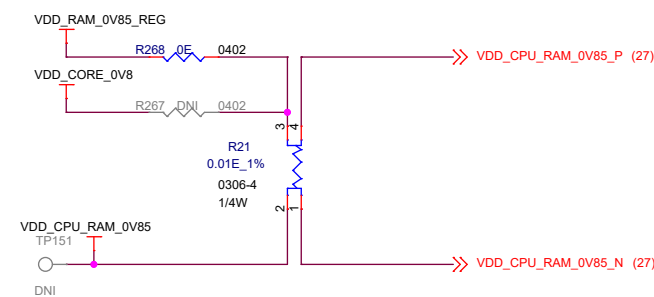
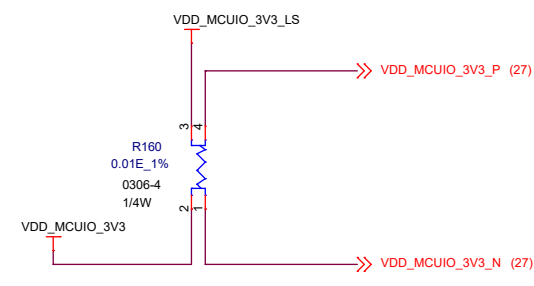
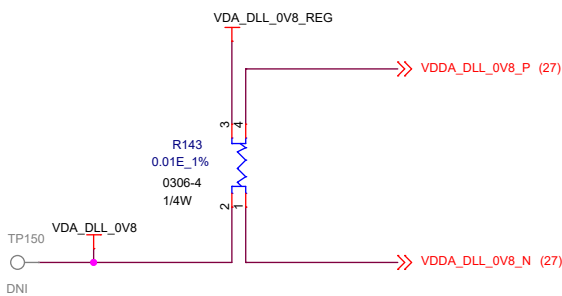
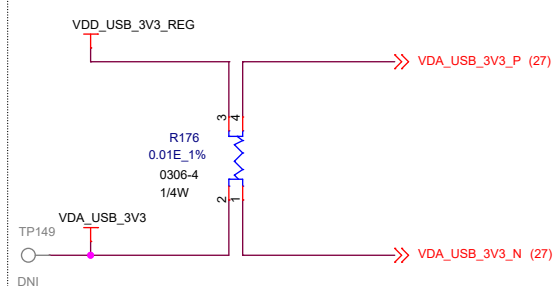
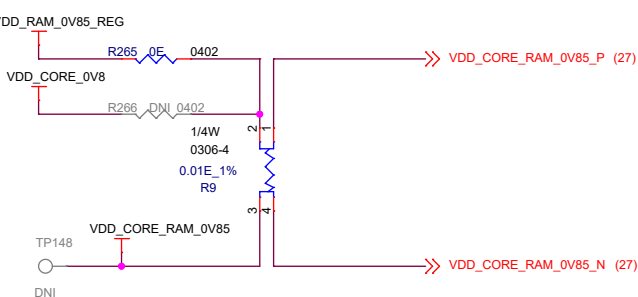
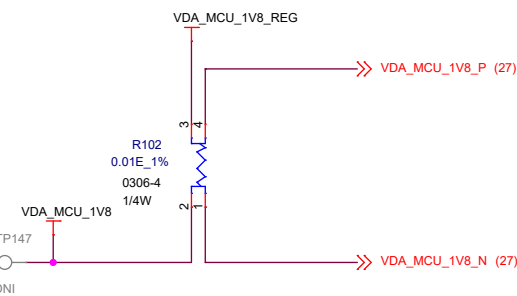
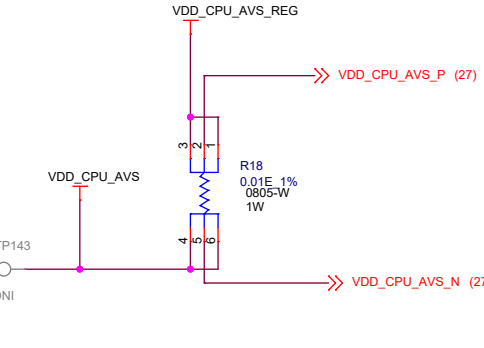
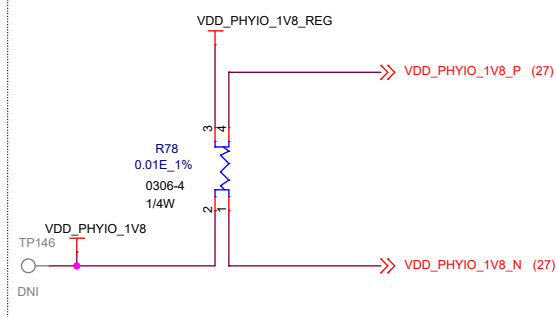
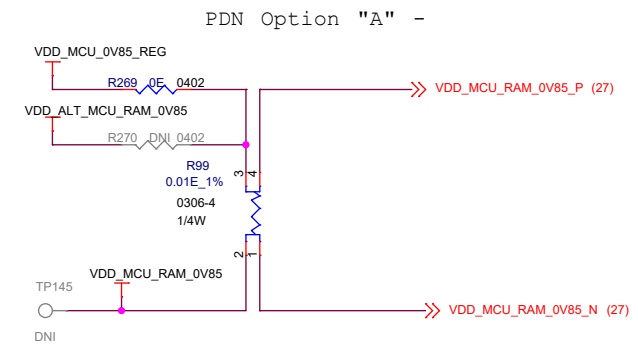
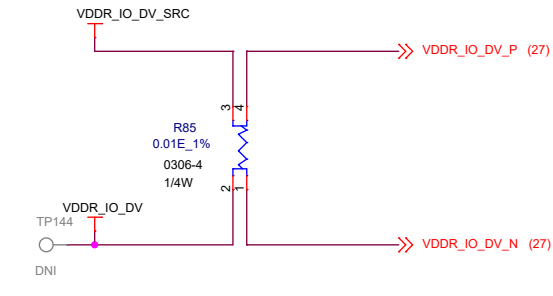
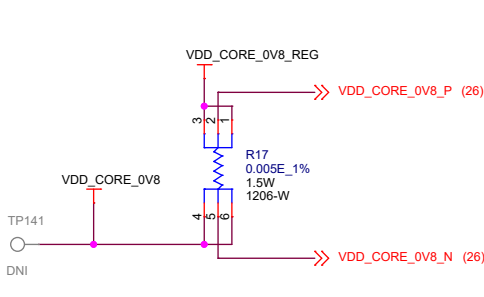
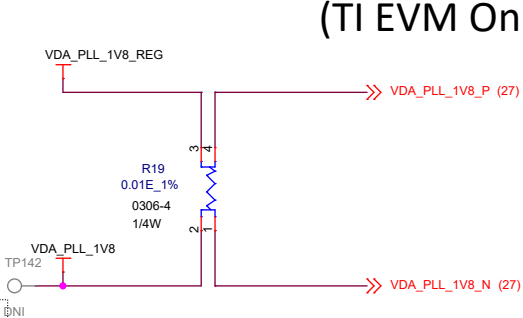
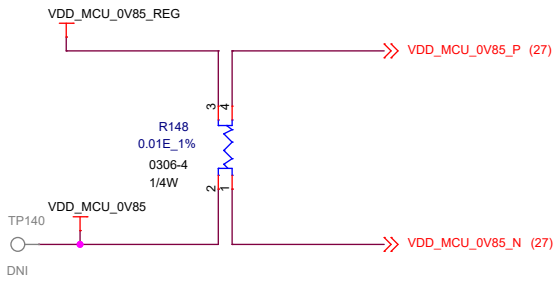
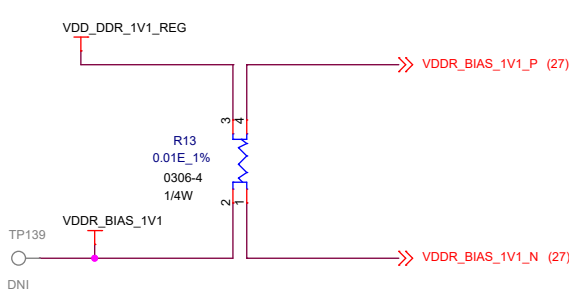


NOTE: PLACE TEMP SENSOR CLOSE TO Power Section



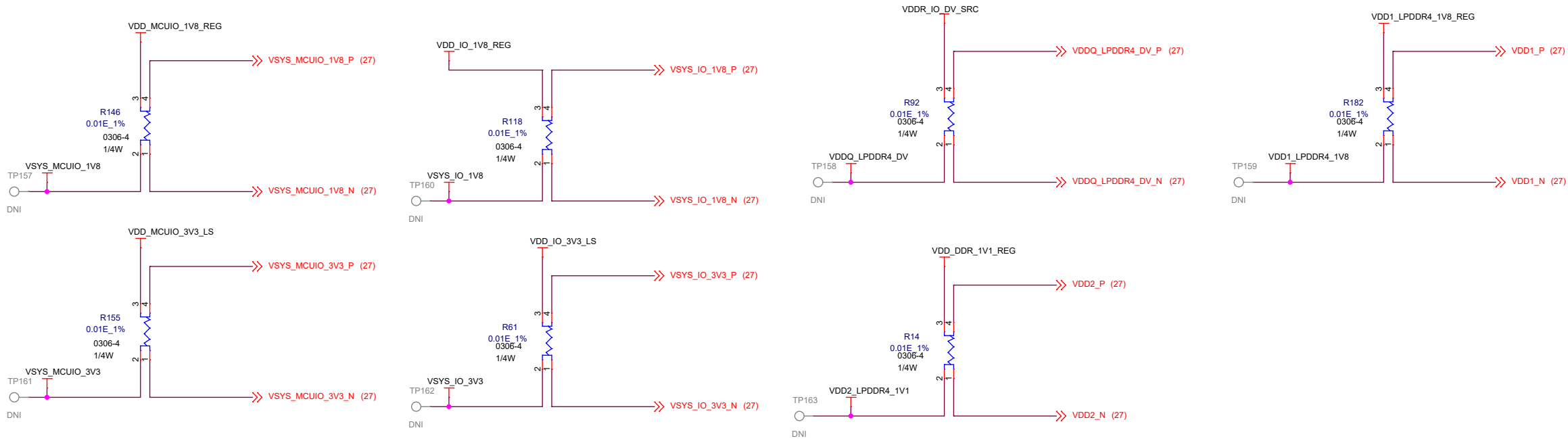
NOTE: PLACE TEMP SENSOR CLOSE TO SOC

SOC Current Sense Resistors

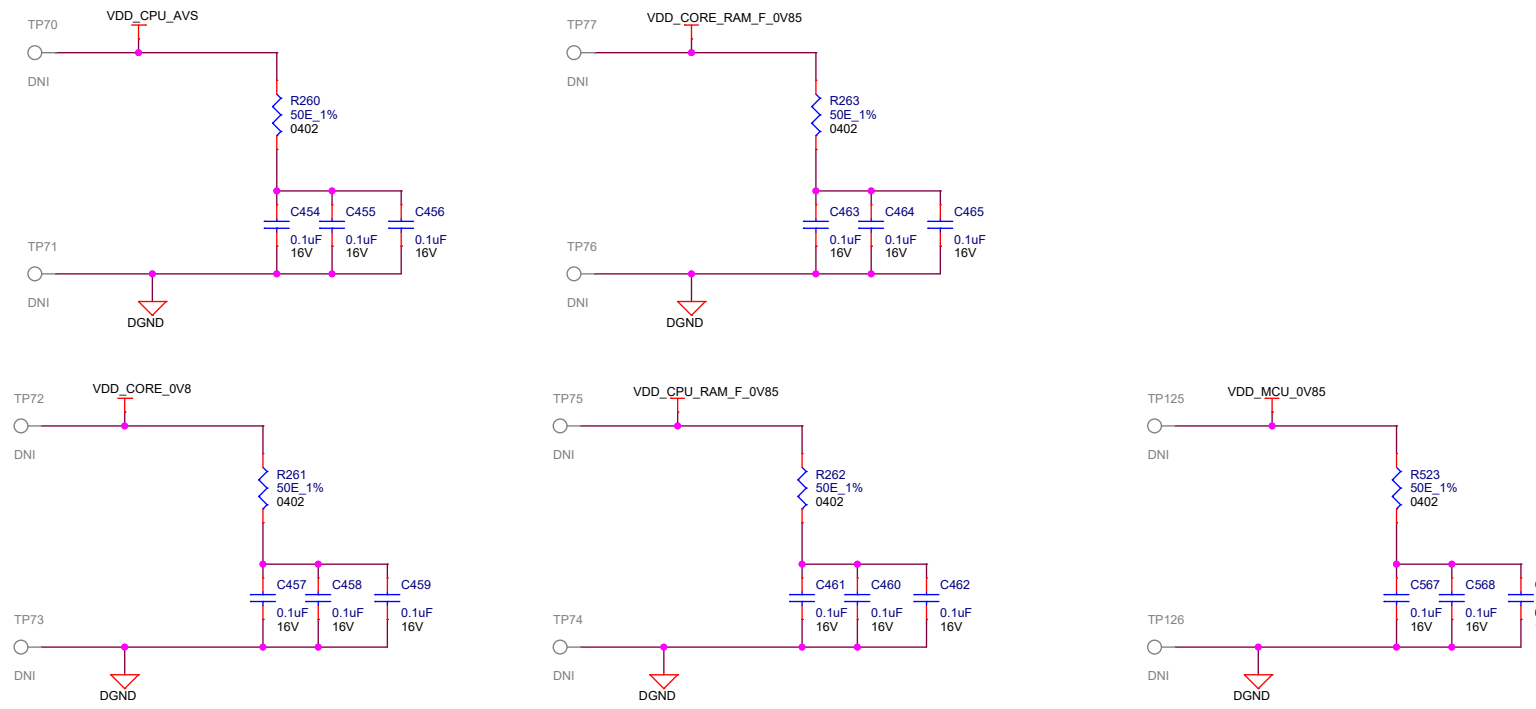


EVM development & evaluation test circuitry
(TI EVM Only)

Peripheral Current Sense Resistors



Supply Rail Kelvin Sensing



ALTERNATE POWER SUPPLY OPTIONS A - D

EVM development & evaluation test circuitry
(TI EVM Only)

TI Internal Evaluations Only

Alternate power resources have been shown for functional & electrical testing on a few key SoC voltage domains.

PDN Options -

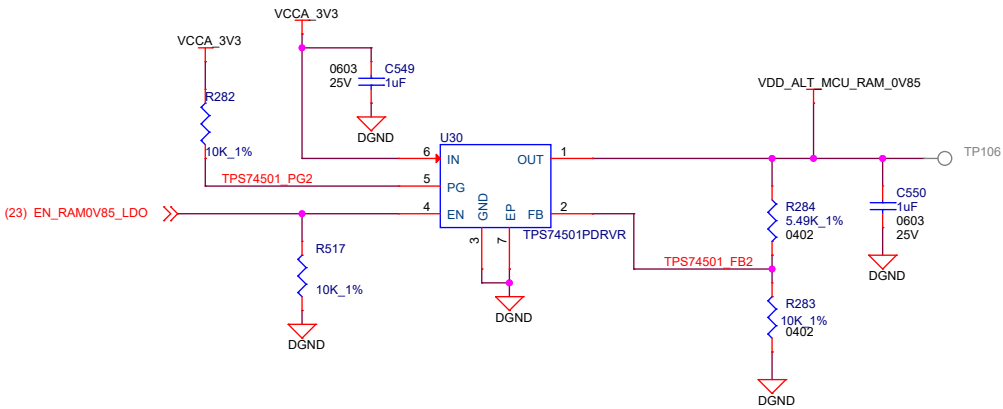
A) Evaluate common 0.85V Buck resource for both MCU CORE and MCU RAM array domains.
Evaluate common 0.85V Buck resource for both Main CORE and Main CORE & CPU RAM arrays.
On EVM boards, PDN options for independent RAM domains are required to support RMA device testing & trouble-shooting.

B) Evaluate an independent low noise LDO for supplying VDD_PHYCORE_0V8 power rail & high speed SERDES (i.e. Sierra, Torrent) PHY Core domains.

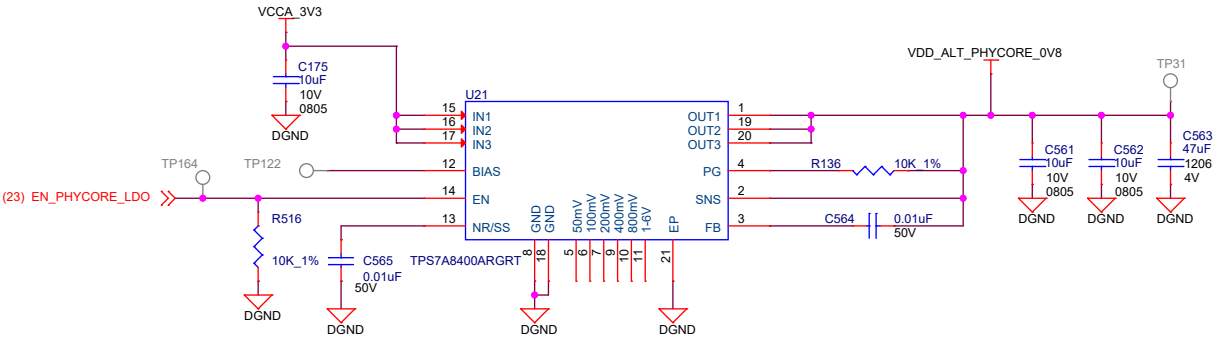
C) Evaluate a Dual LDO source for VDD_SD_DV that can change voltage level using GPIO control signal.

D) Evaluate a standard, low-impedance PMIC LDO or "Tri-State-able", high-impedance LDO for supplying VPP_EFUSE_1V8 power rail & domain.

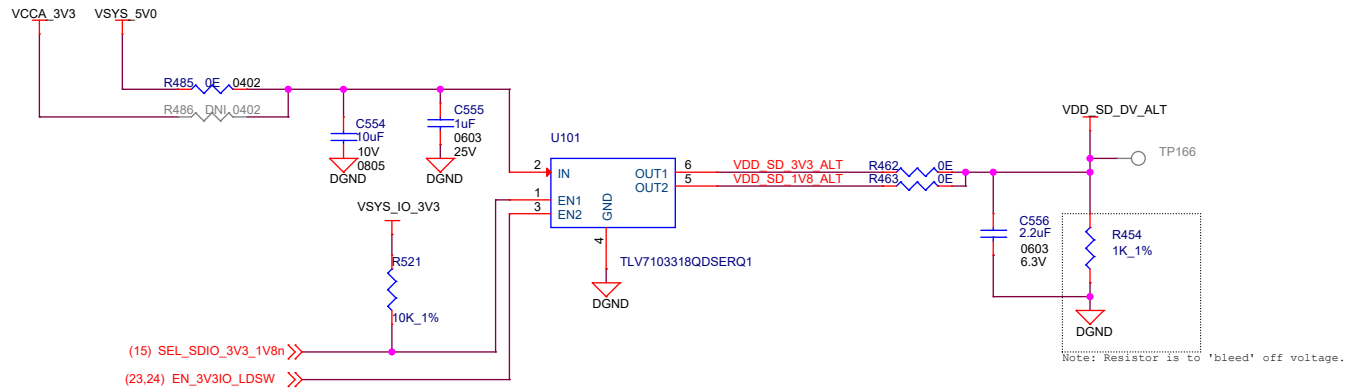
PDN Option - A: VDD_MCU_RAM_0V85_ALT rail's source



PDN Option - B: VDD_PHYCORE_0V8_ALT rail's source

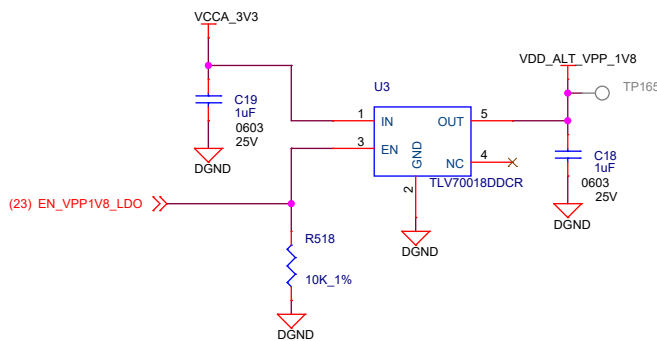


PDN Option - C: VDD_SD_DV_ALT rail's source



VDD_SD_DV_ALT	EN1	EN2	Comments
3.3V	HIGH	HIGH	Both enables driven high during power up seq to support initial 3.3V signaling per SD card protocol
1.8V	LOW	HIGH	SW controls & transition Sd card to high speed 1.8V signaling if card type supports

PDN Option - D: VDD_VPP_1V8_ALT rail's source

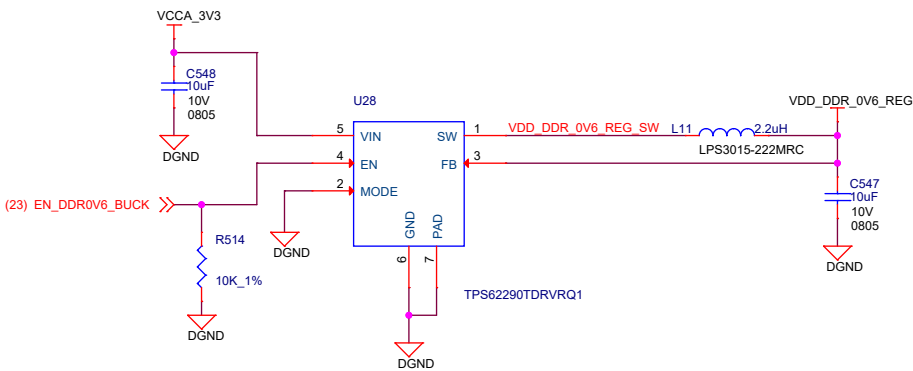


EVM development & evaluation test circuitry
(TI EVM Only)

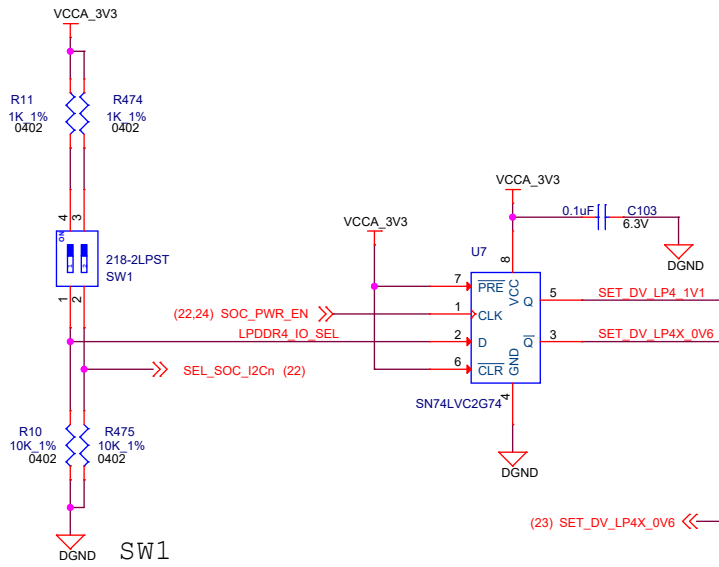
ALTERNATE LPDDR4X POWER SUPPLY OPTION

LP4 vs. LP4x VIO ISOLATION

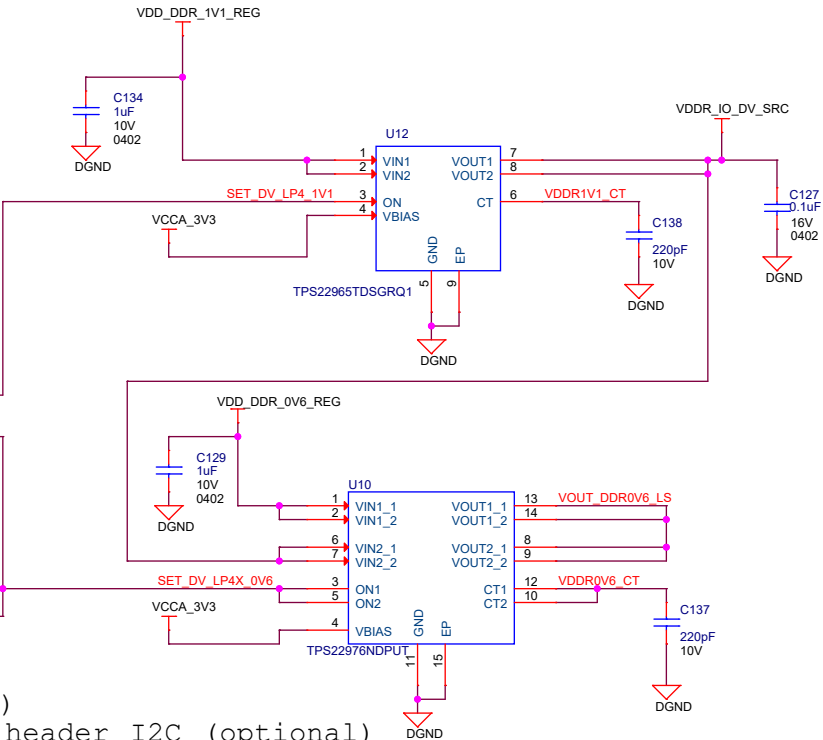
0.6V BUCK CONVERTER



LP4 vs. LP4x SELECTION



- SW1
Pos1 - ON/High = LPDDR4 (default)
 OFF/Low = LPDDR4x (optional)
Pos2 - ON/High = PMIC I2C to Ext header I2C (optional)
 OFF/Low = PMIC I2C to SoC WKUP I2C (default)



EVM Development & Evaluation test circuitry

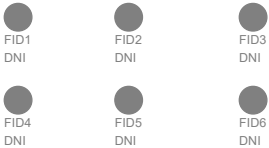
(TI EVM Only)

NOTES, HW & LABELS

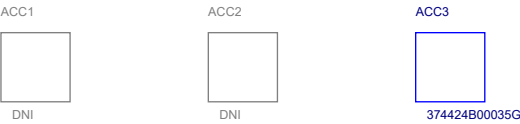
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

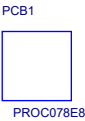
FIDUCIALS



SOCKET, PROCESSOR & HEATSINK AS ACCESSORIES



BARE PCB



LABELS

Board Serial No.



Assembly Revision.



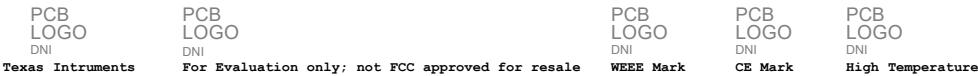
EVM Orderable No.



Orderable Part Numbers

Variant	Label Text
001 = Soldered GP SoC	J721EXSOMG01EVM
002 = Soldered HS SoC	J721EXSOMH01EVM
003 = Socketed SoC	J721EXSOMS01EVM

LOGOs



Project :

J7 EVM



Title
HARDWARE SCHEMATICS

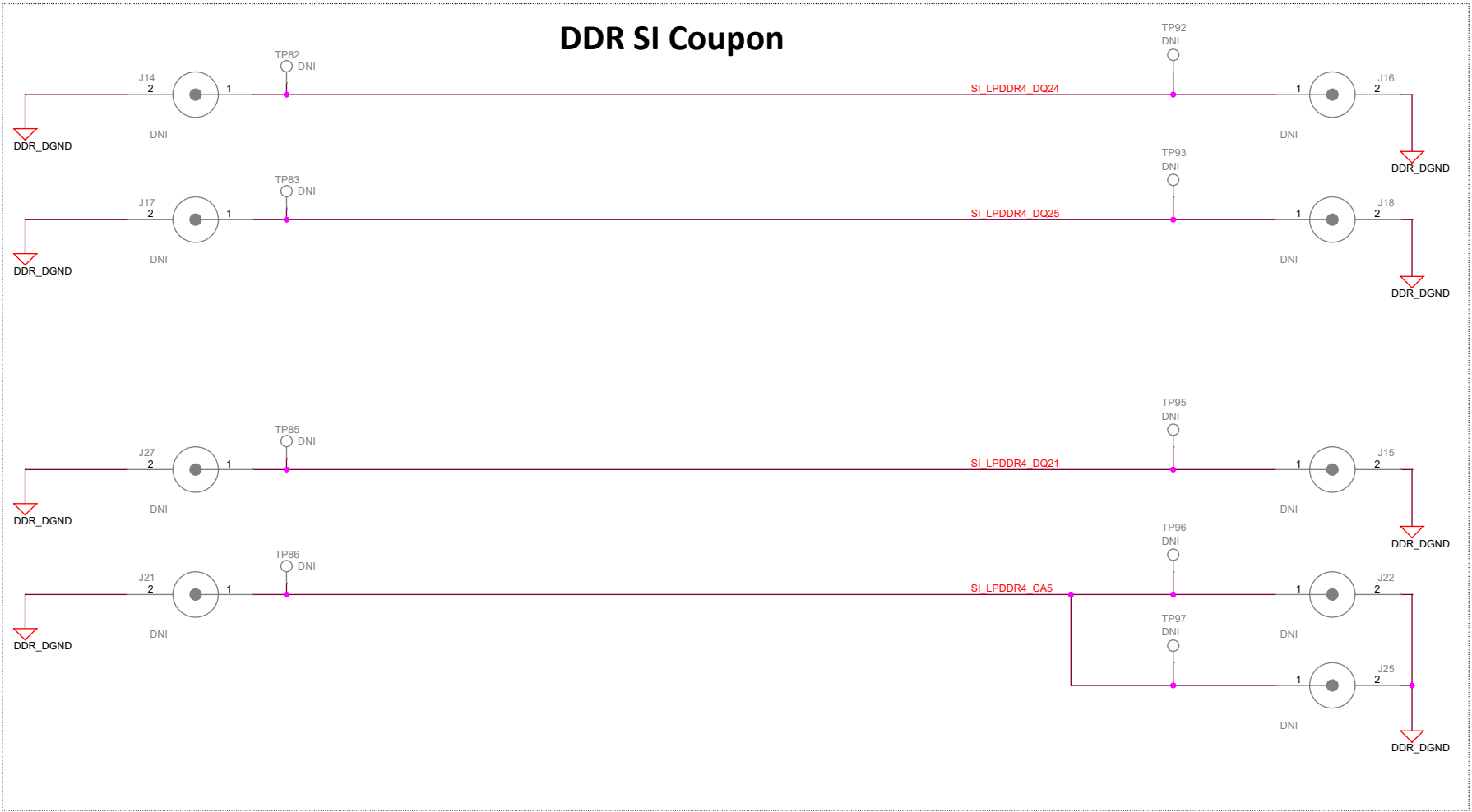
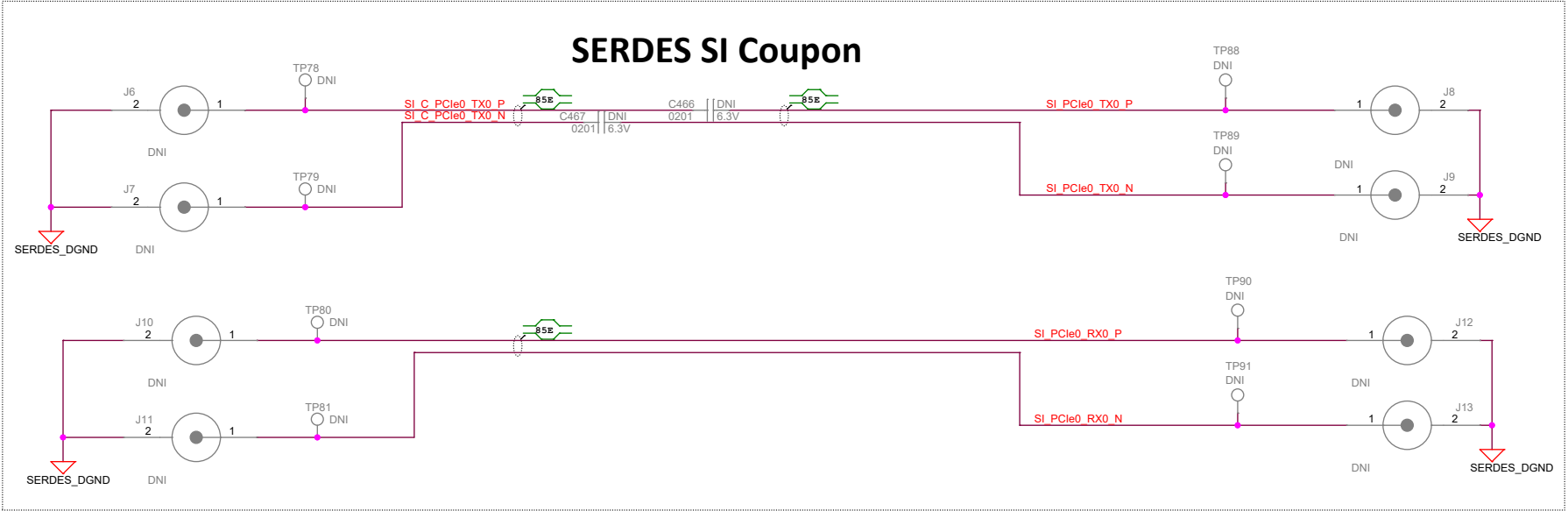
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SI_SIMULATION_COUPON_BD

Note: Test coupon not part of EVM design, to be used for TI test only



**ALL New Designs should use
3-Phase Buck supplying VDD_CPU
(Dual Leo PDN or Leo + Hera PDN)**

DRA829/TDA4VM 3-Phase Dual Leo2.0 PDN-0B

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3-Phase Buck supplying VDD_CPU
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