

J7X COMMON PROCESSOR BOARD

TABLE OF CONTENTS

PAGE	CONTENTS	PAGE	CONTENTS
01	TABLE OF CONTENTS	35	USB 2.0 TYPE-A CONN
02	REVISION HISTORY #1	36	USB 3.0 uAB INTERFACE
03	REVISION HISTORY #2	37	USB TYPE C 3.1
04	BLOCK DIAGRAM	38	2:1 MUX's
05	POWER FLOW DIAGRAM	39	MCU GB ETHERNET
06	POWER SEQUENCE	40	MLB INTERCACE
07	I2C TREE	41	FPD LINK-III DESERIALIZER
08	GPIO EXPANDER MAP/TABLE	42	AUDIO I/F CODEC
09	SOM B-B MOLEX CONNECTORS	43	AUDIO I/F -STEREO LINE IN
10	SOM B-B SAMTEC CONN#1	44	AUDIO I/F- STEREO MIC #1
11	SOM B-B SAMTEC CONN#2	45	AUDIO I/F- STEREO MIC #2
12	INFO/GESI_EXPANSION_CONN	46	AUDIO I/F -STEREO LINE OUT 1
13	CSI2 EXPANSION CONNECTORS	47	AUDIO I/F -STEREO HP OUT 2 & 3
14	ENET_EXPANSION_CONN	48	DSI_FPC
15	SERDES CLOCK GENERATOR #1	49	DSI_FPD_LINK
16	SERDES CLOCK GENERATOR #2	50	DISPLAY PORT INTERFACE
17	PERIPHERAL CLOCK GENERATOR	51	ADC, RTC, I3C, APPLE AUTH
18	RESET BUTTONS	52	x1LANE PCIe CONN
19	RESET INPUTS	53	x4LANE PCIe CONN
20	RESET OUTPUTS	54	PCIe_M.2_INTERFACE
21	GPIO EXPANDERS	55	BOOT MODE BUFFER & SWITCHES
22	SPI NOR FLASH	56	TEST AUTOMATION HEADER
23	MICRO SD CARD INTERFACE	57	OVER VOLTAGE PROTECTION CKT
24	eMMC FLASH	58	POWER SUPPLY #1
25	UFS FLASH	59	POWER SUPPLY #2
26	EEPROM	60	POWER SUPPLY #3
27	DUAL PORT FTDI	61	POWER SUPPLY #4
28	QUAD PORT FTDI	62	EXTERNAL POWER MEASUREMENT
29	JTAG MUX	63	CURRENT MONITORS #1
30	XDS110 DEBUGGER	64	CURRENT MONITORS #2
31	JTAG MIPI 60 CONN	65	CURRENT MONITORS#1 -INA231
32	CAN TRANSCEIVERS #1	66	CURRENT MONITORS#2 -INA231
33	CAN TRANSCEIVERS #2	67	SI_SIMULATION_COUPON_BD
34	USB HUB	68	HARDWARE SCHEMATICS

REV	A
VER	0.2

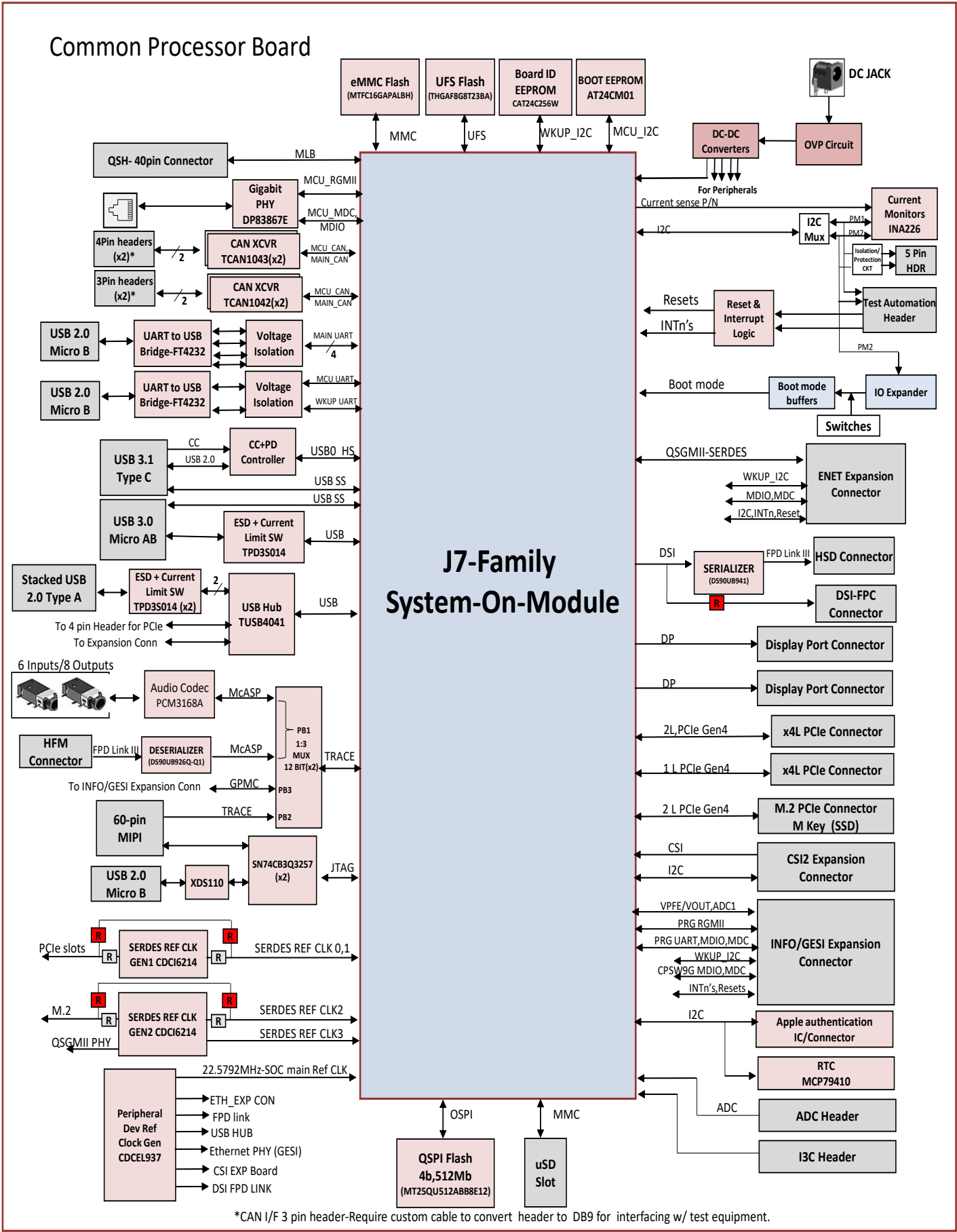
REVISION HISTORY #1

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	10th OCT 2020	Drafted from "PROC079E3C_SCH" Increased the VSYS_3V3 output current rating from 15A to 18A: Changed L3 value from 1uH to 2.2uH Changed C97 value from 0.015uF to 1.8nF Changed C99 value from 2200pF to 87pF Changed R107 value from 10K to 16.9K Increased the VSYS_5V0 output current rating from 5A to 7A: Changed L2 value from 8.2uH to 4.7uH Changed C62 value from 2200pF to 27pF Changed C63 value from 0.015uF to 2.7nF Changed R77 value from 10mE to 5mE Changed R91 value from 10K to 11.8K	Mistral Design Team		
0.2	09th NOV 2021	Drafted from E3D schematics Added support for INA231 (due to availability issues), supporting with dual footprint (populate either INA226 or INA231) Replaced FB8/FB8 with 0E resistor (R943, R944) for improved performance during EMI Compliance Updated VSYS_3V3 and VSYS_3V3_SOM supplies current measurement Baselined to REV A	Mistral Design Team		

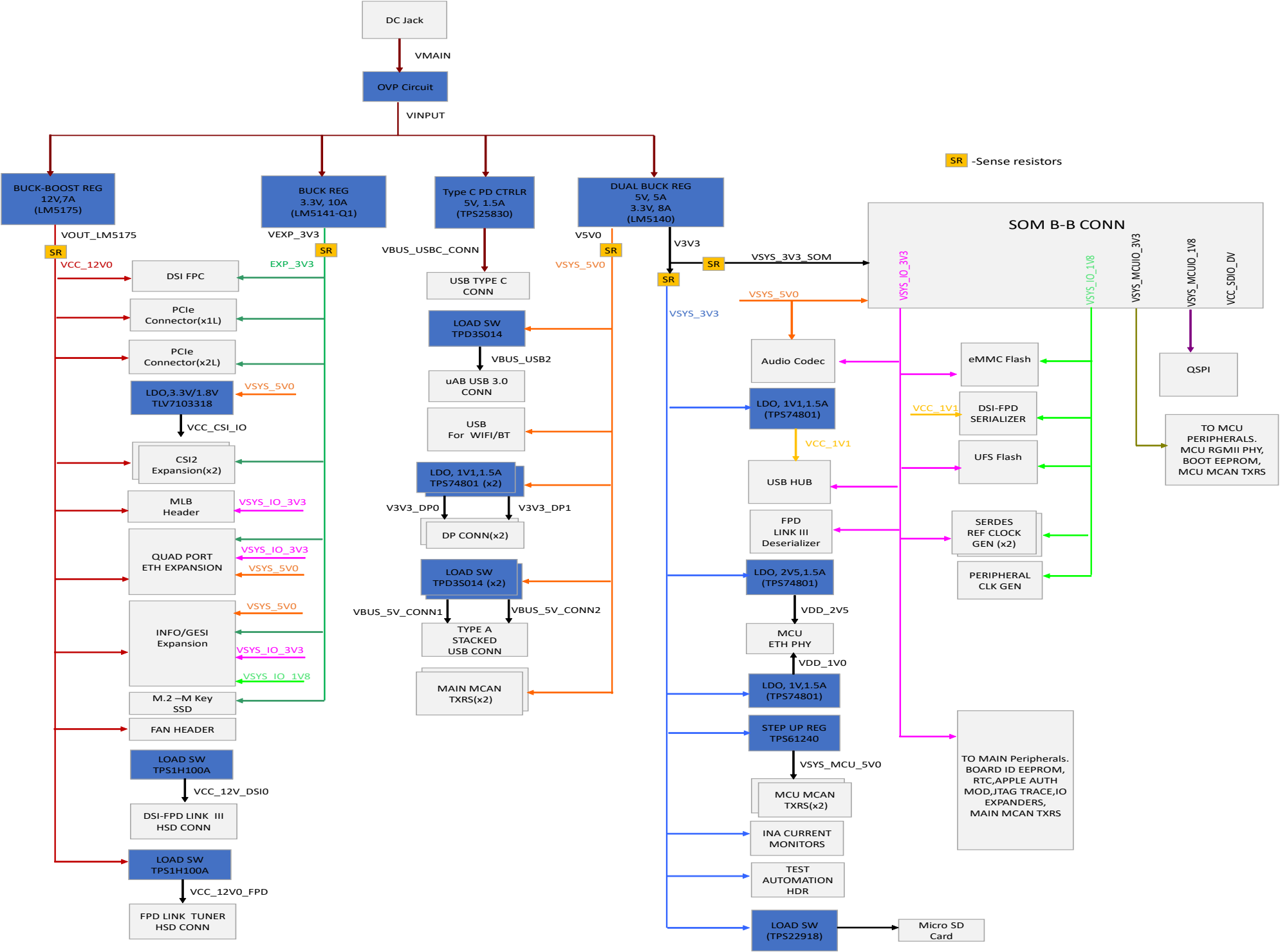
REVISION HISTORY #2

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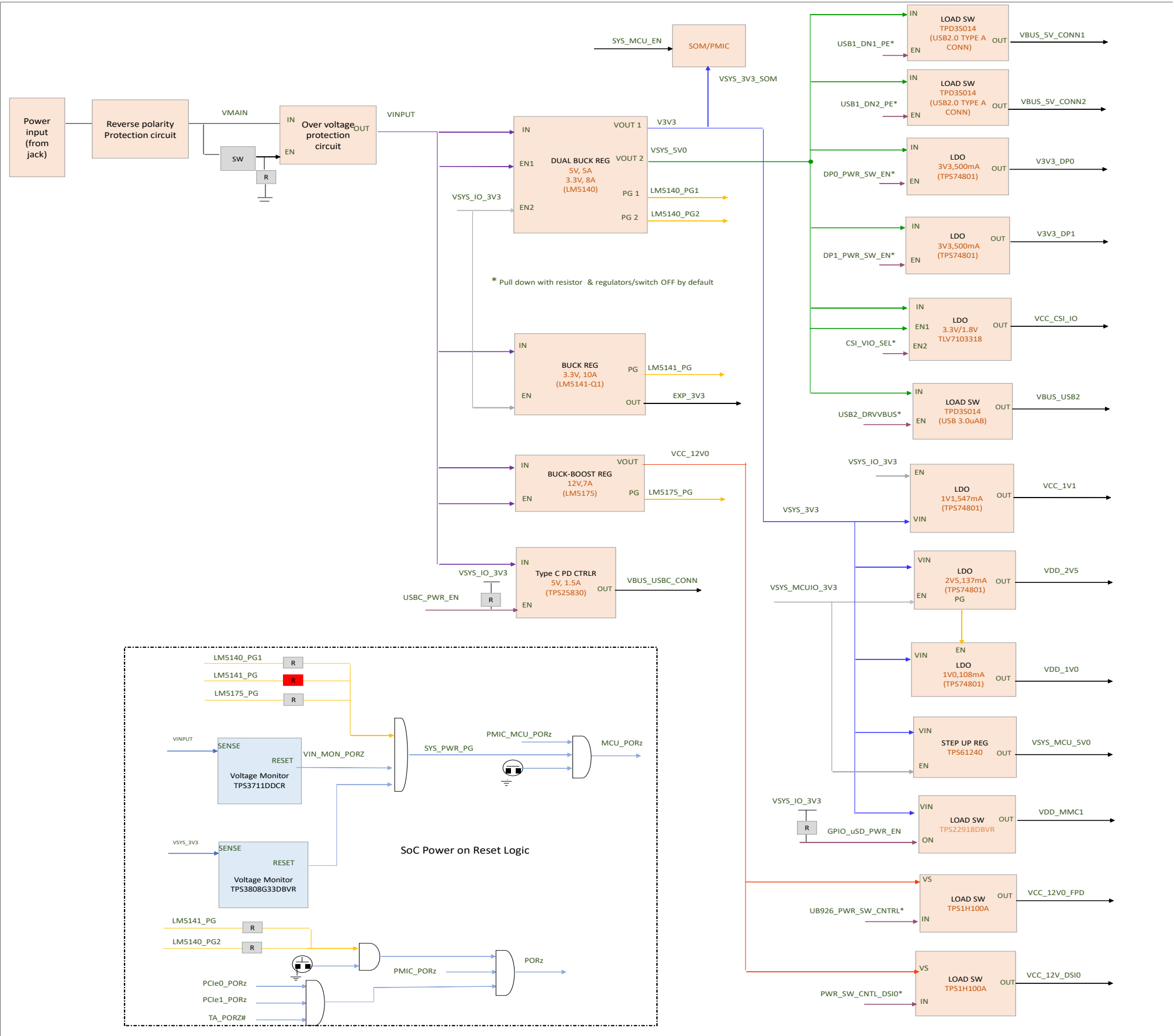
BLOCK DIAGRAM



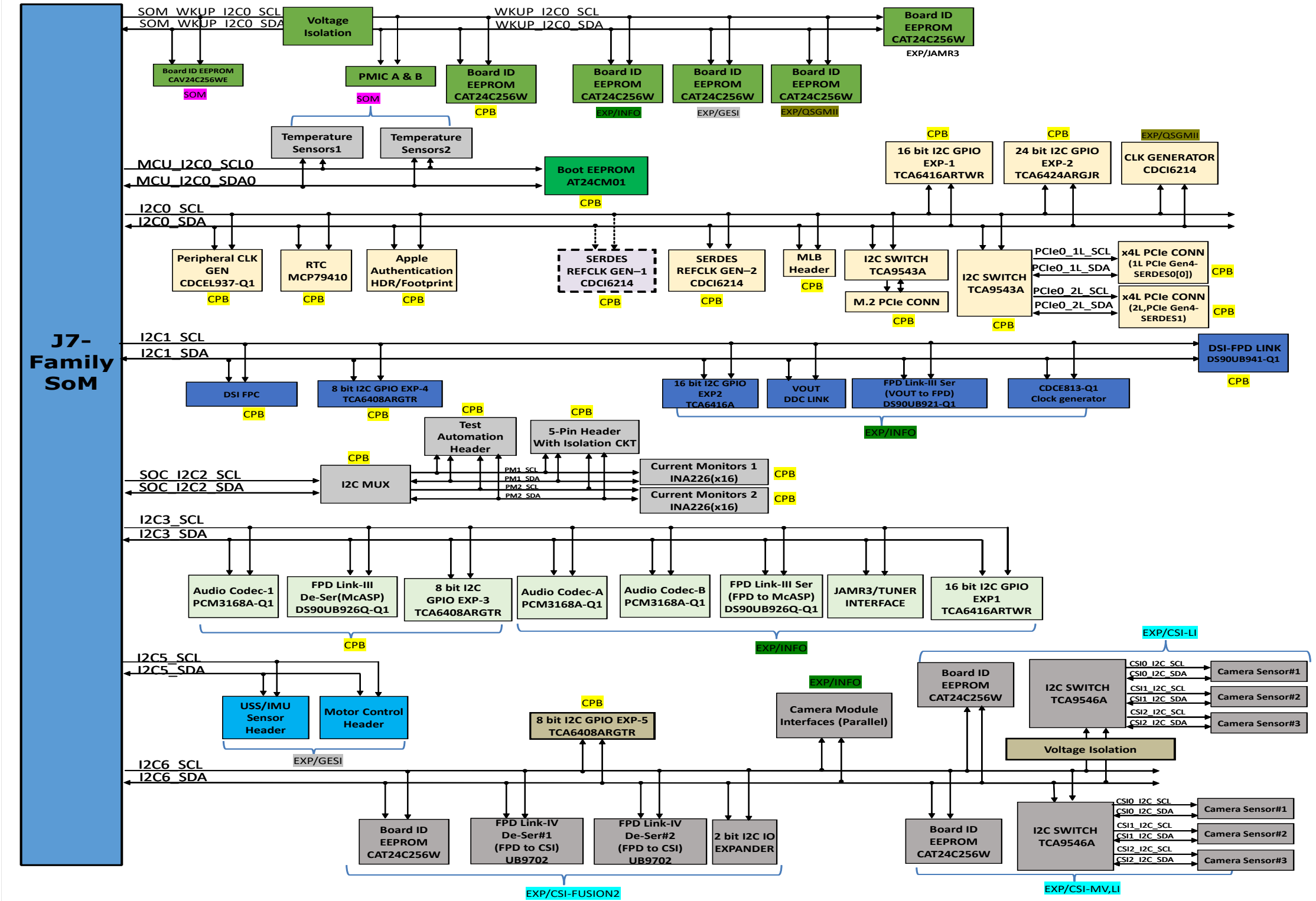
POWER FLOW DIAGRAM



POWER SEQUENCE



I2C TREE



Project :

J7 EVM



Title
I2C TREE

Size
C PROC079 001 J721EXCP01EVM

Date: Friday, December 03, 2021


Sheet 7 of 68

Rev
A

GPIO EXPANDER MAP/TABLE

I2C Bus/Address	GPIO Port	Net name	Direction WRT CTRL	Default state	Active state	Remarks
GPIO Expander - 1 Part# TCA6416ARTWR						
I2C0/0x20	P00	PCIE_2L_MODE_SEL	Input	DIP_SEL	NA	PCIE 2-Lane Mode Select ('0' - Root Complex, '1' - End Point)
	P01	PCIE_2L_PERSTZ	Input	PD	Active low	PCIE 2-Lane Bus Reset ('0' - device reset, '1' - normal operation)
	P02	PCIE_2L_RC_RSTZ	Output	PD	Active low	PCIE 2-Lane RC Reset Control ('0' - device reset, '1' - normal operation)
	P03	PCIE_2L_EP_RST_EN	Output	PD	Active low	PCIE 2-Lane EP Reset Enable ('0' - PERSTz isolated from PORz, '1' PERSTz connected to PORz)
	P04	PCIE_1L_MODE_SEL	Input	DIP_SEL	NA	PCIE 1-Lane Mode Select ('0' - Root Complex, '1' - End Point)
	P05	PCIE_1L_PERSTZ	Input	PD	Active low	PCIE 1-Lane Bus Reset ('0' - device reset, '1' - normal operation)
	P06	PCIE_1L_RC_RSTZ	Output	PD	Active low	PCIE 1-Lane RC Reset Control ('0' - device reset, '1' - normal operation)
	P07	PCIE_1L_EP_RST_EN	Output	PD	Active low	PCIE 1-Lane EP Reset Enable ('0' - PERSTz isolated from PORz, '1' PERSTz connected to PORz)
	P10	PCIE_2L_PRSENT#	Input	PU	Active High	PCIE 2-Lane Hot Plug/Card Detect ('0' - PCIe Card Detected, '1' - no card detected)
	P11	PCIE_1L_PRSENT#	Input	PU	Active High	PCIE 1-Lane Hot Plug/Card Detect ('0' - PCIe Card Detected, '1' - no card detected)
	P12	CDCI1_OE1/OE4	Output	PU	Active High	PCIE 2L Reference Clock Enable ('0 - clock disabled, '1' - clock enabled)
	P13	CDCI1_OE2/OE3	Output	PU	Active High	PCIE 1L Reference Clock Enable ('0 - clock disabled, '1' - clock enabled)
	P14	EXP_MUX1	Output	NA	NA	Expansion Board Mux control1 INFO - VINOUT_MUX_SELO; GESI - PRG1_RGMII/MCAN/PWM_SEL
	P15	EXP_MUX2	Output	NA	NA	Expansion Board Mux control1 INFO - VINOUT_MUX_SEL1; GESI - MDIO_MDC_SELO
	P16	EXP_MUX3	Output	NA	NA	Expansion Board Mux control1 INFO - Not Used; GESI - MDIO_MDC_SEL1
	P17	GESI_EXP_PHY_RSTz	Output	PU	Active High	EXP_RSTz - Terminated with Test point
GPIO Expander - 2 Part# TCA6424ARGJR						
I2C0/0x22	P00	APPLE_AUTH_RSTZ	Output	PD	Active low	Apple Authentication Chip Reset ('0' - device reset, '1' - normal operation)
	P01	MLB_RSTZ	Output	PD	Active low	MLB Interface Board Reset ('0' - board reset, '1' - normal operation)
	P02	GPIO_USD_PWR_EN	Output	PU	Active High	MicroSD Card Power Enable ('0' - power off, '1' - power on)
	P03	USBC_PWR_EN	Output	PU	Active High	USB-TypeC VBUS Controller Power Enable ('0' - power off, '1' - power on)
	P04	USBC_MODE_SEL1	Output	DIP_SEL	NA	USB-Type C Mode Select USBC_MODE_SEL[1:0]: '00' = DFP, '01' = DRP, '1x' = UFP
	P05	USBC_MODE_SELO	Output	DIP_SEL	NA	
	P06	MCAN0_EN	Output	PD	Active High	MCAN0 PHY Enable ('0' - device disabled, '1' normal operation)
	P07	MCAN0_STB#	Output	PD	Active low	MCAN0 PHY Standby ('0' - device standby, '1' - normal operation)
	P10	MUX_SPARE	Output	NA	Test Point	Signal Mux Control ('0' - Not Used, '1' - Not Used)
	P11	MCASP/TRACE_MUX_S0	Output	PU	PU / DIP_SEL	Signal Mux Control, DIP switch allow default to either Trace or GPMC. · TRACE with MIPI-60 Interface (set to '1' / '1') · Expansion for GPMC Support (set to '1' / '0')
	P12	MCASP/TRACE_MUX_S1	Output	PU		Audio Codec/Tuner Support (set to '0' / '1')
	P13	MLB_MUX_SEL	Output	PD		Signal Mux Control ('0' - MCAN2/Expansion, '1' - 3 Wire MLB)
	P14	MCAN_MUX_SEL	Output	PD	NA	Signal Mux Control ('0' - MCAN2/GPIO, '1' - Expansion/EQEP)
	P15	MCASP2/SPI3_MUX_SEL	Output	PD	NA	Signal Mux Control ('0' - Expansion/SPI3, '1' - Tuner I2S/MCASP2)
	P16	PCIE_CLKREQn_MUX_SEL	Output	PD	NA	Signal Mux Control ('0' - PCIE CLKREQn/I3C, '1' - Expansion GPIO)
	P17	CDCI2_RSTZ	Output	PU	Active low	Peripheral Clock Generator ('0' - device reset, '1' - normal operation)
	P20	ENET_EXP_PWRDN	Output	PD	Active High	Ethernet Expansion PHY Powerdown ('0' - normal operation, '1' - device power down)
	P21	ENET_EXP_RESETZ	Output	PU	Active low	Ethernet Expansion Reset ('0' - device reset, '1' - normal operation)
	P22	ENET_I2CMUX_SEL	Input	PD	NA	Signal Mux Control ('0' - No Connect , '1' - I2C0)
	P23	ENET_EXP_SPARE2	Input	NA	NA	Ethernet Expansion Spare2 ('0' - not defined, '1' - not defined)
	P24	M2PCIE_RTSZ	Output	PD	Active High	PCIE M.2 Reset ('0' - device reset, '1' - normal operation)
	P25	USER_INPUT1	Input	DIP_SEL	NA	User Dip Switch Input1 ('0' - User Define, '1' - User Define)
	P26	USER_LED1	Output	PD	Active High	User LED1 Enable ('1' - LED Off, '0' - LED On)
	P27	USER_LED2	Output	PD	Active High	User LED2 Enable ('1' - LED Off, '0' - LED On)
GPIO Expander - 3 Part# TCA6408ARGTR						
I2C3/0x20	P0	CODEC_RSTZ	Output	PD	Active low	Audio Codec Reset ('0' - device reset, '1' - normal operation)
	P1	CODEC_SPARE1	NA	UNUSED	NA	Not used (test point)
	P2	UB926_RESETN	Output	PD	Active low	Tuner Deserializer Reset ('0' - device reset, '1' - normal operation)
	P3	UB926_LOCK	Input	NA	NA	Tuner Deserializer Lock Status ('0' - Lock status, '1' - Lock status)
	P4	UB926_PWR_SW_CNTRL	Output	PD	NA	Tuner Board Power Enable ('0' - power off, '1' - power on)
	P5	UB926_TUNER_RESET	Output	PD	Active low	Tuner Device Reset ('0' - device reset, '1' - normal operation)
	P6	UB926_GPIO_SPARE	Output	PD	NA	Tuner Device Spare ('0' - TBD, '1' - TBD)
I2C1/0x20	P7	UNUSED	NA	NA	NA	No Connect
	GPIO Expander - 4 Part# TCA6408ARGTR					
	P0	DPO_PWR_SW_EN	Output	PD	Active High	DisplayPort0 Power Enable ('0' - power off, '1' - power on)
	P1	DP1_PWR_SW_EN	Output	PD	Active High	DisplayPort1 Power Enable ('0' - power off, '1' - power on)
	P2	UB981_PDB	Output	PD	Active low	DSI Display Power Down/Reset ('0' - device powerdown/reset, '1' - normal operation) Note: Resistor option to DSI_DISP_RSTz
	P3	UB981_GPIO0	Output	NA	NA	Display Dependent. Backlight Enable ('0' - power off, '1' - power on)
	P4	UB981_GPIO1	Output	NA	NA	Display Dependent. Spare
	P5	UB981_GPIO2	Input	NA	NA	Display Dependent. Spare
I2C6/0x20	P6	UB981_GPIO3	Input	NA	NA	Display Dependent. Interrupt ('0' - interrupt pending, '1' - no interrupt)
	P7	PWR_SW_CNTL_DSI0	Output	PD	Active High	Display Panel Power Enable ('0' - power off, '1' - power on)
	GPIO Expander - 5 Part# TCA6408ARGTR					
	P0	CSI2_EXP_RSTZ	Output	PD	Active low	CSI2 Expansion Interface Reset ('0' - device reset, '1' - normal operation)
	P1	CSI2_EXP_A_GPIO0	IO	NA	NA	CSI2 Expansion Board Specific. MV - Used for CSI0_FLASH_EN; LI - Used for CSI1_GPIO2
	P2	CSI2_EXP_A_GPIO1	IO	NA	NA	CSI2 Expansion Board Specific. MV - Used for CSI1_FLASH_EN; LI - Used for CSI0_GPIO1/CSI1_GPIO1
	P3	CSI2_EXP_A_GPIO3	IO	NA	NA	CSI2 Expansion Board Specific. MV - Not used; LI - Used for CSI0_GPIO2
	P4	CSI2_EXP_B_GPIO1	IO	NA	NA	CSI2 Expansion Board Specific. MV - Not used; LI - Used for CSI2_GPIO1
	P5	CSI2_EXP_B_GPIO2	IO	NA	NA	CSI2 Expansion Board Specific. MV - CSI2_XTRIG; LI - Used for CSI2_GPIO0
	P6	CSI2_EXP_B_GPIO3	IO	NA	NA	CSI2 Expansion Board Specific. MV - Not used; LI - Used for CSI2_GPIO2
	P7	CSI2_EXP_B_GPIO4	IO	NA	NA	CSI2 Expansion Board Specific. MV - Not used; LI - Not used

NOTE:EXP_ENET_RSTz Signal Default state changed to Pull down in REV E3

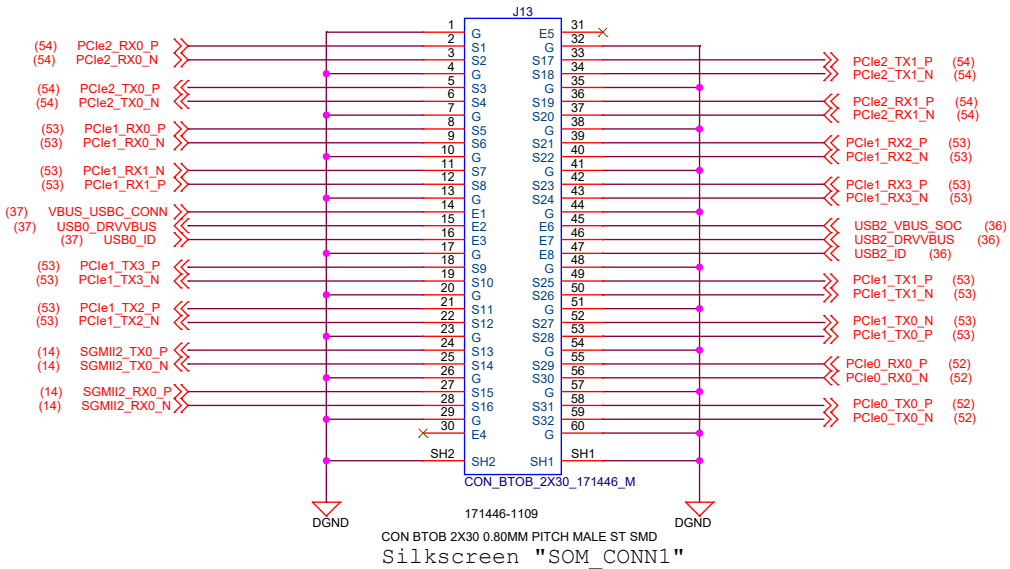
Project : J7 EVM		Title GPIO EXPANDER MAP/TABLE	
		Size C	Rev A
		Date: Friday, December 03, 2021	
		Sheet 8 of 68	

SOM B-B MOLEX CONNECTORS

PCIe M.2

PCIe x4 Lane & USBC

SGMII



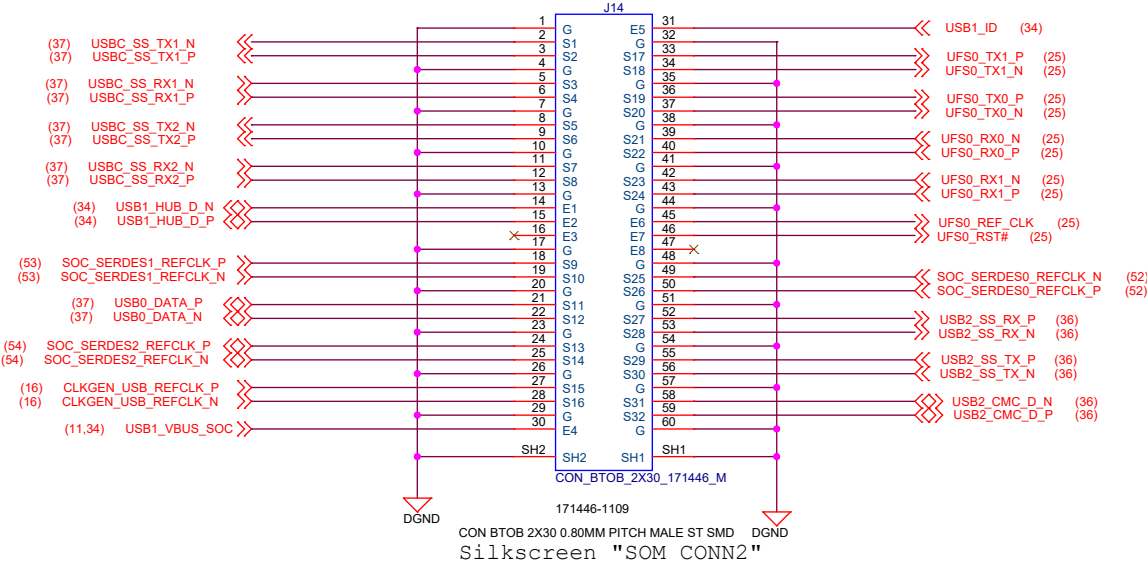
PCIe M.2

PCIe x4 Lane & USB2

PCIe x1 Lane

USB TYPE C

USB1 --> HUB



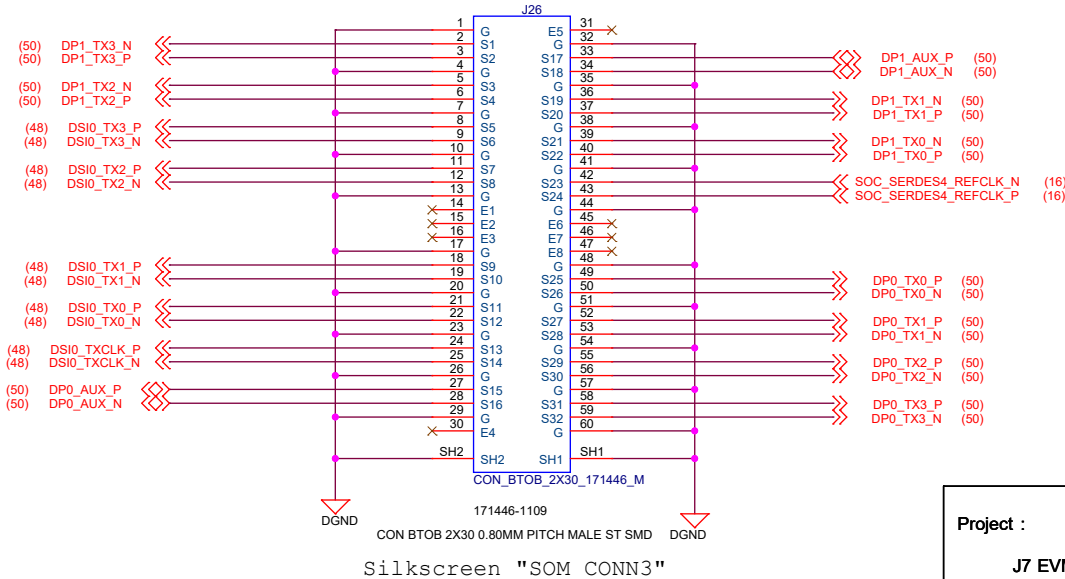
UFS

USB2 --> 3.0 uAB

DP1

DSIO

DP0



DP1

DP0

Project :

J7 EVM



Title
SOM B-B MOLEX CONNECTORS

Size
C
PROC079 001 J721EXCP01EVM

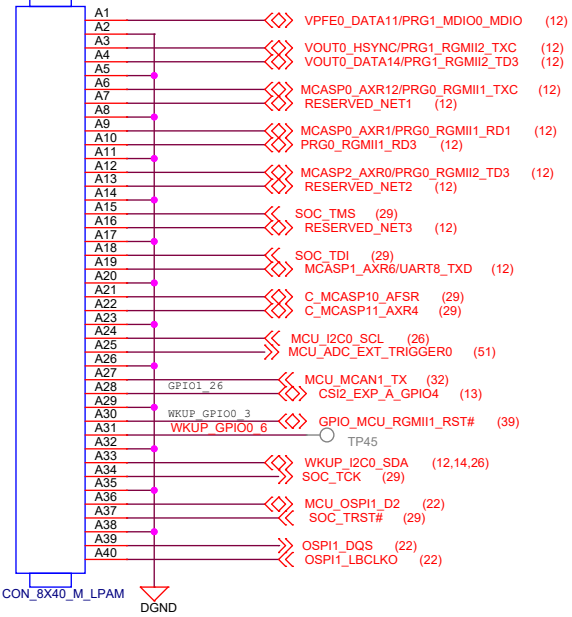
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Sheet 9 of 68

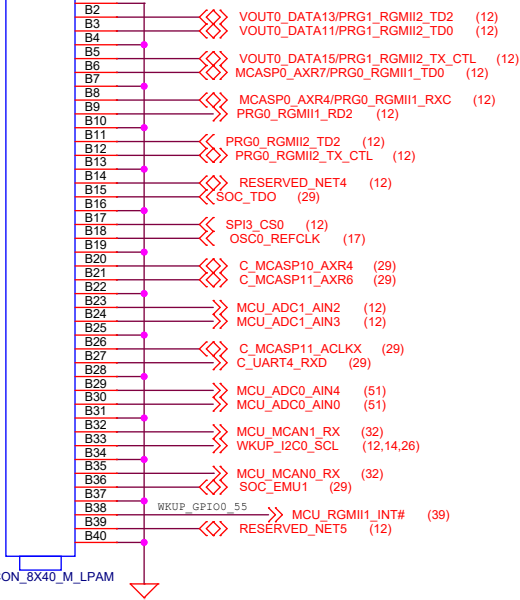
Rev
A

SOM B-B SAMTEC CONN#1

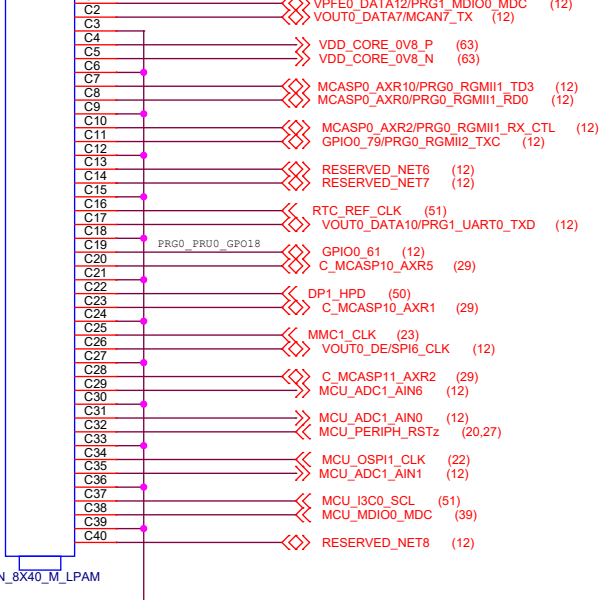
J19A



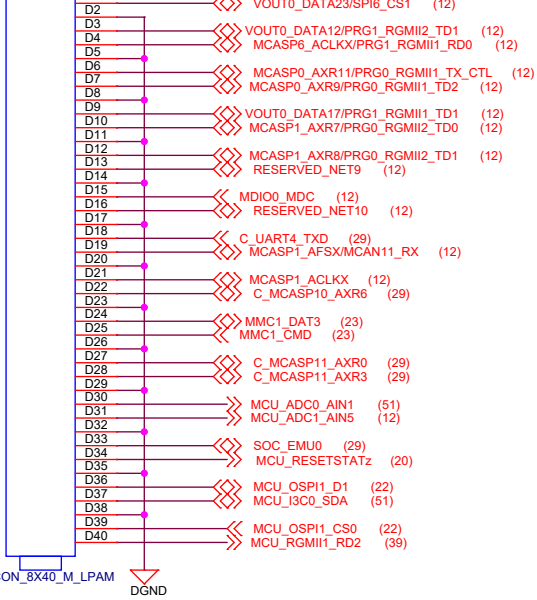
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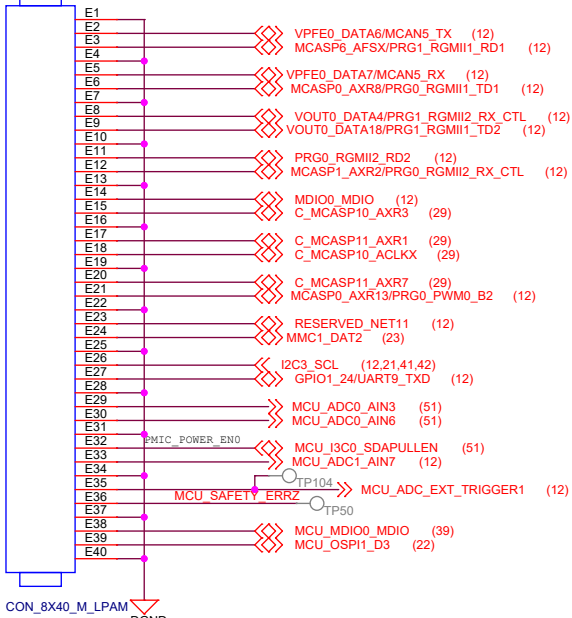
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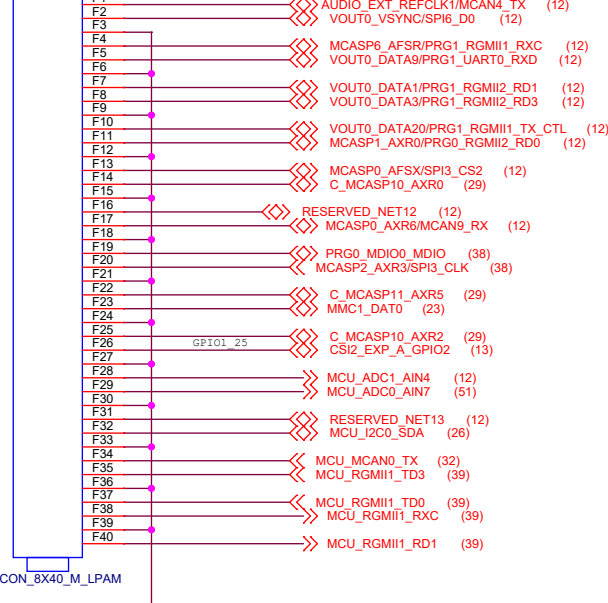
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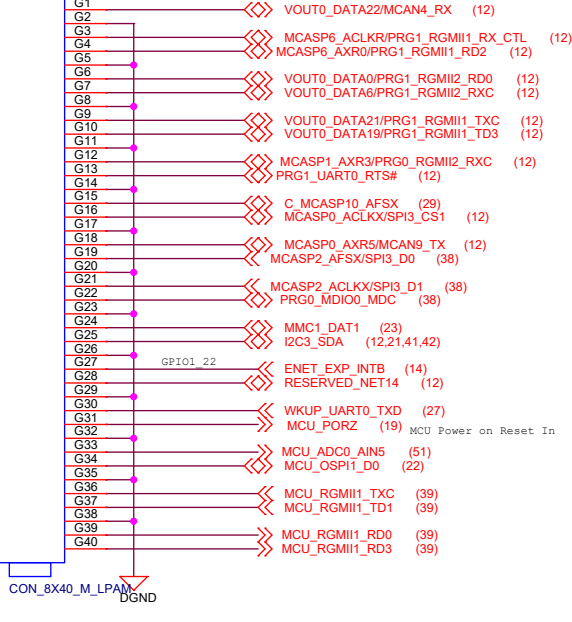
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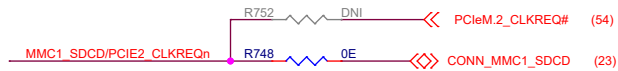
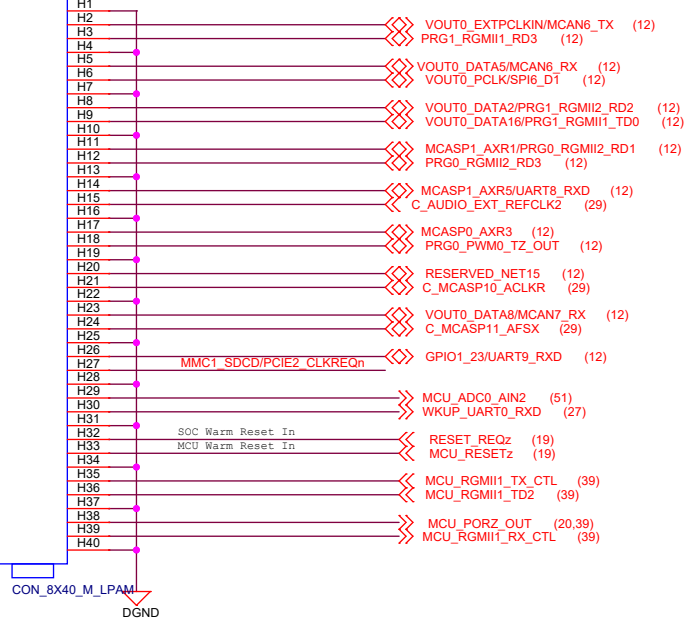
J19F



J19G



J19H

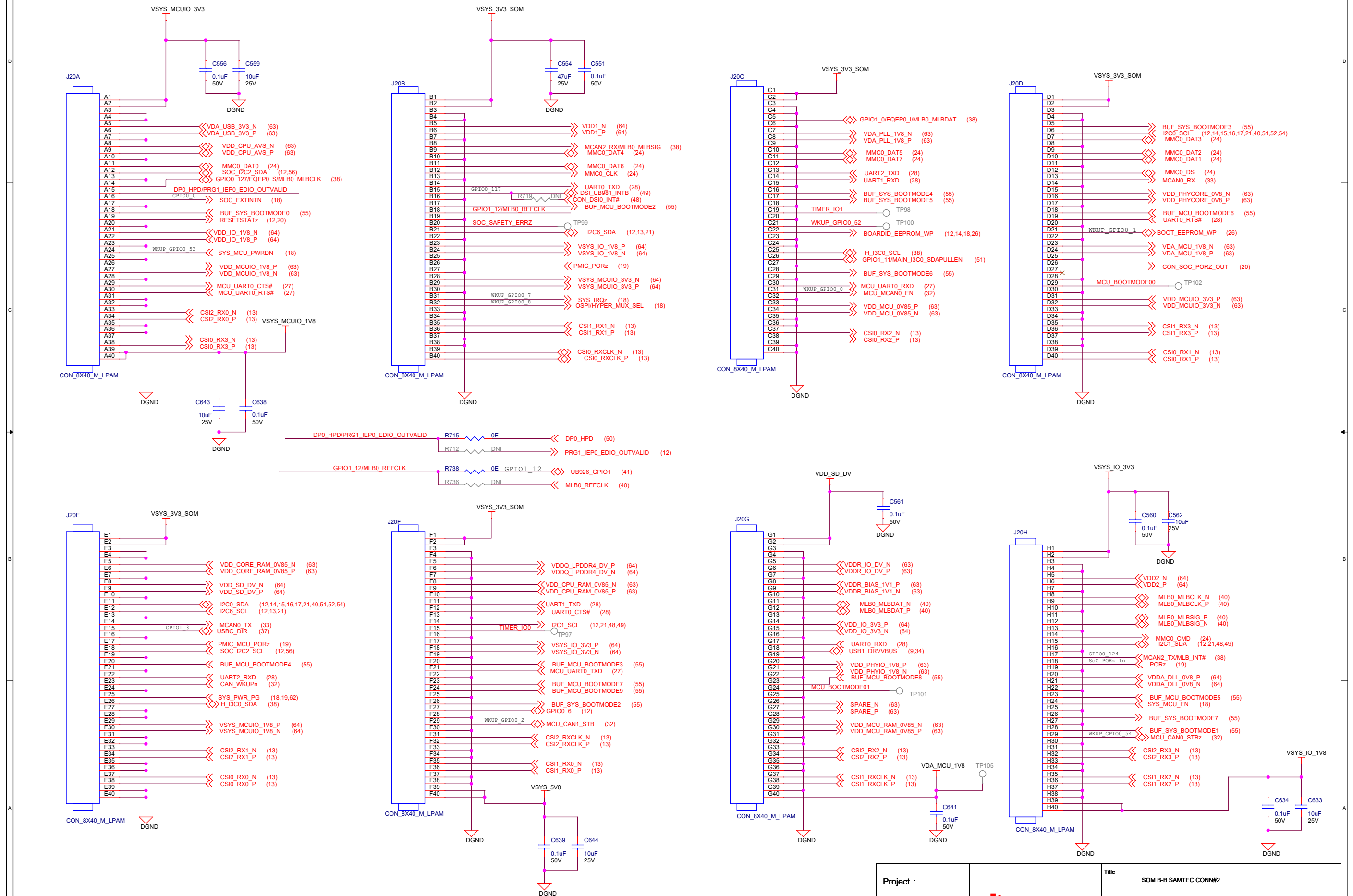


Project :
J7 EVM

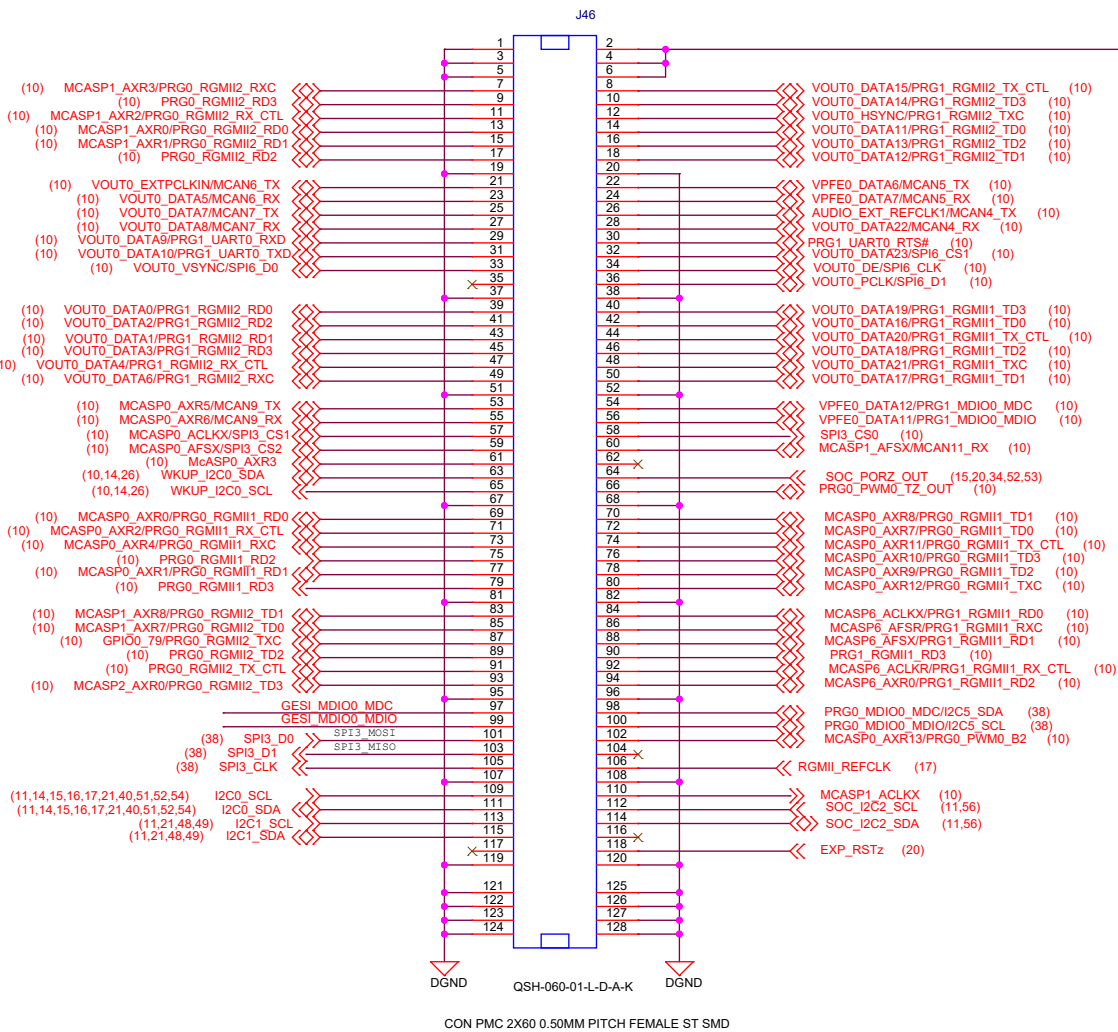


Title		
SOM B-B SAMTEC CONN#1		
Size	Rev	
C	A	
Date:		Sheet
Friday, December 03, 2021		10 of 68

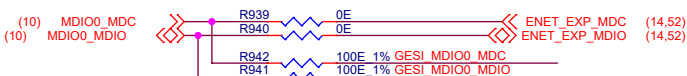
SOM B-B SAMTEC CONN#2



INFO/GESI EXP CONN

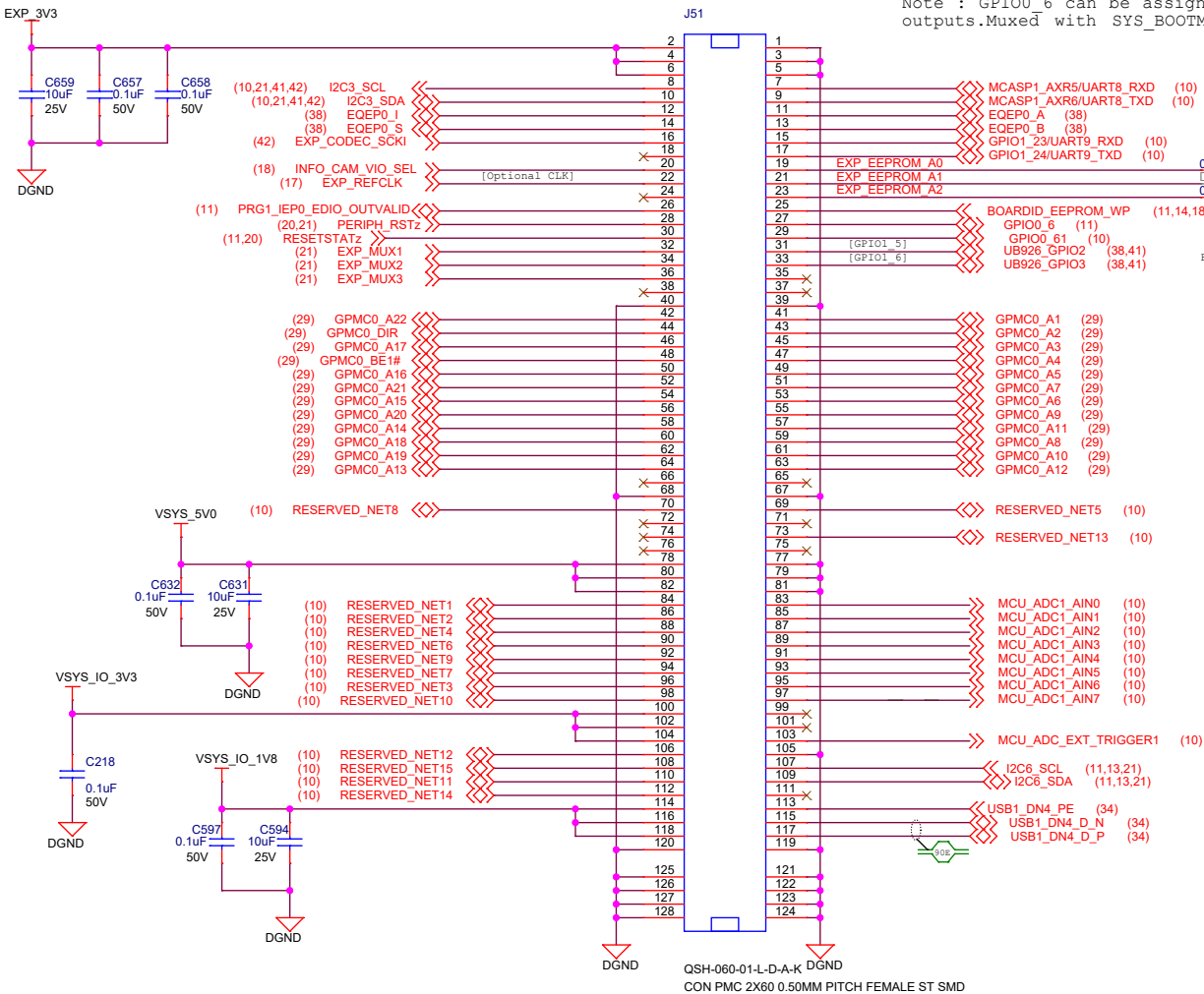


CON PMC 2X60 0.50MM PITCH FEMALE ST SMD




NOTE:Keep this Resistors close to J46

Silkscreen "EVM EXPANSION"

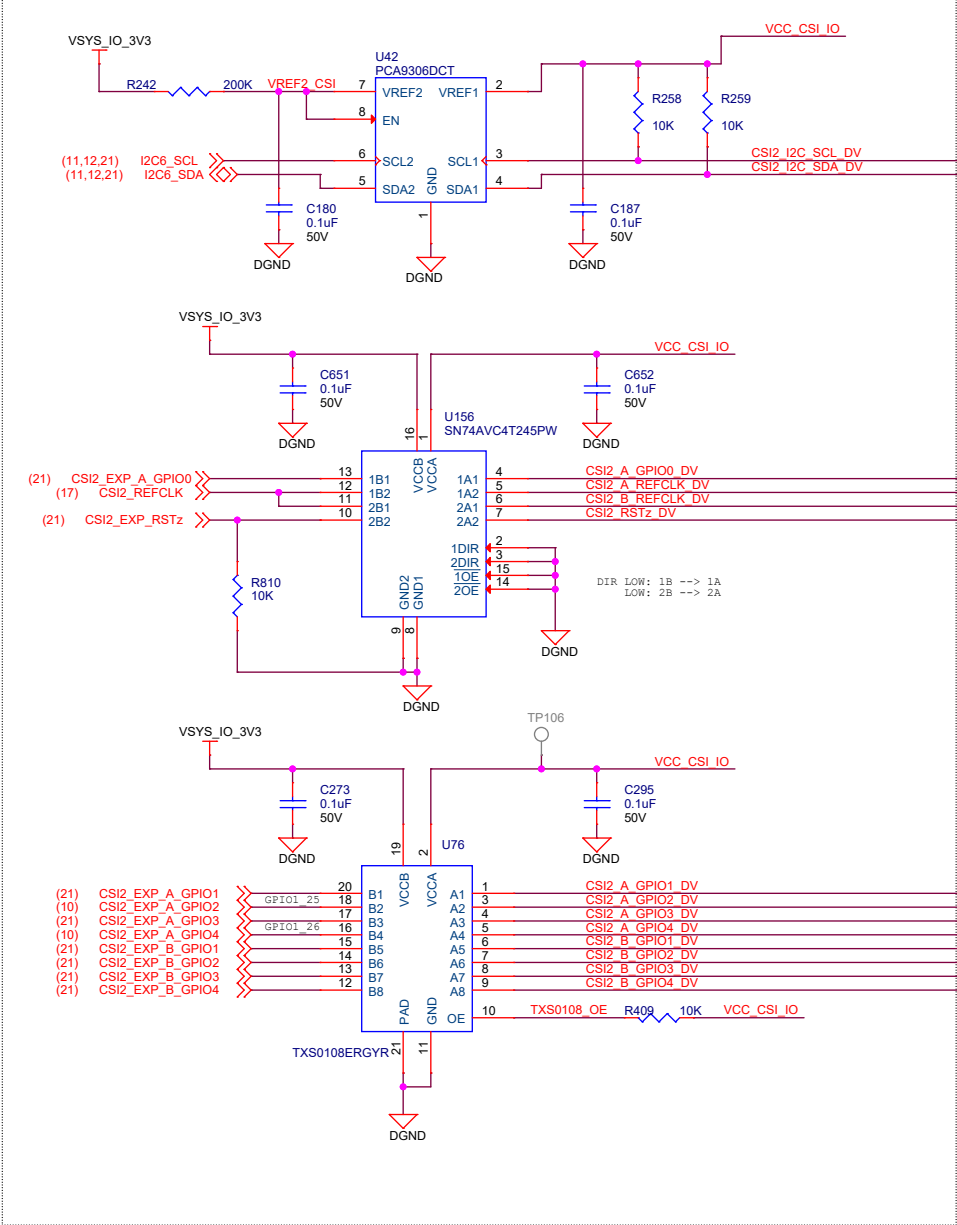


Note : GPIO0_6 can be assigned only as outputs.Muxed with SYS BOOTMODE

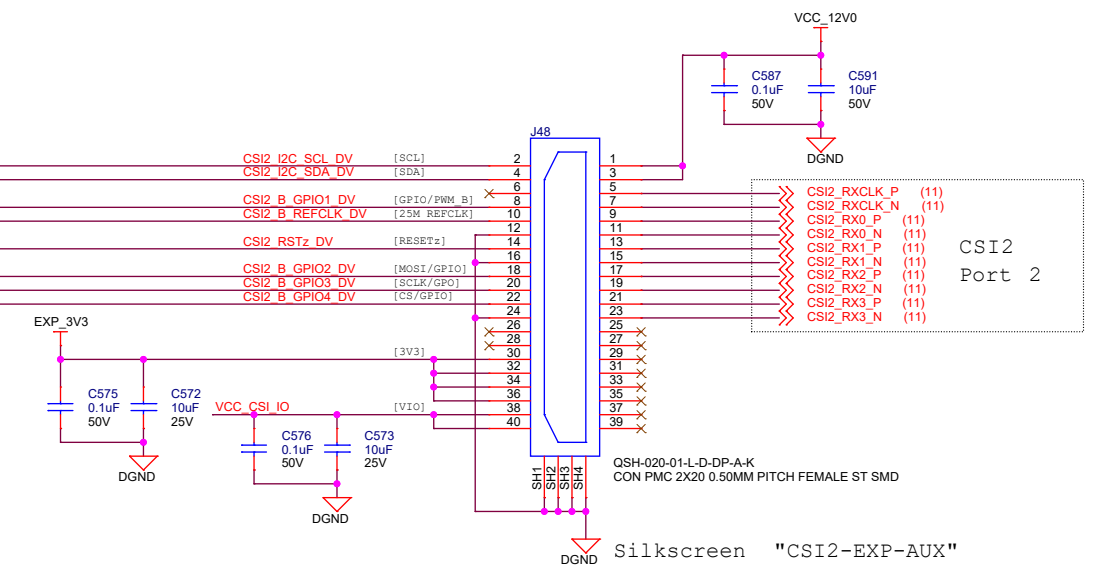
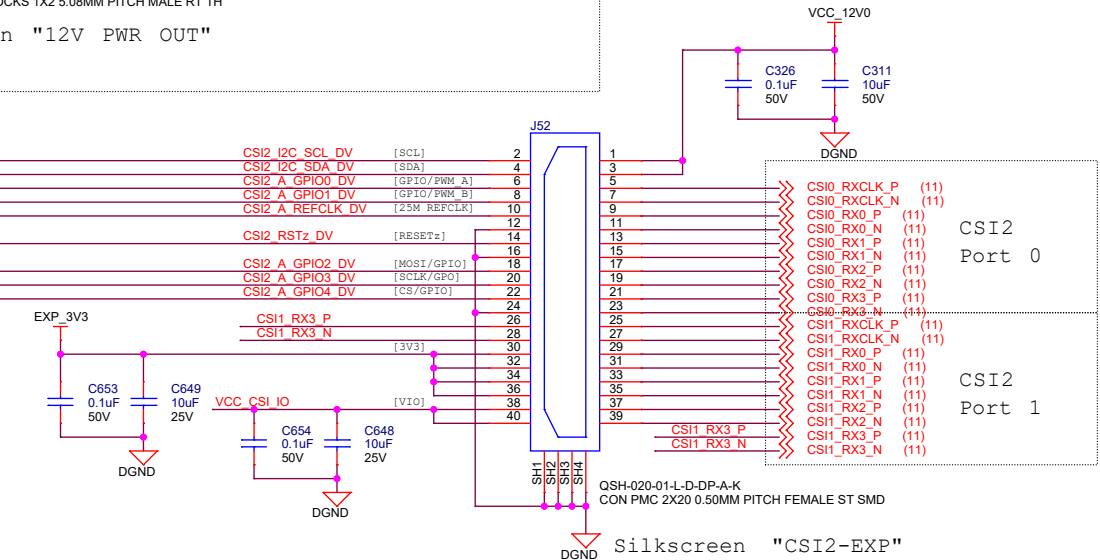
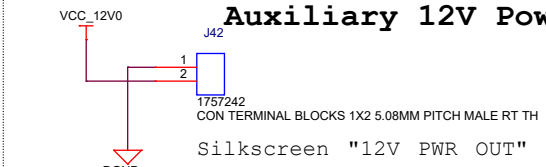
Project : J7 EVM		Title INFO/GESI_EXP_CONN			
		Size	PROC079 001 J721EXCP01EVM		Re
		C			A
		Date:	Friday, December 03, 2021	Sheet	12 of 68

CSI2 EXPANSION CONNECTORS

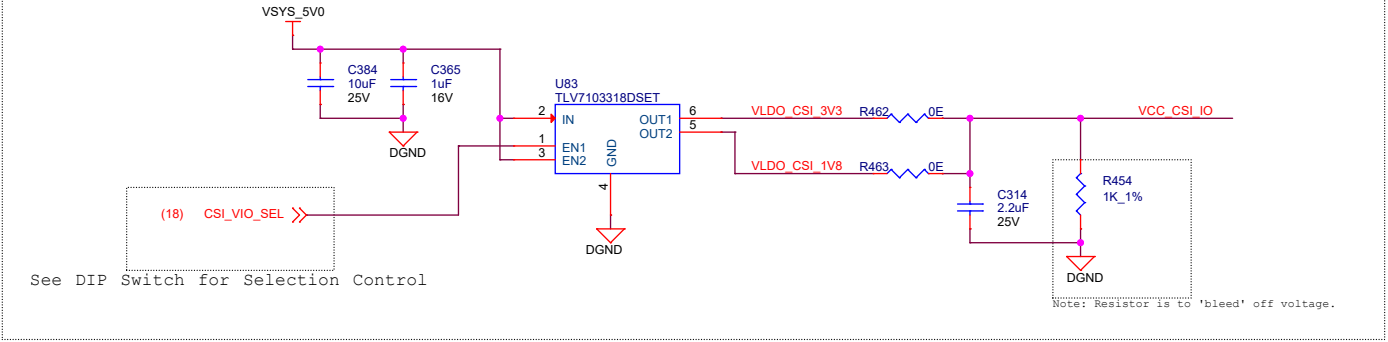
Level Translation for LVCMOS



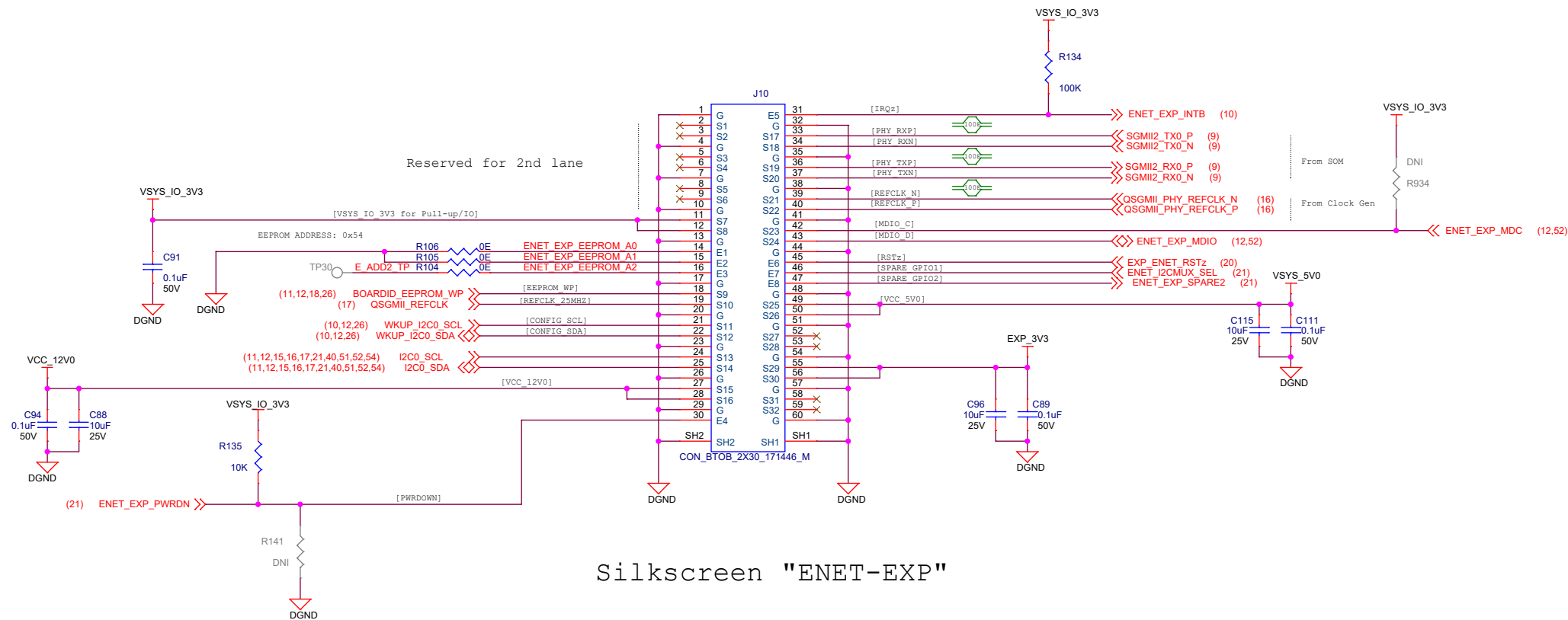
Auxiliary 12V Power Output for CSI2



LVCMOS IO Voltage Selection

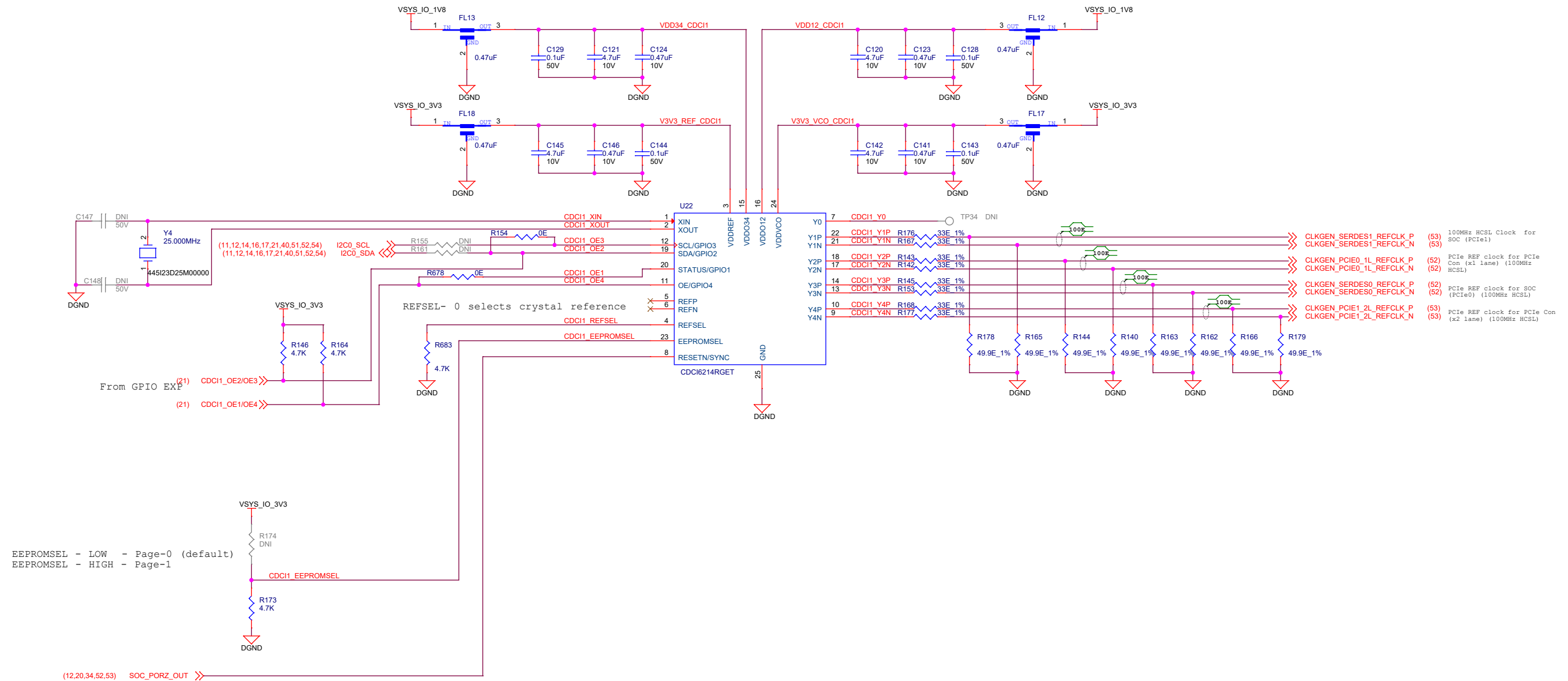


ENET EXPANSION CONNECTOR

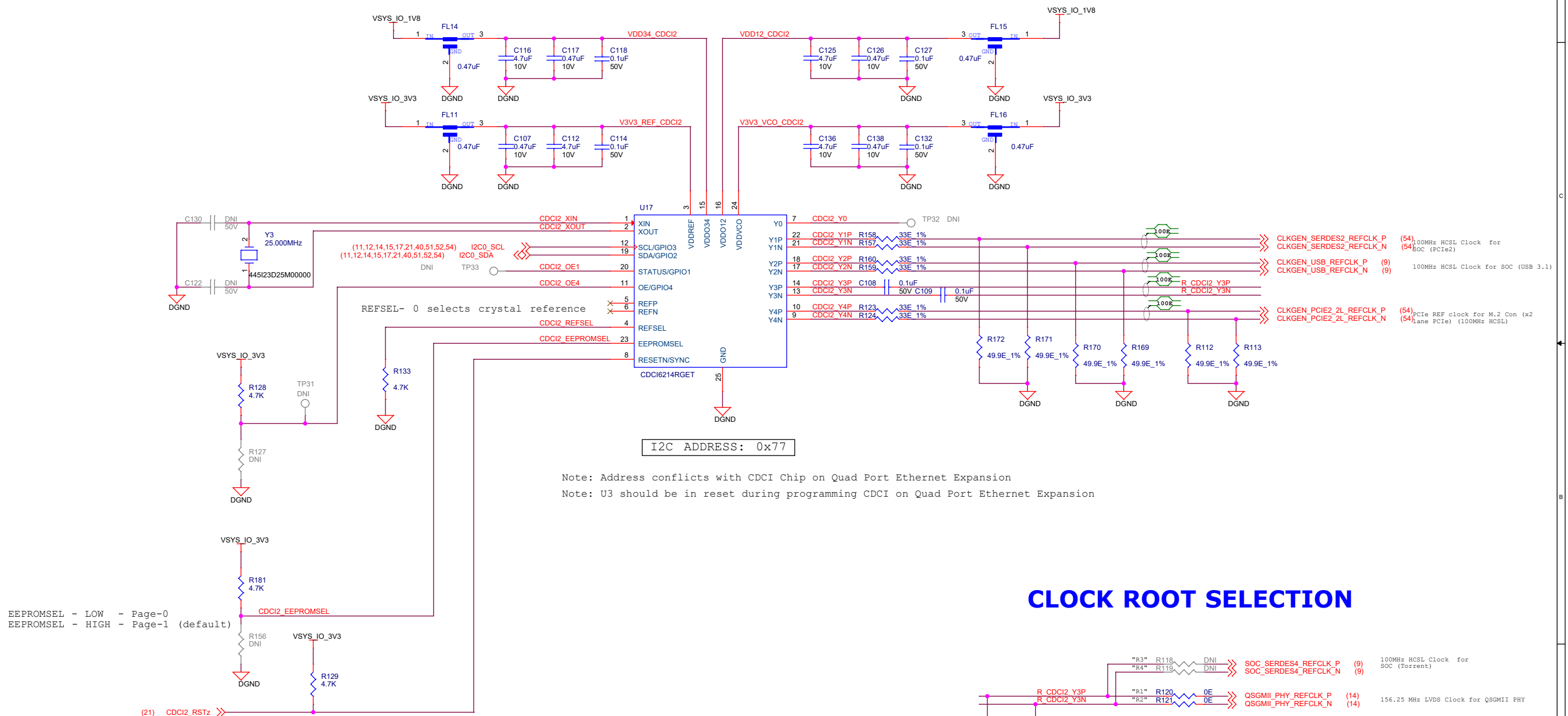


Silkscreen "ENET-EXP"

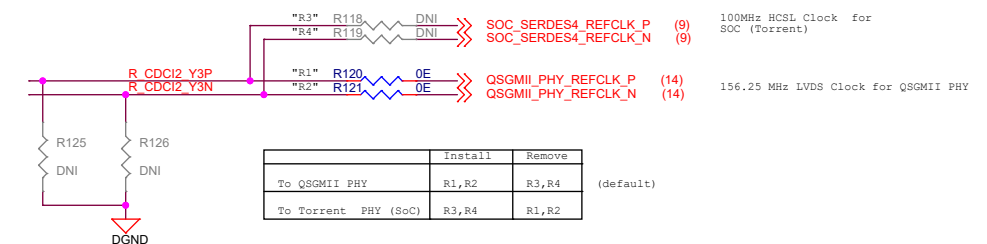
SERDES CLOCK GENERATOR #1



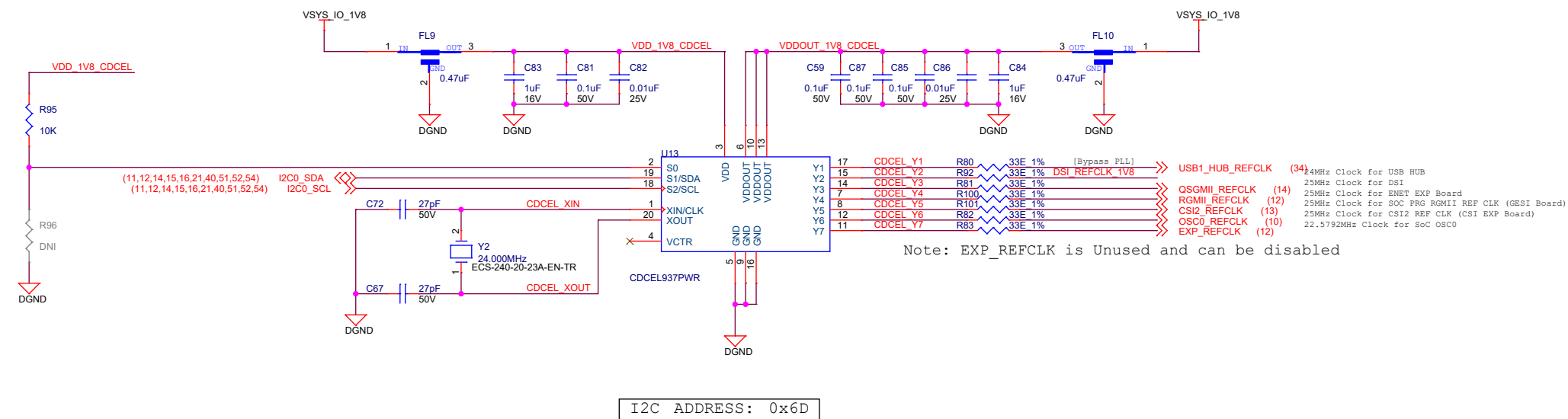
SERDES CLOCK GENERATOR #2



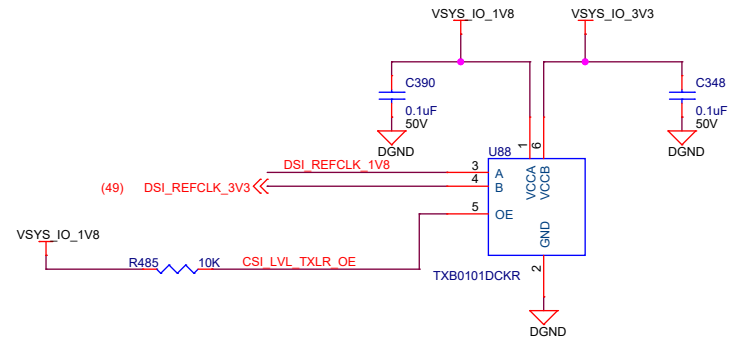
CLOCK ROOT SELECTION



PERIPHERAL CLOCK GENERATOR

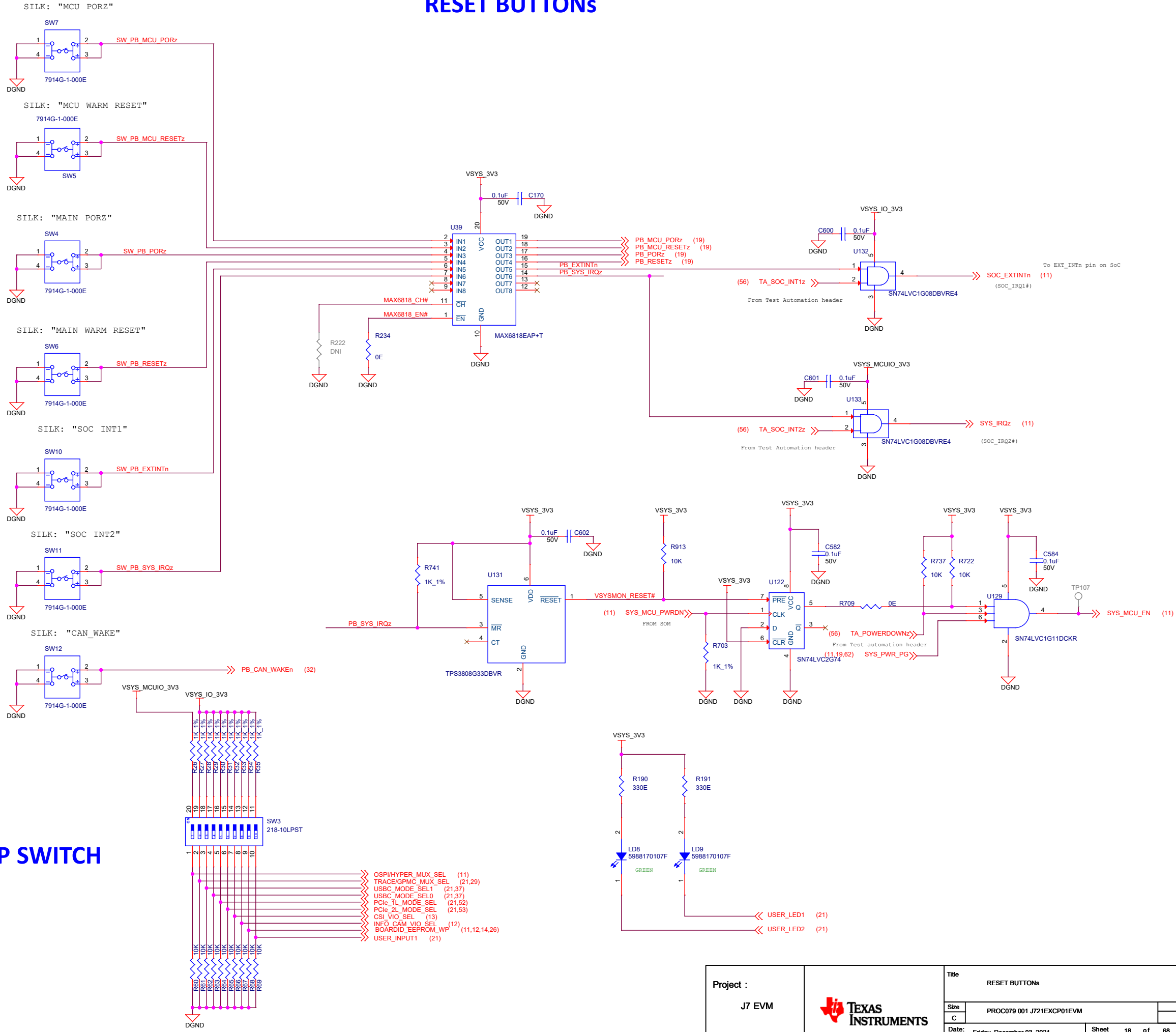


Level Translator for DSI REFCLK



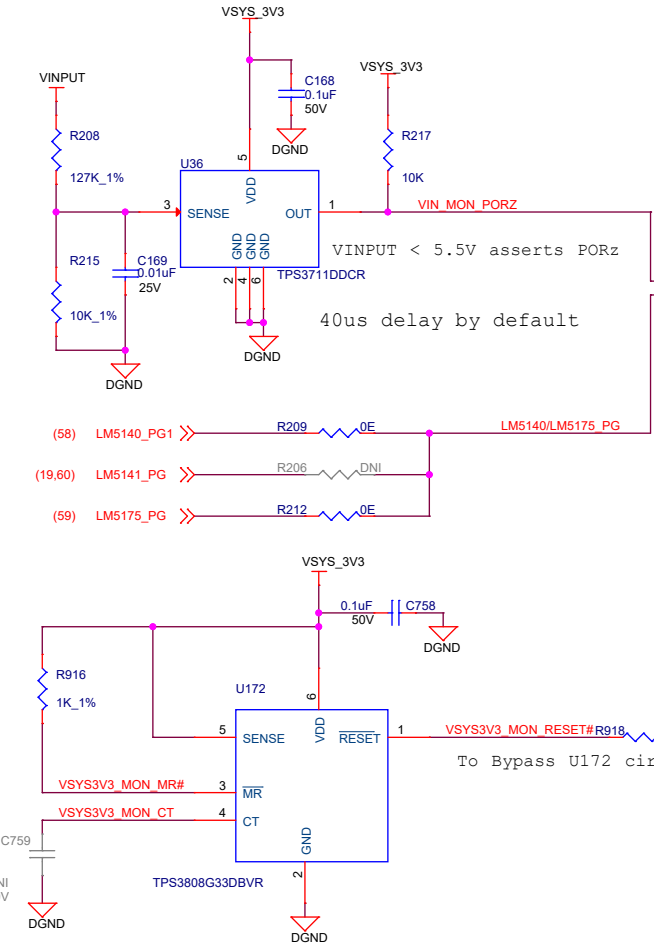
RESET BUTTONs

CONFIG DIP SWITCH

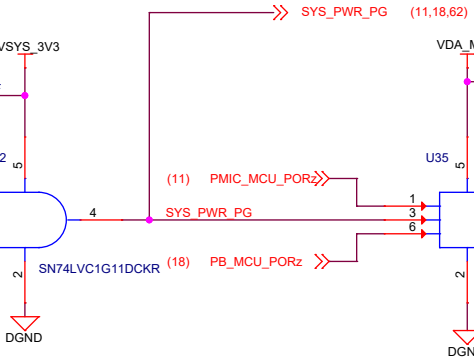


RESET INPUTS

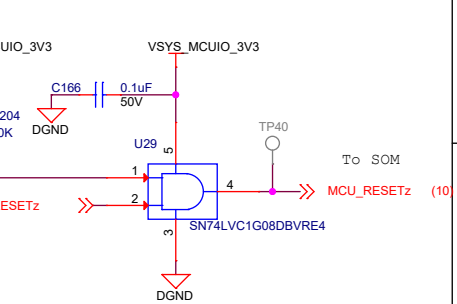
Under Voltage Monitor (VINUT)



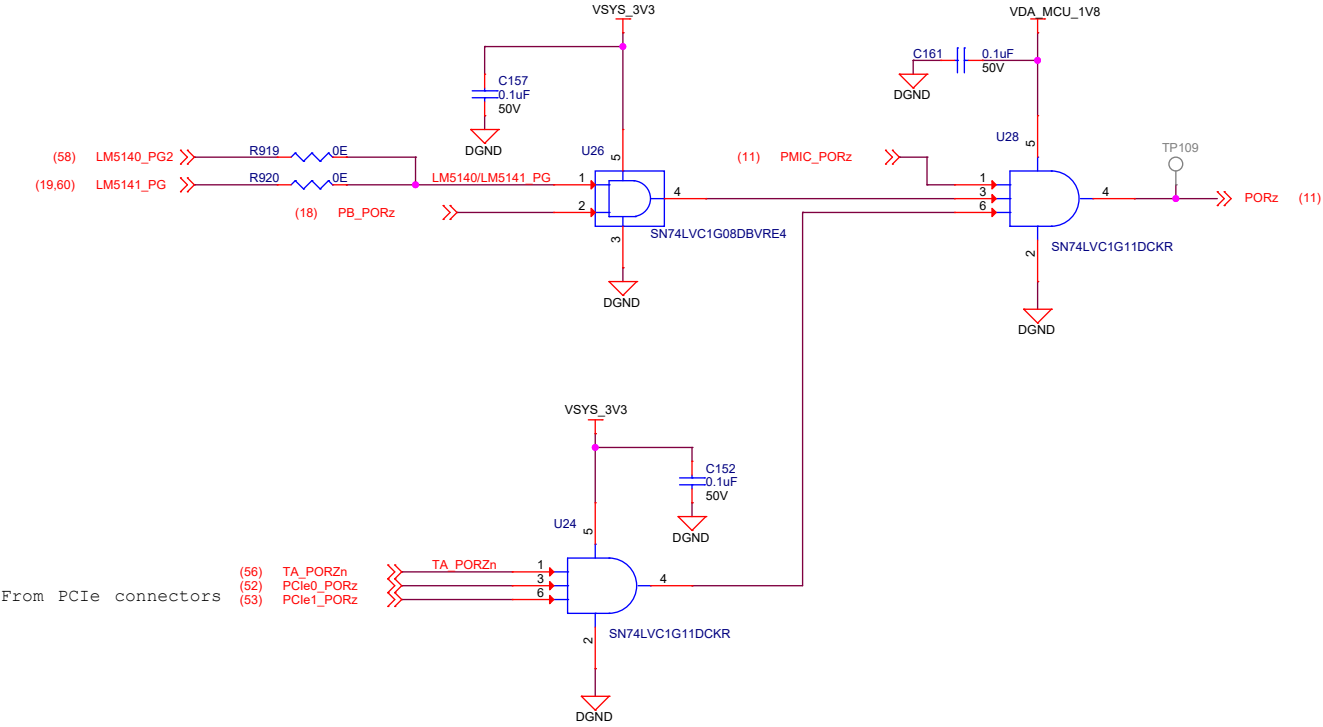
MCU PORz



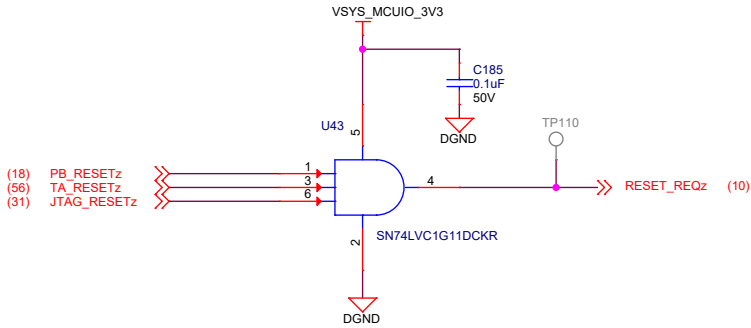
MCU_RESET



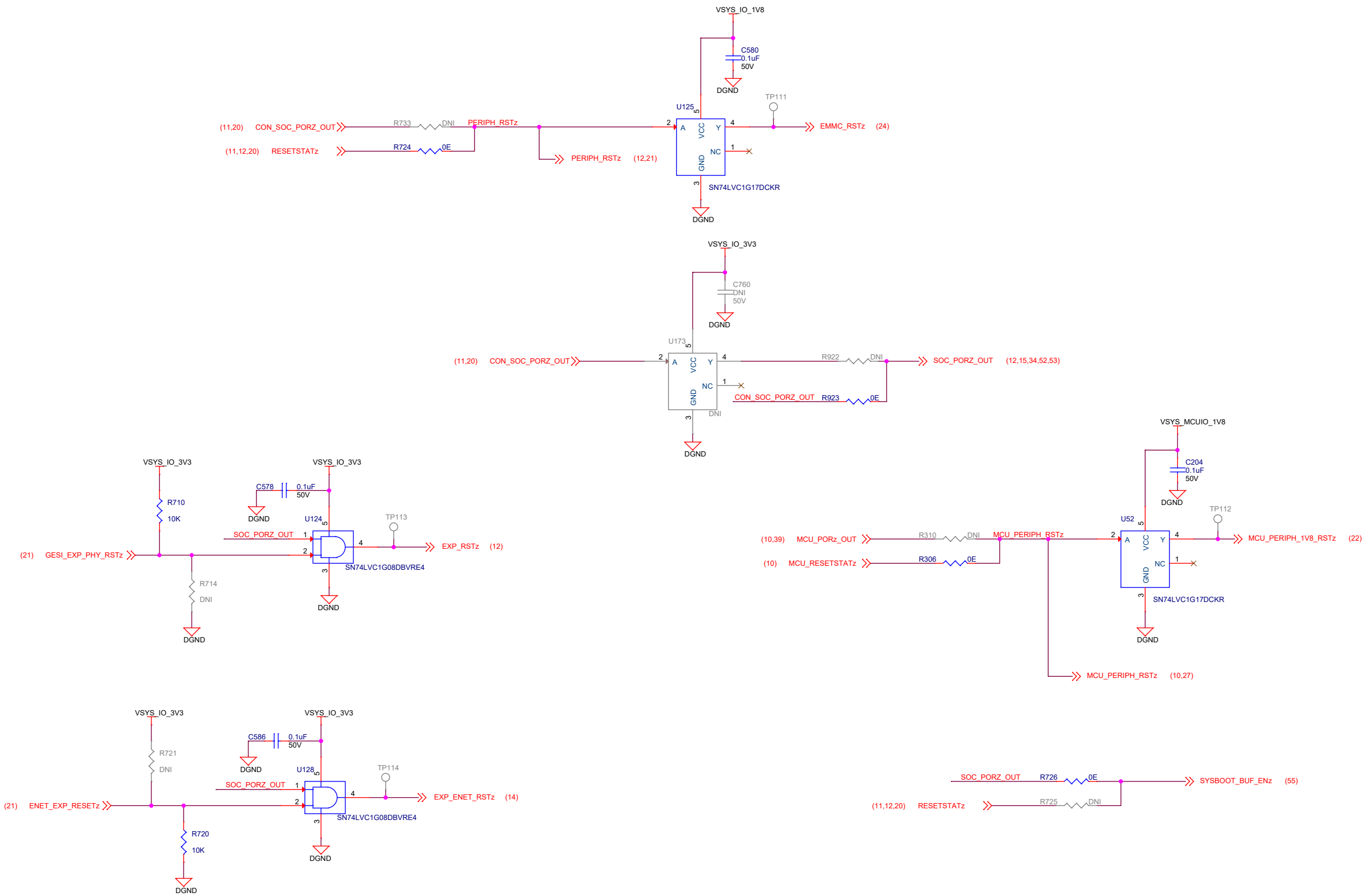
SOC PORz



SOC RESET

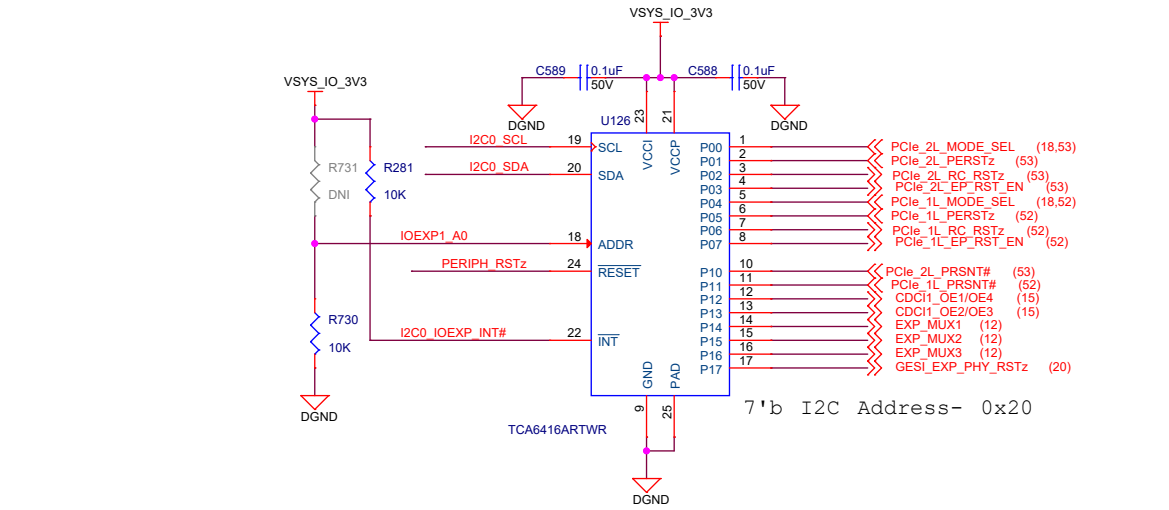


RESET OUTPUTS

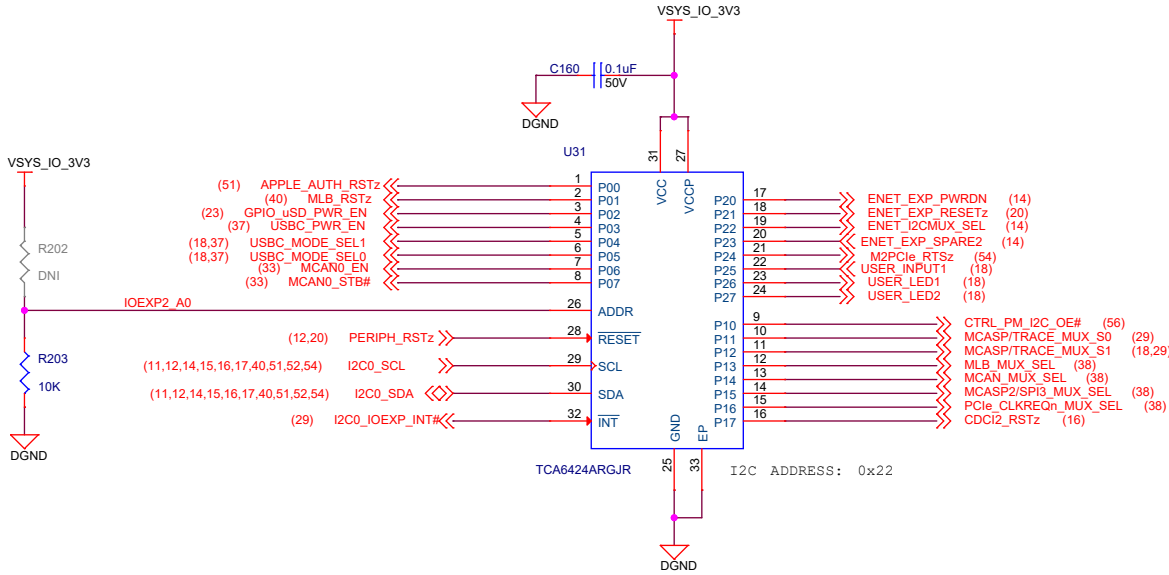


GPIO EXPANDERS

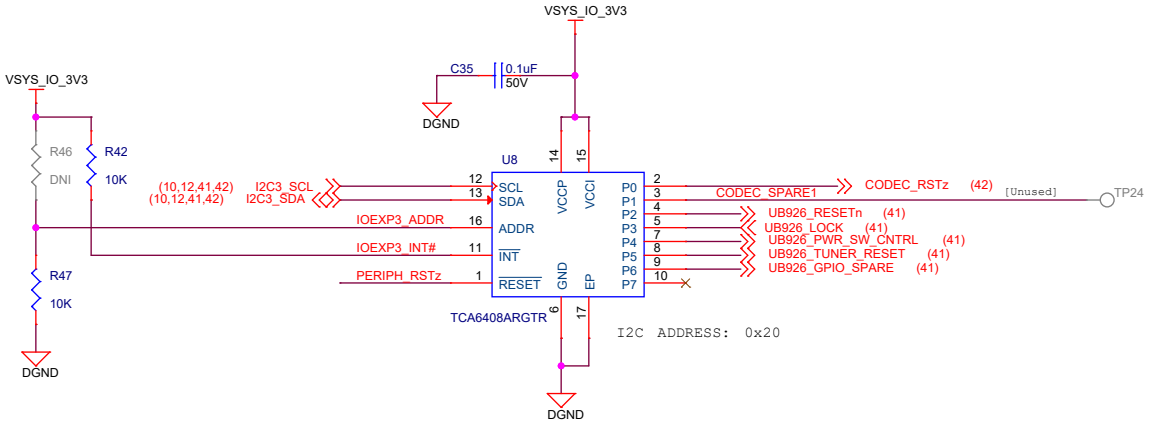
I2C GPIO EXPANDER1



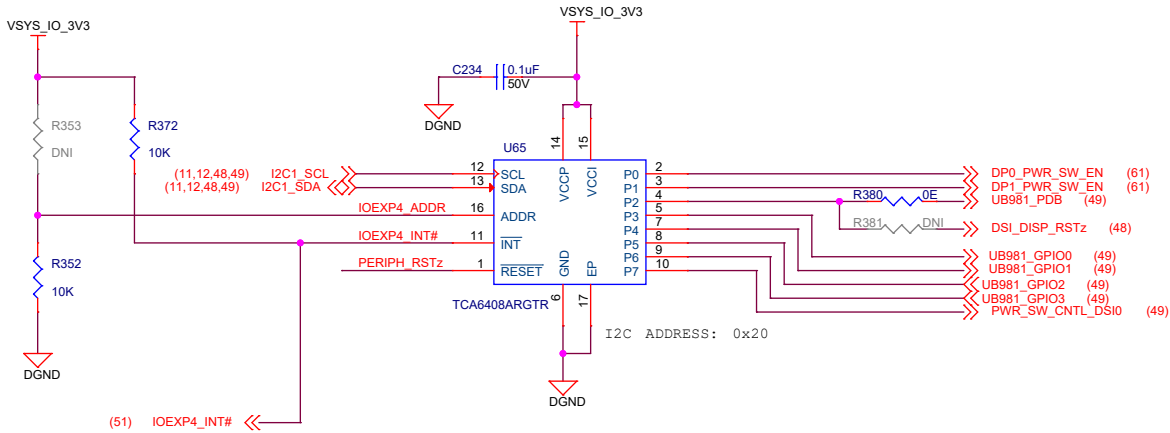
I2C GPIO EXPANDER2



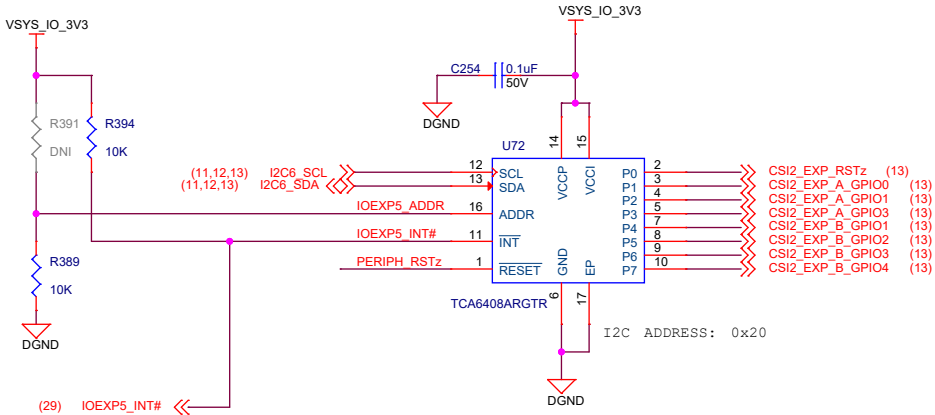
I2C GPIO EXPANDER3



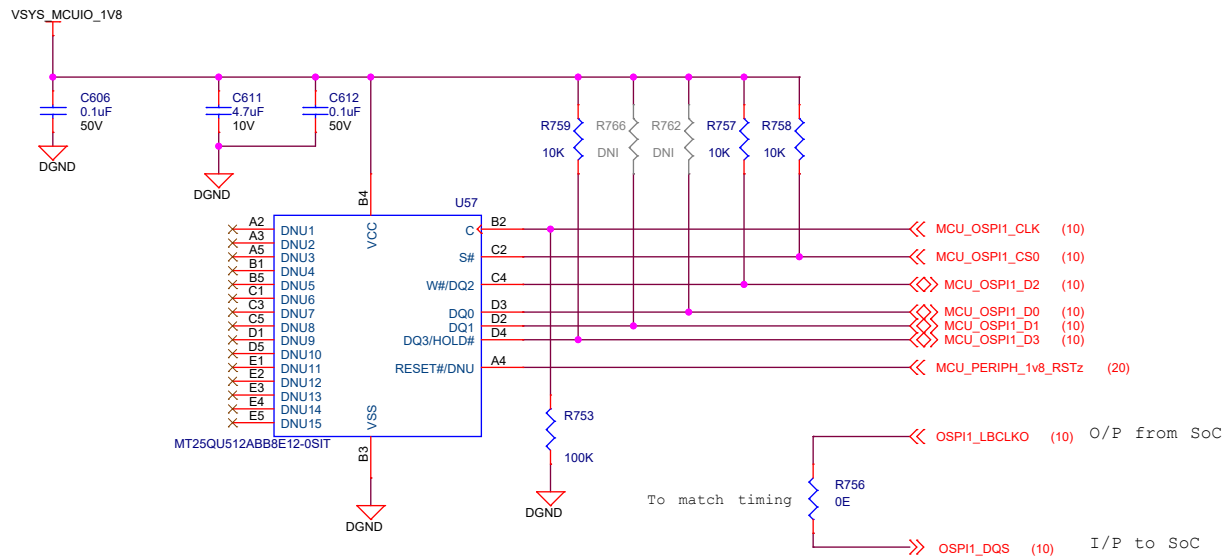
I2C GPIO EXPANDER4



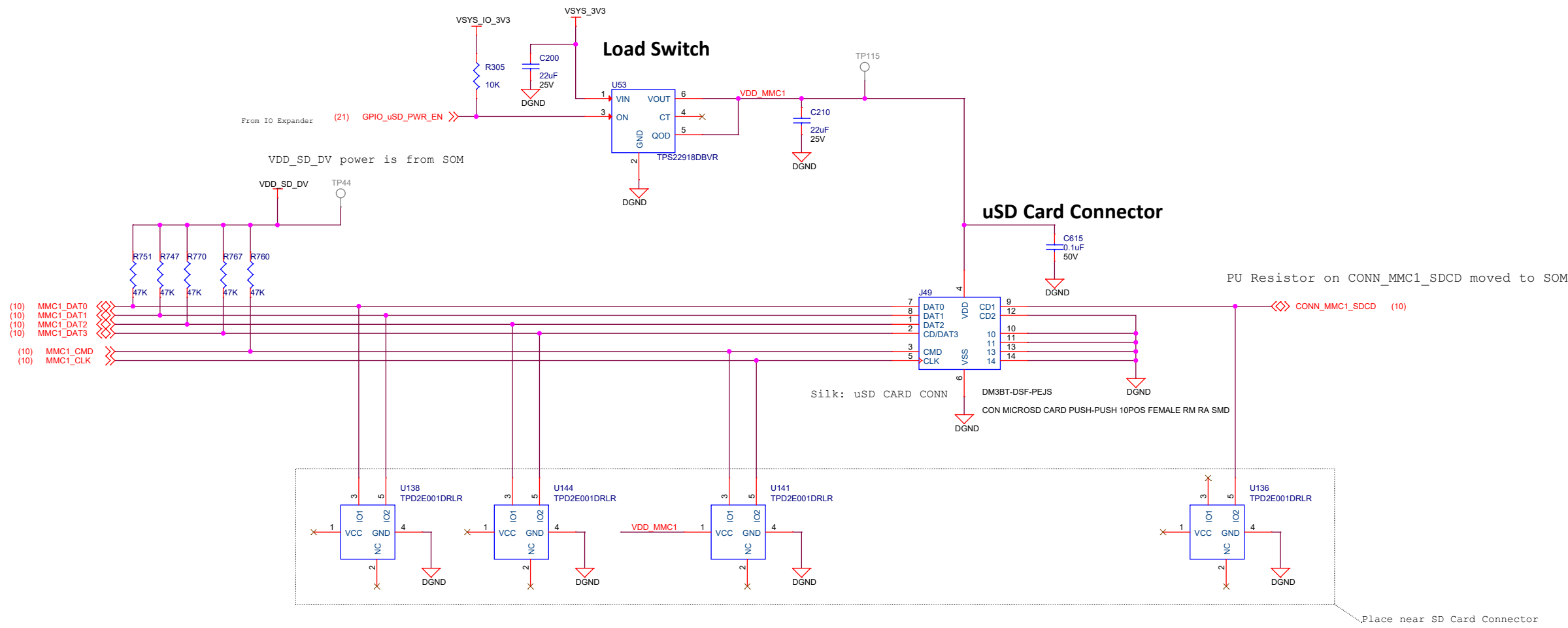
I2C GPIO EXPANDERS



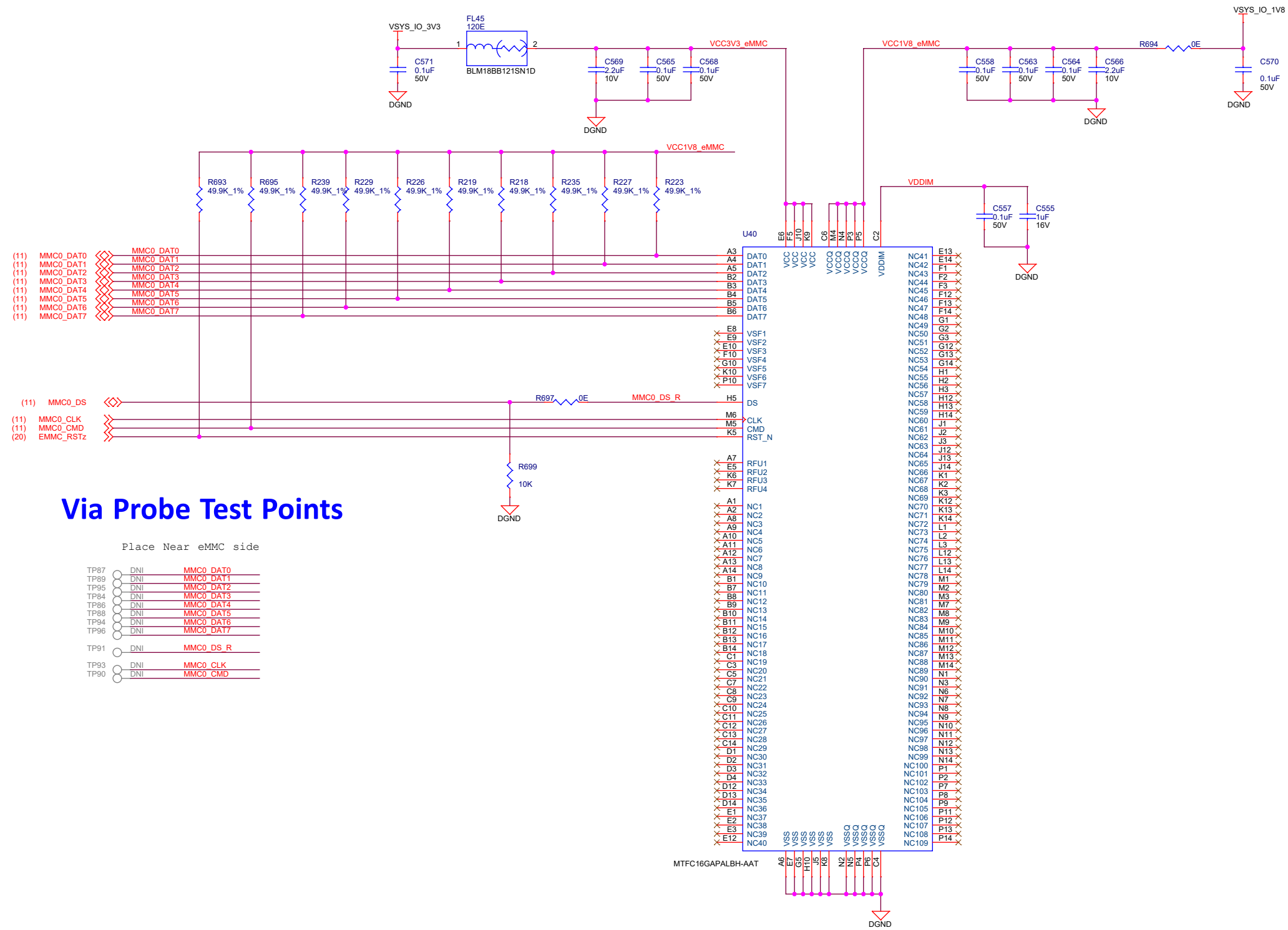
SPI NOR Flash



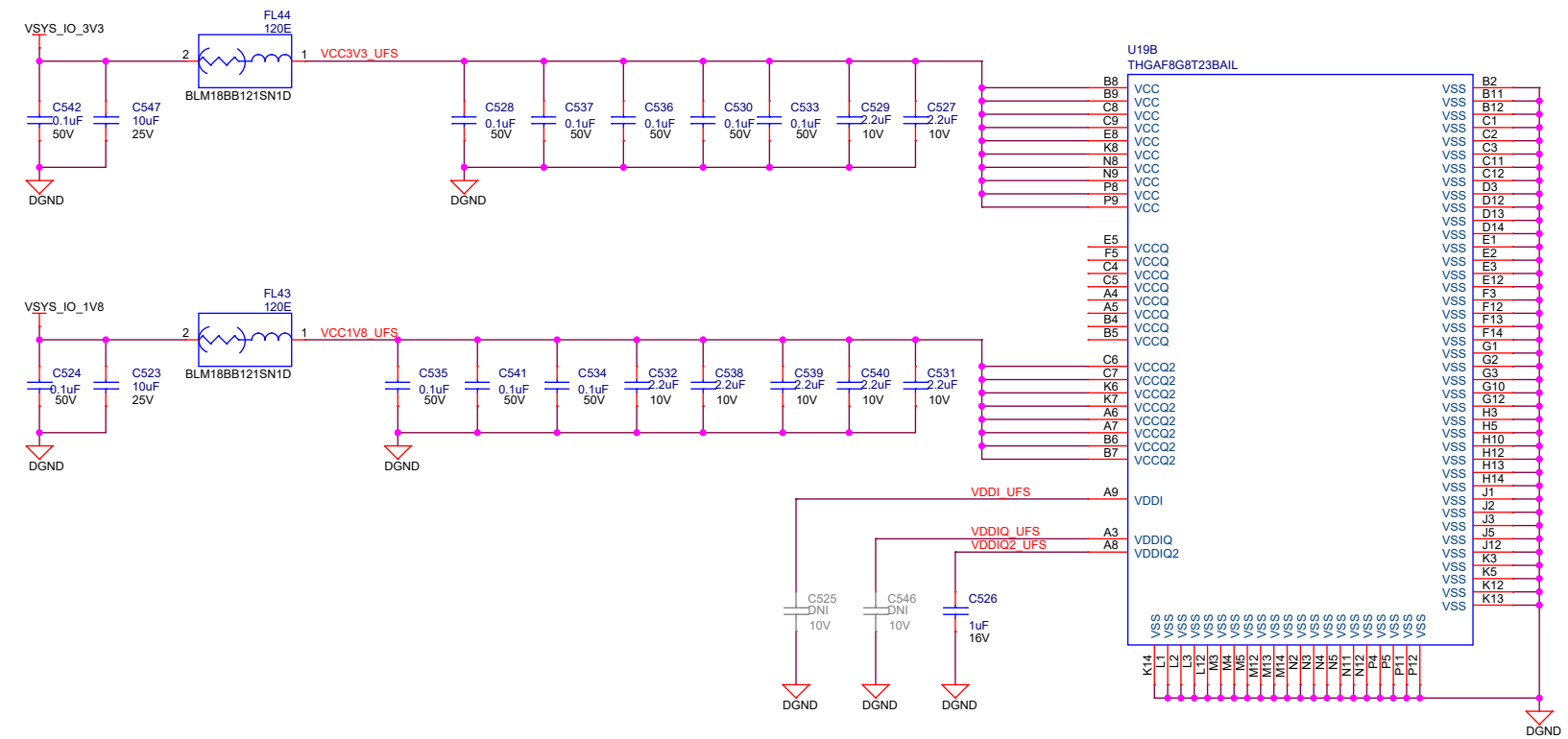
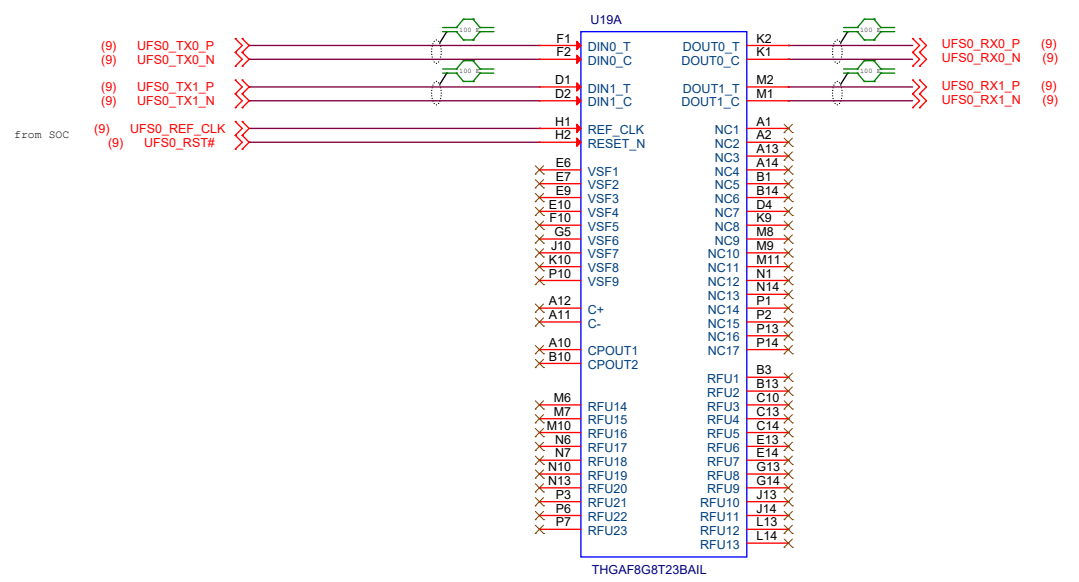
Micro SD CARD INTERFACE



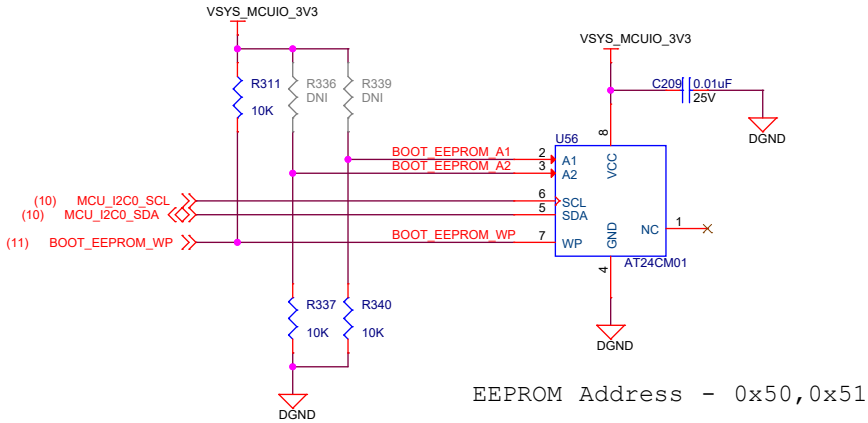
eMMC FLASH



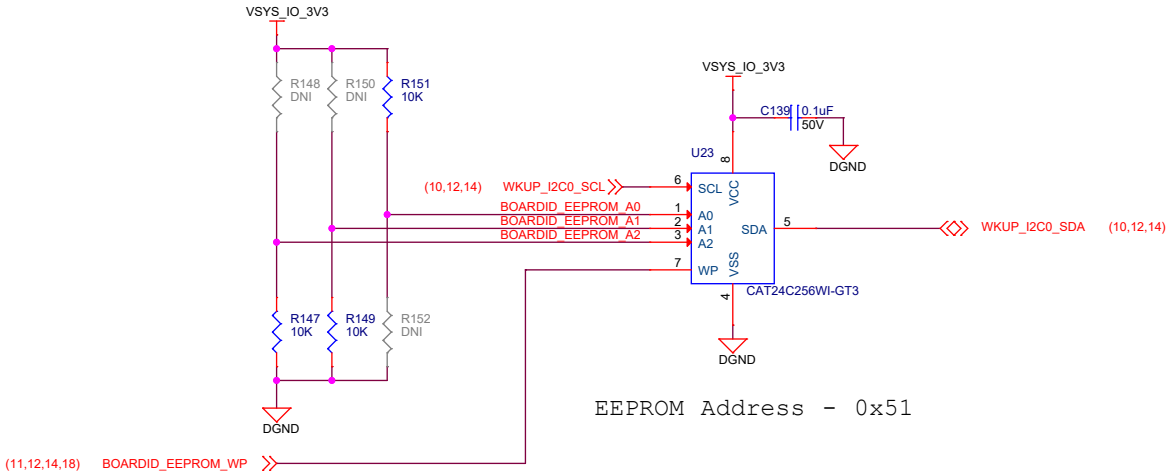
UFS FLASH



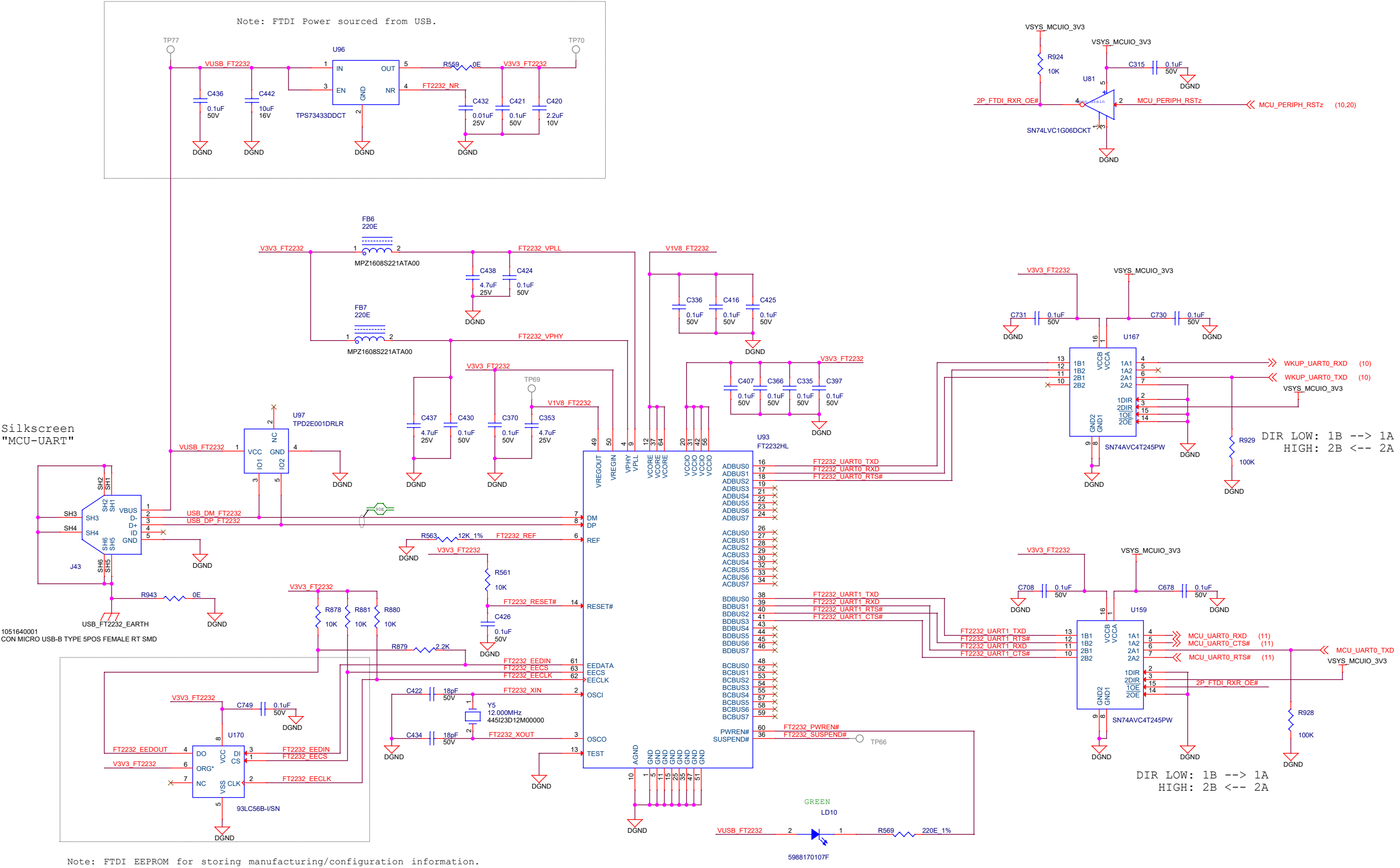
BOOT EEPROM



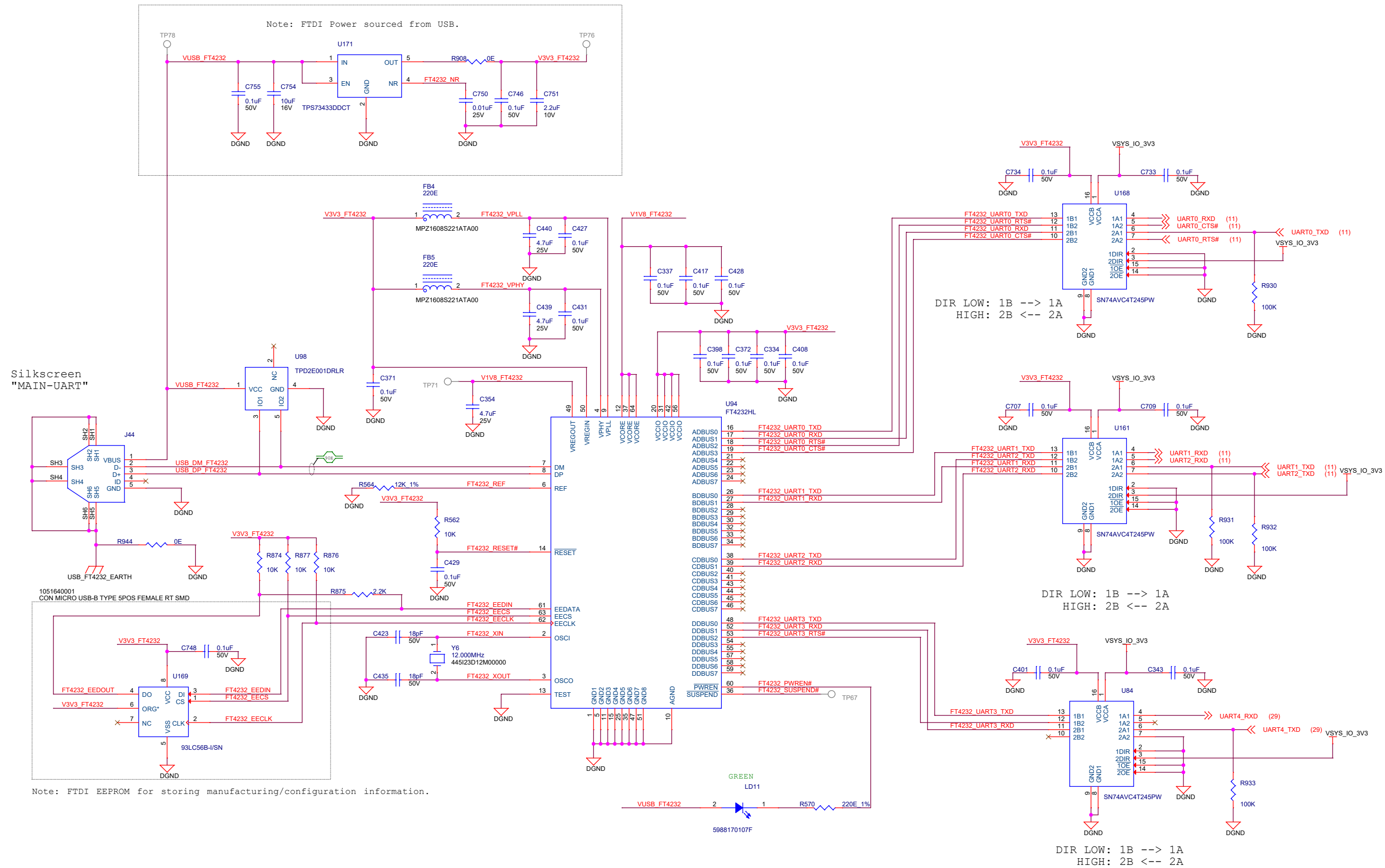
BOARD ID EEPROM



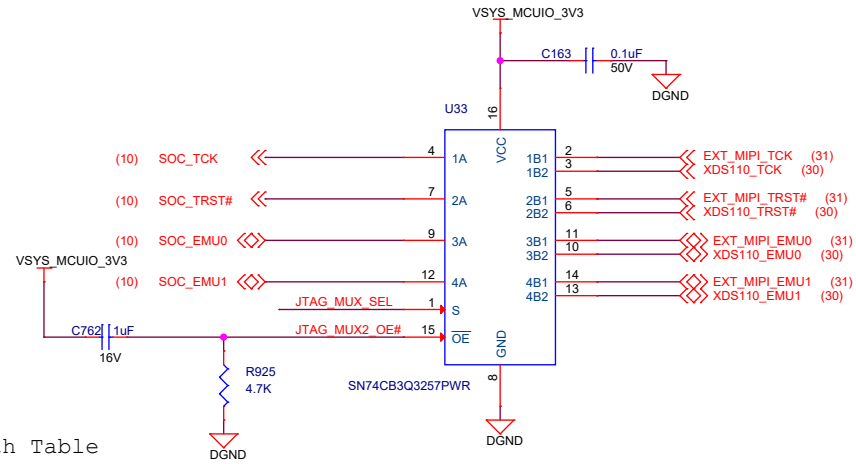
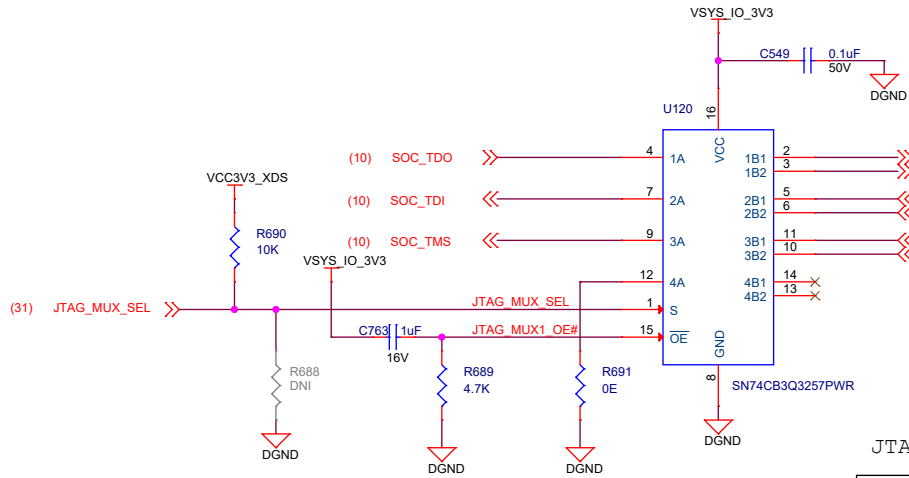
DUAL PORT FTDI



QUAD PORT FTDI

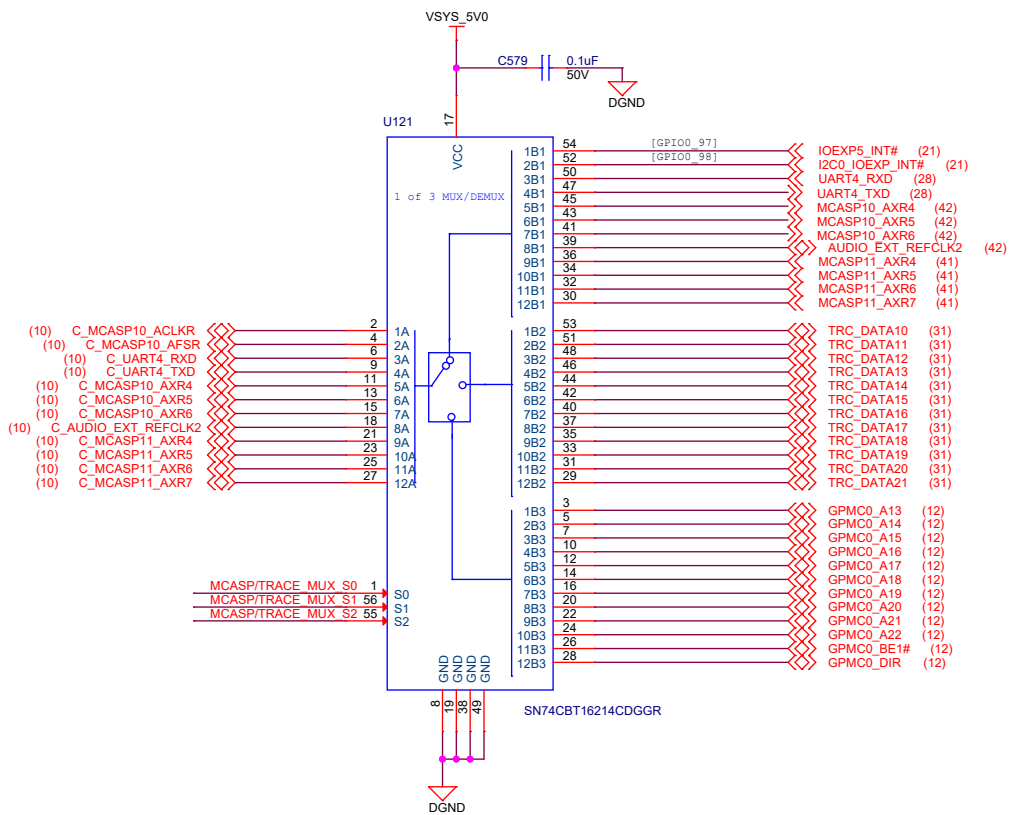
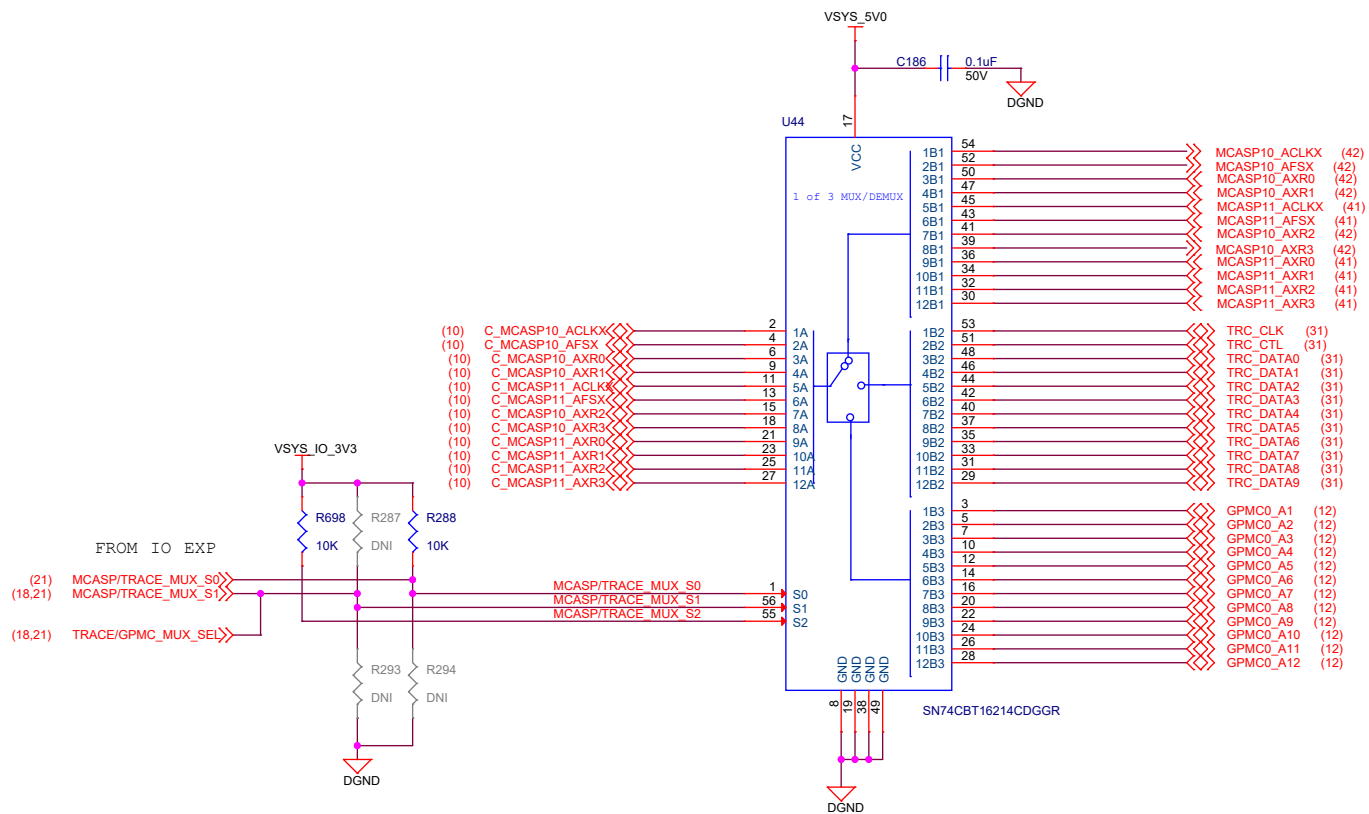


JTAG AND TRACE MUX



JTAG - 1:2 MUX : Truth Table

MUX_SEL	CONDITION	FUNCTION
LOW	External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]
HIGH	No External Emulator attached & XDS110 Powered via USB	A-->B2 port [ON Board EMU]
LOW	External Emulator attached & XDS110 Powered via USB	A-->B1 port [EXTERNAL EMU]
LOW	No External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]

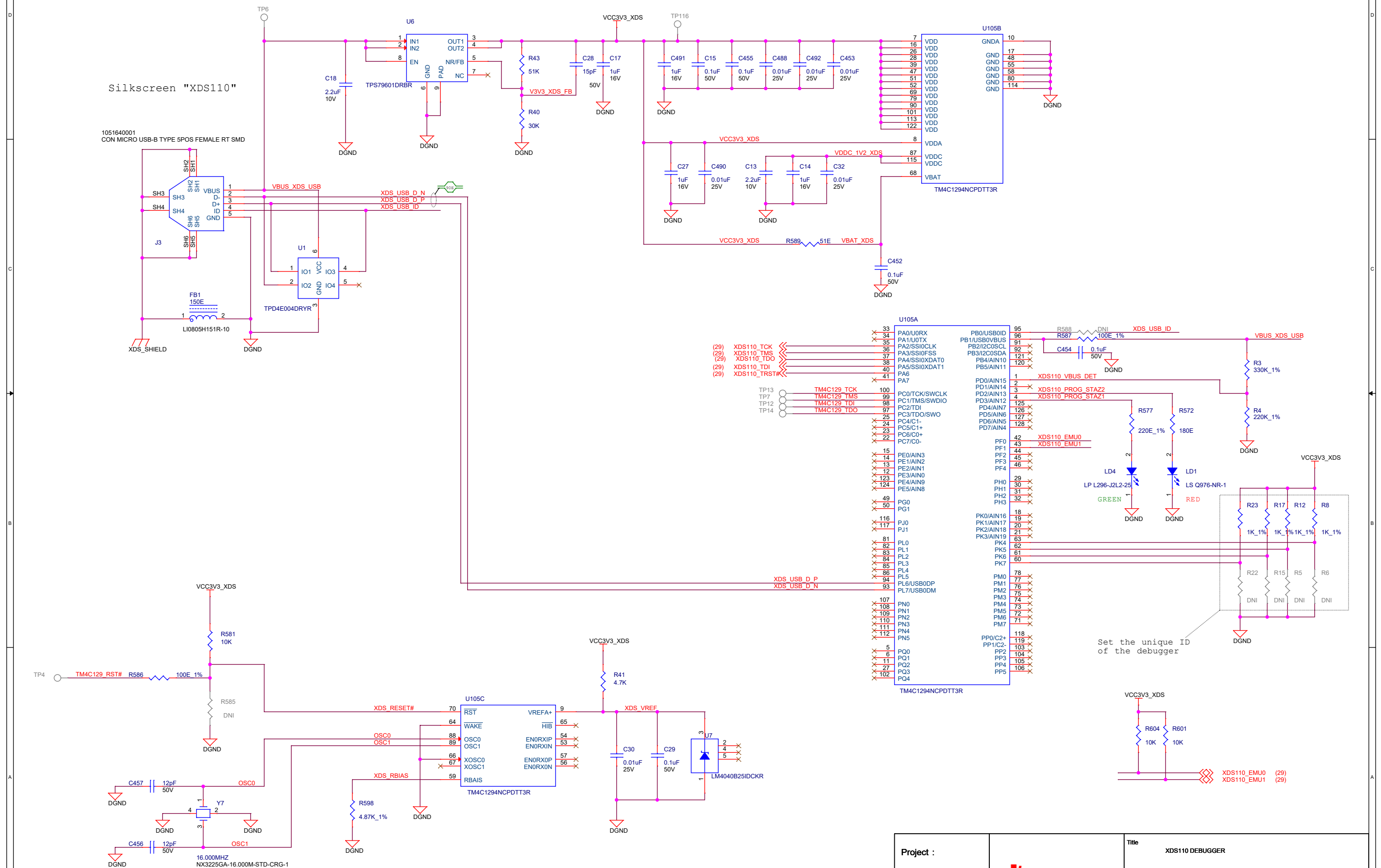


MCASP/TRACE - 1:3 MUX : Truth Table

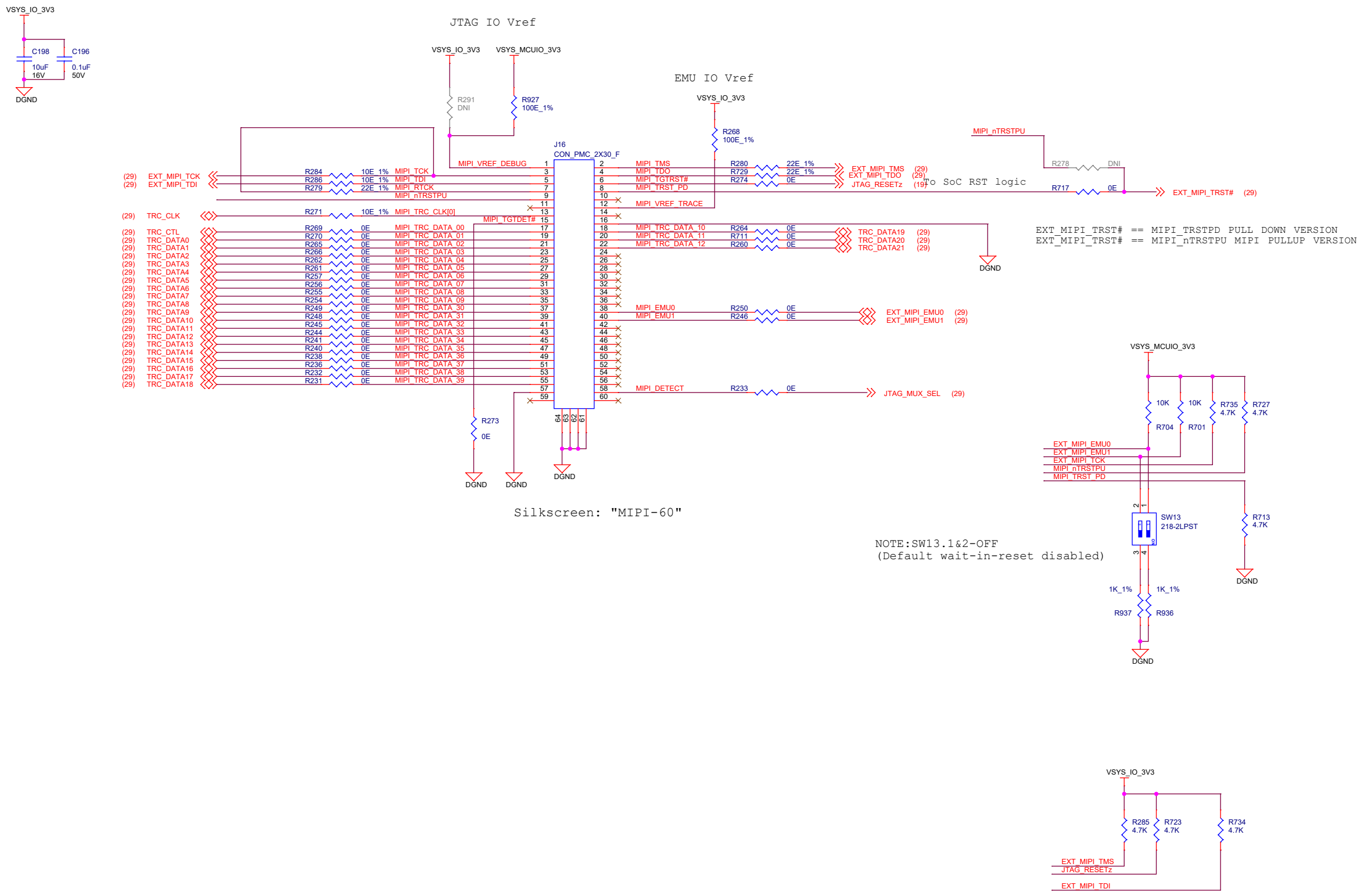
MUX_SEL2	MUX_SEL1	MUX_SEL0	FUNCTION
HIGH	HIGH	LOW	A port = B1 port
HIGH	HIGH	HIGH	A port = B2 port
HIGH	LOW	HIGH	A port = B3 port

(default)

XDS110 DEBUGGER

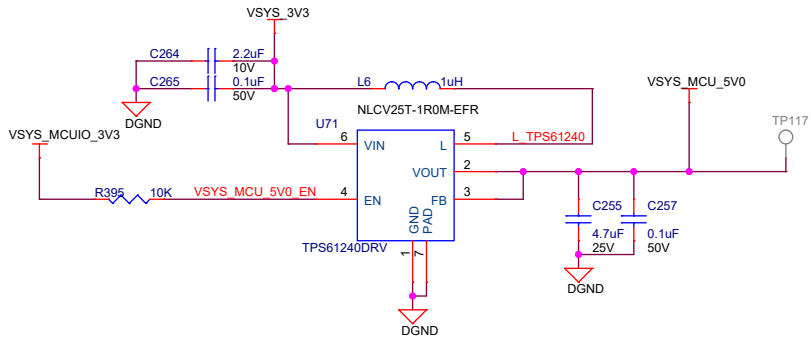


JTAG MIPI60 CONNECTOR



CAN TRANSCEIVERS #1-MCU DOMAIN

VSYS_MCU_5V0 GENERATION

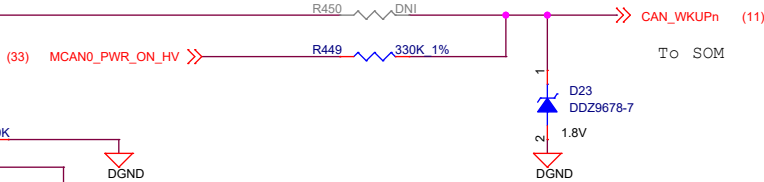
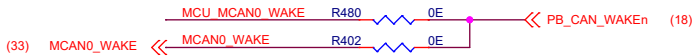
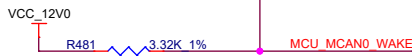


68002-202HLF
CON HDR 1X2 2.54MM PITCH ST TH

(10) MCU_MCAN0_TX >>
(10) MCU_MCAN0_RX <<
(11) MCU_CAN0_STBz >>
(11) MCU_MCAN0_EN <<

Note:TCAN1043 has integrated pull down on EN & nSTB pins

CAN WITH WAKEUP FUNCTION



PCB Silkscreen:
"MCU_CAN0"

HDR_1X4
61300411121
CON HDR 1X4 2.54MM PITCH ST TH

From MCU GPIO

68002-202HLF
CON HDR 1X2 2.54MM PITCH ST TH

(10) MCU_MCAN1_TX >>
(10) MCU_MCAN1_RX <<
(11) MCU_CAN1_STB >>

TCAN1042HGVD

PCB Silkscreen:
"MCU_CAN1"

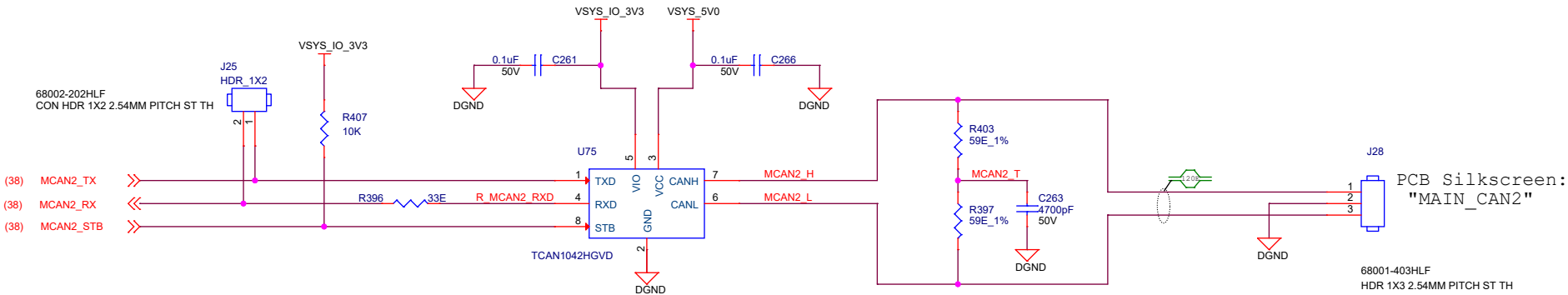
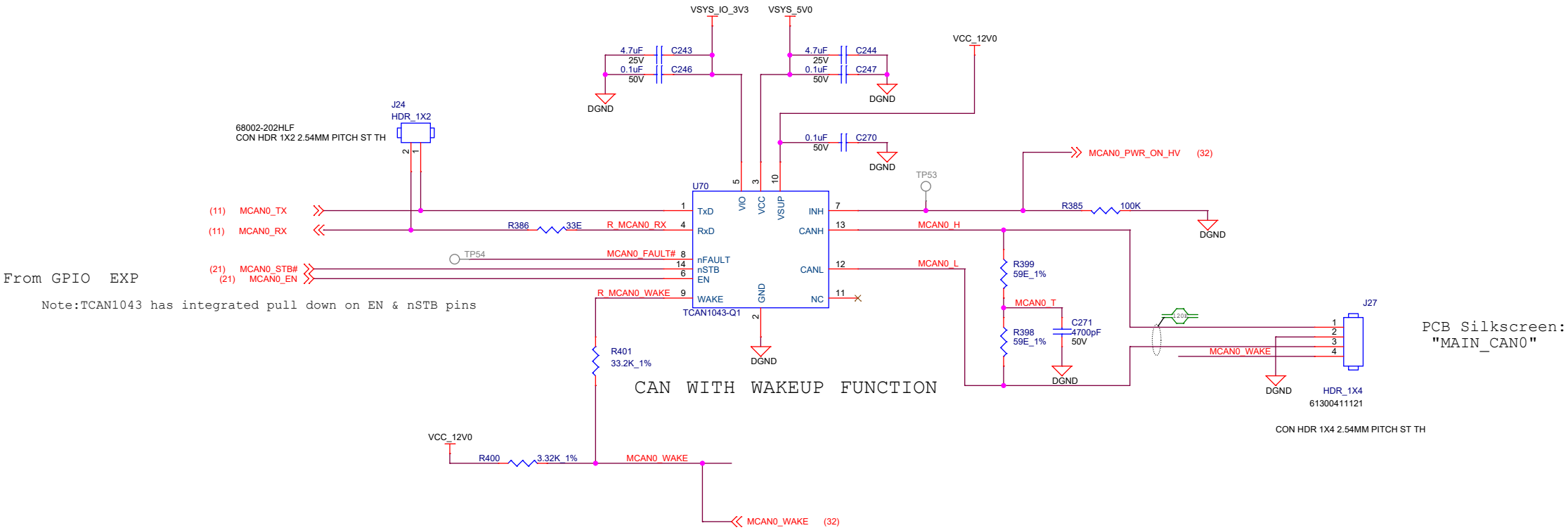
68001-403HLF
HDR 1X3 2.54MM PITCH ST TH

Project :
J7 EVM

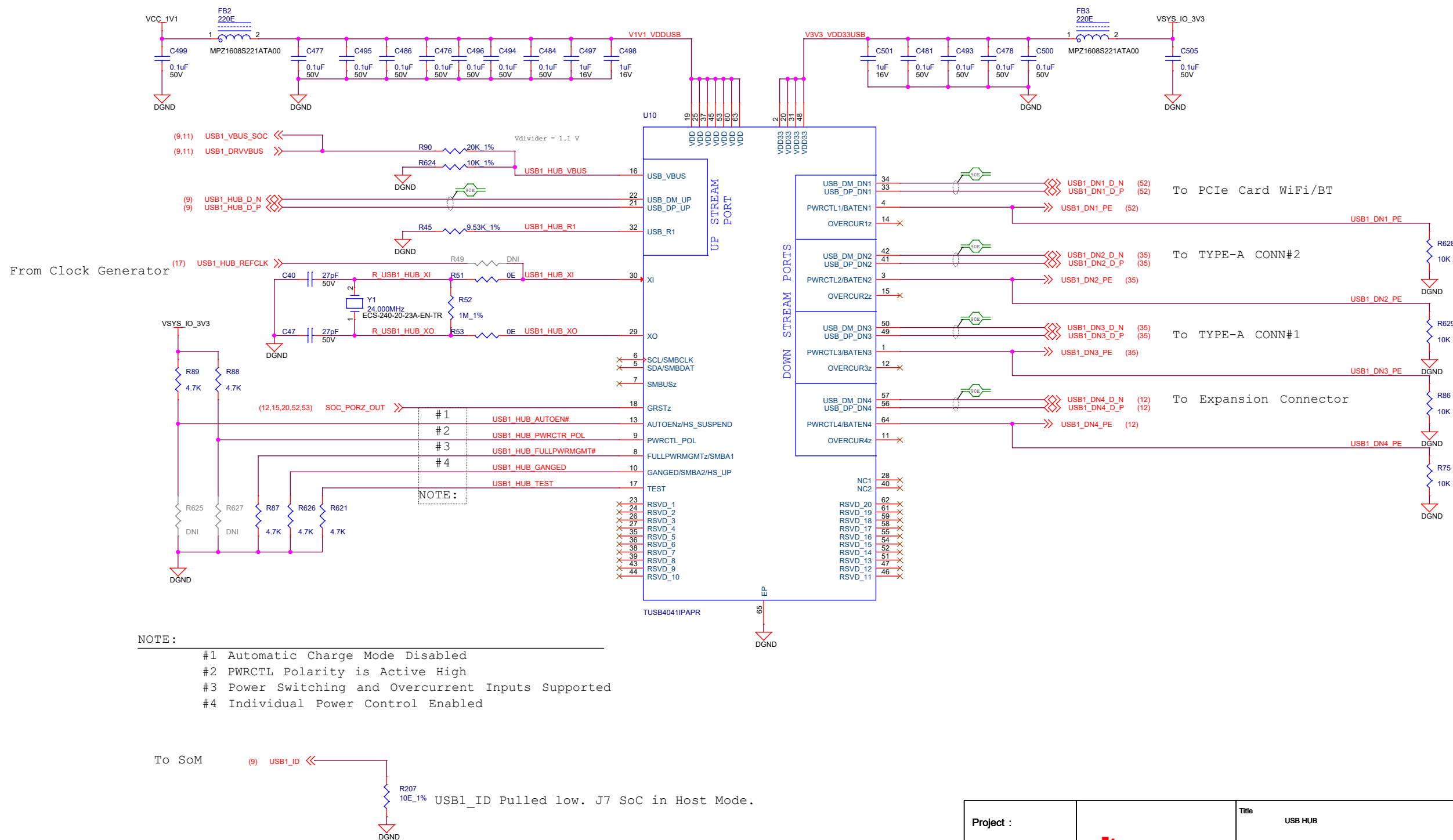


Title CAN TRANSCEIVERS #1		
Size C	PROC079 001 J721EXCP01EVM	Rev A
Date: Friday, December 03, 2021	Sheet 32 of 68	

CAN TRANSCEIVERS #2-MAIN DOMAIN



USB HUB



NOTE:

- #1 Automatic Charge Mode Disabled
- #2 PWRCTL Polarity is Active High
- #3 Power Switching and Overcurrent Inputs Supported
- #4 Individual Power Control Enabled

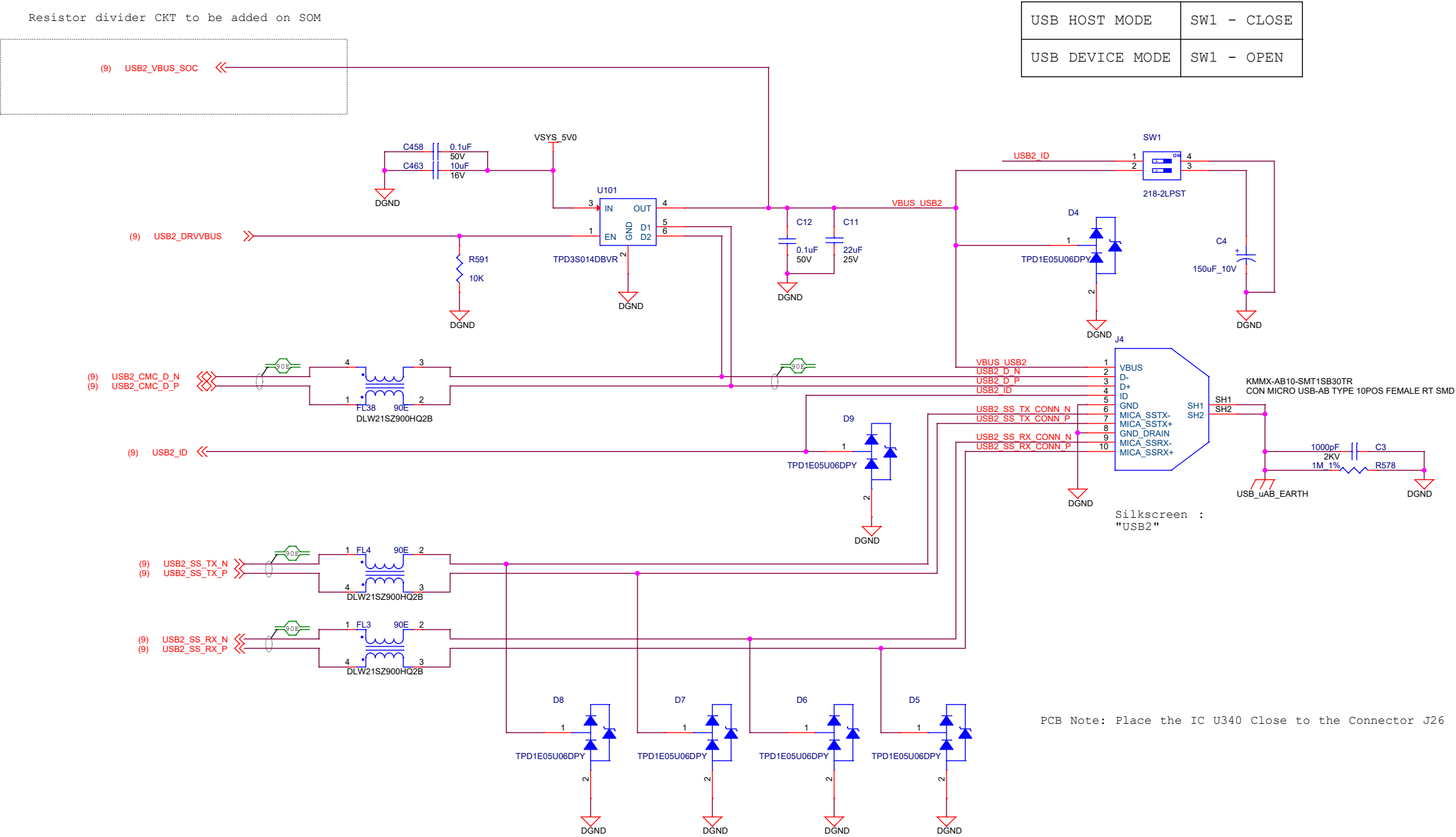
To SoM (9) USB1_ID

R207 10E_1% USB1_ID Pulled low. J7 SoC in Host Mode.

D

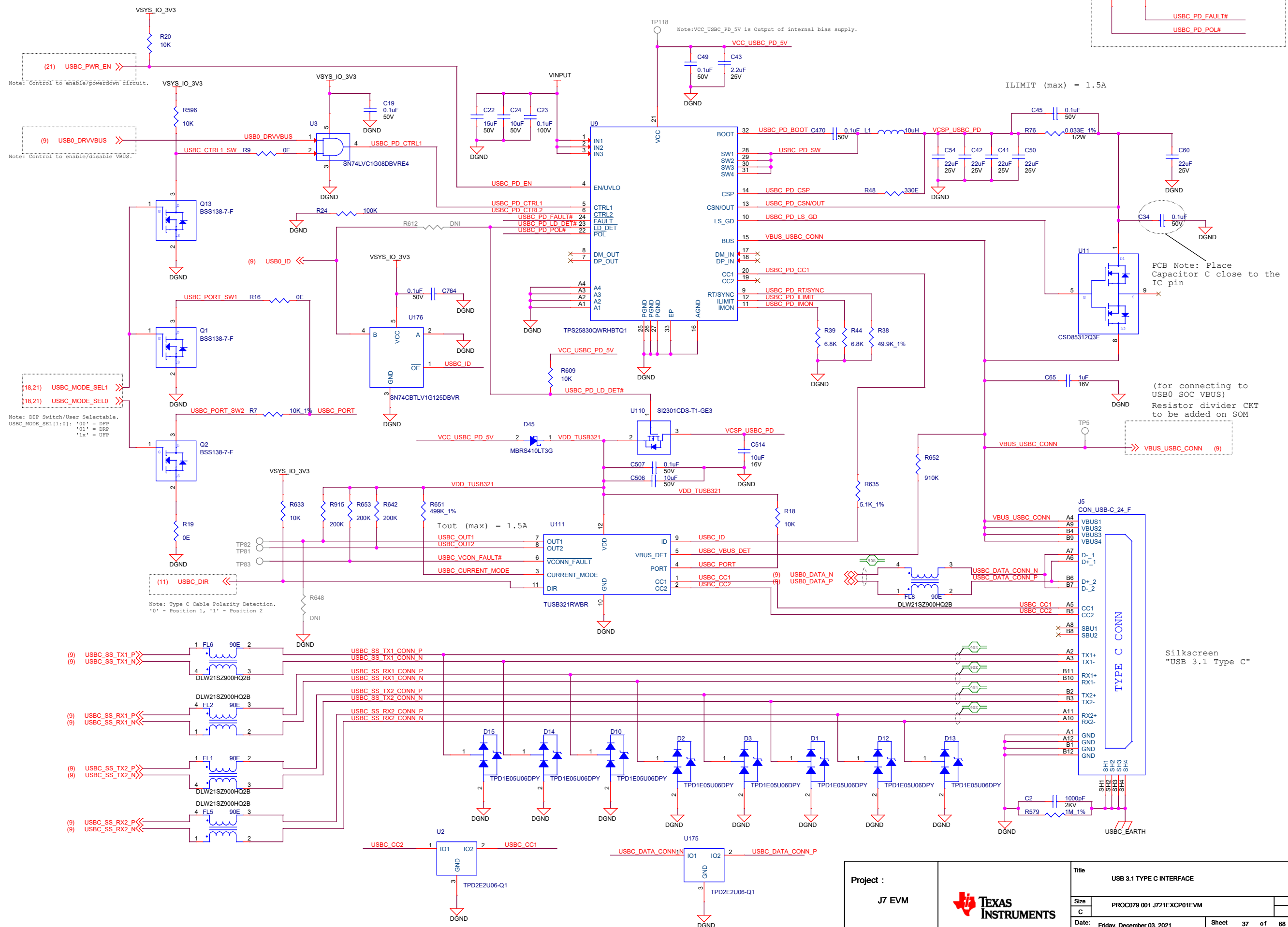


USB 3.0 uAB

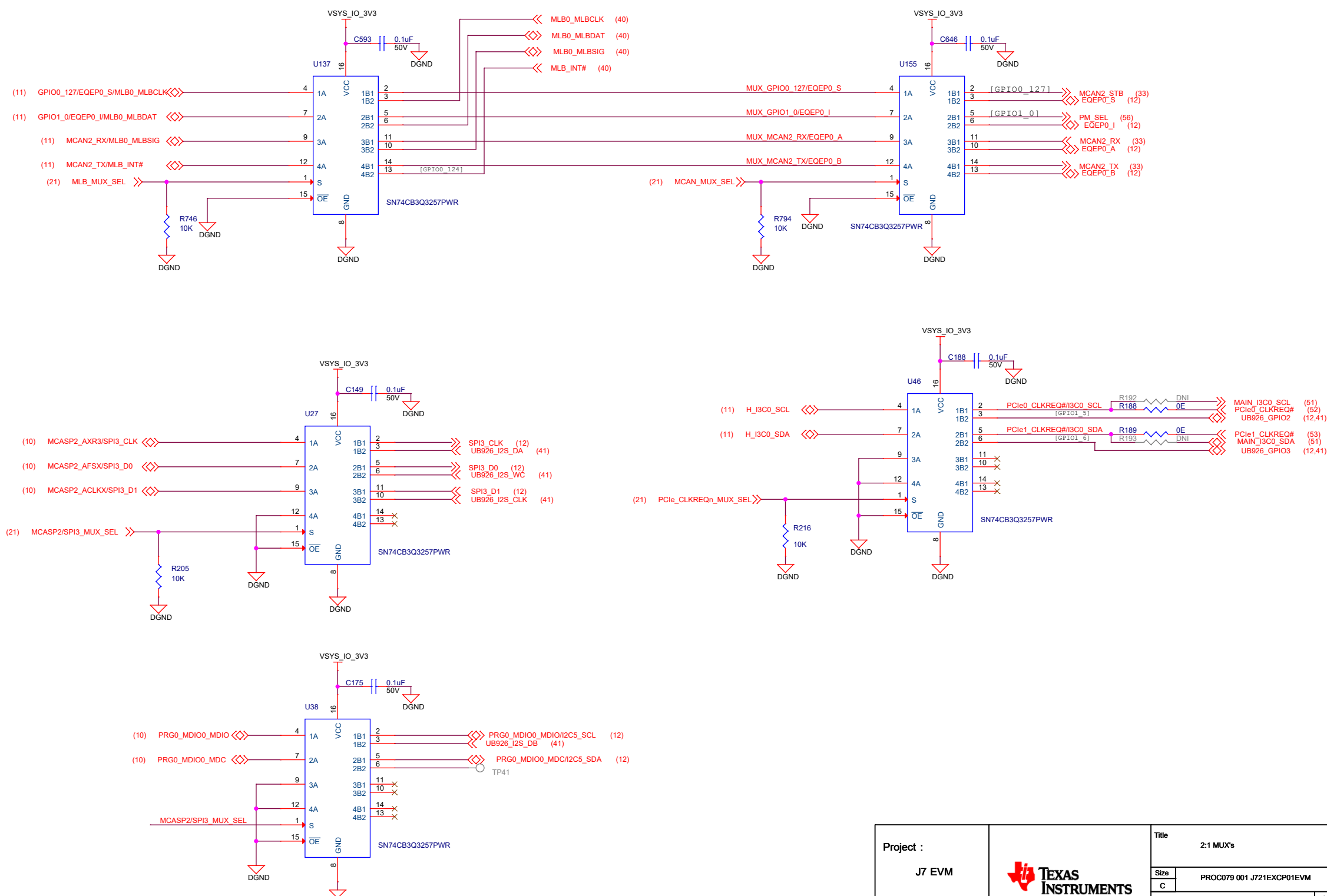


USB HOST MODE	SW1 - CLOSE
USB DEVICE MODE	SW1 - OPEN

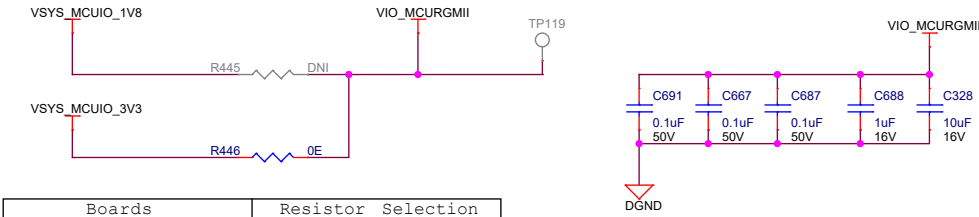
USB 3.1 TYPE C INTERFACE



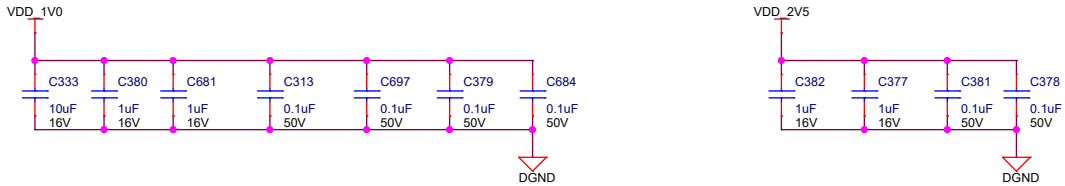
2:1 MUX's



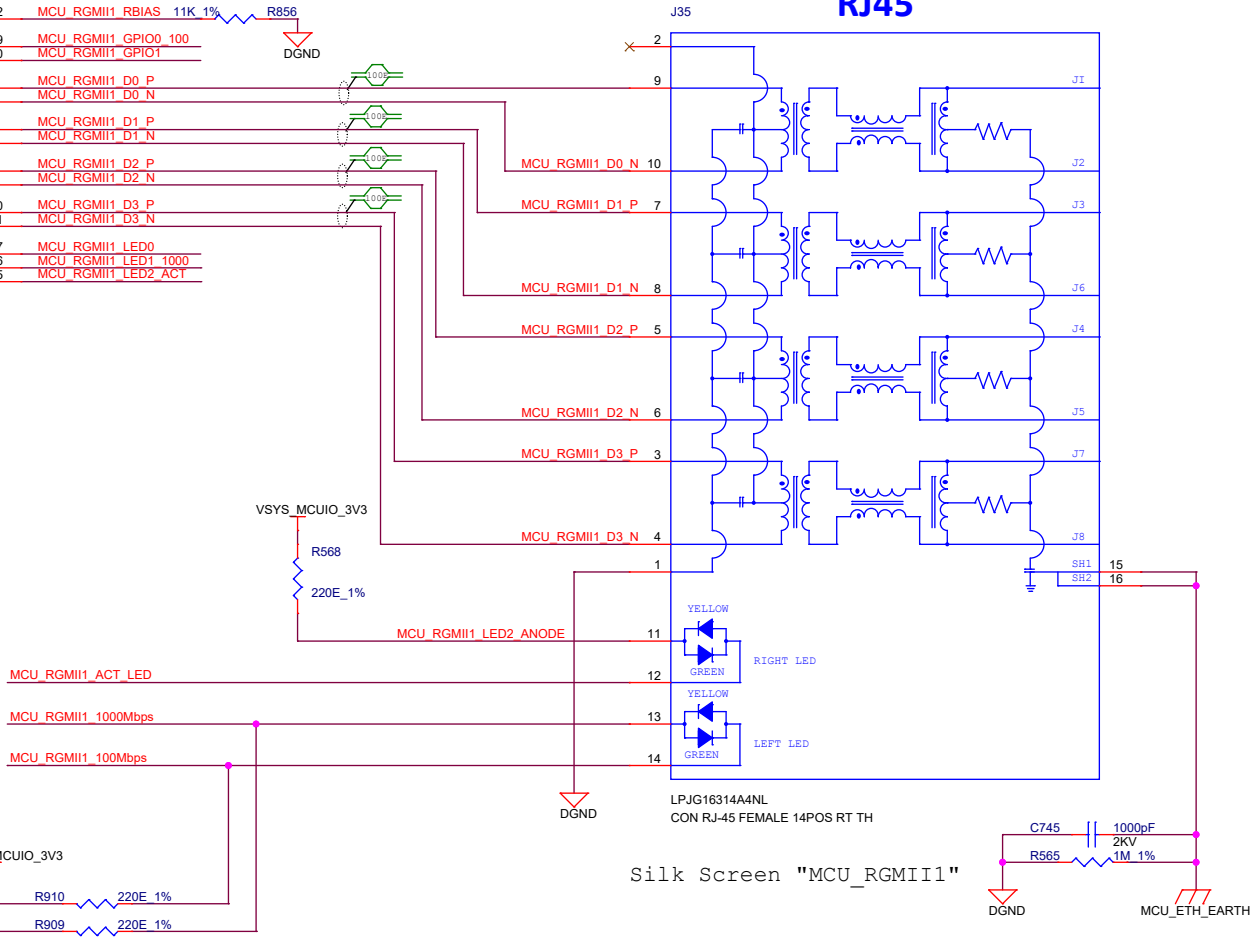
VIO_MCURGMII IO SELECTION



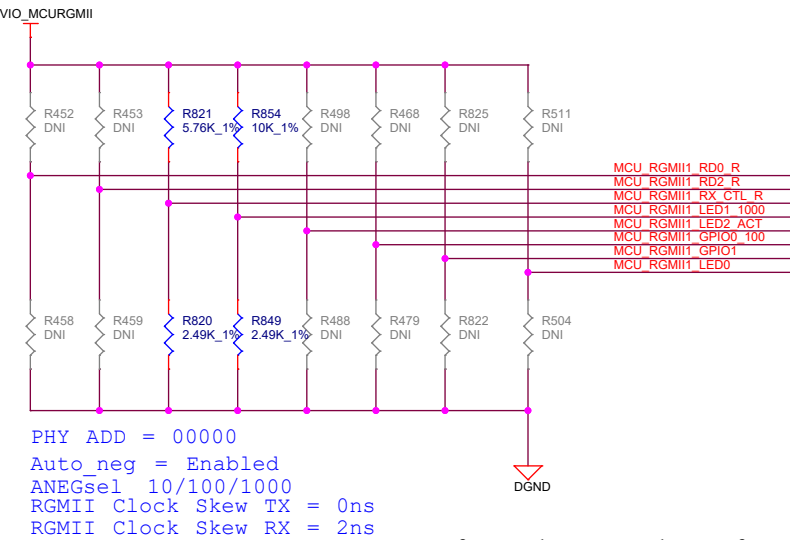
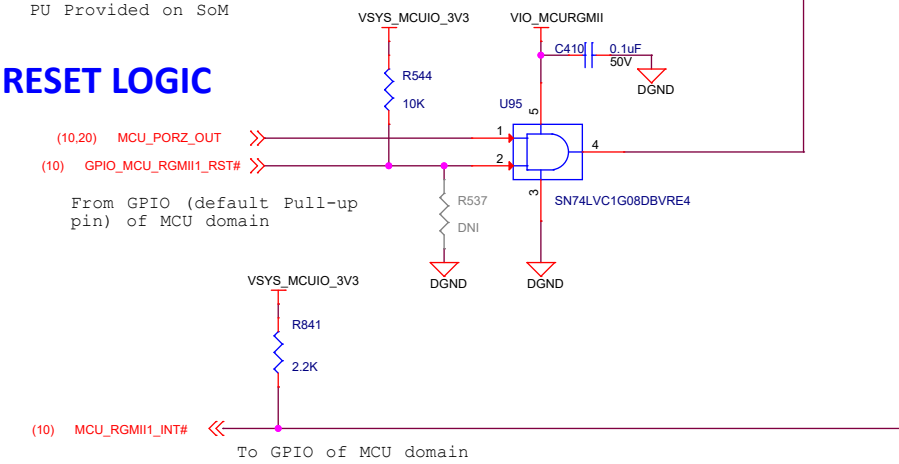
MCU GB ETHERNET



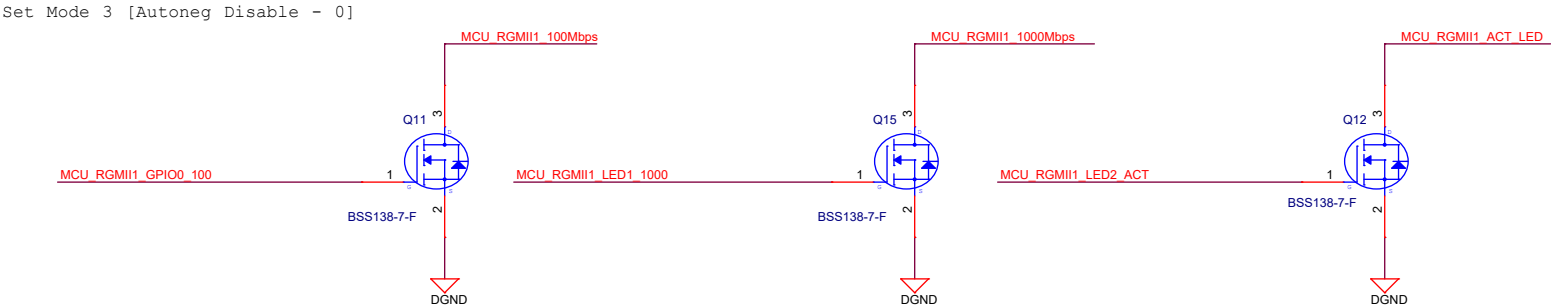
RJ45



RESET LOGIC

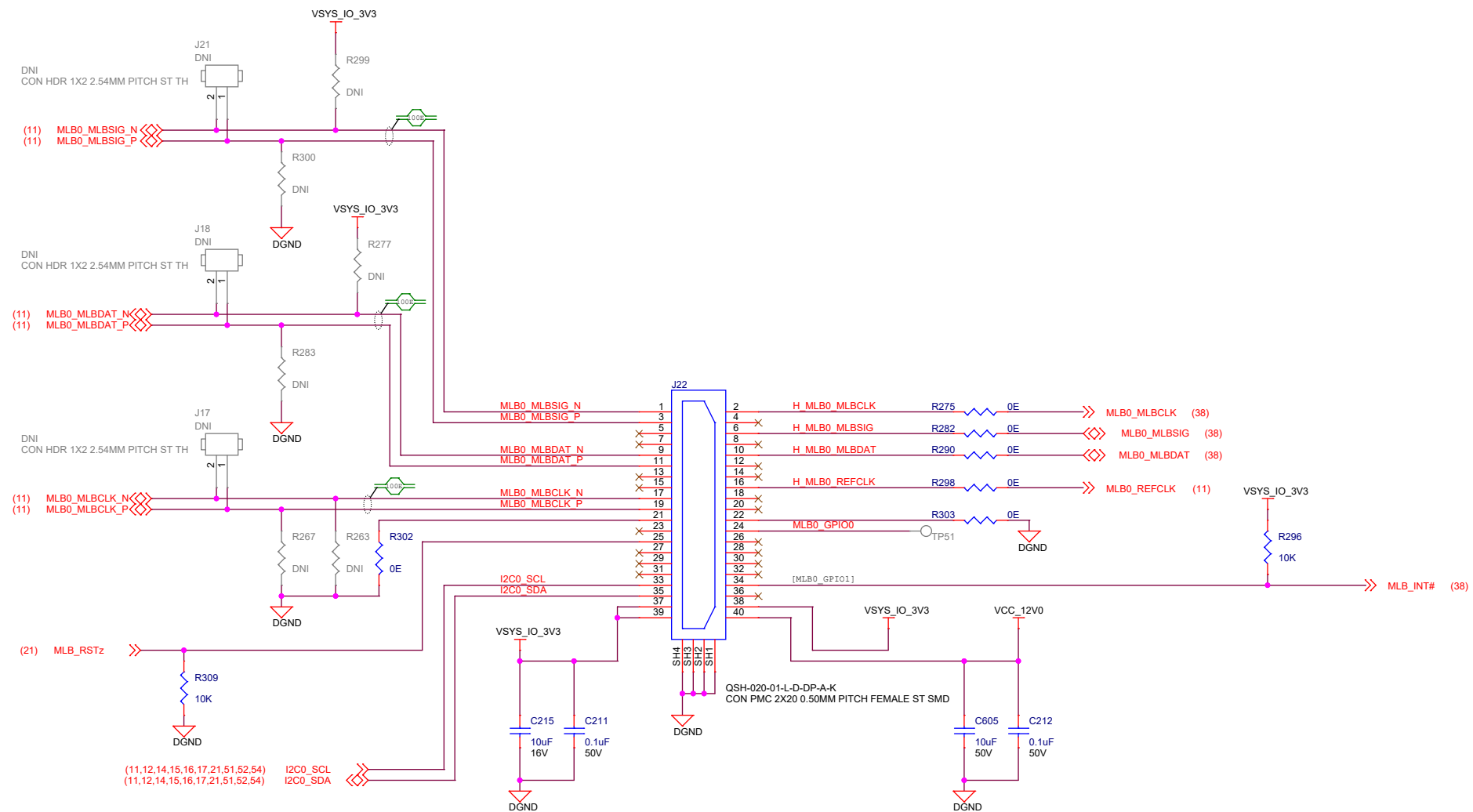


SPEED AND ACTIVITY LED DRIVERS

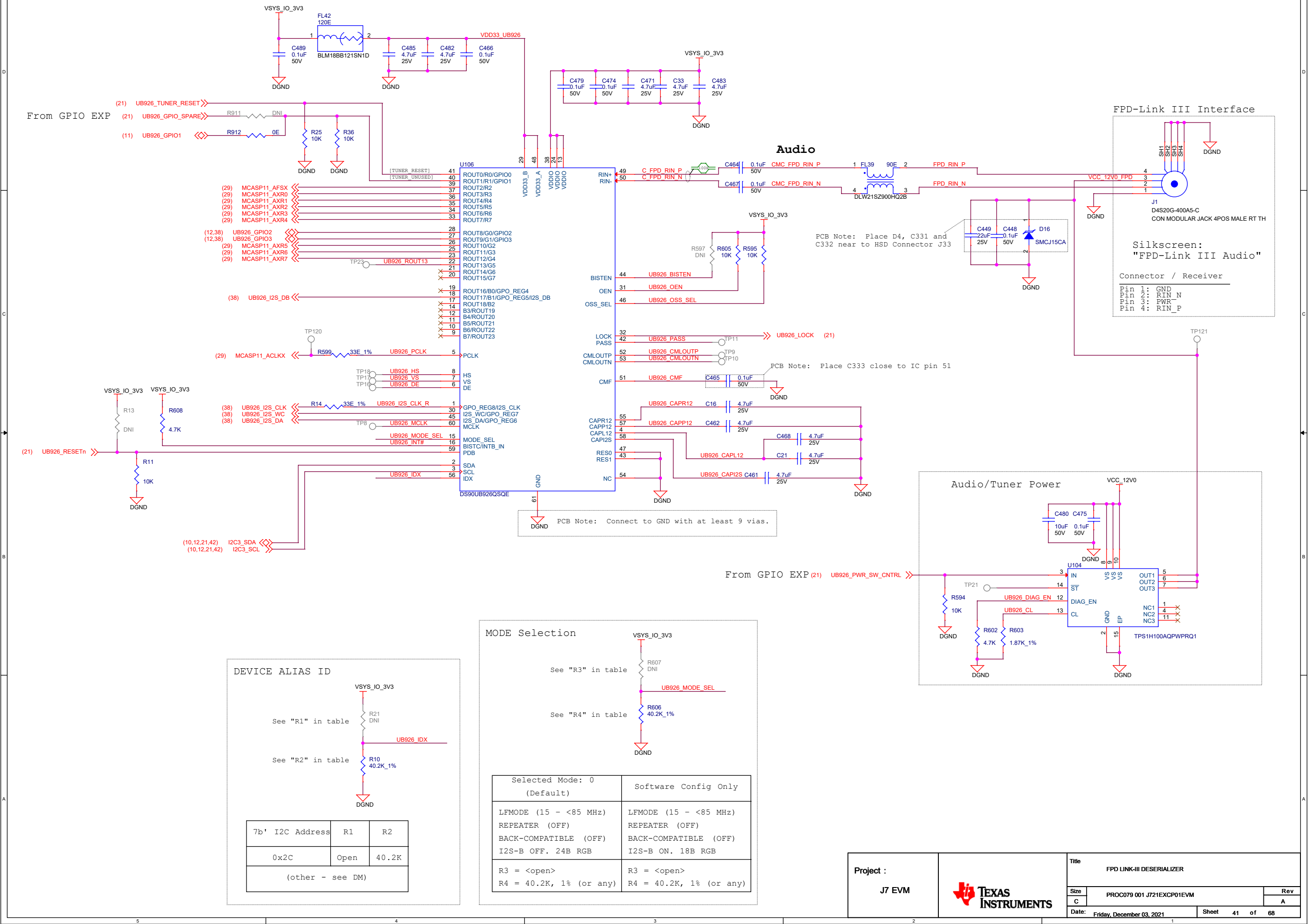


LED_2-MODE1 & LED_1-MODE2-TX SKEW=0ns
GPIO0-MODE1 & GPIO1-MODE1-RX SKEW=2ns

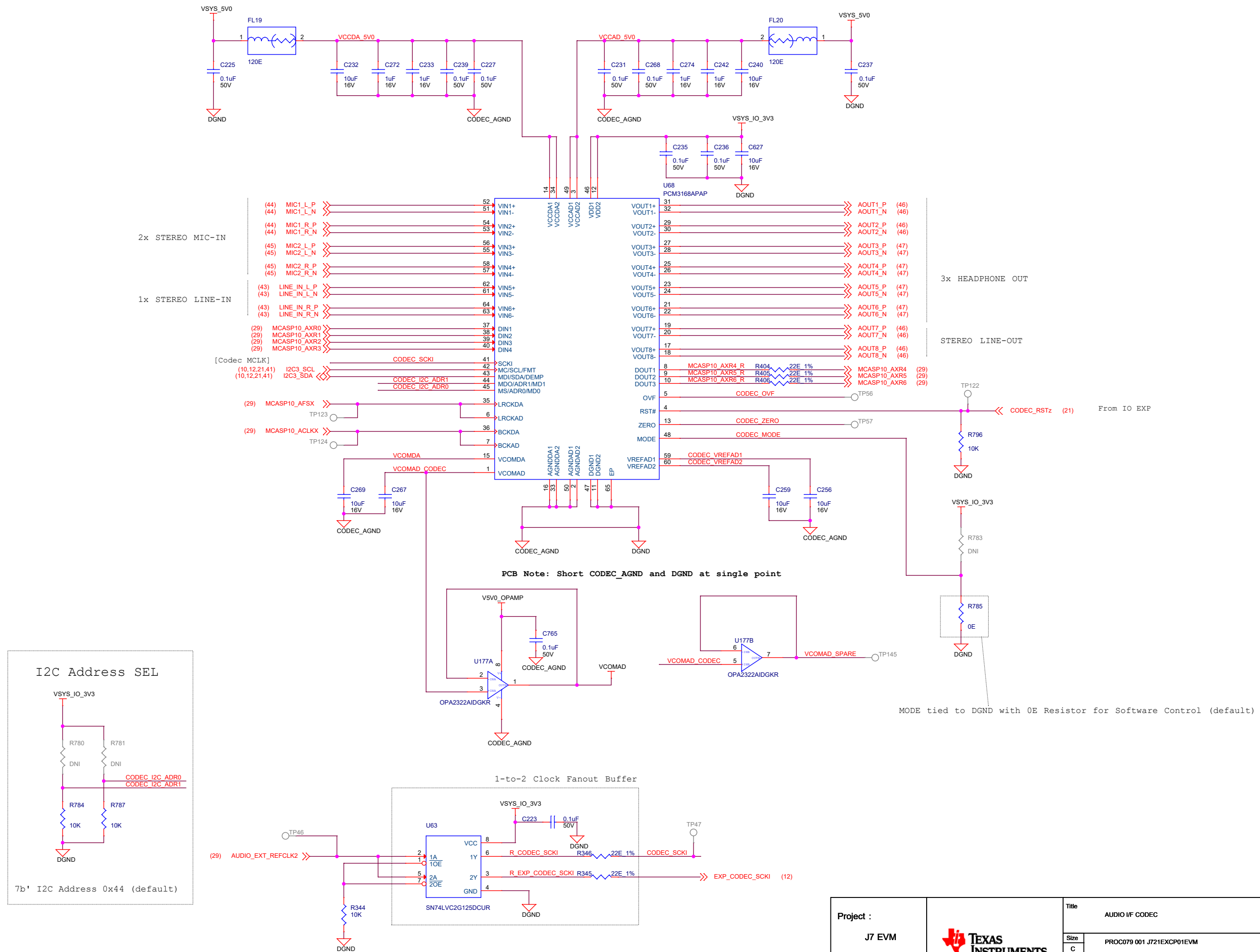
MLB INTERFACE



FPD LINK-III DESERIALIZER

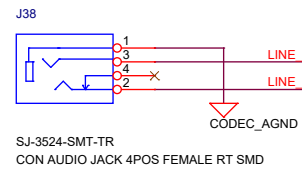


AUDIO I/F CODEC



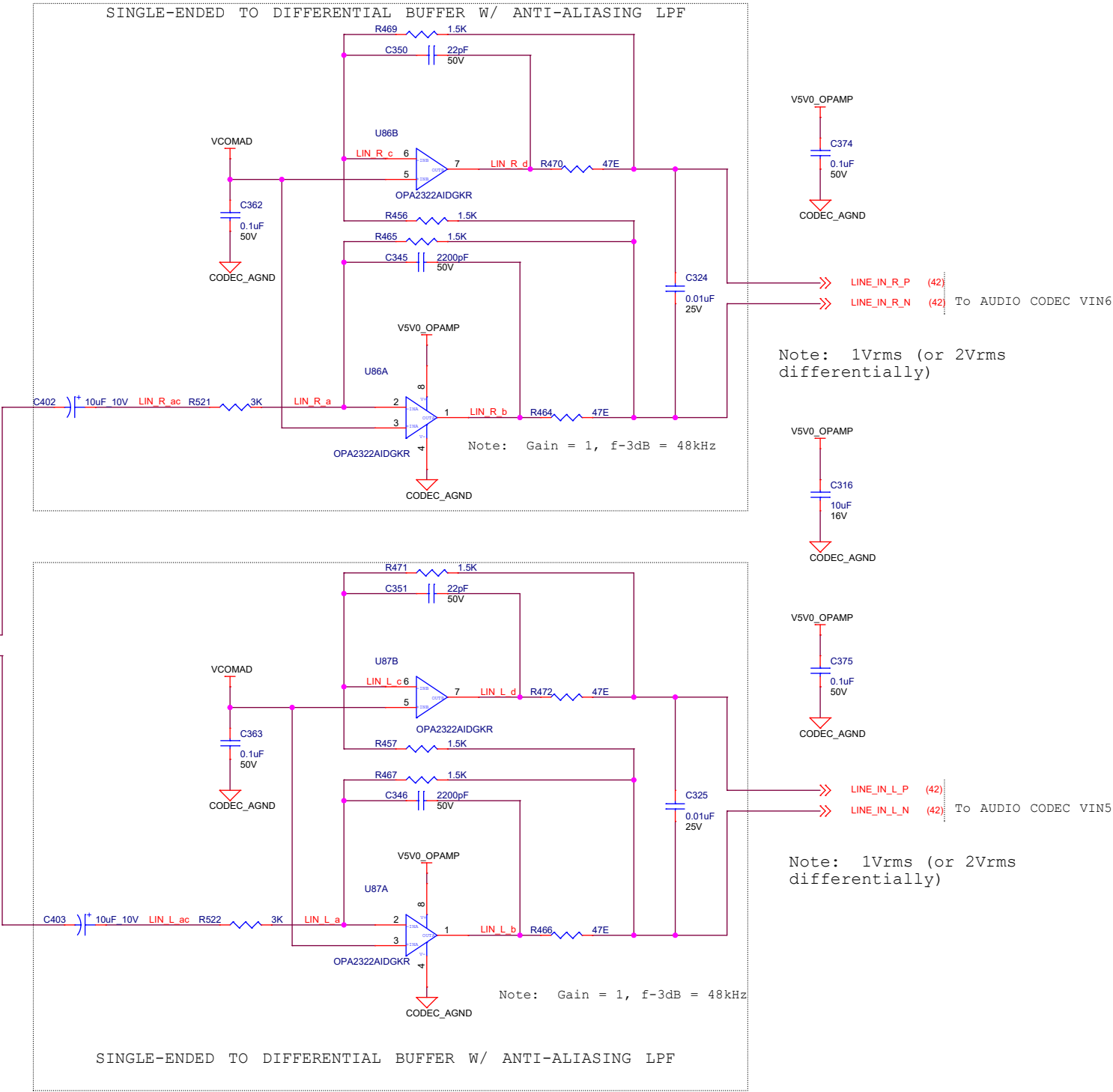
AUDIO I/F - STEREO LINE IN

Line-IN L VIN5
Line-IN R VIN6

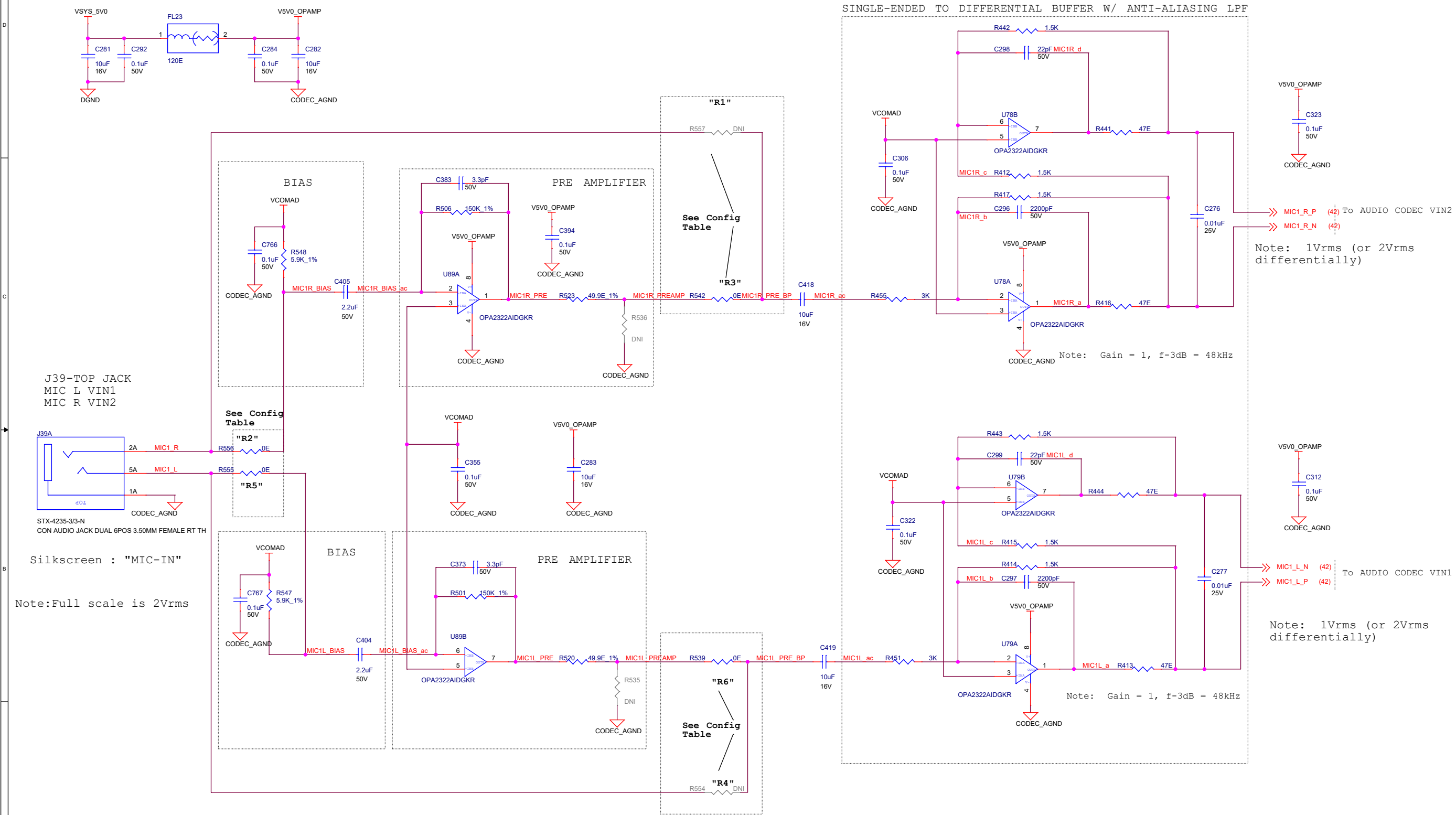


Silkscreen for J34:
"LINE-IN"

Note:Full scale is 2Vrms



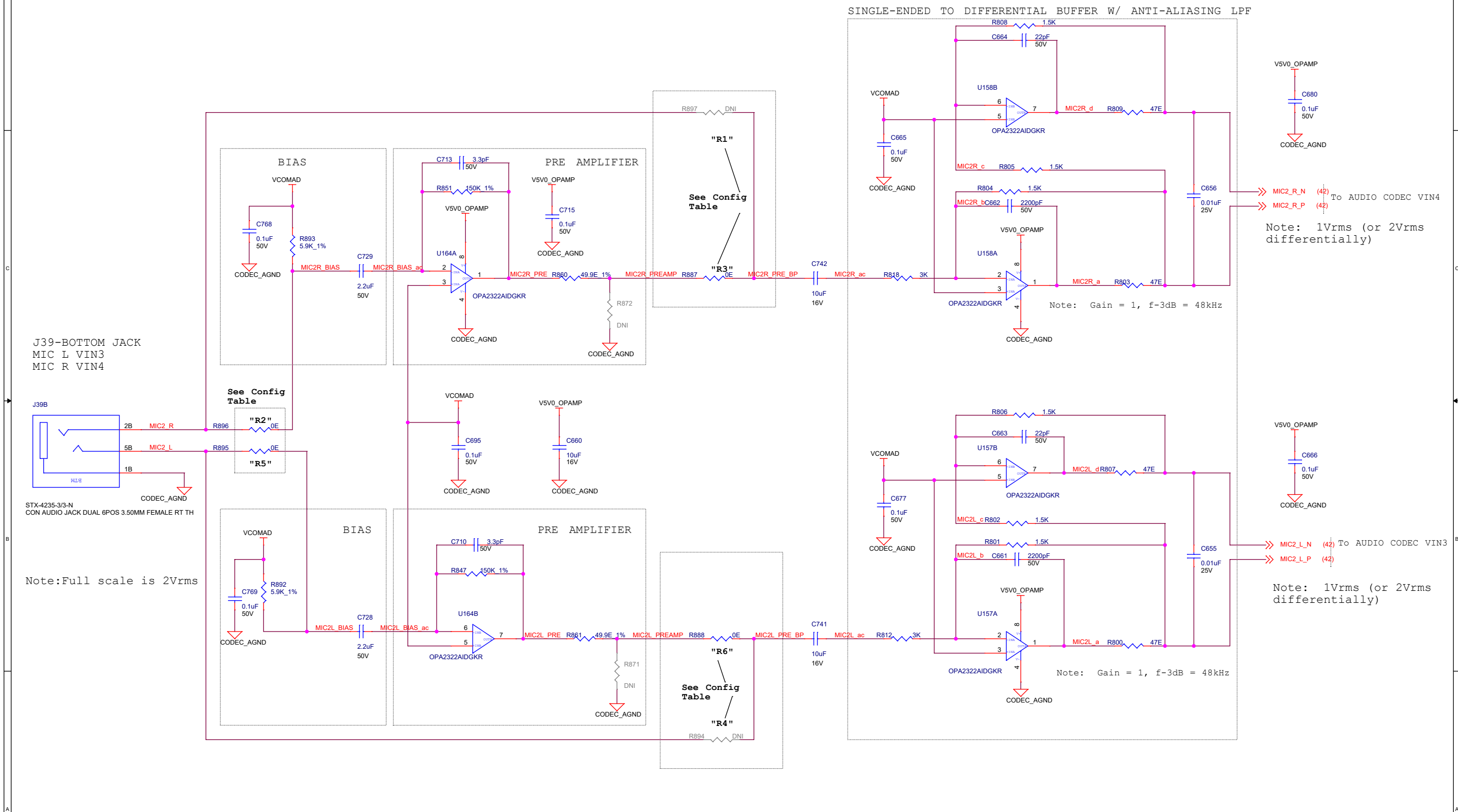
AUDIO I/F - STEREO MIC #1



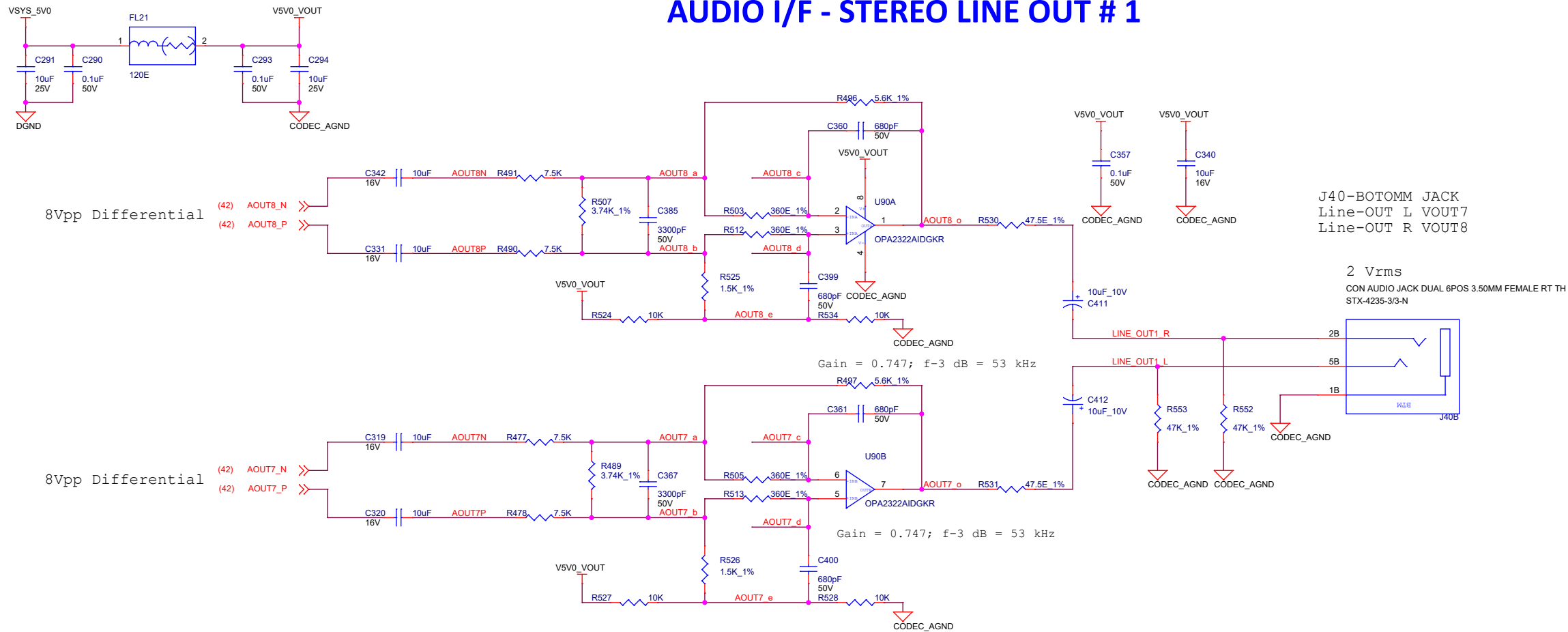
Config Table

		Install	Remove
PASSIVE-MIC (default)	BIAS + PREAMP	R2,R3,R5,R6	R1,R4
ACTIVE-MIC	BIAS ONLY	R1,R2,R4,R5	R3,R6
LINE-INPUT	NO BIAS/PREAMP	R1,R4	R2,R3,R5,R6

AUDIO I/F - STEREO MIC #2



AUDIO I/F - STEREO LINE OUT # 1

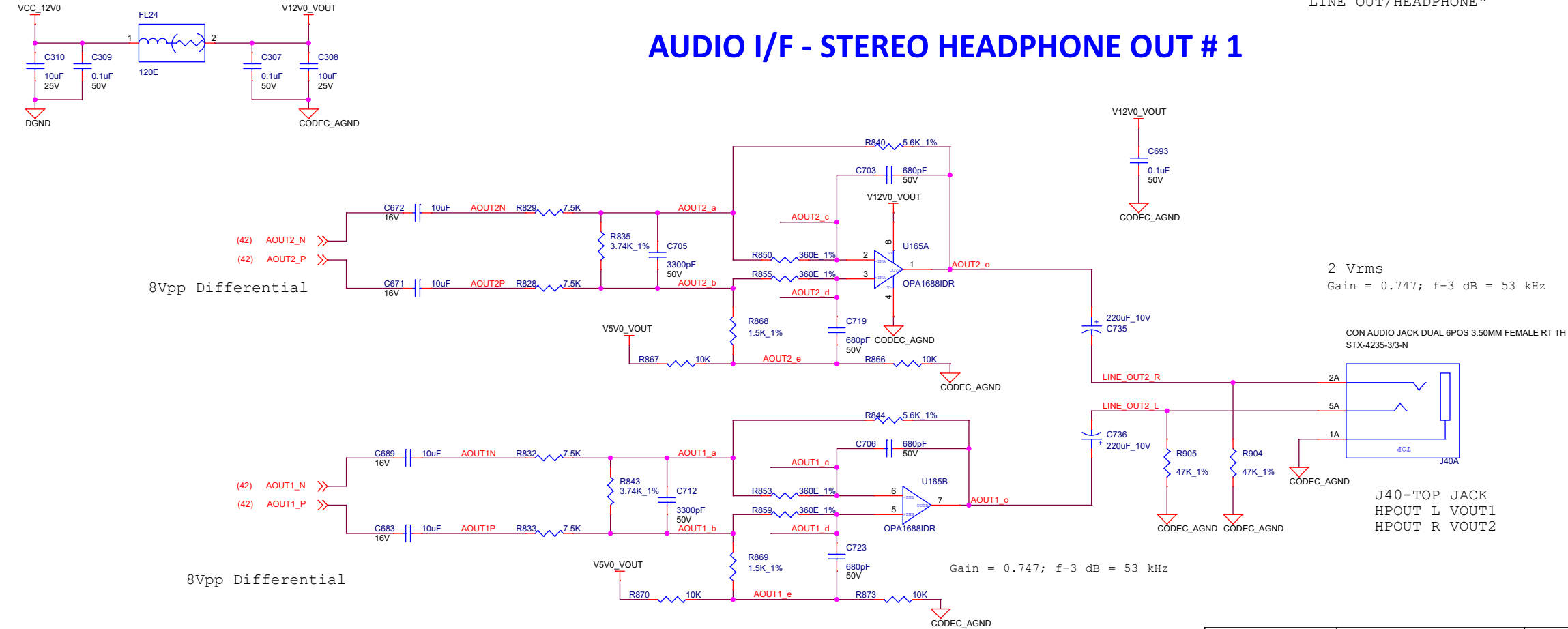


J40-BOTTOM JACK
Line-OUT L VOUT7
Line-OUT R VOUT8

2 Vrms
CON AUDIO JACK DUAL 6POS 3.50MM FEMALE RT TH
STX-4235-3/3-N

Silkscreen for J40: "
LINE OUT/HEADPHONE"

AUDIO I/F - STEREO HEADPHONE OUT # 1

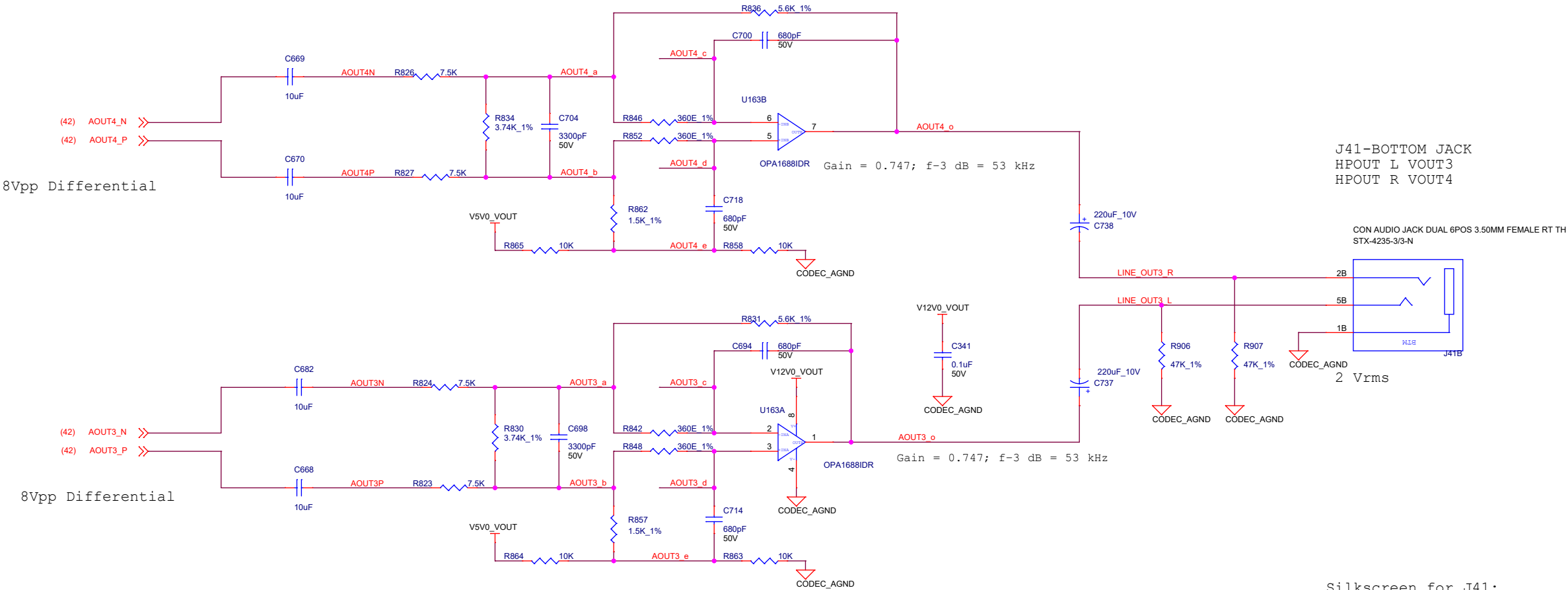


2 Vrms
Gain = 0.747; f-3 dB = 53 kHz

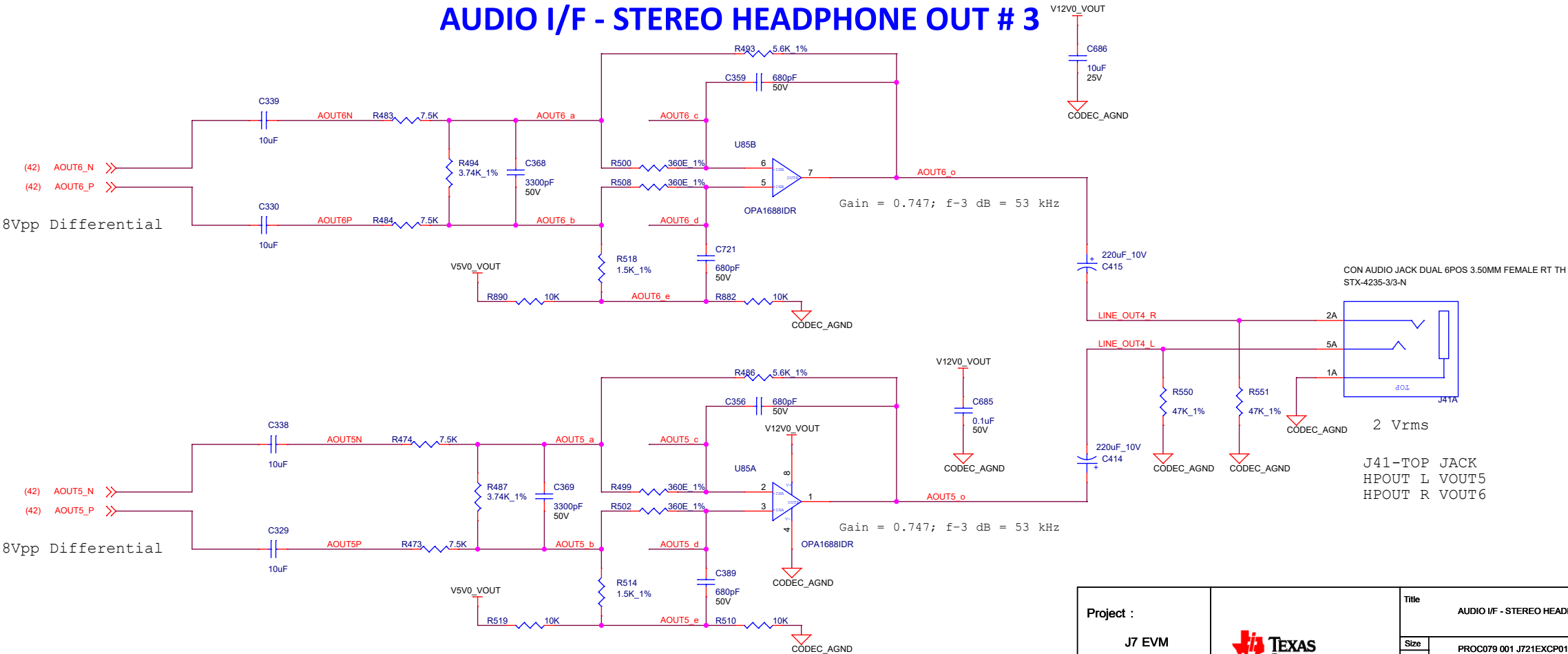
CON AUDIO JACK DUAL 6POS 3.50MM FEMALE RT TH
STX-4235-3/3-N

J40-TOP JACK
HPOUT L VOUT1
HPOUT R VOUT2

AUDIO I/F - STEREO HEADPHONE OUT # 2



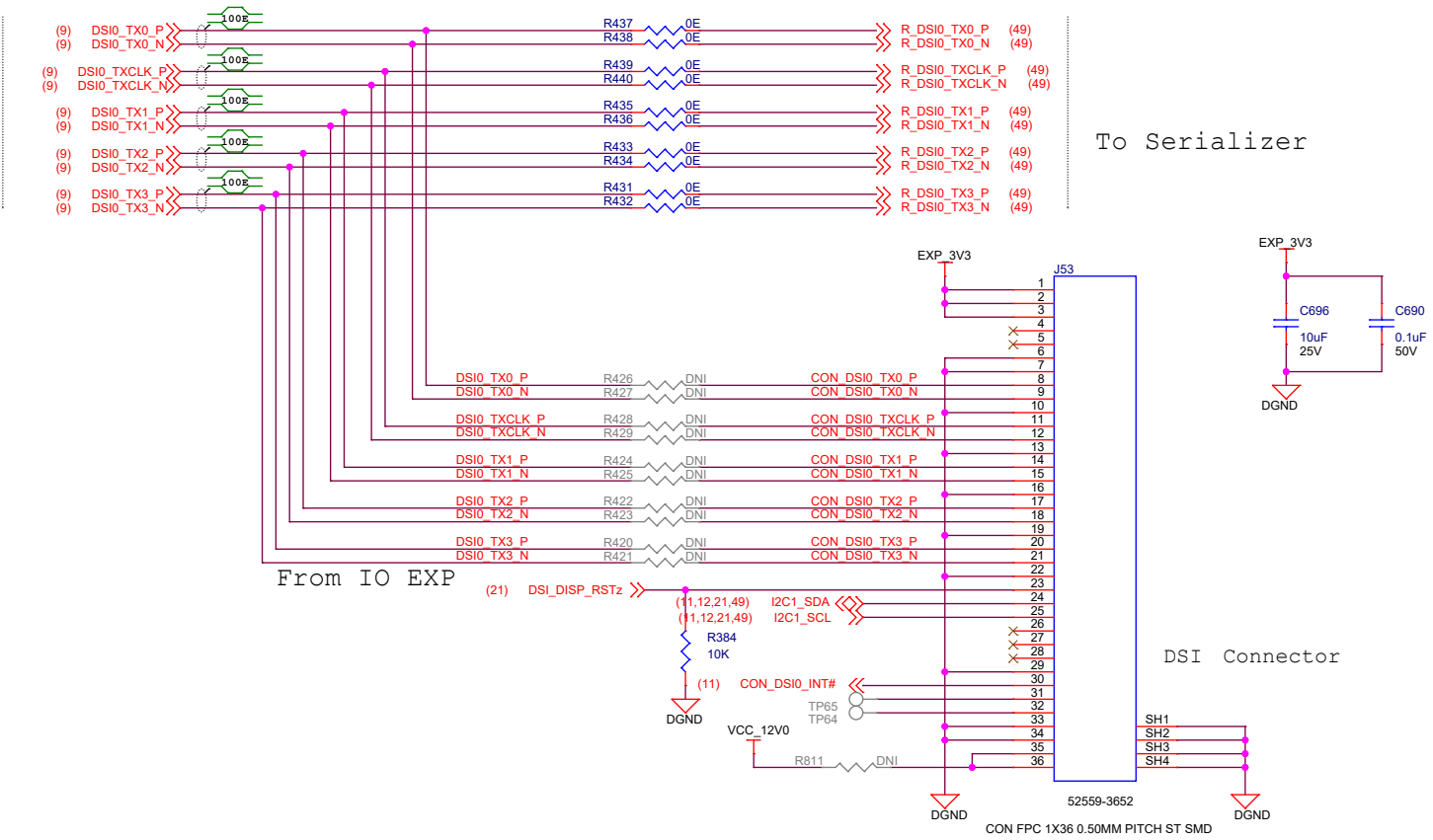
AUDIO I/F - STEREO HEADPHONE OUT # 3



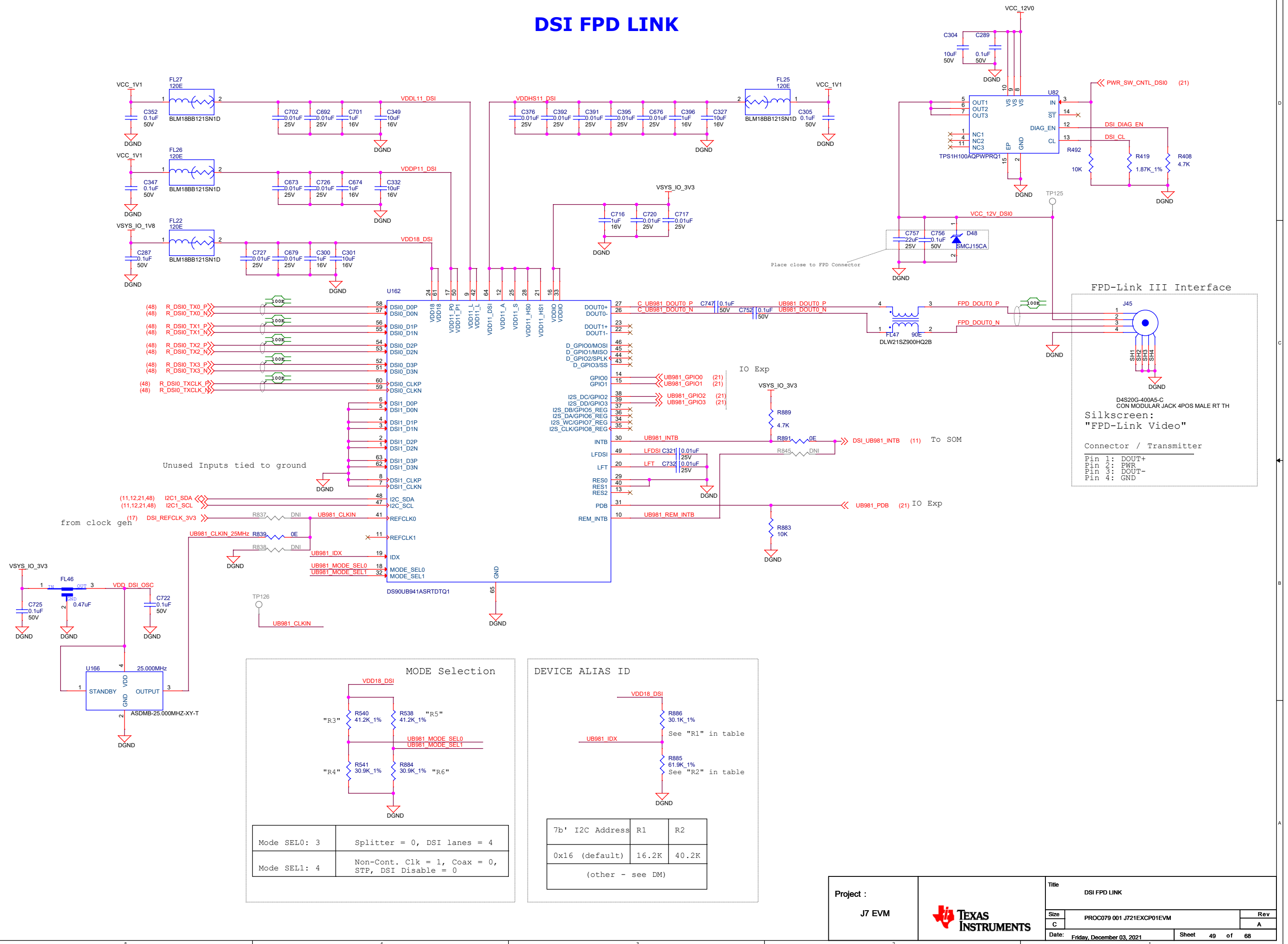
DSI FPC

From SOM

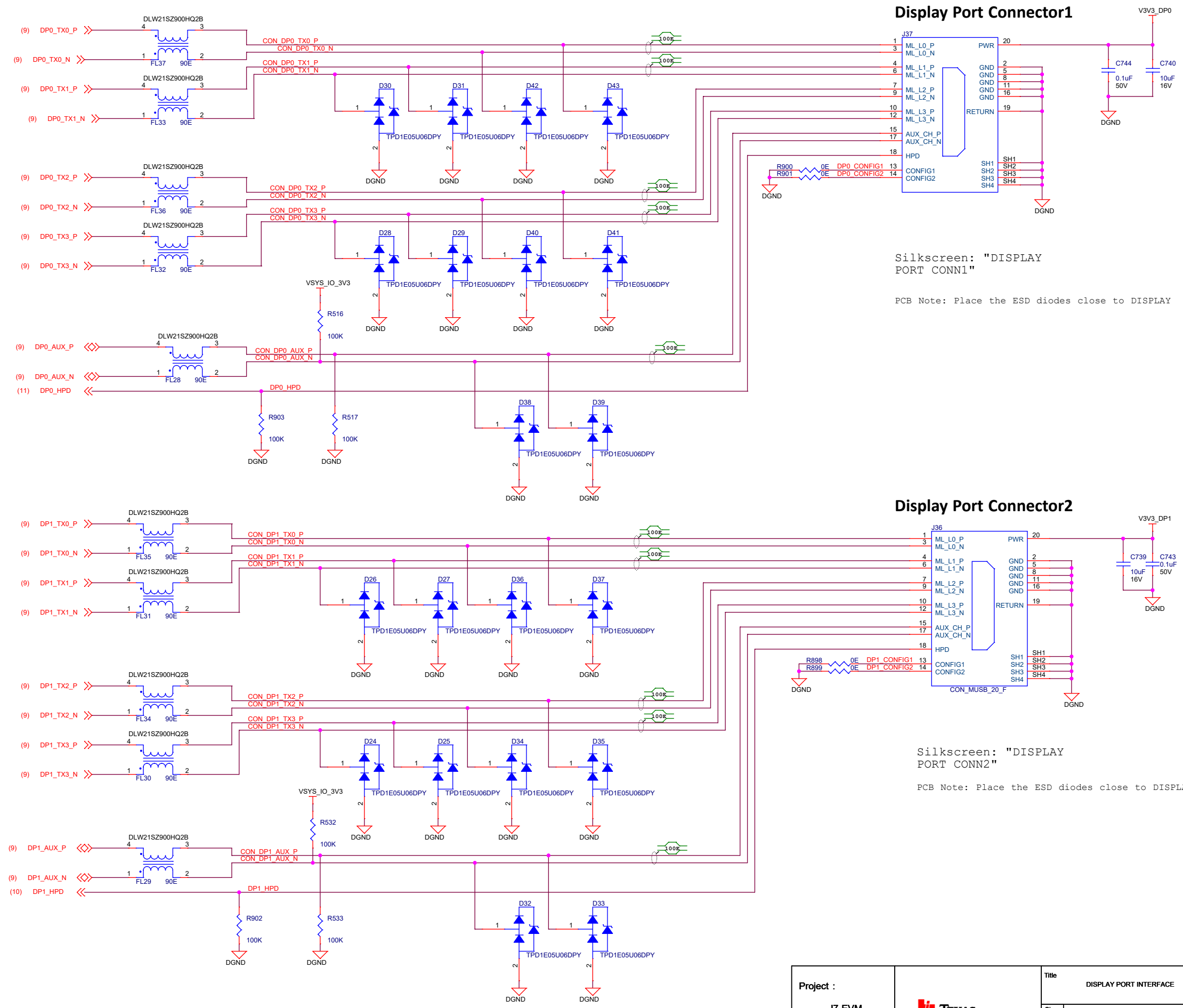
To Serializer



DSI FPD LINK



DISPLAY PORT INTERFACE



Display Port Connector1

Silkscreen: "DISPLAY PORT CONN1"

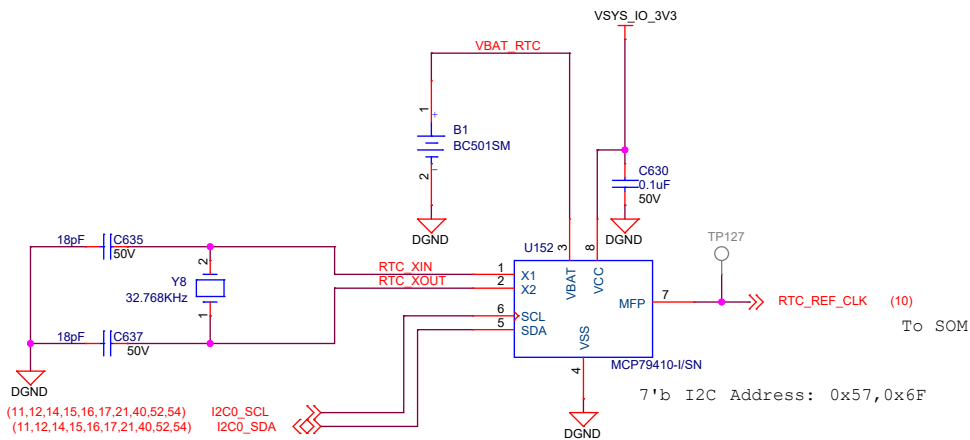
PCB Note: Place the ESD diodes close to DISPLAY PORT CONN1

Display Port Connector2

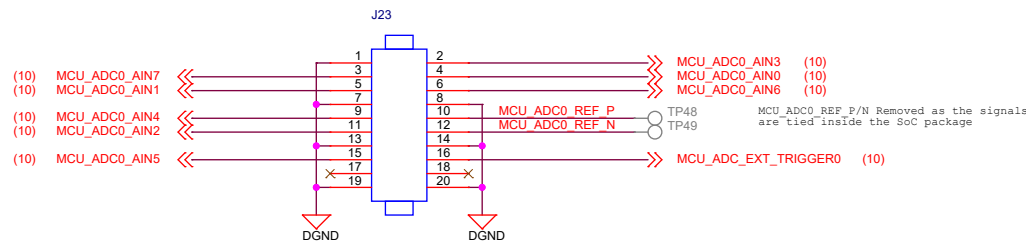
Silkscreen: "DISPLAY PORT CONN2"

PCB Note: Place the ESD diodes close to DISPLAY PORT CONN2

RTC

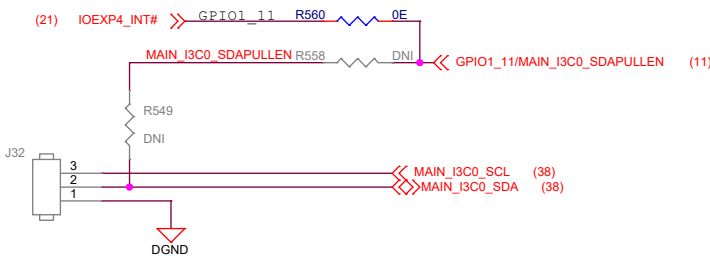


ADC INTERFACE



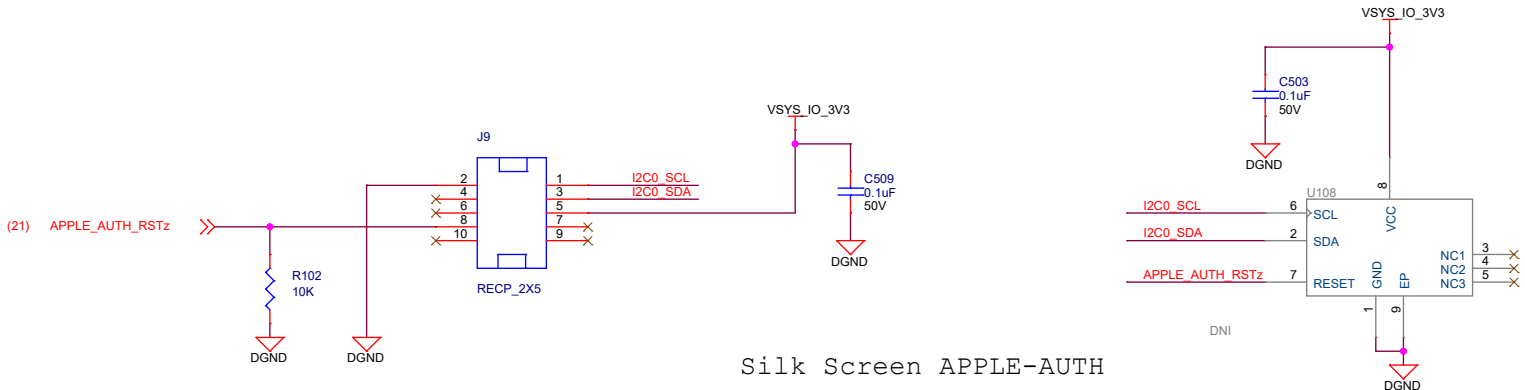
ADC Connector

I3C Headers



Silk Screen MAIN-I3C

Apple Authentication



Silk Screen APPLE-AUTH



Silk Screen MCU-I3C

x4 Lane PCIe Connector

(12,14) ENET_EXP_MDC >>> R137 DNI PCle1 MDIO0_MDC
(12,14) ENET_EXP_MDIO <<< R136 DNI PCle1_MDIO0_MDIO

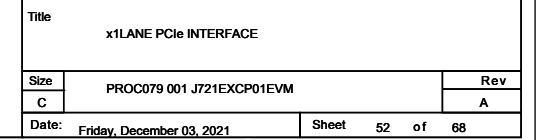


CLOCK ROOT SELECTION

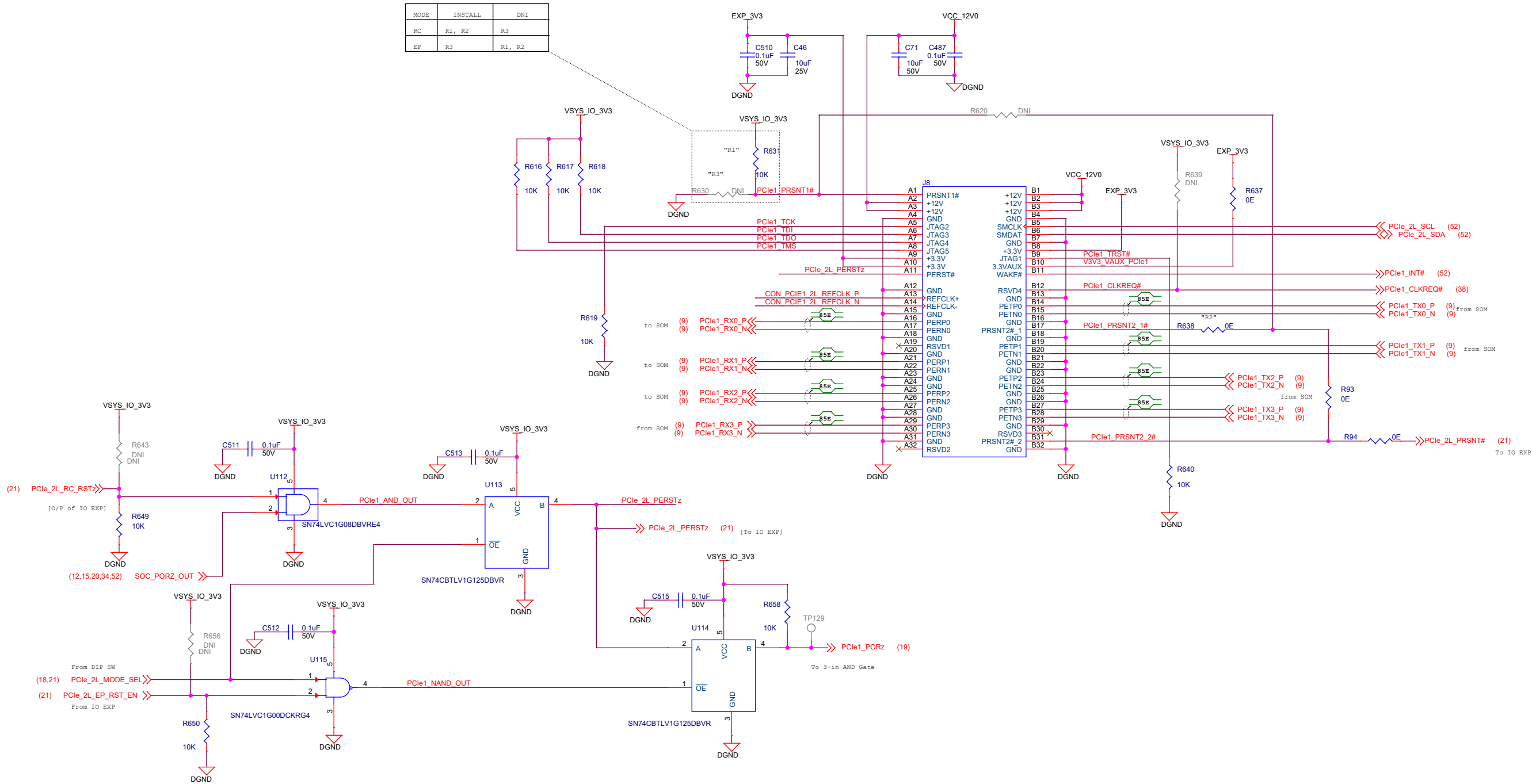
Place R1,R2 close to SOM connector



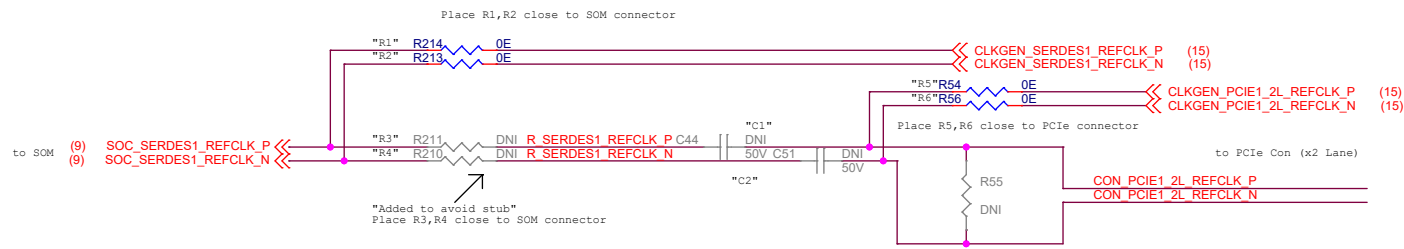
J7 EVM



x4LANE PCIe Interface
x4 Lane PCIe Connector

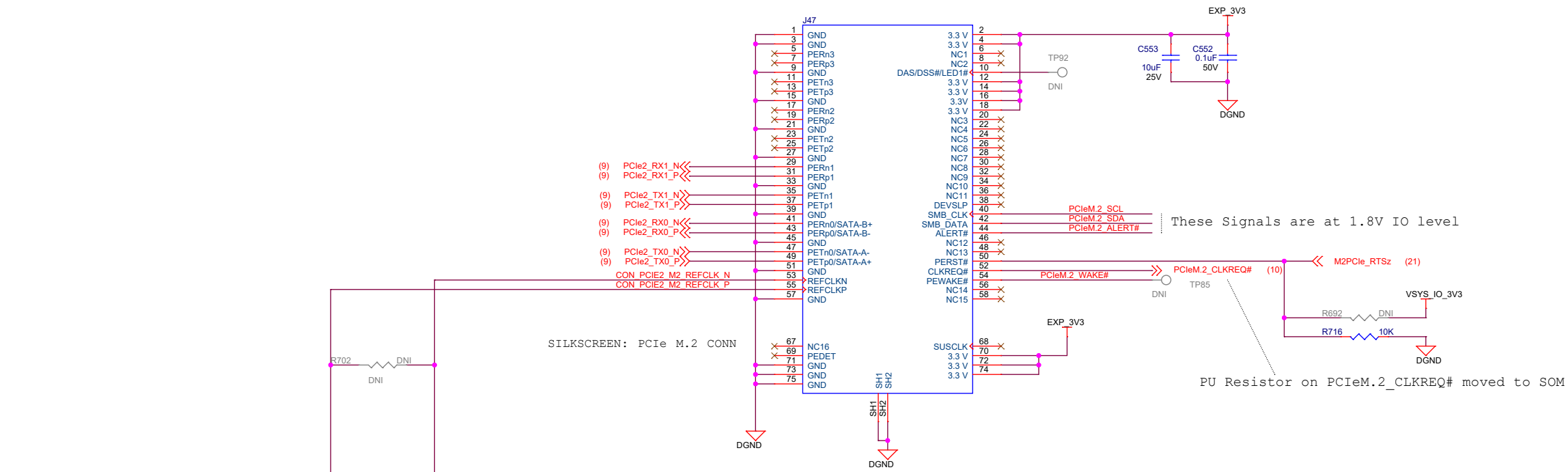


CLOCK ROOT SELECTION

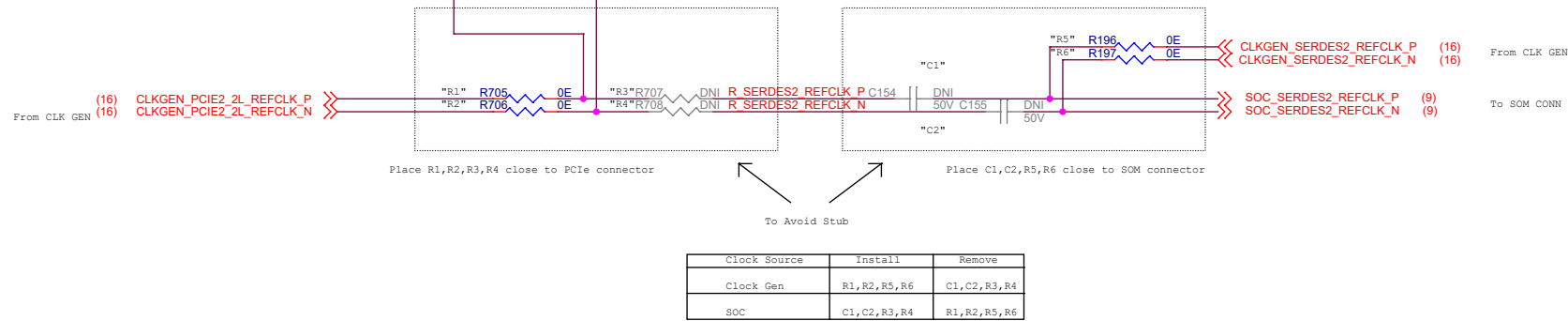


	Install	Remove
PCIe root complex	R1,R2,R5,R6	R3,R4,C1,C2
PCIe end point	R3,R4,C1,C2	R1,R2,R5,R6

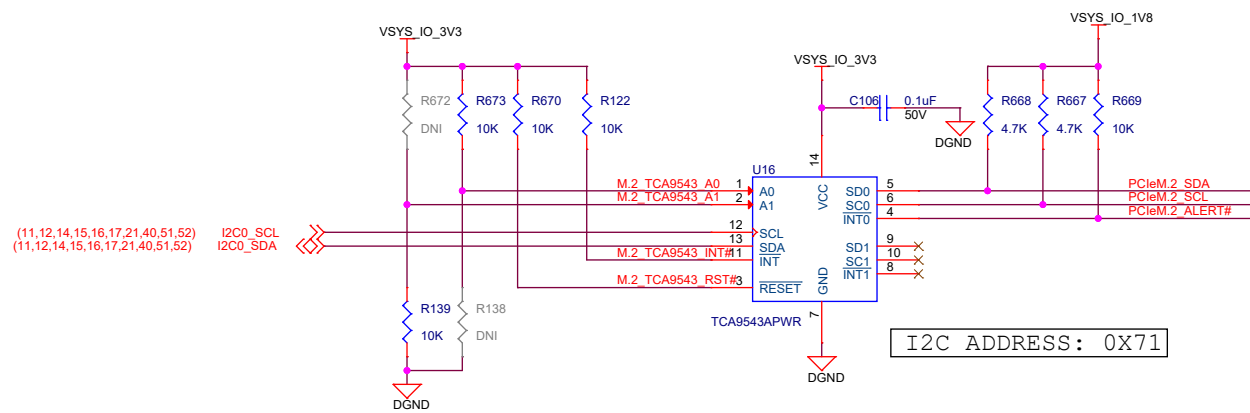
PCie_M.2_INTERFACE



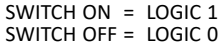
CLOCK ROOT SELECTION



3.3V To 1V8 Level translator



VSYS_3V3


$$\text{DIR} = \text{H: } A \rightarrow B$$

Place TP1 and TP2 with 100mils spacing to insert external jumper

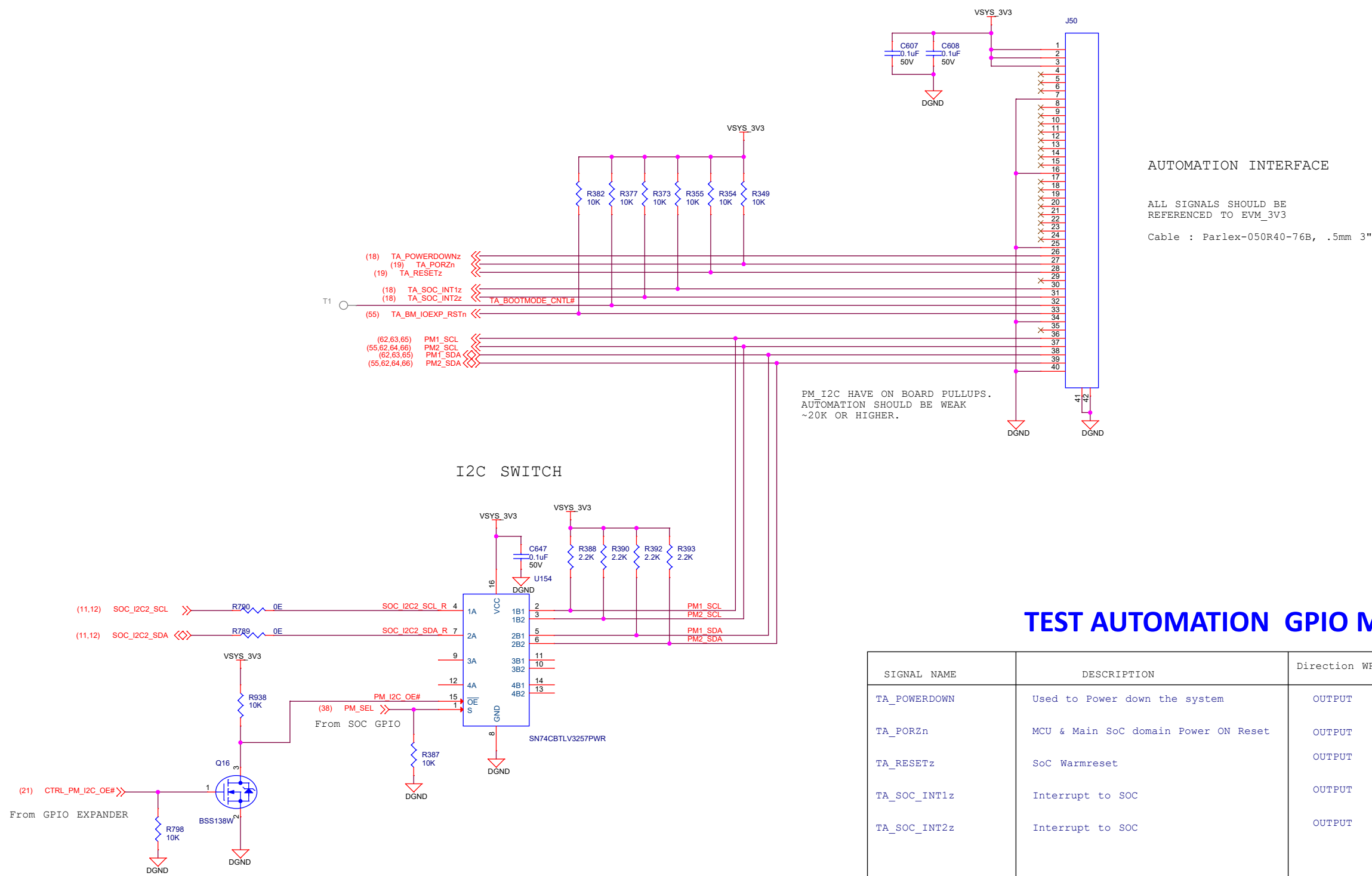
SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0

DIR = H: A \rightarrow B

TA_BM_IOEXP_RSTn	SOC_PORZ_OUT	BOOTMODE Control from Test Automation HDR
HIGH	LOW	Enabled
HIGH	HIGH	Disabled



TEST AUTOMATION HEADER



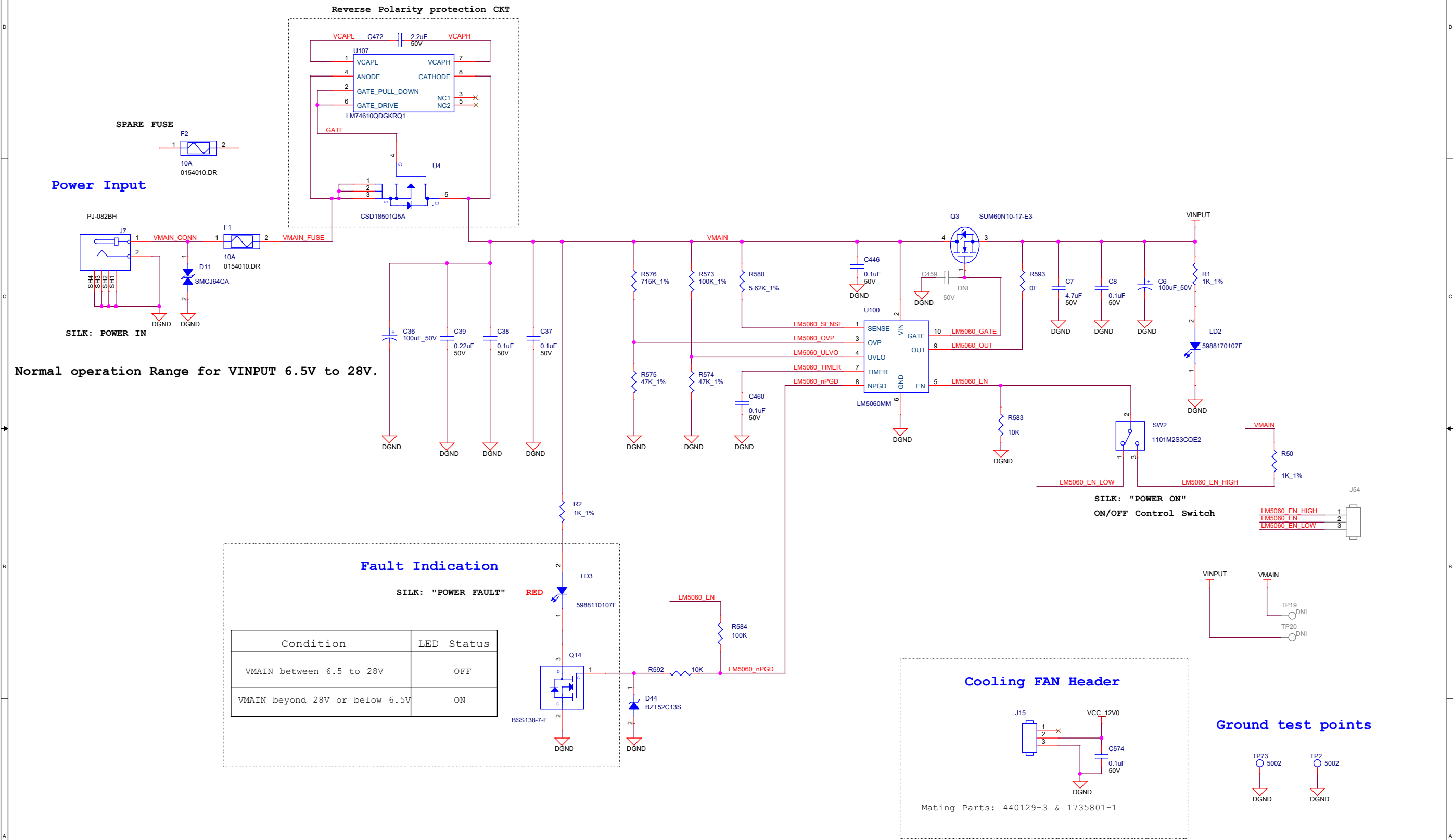
AUTOMATION INTERFACE

ALL SIGNALS SHOULD BE
REFERENCED TO EVM_3V3
Cable : Parlex-050R40-76B, .5mm 3"

TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

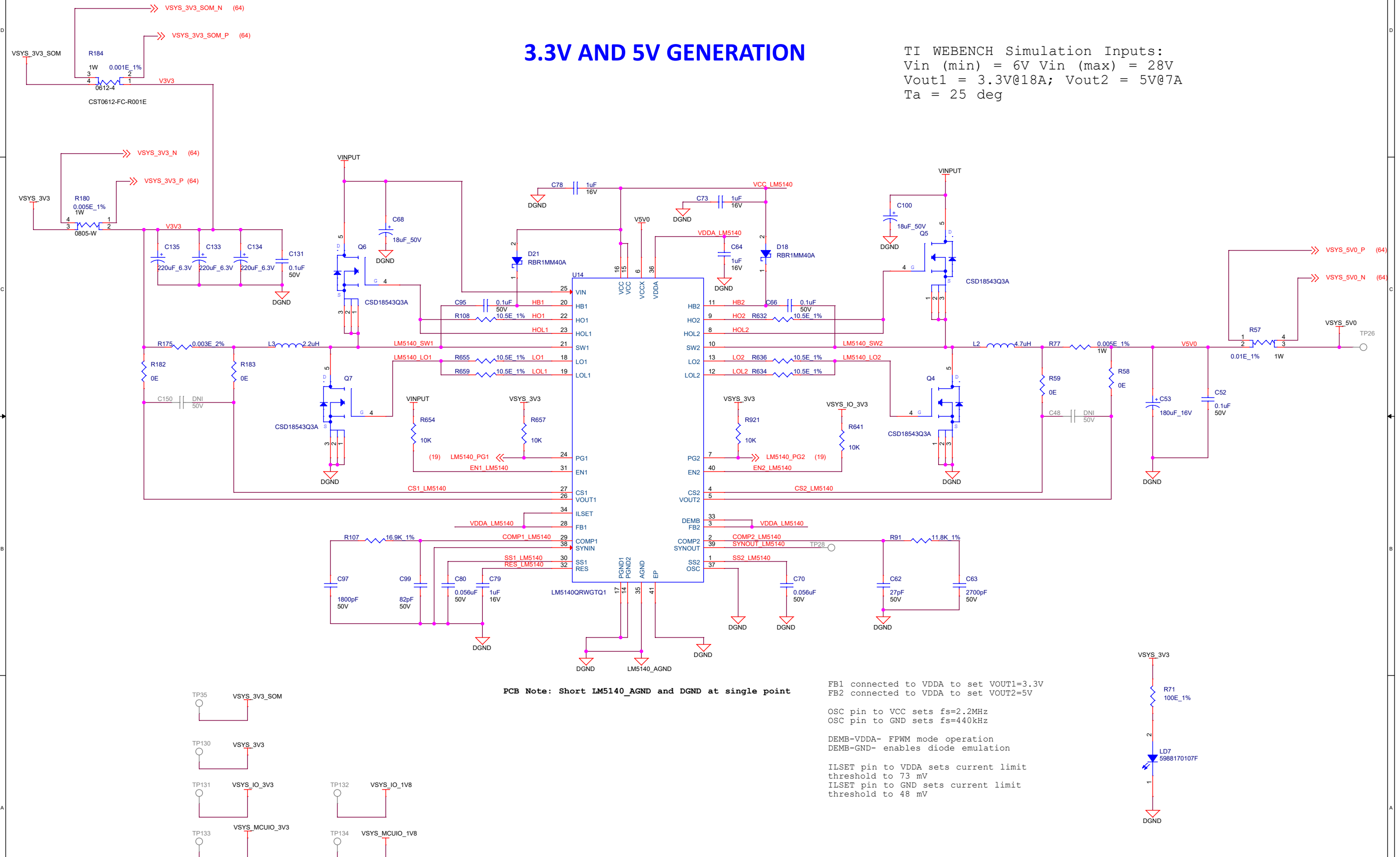
OVER VOLTAGE PROTECTION CIRCUIT




Note: When fault is indicated; set to proper voltage and power cycle the board.

V AND 5V GENERATION

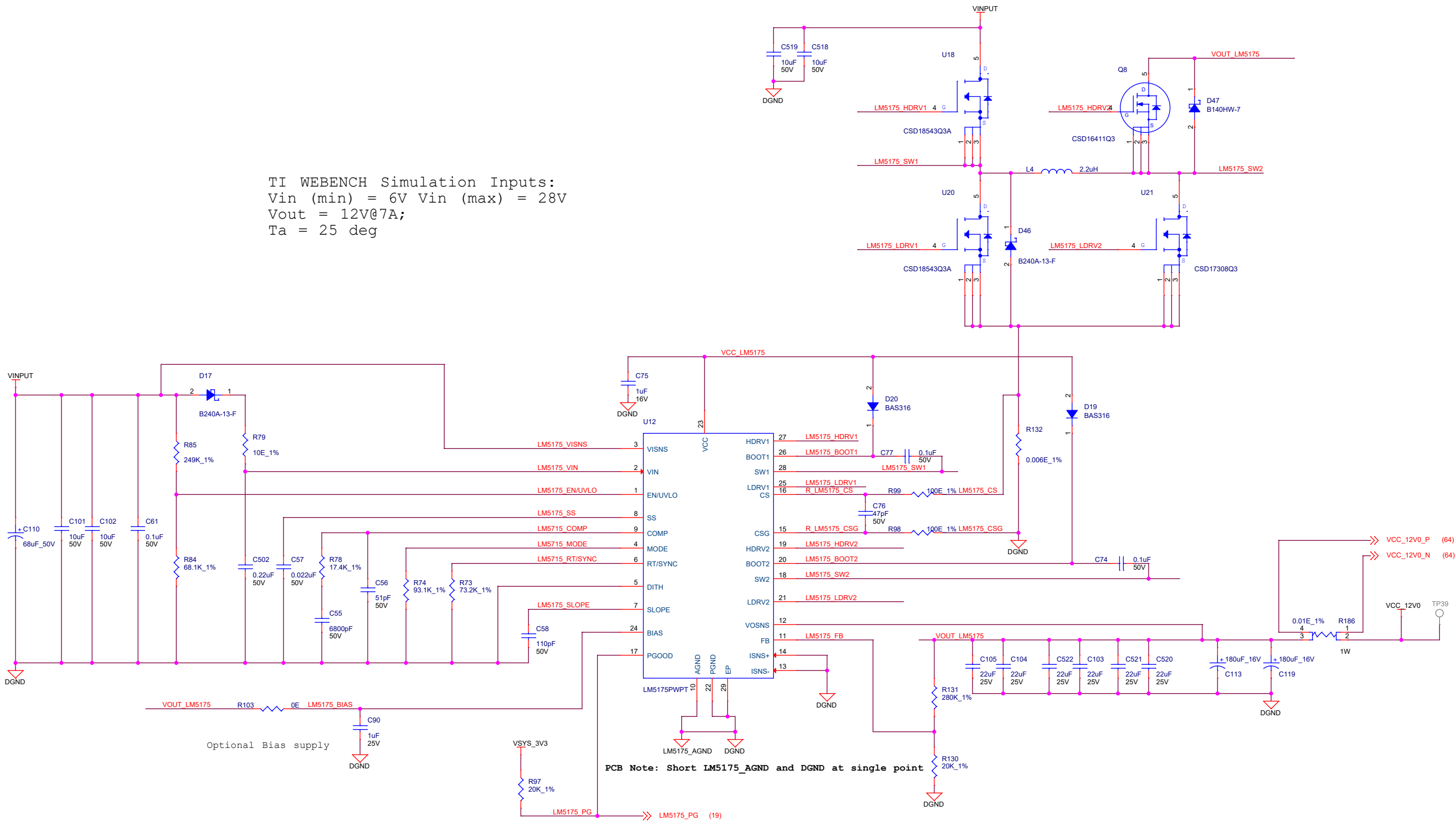
TI WEBENCH Simulation Inputs:
Vin (min) = 6V Vin (max) = 28V
Vout1 = 3.3V@18A; Vout2 = 5V@7A
Ta = 25 deg



Project : J7 EVM		Title POWER SUPPLY #1		
		Size	PROC079 001 J721EXCP01EVM	Rev
		C		A
		Date:	Friday, December 03, 2021	Sheet 58 of 68

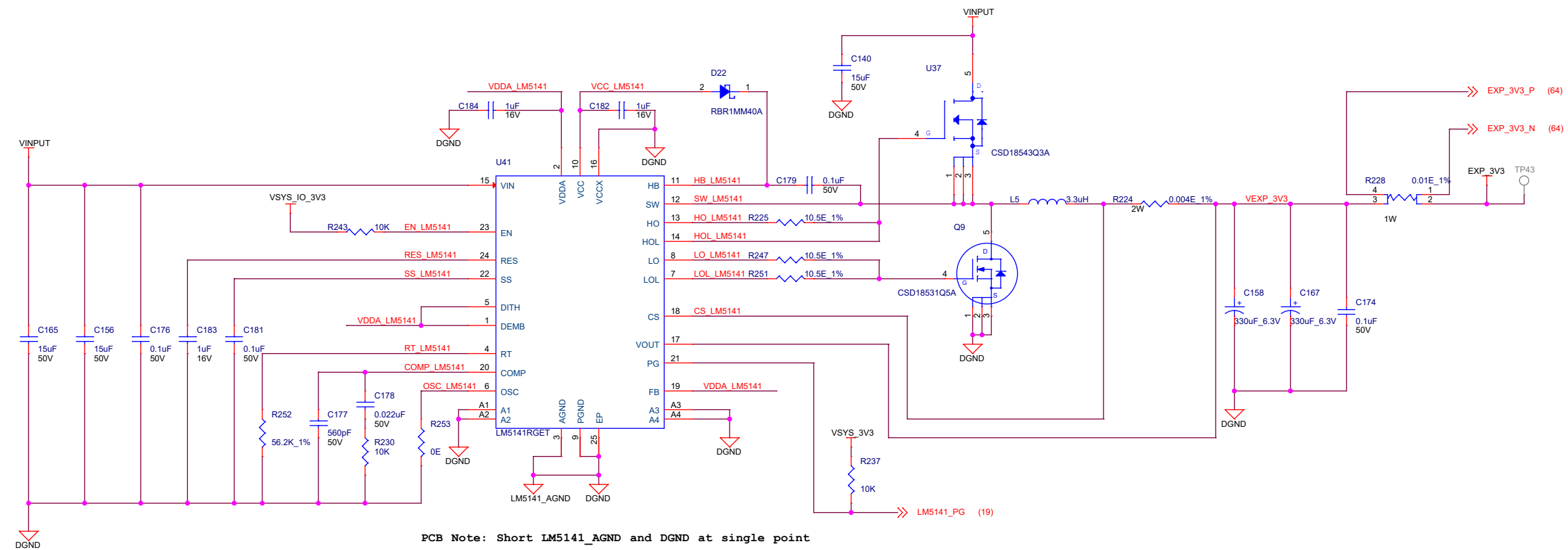
POWER SUPPLY #2

TI WEBENCH Simulation Inputs:
Vin (min) = 6V Vin (max) = 28V
Vout = 12V@7A;
Ta = 25 deg



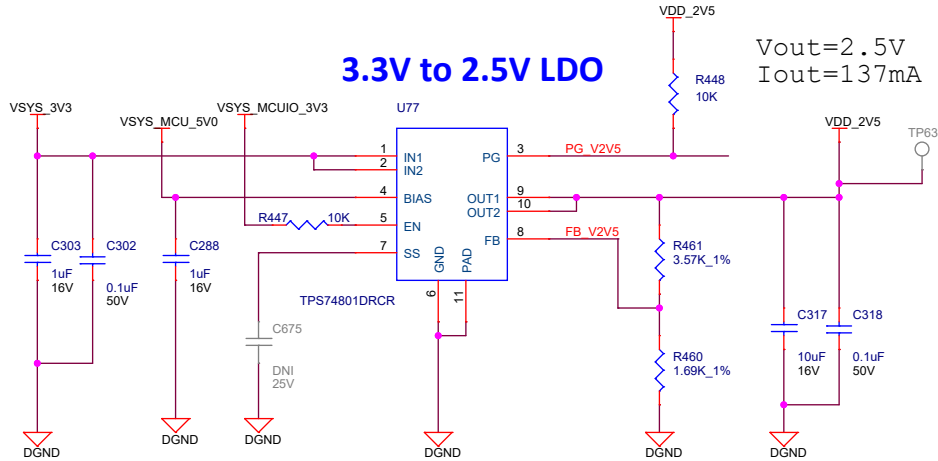
POWER SUPPLY #3

TI WEBENCH Simulation Inputs:
Vin (min) = 8V Vin (max) = 28V
Vout = 3.3V@10A;
Ta = 25 deg



POWER SUPPLY #4

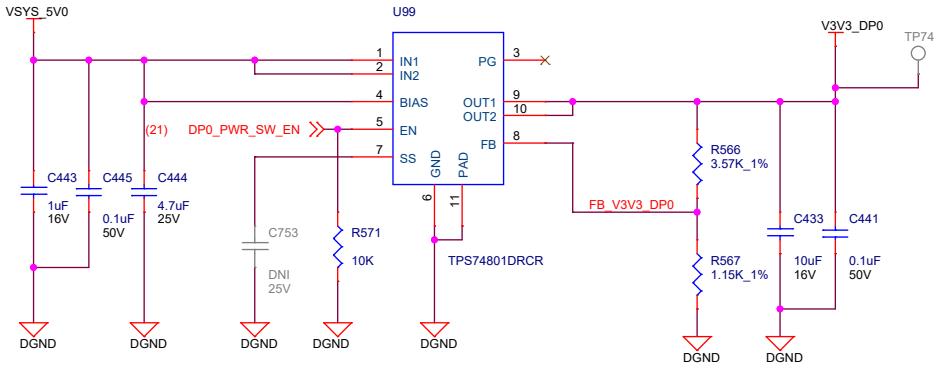
ETHERNET POWER



Display Port0

5V to 3.3V LDO

Vout=3.3V
Iout=500mA

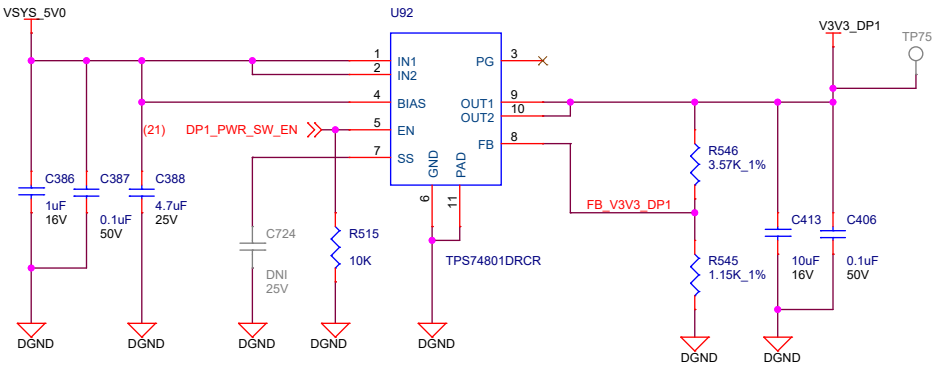


PCB NOTE:Keep 4.7uF capacitor close to BIAS pin.
Keep this circuit close to DP PORT0 Connector

Display Port1

5V to 3.3V LDO

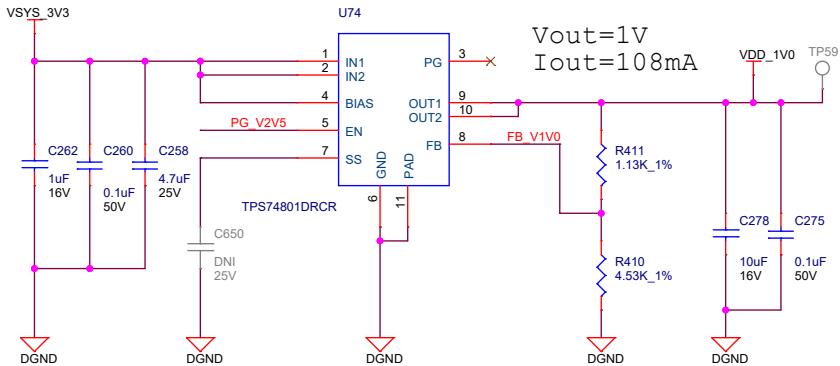
Vout=3.3V
Iout=500mA



PCB NOTE:Keep 4.7uF capacitor close to BIAS pin.
Keep this circuit close to DP PORT1 Connector.

3.3V to 1.0V LDO

Vout=1V
Iout=108mA

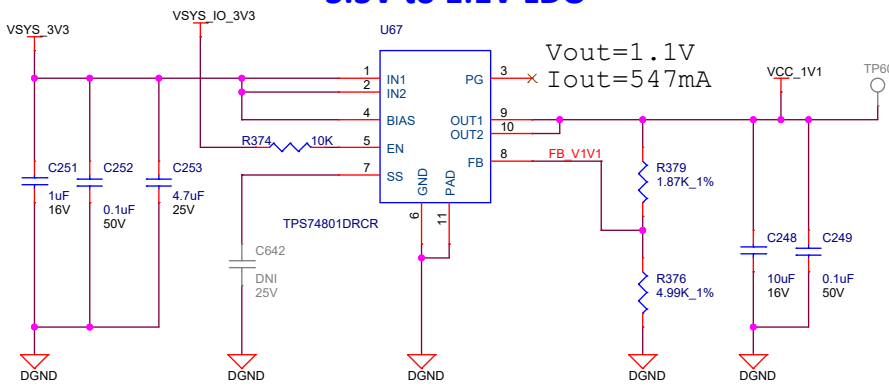


PCB NOTE:Keep 4.7uF capacitor close BIAS pin

FPD-LINK4 and USB HUB POWER

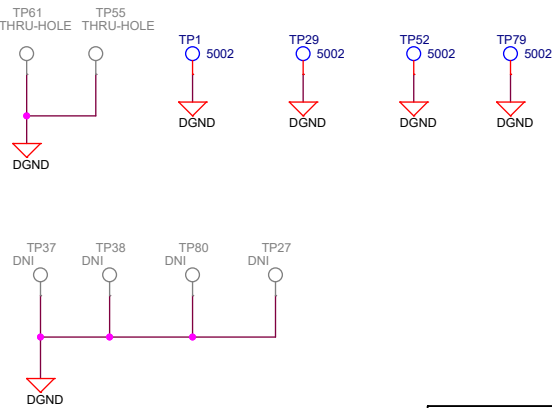
3.3V to 1.1V LDO

Vout=1.1V
Iout=547mA



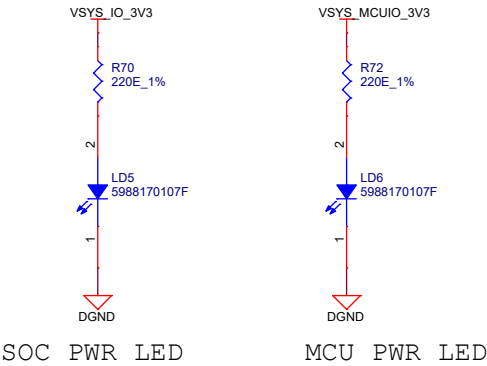
PCB NOTE:Keep 4.7uF capacitor close BIAS pin

GROUND TEST POINTS



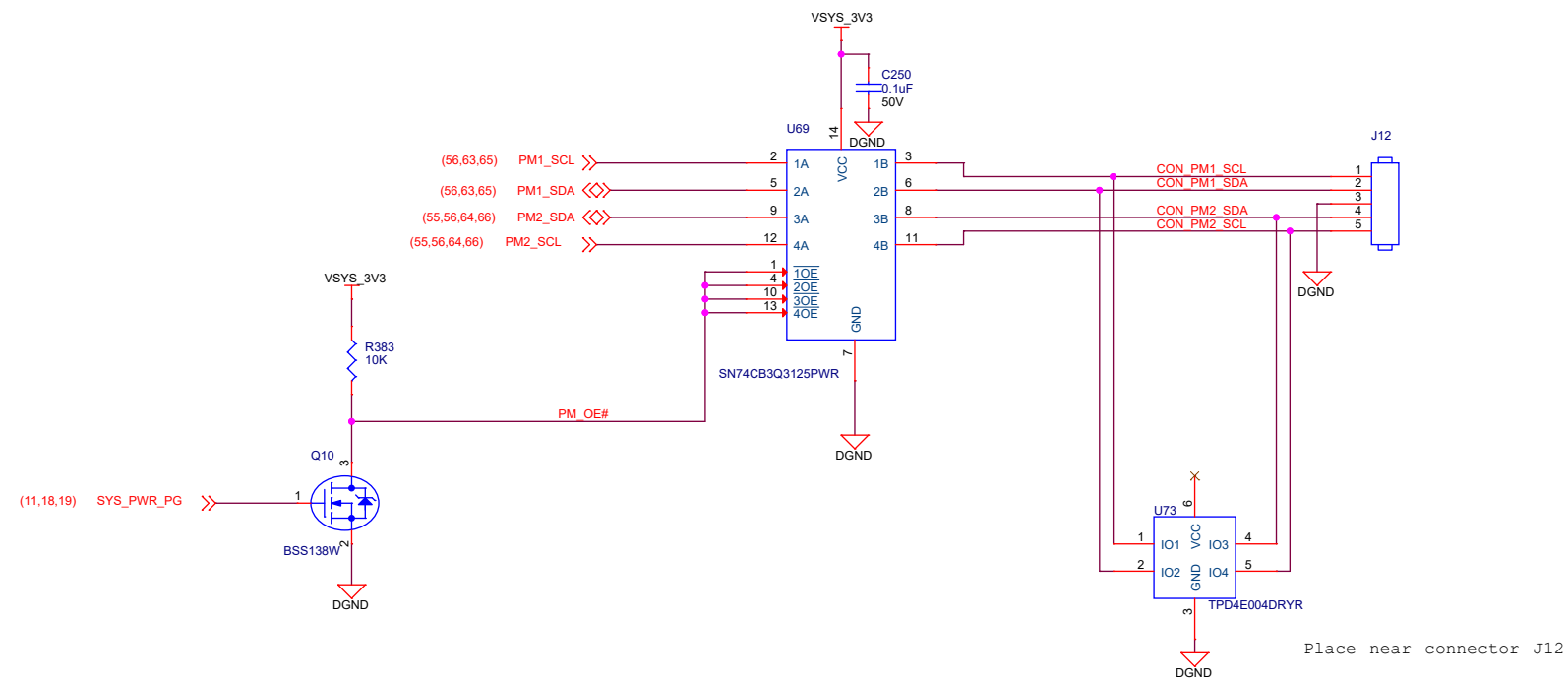
PCB NOTE: Spread the SMD
test points Top and Bottom
Side of PCB

POWER INDICATION LED's



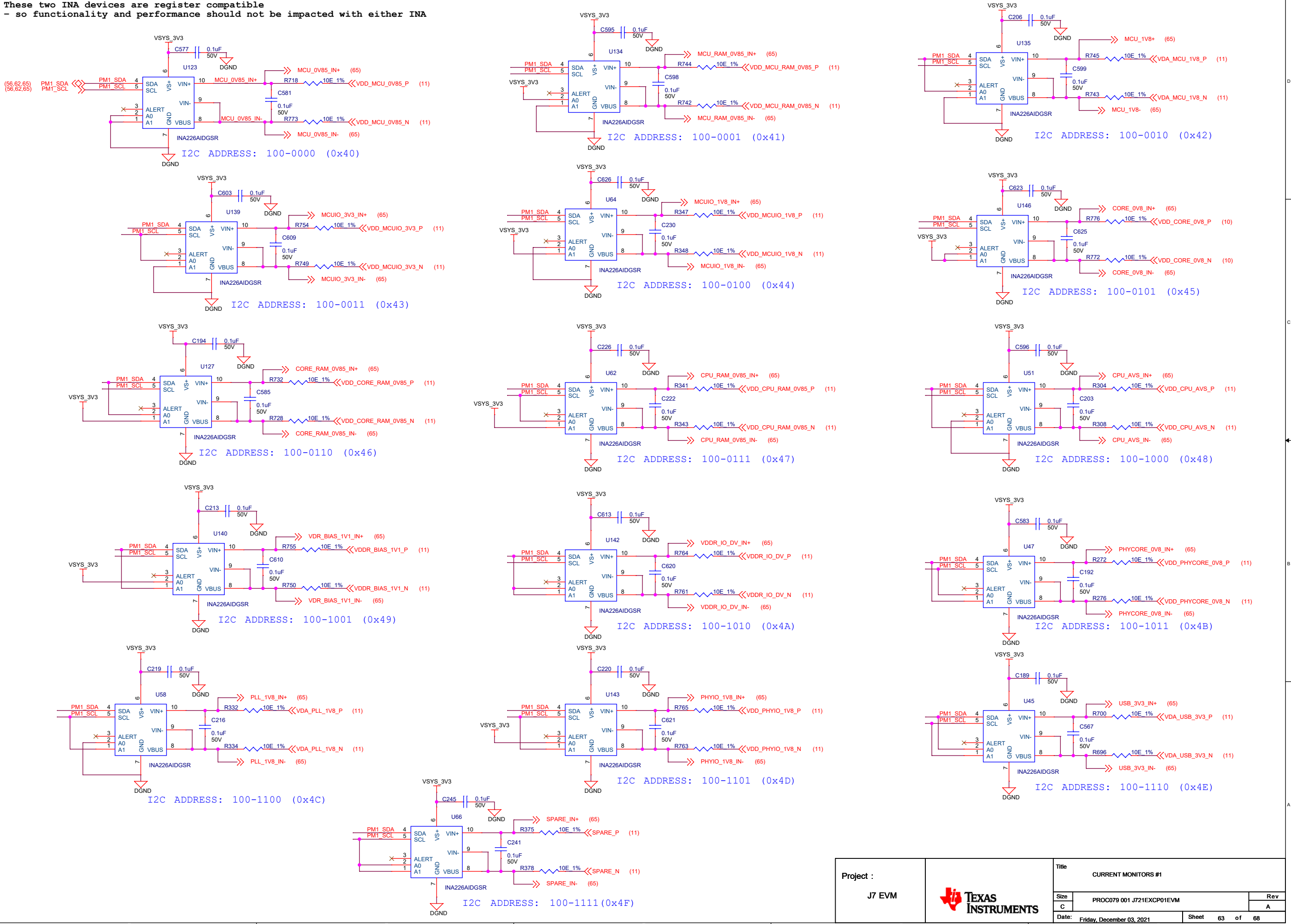
Project : J7 EVM		Title POWER SUPPLY #4	
		Size C	Rev A
		Date: Friday, December 03, 2021	Sheet 61 of 68

EXTERNAL POWER MEASUREMENT WITH ISOLATION



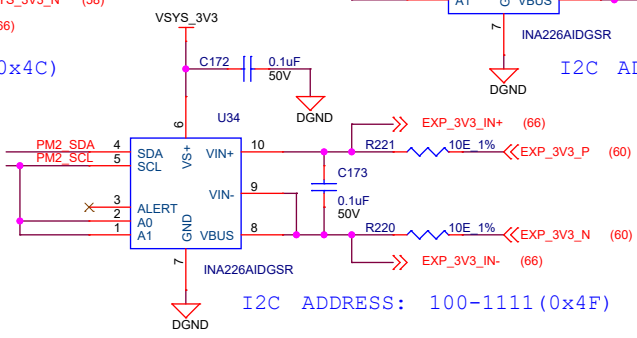
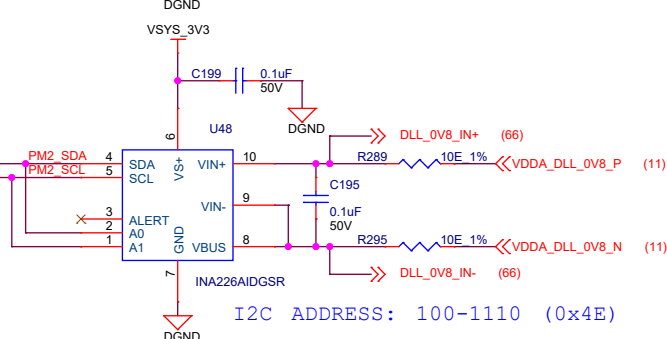
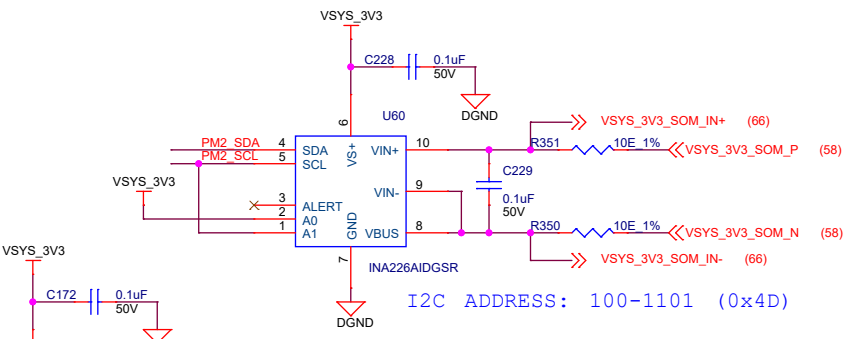
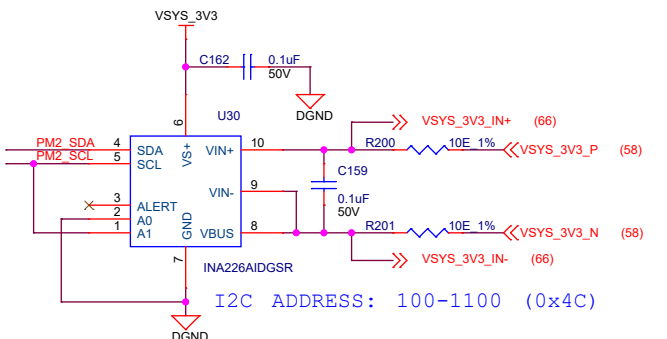
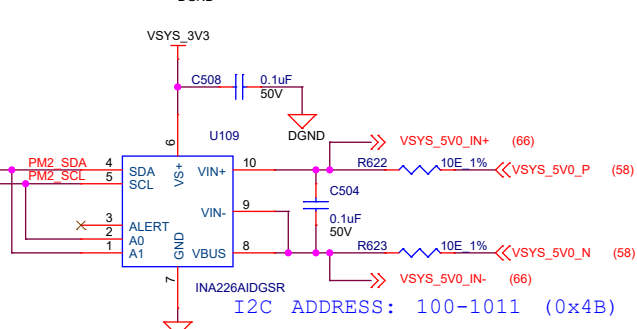
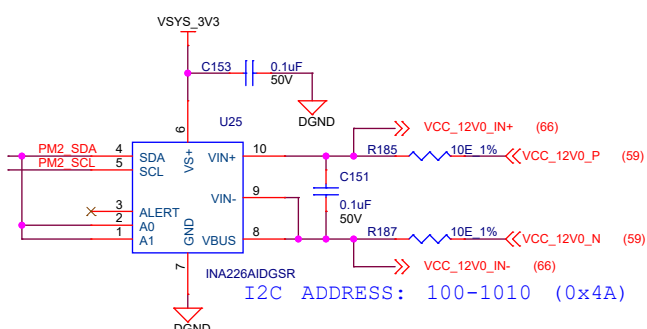
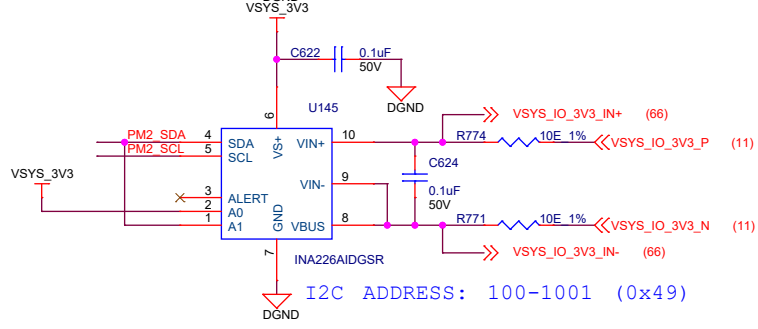
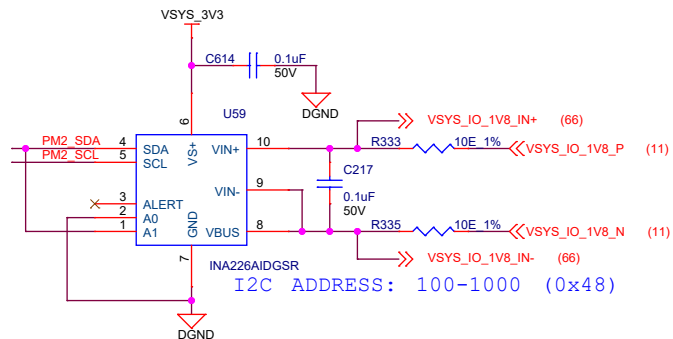
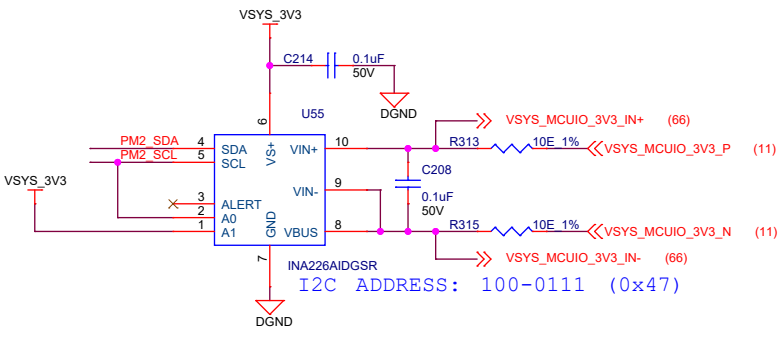
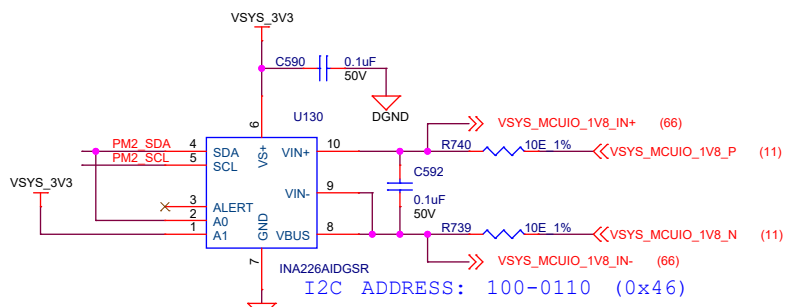
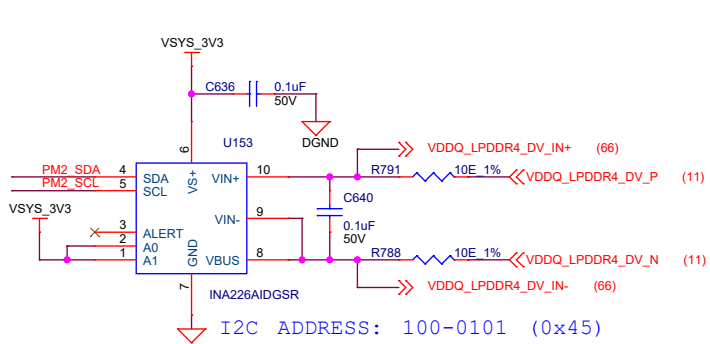
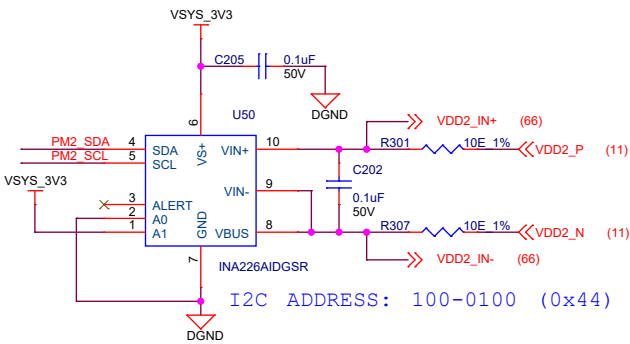
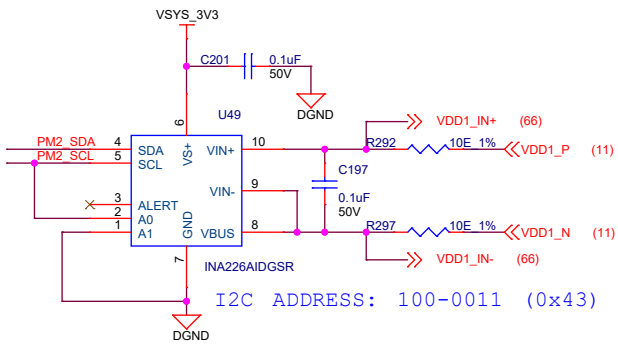
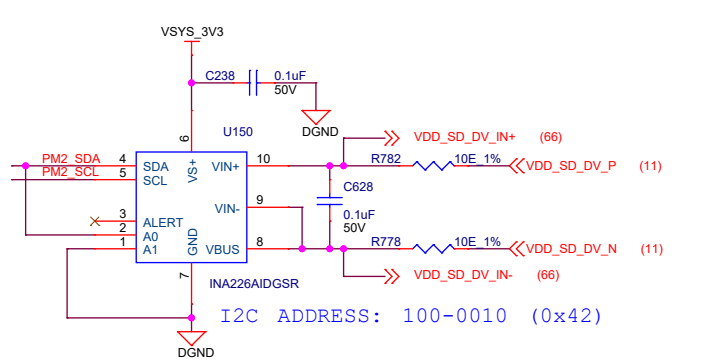
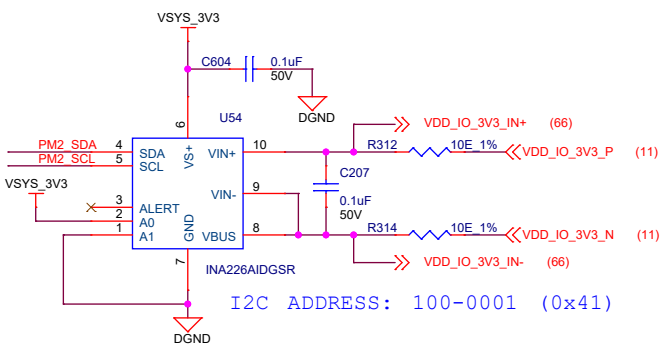
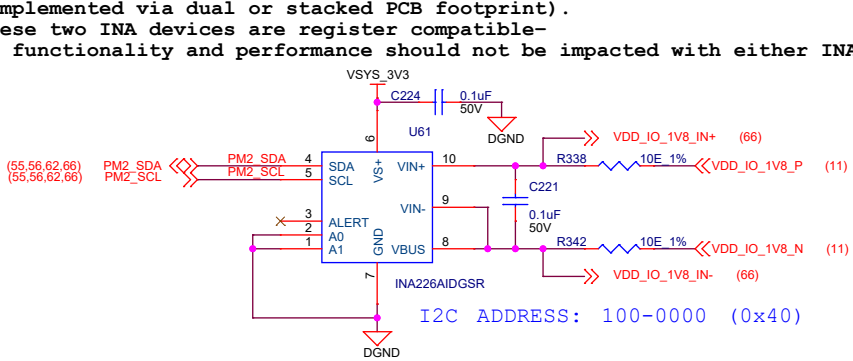
Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible - so functionality and performance should not be impacted with either INA

CURRENT MONITORS #1



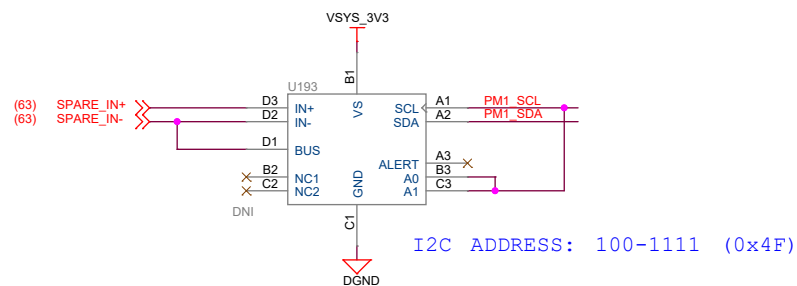
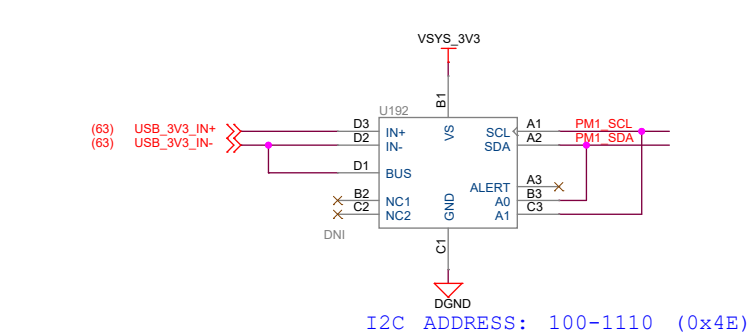
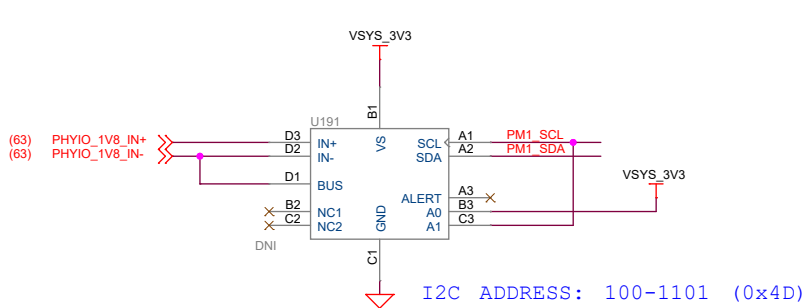
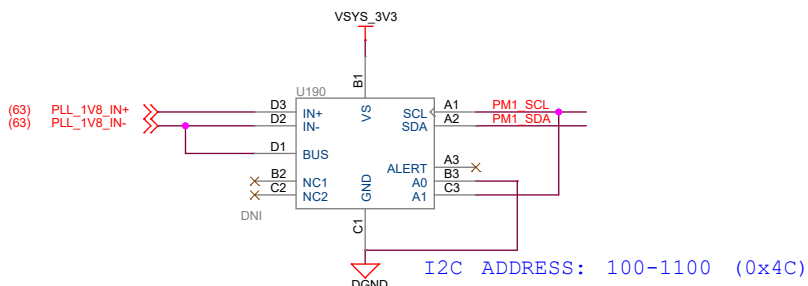
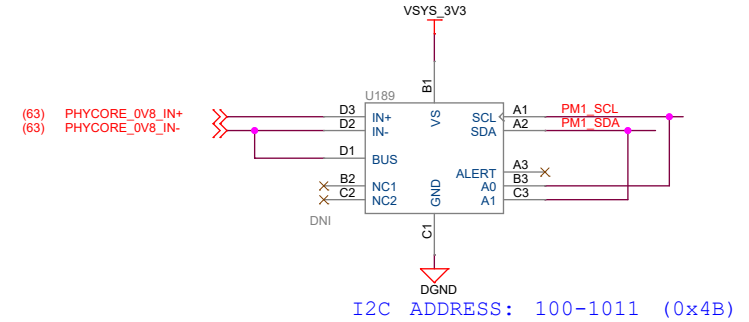
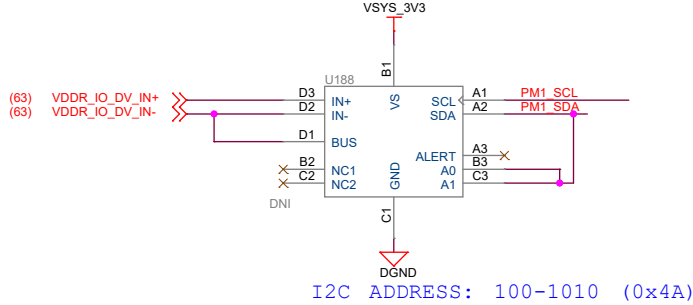
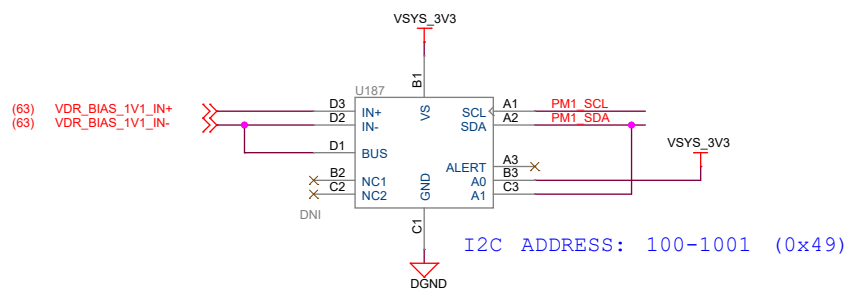
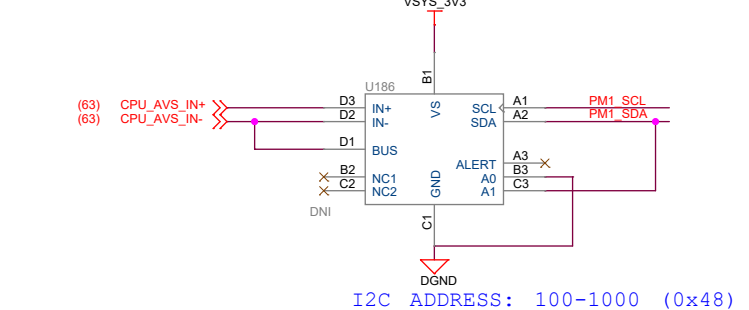
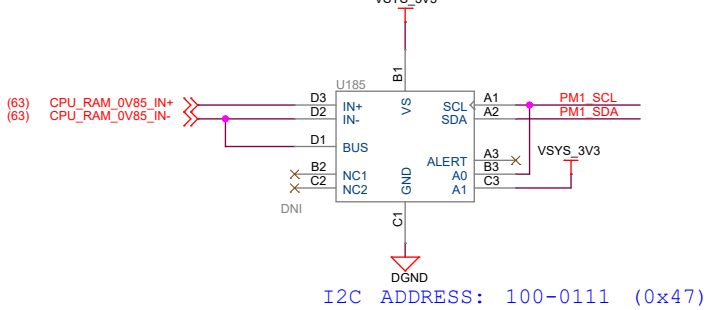
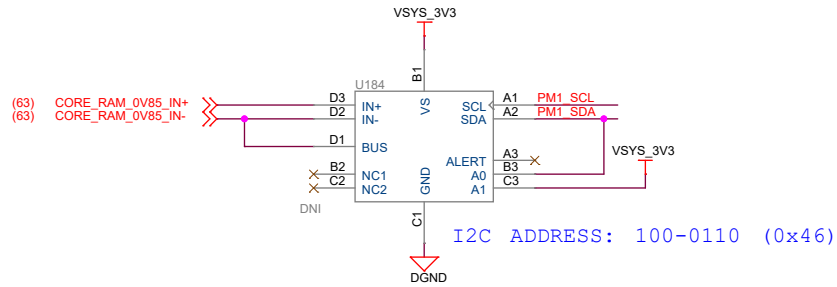
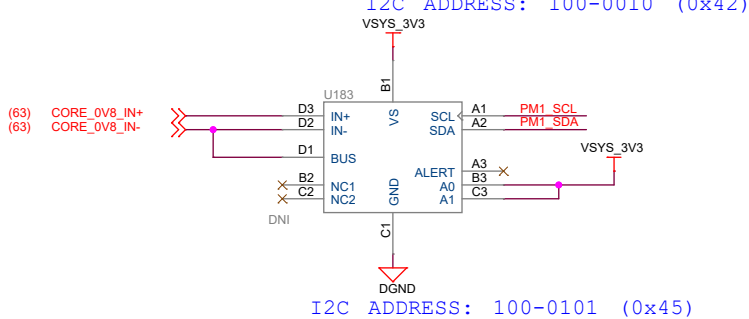
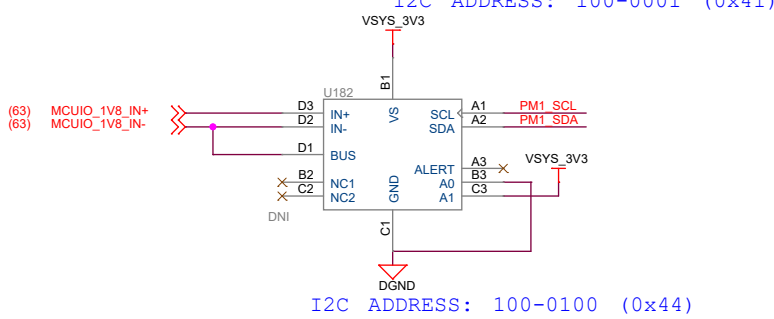
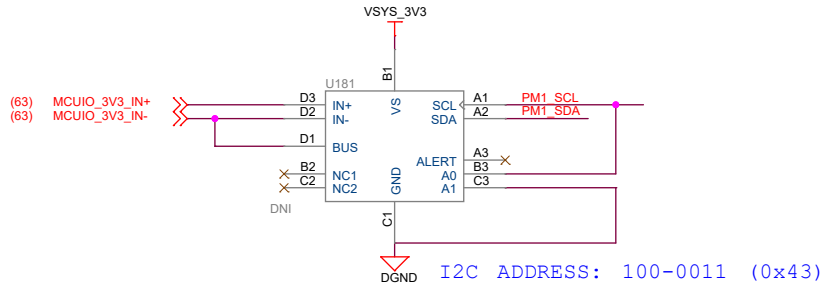
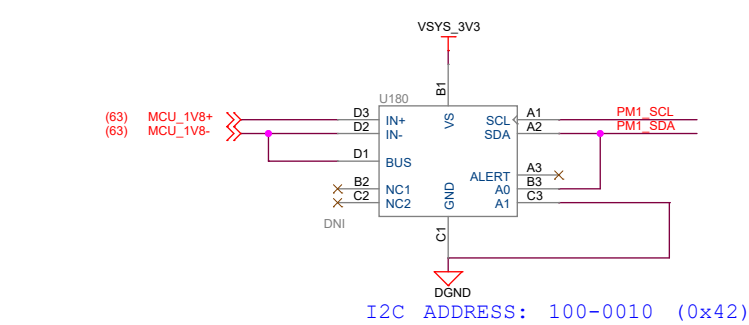
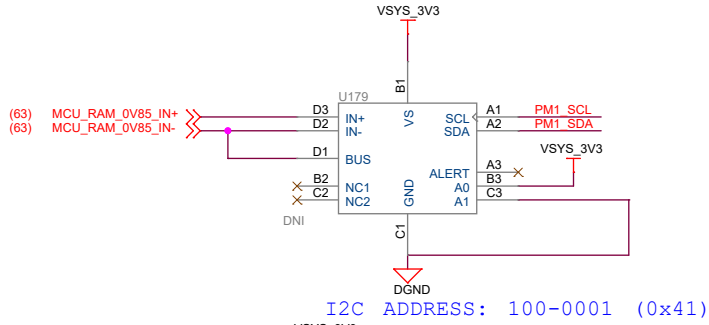
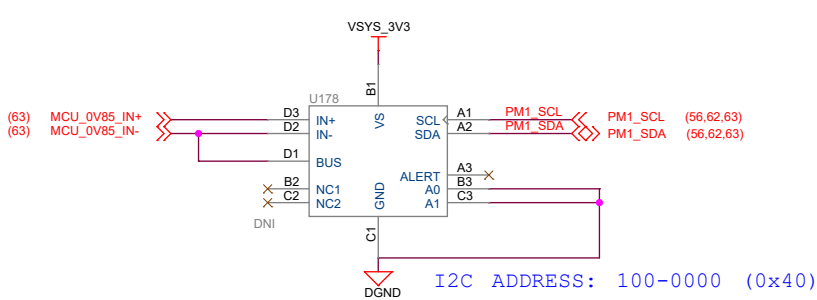
Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA


CURRENT MONITORS #2



CURRENT MONITORS - INA231

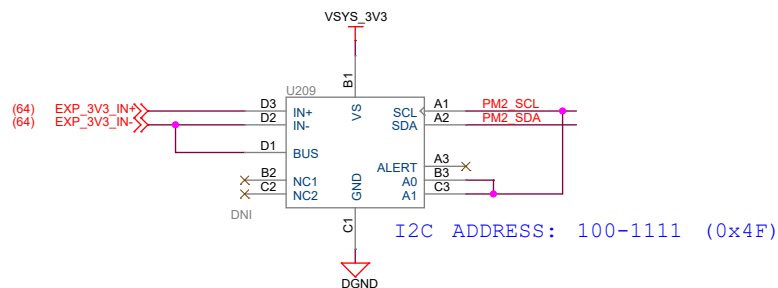
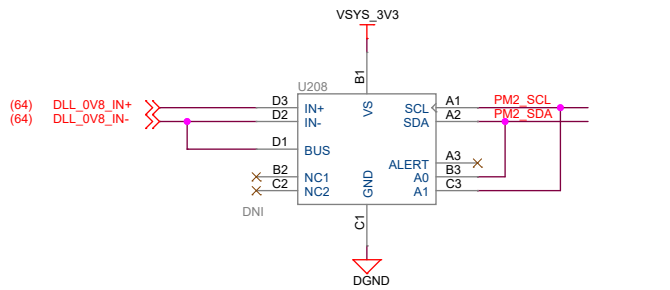
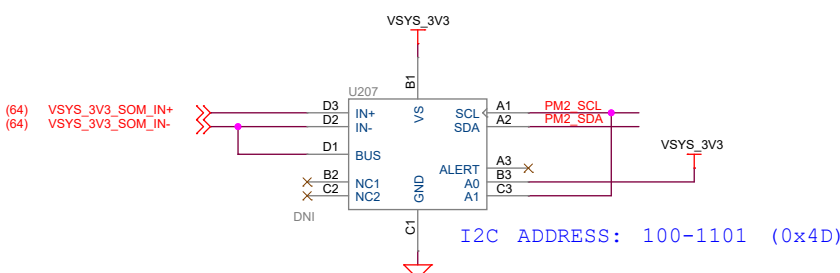
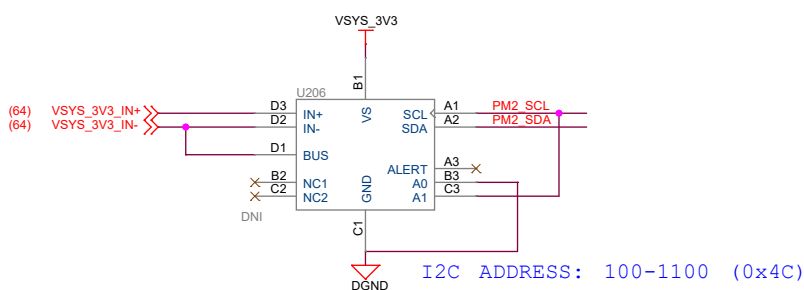
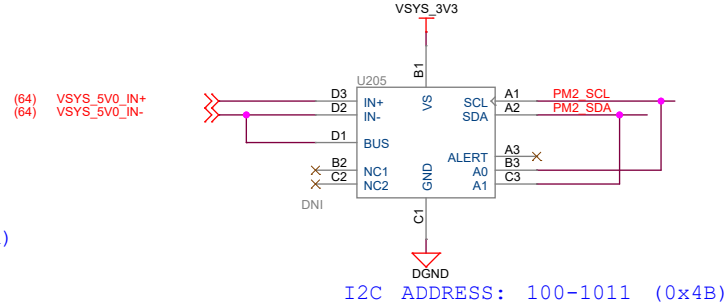
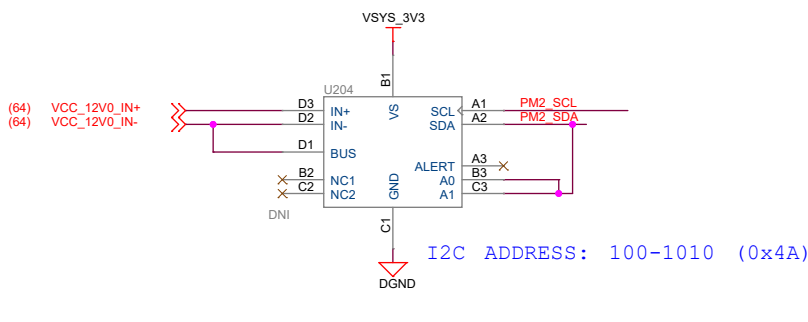
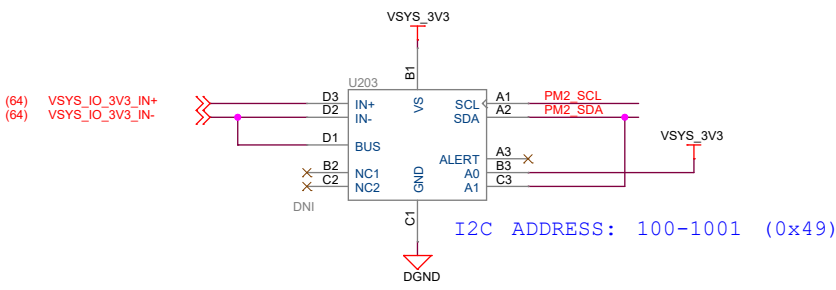
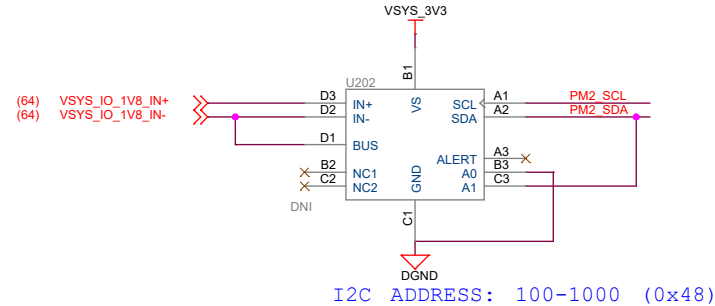
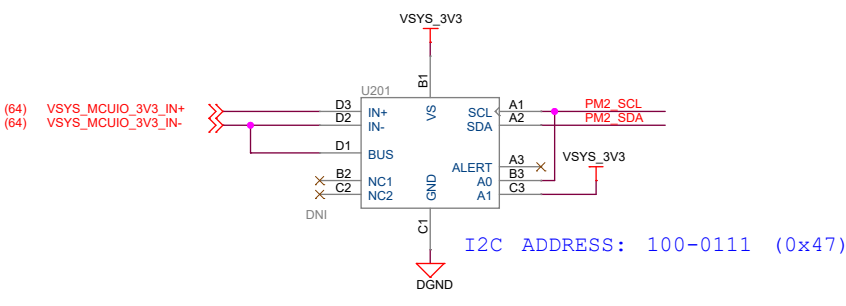
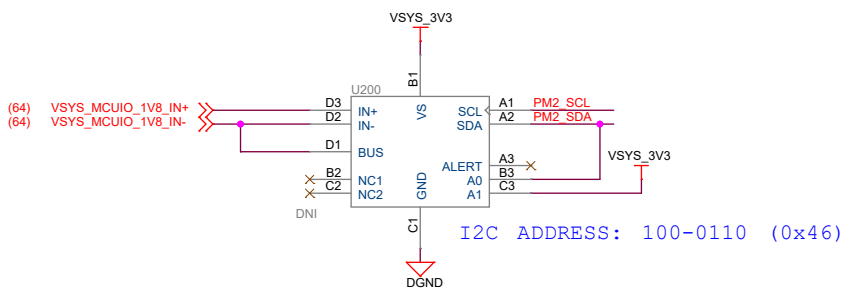
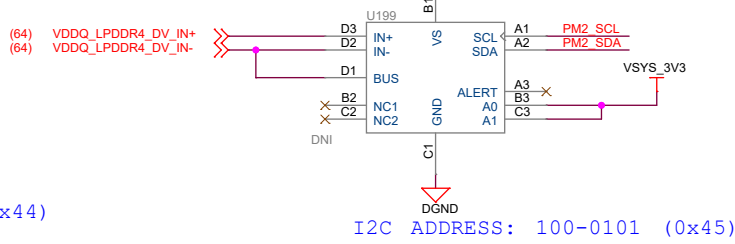
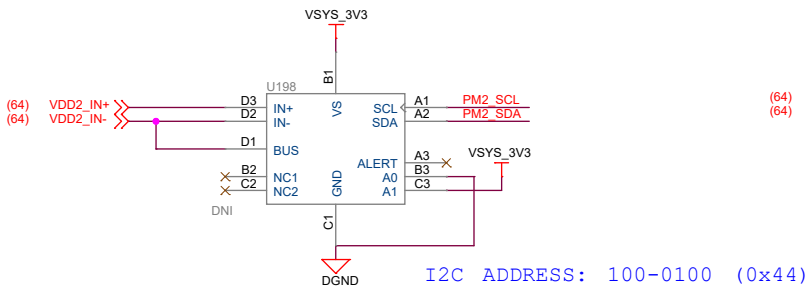
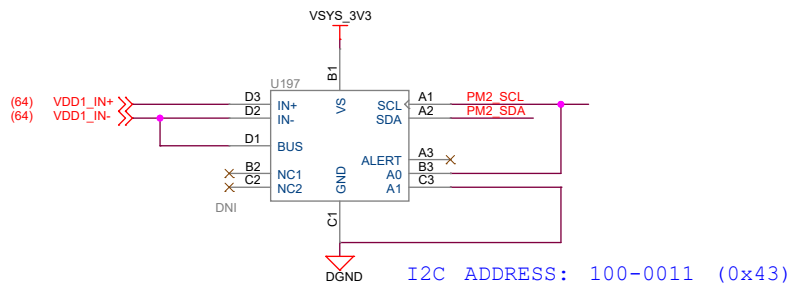
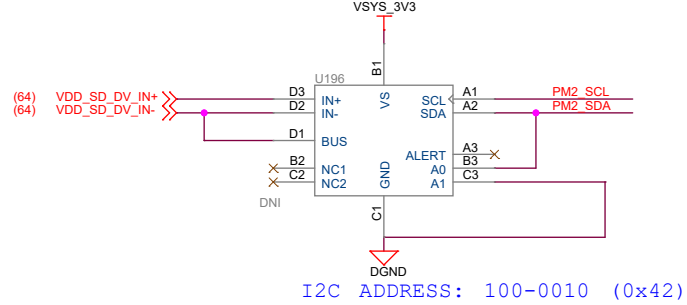
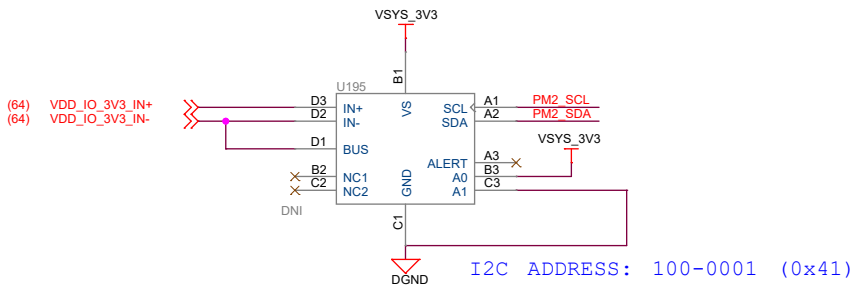
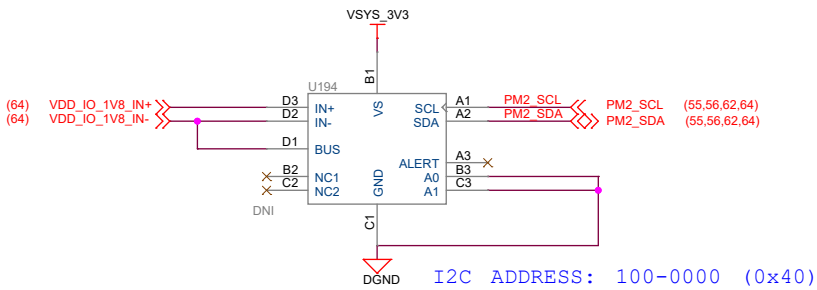
Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA



Project : J7 EVM		Title CURRENT MONITORS#1- INA231			
		Size	PROC079 001 J721EXCP01EVM	Rev	
		C		A	
		Date:	Friday, December 03, 2021	Sheet	65

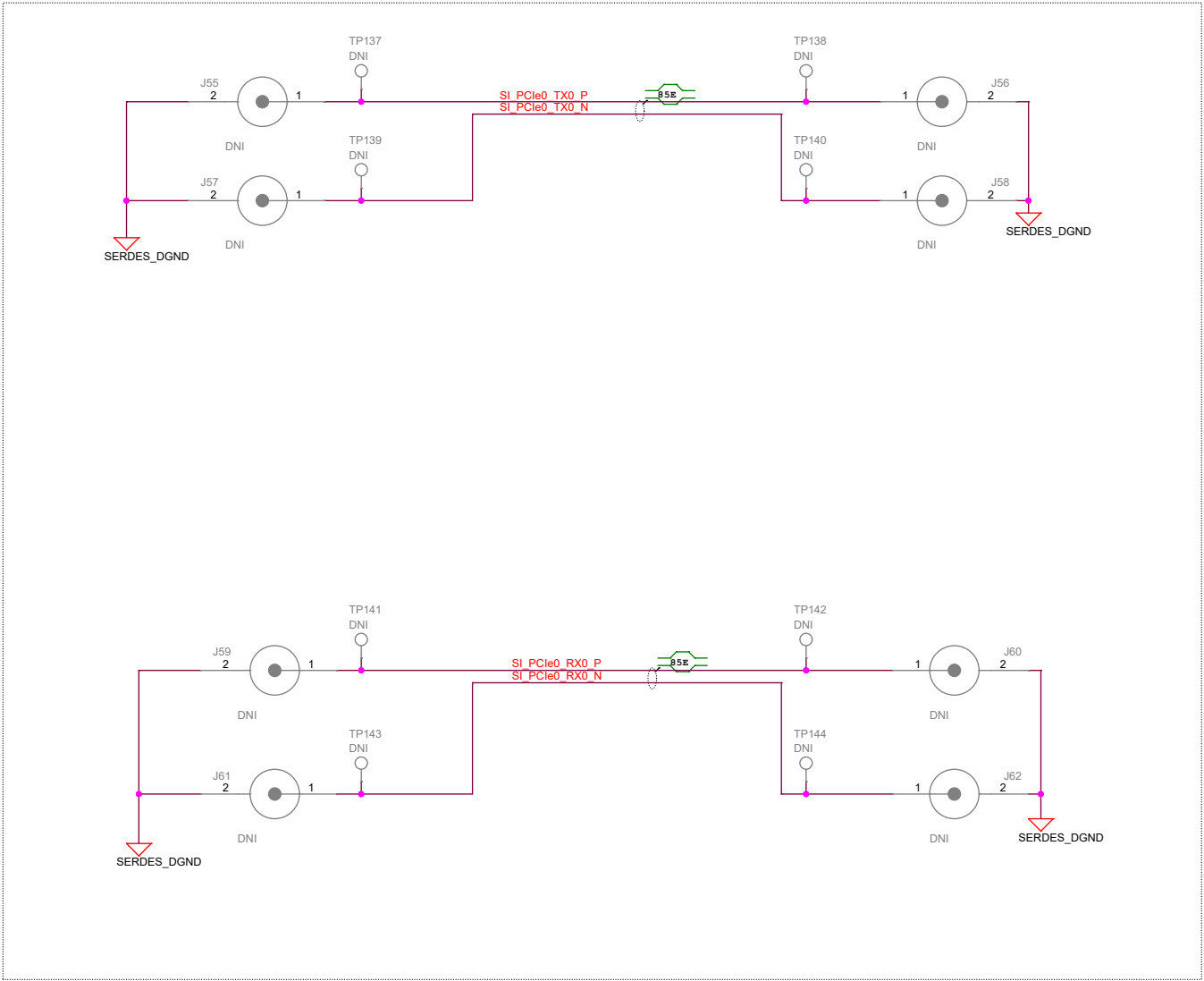
Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

CURRENT MONITORS - INA231



SI_SIMULATION_COUPON_BD

Test coupon not part of EVM design, to be used for TI test only

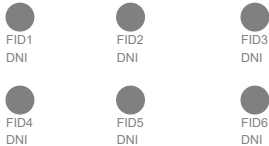


HARDWARE SCHEMATICS

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

FIDUCIALS



LABELS

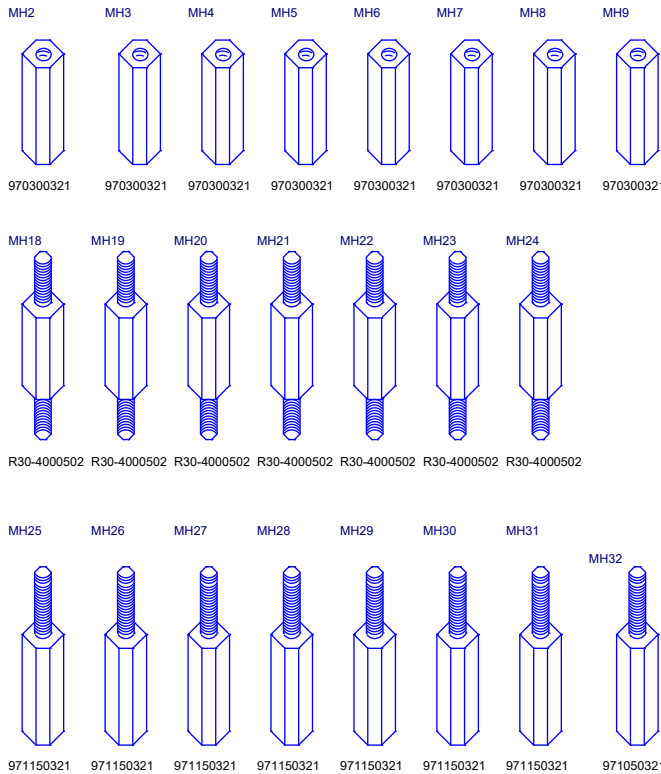
Board Serial No.



Assembly Revision.



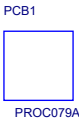
STANDOFFS



JACK SCREWS



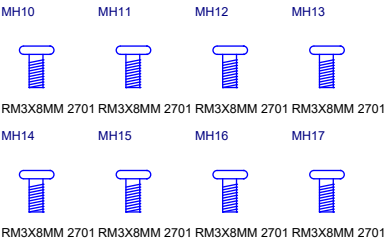
CPB BARE PCB



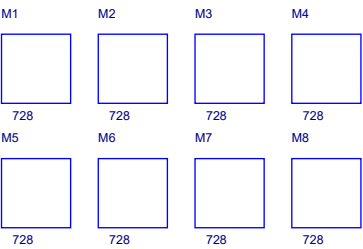
QUAD PORT ETH EXP ASSEMBLED PCB



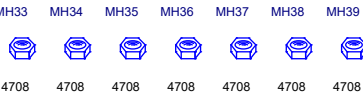
SCREWS



RUBBER FEET



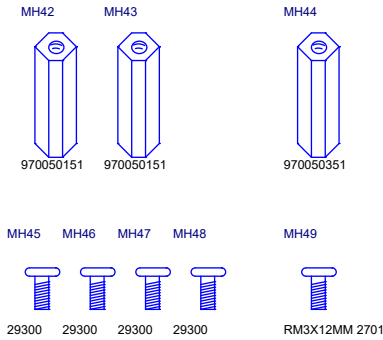
HEX NUT



SCREW & WASHER FOR PCIe M.2



SCREW & WASHER for ENET EXP BRD



LOGOs

