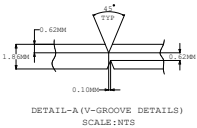


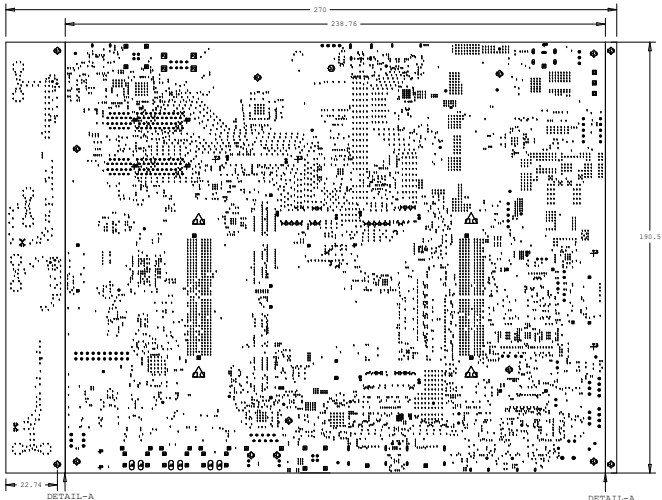
- FACTORY FABRICATE PCB IN ACCORDANCE WITH IPC-6012C, CLASS 2 PER IPC-6011. PCB SHALL BE MANUFACTURED USING 1-EPXED OR EQUIVALENT.
2. MATERIALS:
1. LAMINATE AND PREPREG (B-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/1126.
(MIN/100 170)
 2. COPPER THICK TO BE IN ACCORDANCE WITH IPC-M-150, UNLESS OTHERWISE SPECIFIED.
ALL COPPER WEIGHT FOR INNER LAYERS AND EXTERNAL LAYERS SHALL FOLLOW THE 1126.
THE COPPER FOLY THICKNESS TOLERANCE SHALL BE AS PER IPC 6012B TABLE NO.3-7 AND 3-8.
3. ALL HOLES SHALL BE LOCATED WITHIN 0.150MM DIAMETER OF THIRD POSITION.
LAYERS TO LAYER REGISTRATION SHALL BE WITHIN 0.125MM.
4. NOW AND TRIST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTH.
5. CONDUCTOR WITH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCREASE FOR MATCHING IMPEDANCE MINIMUM SHALL APPROVE THE IDENTIFIED MISTAKE CREATING.
6. TRACE WITH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
7. AUTHORIZED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
8. FINISH:
1. ALL EXPOSED CONDUCTIVE PATTERN AREA NOT COVERED WITH SOLDER MASK BE ENIG.
ELECTROLESS NICKEL/IMMERSION GOLD, ELECTROLESS NICKEL SHALL BE 3-6 MICRONS, THICKNESS IMMERSION GOLD THICKNESS SHALL BE 0.44-0.58 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
 2. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-B-84S, CLASS B, TO BOTH SIDES OF THE BOARD OVER BARE COPPER.
VIA HOLES THAT HAVE MASK SHALL BE FILLED WITH NON CONDUCTIVE INK.
 3. ALL OTHER VIA HOLES SHALL BE FILLED WITH NON CONDUCTIVE INK AND COVERED WITH SOLDER MASK.
ONLY SOLDERMASK THICKNESS THAT ARE 0.08(0.0031) PER SIDE SHALL BE REDUCED IF REQUIRED.
ALL OTHER SOLDER MASK THICKNESS SHALL NOT BE DEGRADED. DIFFERENT COLOURS OF SOLDER MASK SHALL BE GREEN.
9. SILSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILSCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERABLE AREAS.
10. SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 20UM (0.00079).
5. ALL HOLES SURROUNDED BY LAND <0.015" SHALL BE COMPLIANT TO IPC612, CLASS 2.
6. MARKING:
1. BOARD SHALL MEET THE REQUIREMENTS OF UL-756 WITH FLAMMABILITY RATINGS OF MINIMUM 94V-0. UL LOGO, UL FILE NUMBER, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTERS SHALL BE RENDERED IN SILKSCREEN.
7. TEST REQUIREMENTS:
1. 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC612-0-356 NET LIST FOR OPENS AND SHORTS.
8. THERIVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
9. TRIM DROPS SHALL BE ACROSS ON INTERNAL AND EXTERNAL LAYER FOR ALL THE VIA'S AND THROUGH HOLE PADS.
10. FINISHED PCB THICKNESS SHALL BE 0.071" \pm 0.004".
11. MIN TRACE WIDTH/SPACING ON BOARD IS 0.003"/0.003".
12. ALL THE IMPEDANCE SHALL BE MATCHED AS PER IMPEDANCE TABLE WITH \pm 10% TOLERANCE.
13. ALL UNCONNECTED VIA'S SHALL BE SUPPRESSED IN INTERNAL LAYERS.

DRILL CHART: TOP TO BOTTOM						
FIGURE	ALL UNITS ARE IN MILS					
	SIZE	COLLAPSE	PLATED	QTY		
1	8.0	+3.0/+4.0	PLATED	4608		
2	12.0	+3.0/+4.0	PLATED	10		
3	28.0	+3.0/+3.0	PLATED	132		
4	32.0	+2.0/+2.0	PLATED	8		
5	32.0	+2.0/+3.0	PLATED	7		
6	36.0	+3.0/+3.0	PLATED	18		
7	40.0	+3.0/+3.0	PLATED	24		
8	44.0	+2.0/+2.0	PLATED	97		
9	56.0	+3.0/+3.0	PLATED	2		
10	60.0	+3.0/+3.0	PLATED	18		
11	66.0	+3.0/+3.0	PLATED	11		
12	68.0	+3.0/+3.0	PLATED	3		
13	90.0	+3.0/+3.0	PLATED	4		
14	118.0	+3.0/+3.0	PLATED	1		
15	34.0	+2.0/+2.0	NON-PLATED	8		
16	40.0	+3.0/+3.0	NON-PLATED	13		
17	44.0	+2.0/+2.0	NON-PLATED	1		
18	52.0	+3.0/+3.0	NON-PLATED	1		
19	58.0	+3.0/+3.0	NON-PLATED	6		
20	60.0	+3.0/+3.0	NON-PLATED	1		
21	62.0	+2.0/+2.0	NON-PLATED	1		
22	66.0	+3.0/+3.0	NON-PLATED	2		
23	82.0	+2.0/+2.0	NON-PLATED	4		
24	108.0	+3.0/+3.0	NON-PLATED	1		
25	126.0	+3.0/+3.0	NON-PLATED	14		
26	250.0	+6.0/+4.0	NON-PLATED	4		
27	52.0624.0	+3.0/+3.0	PLATED	6		
28	56.0624.0	+3.0/+3.0	PLATED	2		
29	62.0624.0	+2.0/+2.0	PLATED	2		
30	76.0624.0	+2.0/+2.0	PLATED	4		
31	80.0624.0	+3.0/+3.0	PLATED	4		
32	82.0624.0	+2.0/+2.0	PLATED	2		
33	82.0624.0	+3.0/+3.0	PLATED	1		
34	90.0624.0	+2.0/+2.0	PLATED	4		
35	158.0678.0	+3.0/+3.0	NON-PLATED	1		


LAYER STACKUP				
LAYER NAME	FINISHED Cu		X-SECTION	DIELECTRIC THICKNESS [INCHES]
PRIMARY SIDE SILICSPHEN				
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L01 PRIMARY SIDE-1	1.31oz			0.0044
L02				0.004
L03 INNER-SIGNAL-1	1oz.			0.004
L04				0.004
L05 GROUPO-PLANE-2	1oz.			0.0042
L06 INNER-SIGNAL-2	1oz.			0.004
L07				0.004
L08 POWER-PLANE-1	1oz.			0.004
L09				0.004
L10 POWER-PLANE-3	1oz.			0.004
L11				0.004
L12 INNER-SIGNAL-3	1oz.			0.0042
L13				0.004
L14 GROUPO-PLANE-4	1oz.			0.0042
L15				0.004
L16 SECONDARY SIDE	1.31oz			0.0044
L17 GROUPO-PLANE-5				
SECONDARY SIDE SILICSPHEN				



REVISIONS		
REV #	DESCRIPTION	DATE
REV #	CCN #	DDMMYY



MEMBRANCE SPECIFICATIONS						
S/L#	TYPE	LAYER	WACMWIDTH (Mils)	SPACING (Mils)	IMPEDANCE (Ohms)	REF LAYER
1	EDGE COUPLED MICROSTRIP	L1/L2	5	6	120	L4/L13
2	EDGE COUPLED MICROSTRIP	L1/L2	5	5	100	L4/L13
3	EDGE COUPLED MICROSTRIP	L1/L2	5	5	100	L4/L13
4	EDGE COUPLED MICROSTRIP	L1/L2	7.4	5	85	L4/L13
5	EDGE COUPLED MICROSTRIP	L1/L2	5	5	100	L4/L13
6	EDGE COUPLED MICROSTRIP	L1/L2	5	5	100	L4/L13
7	EDGE COUPLED MICROSTRIP	L1/L2	5	5	100	L4/L13
8	EDGE COUPLED MICROSTRIP	L1/L2	5	5	100	L4/L13
9	EDGE COUPLED MICROSTRIP	L1/L2	5	5	100	L4/L13
10	EDGE COUPLED MICROSTRIP	L1/L2	3.8	5	90	L4/L13
11	EDGE COUPLED MICROSTRIP	L1/L2	4.3	5	90	L4/L13
12	EDGE COUPLED MICROSTRIP	L1/L2	4.3	5	85	L4/L13
13	STRIPLINE	L1/L2	5	5	100	L4/L13
14	STRIPLINE	L10/L12	3.8	5	50	L9/L11

SIGNATURES		DATE		 TEXAS INSTRUMENTS	PROC079
LAYOUT BY UAK		081221			
REVIEWED BY ZA		081221			
APPROVED BY AMB		081221			
J7X COMMON PROCESSOR BOARD					
		SIZE D		Rev A	
		SCALE: NONE		SHEET 1 OF 21	