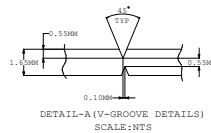


FABRICATION NOTES:

1. FABRICATE PCB IN ACCORDANCE WITH IPC-6012C, CLASS 2, PER IPC-6011.  
PCB SHALL BE MANUFACTURED USING 1-SPED OR EQUIVALENT.
2. MATERIALS:  
a. LAMINATE AND PREPREG (B-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/126.  
(MIN TO 180)  
b. COPPER FOIL TO BE IN ACCORDANCE WITH IPC-M-150, UNLESS OTHERWISE SPECIFIED.  
THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 6012B TABLE 30.3-7 AND 3-8.
3. ALL HOLES SHALL BE LOCATED WITHIN 0.15MM DIAMETER OF THEIR POSITION.  
LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.125MM.
4. BOM AND TEST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTHS.
5. CONDUCTOR WIDTHS SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCASE FOR MATCHING DIFFERENCE MISTRAL SHALL APPROVE THE MODIFIED WIDTHS AND SPACING.  
TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
6. AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
7. FINISH:  
a. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG.  
ELECTROLESS NICKEL/IMMERSION GOLD. ELECTROLESS NICKEL SHALL BE 1-4 MICRONS, TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.04-0.06 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.  
b. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-M-449, CLASS B, TO BOTH SIDES OF THE BOARD OVER BARE COPPER.  
c. VIA HOLE SHALL BE FILLED AND CAP PLATED AS PER TYPE VII REQUIREMENT.  
ONLY SOLDERMASK IMAGES THAT ARE 0.08(0.003") PER SIDE SHALL BE REDUCED IF REQUIRED.  
ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED. DEFAULT COLOUR OF SOLDER MASK BE BLUE.
8. SILESCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILESCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILESCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERABLE AREA.
9. SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 20UM [0.00079"]..
5. ALL HOLES SURROUNDED BY LAND <0.10" SHALL BE COMPLAINT TO IPC6012, CLASS 2.
8. MARKING:  
a. BOARD SHALL MEET THE REQUIREMENTS OF UL-756 WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, UL FILE NUMBER, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE REMEMBERED IN SILESCREEN.
9. TEST REQUIREMENTS:  
a. 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-354 NET LIST FOR OPENS AND SHORTS.
10. TRYING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
11. TRAP DROPS SHALL BE ADDED ON INTERNAL AND EXTERNAL LAYER FOR ALL THE VIA'S AND THROUGH HOLE PADS.
12. FINISHED PCB THICKNESS SHALL BE 0.655 +/-0.010.
13. MIN TACK/WEAR/SCALING ON BOARD IS 0.0015"/0.0012".
14. ALL THE IMPEDANCE SHALL BE MATCHED AS PER REQUIREMENT TABLE WITH +/-10% TOLERANCE.
15. ALL UNCONNECTED VIA'S SHALL BE SUPPRESSED IN INTERNAL LAYERS.
16. FOR DETAILED STACKUP REFER "P00112\_stackup.pdf"
17. ENSURE THAT UL REGISTERED 8-DIGIT NUMBER SHALL BE PRINTED ON PCB SILESCREEN.
18. BACKDRILLING TO BE DONE FROM 14-12.


DRILL CHART: NSIP to BOTTOM				
TEST NUMBER AND DEPTH				
TEST	DEPTH	TEST	DEPTH	TEST
	7.59	+3.0/+3.0	FLATED	23
	10.0	+3.0/+3.0	FLATED	24
	14.0	+3.0/+3.0	FLATED	25
	24.0	+3.0/+3.0	FLATED	26
	34.0	+3.0/+3.0	FLATED	27
	38.0	+3.0/+3.0	FLATED	28
	42.0	+3.0/+3.0	FLATED	29
	45.0	+3.0/+3.0	FLATED	30
	48.0	+2.0/+2.0	FLATED	31
	52.0	+2.0/+2.0	FLATED	32
	55.0	+2.0/+2.0	FLATED	33
	58.0	+2.0/+2.0	FLATED	34
	60.0	+3.0/+3.0	NON-FLATED	35
	62.0	+3.0/+3.0	NON-FLATED	36
	64.0	+3.0/+3.0	NON-FLATED	37
	66.0	+3.0/+3.0	NON-FLATED	38
	68.0	+3.0/+3.0	NON-FLATED	39
	70.0	+3.0/+3.0	NON-FLATED	40
	72.0	+3.0/+3.0	NON-FLATED	41
	74.0	+3.0/+3.0	NON-FLATED	42
	76.0	+3.0/+3.0	NON-FLATED	43
	78.0	+3.0/+3.0	NON-FLATED	44
	80.0	+3.0/+3.0	NON-FLATED	45
	82.0	+3.0/+3.0	NON-FLATED	46
	84.0	+3.0/+3.0	NON-FLATED	47
	86.0	+3.0/+3.0	NON-FLATED	48
	88.0	+3.0/+3.0	NON-FLATED	49
	90.0	+3.0/+3.0	NON-FLATED	50
	92.0	+3.0/+3.0	NON-FLATED	51
	94.0	+3.0/+3.0	NON-FLATED	52
	96.0	+3.0/+3.0	NON-FLATED	53
	98.0	+3.0/+3.0	NON-FLATED	54
	100.0	+3.0/+3.0	NON-FLATED	55
	102.0	+3.0/+3.0	NON-FLATED	56
	104.0	+3.0/+3.0	NON-FLATED	57
	106.0	+3.0/+3.0	NON-FLATED	58
	108.0	+3.0/+3.0	NON-FLATED	59
	110.0	+3.0/+3.0	NON-FLATED	60
	112.0	+3.0/+3.0	NON-FLATED	61
	114.0	+3.0/+3.0	NON-FLATED	62
	116.0	+3.0/+3.0	NON-FLATED	63
	118.0	+3.0/+3.0	NON-FLATED	64
	120.0	+3.0/+3.0	NON-FLATED	65
	122.0	+3.0/+3.0	NON-FLATED	66
	124.0	+3.0/+3.0	NON-FLATED	67
	126.0	+3.0/+3.0	NON-FLATED	68
	128.0	+3.0/+3.0	NON-FLATED	69
	130.0	+3.0/+3.0	NON-FLATED	70
	132.0	+3.0/+3.0	NON-FLATED	71
	134.0	+3.0/+3.0	NON-FLATED	72
	136.0	+3.0/+3.0	NON-FLATED	73
	138.0	+3.0/+3.0	NON-FLATED	74
	140.0	+3.0/+3.0	NON-FLATED	75
	142.0	+3.0/+3.0	NON-FLATED	76
	144.0	+3.0/+3.0	NON-FLATED	77
	146.0	+3.0/+3.0	NON-FLATED	78
	148.0	+3.0/+3.0	NON-FLATED	79
	150.0	+3.0/+3.0	NON-FLATED	80
	152.0	+3.0/+3.0	NON-FLATED	81
	154.0	+3.0/+3.0	NON-FLATED	82
	156.0	+3.0/+3.0	NON-FLATED	83
	158.0	+3.0/+3.0	NON-FLATED	84
	160.0	+3.0/+3.0	NON-FLATED	85
	162.0	+3.0/+3.0	NON-FLATED	86
	164.0	+3.0/+3.0	NON-FLATED	87
	166.0	+3.0/+3.0	NON-FLATED	88
	168.0	+3.0/+3.0	NON-FLATED	89
	170.0	+3.0/+3.0	NON-FLATED	90
	172.0	+3.0/+3.0	NON-FLATED	91
	174.0	+3.0/+3.0	NON-FLATED	92
	176.0	+3.0/+3.0	NON-FLATED	93
	178.0	+3.0/+3.0	NON-FLATED	94
	180.0	+3.0/+3.0	NON-FLATED	95
	182.0	+3.0/+3.0	NON-FLATED	96
	184.0	+3.0/+3.0	NON-FLATED	97
	186.0	+3.0/+3.0	NON-FLATED	98
	188.0	+3.0/+3.0	NON-FLATED	99
	190.0			



LAYER STACKUP				
LAYER NAME	FINISHED Cu	X-SECTION	DIELECTRIC THICKNESS	
			[INCHES]	
PRIMARY SIDE SILKSREEN				
PRIMARY SIDE SOLDERMASK				
L01	PRIMARY SIDE	1.450z		
L02	GROUND-PLANE-1	1oz		0.0037
L03	INNER-SIGNAL-1	0.5oz		0.0035
L04	GROUND-PLANE-2	1oz		0.0043
L05	INNER-SIGNAL-2	0.5oz		0.0035
L06	POWER-PLANE-1	1oz		0.0042
L07	POWER-PLANE-2	1oz		0.010
L08	INNER-SIGNAL-3	0.5oz		0.0043
L09	GROUND-PLANE-3	1oz		0.0035
L10	INNER-SIGNAL-4	0.5oz		0.0043
L11	GROUND-PLANE-4	1oz		0.0035
L12	SECONDARY SIDE	1.450z		0.0037
SECONDARY SIDE SOLDERMASK				
SECONDARY SIDE SILKSREEN				

### IMPEDANCE SPECIFICATIONS

S#	TYPE	LAYER	TRACEWIDTH(Mils)	SPACING (Mils)	IMPEDANCE (Ohms)	REF LAYER
01	EDGE COUPLED MICROSTRIP	L1/L12	4.18	6.32	100	L2/L11
02	EDGE COUPLED MICROSTRIP	L1/L12	5.10	5.4	90	L2/L11
03	EDGE COUPLED MICROSTRIP	L1/L12	6.0	5.5	85	L2/L11
04	EDGE COUPLED MICROSTRIP	L1	6.56	4.94	80	L2/L1
05	EDGE COUPLED MICROSTRIP	L1/L12	7.2	8.3	120	L3/L10
06	MICROSTRIP	L1	9.9	-	38	L2
07	MICROSTRIP	L1/L12	10.4	-	40	L2/L11
08	MICROSTRIP	L1/L12	6.5	-	50	L2/L11
09	EDGE COUPLED STRIPLINE	L3, L8,L10	4.07	7.93	100	L2/L4,L7/L9, L9/L11
10	EDGE COUPLED STRIPLINE	L8,L10	4.82	6.18	90	L2/L4,L7/L9, L9/L11
11	EDGE COUPLED STRIPLINE	L8,L10	5.35	6.15	85	L7/L9,L9/L11
12	EDGE COUPLED STRIPLINE	L3,L5	5.93	6.07	80	L2/L4,L4/L6
13	EDGE COUPLED STRIPLINE	L10	6.4	5.6	76	L9/L11
14	STRIPLINE	L3,L5, L8,L10	4	-	50	L2/L4,L4/L6, L7/L9,L9/L11
15	STRIPLINE	L6	5.0	-	50	L3/L7
16	STRIPLINE	L10	6.8	-	38	L9/L11
17	STRIPLINE	L3,L5, L8,L10	6.25	-	40	L2/L4,L4/L6, L7/L9,L9/L11
18						

SIGNATURES		DATE		 TEXAS INSTRUMENTS	PROC112
LAYOUT BY	VCR	251021			
REVIEWED BY	ZA	251021			
APPROVED BY	AMB	251021			
TDA4VM EDGE AI KIT				SIZE	
				D	
SCALE: NONE				19	
				SHEET	1 OF 19