

# J784S4 EVM PDN-3A

## System Power Sequences

**EVM unit under test = PROC141E5**

(NOTE: This report is applicable to other TDA4x PDN-3x & -8x systems using TPS6594133A-Q1 PMIC that will have very similar power sequencing performance.)

**v1.0      3/31/2025**

# Agenda

- Initial Power Up Overview
- Initial Power Up Sequence
- Controlled Power Up Sequence
- Controlled Power Down Sequence
- Input Power Loss
- Reference Section
- EVM Items

# J784S4 EVM | Initial Power Up Overview

- Initial Power Up Definition

- EVM starts from an OFF power state with all components in an unenergized state. After supplying the EVM with a valid VINPUT voltage, the 1<sup>st</sup> stage pre-regulator will ramp up the VSYS\_3V3 power rail followed by PMIC\_ENABLE asserting high.

1st Stage Pre-Regulator Power Up Summary		
Supply Rail / Net	Ramp Start <sup>1</sup> [ms]	Full Voltage <sup>1</sup> [ms]
VINPUT	0	~0.8
VSYS_3V3	~0.8	3.93 <sup>2</sup>
LM5143_PG1	3.53	3.53
PMIC_ENABLE	23	23.2

Note: 1) Elapsed time is measured referenced to VINPUT crossing 0.1V during ramp-up.

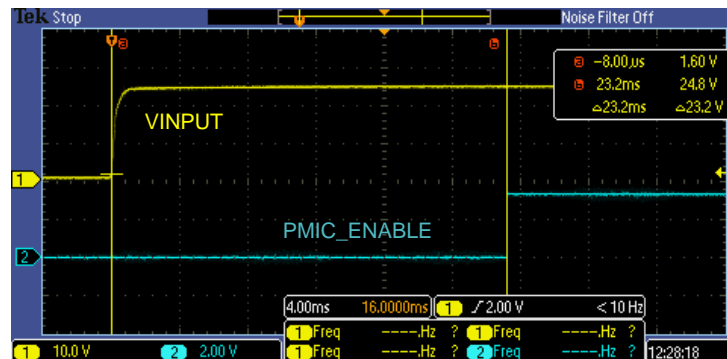
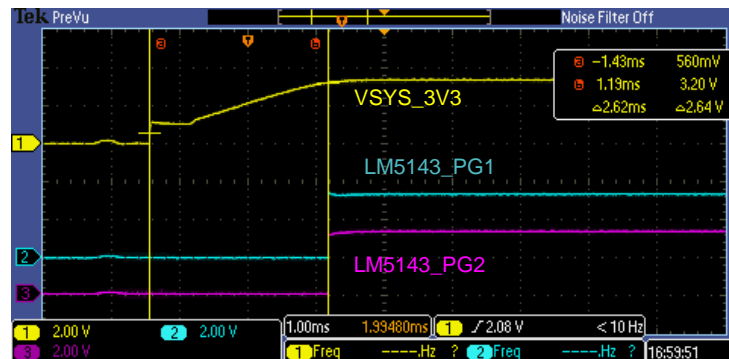
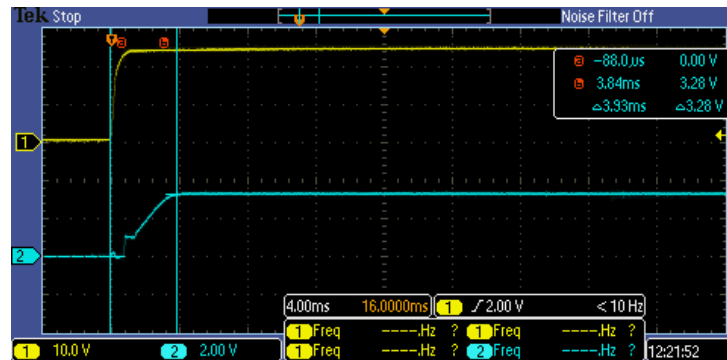
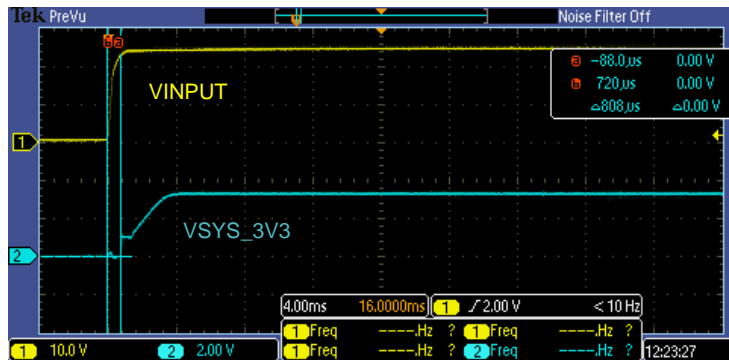
2) VINPUT to VSYS\_3V3 crossing 2.0V level = ~2.1ms

2nd Stage SoC PDN Power Up Summary	
Key PMIC Inputs & Outputs	Full Voltage <sup>1</sup> [ms]
VSYS_SENSE (= VSYS_3V3 from 1st Stage ramped to 2.0V)	0
OVPDRV (= PMIC, Over Voltage Protection Gate Drive signal starts protection FET turning-on)	2.16
VCCA (= Protected 3.3V low voltage supply for PMIC & discrete power resources, fully ramped up)	2.8
VRTC (= PMIC, internal real time clock 1.8V supply)	3.8
VINT (= PMIC, internal digital 1.8V logic supply)	4.24
PMIC_ENABLE (= SYS_MCU_EN from SYS_MCU_PG = VINPUT_VMON & LM5143_PG1/ PG2 & "VSYS_3V3 Time Delay")	20.9 <sup>2</sup>
EN_3V3_VIO (= PMIC, GPIO-09, 1st pwr-up seq signal asserted)	26.8 <sup>2</sup>
nRSTOUT (= PMIC, OD-output pulled to 1.8V, pwr-up seq is completed by releasing signal to go high)	39.8 <sup>2</sup>

Note: 1) Elapsed time is measured referenced to VSYS\_3V3 crossing 2.0V during ramp-up.

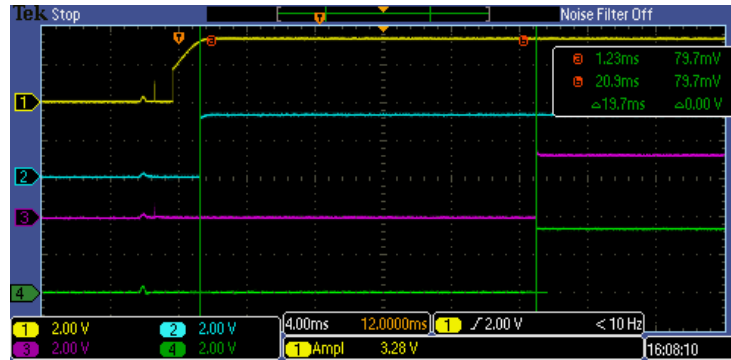
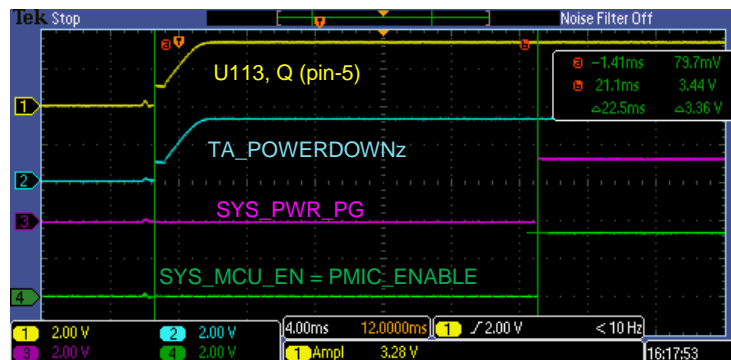
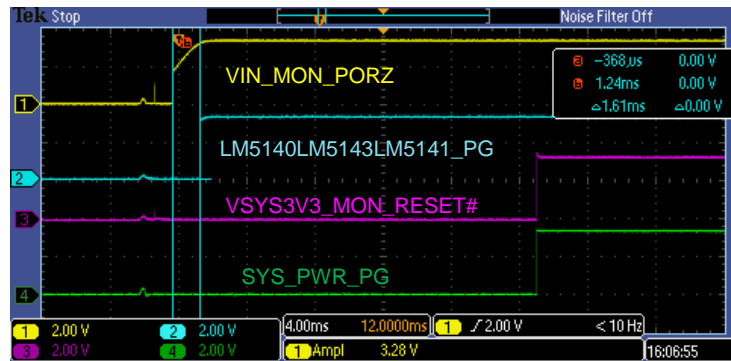
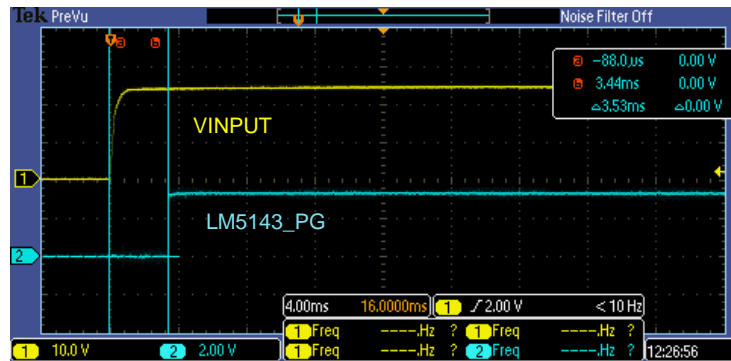
2) See ["EVM Item #1 PMIC\\_ENABLE Delay"](#) in Reference section for details on EVM's 19.7ms time delay

# J784S4 EVM | 1<sup>st</sup> Stage Pre-Regulator

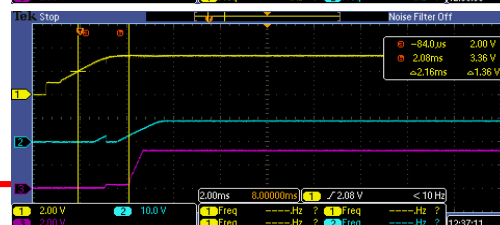
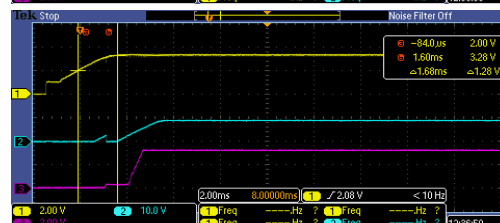
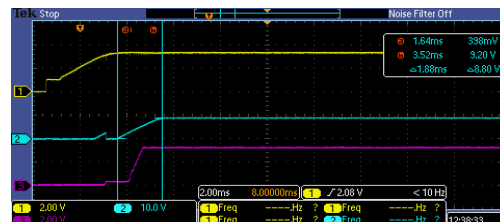
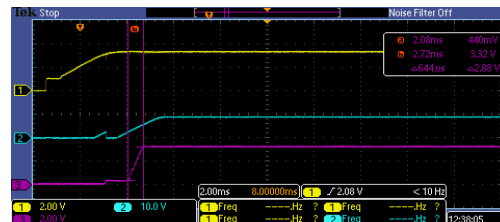
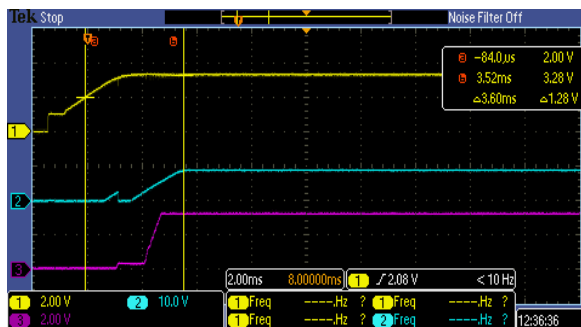
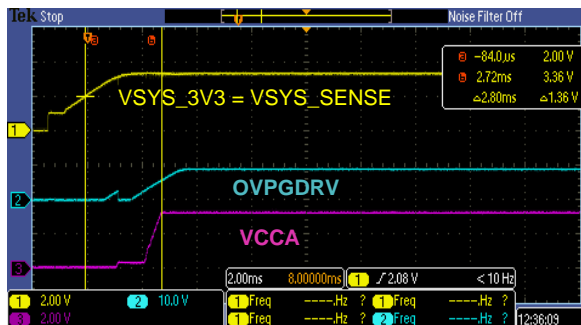
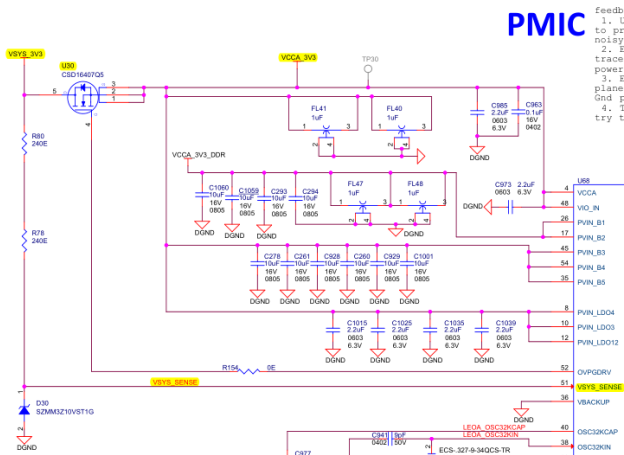


See “EVM Item #1 PMIC ENABLE Delay”

# J784S4 EVM | 1<sup>st</sup> Stage Pre-Regulator



- **PMIC Over-Voltage Protection FET**
  - PMIC's VSYS\_SENSE and OVPGDRV pins protect the device from being damaged by an overvoltage event from the pre-regulator by disconnecting the PMIC's low voltage VCCA-powered pins from VSYS\_3V3.

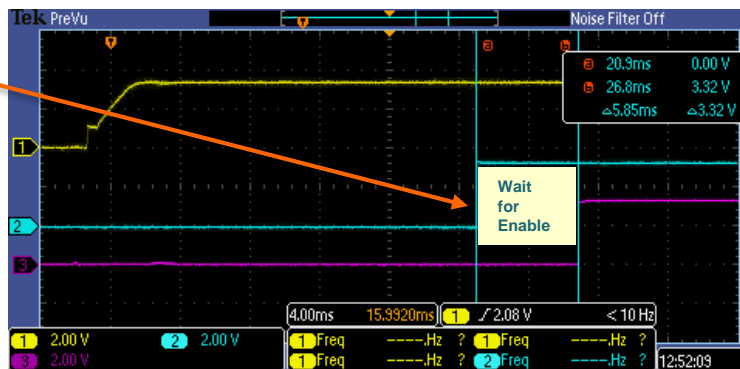
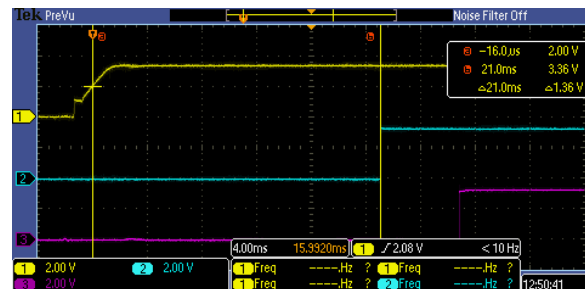
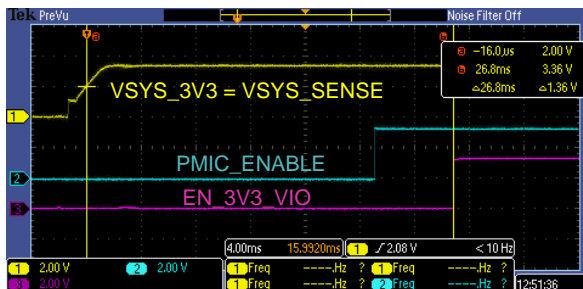




# J784S4 EVM | 2<sup>nd</sup> Stage SoC PDN

## • PMIC Internal Power Up Seq Start

- Each time PMIC is powered up, it executes a “Wait for Enable” state (~5.5ms) immediately after PMIC\_ENABLE is asserted high & before running the power up seq (EN\_3V3\_VIO is 1st signal asserted high during power up seq).
- During most of the “Wait for Enable” time period, the PMIC is auto-detecting the VCCA input supply voltage level (3.3 or 5V) and setting power resource parameters per Vin voltage.
- Two PMIC GPIOs are also latched during “Wait for Enable” state & used as “resource selection” bits as follows:
  - GPIO 8
    - Low => Creates 2x power groups (MCU & Main/SoC) for Isolated PDNs (PDN-3A thru -3F)
    - High => Creates 1x MCU power group for Grouped PDNs (PDN-3G to -3M)
  - GPIO 9
    - Low = Keeps default setting that enables PMIC's watchdog timer
    - High = Disables PMIC's watchdog timer

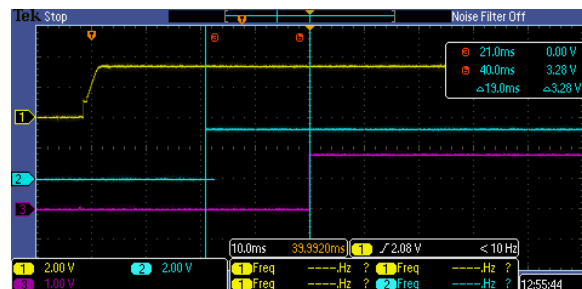
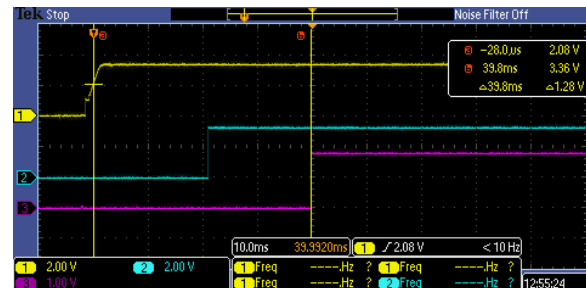
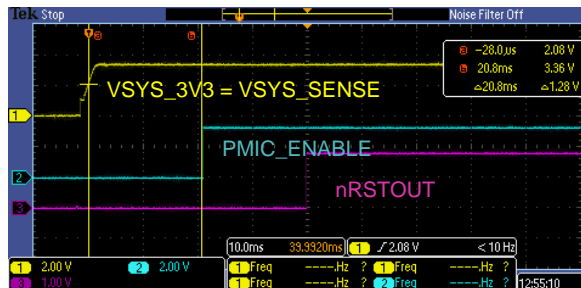




# J784S4 EVM | 2<sup>nd</sup> Stage SoC PDN

- **PMIC Initial Power Up Seq Completion**

- PMIC's nRSTOUT pin = SoC's "MCU\_PORz" input signal asserts high at the end of the SoC's power up seq.



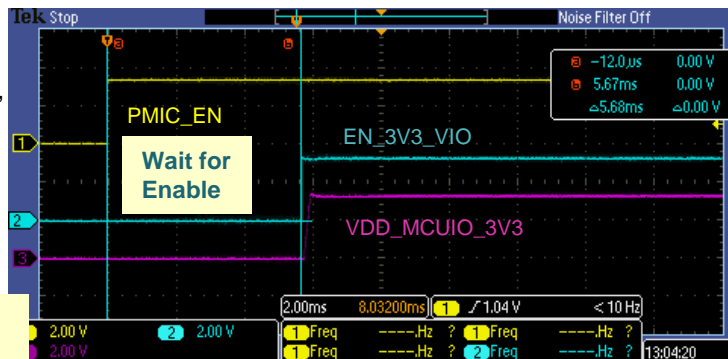
# Initial Power Up | Sequence Breakdown

Resource	Seq Control (PMIC resource settings)	Supply Rail / Net	Expected		Measured		Remarks
			Ramp-Up Start (ms)	Max Ramp-Up (ms)	Ramp-Up Start (ms)	Full Ramp-Up (ms)	
PMIC's Input Enable	Derived from 1 <sup>st</sup> stage PG & Test Automation logic	PMIC ENABLE	-5.6	-5.6	-5.7	-5.7	Wait for Enable state (~5.5ms)
PMIC's GPIO9	(PP, Low -> High, 0us by state machine)	EN_3V3_VIO	0	0	0	0	Time reference to PMIC's 1 <sup>st</sup> pwr up seq state
PMIC	(LDO_2, 0.165A for FET Bypass, 0us)	VDD_MCUIO_3V3	0	0.5	0.1	0.2	See <a href="#">Pwr Seq Timing Diag v0.31</a>
Dscrt Load Switch: TPS22965-Q1	VDD_MCUIO_3V3 # EN_GPIO_RET	VDD_GPIORET_IO_3V3	0.1	1.35	0.12	1.32	
Dscrt Load Switch: TPS22965-Q1	EN_3V3_VIO	VDD_IO_3V3	0.1	1.35	0.36	1.12	
Dscrt LDO: TLV73333P-Q1	EN_3V3_VIO	VDA_USB_3V3	0.1	1.6	1.04	2.24	See <a href="#">EVM Item #2 5V Ramp Delay</a>
Dscrt LDO: TLV7103318-Q1	Control = EN_3V3_VIO	VDD_SD_DV	0.1	0.2	1.44	2.28	See <a href="#">EVM Item #2 5V Ramp Delay</a>
PMIC	(LDO_1, 0.5A, 1.8V, 2000us, 3.6-7.2 V/ms)	VDD_MCUIO_1V8	2	2.1	2.08	2.20	
PMIC	(LDO_4, 0.3A, 1.8V, 2000us, 3.6-7.2 V/ms)	VDA_MCU_1V8	2	2.1	2.16	2.32	
PMIC	(Buck_4, 4.0A, 1.8V, 2000us, 3.6-7.2 V/ms)	VDD_IO_1V8	2.1	2.5	2.20	2.46	
Dscrt LDO: TPS745xxP-Q1	VDD_IO_1V8	VDA_PLL_1V8	2.1	2.8	2.48	2.88	
Dscrt LDO: TPS745xxP-Q1	VDD_IO_1V8	VDA_PHY_1V8	2.1	2.75	2.48	2.88	
Dscrt LDO: TPS745xxP-Q1	VDD_IO_1V8 # EN_DDR_RET_1V1	VDD1_DDR_1V8	2.1	2.75	2.52	2.8	
PMIC	(Buck_5, 2.0A, 0.85V, 3000us, 1.7- 3.4 V/ms)	VDD_MCU_0V85	3.1	3.5	3.24	3.48	
Dscrt LDO: TPS745xxP-Q1	VDD_MCU_0V85 # EN_GPIO_RET	VDD_GPIORET_WK_0V8	3.1	3.75	3.52	3.76	
PMIC	(LDO_3, 0.5A, 0.8V, 3500us, 1.6- 3.2 V/ms)	VDA_DLL_0V8	3.5	3.6	3.64	3.64	
Dscrt 3-Ph Buck: TPS62873Y1-Q0	VDA_DLL_0V8	VDD_CPU_AVS	3.6	4.6	3.68	4.74	
Dscrt 2-Ph Buck: TPS62873Y1-Q1	VDA_DLL_0V8	VDD_CORE_0V8	3.6	4.6	3.76	4.73	
PMIC	(Buck_3, 3.5A, 0.85V, 8500us, 1.7- 3.4 V/ms)	VDD_RAM_0V85	8.6	9.0	8.72	9.04	
PMIC	(Buck_1+2, 7A, 1.1V, 8500us, 1.7- 3.4 V/ms)	VDD_DDR_1V1	8.6	9.0	8.72	9.05	
PMIC's OD "nRSTOUT"	(OD, Low -> High, 12,200us by state machine)	H_MCU_PORZ	13	13.1	12.92	13.24	
PMIC's GPIO11	(OD, Low -> High, 12,200us by state machine)	H_SOC_PORZ	13	13.1	13.32	13.2	

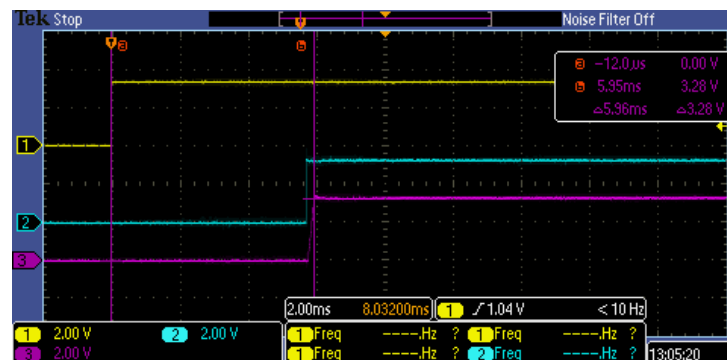
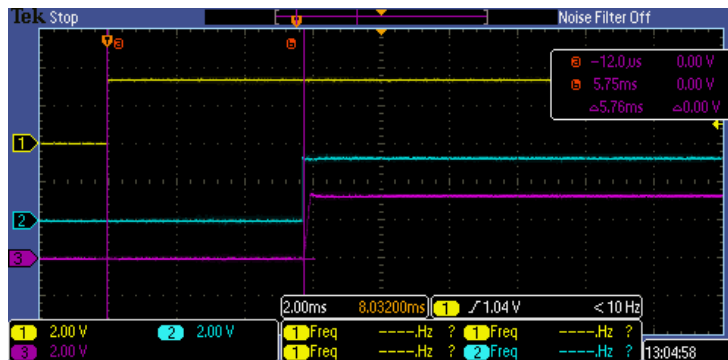
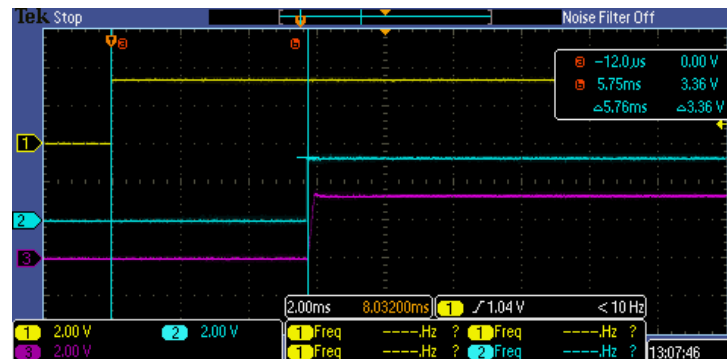
# Initial Pwr Up Seq | T0 Time Step

## Initial Power Up Seq Delayed

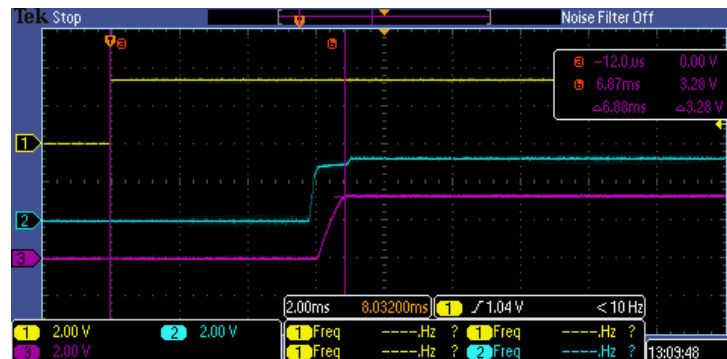
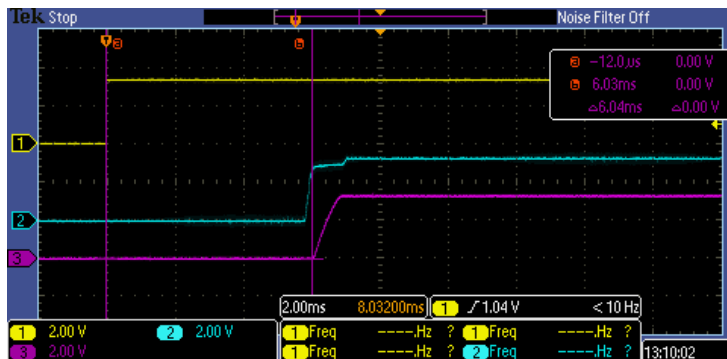
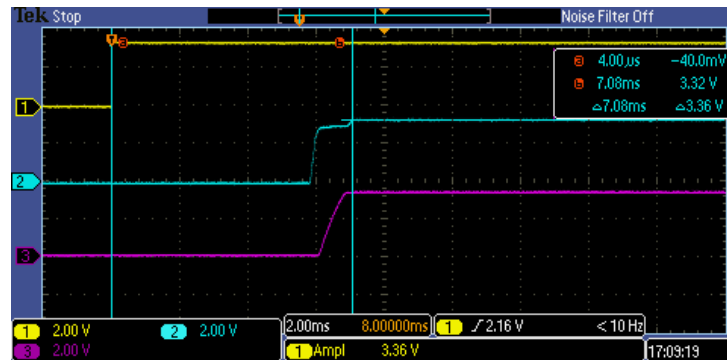
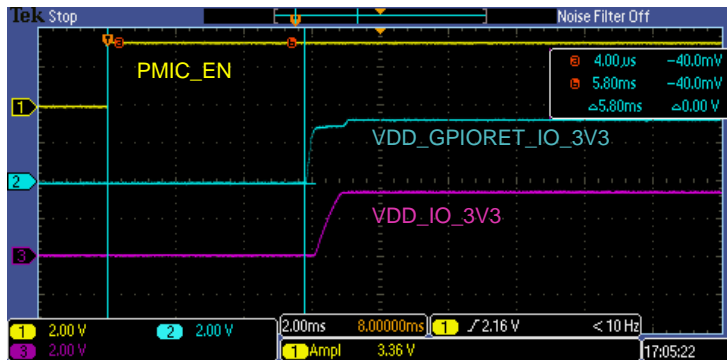
- All time steps will be delayed ~5.5ms from nominal time steps due to "Wait for Enable"



See  
["Wait for Enable" description](#)

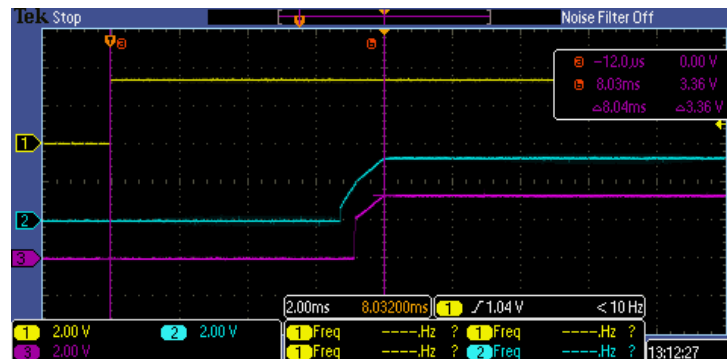
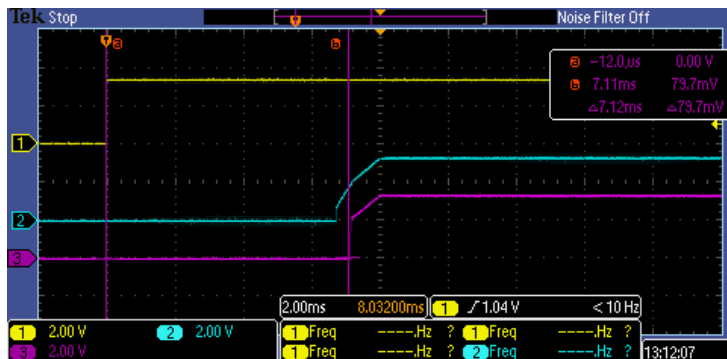
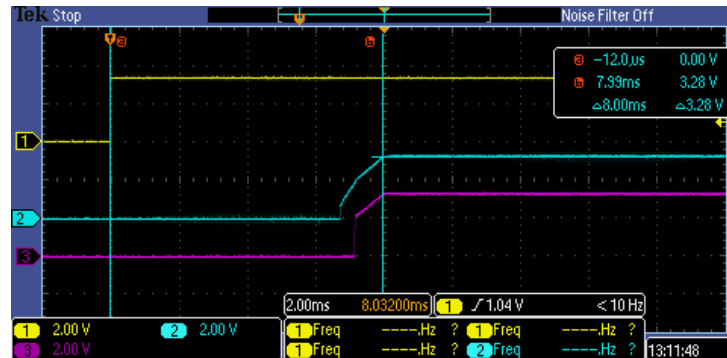
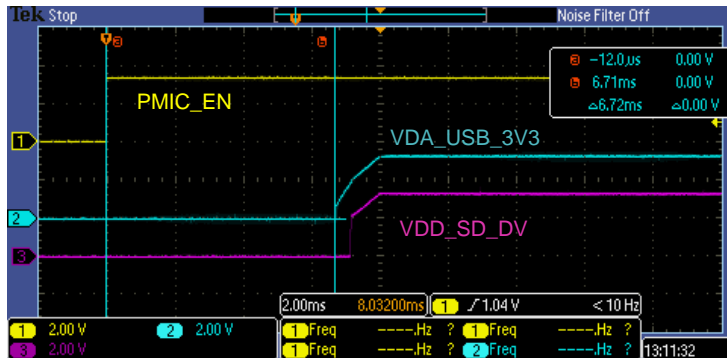


# Initial Pwr Up Seq | T0 Time Step

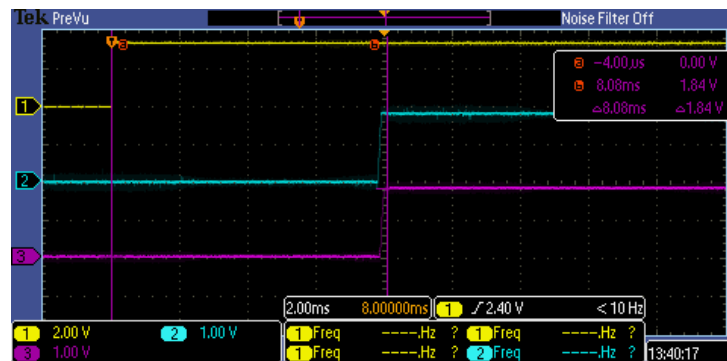
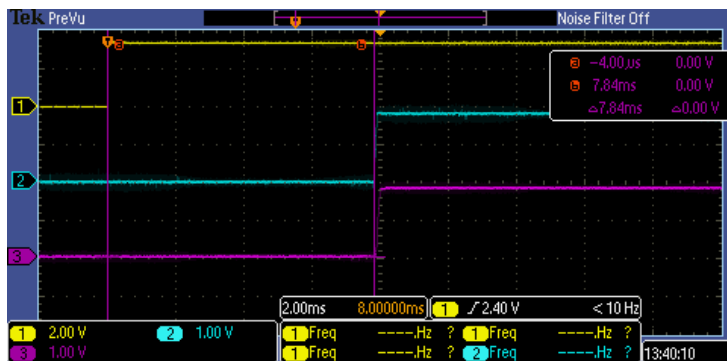
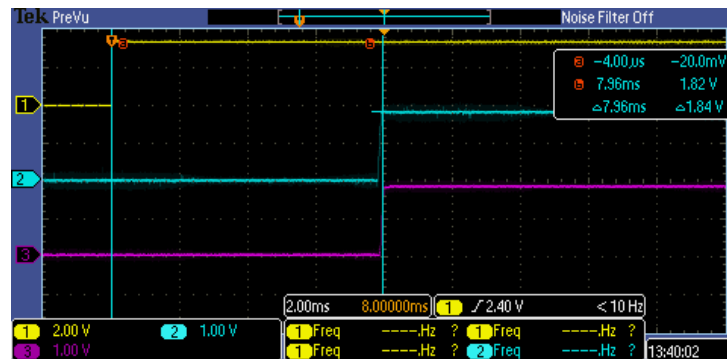
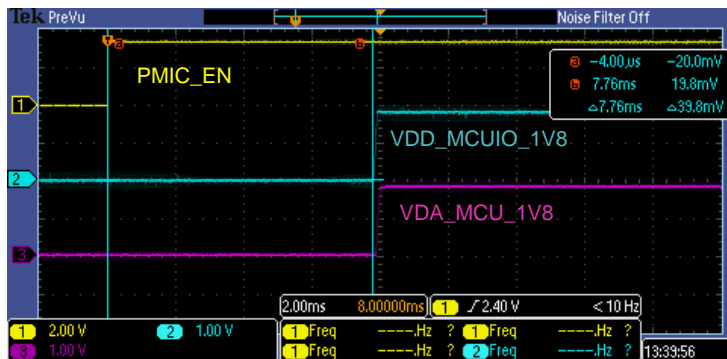


# Initial Pwr Up Seq | T0 Time Step

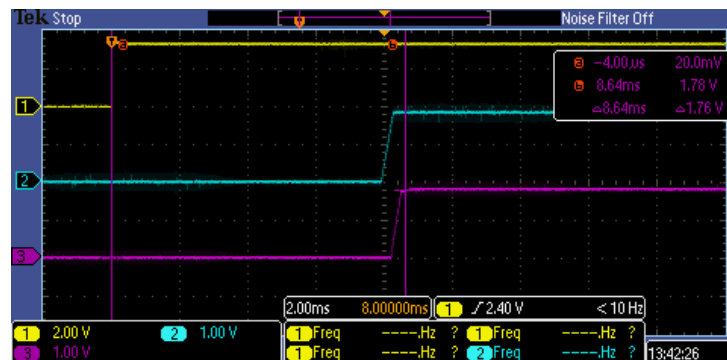
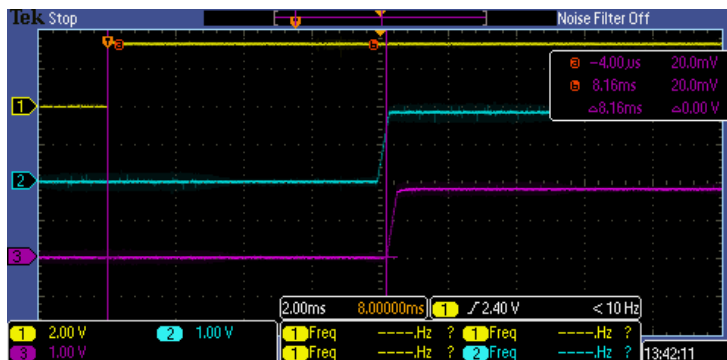
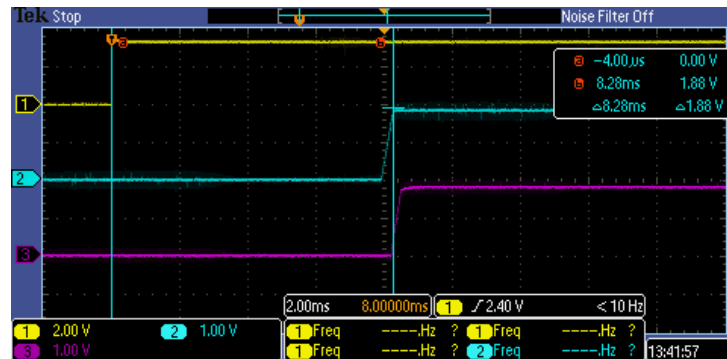
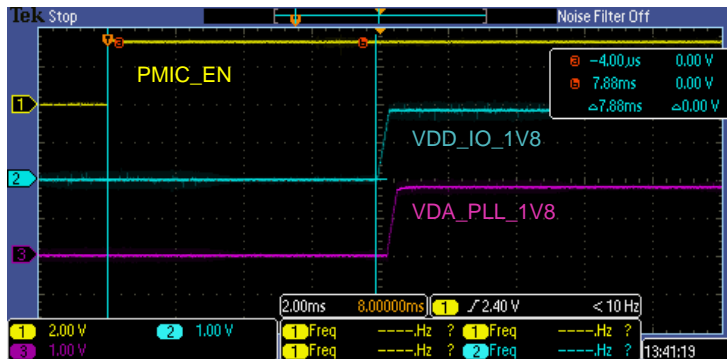
See “[EVM Item #2 5V Ramp Delay](#)”



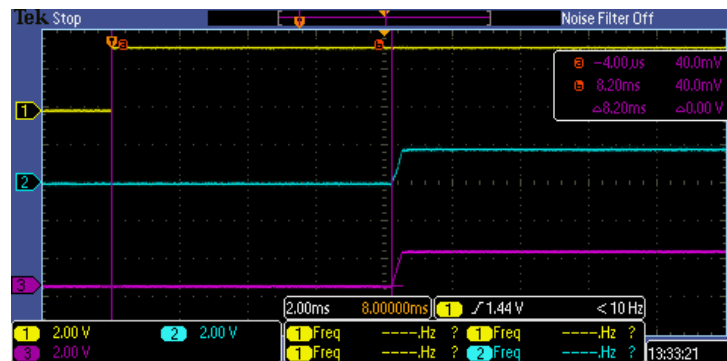
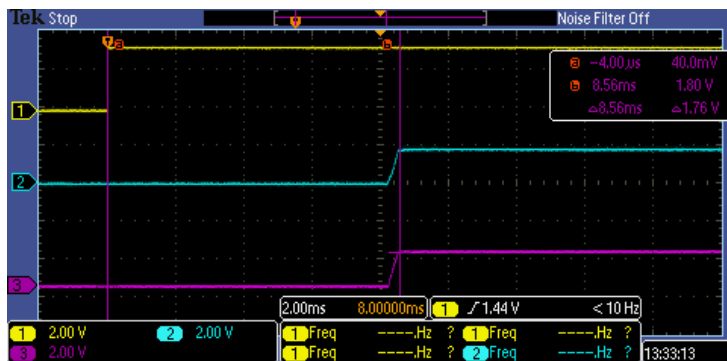
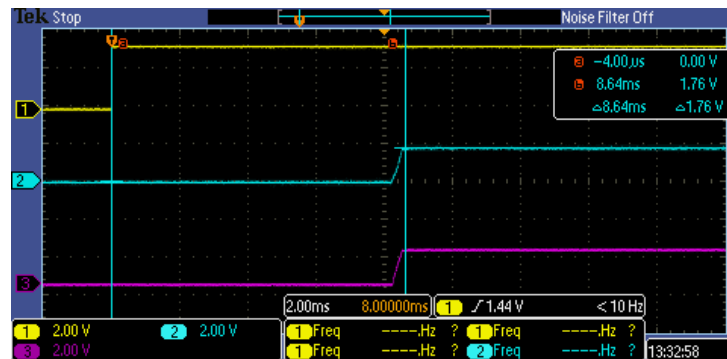
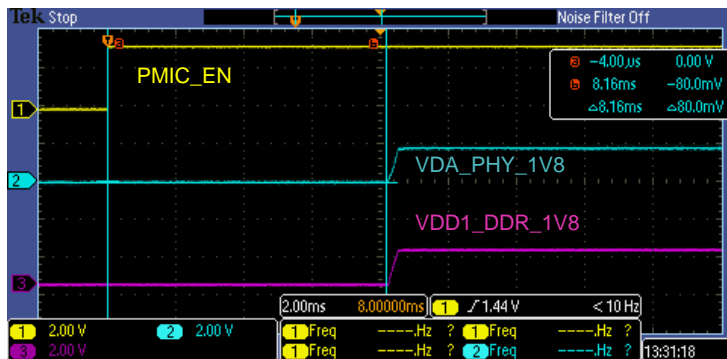
# Initial Pwr Up Seq | T1 Time Step



# Initial Pwr Up Seq | T1 Time Step

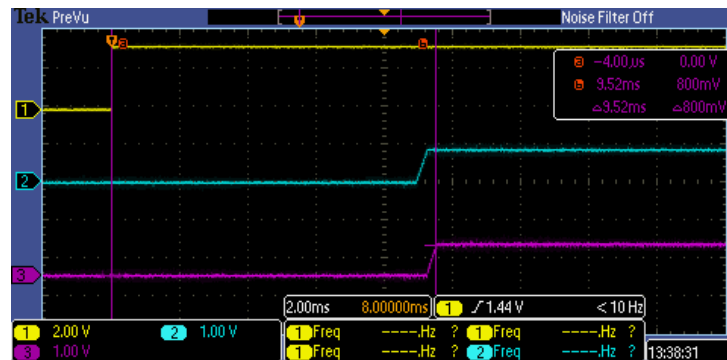
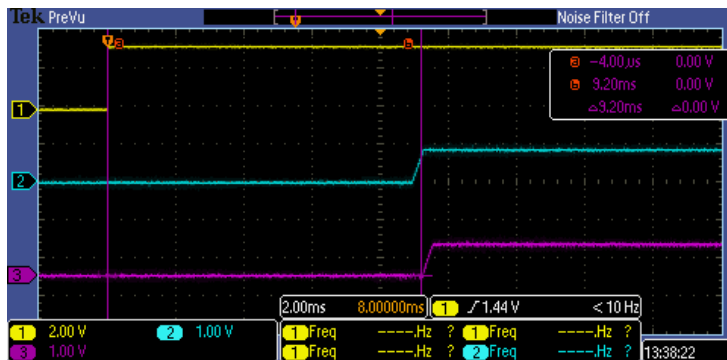
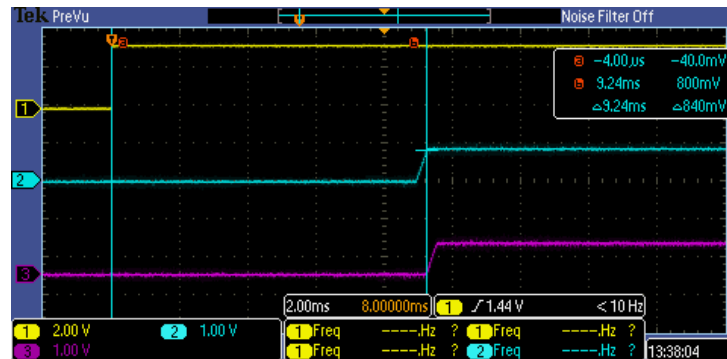
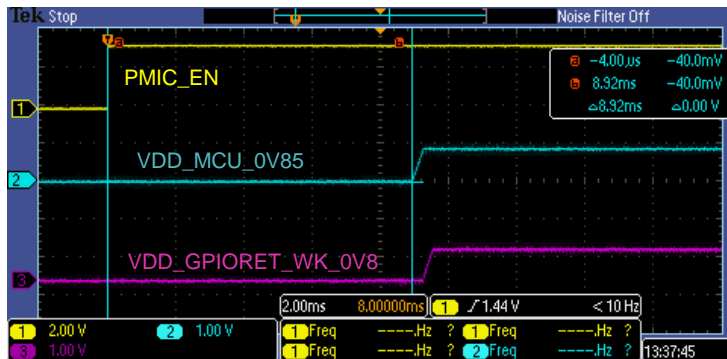


# Initial Pwr Up Seq | T1 Time Step

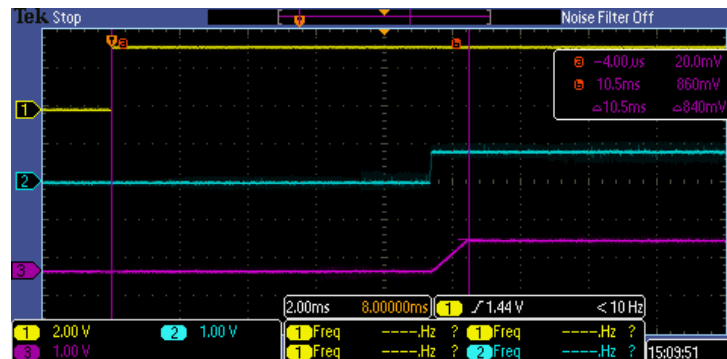
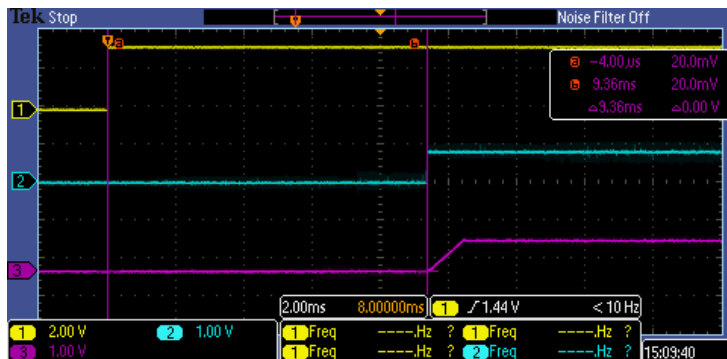
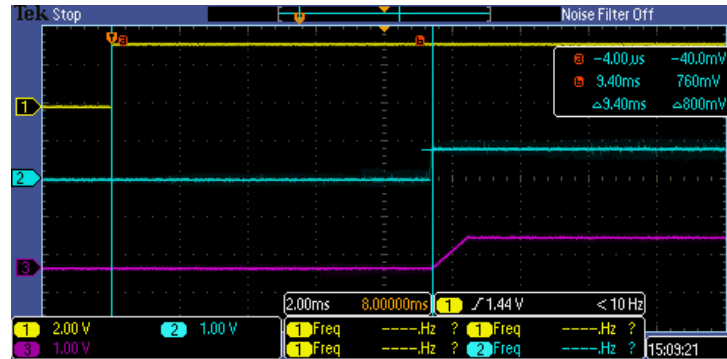
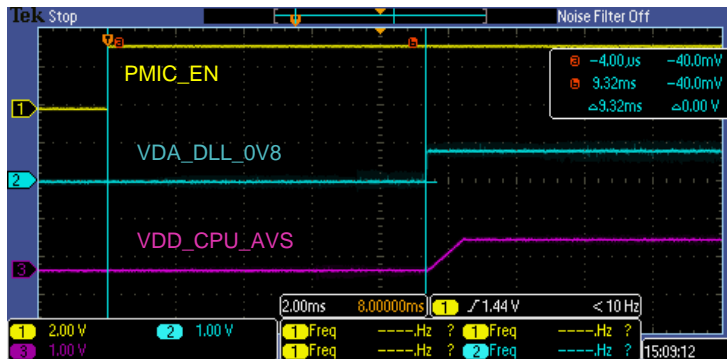




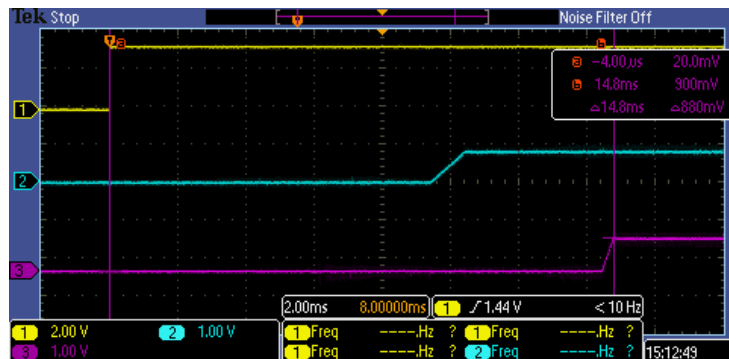
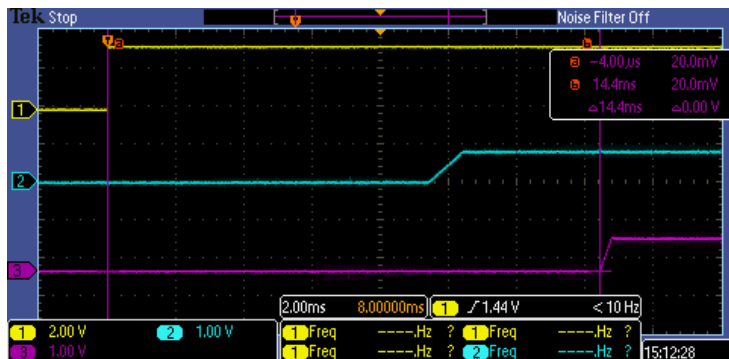
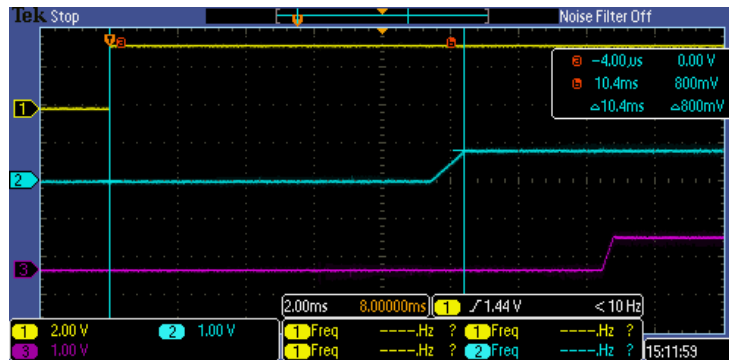
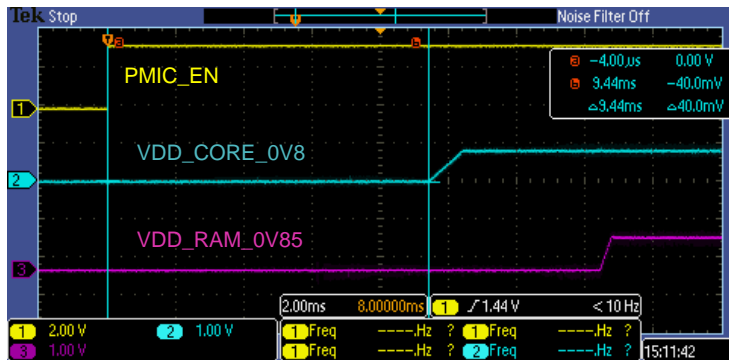
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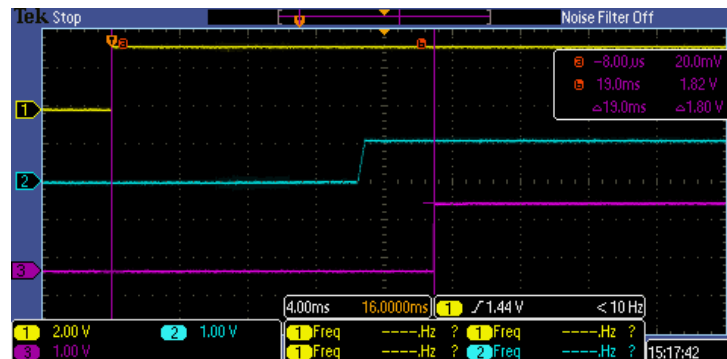
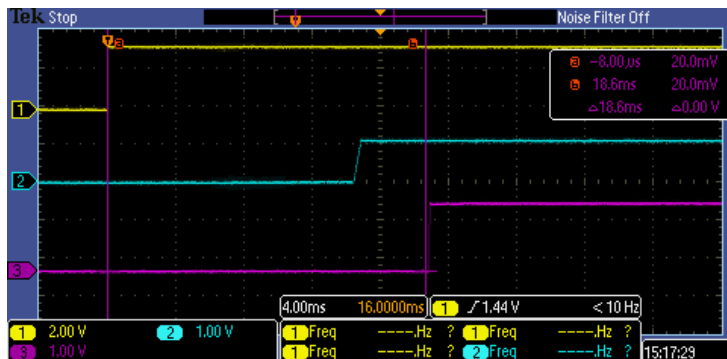
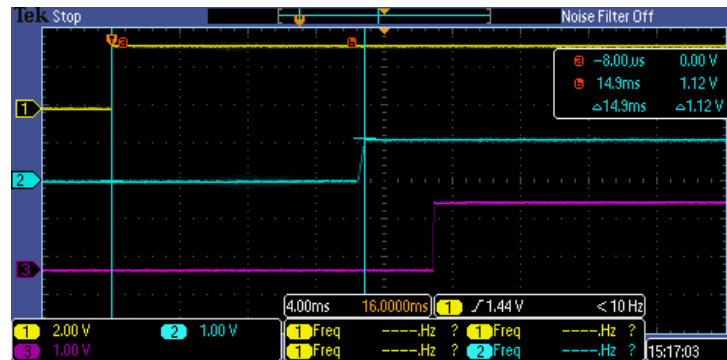
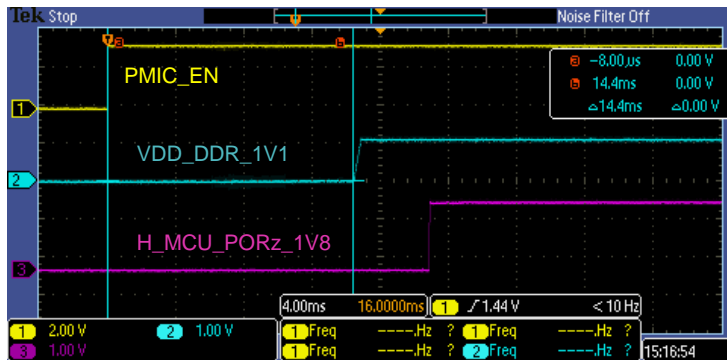
# Initial Pwr Up Seq | T2 Time Step



# Initial Pwr Up Seq | T2 Time Step



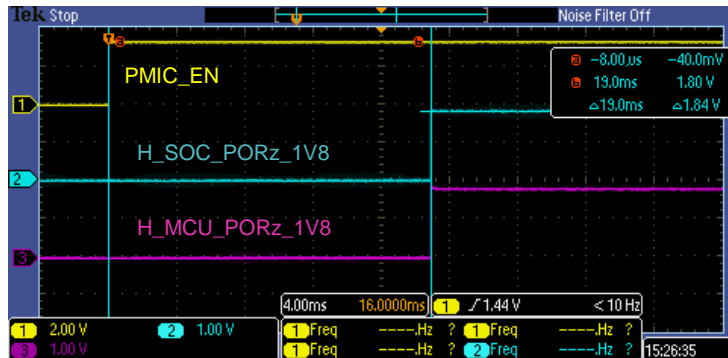
# Initial Pwr Up Seq | T3 Time Step



# Initial Pwr Up Seq | T4 Time Step

- **PMIC Initial Power Up Seq Completion**

- PMIC's nRSTOUT pin = SoC's "MCU\_PORz" input signal asserts high at the end of the SoC's power up seq.



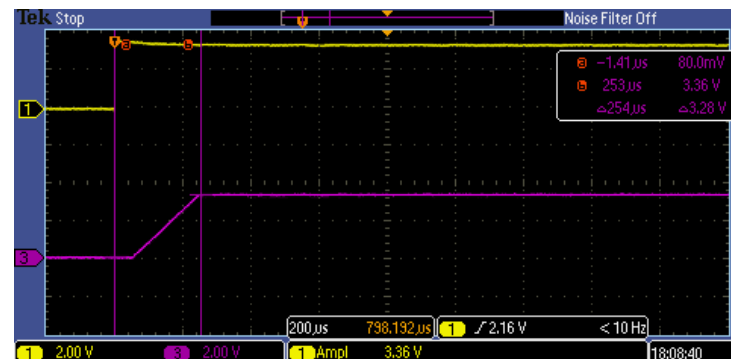
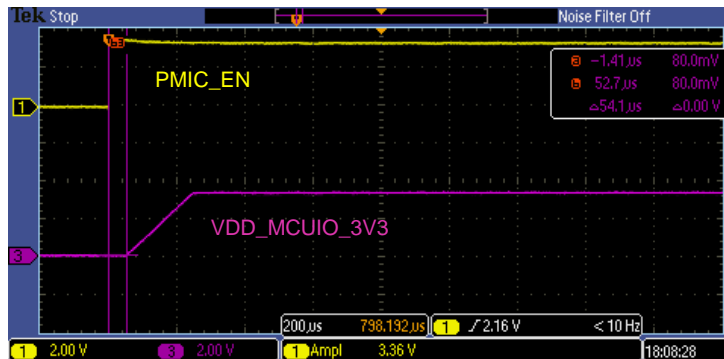
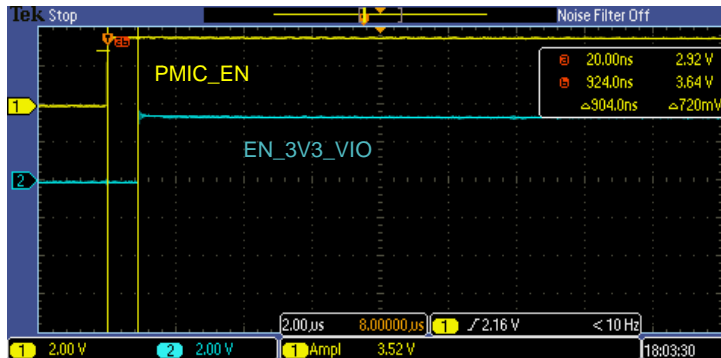
# Controlled Power Up | Sequence Breakdown

Resource	Seq Control (PMIC resource settings)	Supply Rail / Net	Expected		Measured		Remarks
			Ramp-Up Start (ms)	Max Ramp-Up (ms)	Ramp-Up Start (ms)	Full Ramp-Up (ms)	
PMIC's Input Enable	Derived from 1 <sup>st</sup> stage PG & Test Automation logic	PMIC ENABLE	-0.1	-0.1	-0.1	-0.1	No "Wait for Enable" delay, no power cycle of PMIC
PMIC's GPIO9	(PP, Low -> High, 0us by state machine)	EN_3V3_VIO	0	0	0	0	Time reference to PMIC's 1 <sup>st</sup> pwr up seq state
PMIC	(LDO_2, 0.165A for FET Bypass, 0us)	VDD_MCUIO_3V3	0	0.5	0.05	0.25	See <a href="#">Pwr Seq Timing Diag v0.31</a>
Dscrt Load Switch: TPS22965-Q1	VDD_MCUIO_3V3 # EN_GPIO_RET	VDD_GPIORET_IO_3V3	0.1	1.35	0.11	1.37	
Dscrt Load Switch: TPS22965-Q1	EN_3V3_VIO	VDD_IO_3V3	0.1	1.35	0.35	1.21	
Dscrt LDO: TLV73333P-Q1	EN_3V3_VIO	VDA_USB_3V3	0.1	1.6	1.01	2.31	See <a href="#">EVM Item #2 5V Ramp Delay</a>
Dscrt LDO: TLV7103318-Q1	EN_3V3_VIO	VDD_SD_DV	0.1	0.2	1.43	2.29	See <a href="#">EVM Item #2 5V Ramp Delay</a>
PMIC	(LDO_1, 0.5A, 1.8V, 2000us, 3.6-7.2 V/ms)	VDD_MCUIO_1V8	2.0	2.1	2.05	2.23	
PMIC	(LDO_4, 0.3A, 1.8V, 2000us, 3.6-7.2 V/ms)	VDA_MCU_1V8	2.0	2.1	2.15	2.31	
PMIC	(Buck_4, 4.0A, 1.8V, 2000us, 3.6-7.2 V/ms)	VDD_IO_1V8	2.1	2.5	2.19	2.57	
Dscrt LDO: TPS745xxP-Q1	VDD_IO_1V8	VDA_PLL_1V8	2.1	2.8	2.49	2.81	
Dscrt LDO: TPS745xxP-Q1	VDD_IO_1V8	VDA_PHY_1V8	2.1	2.75	2.47	2.83	
Dscrt LDO: TPS745xxP-Q1	VDD_IO_1V8 # EN_DDR_RET_1V1	VDD1_DDR_1V8	2.1	2.75	2.51	2.85	
PMIC	(Buck_5, 2.0A, 0.85V, 3000us, 1.7- 3.4 V/ms)	VDD_MCU_0V85	3.1	3.5	3.19	3.57	
Dscrt LDO: TPS745xxP-Q1	VDD_MCU_0V85 # EN_GPIO_RET	VDD_GPIORET_WK_0V8	3.1	3.75	3.51	3.83	
PMIC	(LDO_3, 0.5A, 0.8V, 3500us, 1.6- 3.2 V/ms)	VDA_DLL_0V8	3.5	3.6	3.61	3.69	
Dscrt 3-Ph Buck: TPS62873Y1-Q0	VDA_DLL_0V8	VDD_CPU_AVS	3.6	4.6	3.69	4.73	
Dscrt 2-Ph Buck: TPS62873Y1-Q1	VDA_DLL_0V8	VDD_CORE_0V8	3.6	4.6	3.7	4.78	
PMIC	(Buck_3, 3.5A, 0.85V, 8500us, 1.7- 3.4 V/ms)	VDD_RAM_0V85	8.6	9.0	8.7	9.1	
PMIC	(Buck_1+2, 7A, 1.1V, 8500us, 1.7- 3.4 V/ms)	VDD_DDR_1V1	8.6	9.0	8.74	9.22	
PMIC's OD "nRSTOUT"	(OD, Low -> High, 12,200us by state machine)	H_MCU_PORZ	13	13.1	13.2	13.2	
PMIC's GPIO11	(OD, Low -> High, 12,200us by state machine)	H_SOC_PORZ	13	13.1	13.2	13.2	

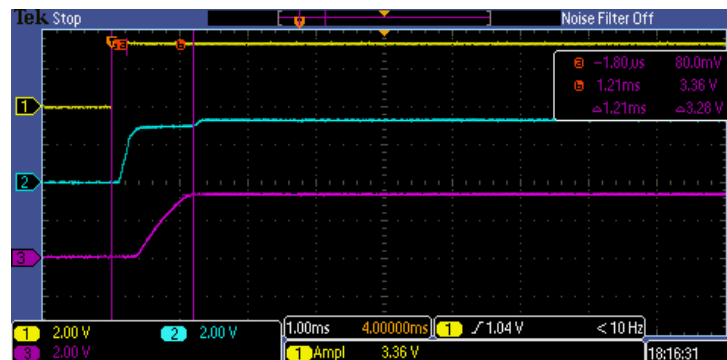
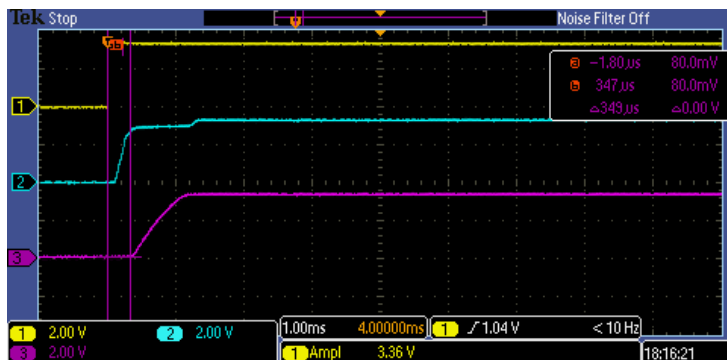
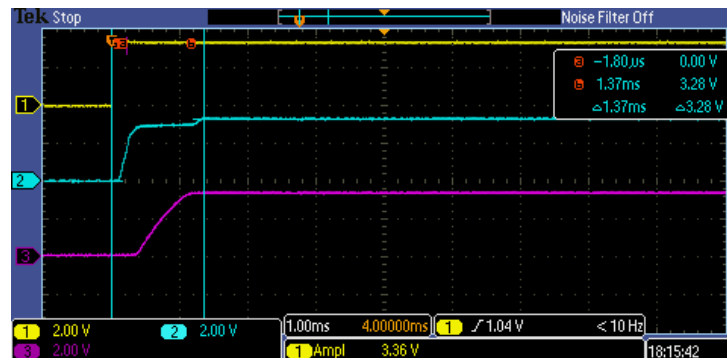
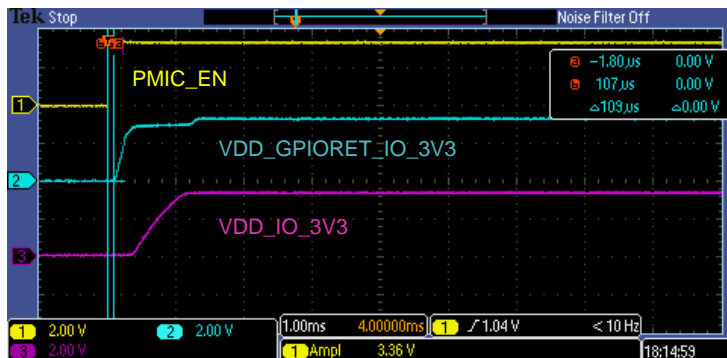
# Controlled Power Up | T0 Time Step

- Controlled Power Up Definition

- EVM & PMIC have already completed an initial power up seq and have remained energized while PMIC\_EN was set low to disable the SoC.
- After asserting PMIC\_ENABLE high, PMIC will immediately begin an SoC power up sequence.



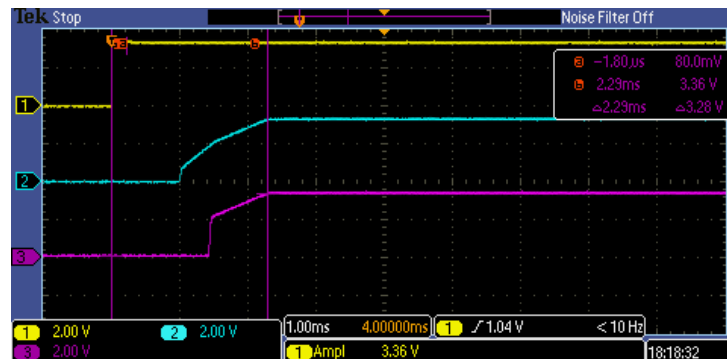
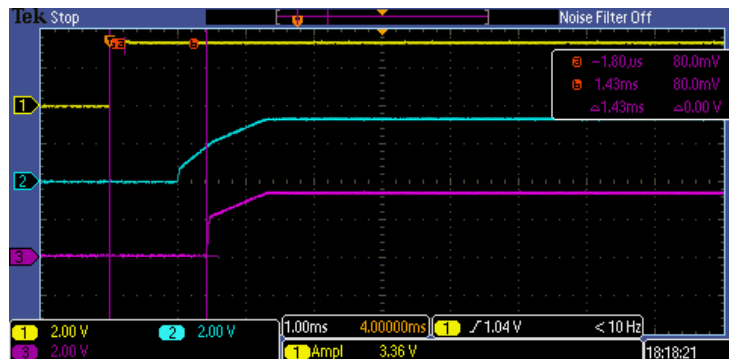
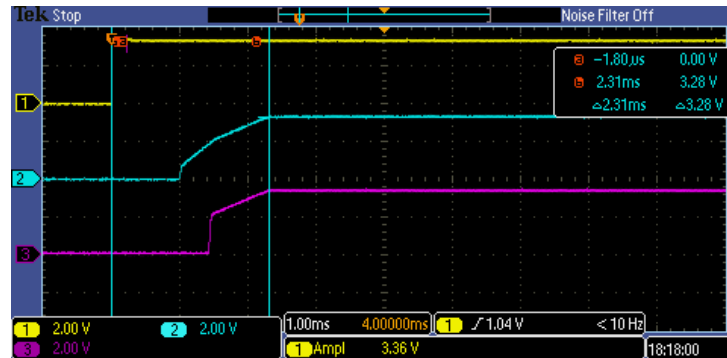
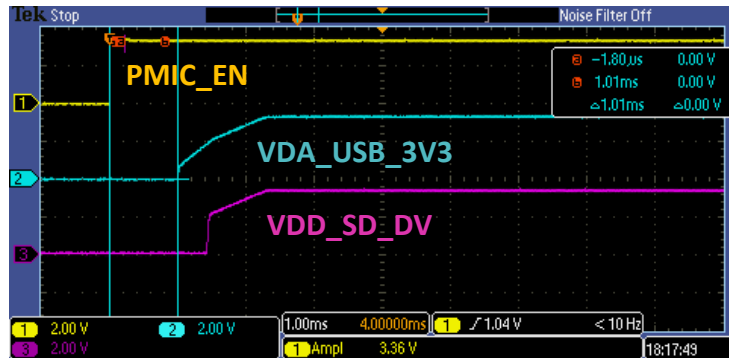
# Controlled Power Up | T0 Time Step



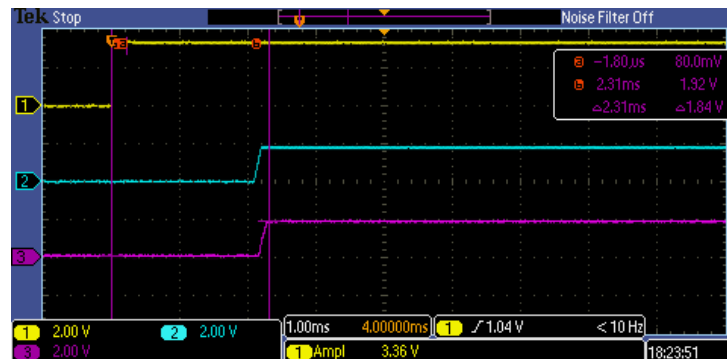
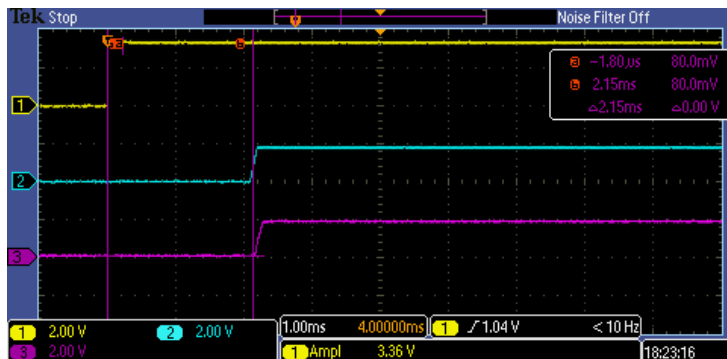
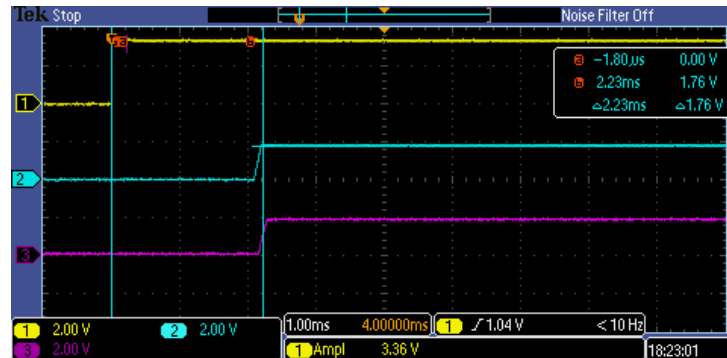
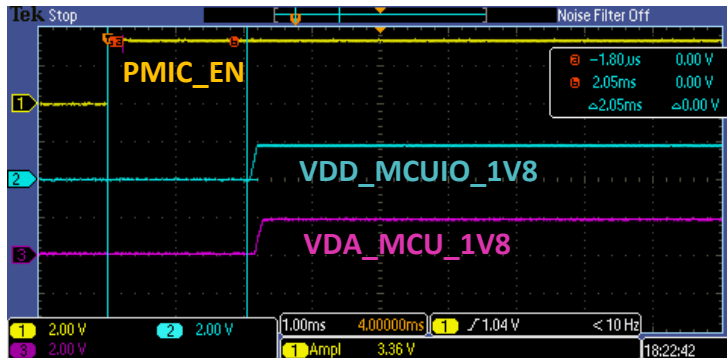


# Controlled Power Up | T0 Time Step

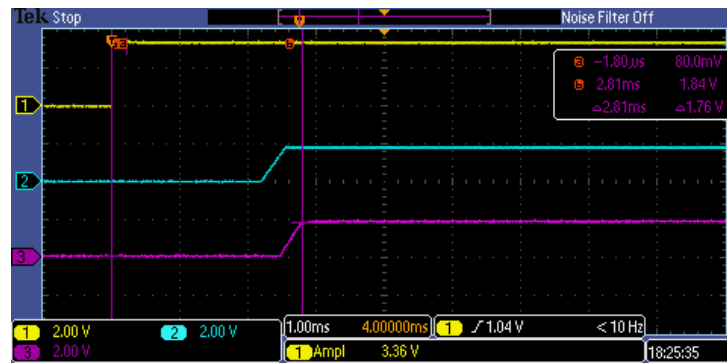
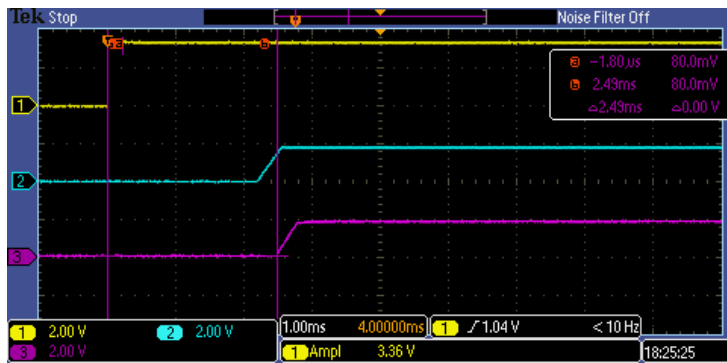
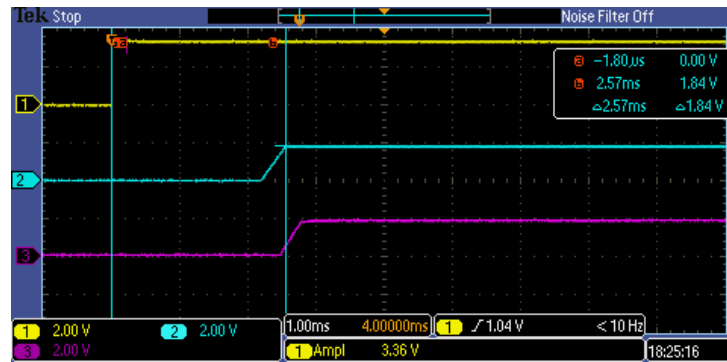
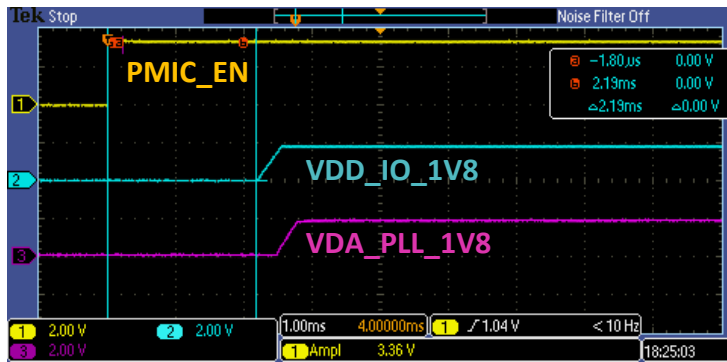
See [“EVM Item #2 5V Ramp Delay”](#)



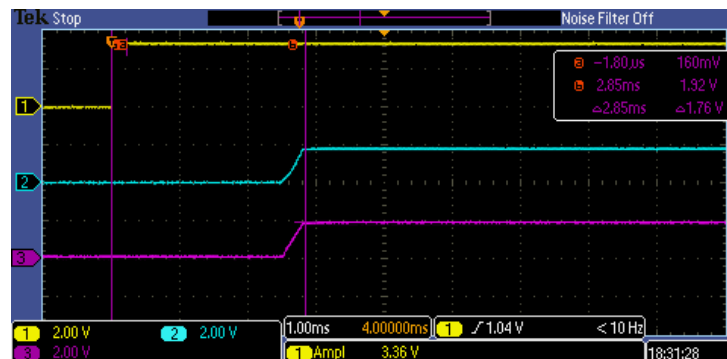
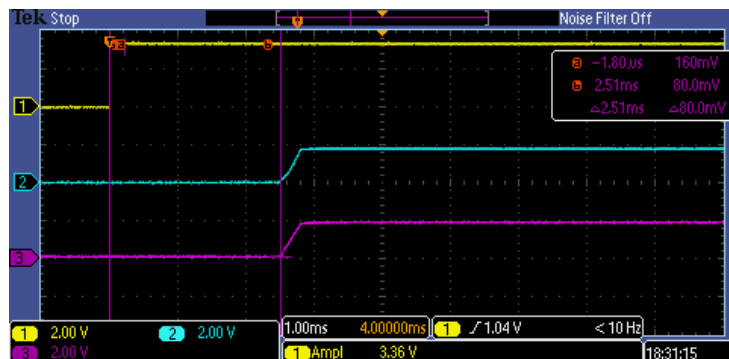
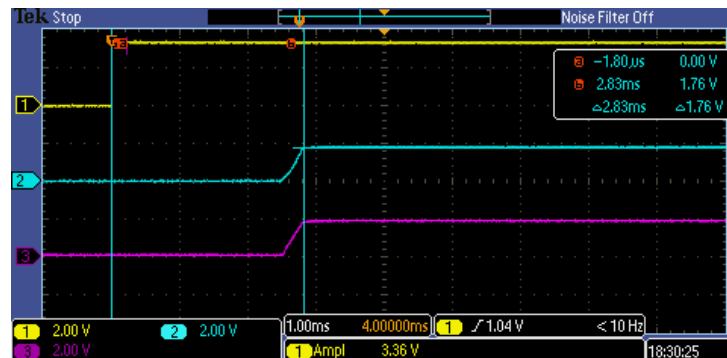
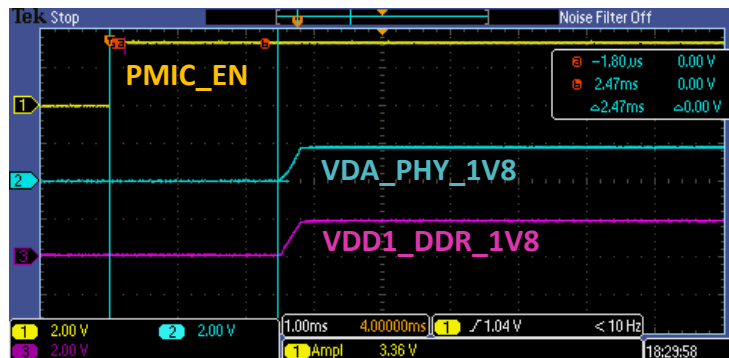
# Controlled Power Up | T1 Time Step



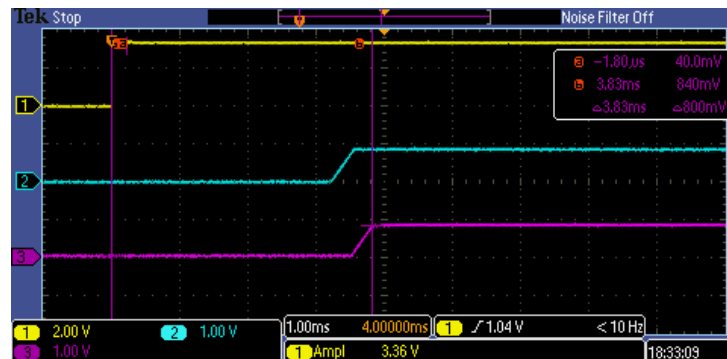
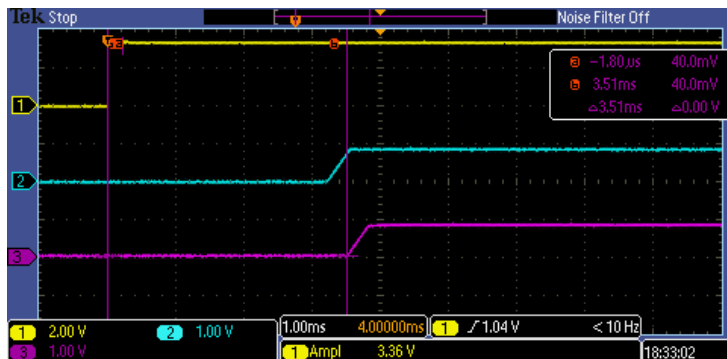
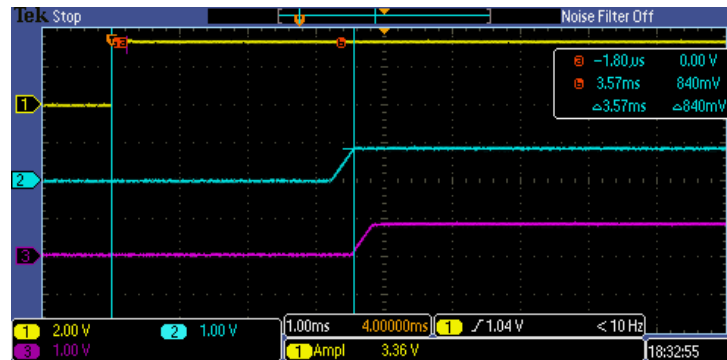
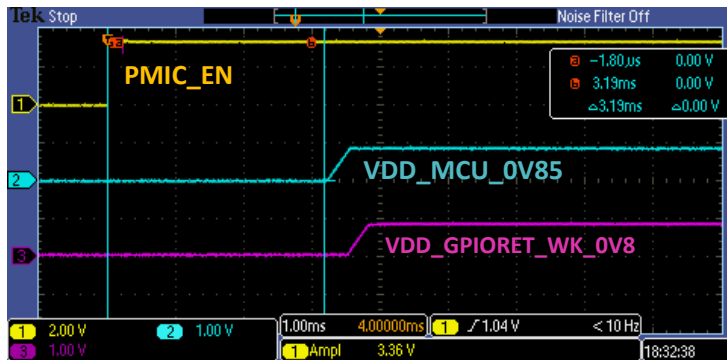
# Controlled Power Up | T1 Time Step



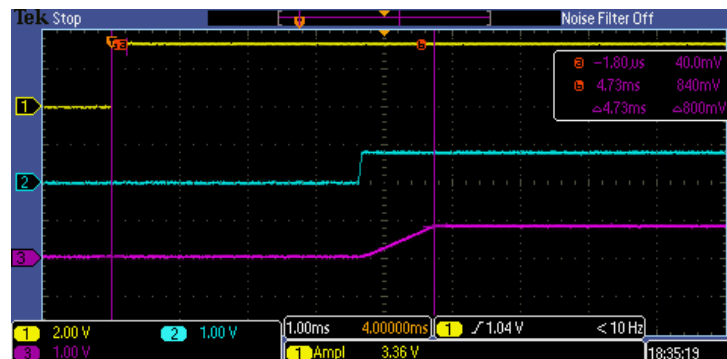
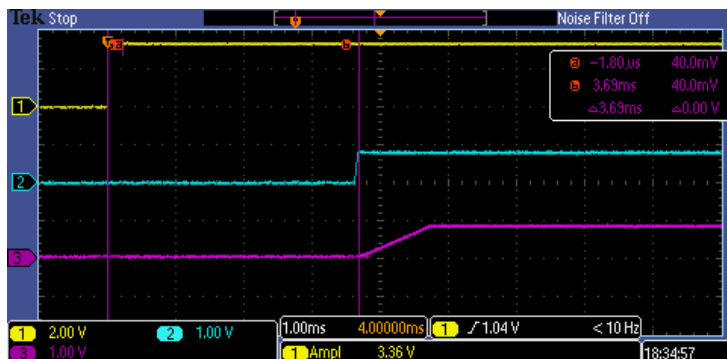
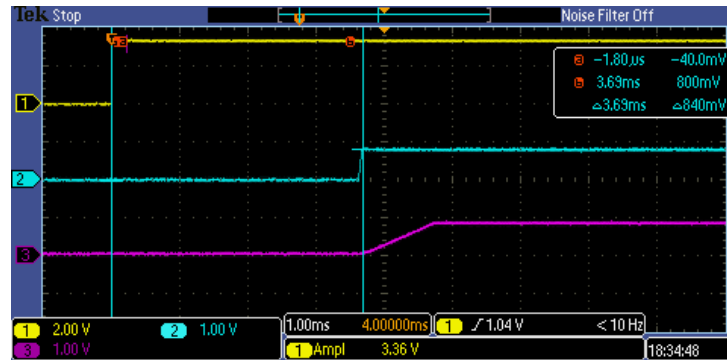
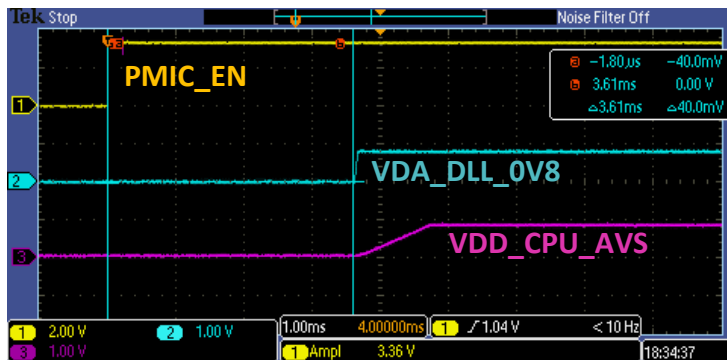
# Controlled Power Up | T1 Time Step



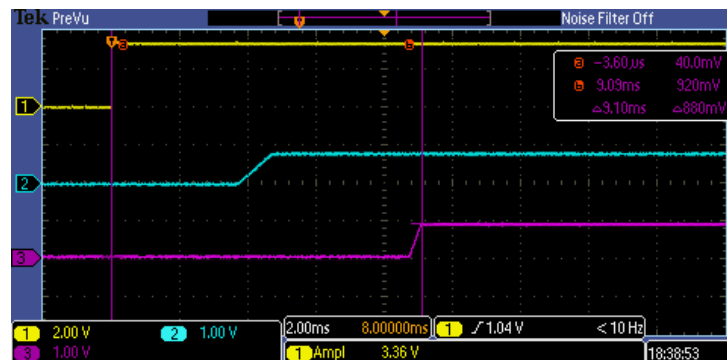
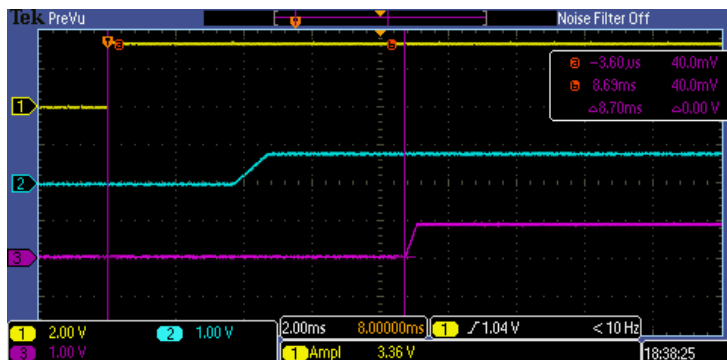
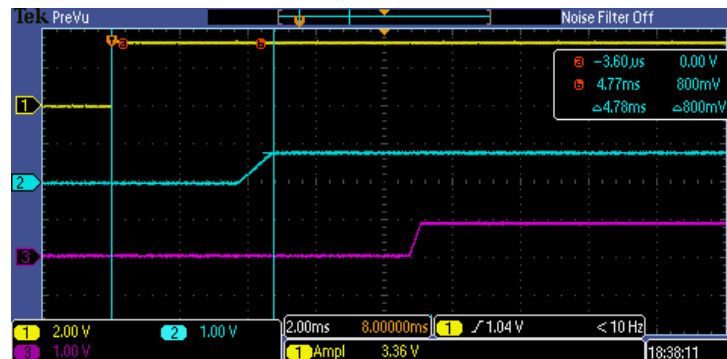
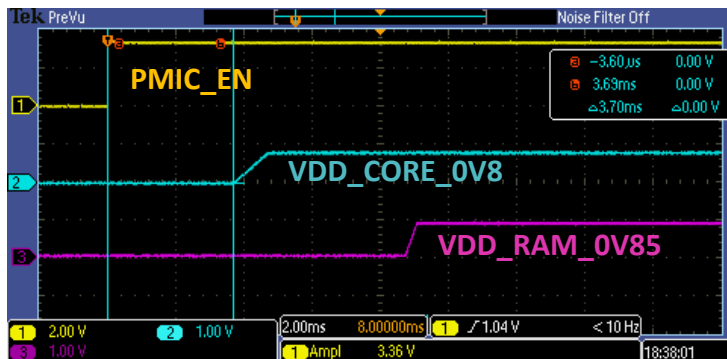
# Controlled Power Up | T2 Time Step



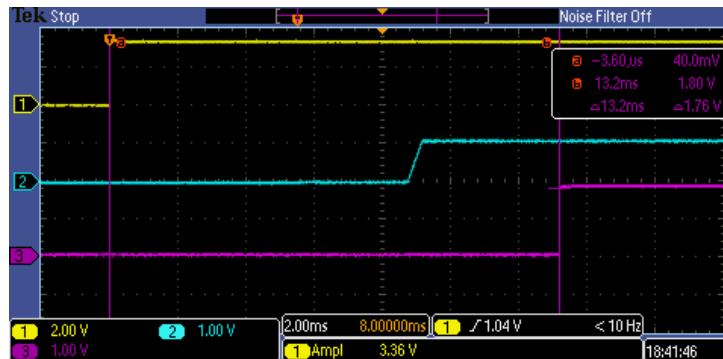
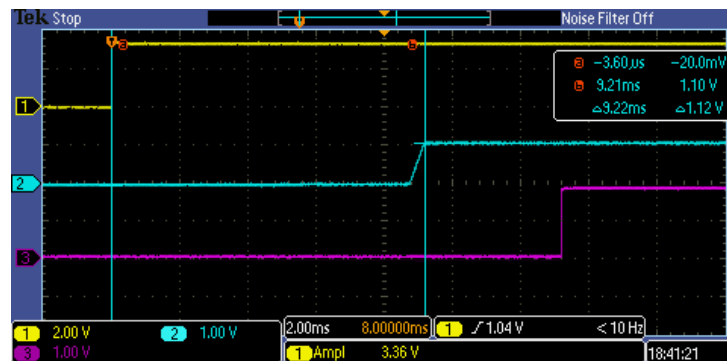
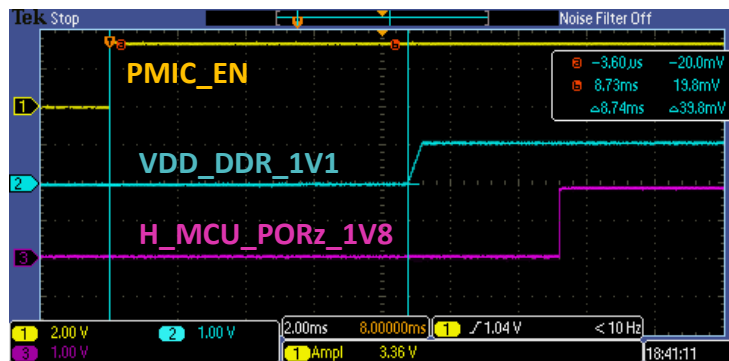
# Controlled Power Up | T2 Time Step



# Controlled Power Up | T2 Time Step

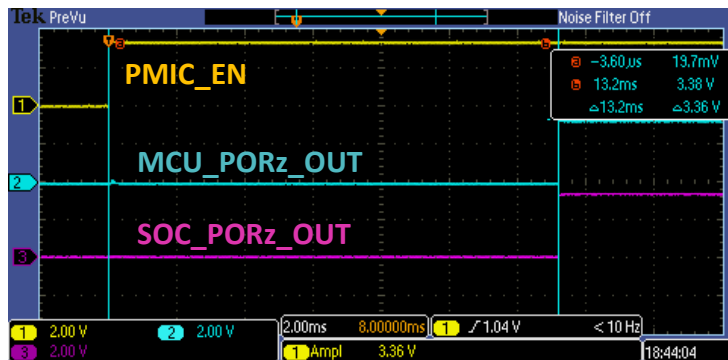
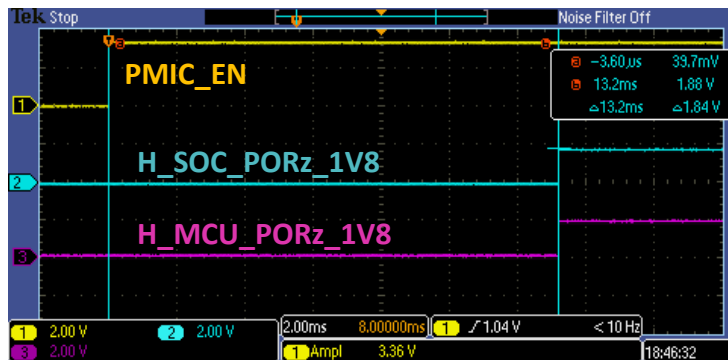


# Controlled Power Up | T3 Time Step





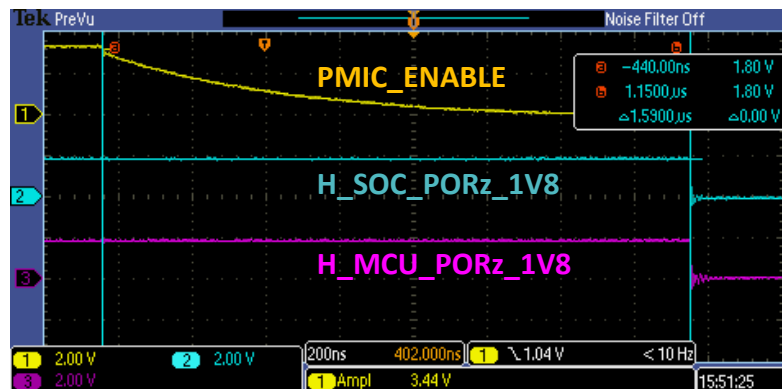
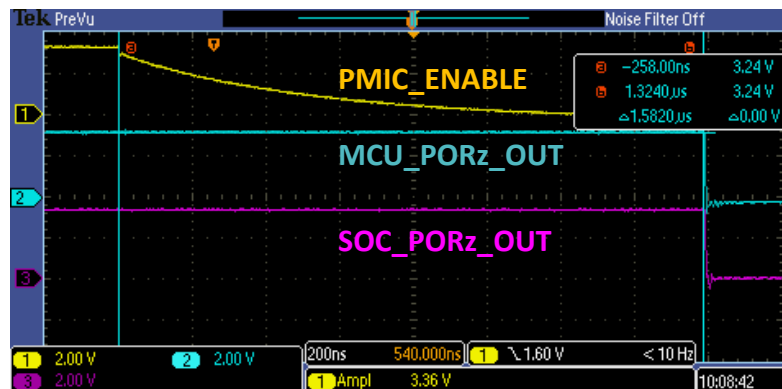
# Controlled Power Up | T4 Time Step



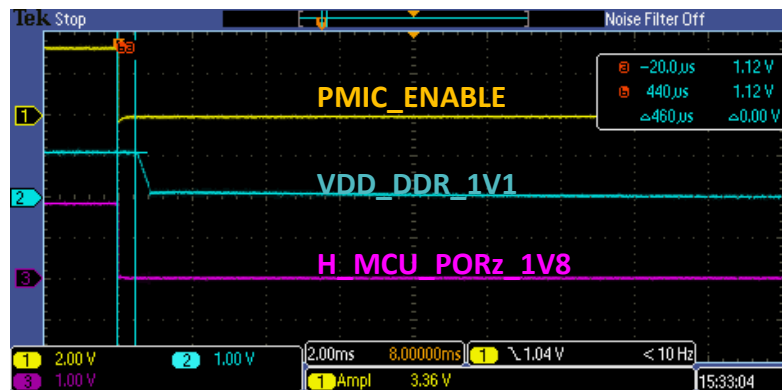
# Controlled Power Down | Sequence Breakdown

Resource	Seq Control (PMIC resource settings)	Supply Rail / Net	Expected	Measured	Remarks
			Ramp-down Start (mS)	Ramp-down Start (mS)	
PMIC's Input Enable	Derived from 1 <sup>st</sup> stage PG & Test Automation logic	PMIC ENABLE	0	0	Scope ref to PMIC_EN which adds 0.1ms to Expected & DM timing diags ref PORz
PMIC's GPIO11	(OD, Low -> High, 0us by state machine)	H_SOC_PORZ	0.1	0.16	PORz & PORz_OUT at same time for Controlled pwr down
PMIC's OD "nRSTOUT"	(OD, Low -> High, 0us by state machine)	H_MCU_PORZ	0.1	0.16	PORz & PORz_OUT at same time for Controlled pwr down
PMIC	(Buck_1+2, 7A, 1.1V, 500us, 1.7- 3.4 V/ms)	VDD_DDR_1V1	0.6	0.46	
PMIC	(Buck_3, 3.5A, 0.85V, 500us, 1.7- 3.4 V/ms)	VDD_RAM_0V85	0.6	0.52	
PMIC	(LDO_3, 0.5A, 0.8V, 3000us, 1.6- 3.2 V/ms)	VDA_DLL_0V8	1.1	1.06	
Dscrt 2-Ph Buck: TPS62873Y1-Q1	VDA_DLL_0V8	VDD_CORE_0V8	2.1	2.44	Time delay due to VDA_DLL_0V8 discharge & buck turn ON & ramp
Dscrt 3-Ph Buck: TPS62873Y1-Q0	VDA_DLL_0V8	VDD_CPU_AVS	2.1	2.46	Time delay due to VDA_DLL_0V8 discharge & buck turn ON & ramp
PMIC	(Buck_5, 2.0A, 0.85V, 3000us, 1.7- 3.4 V/ms)	VDD_MCU_0V85	2.1	2.02	
Dscrt LDO: TPS745xxP-Q1	(Cntrl = VDD_MCU_0V85 # EN_GPIO_RET)	VDD_GPIORET_WK_0V8	2.1	2.22	
Dscrt LDO: TPS745xxP-Q1	(Cntrl = VDD_IO_1V8 # EN_DDR_RET_1V1)	VDD1_DDR_1V8	3.1	3.24	
Dscrt LDO: TPS745xxP-Q1	(Cntrl = VDD_IO_1V8)	VDA_PHY_1V8	3.1	3.24	
Dscrt LDO: TPS745xxP-Q1	(Cntrl = VDD_IO_1V8)	VDA_PLL_1V8	3.1	3.24	
PMIC	(Buck_4, 4.0A, 1.8V, 2000us, 3.6-7.2 V/ms)	VDD_IO_1V8	3.1	3.0	
PMIC	(LDO_4, 0.3A, 1.8V, 2000us, 3.6-7.2 V/ms)	VDA_MCU_1V8	3.1	3.08	
PMIC	(LDO_1, 0.5A, 1.8V, 2000us, 3.6-7.2 V/ms)	VDD_MCUIO_1V8	3.1	3.08	
Dscrt LDO: TLV7103318-Q1	(Cntrl = EN_3V3_VIO)	VDD_SD_DV	3.6	3.6	
Dscrt LDO: TLV73333P-Q1	(Cntrl = EN_3V3_VIO)	VDA_USB_3V3	3.6	3.56	
Dscrt: Load Switch, TPS22965-Q1	(Cntrl = EN_3V3_VIO)	VDD_IO_3V3	3.6	3.48	
Dscrt: Load Switch, TPS22965-Q1	(Cntrl = VDD_MCUIO_3V3 # EN_GPIO_RET)	VDD_GPIORET_IO_3V3	3.6	5.6	See EVM Item #3 GPIORET Delay
PMIC	(LDO_2, 0.165A for FET Bypass, 0us, NA)	VDD_MCUIO_3V3	3.6	3.48	
PMIC	PMIC (GPIO_9 = GPO, VIO, PP, Low @ T0, High @ 0us	EN_3V3_VIO	3.6	3.48	

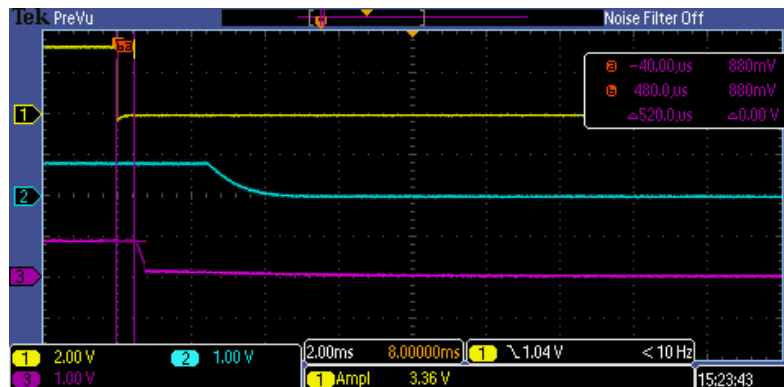
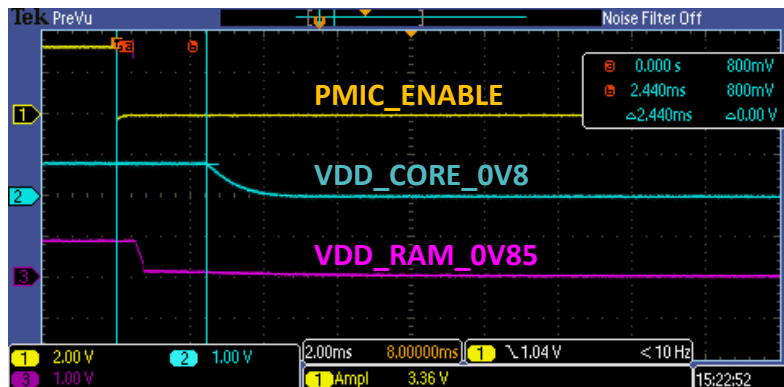
# Controlled Power Down | T0 Time Step



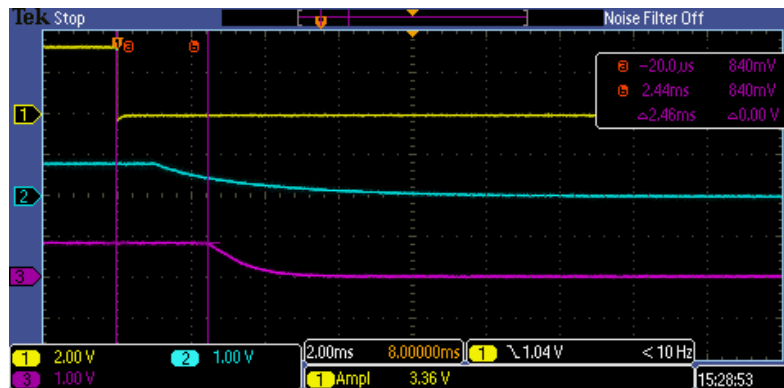
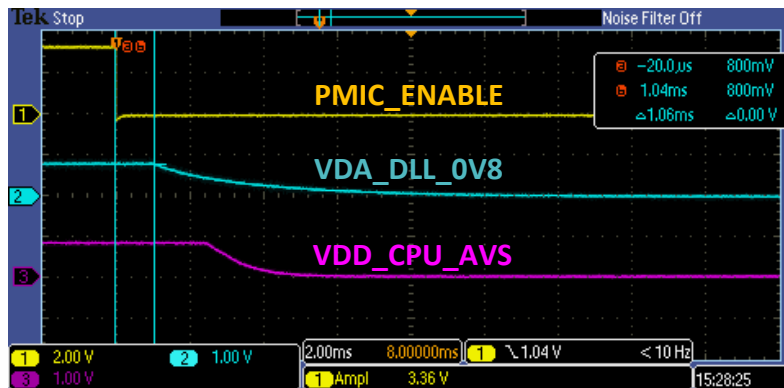
# Controlled Power Down | T1 Time Step



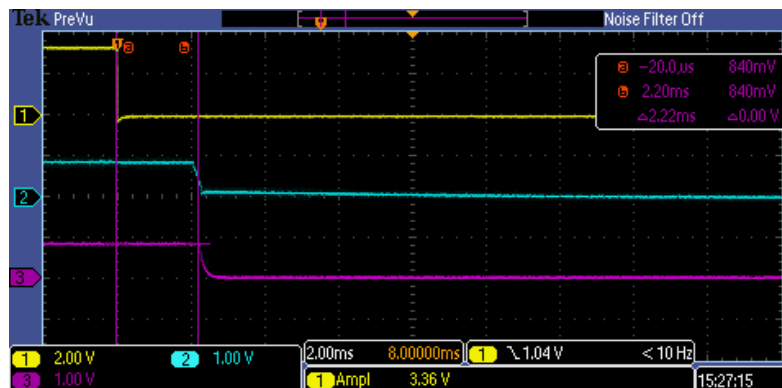
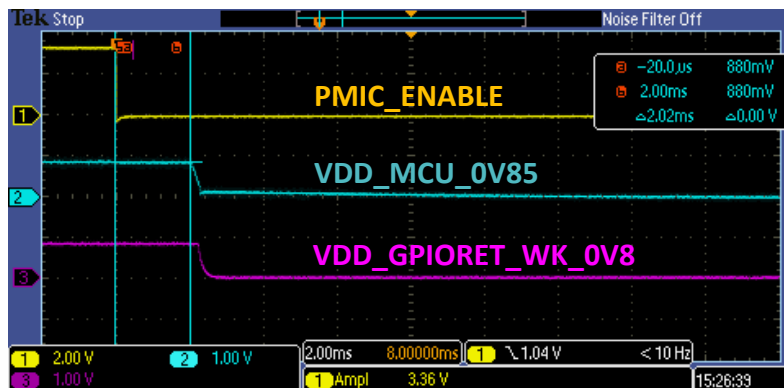
# Controlled Power Down | T2 Time Step



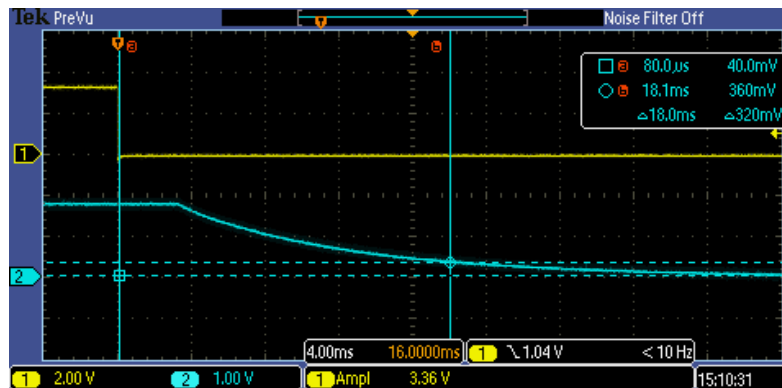
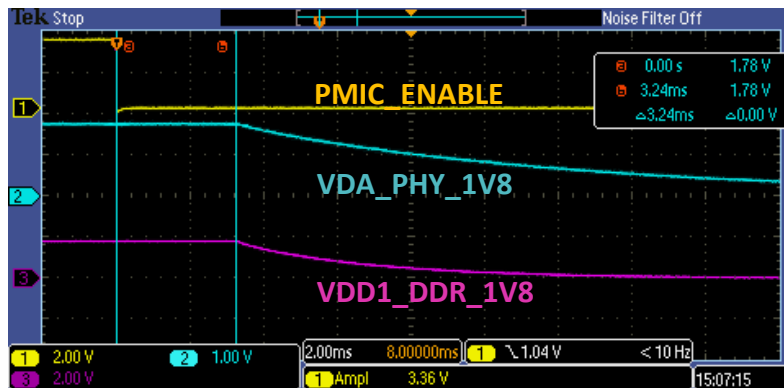
# Controlled Power Down | T2 Time Step



# Controlled Power Down | T2 Time Step



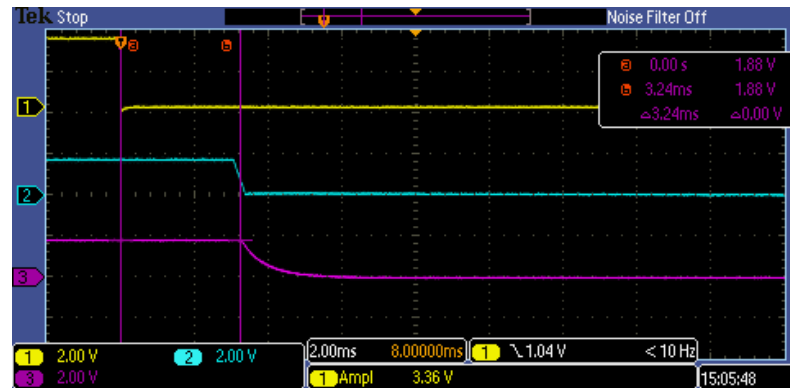
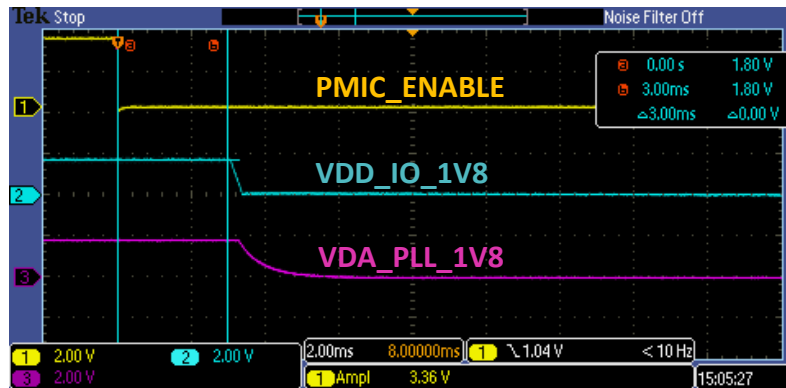
# Controlled Power Down | T3 Time Step



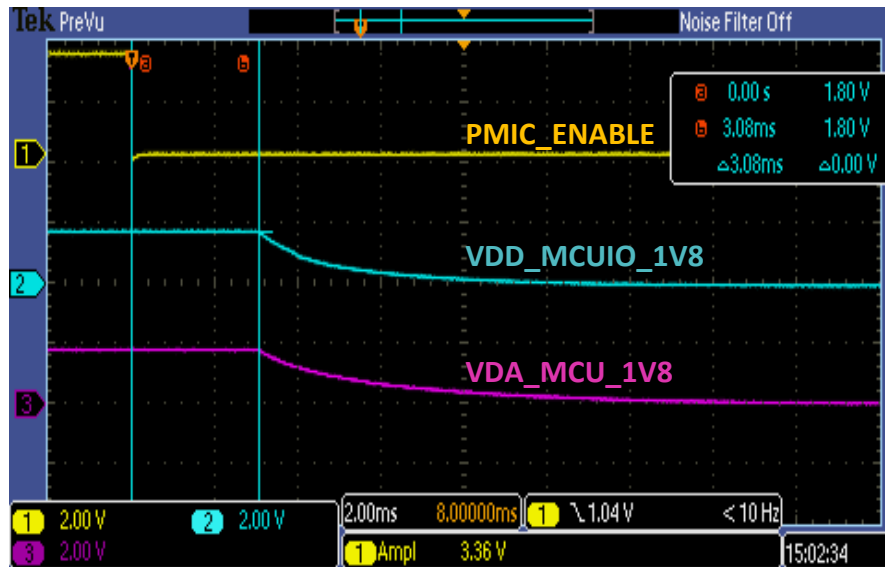
Maximum time to take power down <0.3V



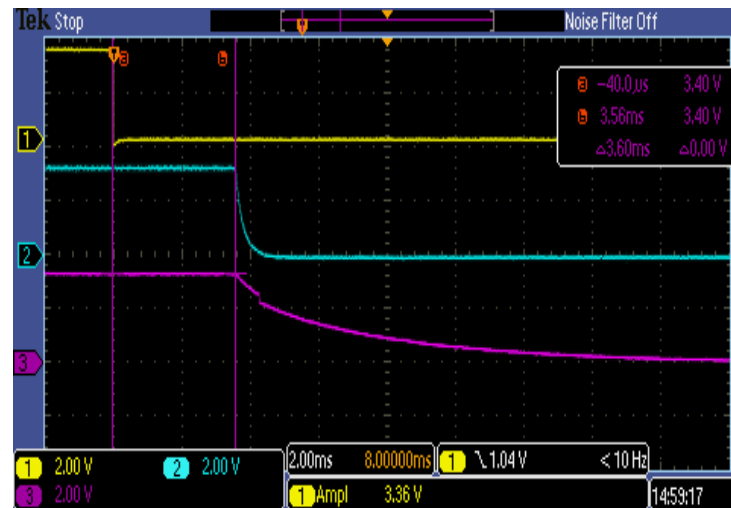
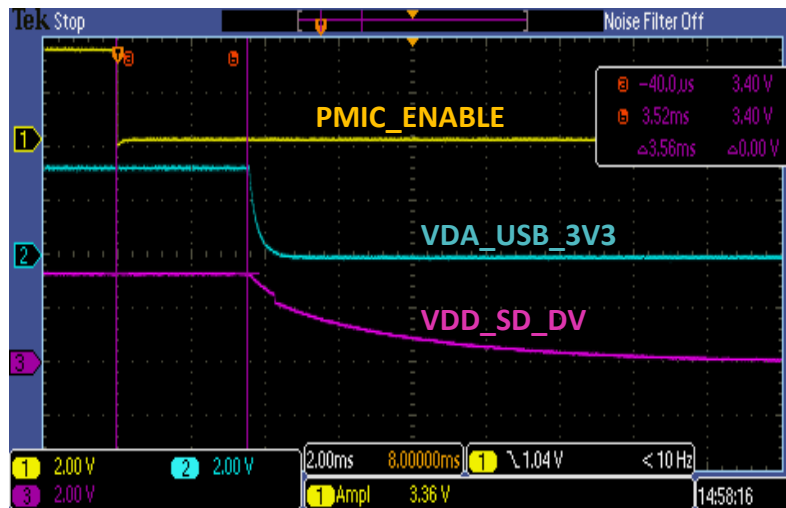
# Controlled Power Down | T3 Time Step



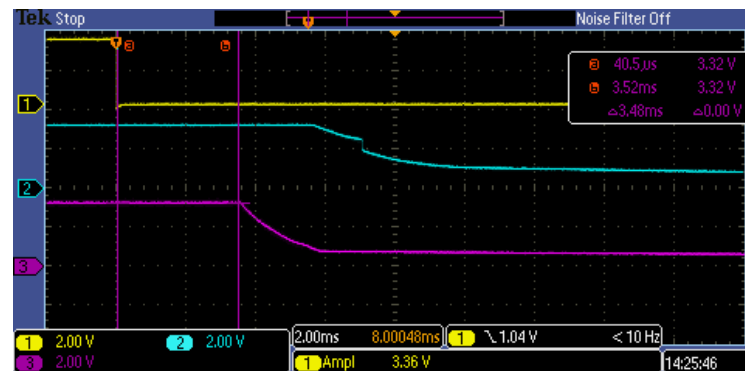
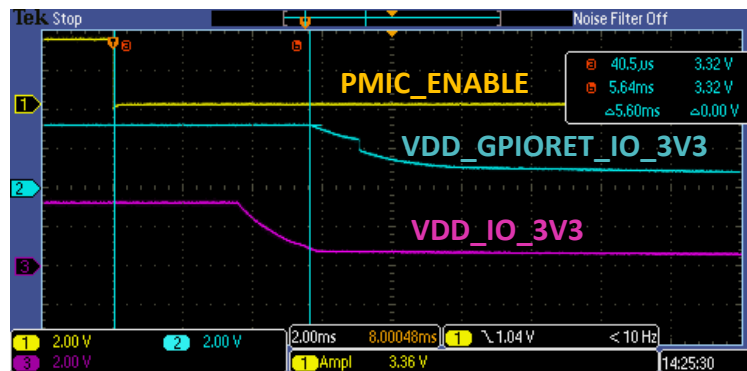
# Controlled Power Down | T3 Time Step



# Controlled Power Down | T4 Time Step

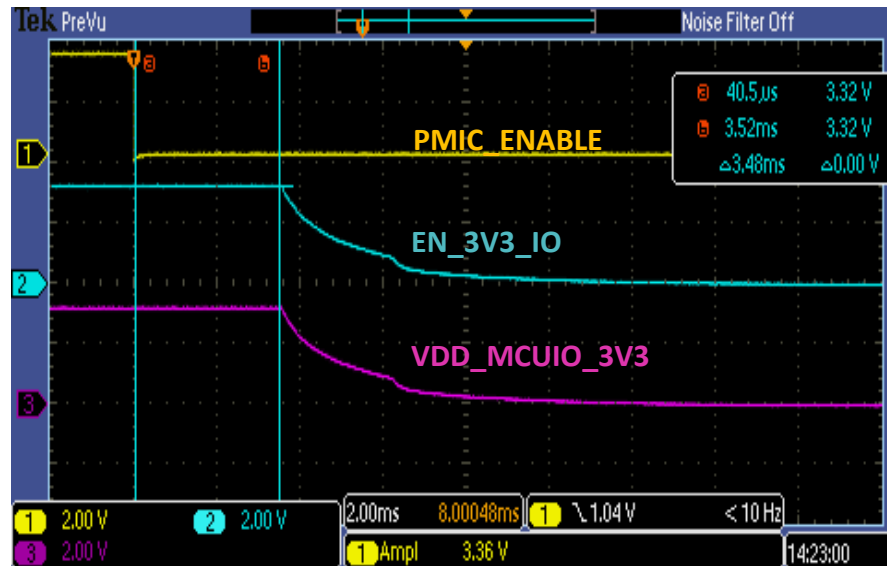


# Controlled Power Down | T4 Time Step



See  
[“EVM Item #3 GPIORET Disable Delay”](#)

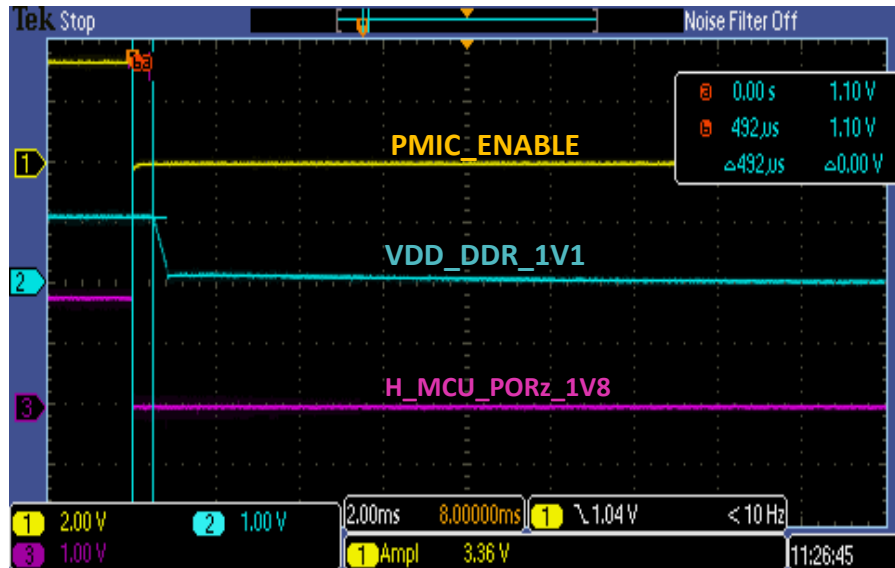
# Controlled Power Down | T4 Time Step



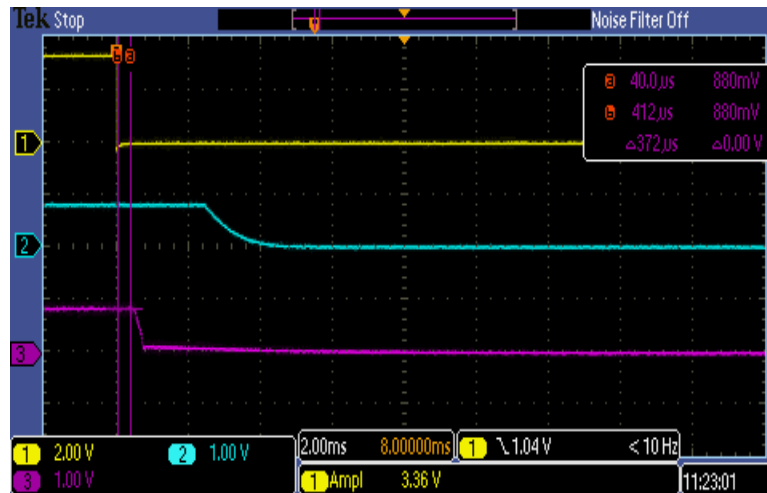
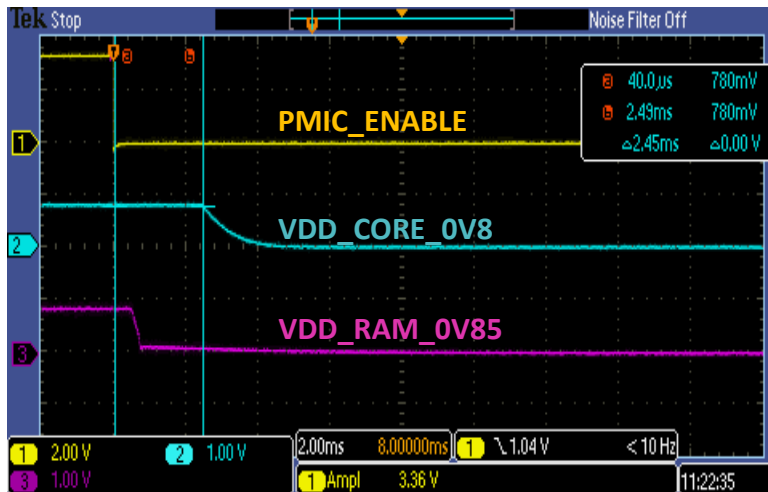
# Input Power Loss | Sequence Breakdown

PMIC – Resource	Control	Supply Rail / Net	Expected	Measured	Remark
			Ramp-down Start (mS)	Ramp-down Start (mS)	
PMIC	(ENABLE/Pin-20 = ENABLE)	PMIC ENABLE	0	0	Scope ref to PMIC_EN which adds 0.1ms to Expected & DM timing diags ref PORz
		SOC_PORZ_OUT	0.1	0	PORZ_OUT leads PORZ due to EVM "Input Pwr Loss Early Warning"
		MCU_PORZ_OUT	0.1	0	PORZ_OUT leads PORZ due to EVM "Input Pwr Loss Early Warning"
PMIC	(GPIO_11 = GPO, OD, Low -> High, 12,200us, NA)	H_SOC_PORZ	0.1	0	PORZ_OUT leads PORZ due to EVM "Input Pwr Loss Early Warning"
PMIC	(nRSTOUT/OD, Low -> High, 12,200us, NA)	H_MCU_PORZ	0.1	0	PORZ_OUT leads PORZ due to EVM "Input Pwr Loss Early Warning"
PMIC	(Buck_1+2, 7A, 1.1V, 8500us, 1.7- 3.4 V/ms)	VDD_DDR_1V1	0.6	0.49	
PMIC	(Buck_3, 3.5A, 0.85V, 8500us, 1.7- 3.4 V/ms)	VDD_RAM_0V85	0.6	0.37	
PMIC	(LDO_3, 0.5A, 0.8V, 3000us, 1.6- 3.2 V/ms)	VDA_DLL_0V8	1.1	1.05	
Dscrt 2-Ph Buck: TPS62873Y1-Q1	(Cntrl = VDA_PLL_0V8)	VDD_CORE_0V8	2.1	2.45	
Dscrt 3-Ph Buck: TPS62873Y1-Q0	(Cntrl = VDA_PLL_0V8)	VDD_CPU_AVS	2.1	2.37	
Dscrt LDO: TPS745xxP-Q1	(Cntrl = VDD_MCU_0V85 # EN_GPIO_RET)	VDD_GPIORET_WK_0V8	2.1	2.24	
PMIC	(Buck_5, 2.0A, 0.85V, 3000us, 1.7- 3.4 V/ms)	VDD_MCU_0V85	2.1	2.04	
Dscrt LDO: TPS745xxP-Q1	(Cntrl = VDD_IO_1V8 # EN_DDR_RET_1V1)	VDD1_DDR_1V8	3.1	3.35	
Dscrt LDO: TPS745xxP-Q1	(Cntrl = VDD_IO_1V8)	VDA_PHY_1V8	3.1	3.31	
Dscrt LDO: TPS745xxP-Q1	(Cntrl = VDD_IO_1V8)	VDA_PLL_1V8	3.1	3.27	
PMIC	(Buck_4, 4.0A, 1.8V, 2000us, 3.6-7.2 V/ms)	VDD_IO_1V8	3.1	3.07	
PMIC	(LDO_4, 0.3A, 1.8V, 2000us, 3.6-7.2 V/ms)	VDA_MCU_1V8	3.1	3.03	
PMIC	(LDO_1, 0.5A, 1.8V, 2000us, 3.6-7.2 V/ms)	VDD_MCUIO_1V8	3.1	2.95	
Dscrt LDO: TLV7103318-Q1	(Cntrl = EN_3V3_VIO)	VDD_SD_DV	3.6	3.56	
Dscrt LDO: TLV73333P-Q1	(Cntrl = EN_3V3_VIO)	VDA_USB_3V3	3.6	3.52	
Dscrt: Load Switch, TPS22965-Q1	(Cntrl = EN_3V3_VIO)	VDD_IO_3V3	3.6	3.5	
Dscrt: Load Switch, TPS22965-Q1	(Cntrl = VDD_MCUIO_3V3 # EN_GPIO_RET)	VDD_GPIORET_IO_3V3	3.6	5.8	See <a href="#">EVM Item #3 GPIORET Delay</a>
PMIC	(LDO_2, 0.165A for FET Bypass, 0us, NA)	VDD_MCUIO_3V3	3.6	3.54	
PMIC	PMIC (GPIO_9 = GPO, VIO, PP, Low @ T0, High @ 0us)	EN_3V3_VIO	3.6	3.54	
PMIC's VCCA	VCCA < ~2.7V shuts down PMIC's internal logic VINT	VINT = 0V		65	See <a href="#">EVM Item #4 Input Pwr Loss Early Warning</a>

# Input Power Loss | T0 & T1 Time Steps

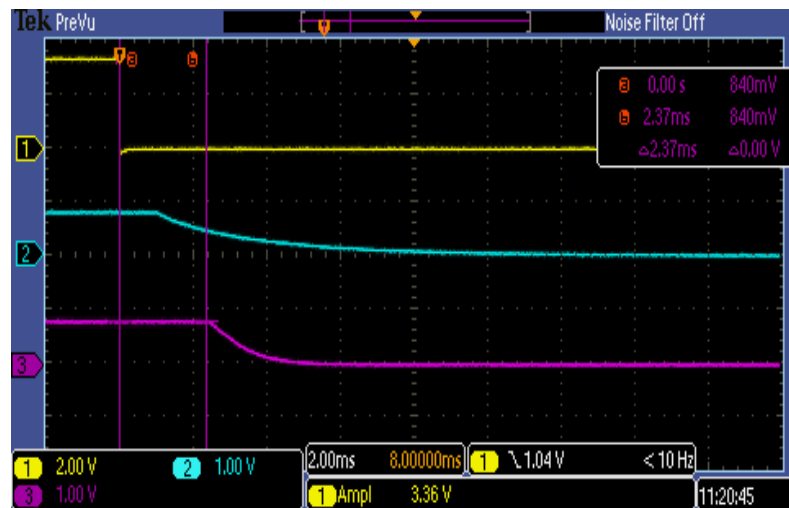
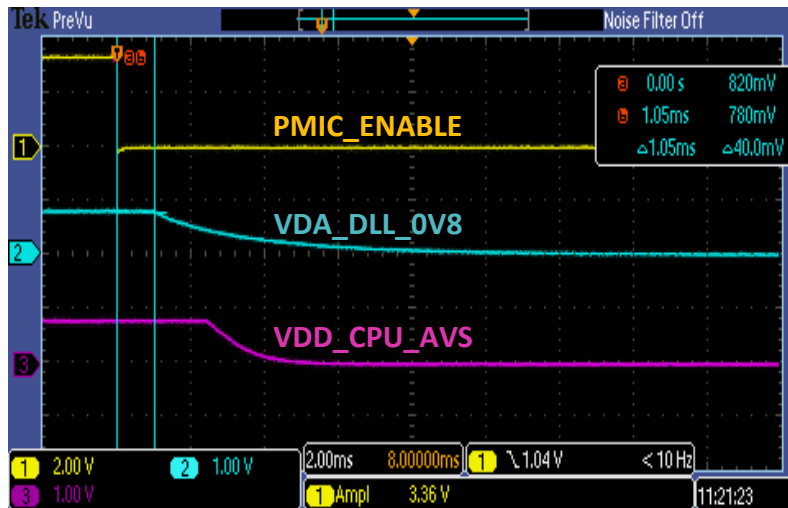


# Input Power Loss | T2 Time Step

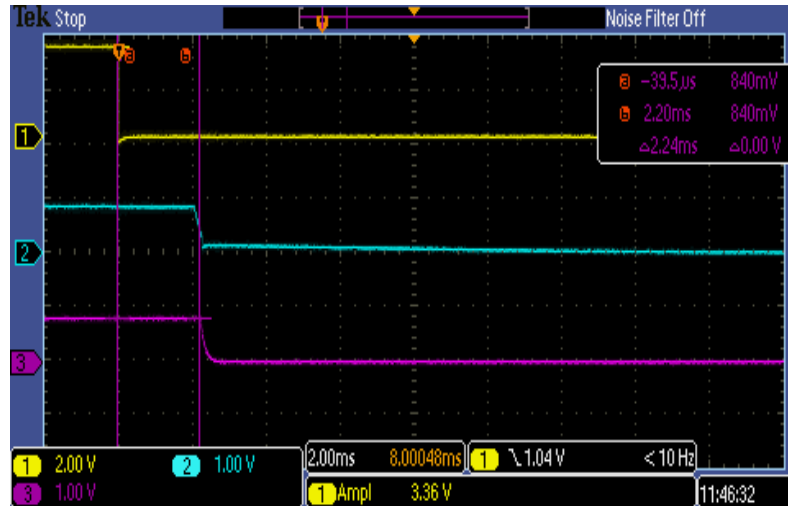
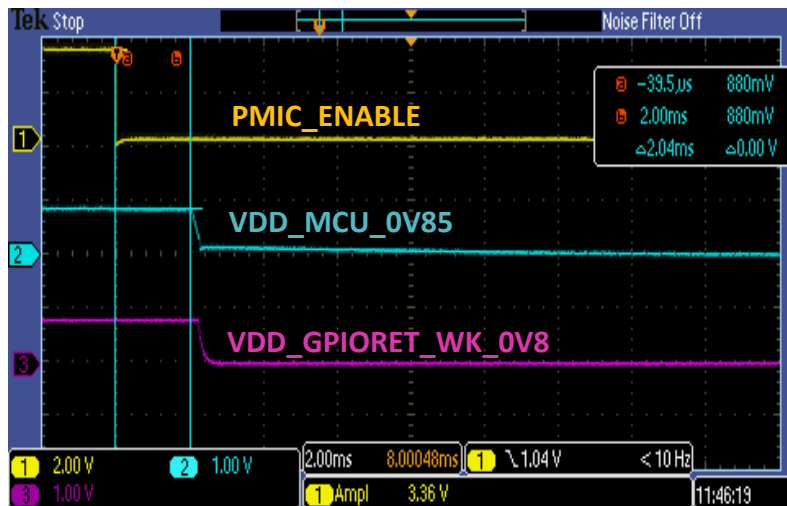




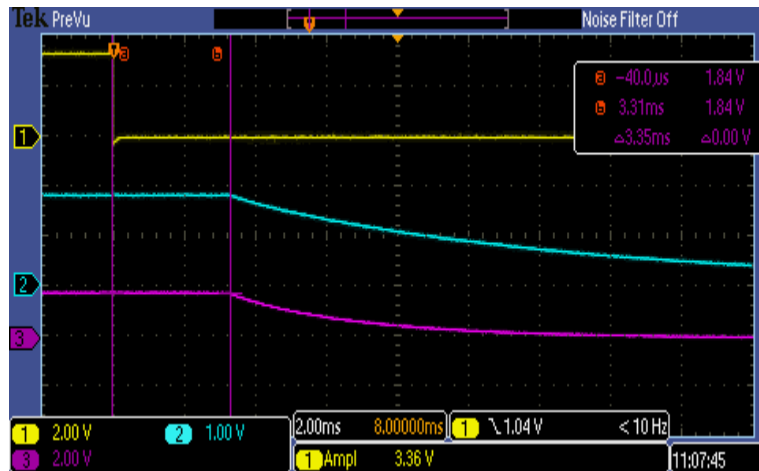
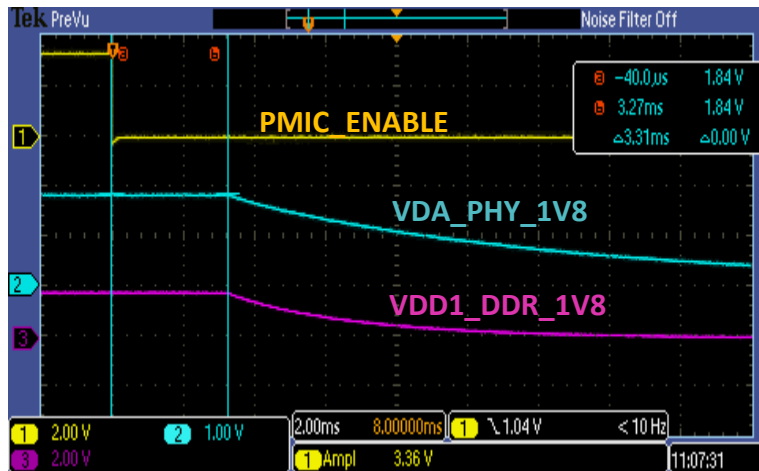
# Input Power Loss | T2 Time Step



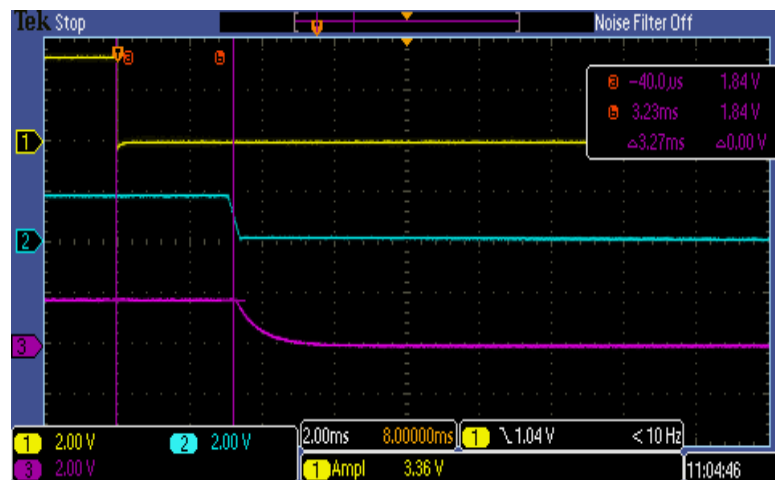
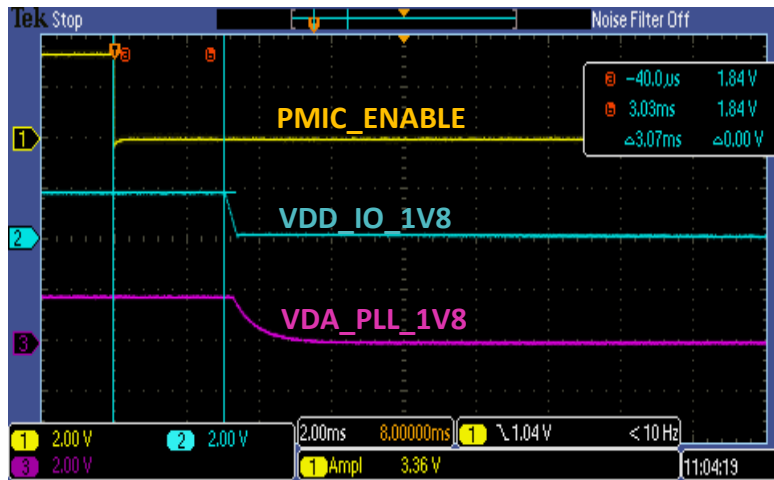
# Input Power Loss | T2 Time Step



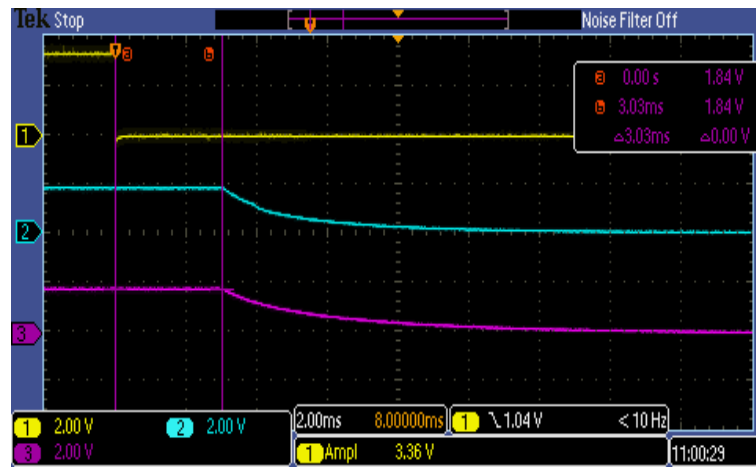
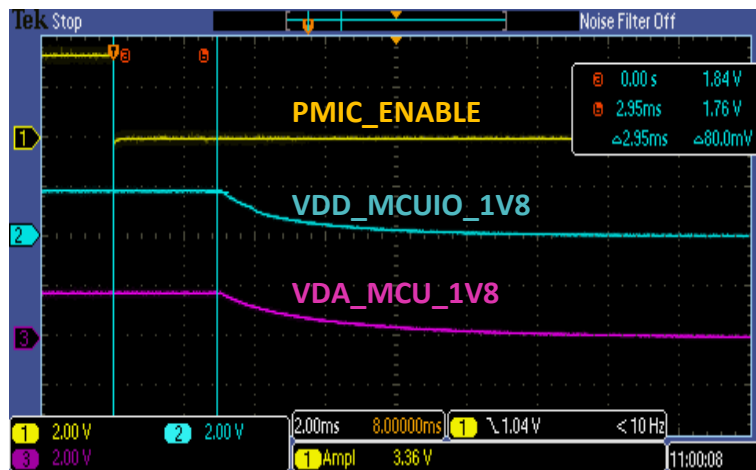
# Input Power Loss | T3 Time Step



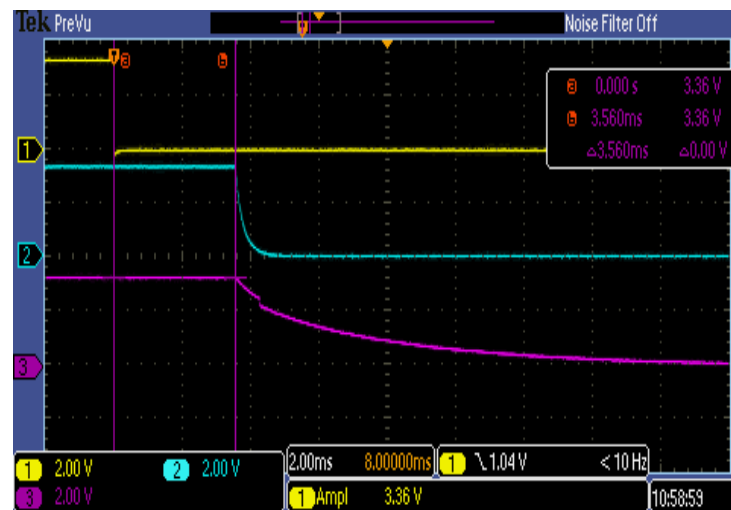
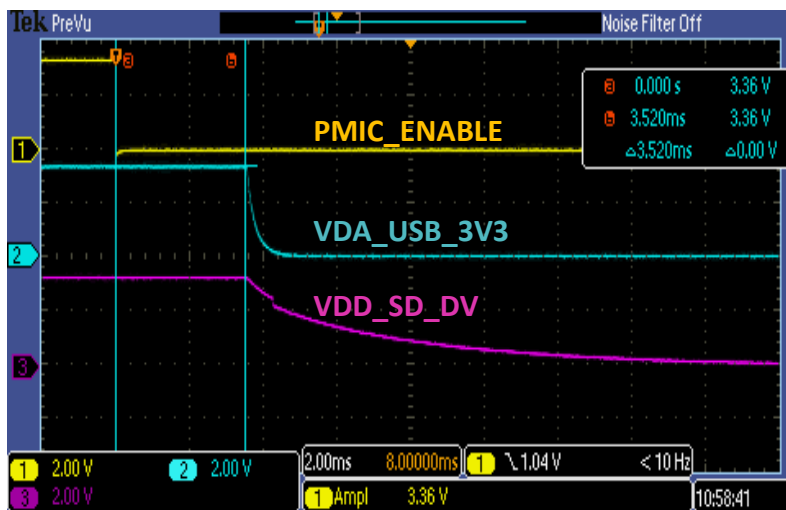
## Input Power Loss | T3 Time Step



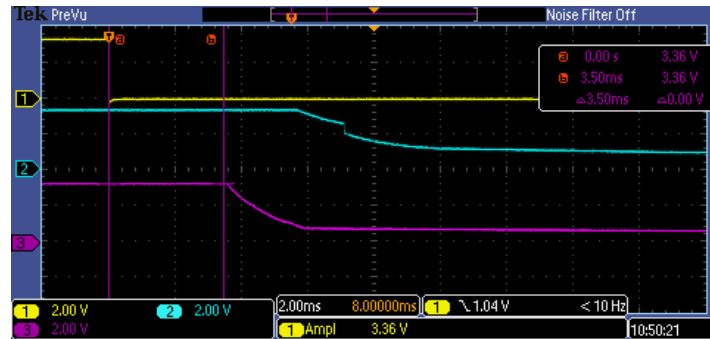
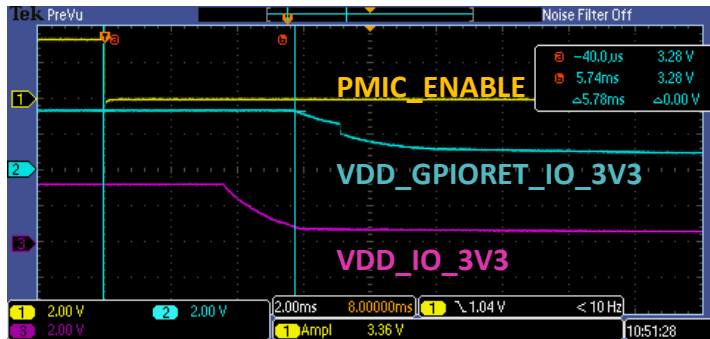
# Input Power Loss | T3 Time Step



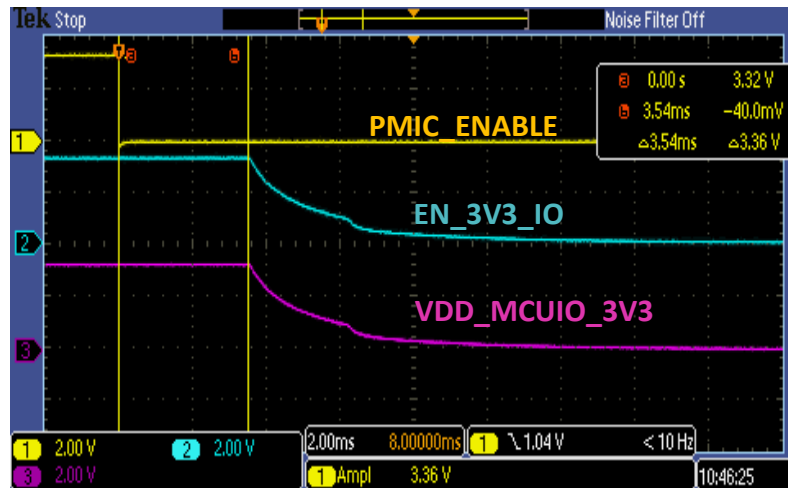
# Input Power Loss | T4 Time Step



# Input Power Loss | T4 Time Step



# Input Power Loss | T4 Time Step





# Reference Section

# EVM Reference | PMIC & NVM Specific Start-Up

## Leo PMIC (TPS6594x-Q1) Data Manual

### 8.4.1.4 Device Start-up Timing

Figure 8-44 shows the timing diagram of the TPS6594-Q1 after the first supply detection.

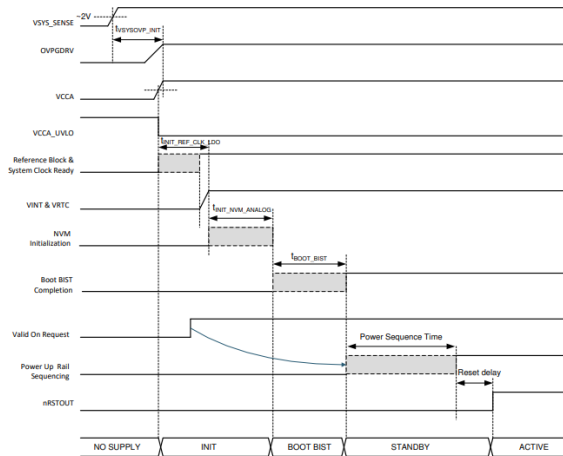


Figure 8-44. Device Start-up Timing Diagram

### Note:

The PMIC “133A” NVM adds a new “Wait for Enable” state (5.5ms max) following “Boot BIST” state and before a Valid ON request begins a power up seq, as shown below. This enables the PMIC to latch logic levels on GPIO8 & GPIO9 that direct the PMIC’s state machine to configure resources as needed for different PDN schemes during the power up seq execution.

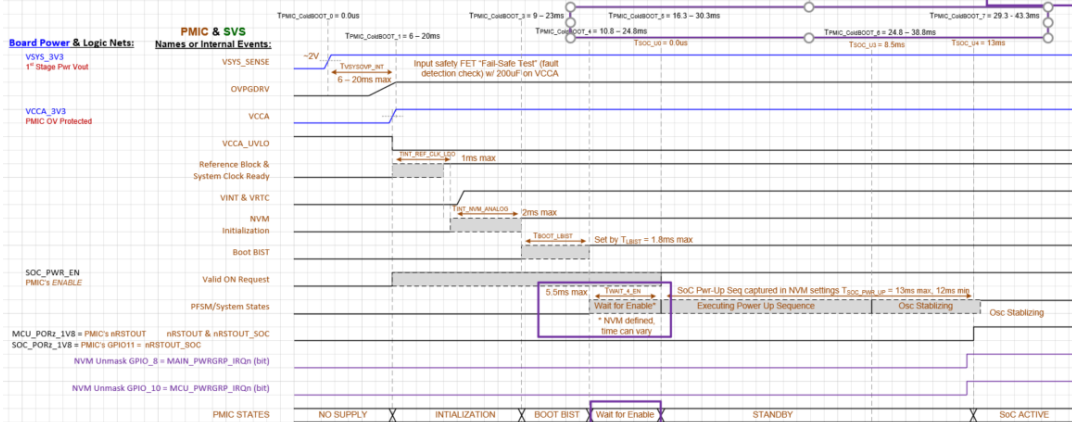
### TPS6594133A PMIC + TPS389006004 SVS Cold Boot-up Timing for PDN-3x

Leo PMIC-A, PN TPS6594133ARWERQ1 (TI PN ID = 1, MP Buck Rails = 2, PG2.0 NVM ID = 3A Rev 5)

HCPS-A & B, Tulip PN TPS62873Y1QWRXSQR1 (15A PN ID = 3, Jacinto7 Family ID = Y1)

Safety Voltage Supervisor, PN TPS389006004RTERQ1 (OTP ID = 004 = new common PN for use with J7 PDN-3x scheme)

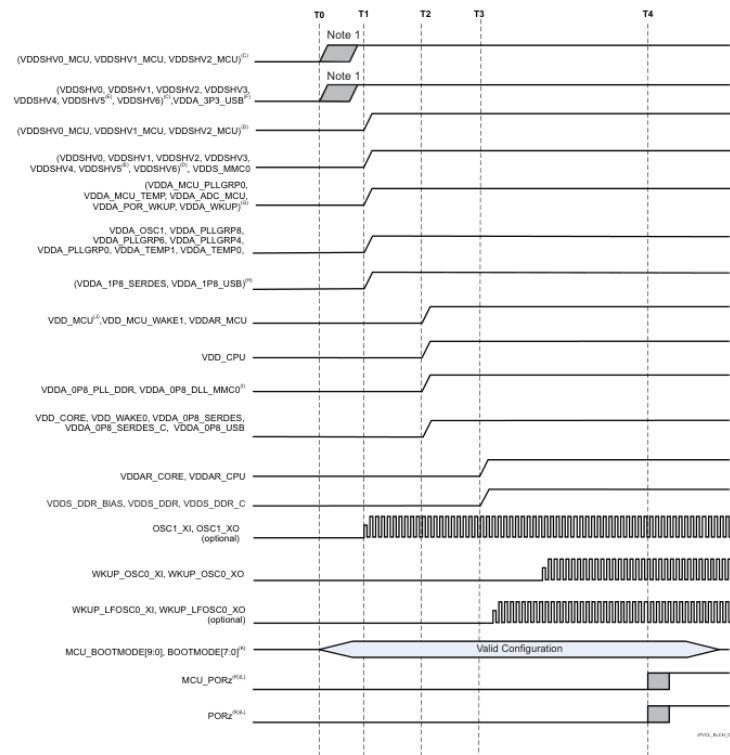
Rev	Date
V0.1	5/21/2022
V0.2	5/24/2022
V0.3	5/31/2022
V0.4	6/2/2022
V0.5	6/30/2022
V0.6	8/31/2022
V0.27	11/20/2024



# EVM Reference | SoC Data Manual



TDA4VH-Q1, TDA4AH-Q1, TDA4VP-Q1, TDA4AP-Q1  
SPRSP79B – FEBRUARY 2023 – REVISED DECEMBER 2023



## A. Time stamp markers:

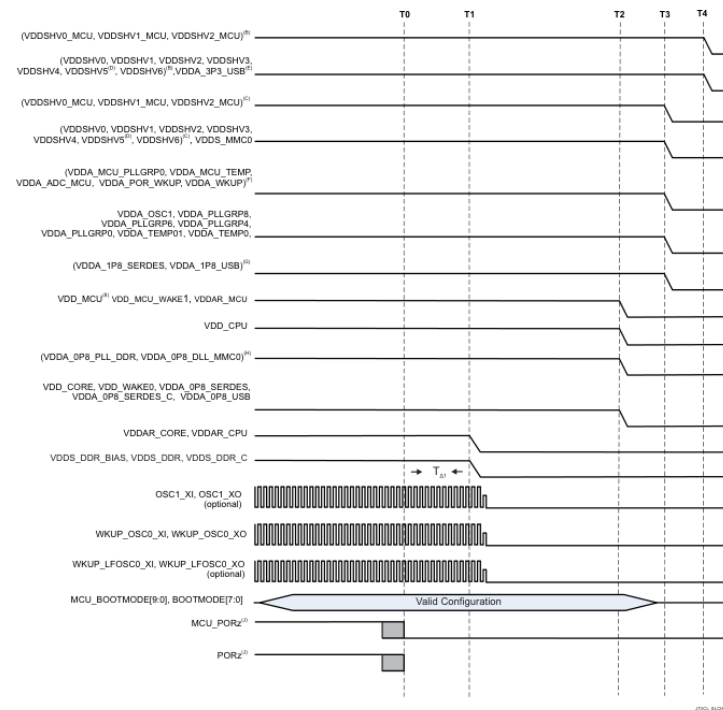
- T0 – All 3.3-V voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (0 ms)
- T1 – All 1.8-V voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (2 ms)
- T2 – All core voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (3 ms)
- T3 – All RAM array voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (4 ms)
- T4 – OSC1 is stable and PORZ/MCU\_PORZ are de-asserted to release processor from reset. (13 ms)



TDA4VH-Q1, TDA4AH-Q1, TDA4VP-Q1, TDA4AP-Q1  
SPRSP79B – FEBRUARY 2023 – REVISED DECEMBER 2023

## 6.10.2.5 Isolated MCU and Main Domains Power- Down Sequencing

Figure 6-6 describes the device power-down sequencing.



## A. Time stamp markers:

- T0 – MCU\_PORZ and PORZ assert low to put all processor resources in safe state. (0 ms)
- T1 – Main DDR, SRAM Core, and SRAM CPU power domains start ramp-down. (0.5 ms)
- T2 – All core voltages start supply ramp-down. (2.5 ms)
- T3 – All 1.8V voltages start supply ramp-down. (3.0 ms)
- T4 – All 3.3V voltages start supply ramp-down. (3.5 ms)

# EVM Reference | SoC Power Up & Down Sequence Timing

## J784S4 EVM Leo + 2x High-Current Pwr Stages(HPCS) PDN-3A

Leo PMIC-A, PN TP56594133ARWERQ1 (Ti PN ID = 1, MP Buck Rails = 3, PG2.0 NVM ID = 3A Rev 4 or higher)

HPCS-A & B, Tulip PN TP562873Y1QWRWSRQ1 (ISA PN ID = 3, Jacinto7 Family ID = Y1)

Safety Voltage Supervisor, PN TP538900604RTERQ1 (OTP ID = 004 = new common PN for use with Jacinto7)

J784S4 PDN-3A scheme)

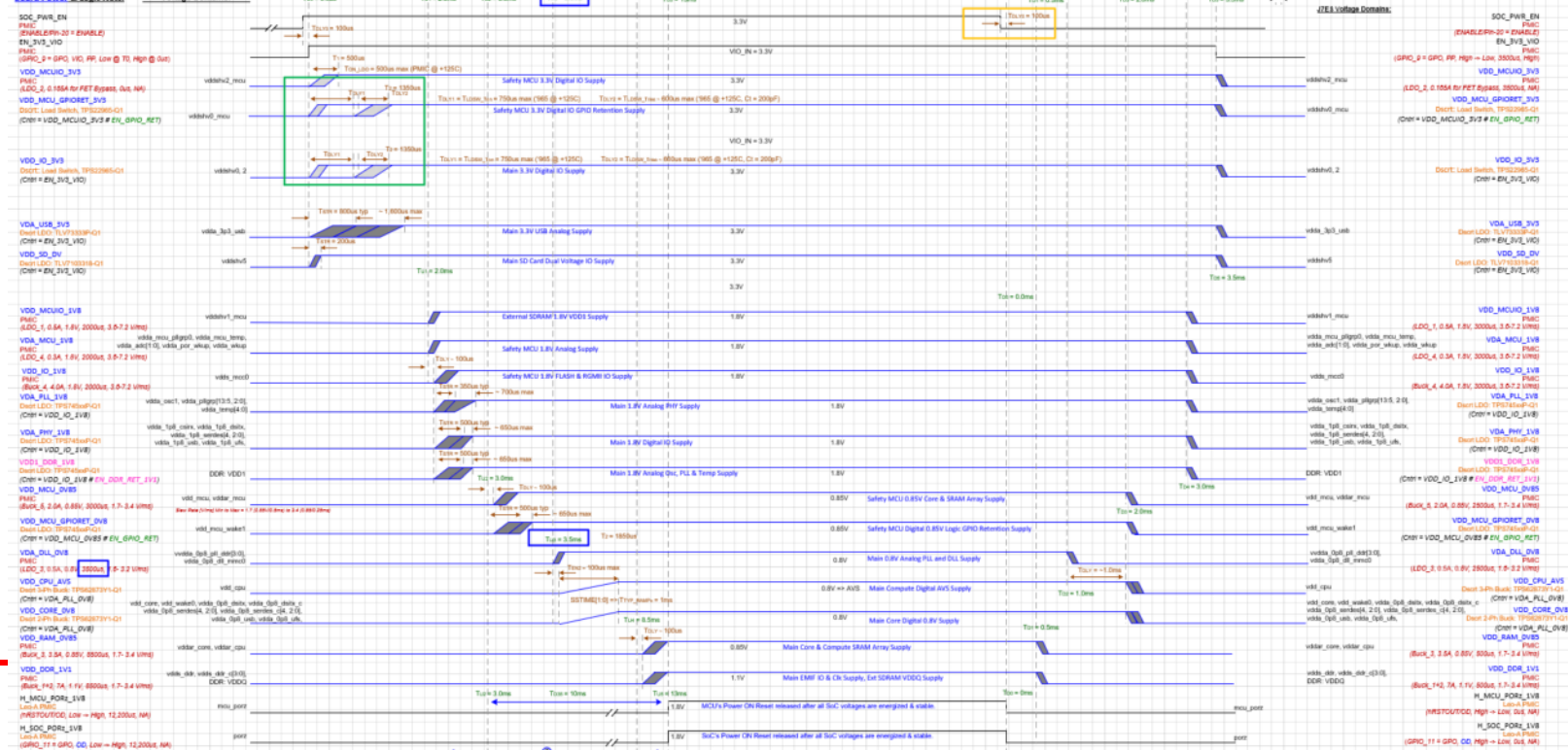
Rev	Date	By	Desc
VO.23	10/26/2023	BMC	1. Increase time btw pwr up seq Time Step #2 vs #3 to add 0.5ms margin btw VDD_MCU_OVB5 vs VDD_CORE_OVB8 for worst case per SoC errata (2406)
VO.23c	12/06/2023	BMC	2. Updated PMIC PN NVM revision from v2 to v4
VO.29	2/07/2025	BMC	3. Added new power up seq constraints list for quick reference as needed to align with Errata (2406 "IO Glitches during Pwr Up Seqs")
VO.30	2/19/2025	BMC	1. Corrected power up seq timing diagram to correctly show time btw pwr up seq Time Step #2 vs #3 as only 0.5ms (instead of 1.0ms)
VO.31	3/21/2025	BMC	1. Corrected diag to show SOC_PWR_EN (PMIC_ENABLE input) signal asserting low 0.3ms (PMIC's internal delay T <sub>EN</sub> ) before PMIC's state machine begins executing power down seq by 1 <sup>st</sup> setting MCU_PORZ & SOC_PORZ low.
		BMC	2. Corrected diag to show both VDD_GPIORET_IO_3V3 & VDD_IO_3V3 min enable time could be ~0.1ms after enabling signals (VDD_MCUIO_3V3 & EN_3V3_IO respectively).
		BMC	3. An "Immediate Shutdown/Power Down Seq" has recently been approved and will be add to an upcoming data manual version. This simplifies SoC power down to only require both PORZ signals to be set low for 1-2us before disabling SOC input supplies in any order

- Control Signal Rats / SoC voltage domains
- Control Signal Rats / SoC voltage domains
- Control Signal Rats / SoC voltage domains

Current Capacity, Boost Voltage, Delay After Enable [ns], Slow Rate [mV/us]  
Function, Rail Voltage, Output Buffer Type, Logic @ T=0, Logic @ Elapsed time [us]  
Power Resource and Board Power Rail counts that transition during power sequences  
"AND" logic  
Verified per NVM file

NVM Settings, Plan-Up Seq

Board Power & Logic Lists:



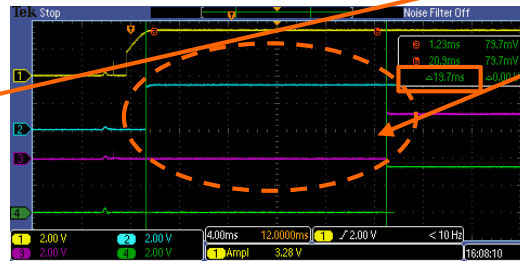
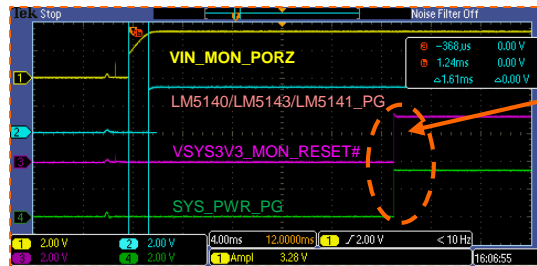
# TI Reference | Website Links

## Source References & Links

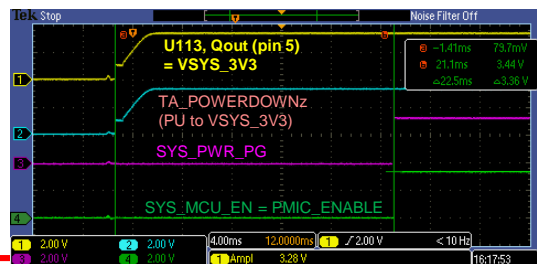
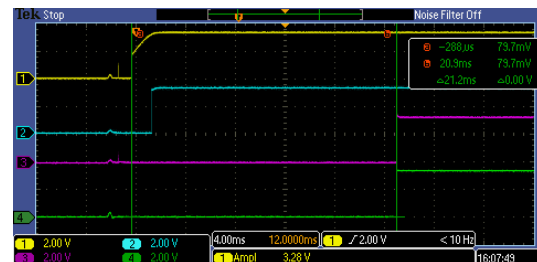
1. [TDA4VH-Q1, TDA4AH-Q1, TDA4VP-Q1, TDA4AP-Q1 Jacinto™ Processors datasheet \(Rev. B\)](#)  
Data Manual
2. [J784S4XEVm Evaluation board | TI.com](#)  
EVM Schematic PROC141E5\_SCH and J784S4 EVM PDN-3A detailed block diagram with power sequences
3. [TPS6594-Q1 Power Management IC \(PMIC\) for Processors with 5 Bucks and 4 LDOs datasheet \(Rev. B\)](#)  
TPS6594x-Q1 Datasheet
4. [Powering Jacinto 7 SoC For Isolated Power Groups With TPS6594133A-Q1 + Dual HCPS](#)  
TPS6594133A User's Guide

# EVM Items

# EVM Item #1 | PMIC\_ENABLE Delay

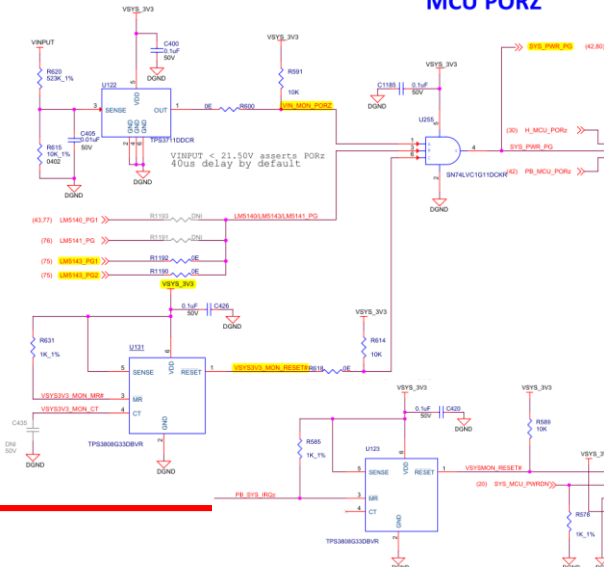


The VSYS3V3\_MON\_RESET# signal delays SYS\_PWR\_EN = PMIC\_ENABLE signal asserting high by ~19.7ms after VSYS\_3V3 ramps.

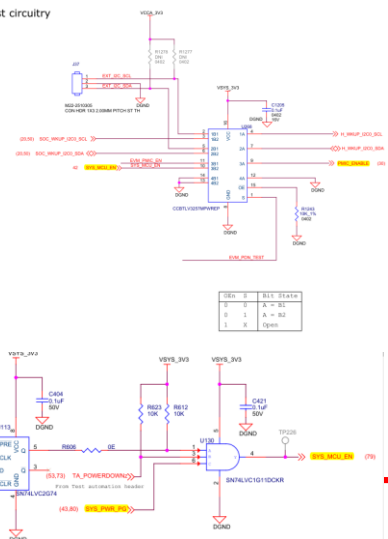


Under Voltage Monitor (VINPOT)

MCU PORZ



Test circuitry



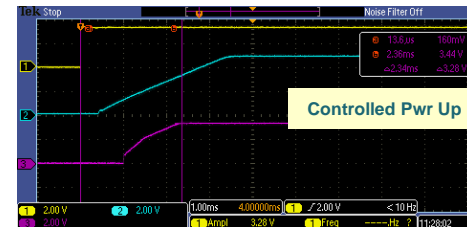
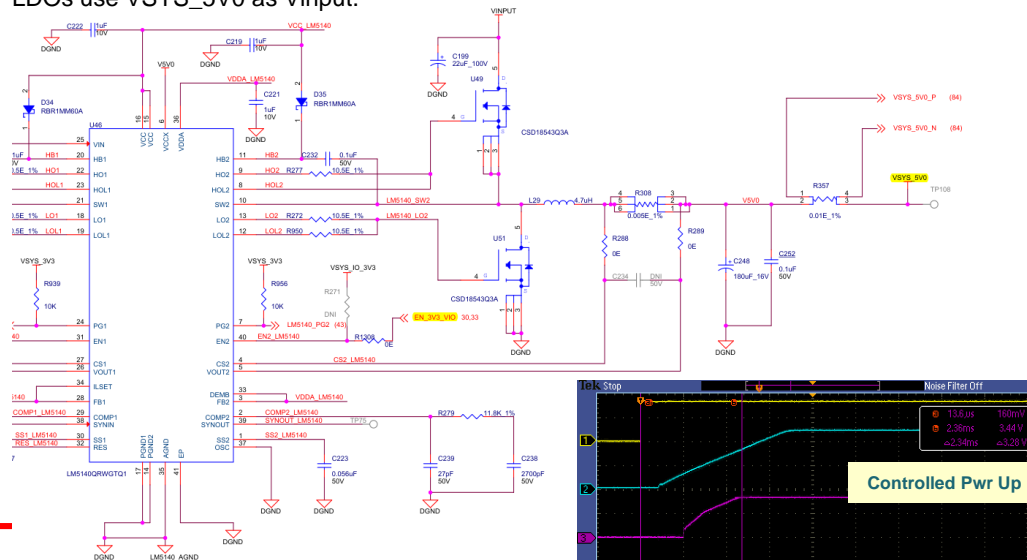
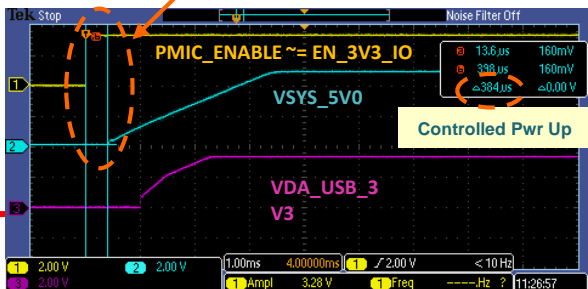
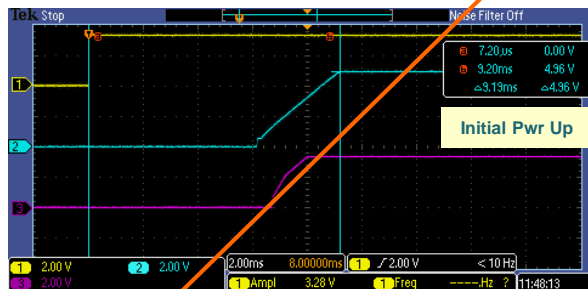
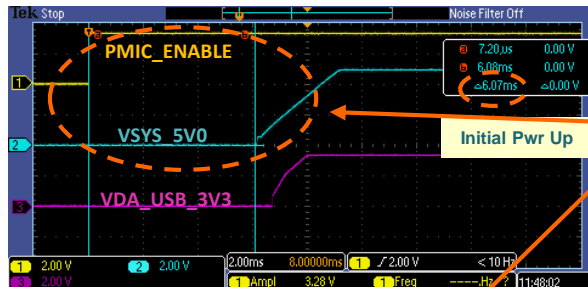
# EVM Item #2 | 5V Ramp Delay

VSYS\_5V0 1<sup>st</sup> stage is delayed until after PMIC is enabled by using 2<sup>nd</sup> stage EN\_3V3\_VIO signal (~0.1ms after PMIC\_ENABLE & 1<sup>st</sup> step in SoC pwr up seq) as enable input.

Resulting in 2x different time delays for enabling VSYS\_5V0 dependent on whether the EVM has experienced:

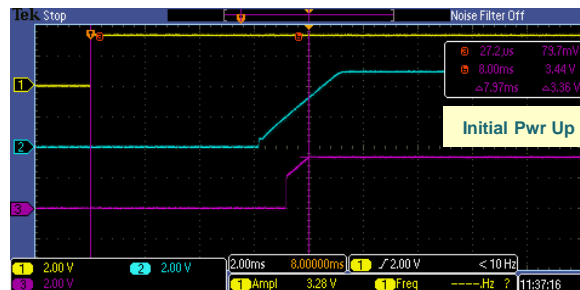
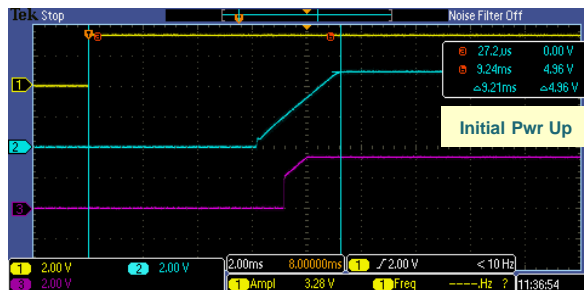
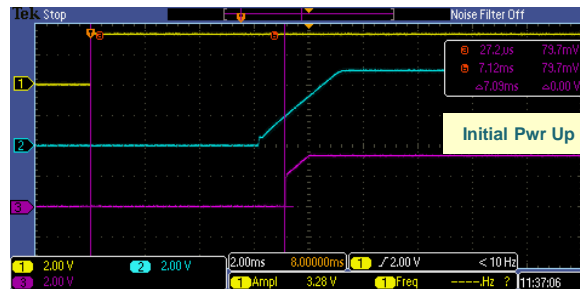
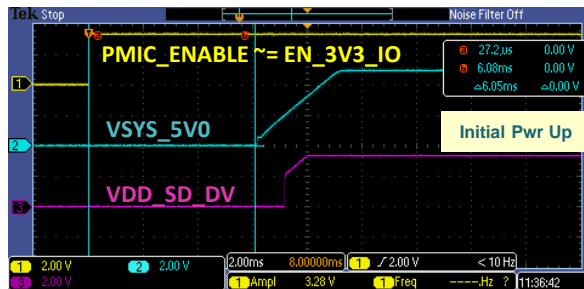
1. An Initial Power Up resulting in ~6.0ms delay due to PMIC's "Wait for Enable" state that occurs after PMIC\_ENABLE goes high & before EN\_3V3\_VIO goes high.
2. A Controlled Power Up resulting in ~0.4ms delay since PMIC has already pass through the "Wait for Enable" state after initial power up.

Additional, both VDA\_USB\_3V3 and VDD\_SD\_DV SoC power rail ramps are delayed since their LDOs use VSYS\_5V0 as Vinput.

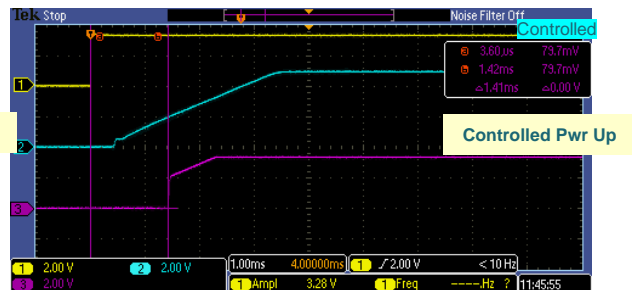
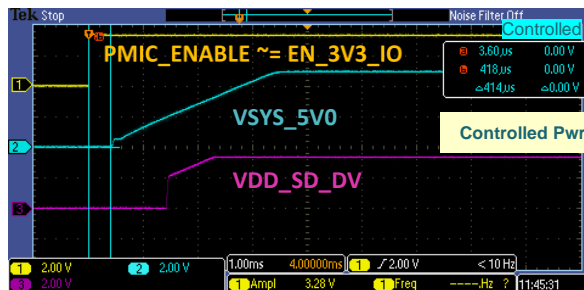




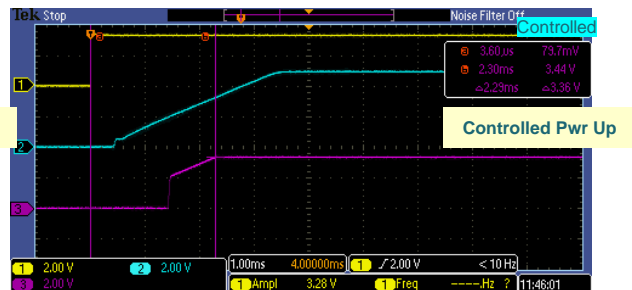
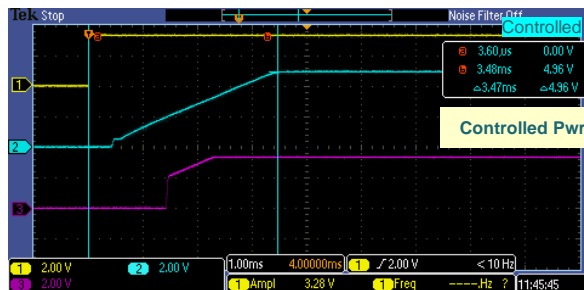
# EVM Item #2 | 5V Ramp Delay



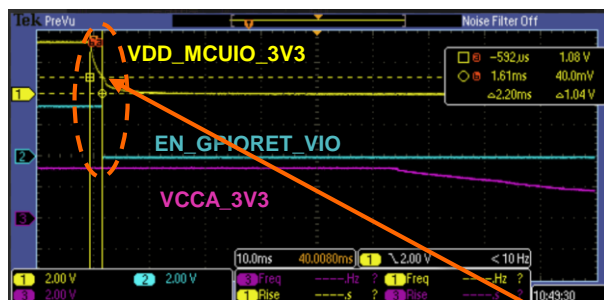
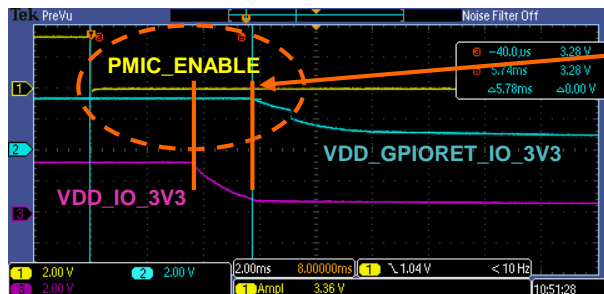
# EVM Item #2 | 5V Ramp Delay



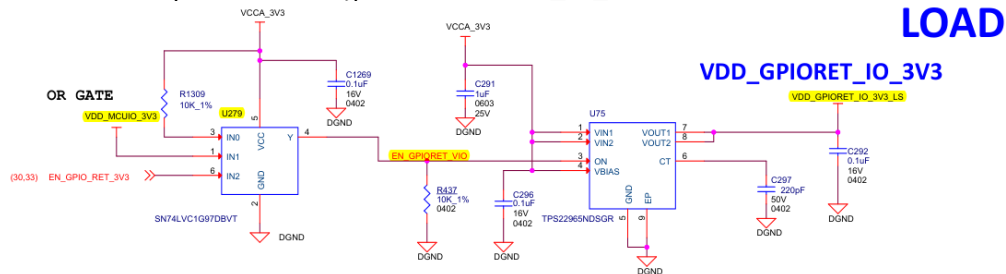
power cycled



# EVM Item #3 | GPIORET Disable Delay



VDD\_GPIORET\_IO\_3V3 disable is delayed by ~2ms from expected time alignment with VDD IO 3V3.



TEXAS  
INSTRUMENTS

SN74LVC1G97-Q1

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SCES561D - MARCH 2004 - REVISED APRIL 2008

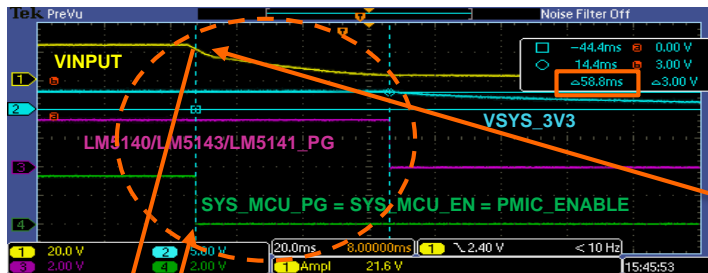
## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>TH</sub> Positive-going input threshold voltage		1.65 V	0.6		1.4	V
		2.3 V	1		1.8	
		3 V	1.3		2.2	
		4.5 V	1.9		3.1	
		5.5 V	2.2		3.6	
V <sub>TL</sub> Negative-going input threshold voltage		1.65 V	0.3		0.7	V
		2.3 V	0.5		1	
		3 V	0.7		1.4	
		4.5 V	1		2	
		5.5 V	1.2		2.3	

~2ms delay in disabling VDD\_GPIORET\_IO\_3V3 LDO is due to VDD\_MCUIO\_3V3 discharge time from 3.3 to ~1.1V, dropping below the OR gate's (U279) V<sub>TH</sub> (negative -going input threshold voltage) that ranges from 0.7 to 1.4V.

# EVM Item #4 | Input Power Loss Early Warning

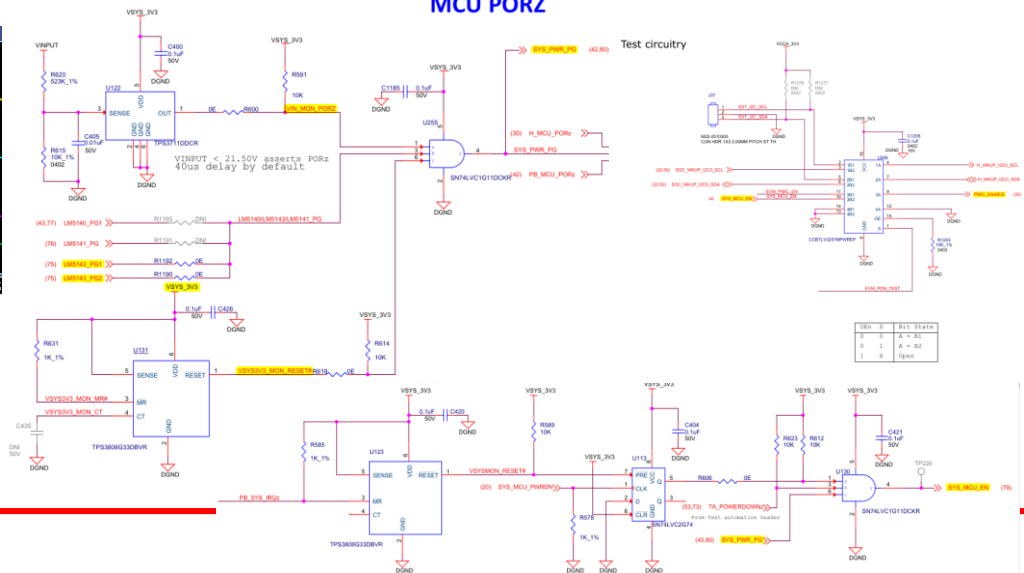
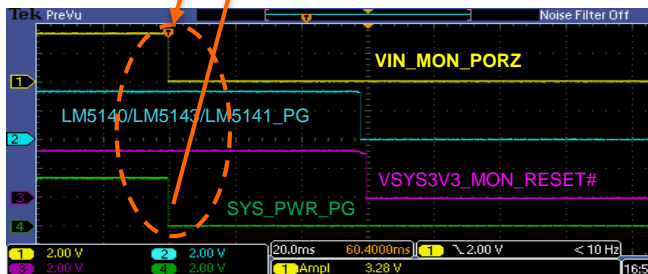


EVM uses a voltage supervisor IC (VMON, U122) to provide an “Input Power Loss Early Warning”. The VMON’s output (VIN\_MON\_PORZ) sets low when EVM’s VININPUT drops below ~21.5V. This results in PMIC\_ENABLE going low to begin SoC power down seq ~59ms before VSYS\_3V3 drops out of regulation & begins to discharge.

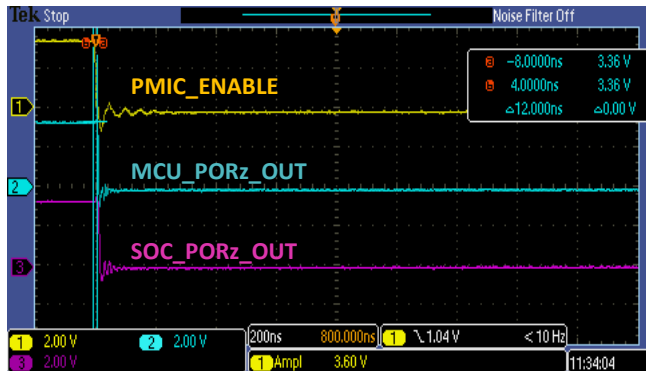
Input Power Loss Earlier Warning

Under Voltage Monitor (VININPUT)

MCU PORZ

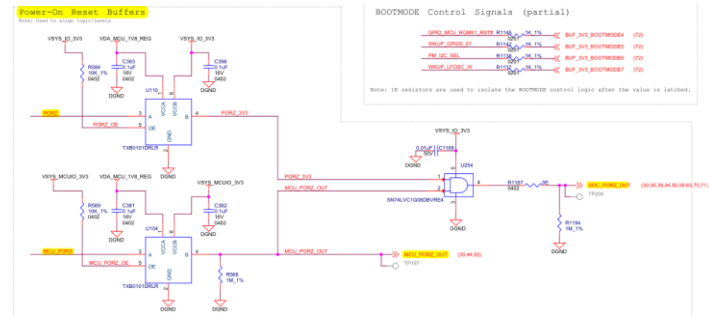


# EVM Item #4 | Input Power Loss Early Warning



RESET INPUTS

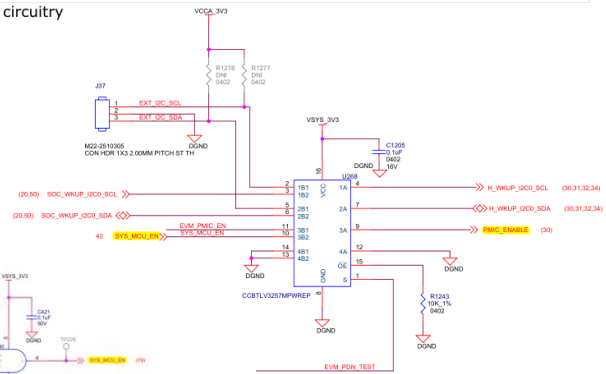
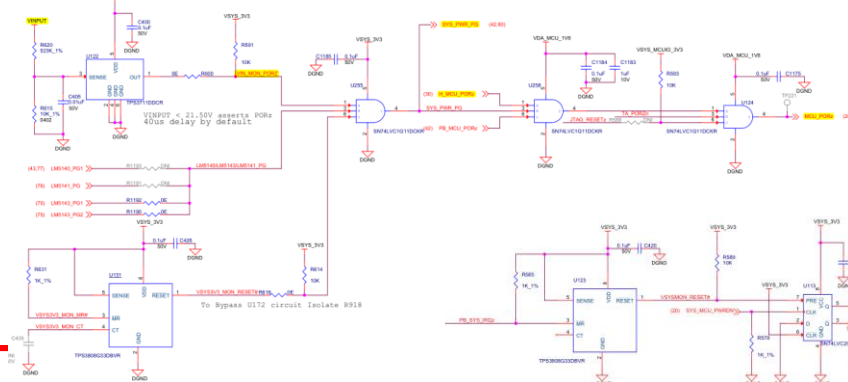
- Input power loss event will set MCU\_PORz\_OUT, SOC\_PORz\_OUT & PMIC\_ENABLE low immediately due to UV VMON (U122) responding to VININPUT voltage dropping below ~21.5V.



Test circuitry

Under Voltage Monitor (VINPUT)

MCU PORz



OE#	Bit State
0	A = B1
0	A = B2
1	Open

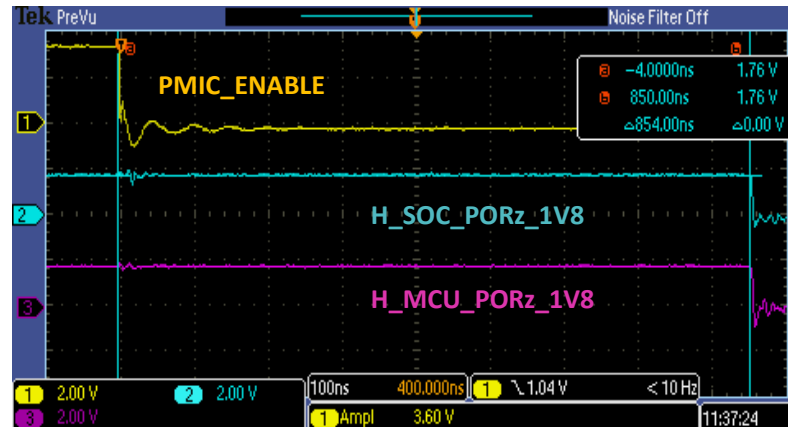
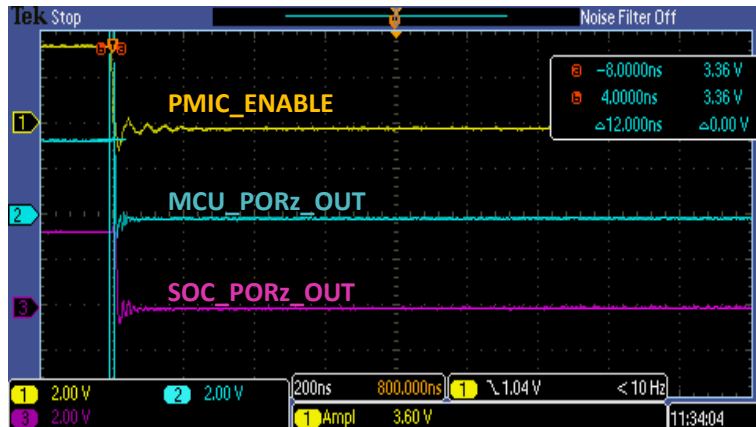
# EVM Item #4 | Input Power Loss Early Warning

- Input power loss event will set MCU\_PORz\_OUT, SOC\_PORz\_OUT & PMIC\_ENABLE low immediately due to UV VMON (U122) responding to VINUT voltage dropping below ~21.5V.
- PMIC outputs (shown below) will lag MCU\_PORz\_OUT, SOC\_PORz\_OUT & PMIC\_ENABLE due to PMIC's state machine ~0.1us delay before setting outputs low (shown below) as 1<sup>st</sup> step in pwr down seq.

PMIC Outputs = SCH Nets

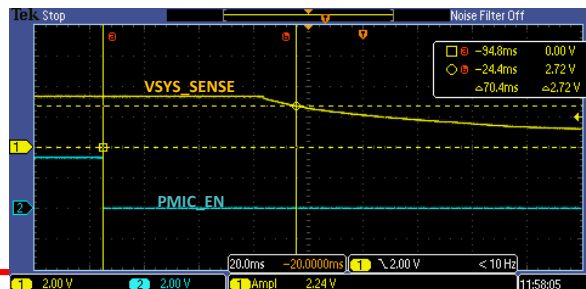
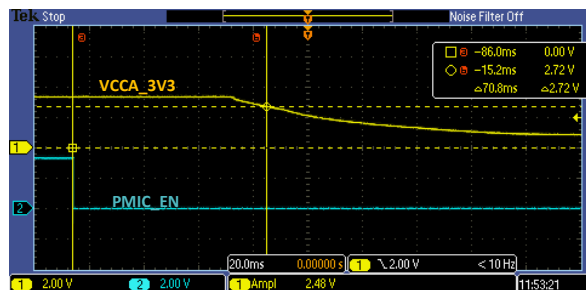
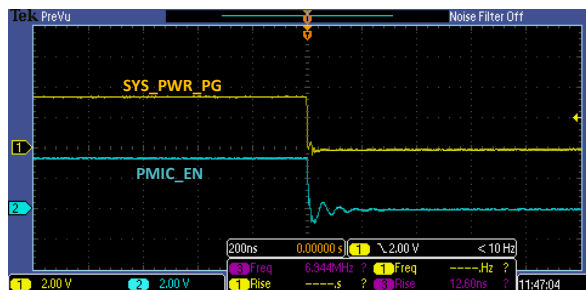
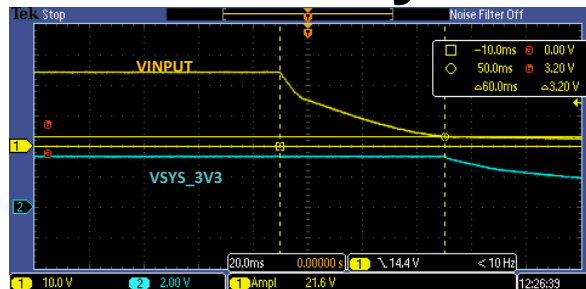
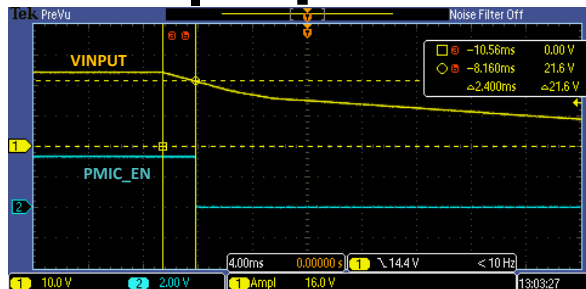
nRSTOUT = H\_MCU\_PORz\_1V8 and

GPIO\_11 = H\_SOC\_PORz\_1V8



# EVM Item #4 | Input Power Loss Early Warning

Additional timing details



# EVM Item #4 | Input Power Loss Early Warning

PMIC VRTC and VINT internal supplies with respect to PMIC\_EN

