

SK-AM68 Processor Starter Kit

Base Board

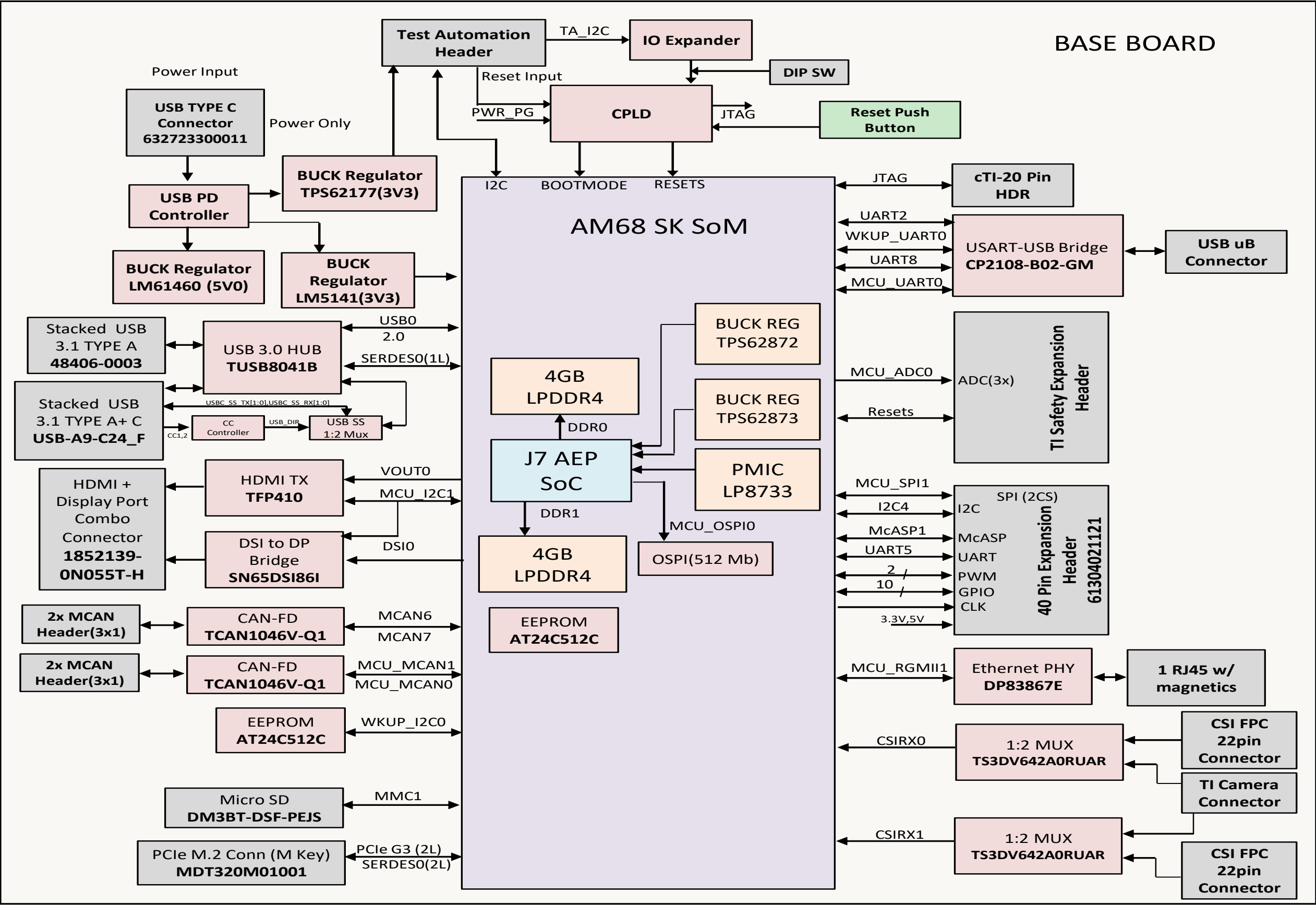
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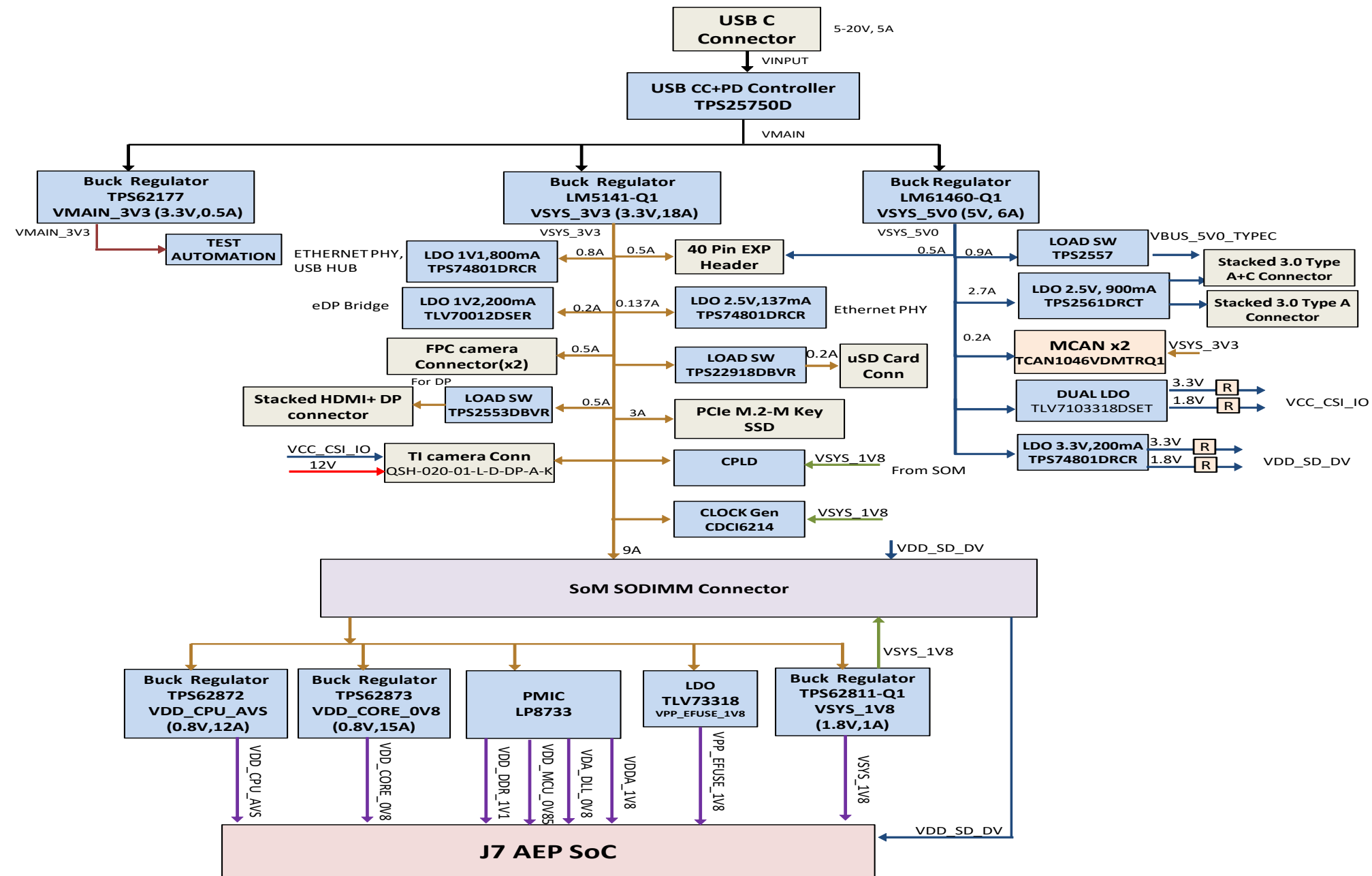
REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	16 SEP 2021	Initial Design	Mistral Design Team		
	26 OCT 2021	Updated Schematics	Mistral Design Team		
	28 OCT 2021	Updated schematics for TI review comments - Part1	Mistral Design Team		
	2 NOV 2021	Updated schematics for TI review comments - Part2	Mistral Design Team		
	9 NOV 2021	Updated for SoM changes(split the VSYS_3V3 Supply pins in the connector)	Mistral Design Team		
	16 NOV 2021	Updated for TI review comments	Mistral Design Team		
	18 NOV 2021	Added GPIO mapping table and power flow diagram Swapped CSI, HDMI signals on DIMM connector for routing ease om SoM	Mistral Design Team		
	24 NOV 2021	Changed connector pinouts on DIMM connector for routing ease on SoM board Swapped USB load switch outputs to connectors for routing ease Moved VSYS_IO_3V3 current monitor to base board	Mistral Design Team		
	25 NOV 2021	Swapped PCIe and USB signals on DIMM connector for routing ease on SoM	Mistral Design Team		
	26 NOV 2021	Changed CPLD part to XC2C64A-7VQG44C	Mistral Design Team		
	30 NOV 2021	Replaced VSYS_IO_3V3 by VSYS_3V3 and removed VSYS_IO_3V3/VSYS_3V3 current monitor circuitry	Mistral Design Team		
	1 AUG 2022	Updated VSYS_3V3 for 20A current requirement Added buffer for DP0_HPD Updated DSI to eDP section as per latest AEP SOM Changed J10 to Type A+C connector Added second RPI 4L camera connector and updated CSI section	Mistral Design Team		
	11 AUG 2022	Updated for TI review comments Updated CPLD section and added fuse for fan	Mistral Design Team		
	16 AUG 2022	Updated RPi pinouts Changed 5V fuse part number to 0ZCJ0025AF2E	Mistral Design Team		
	17 AUG 2022	Updated DIMM connector connections for changes on SOM for MCU_SPI signals	Mistral Design Team		
	29 AUG 2022	Updated block diagrams	Mistral Design Team		
	01 SEP 2022	Changed LD3 supply to VSYS_3V3 Changed 100uF electrolytic caps to 22uF ceramic caps fpr VSYS_3V3 input in order to reduce the height Changed L15 to SRP1238A-1R2M & L16 to XAL7030-562MEC	Mistral Design Team		
	07 SEP 2022	Added mechanicals for SOM board maying Updated R201 pull up supply R201	Mistral Design Team		
	09 SEP 2022	Added decaps for VSYS_3V3 rail	Mistral Design Team		
	19 SEP 2022	DNI'd resistor R3757 to support 1.5A current for USB type C	Mistral Design Team		

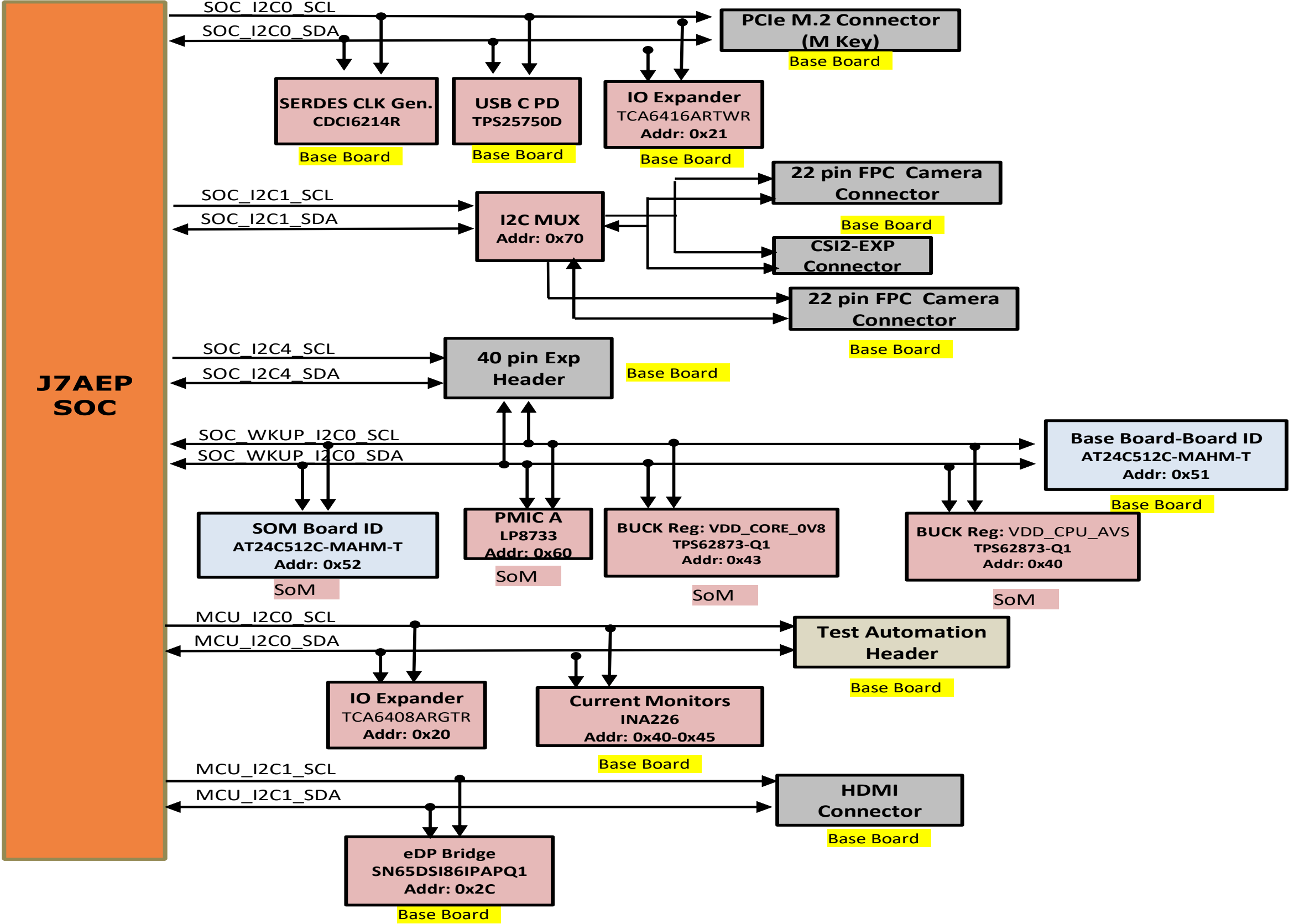
SYSTEM BLOCK DIAGRAM



POWER FLOW DIAGRAM



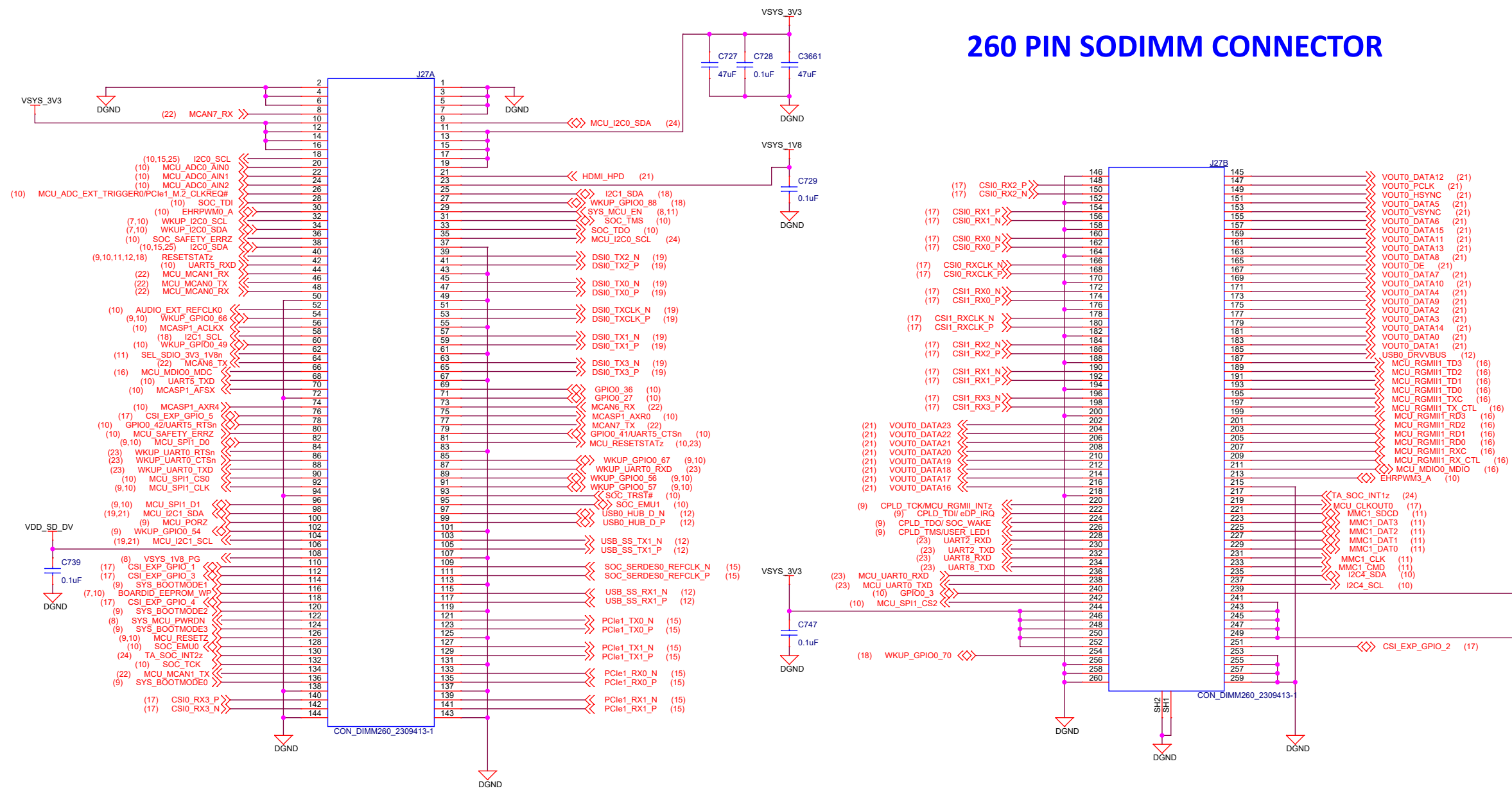
I2C TREE



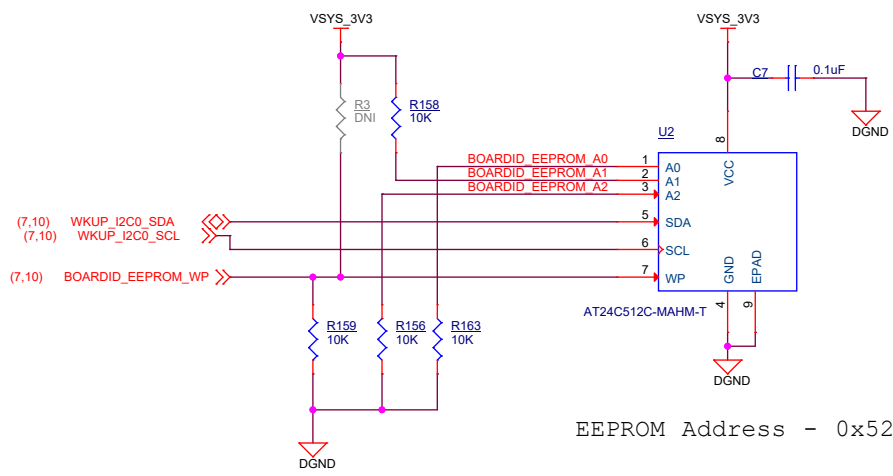
GPIO MAPPING TABLE

J7x SoM - GPIO Mapping Table						
WKUP Domain						
J7AEP Mapping		Net name	Input/ Output	Default	State	Remarks
Package Signal Name	GPIO Number					
MCU_OSPIO_CSn1	WKUP_GPIO0_28	EN_EFUSE_VPP	Output	PU	Active High	Enable pin for VPP_EFUSE supply
MCU_OSPIO_CSN2	WKUP_GPIO0_29	CPLD_TMS/USER_LED1	Output	NA	NA	JTAG signals for CPLD & USER LED enable signal. 1:2 Mux on base board
MCU_OSPI1_CLK	WKUP_GPIO0_31	CPLD_TCK/MCU_RGMII_INTz	Input	PD	NA	JTAG signals for CPLD & MCU_RGMII_INT signal. 1:2 Mux on base board
MCU_OSPI1_CSN0	WKUP_GPIO0_38	CSI_EXP_GPIO_4	I/O	NA	NA	GPIO Signals for CSI expansion connector
MCU_OSPI1_CSN1	WKUP_GPIO0_39	PMIC_INTN_1V8	Input	PU	Active low	Interrupt signal from PMIC
MCU_OSPI1_D0	WKUP_GPIO0_34	CPLD_TDI/ eDP_IRQ	Input	NA	NA	JTAG signals for CPLD & Interrupt signal from eDP bridge. 1:2 Mux on base board
MCU_OSPI1_D1	WKUP_GPIO0_35	CSI_EXP_GPIO_5	I/O	NA	NA	GPIO Signals for CSI expansion connector
MCU_OSPI1_D2	WKUP_GPIO0_36	CSI_EXP_GPIO_2	I/O	NA	NA	GPIO Signals for CSI expansion connector
MCU_OSPI1_D3	WKUP_GPIO0_37	CSI_EXP_GPIO_3	I/O	NA	NA	GPIO Signals for CSI expansion connector
MCU_OSPI1_DQS	WKUP_GPIO0_33	CPLD_TDO/ SOC_WAKE	Output	NA	NA	JTAG signals for CPLD
MCU_OSPI1_LBCLKO	WKUP_GPIO0_32	CSI_EXP_GPIO_1	I/O	NA	NA	GPIO Signals for CSI expansion connector
MCU_SPI0_CLK	WKUP_GPIO0_54	WKUP_GPIO0_54	Output	BOOTMODE	Active low	CPLD_JTAG/GPIOOn_SEL. Mux select signal for CPLD JTAG and GPIO's
MCU_SPI0_CS0	WKUP_GPIO0_70	WKUP_GPIO0_70	I/O	BOOTMODE	NA	FPC Camera GPIO signals
MCU_SPI0_D1	WKUP_GPIO0_69	SYS_MCU_PWRDN	Output	BOOTMODE	Active High	System Power Down ('0' - normal operation, '1' - system power down)
WKUP_GPIO0_10	WKUP_GPIO0_10	MCU_ADC_EXT_TRIGGER0/PCIE_1_M.2_CLKREQ#				ADC external trigger from TI safety header(Default connection)/CLKREQ#
WKUP_GPIO0_11	WKUP_GPIO0_11	MCU_CLKOUT0	Output	NA	NA	25MHz reference clock for CSI expansion connector
WKUP_GPIO0_15	WKUP_GPIO0_15	MCU_SPI1_CS2	Output	BOOTMODE	Active low	MCU SPI1 signals
WKUP_GPIO0_49	WKUP_GPIO0_49	WKUP_GPIO0_49	I/O	NA	NA	GPIO signal for 40 pin expansion header
WKUP_GPIO0_57	WKUP_GPIO0_57	WKUP_GPIO0_57	I/O	BOOTMODE	NA	GPIO signal for 40 pin expansion header
WKUP_GPIO0_56	WKUP_GPIO0_56	WKUP_GPIO0_56	I/O	BOOTMODE	NA	GPIO signal for 40 pin expansion header
WKUP_GPIO0_66	WKUP_GPIO0_66	WKUP_GPIO0_66	I/O	BOOTMODE	NA	GPIO signal for 40 pin expansion header
WKUP_GPIO0_67	WKUP_GPIO0_67	WKUP_GPIO0_67	I/O	BOOTMODE	NA	GPIO signal for 40 pin expansion header
PMIC_POWER_EN1	WKUP_GPIO0_88	WKUP_GPIO0_88	I/O	NA	NA	FPC Camera GPIO signals
MCU_ADC1_AIN0	WKUP_GPIO0_79	SOC_INT1z	Input	PU	Active low	Test automation INT signal
MCU_ADC1_AIN1	WKUP_GPIO0_80	SOC_INT2z	Input	PU	Active low	Test automation INT signal
Main Domain						
ECAPO_IN_APWM_OUT	GPIO0_49	SEL_SDIO_3v3_1v8n	Output	PU	Active low	VDD_SD_DV 1.8V or 3.3V selection control
TIMER_IO0	GPIO0_58	MMC1_SDCD	Input	PU	Active low	SD card detect signal
TIMER_IO1	GPIO0_59	USB0_DRVVBUS	Output	NA	Active High	USB VBUS Drive signal
EXTINTN	GPIO0_0	HDMI_HPD	Input	NA	Active High	HDMI hot plug detect signal
MCAN1_TX	GPIO0_27	GPIO0_27	I/O	NA	NA	GPIO signal for 40 pin expansion header
MCAN13_TX	GPIO0_3	GPIO0_3	I/O	NA	NA	GPIO signal for 40 pin expansion header
MCASPO_AXR8	GPIO0_36	GPIO0_36	I/O	NA	NA	GPIO signal for 40 pin expansion header
MCASPO_AXR13	GPIO0_41	GPIO0_41/UART5_CTSn	I/O	NA	NA	GPIO signal for 40 pin expansion header/ UART5_CTS Signal
MCASPO_AXR14	GPIO0_42	GPIO0_42/UART5_RTSn	I/O	NA	NA	GPIO signal for 40 pin expansion header/ UART5_RTS Signal
GPIO Expander on Base Board						
Port NO		I2C Instance	Input/O utput	Default	State	Usage
P00	CSI_VIO_SEL	I2C0 ADDR: 0x21	Output	PD	Active High	Enable for VCC_CSI_IO supply generation load switch
P01	CSI_SEL_FPC_EXPn		Output	PD	Active High	CSI MUX selection
P02	HDMI_PDn		Output	PD	Active Low	Power down signal for HDMI Transmitter
P03	HDMI_LS_OE		Output	PU	Active High	HDMI current limit load switch enable
P04	DP0_3V3_EN		Output	PD	Active High	Enable signal for Display port load switch
P05	BOARDID_EEPROM_WP		Output	PD	Active High	Board id Eeprom Write protect signal
P06	CAN_STB		Output	PD	Active High	Standby signals for MAIN & MCU domain
P10	GPIO_uSD_PWR_EN		Output	PU	Active High	CAN Transceivers
P11	eDP_ENABLE		Output	PU	Active High	Micro SD card Load switch enable
P12	IO_EXP_PCIE1_M.2_RTSz		Output	PD	Active High	Used for Enable of DSI to eDP Bridge
P13	IO_EXP_MCU_RGMII_RST#		Output	NA	Active Low	PCIe Reset input to CPLD
P14	IO_EXP_CSI2_EXP_RSTz		Output	NA	Active Low	MCU_RGMII reest input to CPLD
P16	CSI0_B_GPIO1		Output	PD	Active Low	CSI expansion connector reset
P17	CSI1_B_GPIO1		Output	NA	NA	FPC Camera1 GPIO signal
			Output	NA	NA	FPC Camera2 GPIO signal

260 PIN SODIMM CONNECTOR

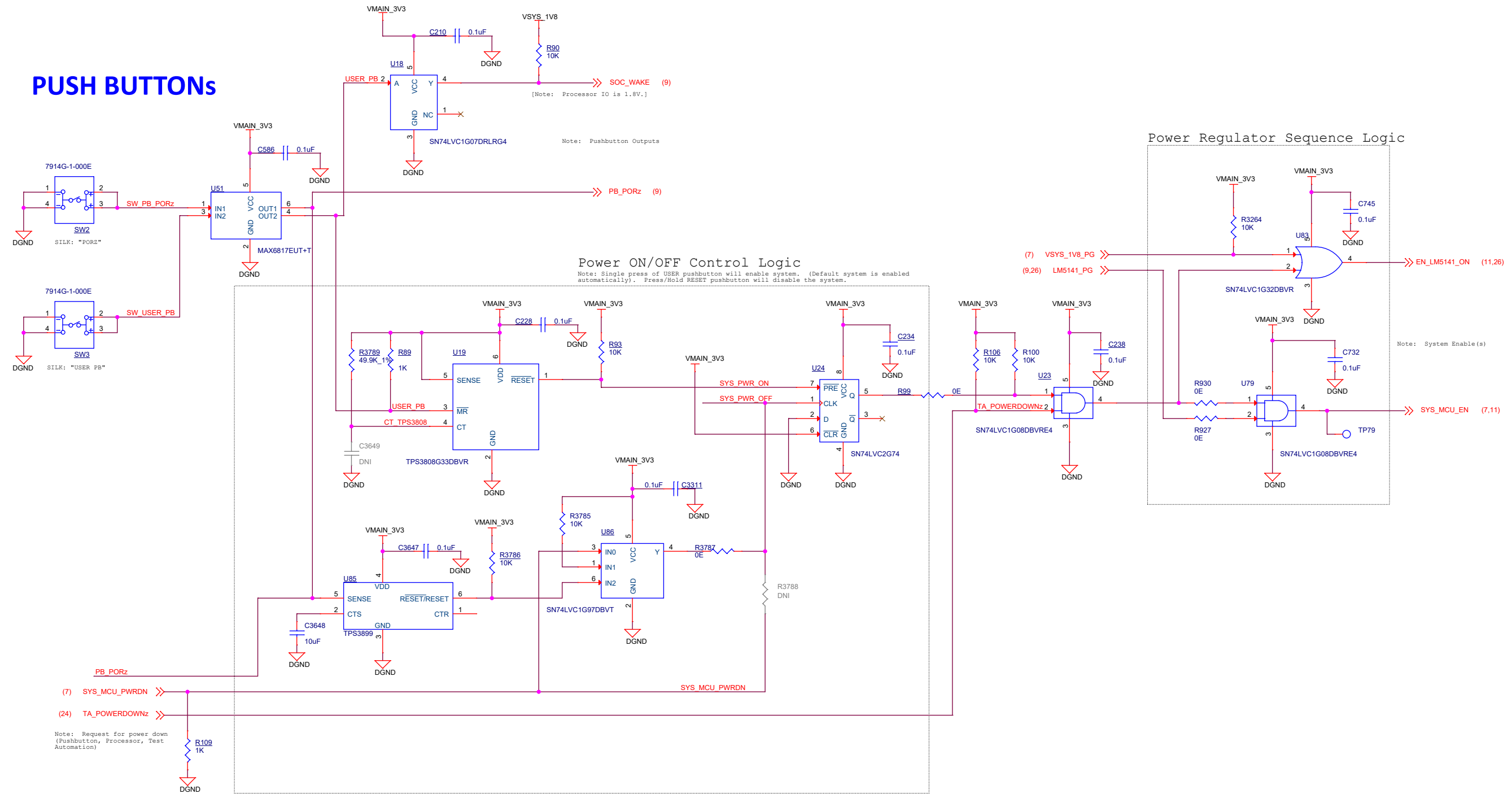


BOARD ID/CONFIG EEPROM



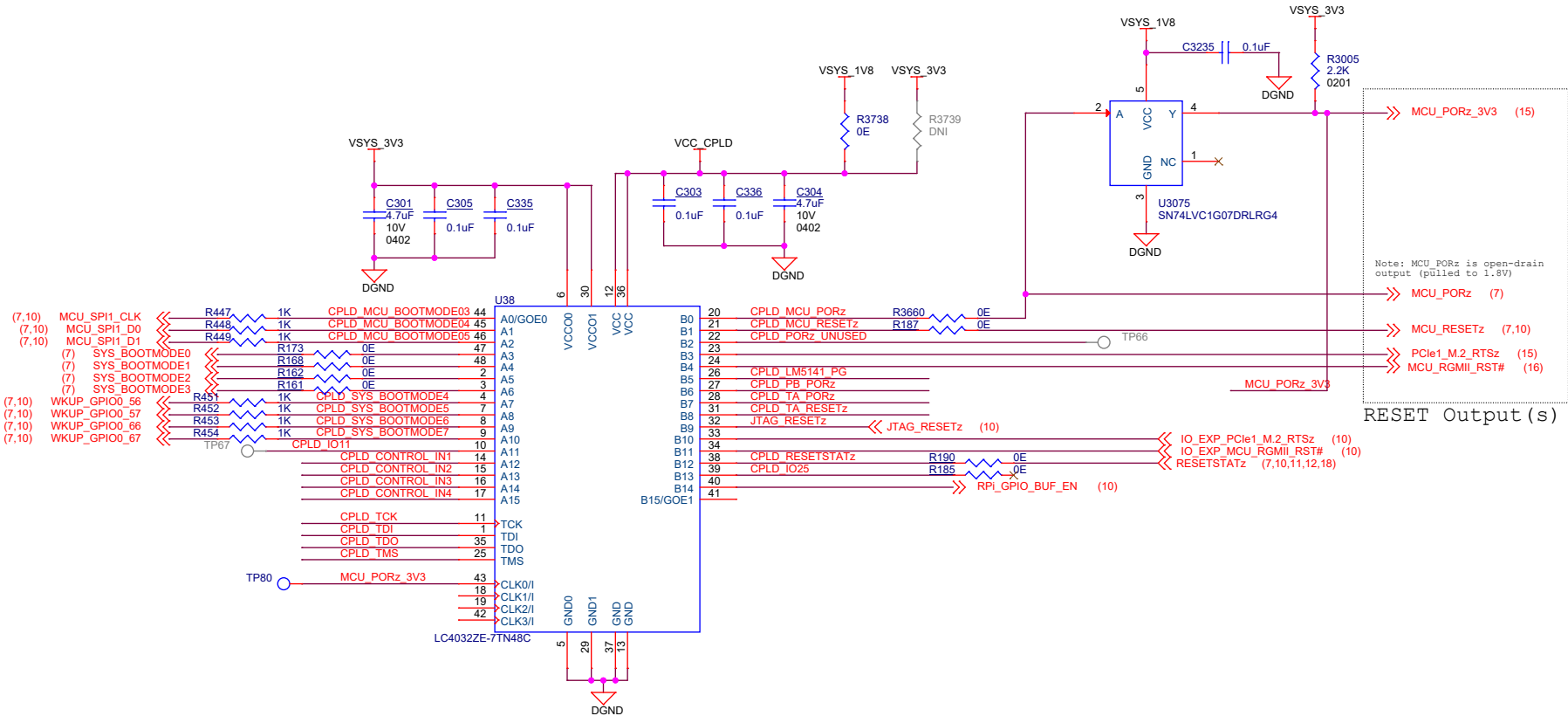
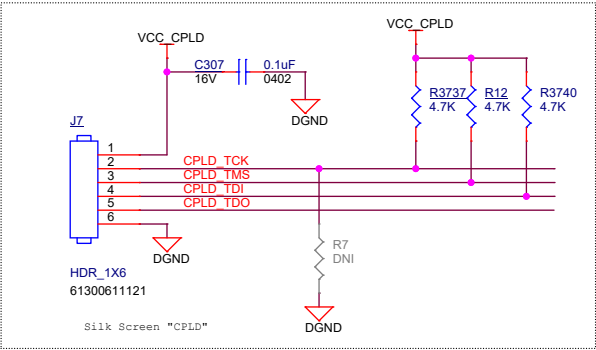
Project : TDA4VM Edge AI Kit		Title: SOM SODIMM CONN	
Date: Monday, September 19, 2022		Size: C	Rev: E1
Sheet 7 of 29		Date: Monday, September 19, 2022	

PUSH BUTTONs

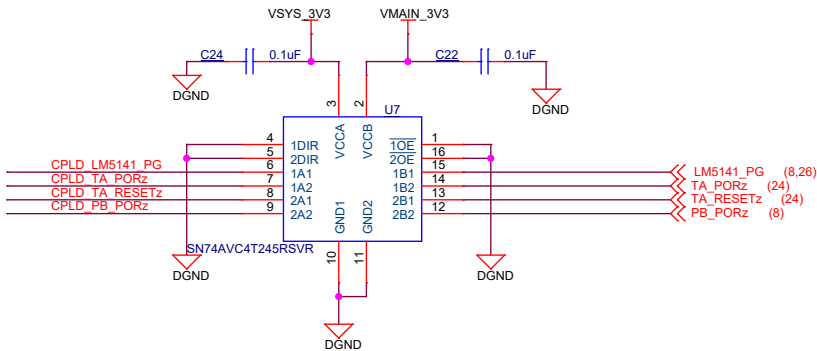
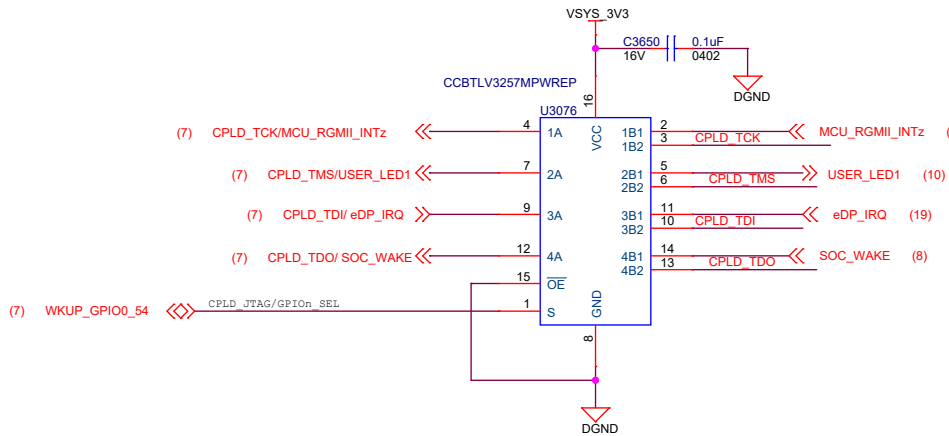


RESET/BOOTMODE LOGIC

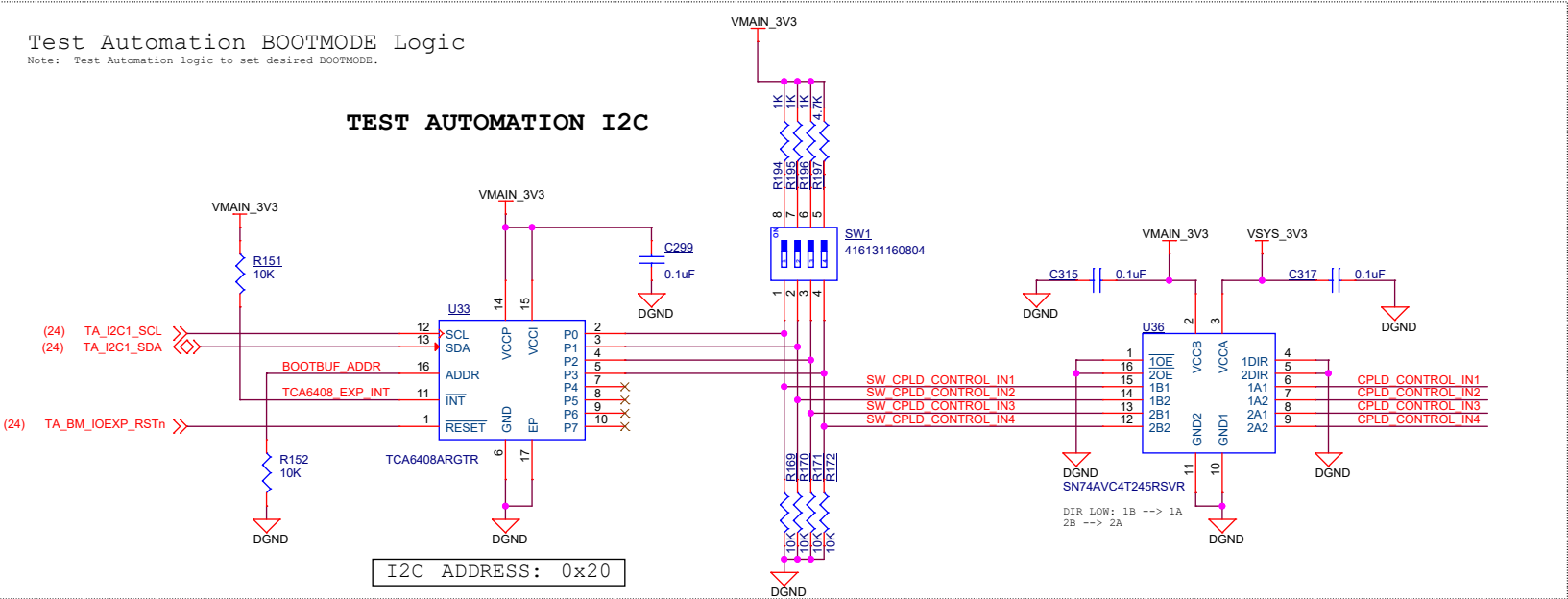
CPLD Programming Header



RESET Output (s)



Note: Isolation Logic Between Power Domain(s)

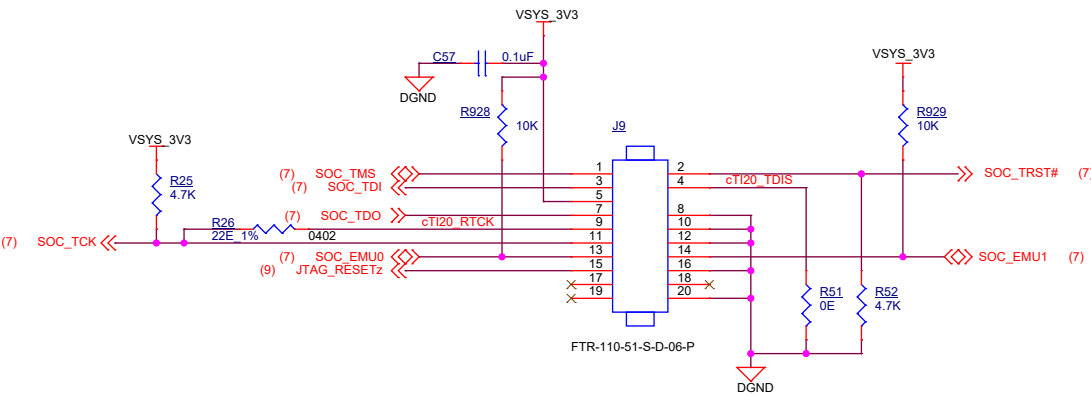


BOOTMODE SETTING

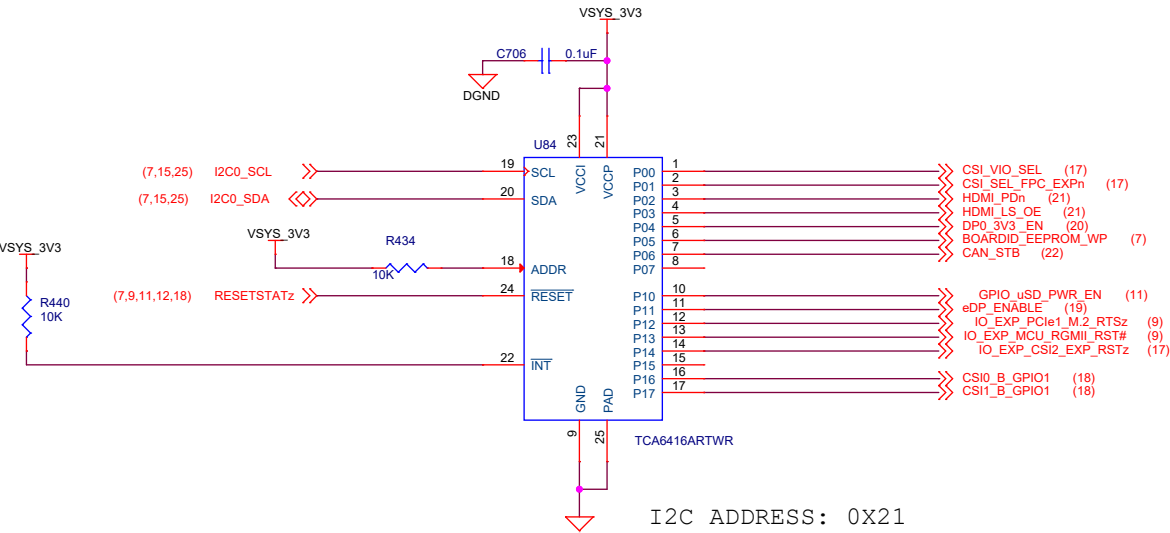
Bootmode is set using Dip Switch [SW1].

SW1.3	SW1.2	SW1.1	BOOTMODE
0	0	0	SD
0	0	1	NO Boot
0	1	0	ETHERNET
1	0	0	xSPI - 1S
1	0	1	UART
1	1	0	PCIE
1	1	1	xSPI SFDP

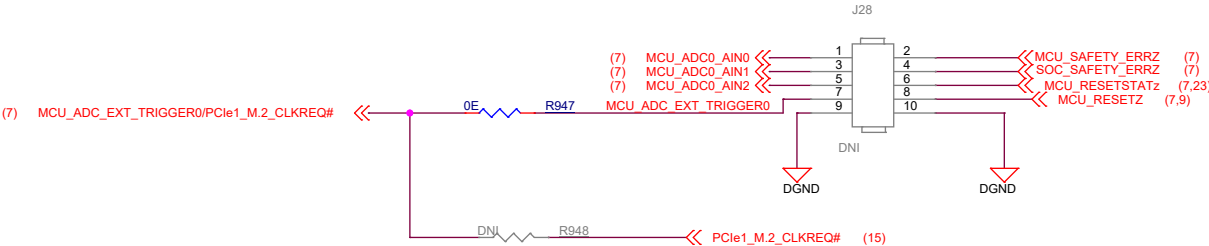
JTAG INTERFACE (cTI 20-PIN)



I2C IO EXPANDER

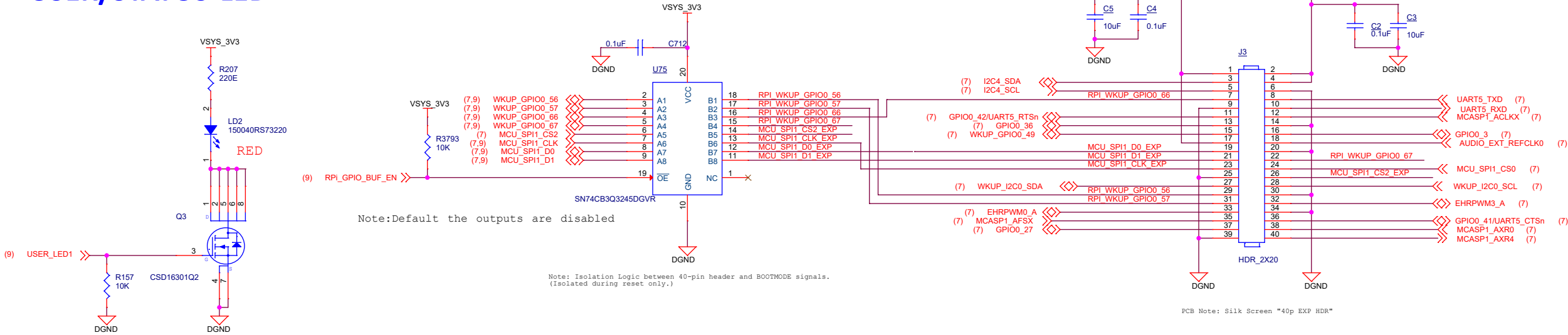


SAFETY STATUS INTERFACE

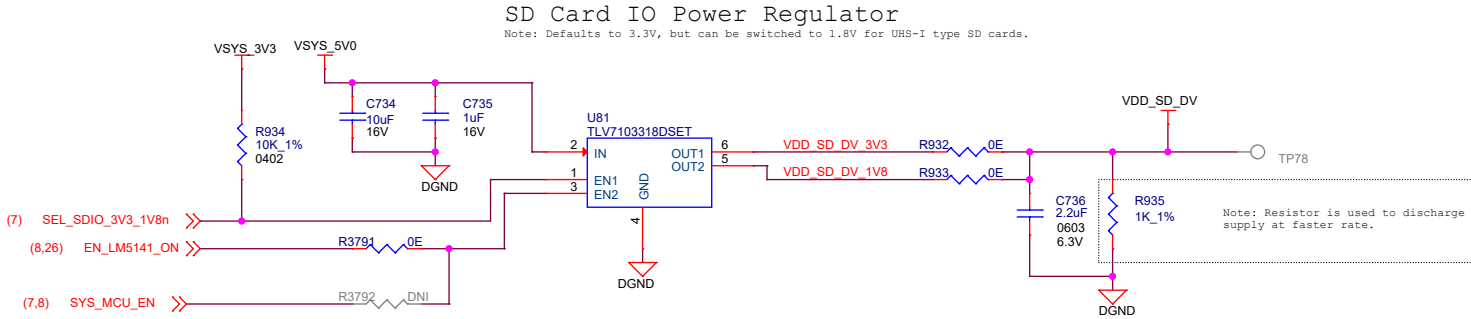
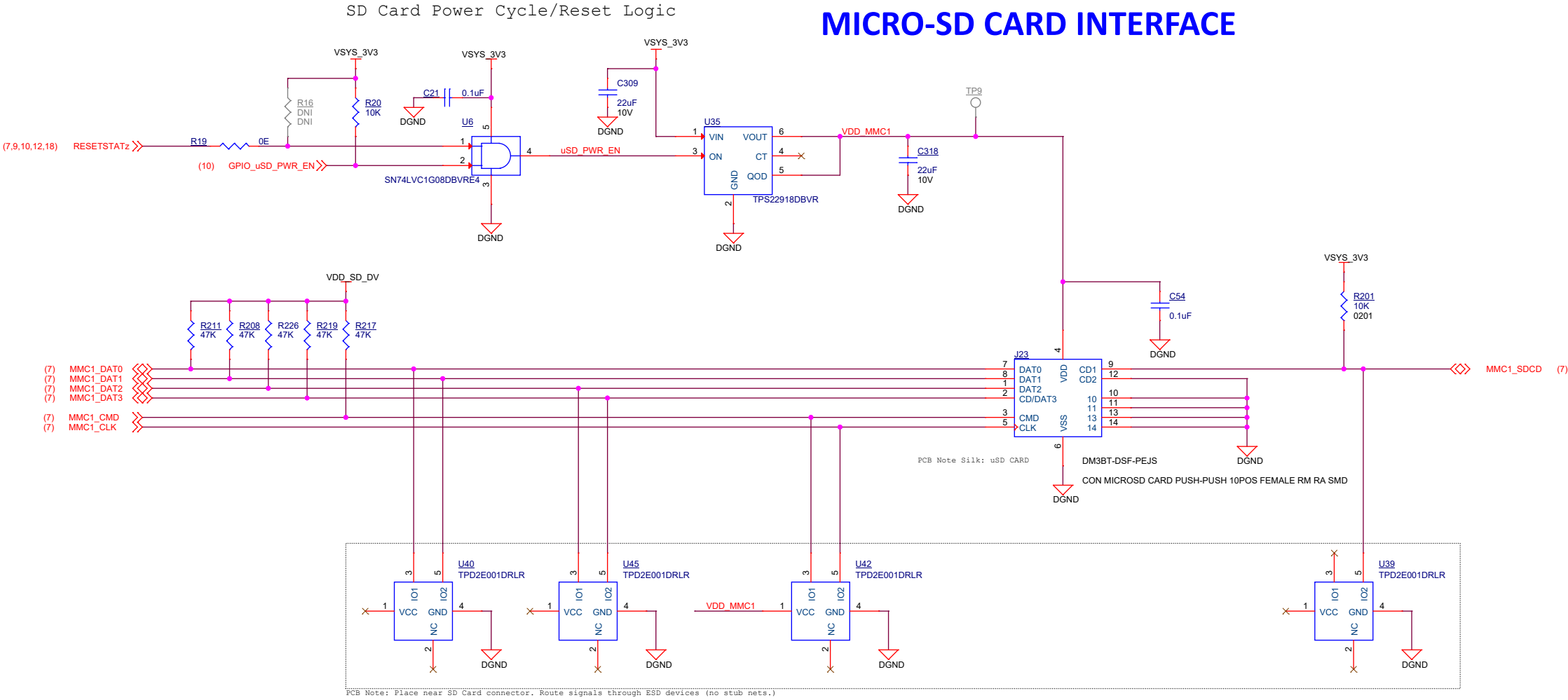


40PIN EXPANSION INTERFACE

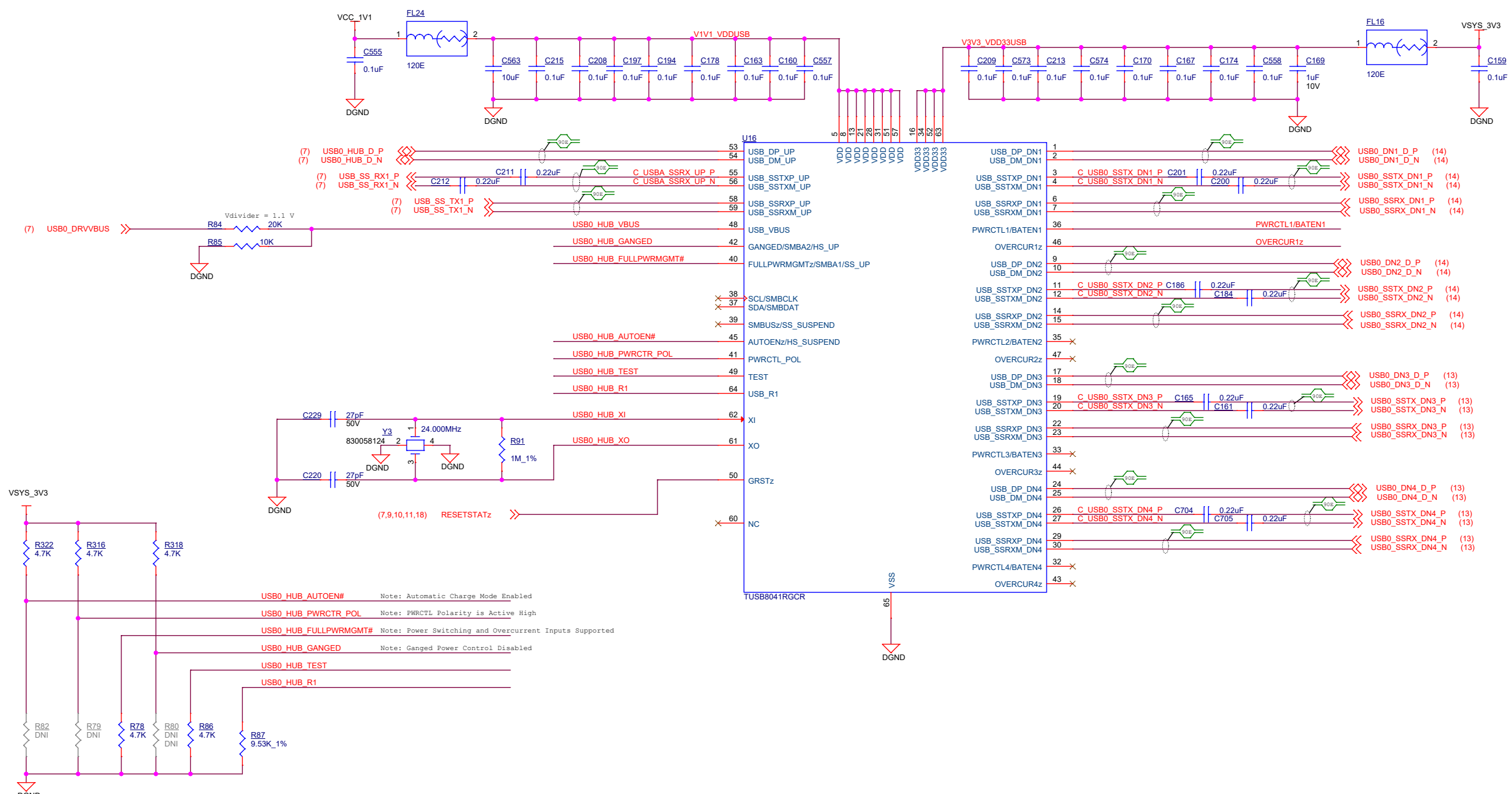
USER/STATUS LED



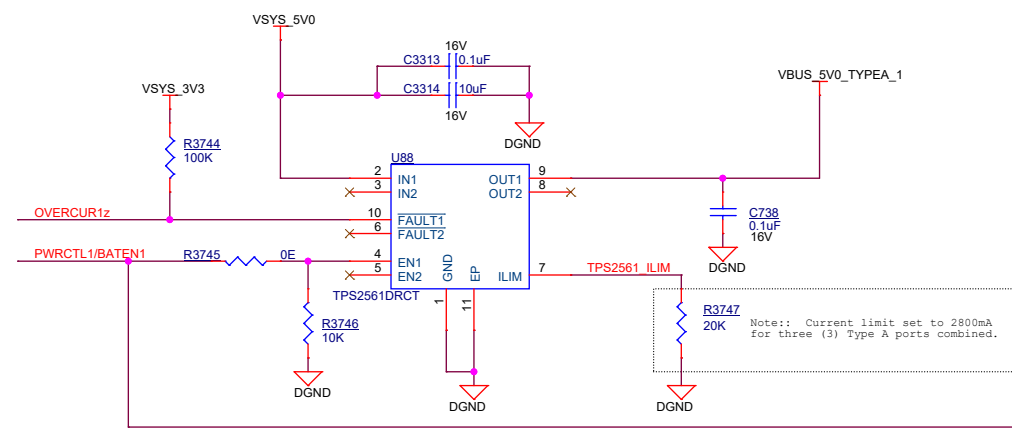
MICRO-SD CARD INTERFACE



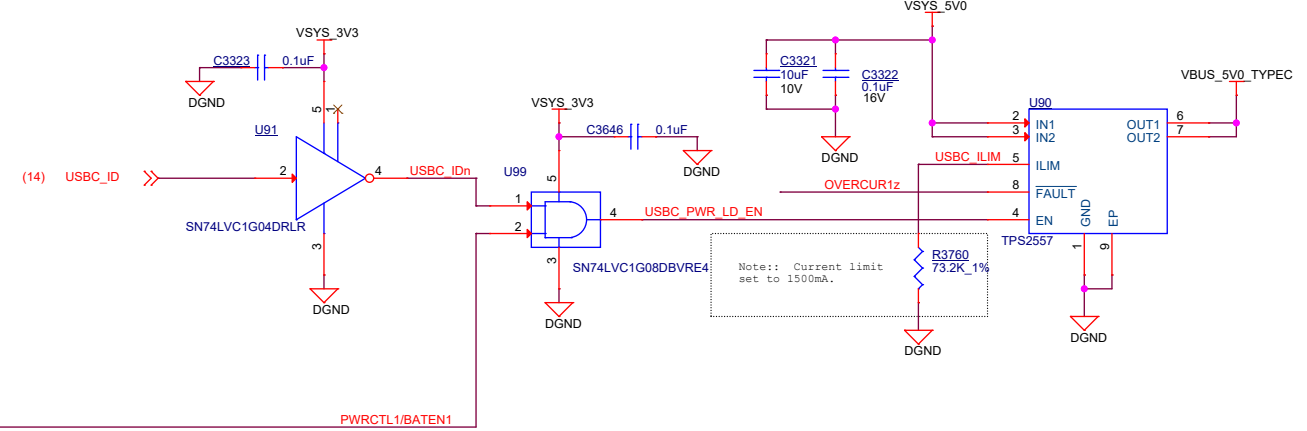
USB3.0 SS HUB



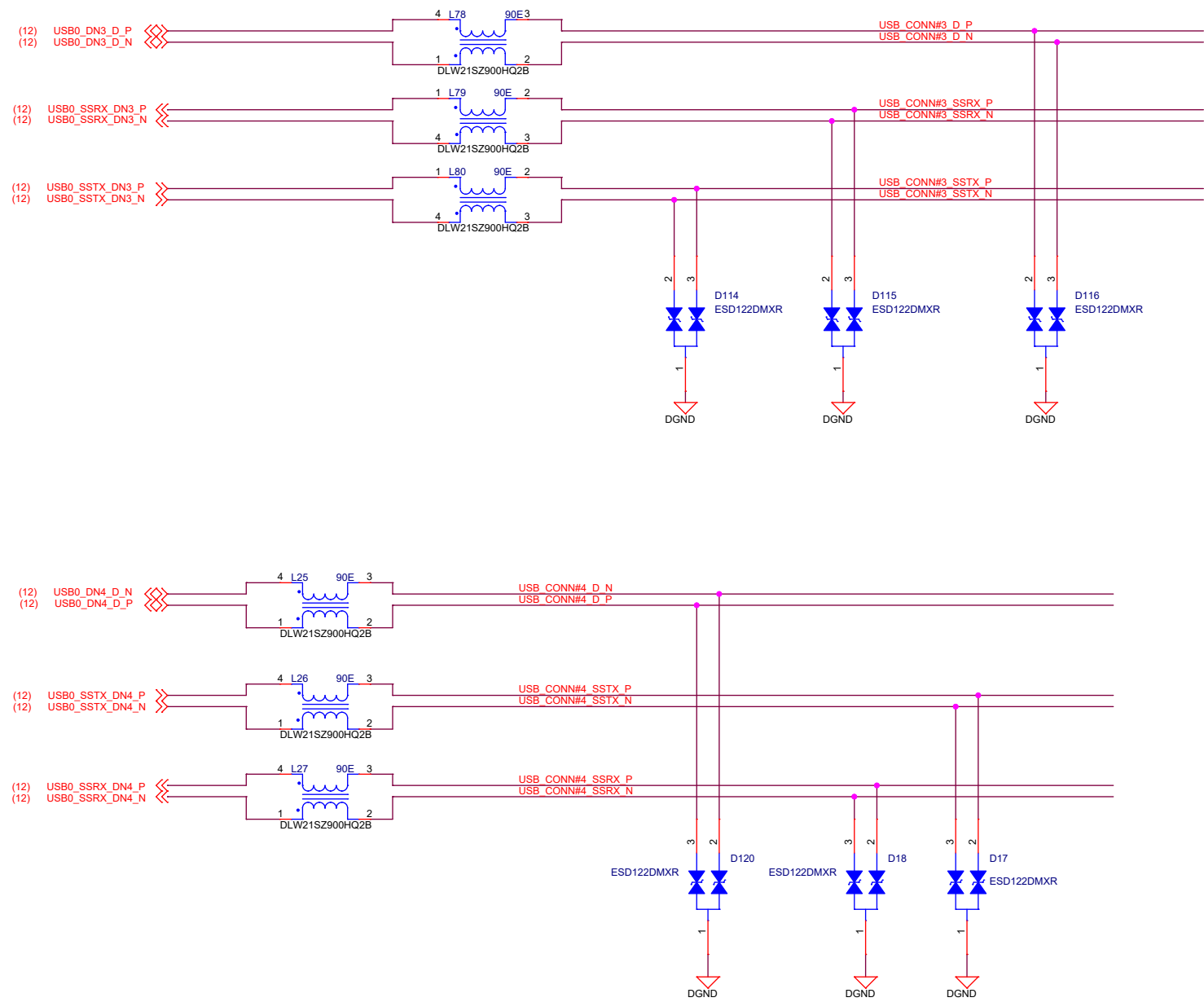
VBUS Power Control Logic Type A



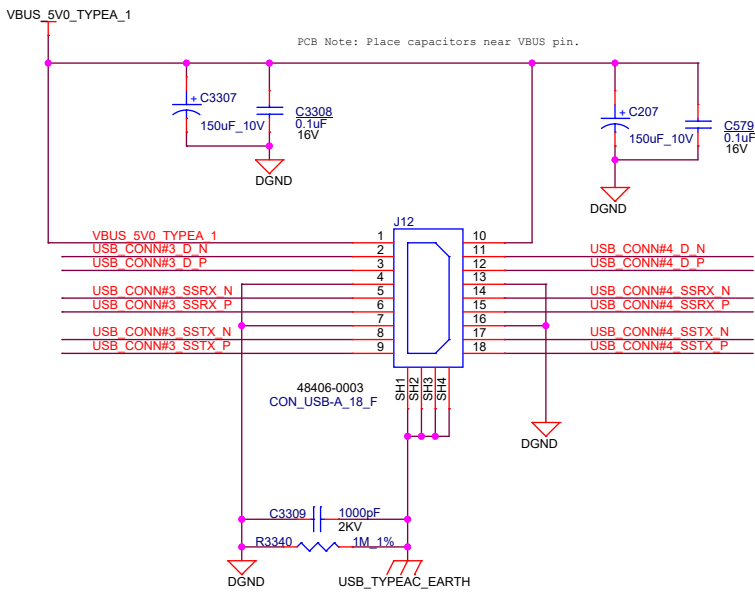
VBUS Power Control Logic Type C



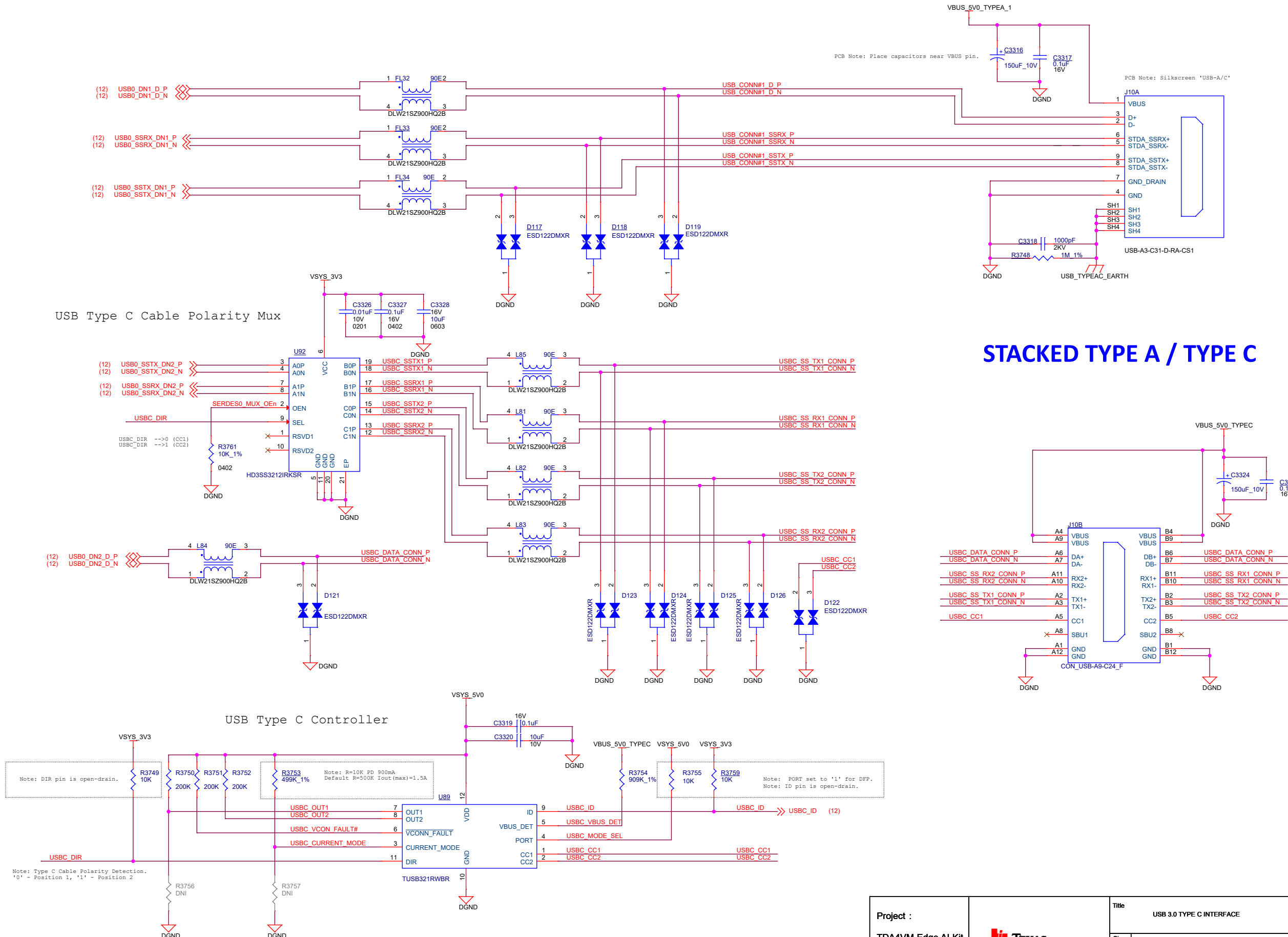
USB 3.0 SS INTERFACE (Port 3, 4)



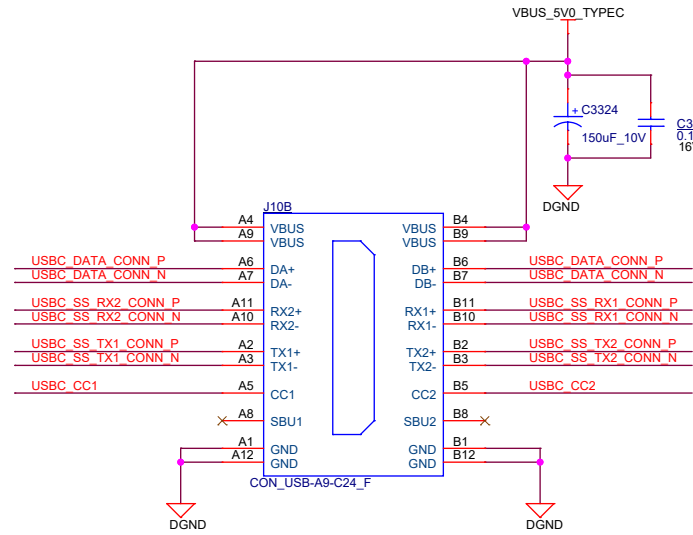
STACKED TYPE A / TYPE A




USB 3.0 SS INTERFACE (Port 1, 2)



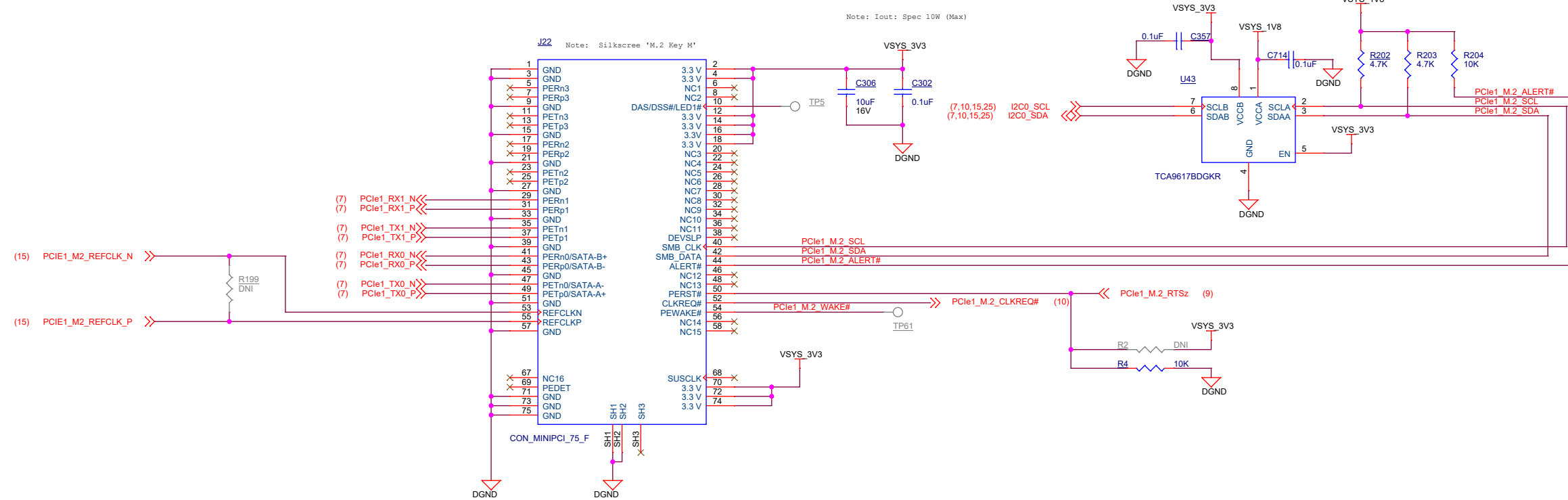
STACKED TYPE A / TYPE C



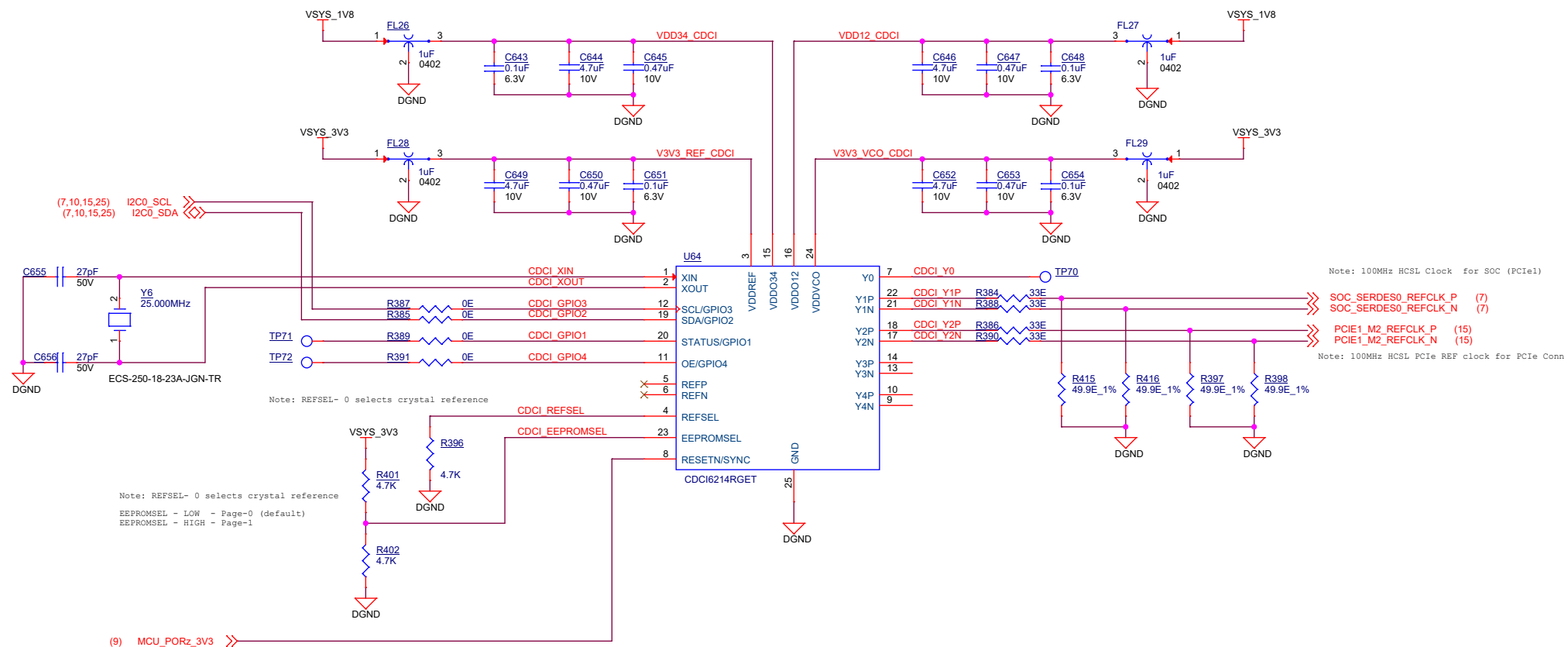
Project :	 TEXAS INSTRUMENTS	Title USB 3.0 TYPE C INTERFACE		
TDA4VM Edge AI Kit		Size	PROC125 001 AM68 SK	Rev
		C		B
		Date:	Monday, September 26, 2022	Sheet 14 of 29

PCIe M.2 KEY-M INTERFACE

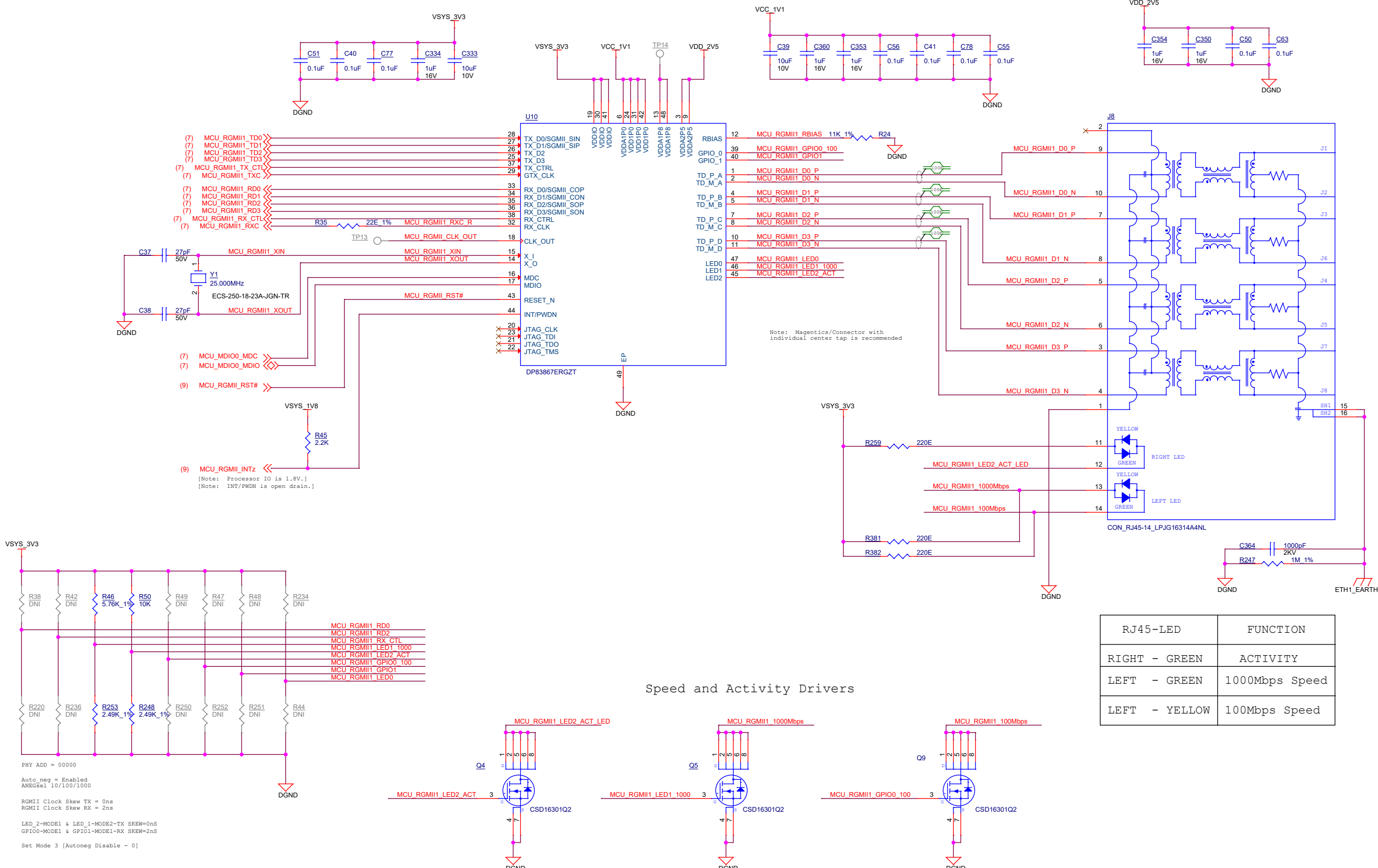
3.3V to 1.8V Level Translator



PCIe Reference Clock Generator

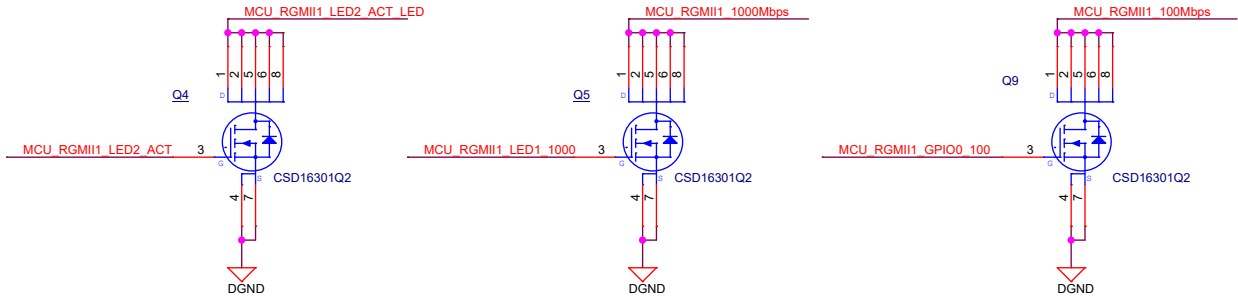


GIGABIT ETHERNET



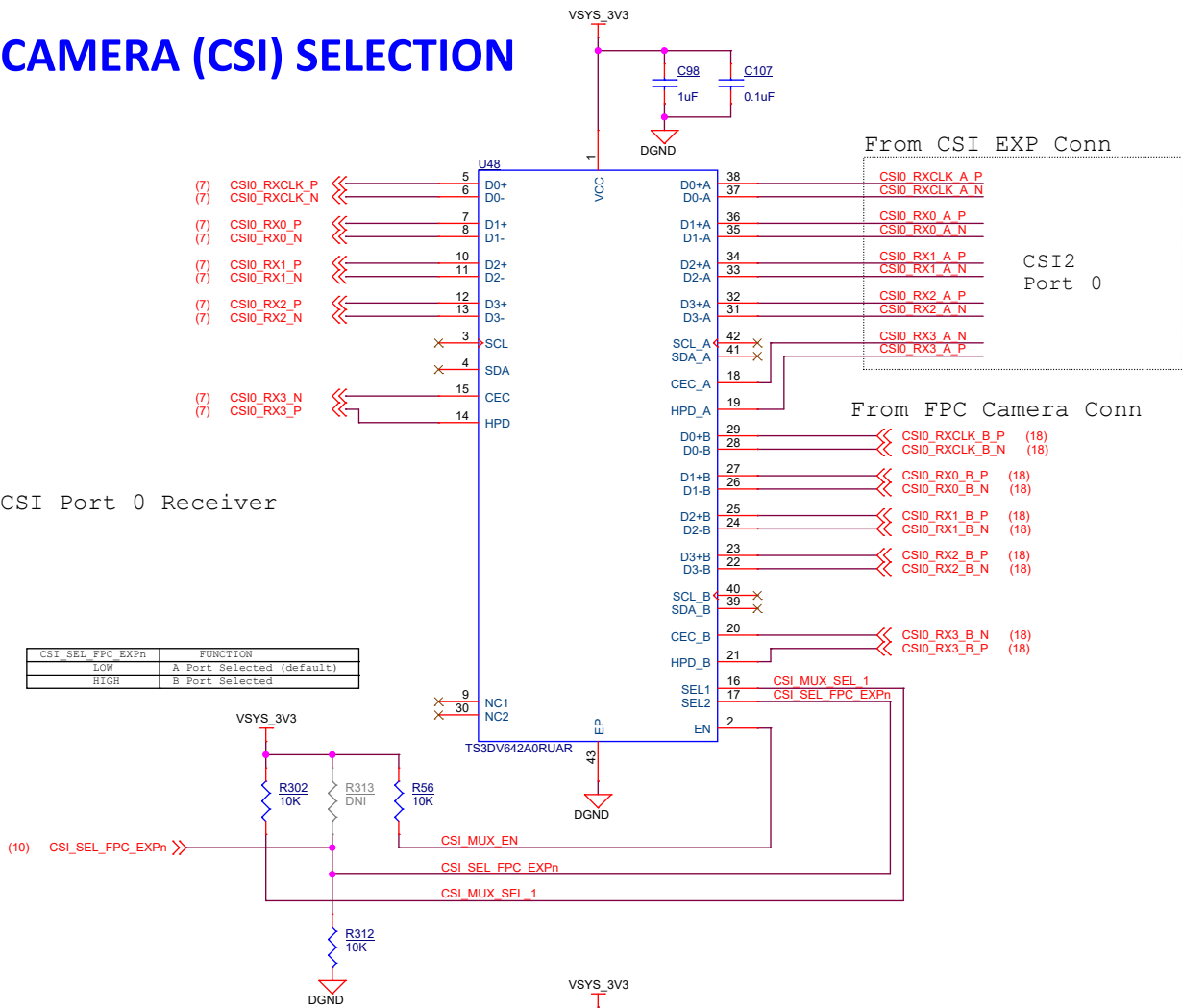
RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

Speed and Activity Drivers

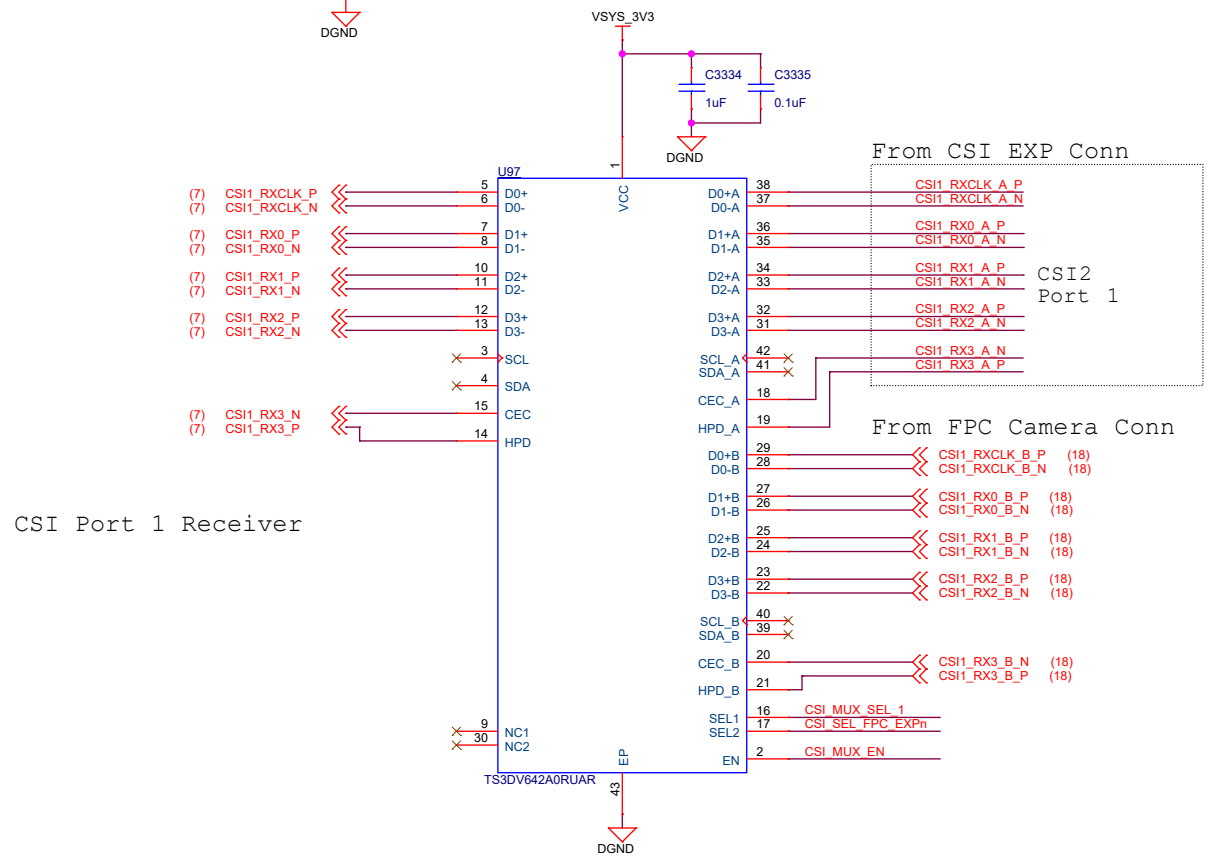


CAMERA (CSI) SELECTION

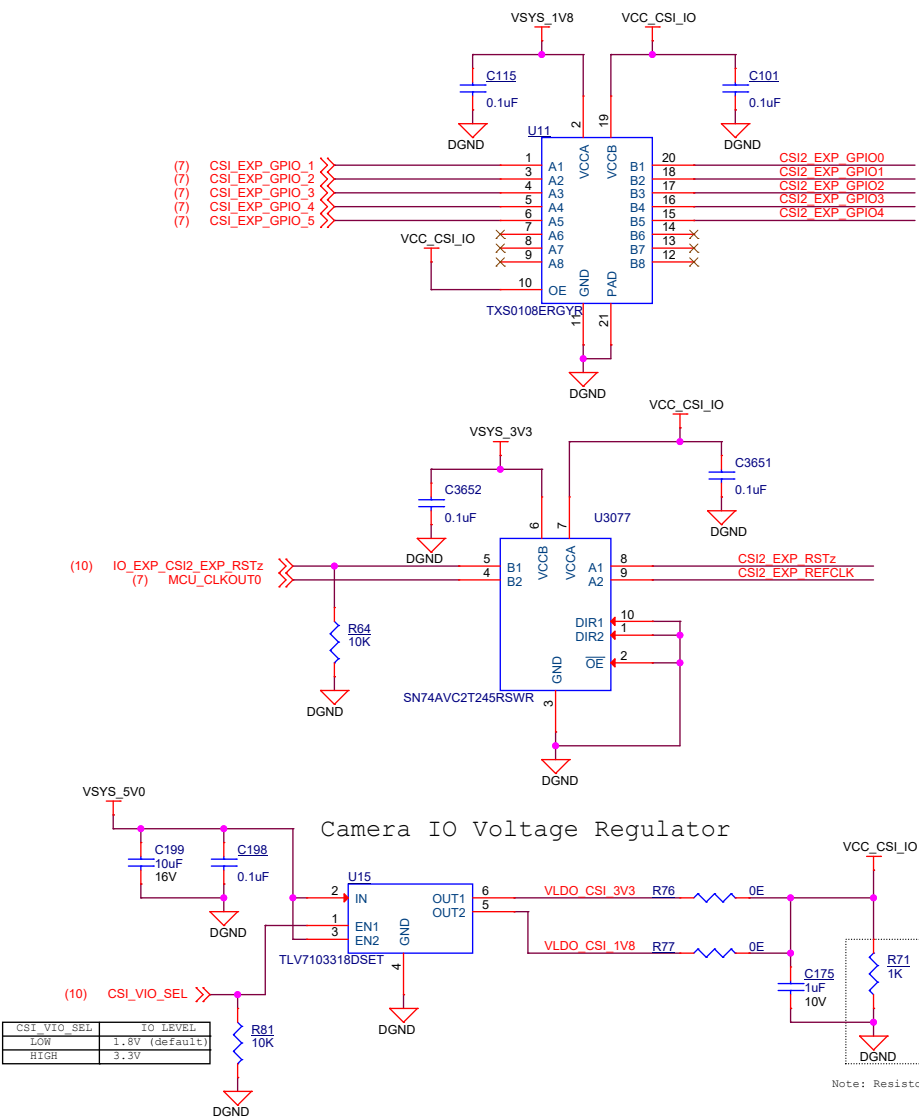
CSI Port 0 Receiver



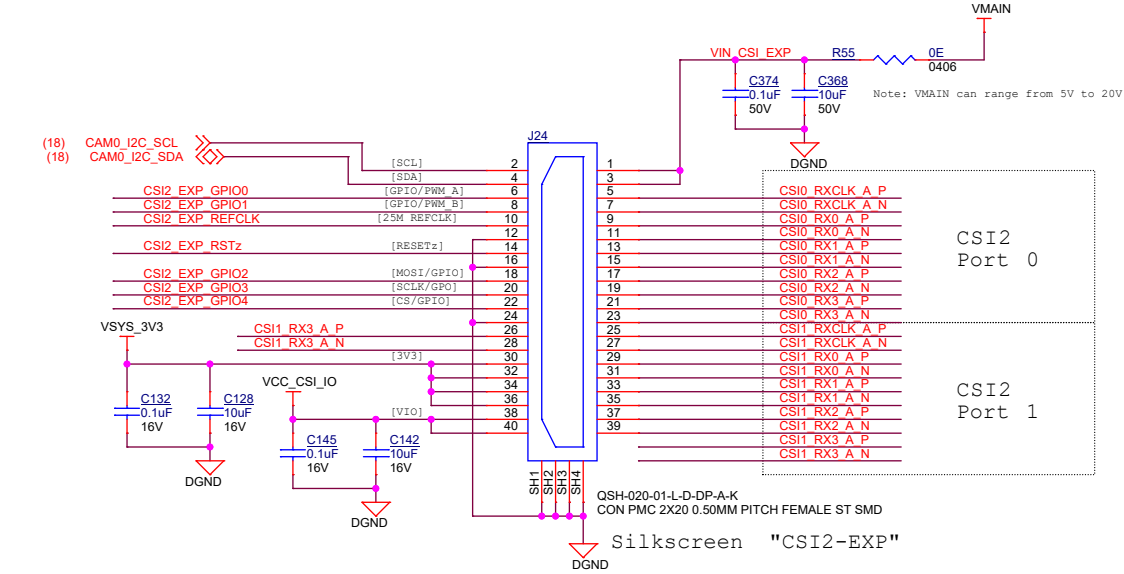
CSI Port 1 Receiver



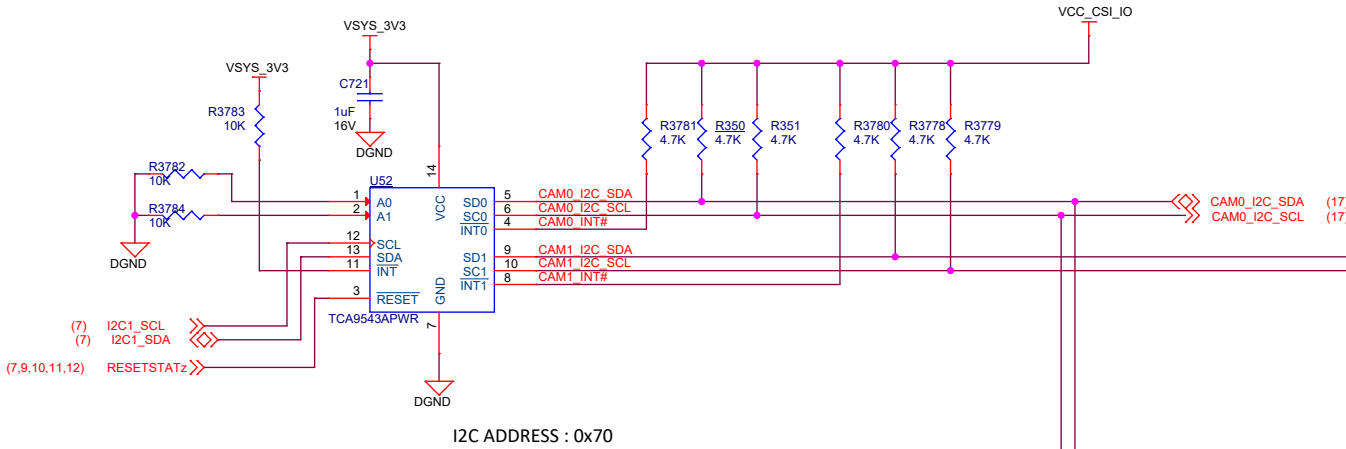
Camera IO Level Translation



CAMERA (CSI) EXPANSION



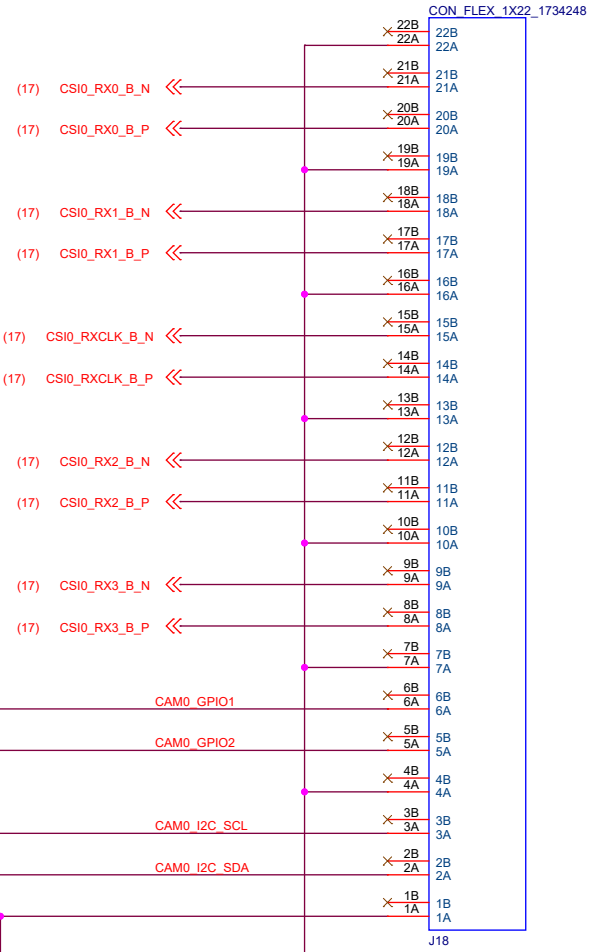
Camera I2C Bus Switch / Level Translation



CAMERA (CSI) FPC CONNECTORS

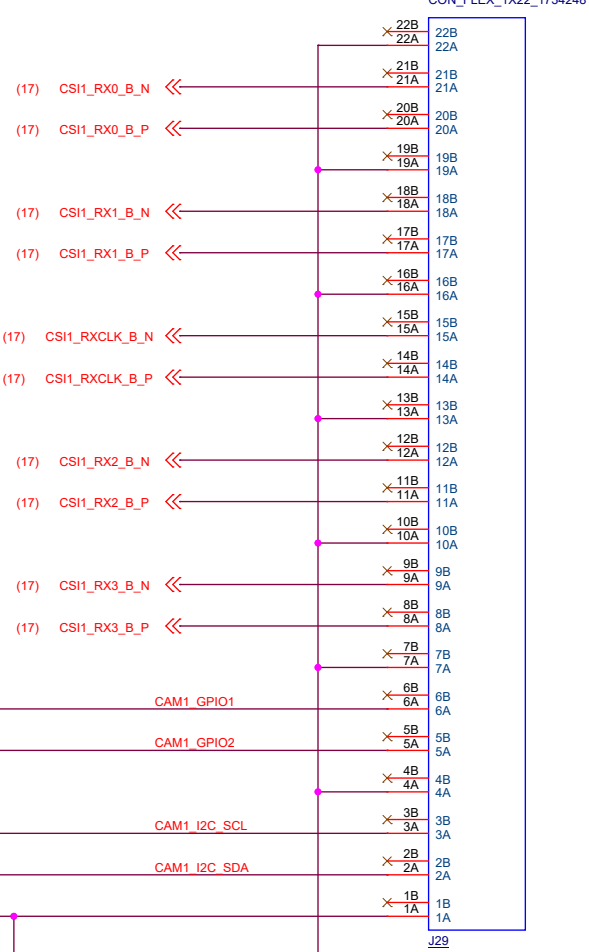
Silk Screen "CAM1"

FPC Camera Connector -1

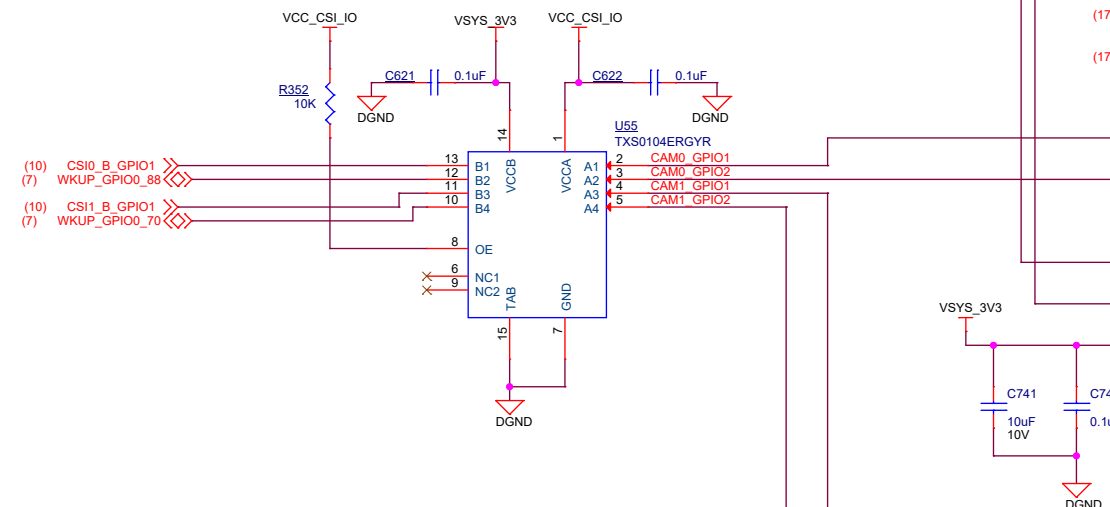


Silk Screen "CAM2"

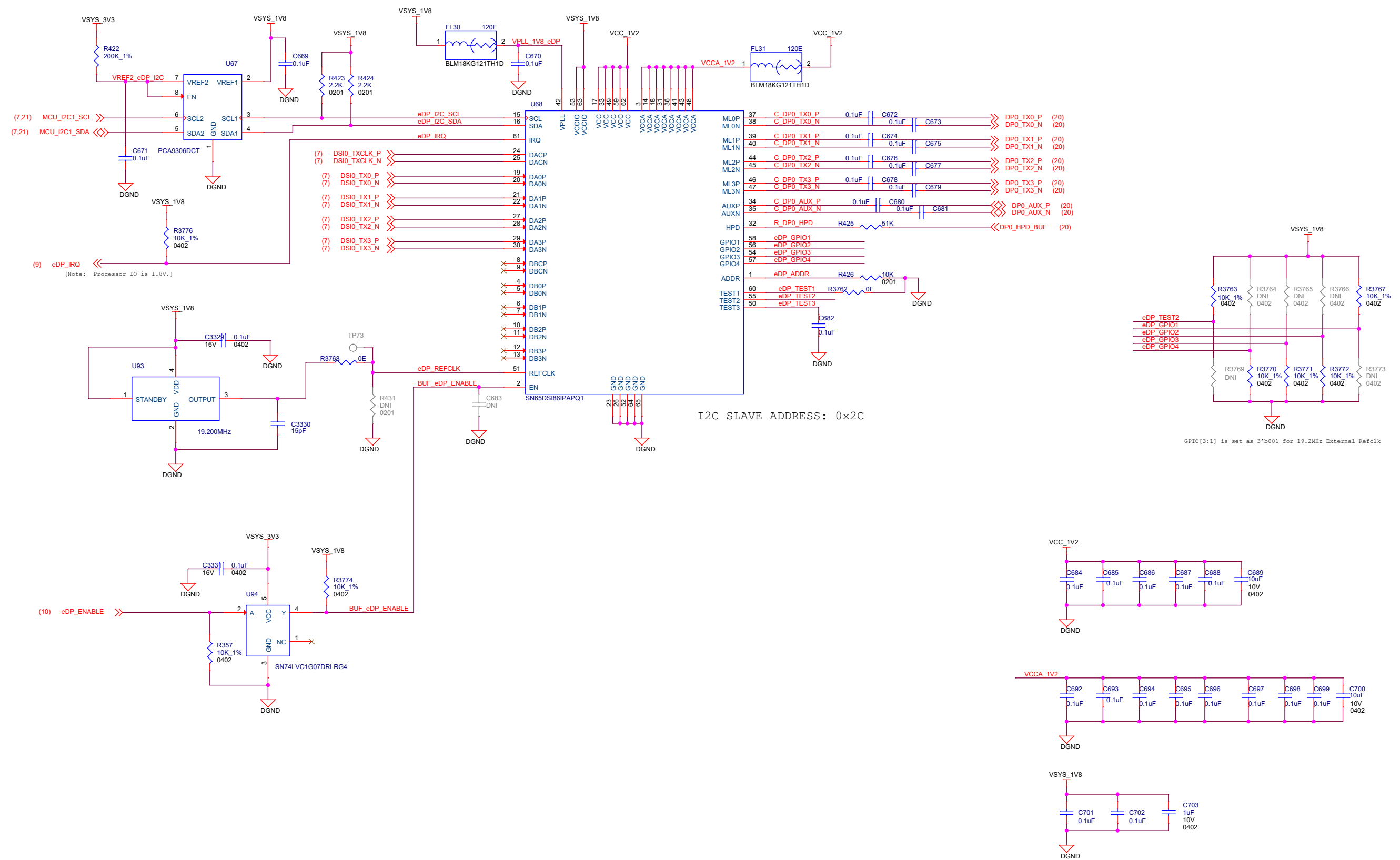
FPC Camera Connector -2



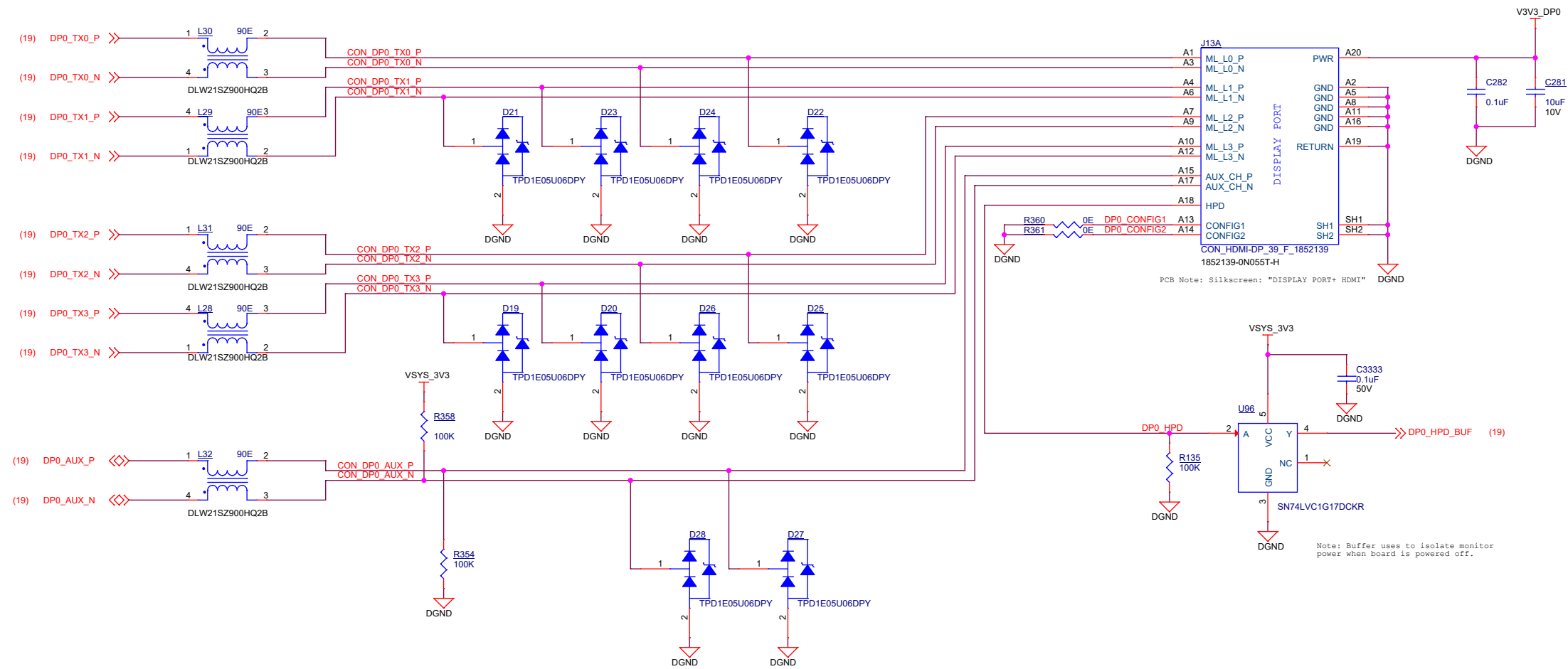
FPC Camera GPIO Level Translation



DISPLAYPORT BRIDGE

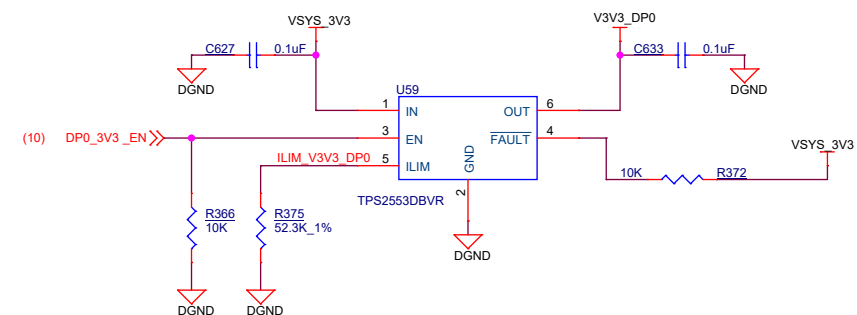


DISPLAYPORT INTERFACE

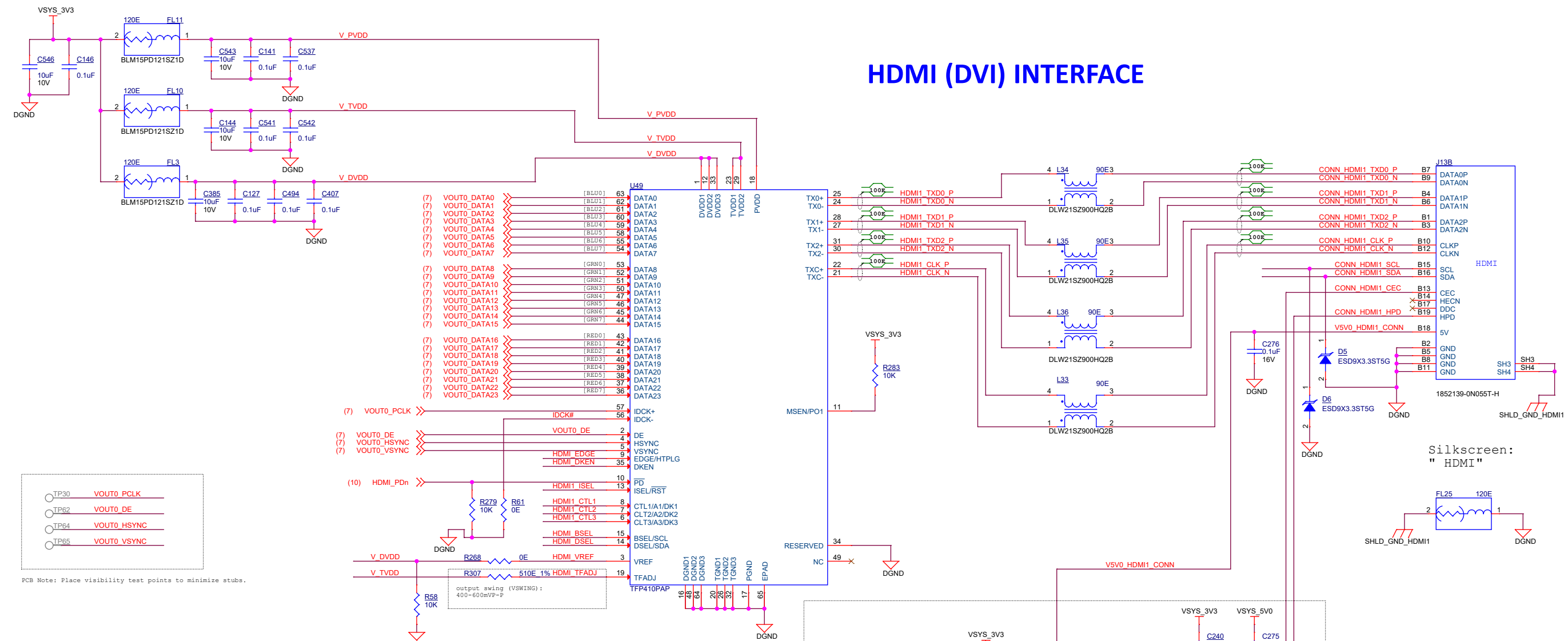


PCB Note: Place all ESD diodes close to DISPLAY PORT CONN, route trace through connector so no stub is created.

Display Port Cable Power Control



HDMI (DVI) INTERFACE

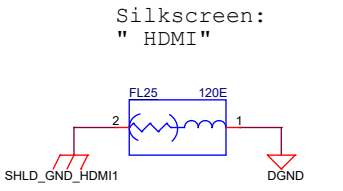
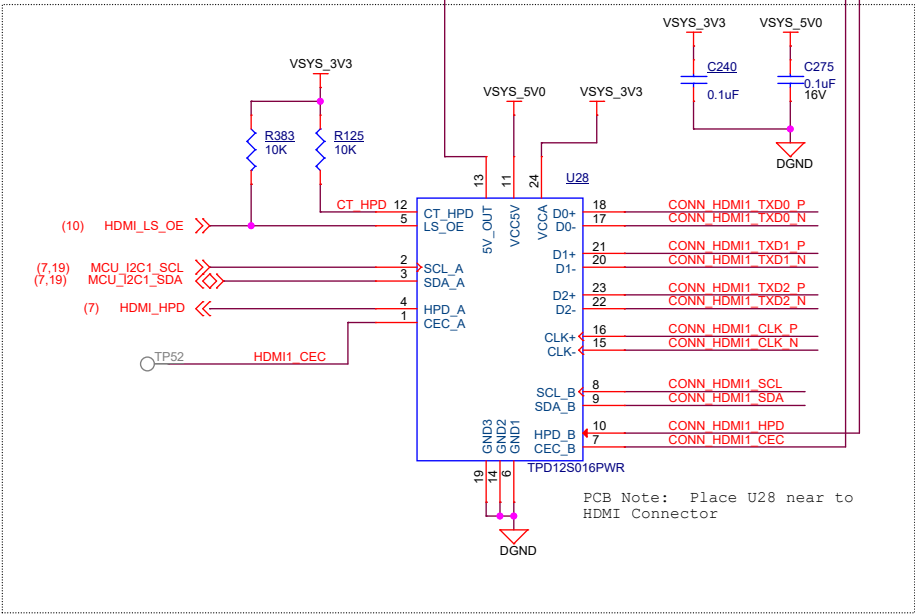


DVI Configuration Settings

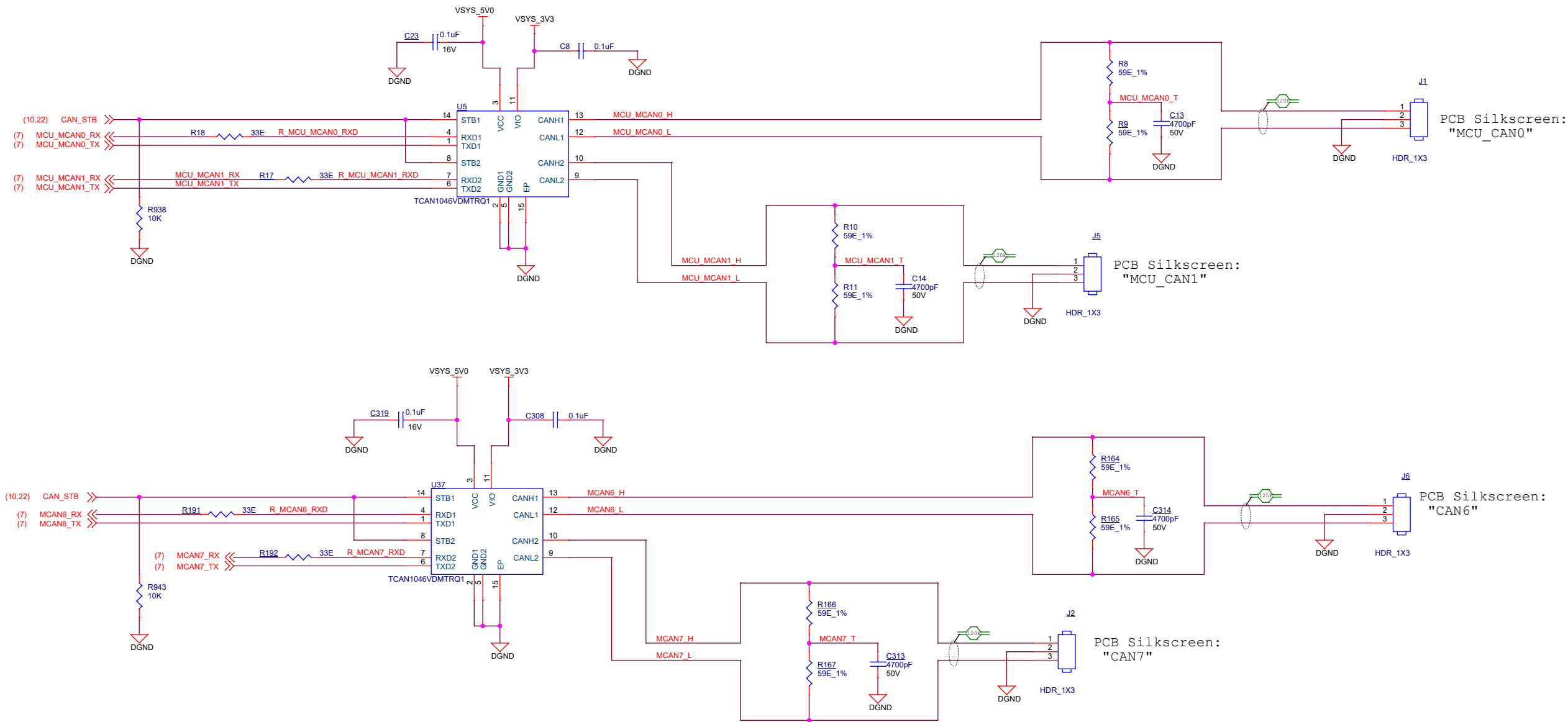
output swing (VSWING):
400-600mVp-p

VREF	BSEL	EDGE	DSEL	BUS WIDTH	LATCH MODE	CLOCK MODE	CLOCK EDGE
0.55V-0.9V	1	0	0	24-bit	Single-ended	Falling	Single-ended
Default	1	1	0	24-bit	Single-ended	Raising	Single-ended

ISEL:- Low (default): I2C interface is disabled and chip configuration is specified by BSEL, DSEL, EDGE, VREF pins
When ISEL: L, DSEL-H- enables de-skew function (default)

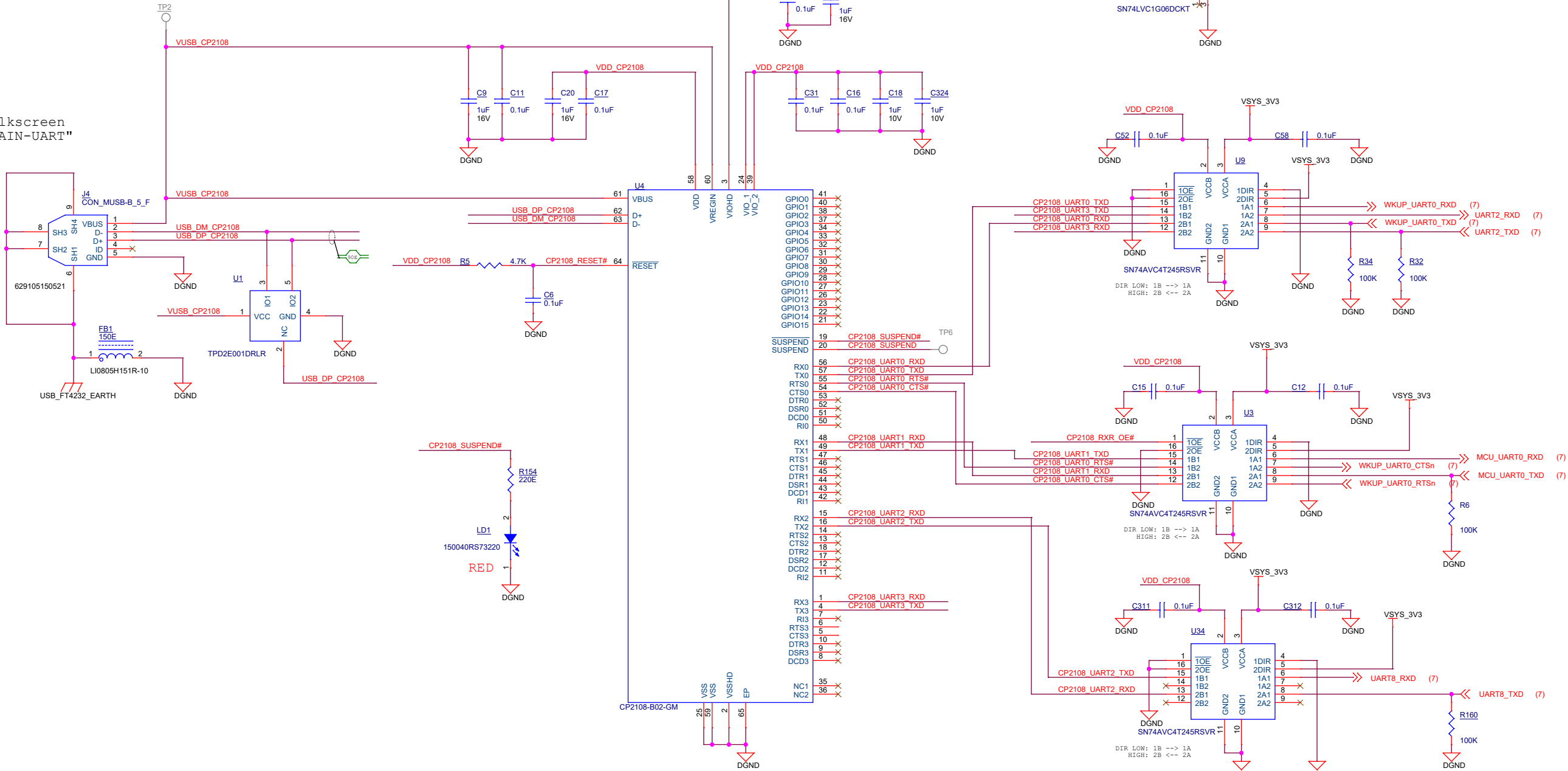


CAN-BUS INTERFACE

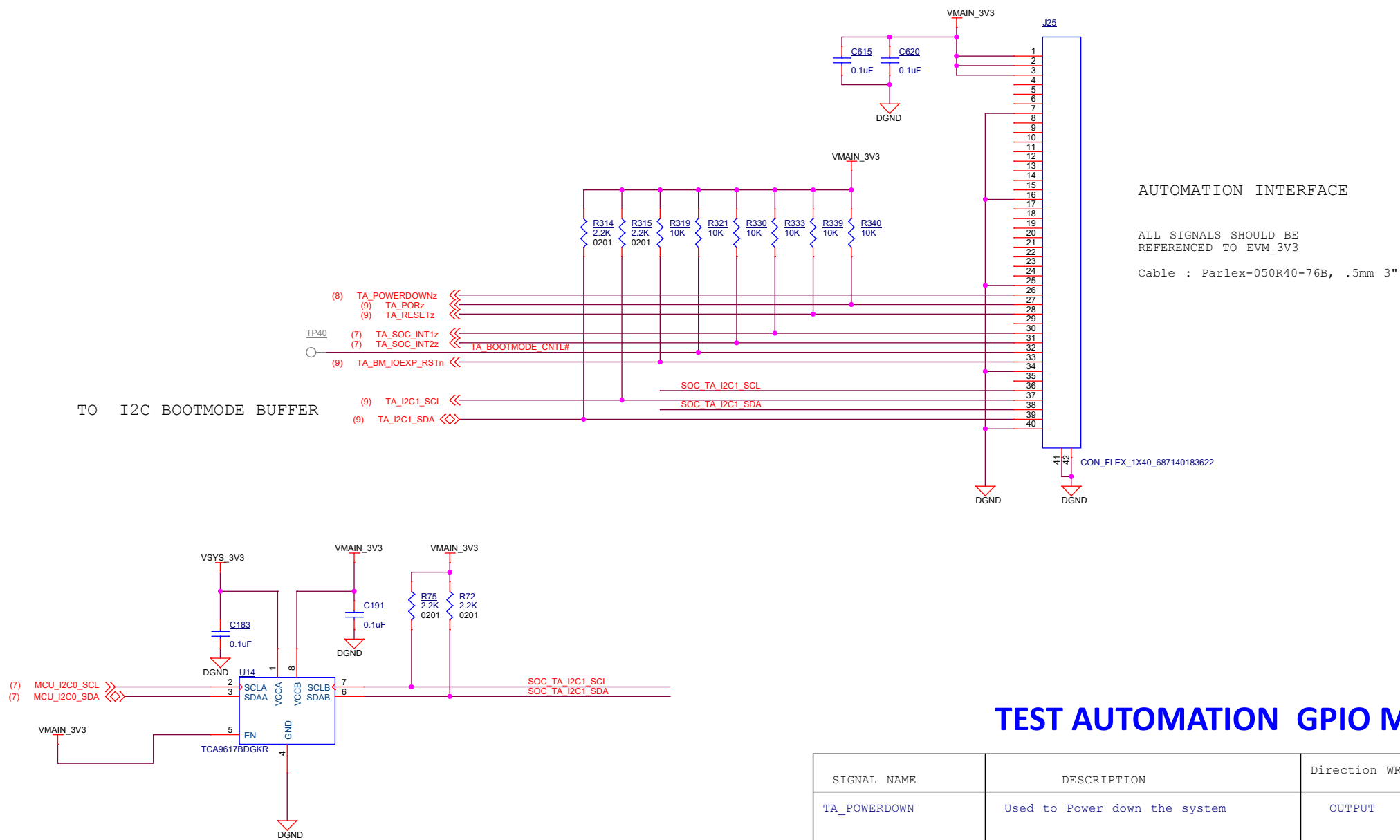


QUAD PORT CONSOLE

Silkscreen
"MAIN-UART"



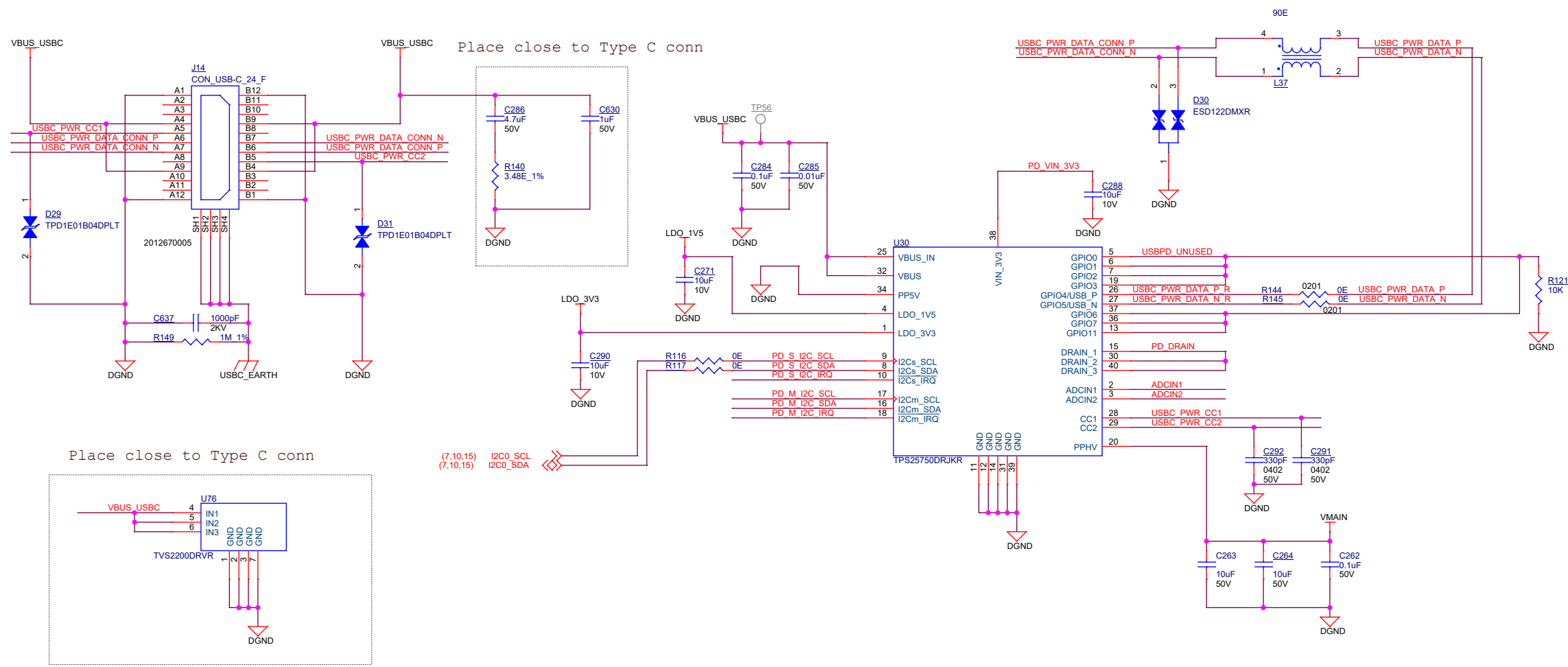
TEST AUTOMATION HEADER



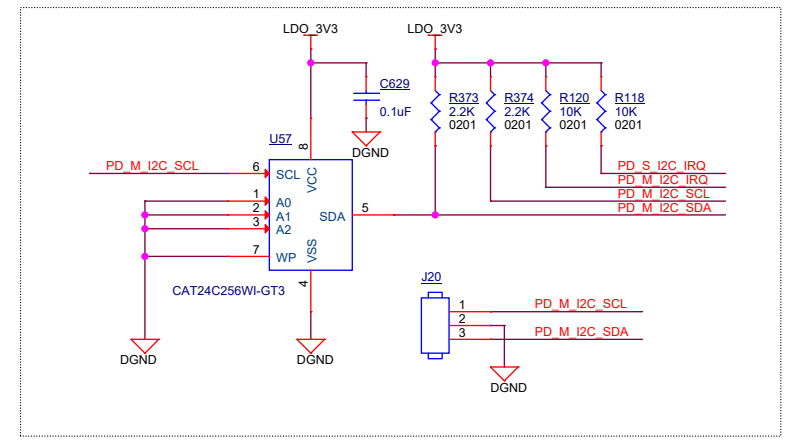
TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

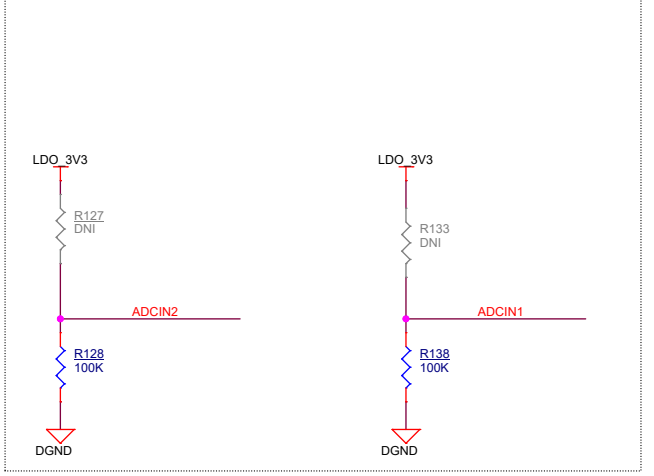
USB-C Power



EEPROM & PROGRAMMING HEADER

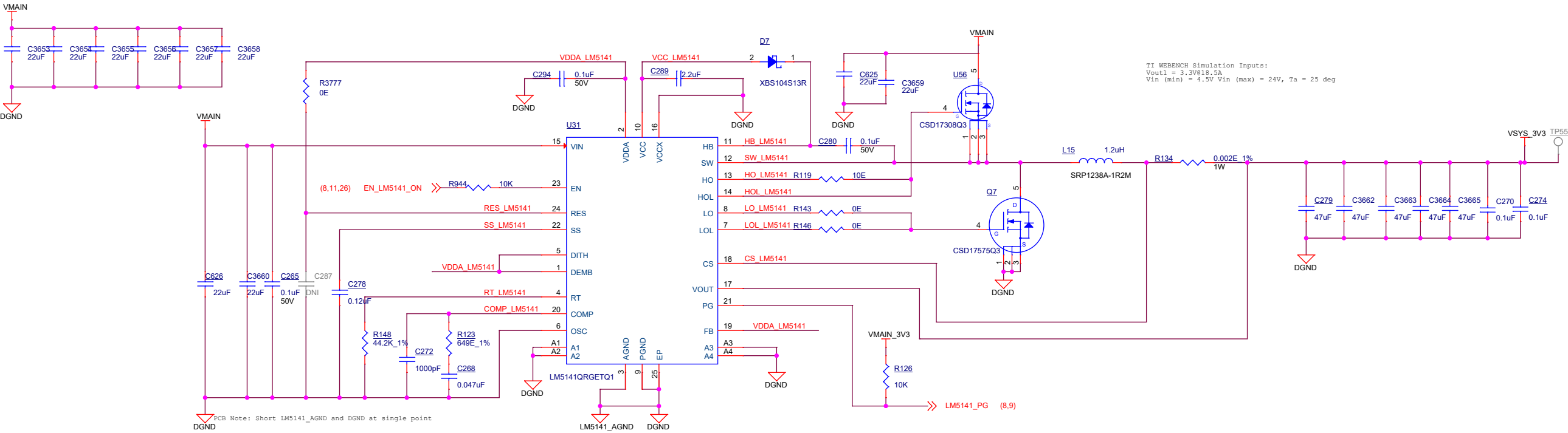


ALWAYS ENABLE SINK I2C SLAVE ADDRESS 0x20h (#01)

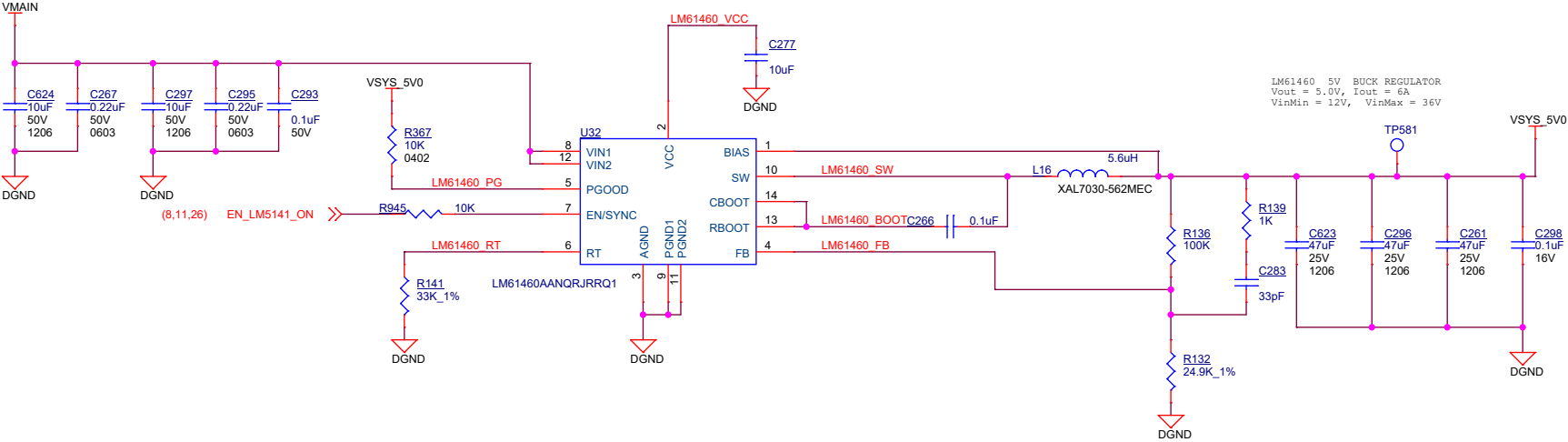


POWER REGULATORS / SWITCHING

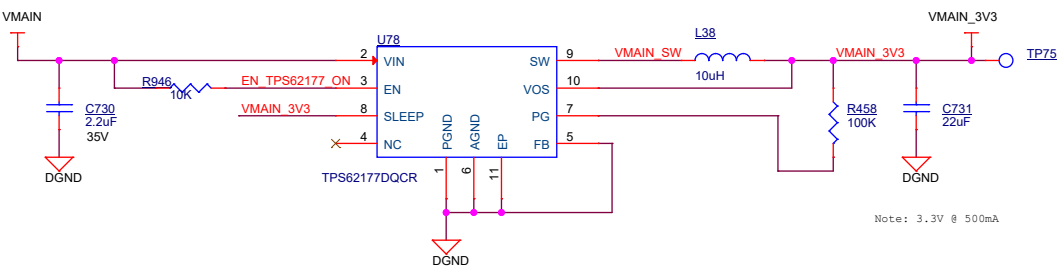
System 3.3V Regulator



System 5.0V Regulator

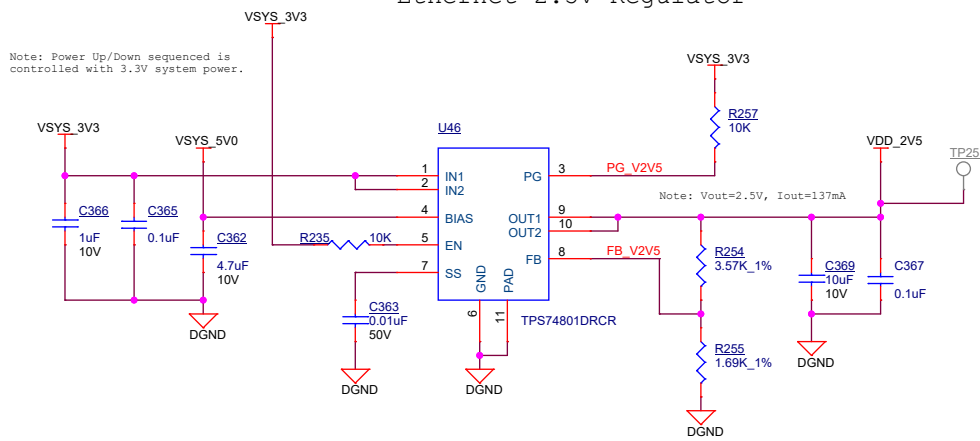


System Management 3.3V Regulator

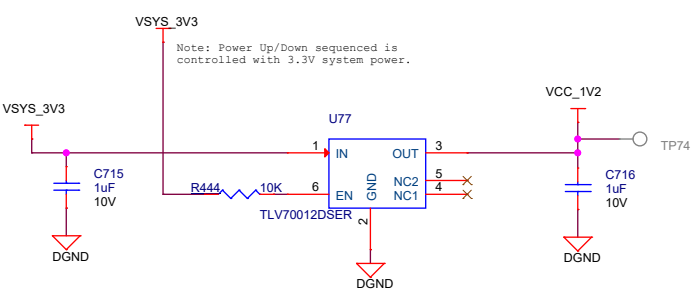


POWER REGULATORS / LINEAR DROPOUT

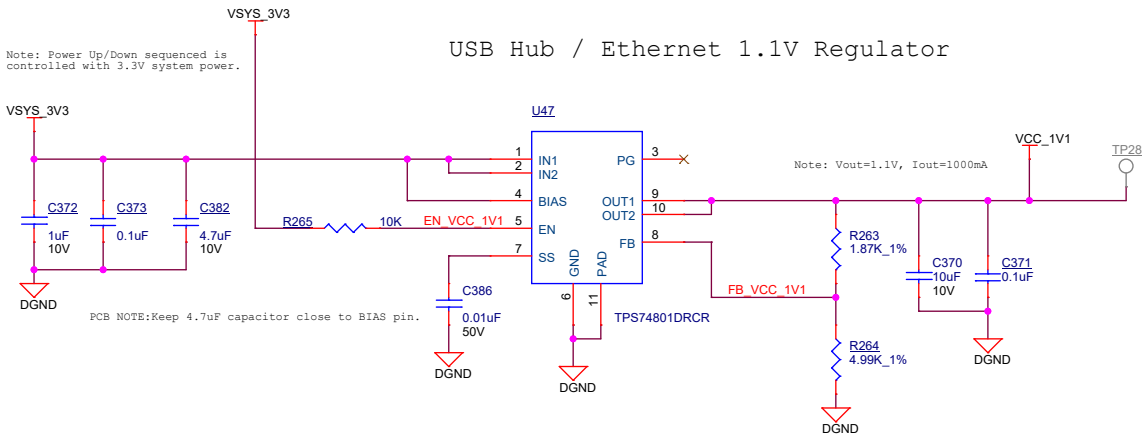
Ethernet 2.5V Regulator



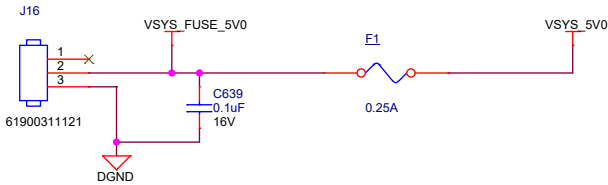
DisplayPort Bridge 1.2V Regulator



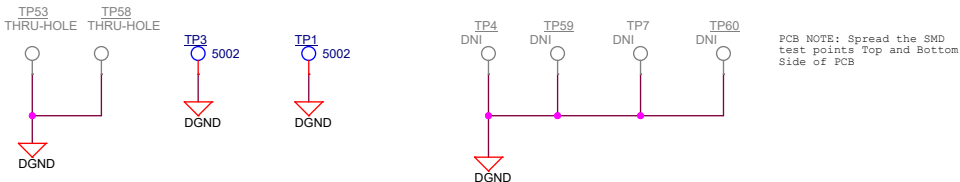
USB Hub / Ethernet 1.1V Regulator

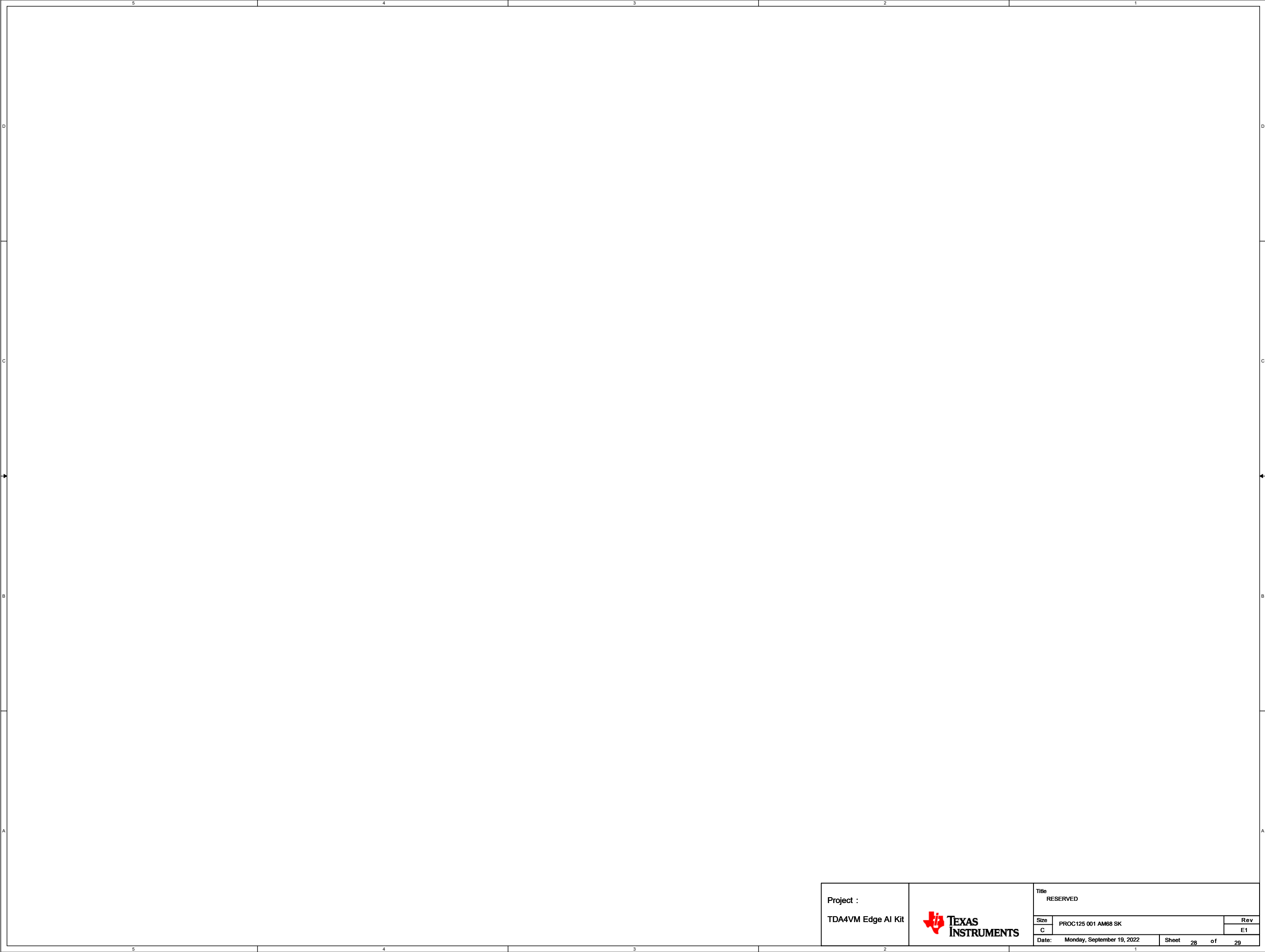



FAN INTERFACE



GROUND TEST POINTS





Project : TDA4VM Edge AI Kit				Title RESERVED	
				Size C	Rev E1
				Date: Monday, September 19, 2022	Sheet 28 of 29

NOTES, HW & LABELS

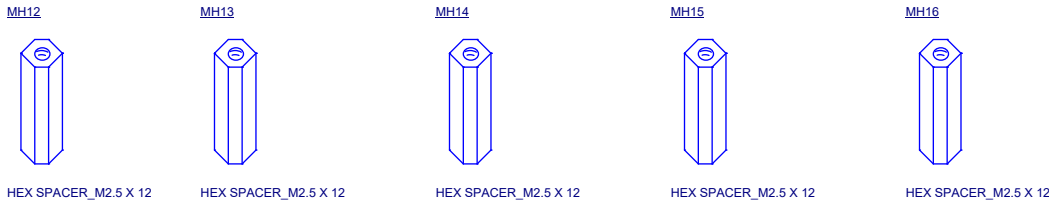
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

SCREWS



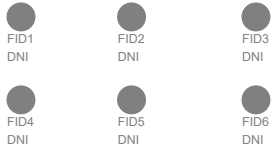
STANDOFFs



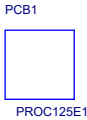
WASHER



FIDUCIALS



BARE PCB



LABELS

Board Serial No.

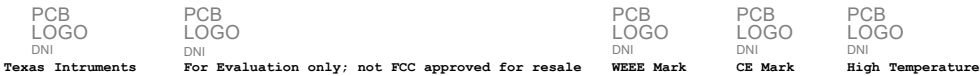


Assembly Revision.



OPN: SK - AM68

LOGOs



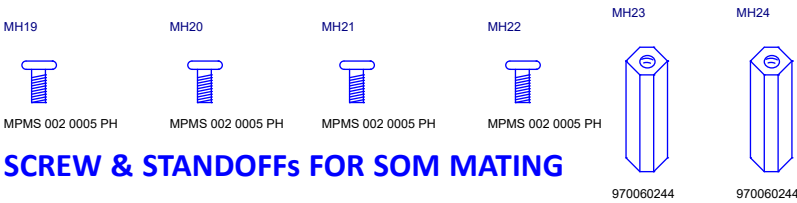
SCREW & WASHER FOR PCIe M.2



Added for placement



SCREW & STANDOFFs FOR SOM MATING



Project :
TDA4VM Edge AI Kit



Title		
HARDWARE SCHEMATICS		
Size	Rev	
C	PROC125 001 AM68 SK	E1
Date:	Tuesday, October 04, 2022	Sheet 29 of 29