

87654321

REVISIONS

REV #DESCRIPTIONDATE

REV #CCN #150922

FABRICATION NOTES:

1. FABRICATE PCB IN ACCORDANCE WITH IPC-6013, CLASS 2, PER IPC-4101. PCB SHALL BE MANUFACTURED USING HT-40 OR EQUIVALENT.

2. MATERIALS:

1. LAMINATE AND PREPREG (B-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/128, (V90/76/100)

2. COPPER FOIL, TO BE IN ACCORDANCE WITH IPC-MF-106, UNLESS OTHERWISE SPECIFIED. ALL COPPER WEIGHT FOR INNER SIGNAL LAYERS AND INNER PLANE LAYERS IS TO BE 20µm (1 oz./sq.). FOR OUTER LAYERS, 1.5-2.0 oz. COPPER WEIGHT IS TO BE CONSIDERED "PRIMED". THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC DESIGN RULES 3-7 AND 3-8.

3. ALL HOLES SHALL BE LOCATED WITHIN 0.100mm DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.100mm.

4. BOM AND TRIST SHALL NOT EXCEED MORE THAN 0.10% OF THE DESIGN LENGTH.

5. CONDUCTOR WIDTH SHALL NOT BE LESS THAN 100µm FROM ITS ORIGINAL DATA. INCREASE FOR HATCHING IMPEDANCE MISTAKE SHALL APPROXIMATE THE MODIFIED WIDTH AND SPACING. TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.

6. AUTOMATIC OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.

7. FINISH:

1. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENGL. ELECTROLESS NICKEL/IMMERSION GOLD. ELECTROLESS NICKEL SHALL BE 0.4 MICRONS. TYPICAL DIMENSION GOLD THICKNESS SHALL BE 0.04-0.06 MICRONS OF SOLDERABLE DIMENSION ROAD SURFACE.

2. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-SM-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. VIA HOLES THAT HAVE MASK OPEN SHALL BE FILLED WITH NON CONDUCTIVE INK AND CAP PLATED. ALL OTHER VIA HOLES SHALL BE FILLED WITH NON CONDUCTIVE INK AND COVERED WITH SOLDER MASK. ONLY SOLDERMASK THINGS THAT ARE 0.100-0.200" PCD SIZE SHALL BE REPOSED IF REQUIRED. ALL OTHER SOLDER MASK THINGS SHALL NOT BE ENLARGED. DEFAULT COLOUR OF SOLDER MASK SHALL BE BLUE.

3. SILKSCREEN SHALL BE WHITE. PERMANENT. ORGANIC. NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERABLE AREA.

4. SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 120µm (0.0049"). INCREASE OF LASER VIAL'S, BLIND VIAL'S SHALL NOT BE LESS THAN 120µm (0.0049") AND BURRED VIAL'S SHALL NOT BE LESS THAN 100µm (0.0039").

5. ALL HOLES SURROUNDED BY LAMB 0.05-0.05" SHALL BE COMPLIANT TO IP6041, CLASS B.

8. MARKING:

1. BOARD SHALL MEET THE REQUIREMENTS OF UL-794 WITH FLAMMABILITY RATING OF MAXIMUM 94V-0. UL LOGO IN FILE NUMBER, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE MARKED IN SILKSCREEN.

9. TEST REQUIREMENTS:

1. 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-8-396 NET LIST FOR OPEN AND SHORTS.

10. THERMAL IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.

11. TEAR DROPS SHALL BE ADDED ON INTERNAL AND EXTERNAL LAYER FOR ALL THE VIAS AND THROUGH HOLE PADS.

12. FINISHED PAD THICKNESS SHALL BE 0.004" +/-0.001.

13. MIN TRACE WIDTH/SPACING ON BOARD IS 0.085/0.085".

14. ALL THE IMPEDANCE SHALL BE MATCHED AS PER IMPEDANCE TABLE WITH +/-10% TOLERANCE.

15. ENSURE THAT UL REGISTERED E-FILE NUMBER SHALL BE PRINTED ON PCB SILKSCREEN

16. ALL UNCONNECTED VIAS SHALL BE SUPPRESSED IN INTERNAL LAYERS.

17. MICRODRESSING TO BE DONE FROM LIT TO LAY.

18. FOR DETAILED STACKUP, PROCES, STACKUP.PDF SHALL BE REFERRED

19. RECOMMENDED PLATING FOR CONTACT PAD ARE:

1) VARIATION 444-003 PLATING 0.14 MICROMETERS MINIMUM OVER 2.00 MICROMETERS MINIMUM NICKEL.

20. THE ADDITION OF THIS LEVEL IS A FABRICATION OPTION AND IS NOT REQUIRED. THE LEVEL IS NOT HIT THE PLATED CONTACTS.

ALL WHITE ARE TO BE ENGL

FIGURE SIZE TOLERANCE PLATED DVT

START 1.5 1.5 1.5 1.5

END 1.5 1.5 1.5 1.5

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SHALL 'GAIN' TOP TO BOTTOM

FIGURE SIZE TOLERANCE PLATED DVT

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END 1.5 1.5 1.5 1.5

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IMPEDANCE SPECIFICATIONS

SL# TYPE LAYER TRACEWIDTH(MIL) SPACING(MIL) IMPEDANCE(Ohms) REF. LAYER

01 EDGE COUPLED MICROSTRIP L1/L12 4.8 7 100 L2/L11

02 EDGE COUPLED MICROSTRIP L1/L12 5.1 5 80 L2/L11

03 EDGE COUPLED MICROSTRIP L1/L12 6 5 85 L2/L11

04 EDGE COUPLED MICROSTRIP L1/L12 7 5 80 L2/L11

05 EDGE COUPLED MICROSTRIP L1/L12 11 8 66 L2/L11

06 MICROSTRIP L1/L12 14 - 33 L2/L11

07 MICROSTRIP L1/L12 19 - 40 L2/L11

08 MICROSTRIP L1/L12 6.5 - 50 L2/L11

09 EDGE COUPLED STRIPLINE L8 3 6.5 66 L2/L4

10 EDGE COUPLED STRIPLINE L3,L5 4.6 3 80 L2/L4,L4/L6

11 EDGE COUPLED STRIPLINE L10 4.2 5 85 L9/L11

12 EDGE COUPLED STRIPLINE L3,L10 4 8 90 L2/L4,L4/L6,L9/L11

13 EDGE COUPLED STRIPLINE L3,L5,L10 3 5 100 L2/L4,L4/L6,L9/L11

14 STRIPLINE L3 3 - 33 L2/L4

15 STRIPLINE L3,L5 5 - 40 L2/L4,L4/L6

16 STRIPLINE L3,L5,L8,L10 3.2 - 50 L2/L4,L4/L6,L7/L9,L9/L11

17 STRIPLINE L8 6.5 - 33 L7/L9

LAYER STACKUP

LAYER NAME FINISHED Cu X-SECTION DIELECTRIC THICKNESS [INCHES]

PRIMARY SIDE SILKSCREEN

PRIMARY SIDE SOLDERMASK

001 PRIMARY SIDE 1.456

002 GROUND-PLANE-1 142 0.0037

003 INNER-SIGNAL-1 0.142 0.0030

004 GROUND-PLANE-2 142 0.0030

005 INNER-SIGNAL-2 0.142 0.0030

006 POWER-PLANE-1 142 0.0030

007 POWER-PLANE-2 142 0.0030

008 INNER-SIGNAL-3 0.142 0.0030

009 GROUND-PLANE-3 142 0.0030

010 INNER-SIGNAL-4 0.142 0.0030

011 GROUND-PLANE-4 142 0.0030

012 SECONDARY SIDE 1.456 0.0037

SECONDARY SIDE SOLDERMASK

SIGNATURES DATE

LAYOUT BY SK 150922

REVIEWED BY ZA 150922

APPROVED BY AMB 150922

SCALE: NONE

SIZE D

Rev E1

SHEET 1 OF 19

TEXAS INSTRUMENTS

PROC3131E

JTAEP SK SON BOARD