

# AM69 Processor Starter Kit

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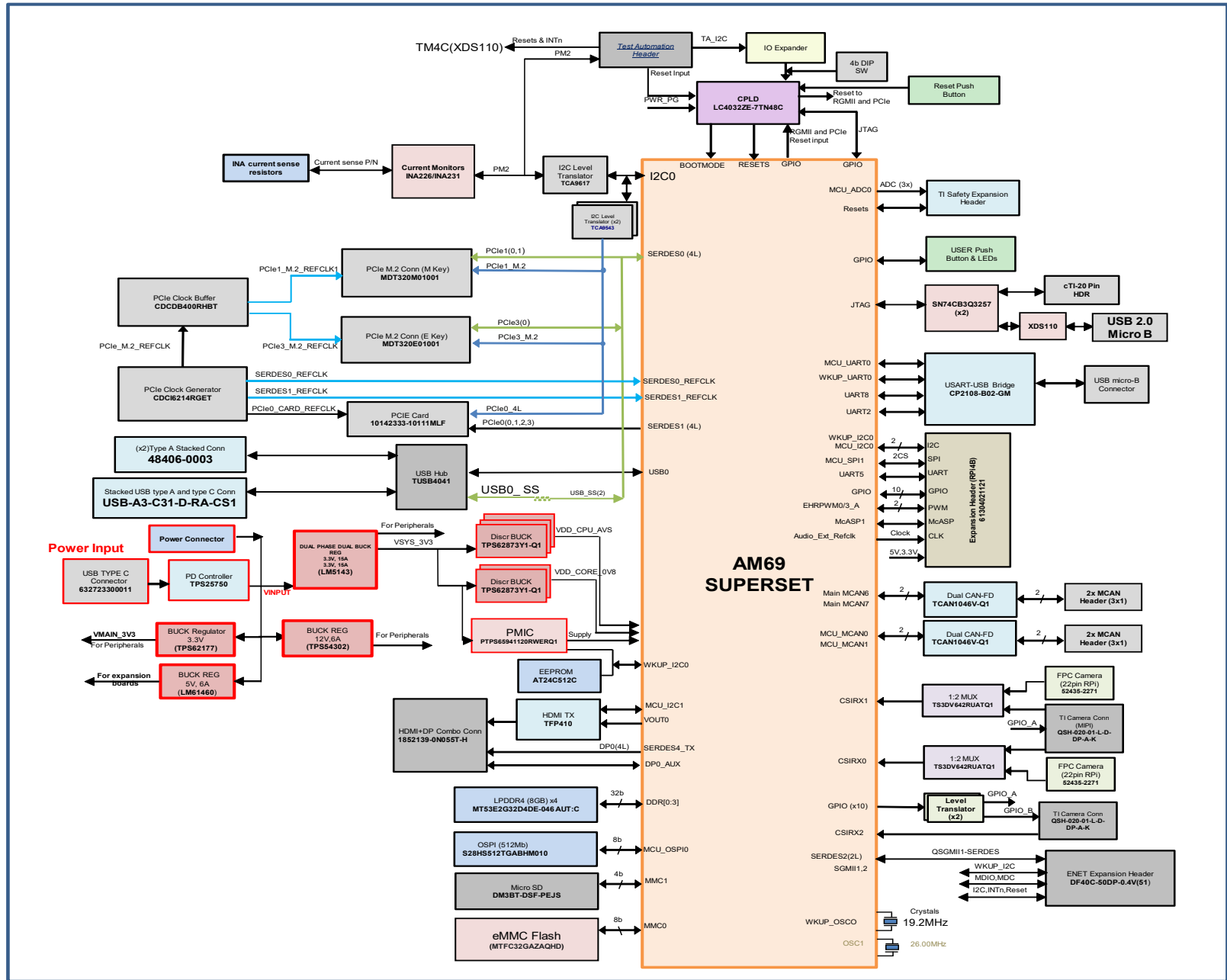
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REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E2	21 OCT 2022	Taken AM69 SK Rev E1 design as reference and Added CDCI6214 clock generators for PCIe devices	Mistral Design Team		
	2 NOV 2022	1. Replaced U113 with clock buffer CDCDB400 as a clock source for PCIe M key and E key. 2. Updated U50 connection to provide resistor mux for CDCI1_OE2/OE3 and CDCI1_OE1/OE4 signals from U112	Mistral Design Team		
E2A	23 FEB 2023	Added ECN information for TIVA automation rework.	Mistral Design Team		
E2B	13 MAR 2023	1.Updated L1 L6 part number to XAL7070-122MEC 2.Updated U76 U78 part number to BSZ019N03LSATMA1	Mistral Design Team		
E3	16 MAR 2023	1.Updated L1 L6 part number to XAL7070-102MEC 2.Updated U76 U78 part number to CSD18563Q5A 3.Updated U75 U81 part number to CSD18543Q3A. 4. C36, R48,C42, R50 values have been modified. 5.TA_I2C_SCL , TA_I2C_SDA have been swapped with PM2_SCL, PM2_SDA. 6.Updated FB1, L28, R130, R368,R347,R267 to 0E for EMC compliance. 7.Made C801, C448, C441,C111 DNI.	Mistral Design Team		
E4	24 SEP 2024	SCH updates aligned to "J7AHP SK ECN1 v0.4.xlsx"  1.Updated C89, 91, 93 part number to GCM32ER71A226KE12L 2.Updated C112 and C150 part number to 04025U200FAT2A 3.Updated C100 part number to GCM155R71H472KA37D and C66 part number to GCM155R71H152KA37. 4.Updated R62 part number to RC0402JR-072K4L and R91 to RC0402JR-071K2L. 5.DNI'd C90, C92, C94, C113, C154 and R158. 6.Changed U34 part number to TPS7A2118POWDRBRQ1 7.Added 80E(Part# RT0402FRE0780RL) parallel to C254. 8.Updated PMIC(U48) BOM description and renamed GPIO pin net names. 9.Added U114,U3047, U3048 for isolating TA reset and control pins shared with the U82 IC. 10. Installed 10uF, 3-T, 0603 caps at FL44, FL45 & FL46 11. Added Rpu(R699) for disabling watchdog timer during power up seq. 12. Changed all SOC_PWRGRP_IRQn net names to DSCRT_PWRGRP_IRQn 13. Changed PMIC_WDOG_DISABLE net name to EN_GRP_PDN 14. Renamed U93.4 pin net name to USBC_PWR_EN_OUT 15. U55(12V0) IC EN pin is pulled down by R1307 and R554, R253 value is changed to 0E.	Mistral Design Team		
	18 MAR 2024	R559 DNI'd and net "EN_3V3_VIO_OR" blue wired and connected to U111.4	Mistral Design Team		


# SYSTEM BLOCK DIAGRAM



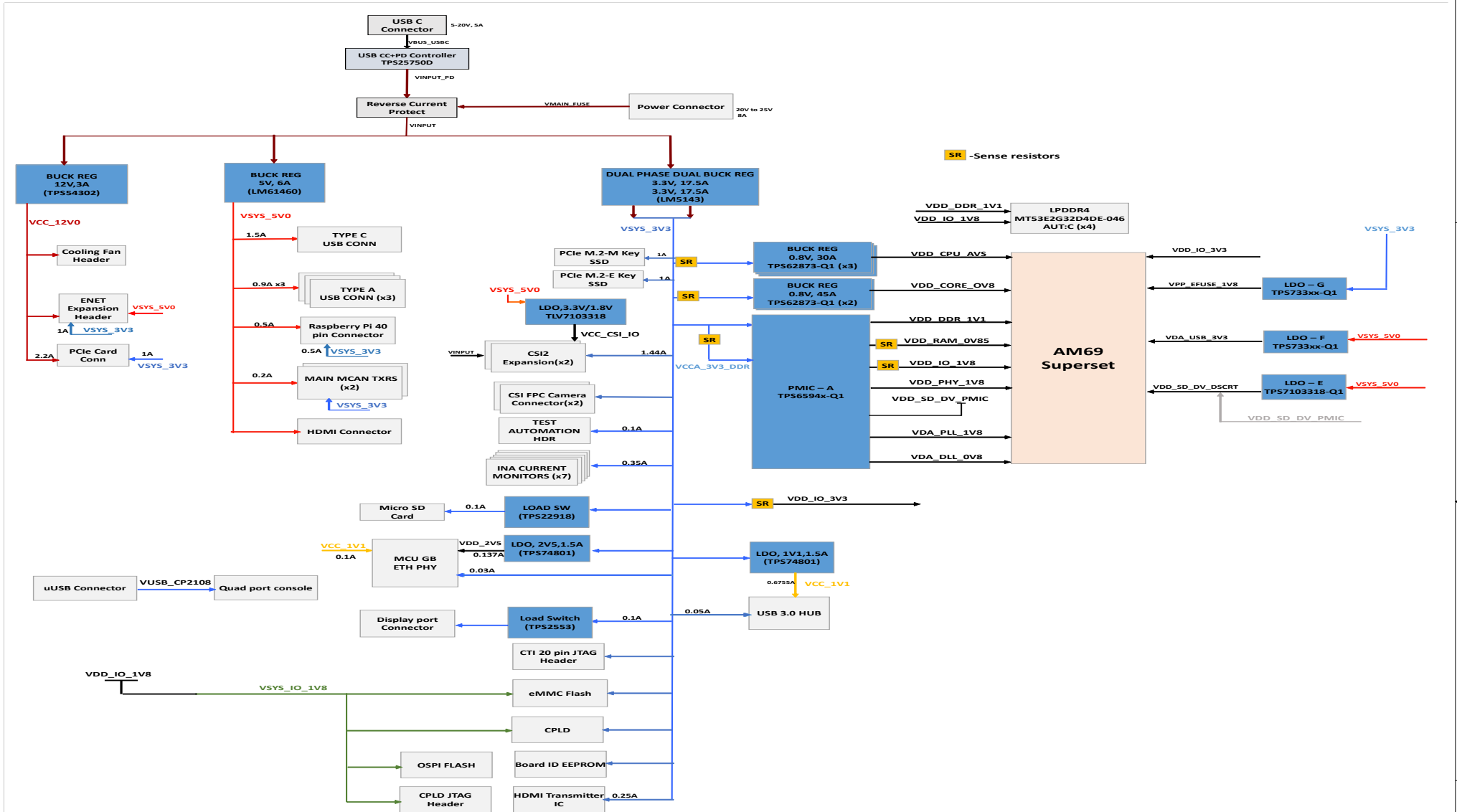
## PDN Recommended for New Designs

Refer to PDN file entitled 'AM69 SK Single Leo Dual HCPS PDN-3H.IN v0.25' which is included in the released design zip file

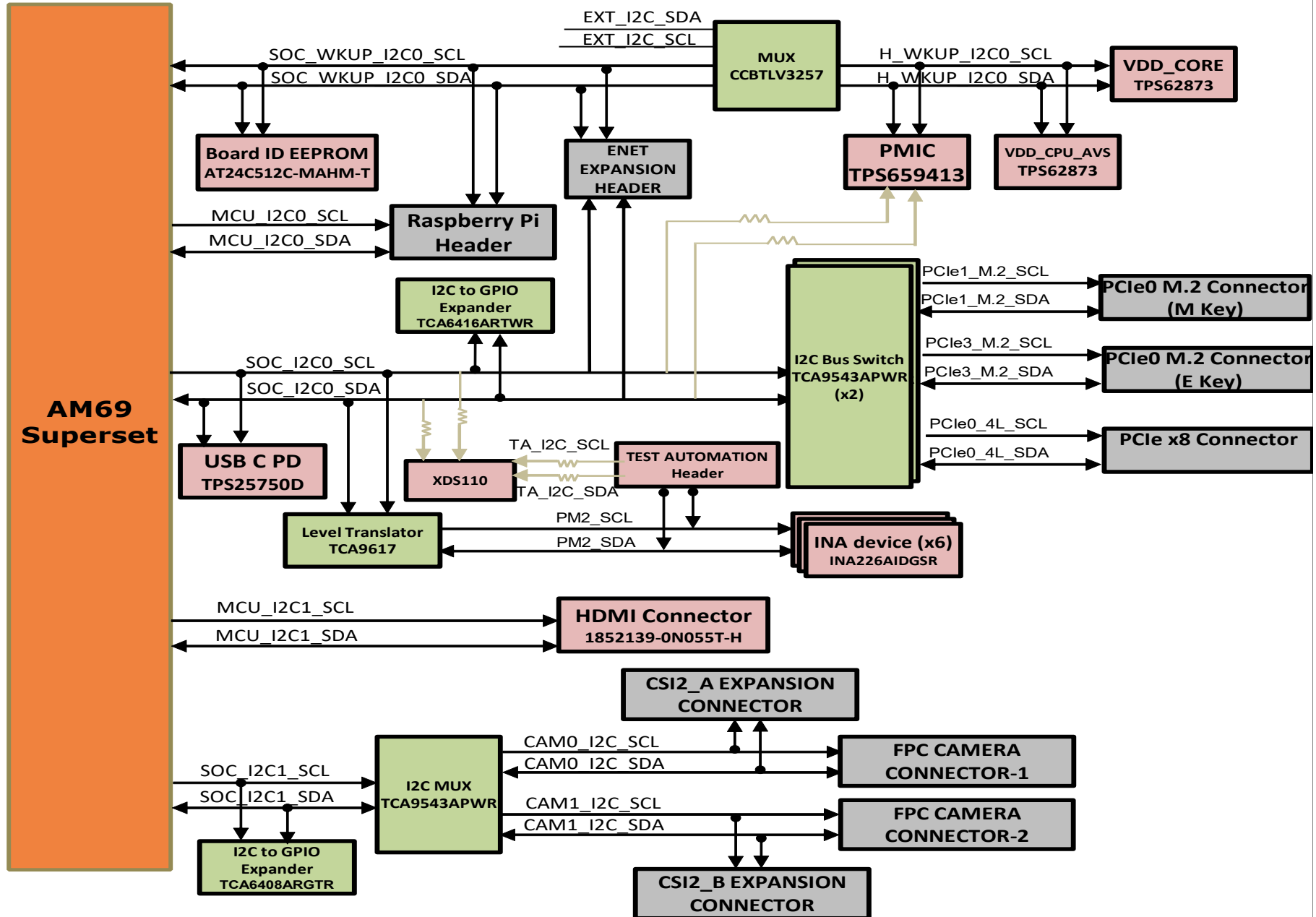
The AM69 SK SCH & PCB have implemented the PDN-3H.IN variant that supports reduced PDN features without low power modes (PDN-3H.yz), Industrial products (PDN-3x.Iz), No functional safety (PDN-3x.yN)

Project : AM69 Edge AI Kit				Title SoC EVM PMIC PDN-0.6	
Size C		PROC154E4 001 SK AM69			Rev E4
Date: Monday, May 05, 2025		Sheet 4 of 62			

# AM69 SK POWER FLOW DIAGRAM



## I2C TREE



## I2C TABLE

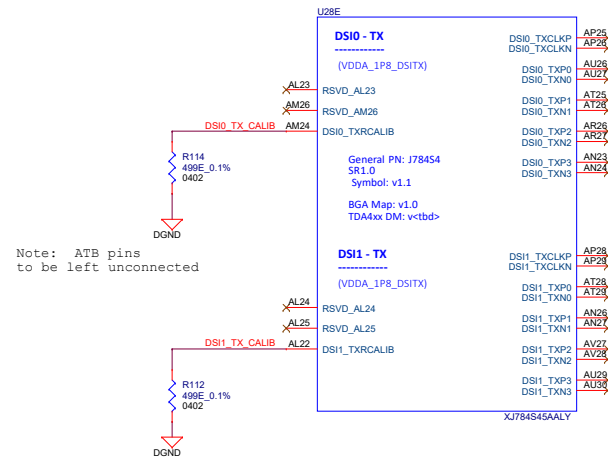
AM69 SK I2C Slave Address Table			
SOC I2C Port	Device Description	Part#	I2C Address
WKUP_I2C0	PMIC	TPS6594133ARWERQ1	0x48, 0x49, 0x4A & 0x4B
	VDD_CPU_AVS High-Current Power Stage A	TPS62873Y1QWRXSQR1	0x40
	VDD_CORE_0V8 High-Current Power Stage B	TPS62873Y1QWRXSQR1	0x43
	Raspberry Pi Header	61304021121	
	Board ID EEPROM	AT24C512C-MAHM-T	0x51
	ENET Expansion Header	171446-1109	0x57
MCU_I2C0	Raspberry Pi Header	61304021121	
MAIN_I2C0	Test Automation Header	687140183622	
	INA226 device for VCCA_3V3_CORE	INA226AIDGSR	0x45
	INA226 device for VCCA_3V3_CPU_AVS	INA226AIDGSR	0x4F
	INA226 device for VCCA_3V3_DDR	INA226AIDGSR	0x4D
	INA226 device for VDD_RAM_0V85	INA226AIDGSR	0x46
	INA226 device for VDD_IO_3V3	INA226AIDGSR	0x41
	INA226 device for VDD_IO_1V8	INA226AIDGSR	0x40
	PCIe_M.2_Interface M Key	MDT320M01001	
	PCIe_M.2_Interface E Key	MDT320E01001	
	Ext Power Measurement Header	61300311121	
	PCIe Card Slot	10018783-10202TLF	
	USB C PD Controller	TPS25750D	0x20
	Level Translator-1	TCA9543APWR	0x71
	Level Translator-2	TCA9543APWR	0x72
	GPIO Expander	TCA6416ARTWR	0x21
	PMIC	TPS6594133ARWERQ1	
	ENET Expansion Header	171446-1109	0x77
MCU_I2C1	HDMI Connector	1852139-0N055T-H	
MAIN_I2C1	FPC Camera Connector 1	52435-2271	
	FPC Camera Connector 2	52435-2271	
	CSI2_A Expansion Connector	QSH-020-01-L-D-DP-A-K	
	CSI2_B Expansion Connector	QSH-020-01-L-D-DP-A-K	
	GPIO Expander	TCA6408ARGTR	0x21
	Level Translator	TCA9543APWR	0x70

GPIO MAPPING TABLE

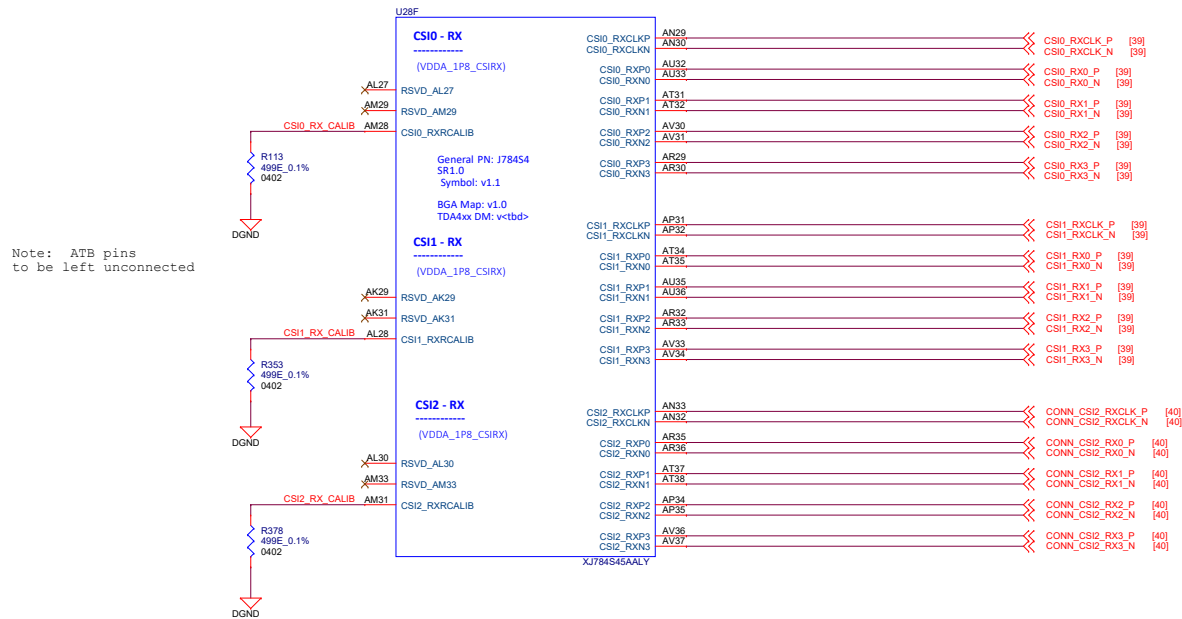
GPIO Mapping						
WKUP Domain						
J7AHP Mapping		Net Name	Input/Output	Default	State	Usage
Package Signal Name	GPIO					
MCU_OSPiO_CSn1	WKUP_GPIO0_28	EN_EFUSE_VPP	O	PD	Active High	Enable for VPP_EFUSE_1V8_LDO
MCU_OSPiO_CSn2	WKUP_GPIO0_29	CPiLD_TMS/CSiB_EXP_GPiO1	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_CLK	WKUP_GPIO0_31	CPiLD_TCK/CSiB_EXP_GPiO2	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_LBCLKO	WKUP_GPIO0_32	CSi_EXP_GPiO_1	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_DQS	WKUP_GPIO0_33	CPiLD_TDO/CSiB_EXP_GPiO3	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_D0	WKUP_GPIO0_34	CPiLD_TDI/CSiB_EXP_GPiO4	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_D1	WKUP_GPIO0_35	CSi_EXP_GPiO_5	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_D2	WKUP_GPIO0_36	CSi_EXP_GPiO_2	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_D3	WKUP_GPIO0_37	CSi_EXP_GPiO_3	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_CSn0	WKUP_GPIO0_38	CSi_EXP_GPiO_4	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_CSn1	WKUP_GPIO0_39	CSiB_EXP_GPiOS	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_SPiO_CLK	WKUP_GPIO0_54	WKUP_GPIO0_54	O	Bootmode	Active High	Select line for CPiLD's Mux
MCU_SPiO_D0	WKUP_GPIO0_55	USER_LED1	O	Bootmode	Active High	User LED
MCU_SPiO_D1	WKUP_GPIO0_69	SYS_MCU_PWRDN	O	Bootmode	Active High	System Power Down ('0' - normal operation '1' - system power down)
MCU_SPiO_CS0	WKUP_GPIO0_70	WKUP_GPIO0_70	IO	NA	NA	GPIO signal for FPC camera Connector
WKUP_GPIO0_10	WKUP_GPIO0_10	HDMI_LS_OE	O	PU	Active High	Level Shifter Output Enable for HDMI
WKUP_GPIO0_14	WKUP_GPIO0_14	HDMI_PdN	O	Bootmode	Active Low	Power Down Signal for HDMI
WKUP_GPIO0_49	WKUP_GPIO0_49	WKUP_GPIO0_49	IO	NA	NA	GPIO signal for 40 pin Expansion Header
PMiC_POWER_EN1	WKUP_GPIO0_88	WKUP_GPIO0_88	IO	NA	NA	GPIO signal for FPC camera Connector
WKUP_GPIO0_56	WKUP_GPIO0_56	WKUP_GPIO0_56	IO	NA	NA	GPIO signal for 40 pin Expansion Header
WKUP_GPIO0_57	WKUP_GPIO0_57	WKUP_GPIO0_57	IO	NA	NA	GPIO signal for 40 pin Expansion Header
MCU_ADCL_AiN0	WKUP_GPIO0_79	SOC_INT1z	I	PU	Active Low	Test Automation INT signal
MCU_ADCL_AiN1	WKUP_GPIO0_80	SOC_INT2z	I	PU	Active Low	Test Automation INT signal
MCU_ADCL_AiN2	WKUP_GPIO0_81	MCU_RGMiI_INT#	I	PU	Active Low	Interrupt Signal from RGMiI
MCU_ADCL_AiN3	WKUP_GPIO0_82	SOC_WAKE	I	PU	Active High	SOC wake signal from Reset Button
MCU_ADCL_AiN4	WKUP_GPIO0_83	PMiC_INTn	I	PU	Active Low	PMiC Interrupt signal
MCU_ADCL_AiN5	WKUP_GPIO0_84	ENET1_EXP_INTB	I	NA	NA	Interrupt Signal from ENET Expansion Header
MCU_ADCL_AiN6	WKUP_GPIO0_85	IO_EXP_I2C0_INTB	O	NA	NA	I2C0 Interrupt Signal to ENET Expansion Header
WKUP_GPIO0_66	WKUP_GPIO0_66	WKUP_GPIO0_66	IO	PU	NA	GPIO signal for 40 pin Expansion Header
WKUP_GPIO0_67	WKUP_GPIO0_67	WKUP_GPIO0_67	IO	NA	NA	GPIO signal for 40 pin Expansion Header
Main Domain						
EXTINTn	GPIO0_0	HDMI_HPD	I	NA	Active High	HDMI hot plug detect signal
MCAN13_TX	GPIO0_3	GPIO0_3	IO	NA	NA	GPIO signal for 40 pin Expansion Header
MCAN13_RX	GPIO0_4	DP0_3V3_EN	O	PD	Active High	Enable signal for Display port Current Limiter
MCAN1_TX	GPIO0_27	GPIO0_27	IO	NA	NA	GPIO signal for 40 pin Expansion Header
MCASPO_AXR8	GPIO0_36	GPIO0_36	IO	NA	NA	GPIO signal for 40 pin Expansion Header
ECAP0_IN_APWM_OUT	GPIO0_49	SEL_SDIO_3V3_1V8n	O	PU	Active Low	One of Enable signal for VDD_SD_DV
GPIO Expander						
Port No	GPIO	I2C	Input/Output	Default	State	Usage
P0	CSI_ViO_SEL	MAIN_I2C1 Address : 0x21 Part No - TCA6408ARGTR	O	PD	Active High	Enable signal for Camera IO supply
P1	CSI_MUX_SEL_2		O	PD	Active High	Select lines for CSI mux
P2	CSI2_RSTz		O	PD	Active Low	Reset signal for CSI Expansion Connector
P3	IO_EXP_CAM0_GPiO1		IO	NA	NA	GPIO signals for FPC Camera Connector
P4	IO_EXP_CAM1_GPiO1		IO	NA	NA	GPIO signals for FPC Camera Connector
P00	BOARDID_EEPROM_WP	MAIN_I2C0 Address : 0x21 Part No - TCA6408ARGTR	O	PD	Active High	Board ID EEPROM Write Protect
P01	CAN_STB		O	PD	Active High	Stand By Input for CAN Transceiver
P02	GPIO_uSD_PWR_EN		O	PU	Active High	One of Enable signal for Micro SD Load Switch
P03	IO_EXP_MCU_RGMiI_RST#		O	NA	Active Low	MCU_RGMiI Resetz signal to CPiLD
P04	IO_EXP_PCiE0_4L_PERST#		O	NA	Active Low	PCiE 4 lane Resetz signal to CPiLD
P05	IO_EXP_PCiE1_M2_RTSz		O	NA	Active Low	PCiE M Key Resetz signal to CPiLD
P06	IO_EXP_PCiE3_M2_RTSz		O	NA	Active Low	PCiE E Key Resetz signal to CPiLD
P07	PM_INA_BUS_EN		O	PU	Active High	Enable signal for PM2 I2C lines
P10	ENET1_EXP_PWRDN		O	PU	Active High	Power Down Signal for Enet Expansion Header
P11	EXP1_ENET_RSTz		O	NA	Active Low	Reset Signal for Enet Expansion Header
P12	ENET1_I2CMUX_SEL		O	NA	Active High	I2C mux select Signal for Enet Expansion Header
P13	PCiE0_CLKREQ#		I	PU	Active Low	PCiE Card Clock request Signal
P14	PCiE1_M2_CLKREQ#		I	PU	Active Low	PCiE M Key Clock request Signal
P15	PCiE3_M2_CLKREQ#		I	PU	Active Low	PCiE E Key Clock request Signal
P16	CDCl1_OE2/OE3		IO	PU	NA	GPIO signal CDCl Clock Generator
P17	CDCl1_OE1/OE4		IO	PU	NA	Output Enable for CDCl Clock Generator
P0	SW_CPiLD_CONTROL_IN1	TEST AUTOMATION I2C Address : 0x20 Part No - TCA6408ARGTR	O	NA	NA	CPiLD Switch Control Signals for Bootmode Logic
P1	SW_CPiLD_CONTROL_IN2		O	NA	NA	CPiLD Switch Control Signals for Bootmode Logic
P2	SW_CPiLD_CONTROL_IN3		O	NA	NA	CPiLD Switch Control Signals for Bootmode Logic
P3	SW_CPiLD_CONTROL_IN4		O	NA	NA	CPiLD Switch Control Signals for Bootmode Logic



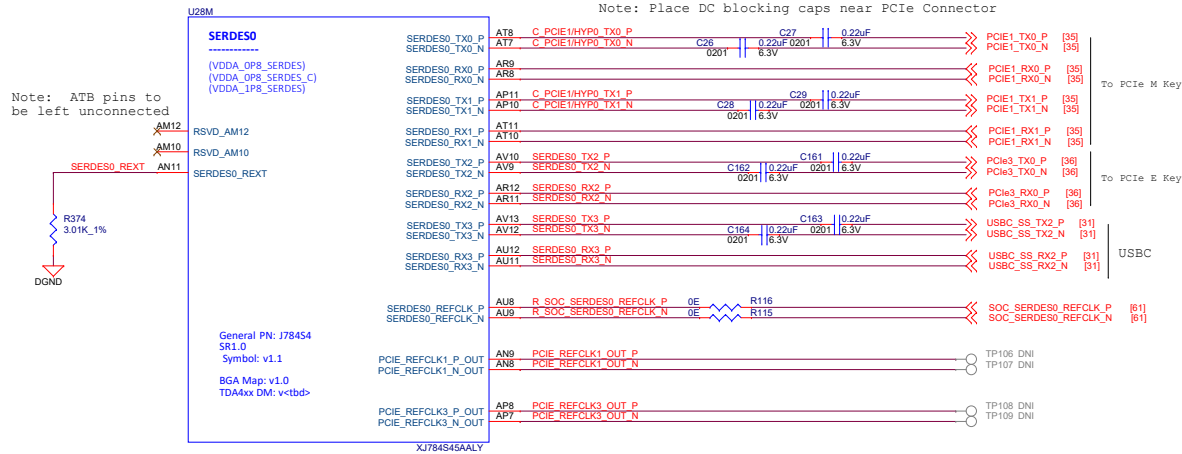
# DSI



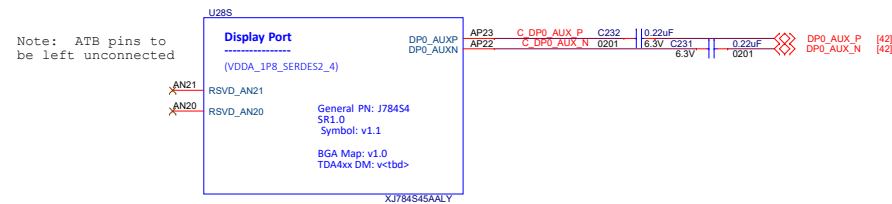
# CSI



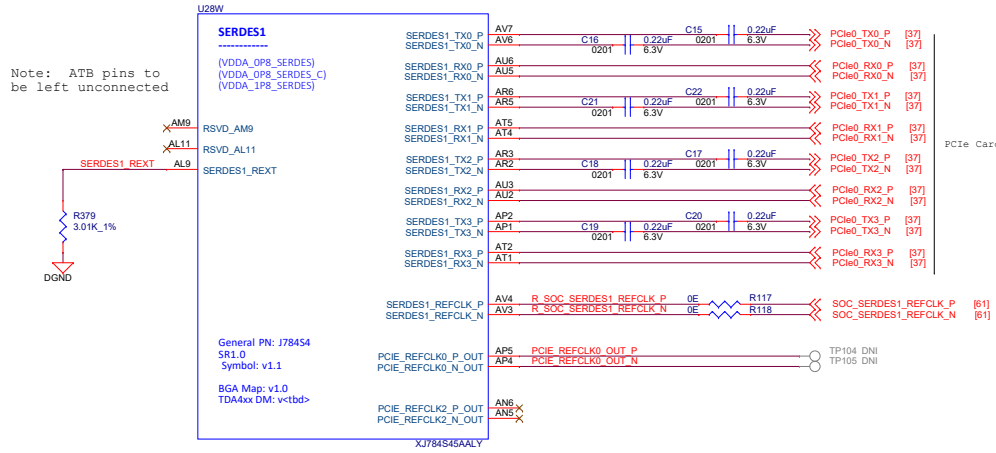
# SERDES0



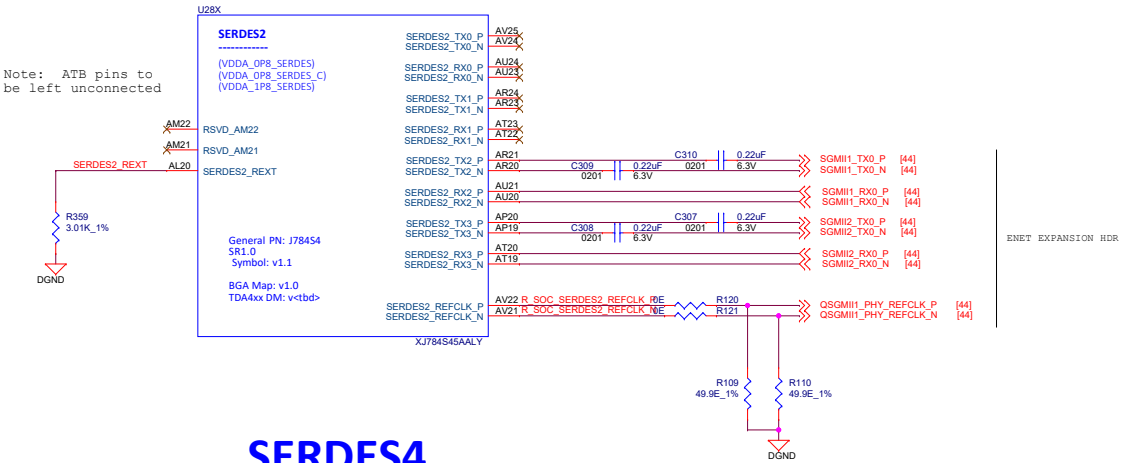
# DP\_AUX



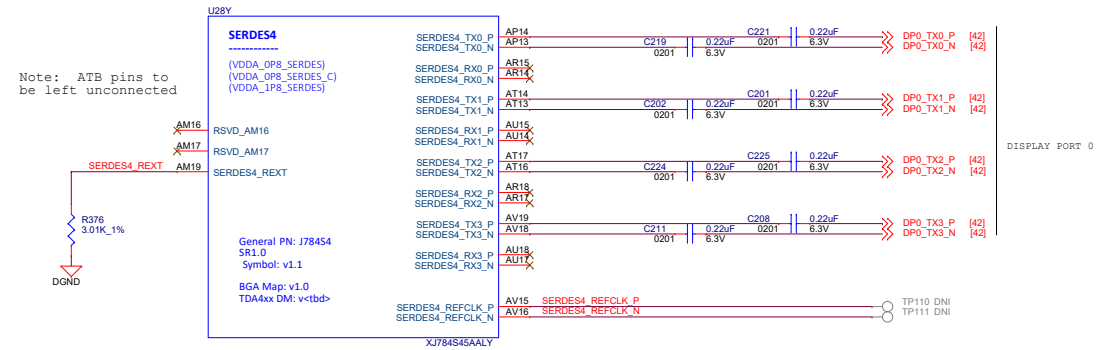
# SERDES1



# SERDES2



# SERDES4



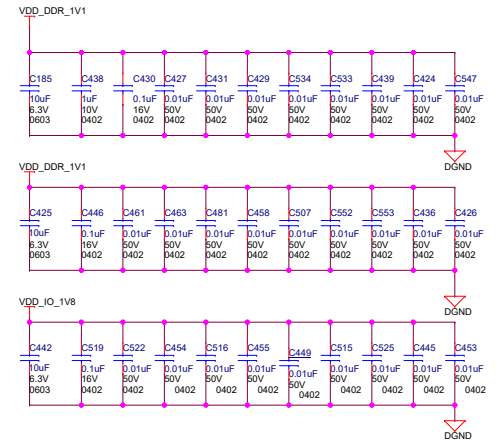
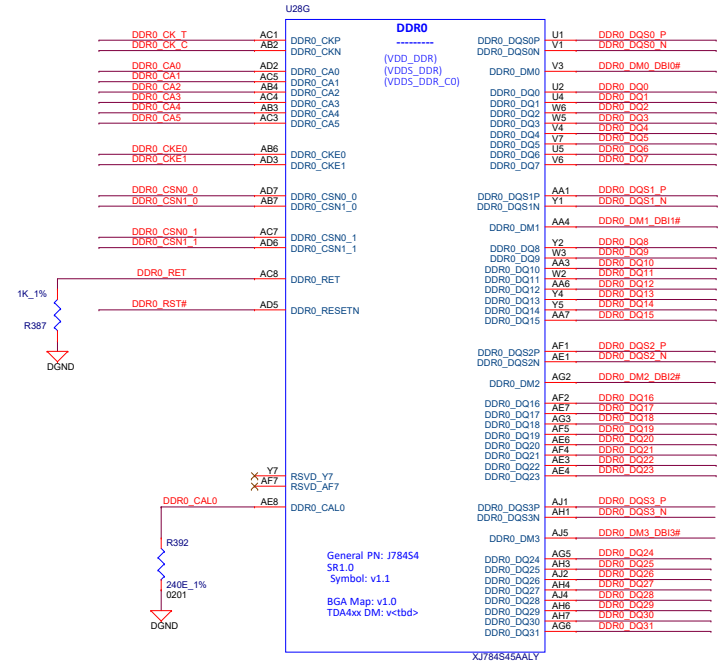
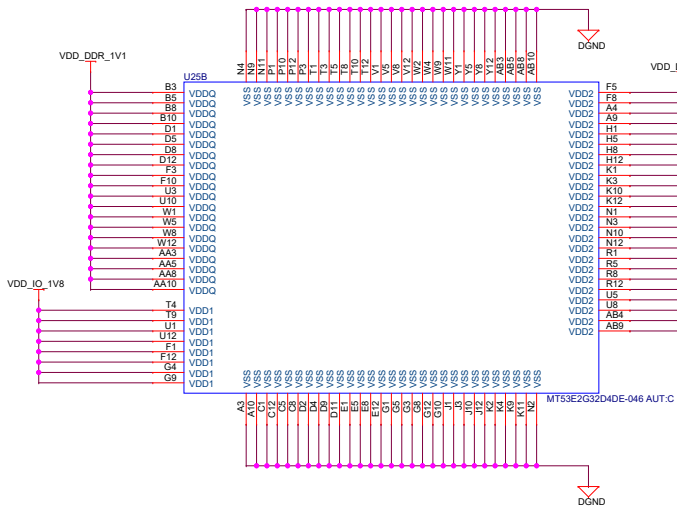
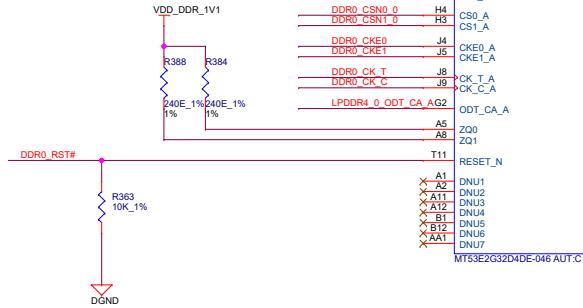
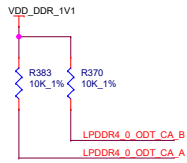
Project :  
AM69 Edge AI Kit



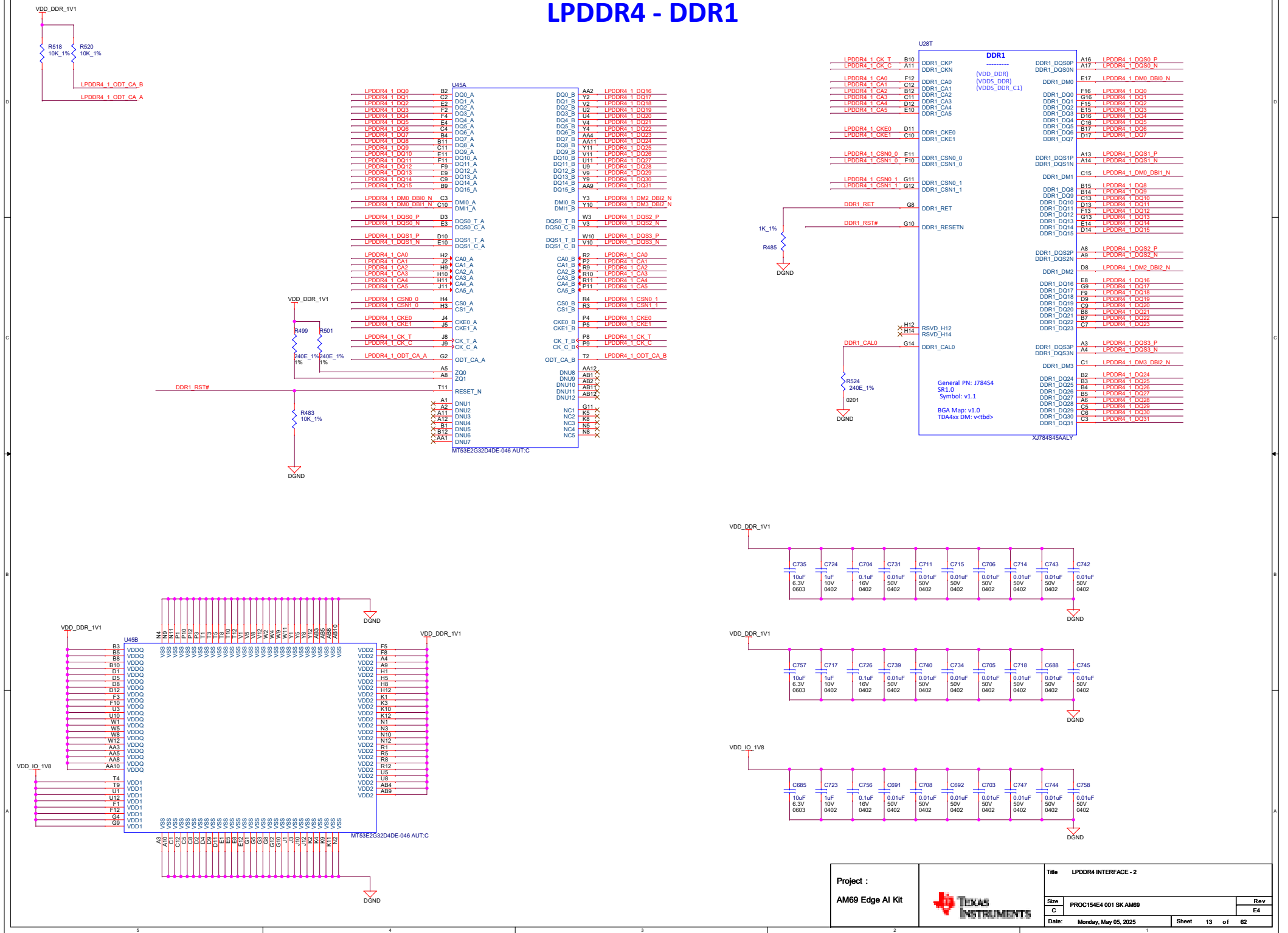
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Size	PROC154E4 001 SK AM69	R
C		E
Date:	Monday, May 05, 2025	Sheet 11 of 62

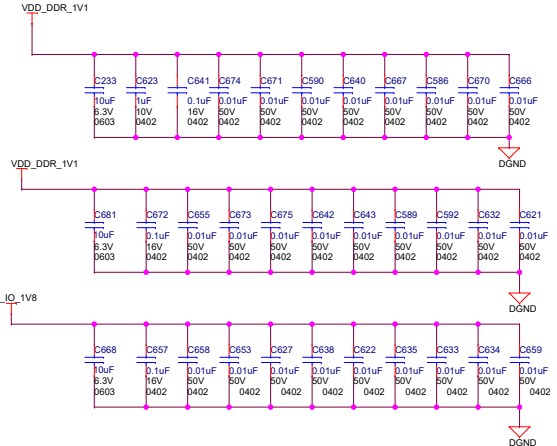
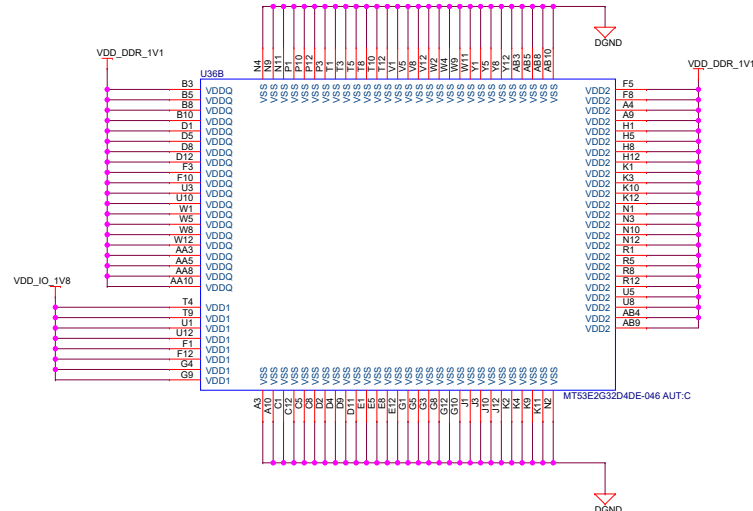
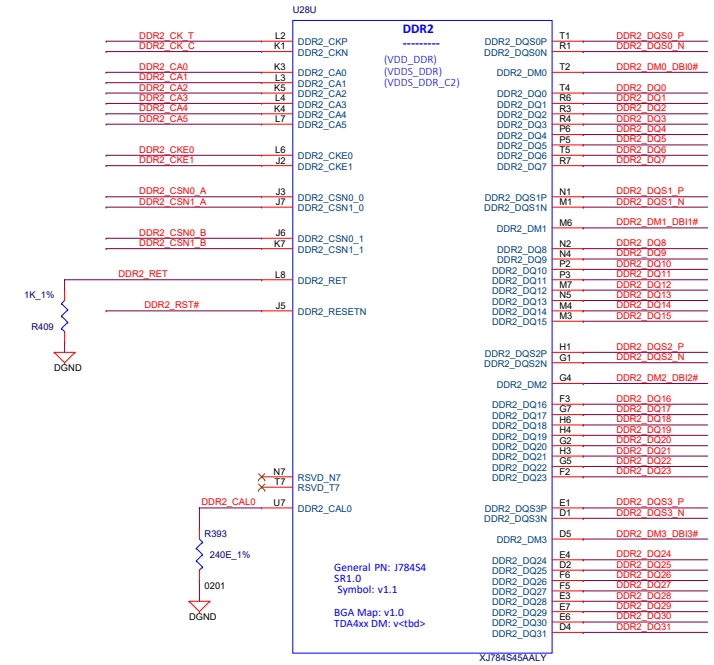
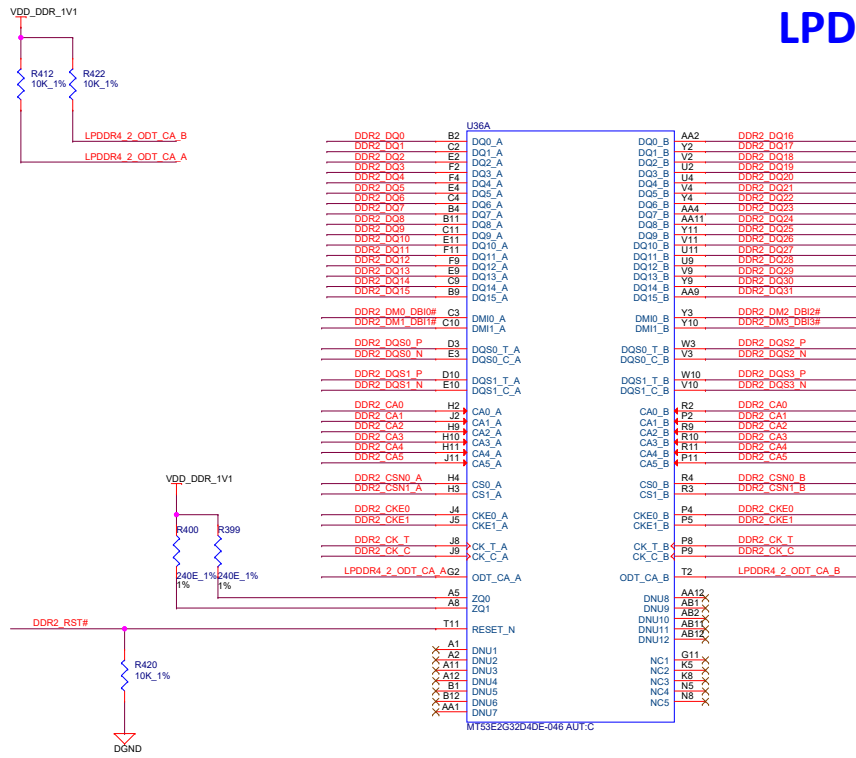
## LPDDR4 - DDR0



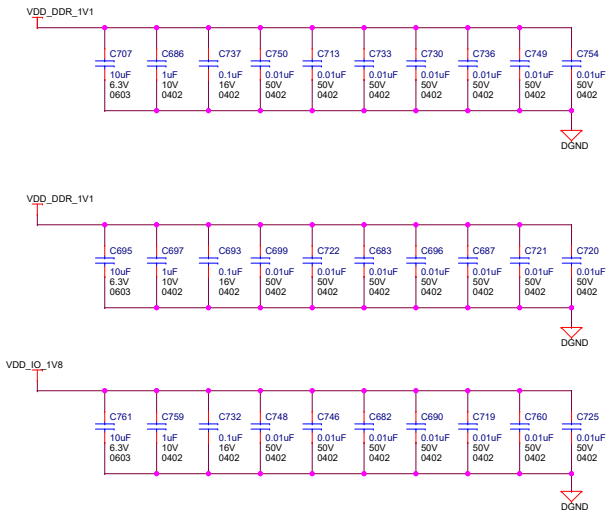
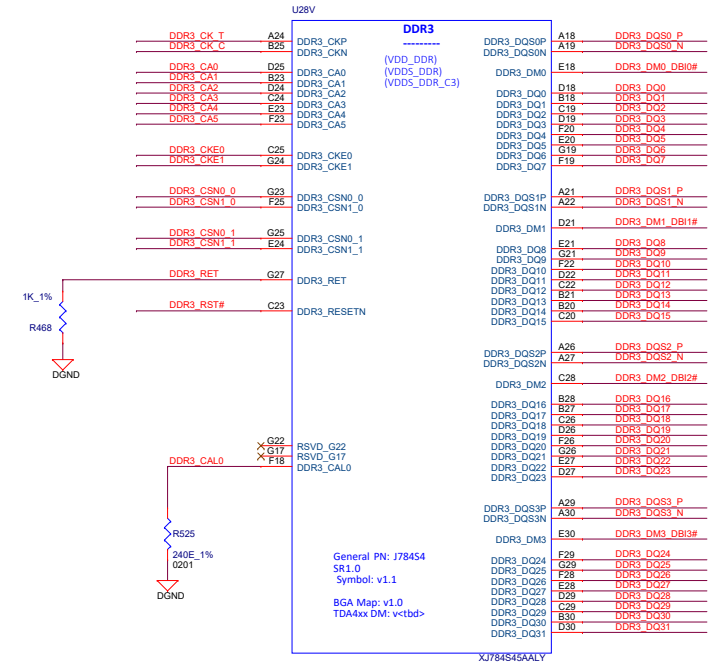
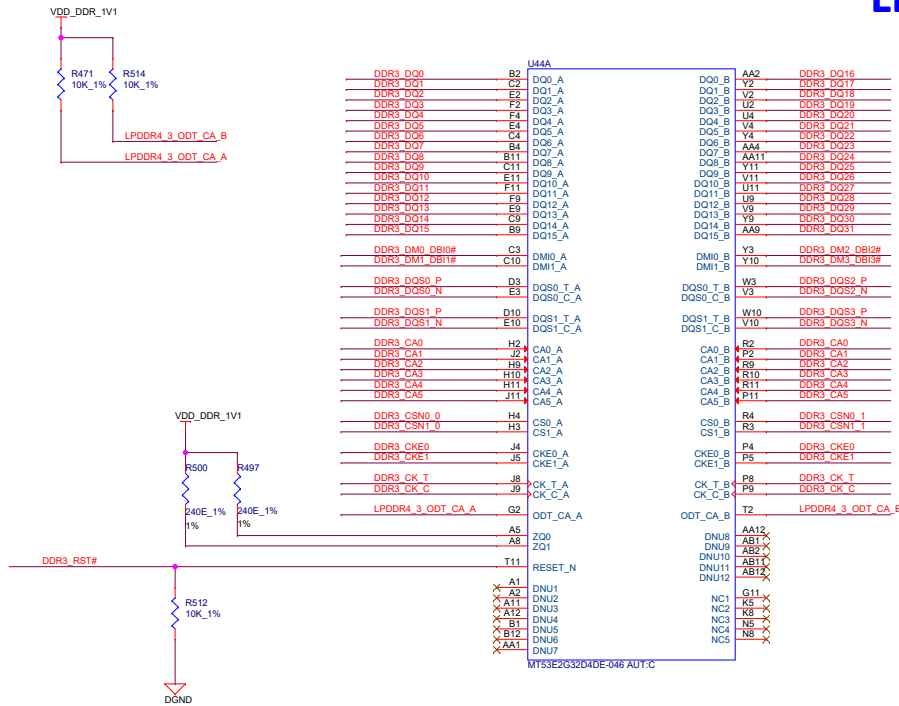
## LPDDR4 - DDR1



# LPDDR4 - DDR2

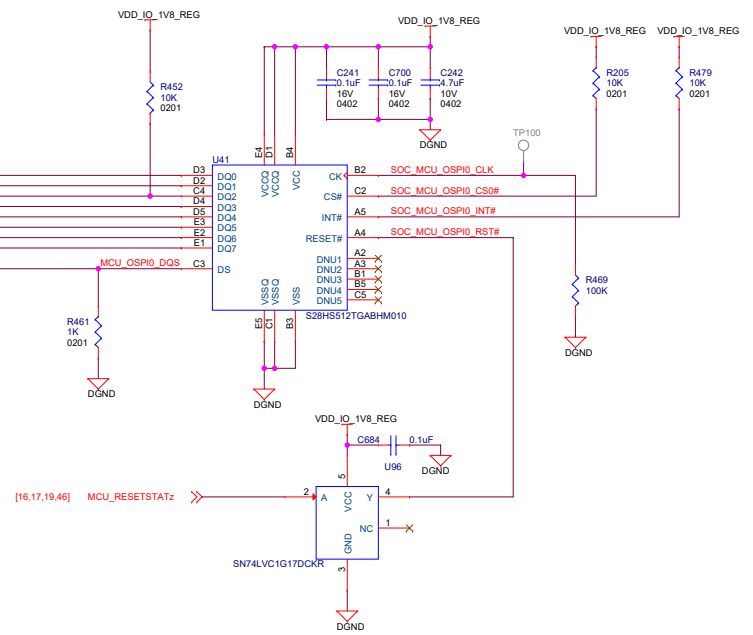
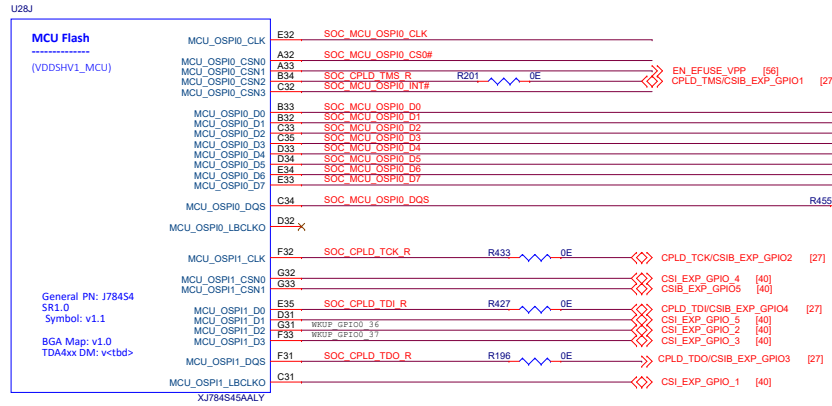


## LPDDR4 - DDR3



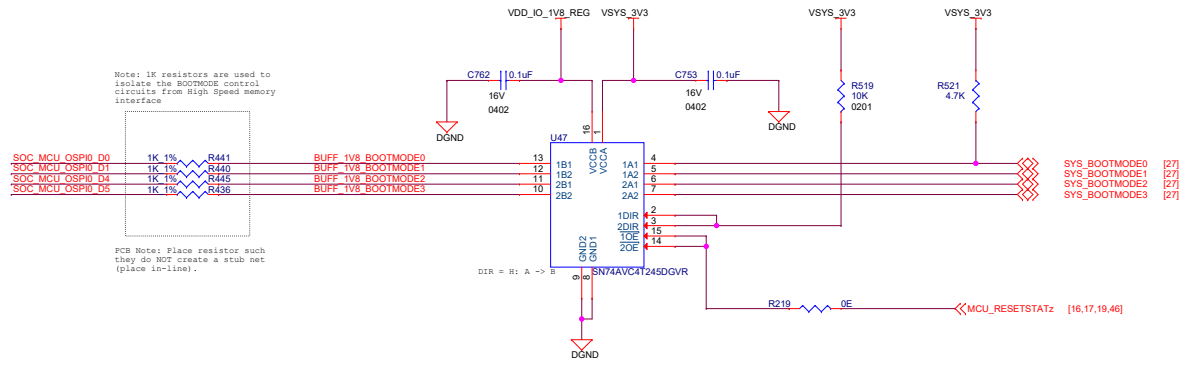
MCU FLASH

OSPI FLASH



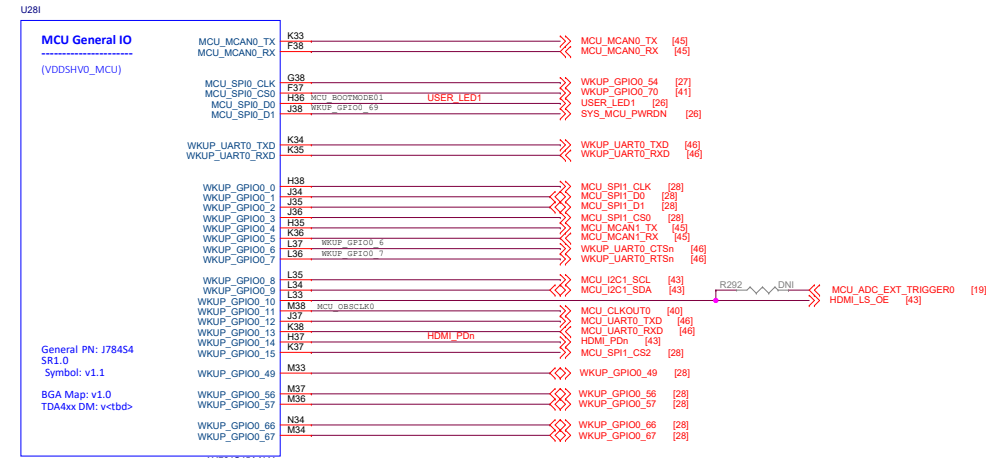
BOOTMODE Control Logic

Note: Logic used to configure BOOTMODE settings during reset. This is four (4) of a total of eighteen (18) boot pins. Specific value is user configured (dip switch).

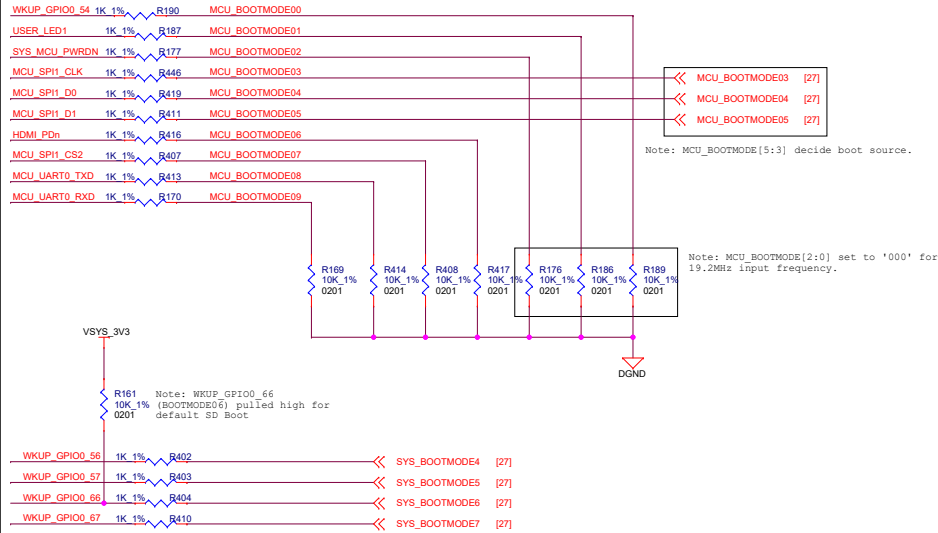




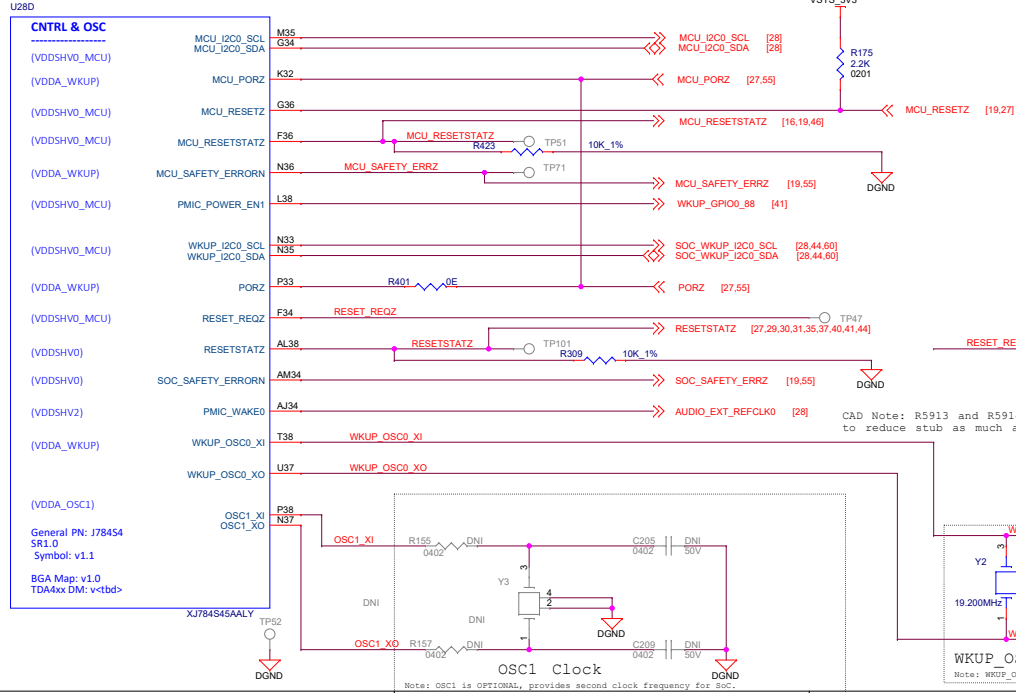
MCU & MAIN GENERAL IO, OSC CLKS



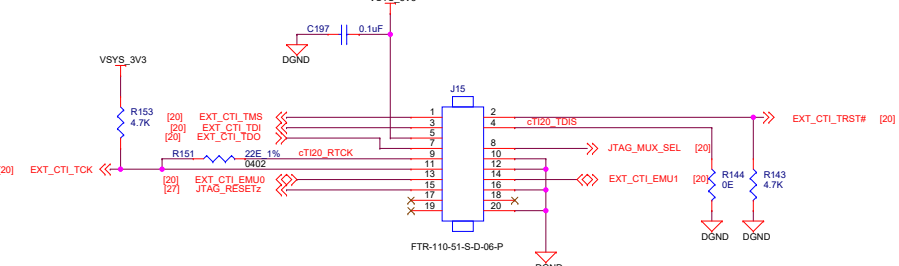
BOOTMODE



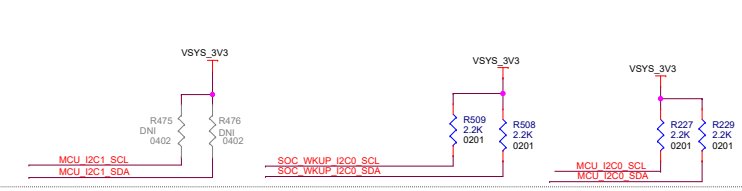
CONTROL & OSC



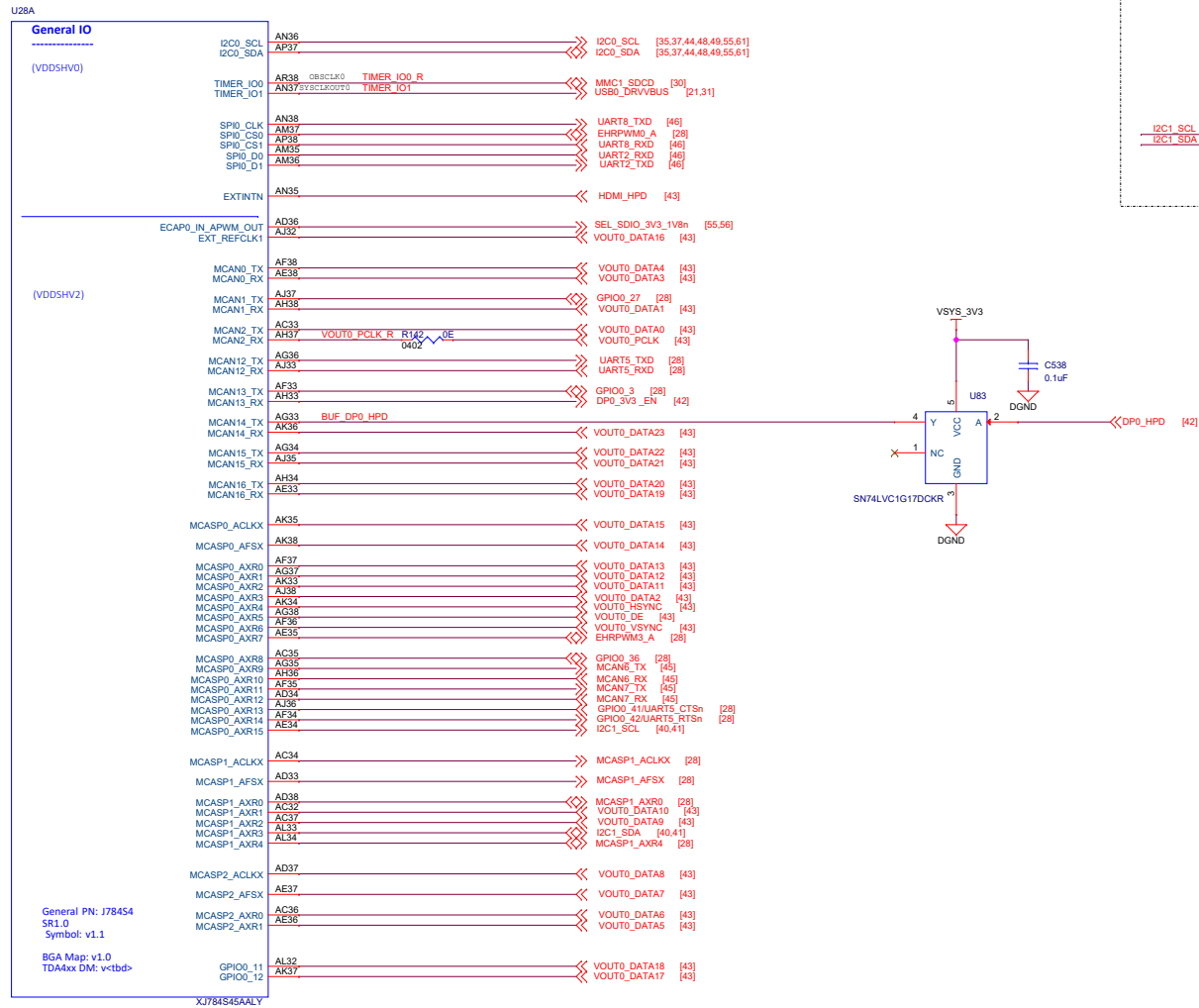
cTI 20PIN JTAG HEADER



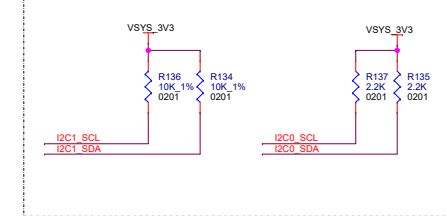
MCU/WKUP I2C Pull-ups



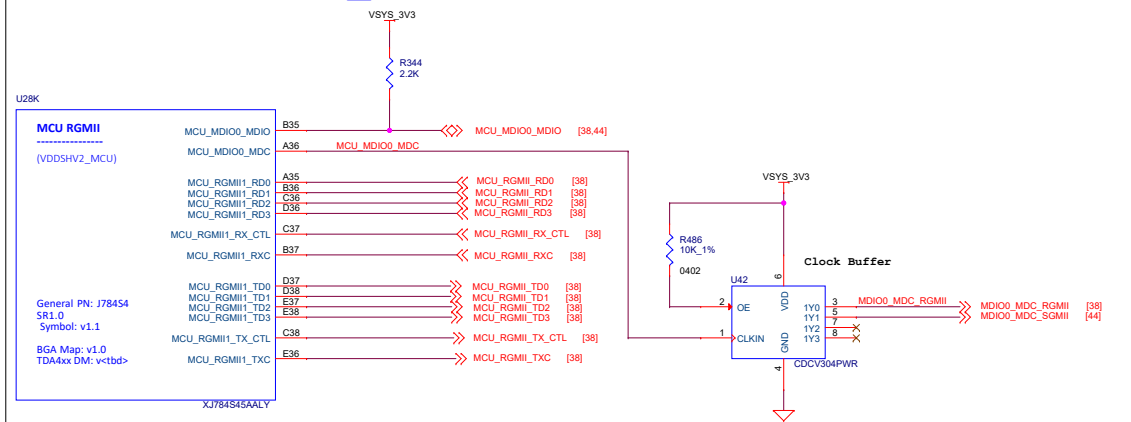
# GENERAL IO



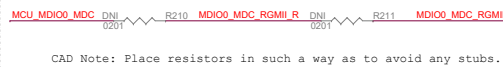
I2C Pull Ups



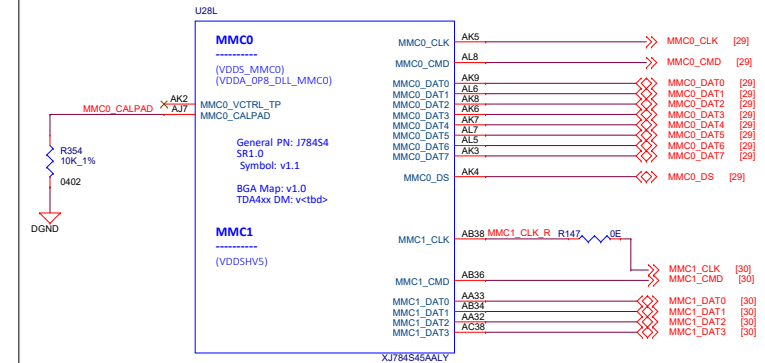
## MCU\_RGMII



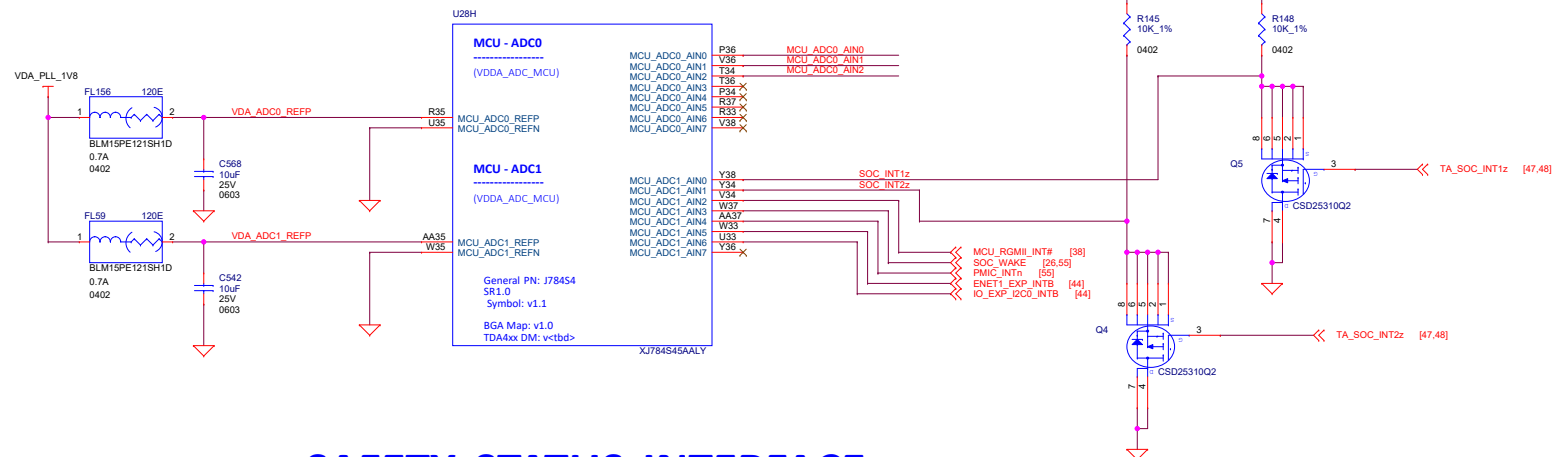
```
Resistor option to bypass clock buffer.
```



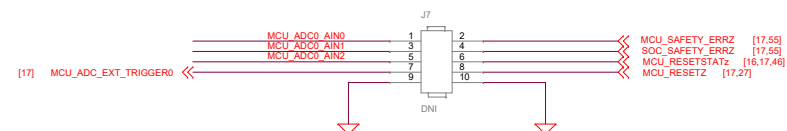
## MMC0 and MMC1



## MCU\_ADC



## SAFETY STATUS INTERFACE



Project :  
AM69 Edge AI Kit



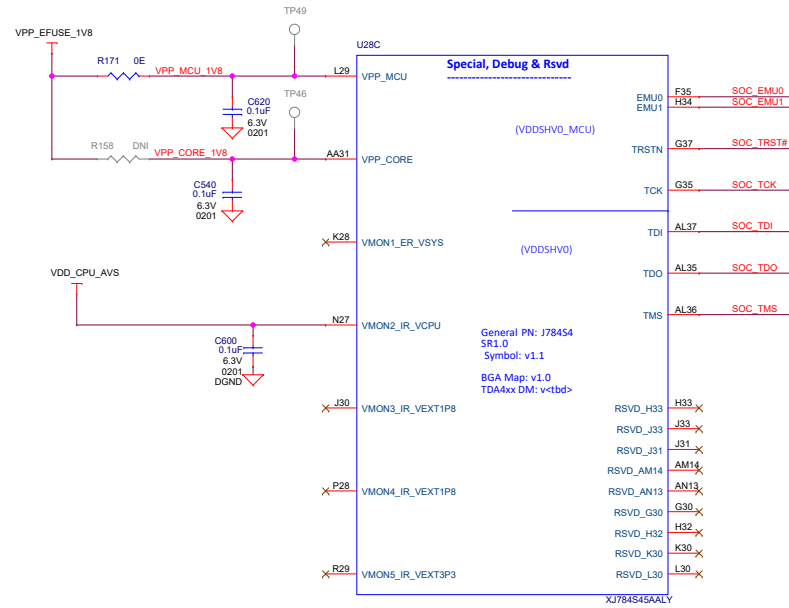
Title	SOC - MCU RGMII / MMC[0:1] / MCU ADC
-------	--------------------------------------

Size	DDG45454.001 SK AM30
------	----------------------

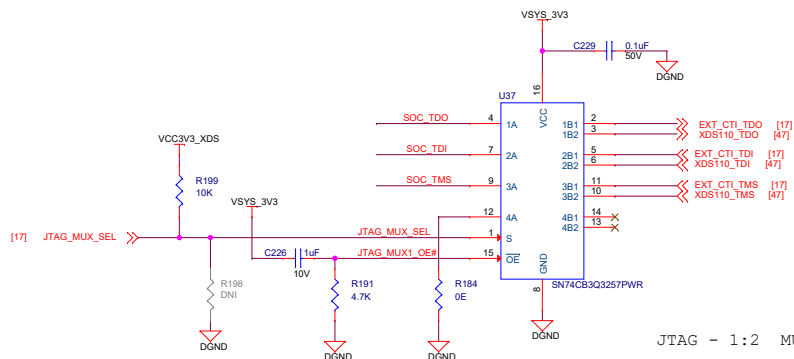
C	PROC154E4 001 SK AM69
---	-----------------------

Date: Monday, May 05, 2025	Sheet 19 of 62
----------------------------	----------------

## SPECIAL, DEBUG & RSVD

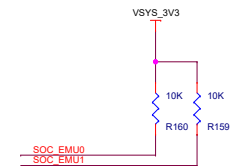
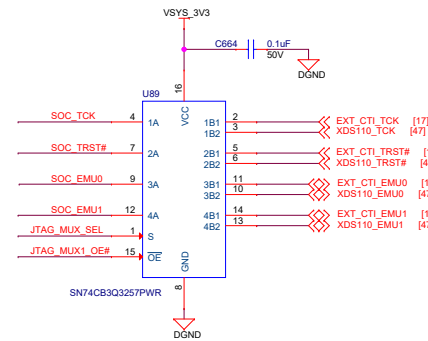


## JTAG CONNECTOR AND XDS110 MUX



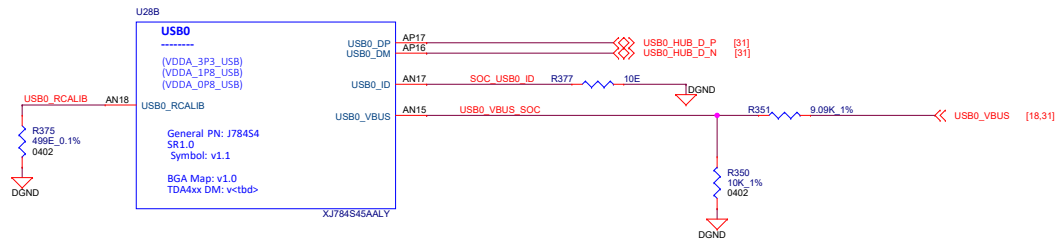
JTAG - 1:2 MUX : Truth Table

MUX_SEL	CONDITION	FUNCTION
LOW	External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU] (default)
HIGH	No External Emulator attached & XDS110 Powered via USB	A-->B2 port [ON Board EMU]

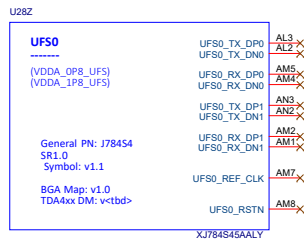


USB0 2.0

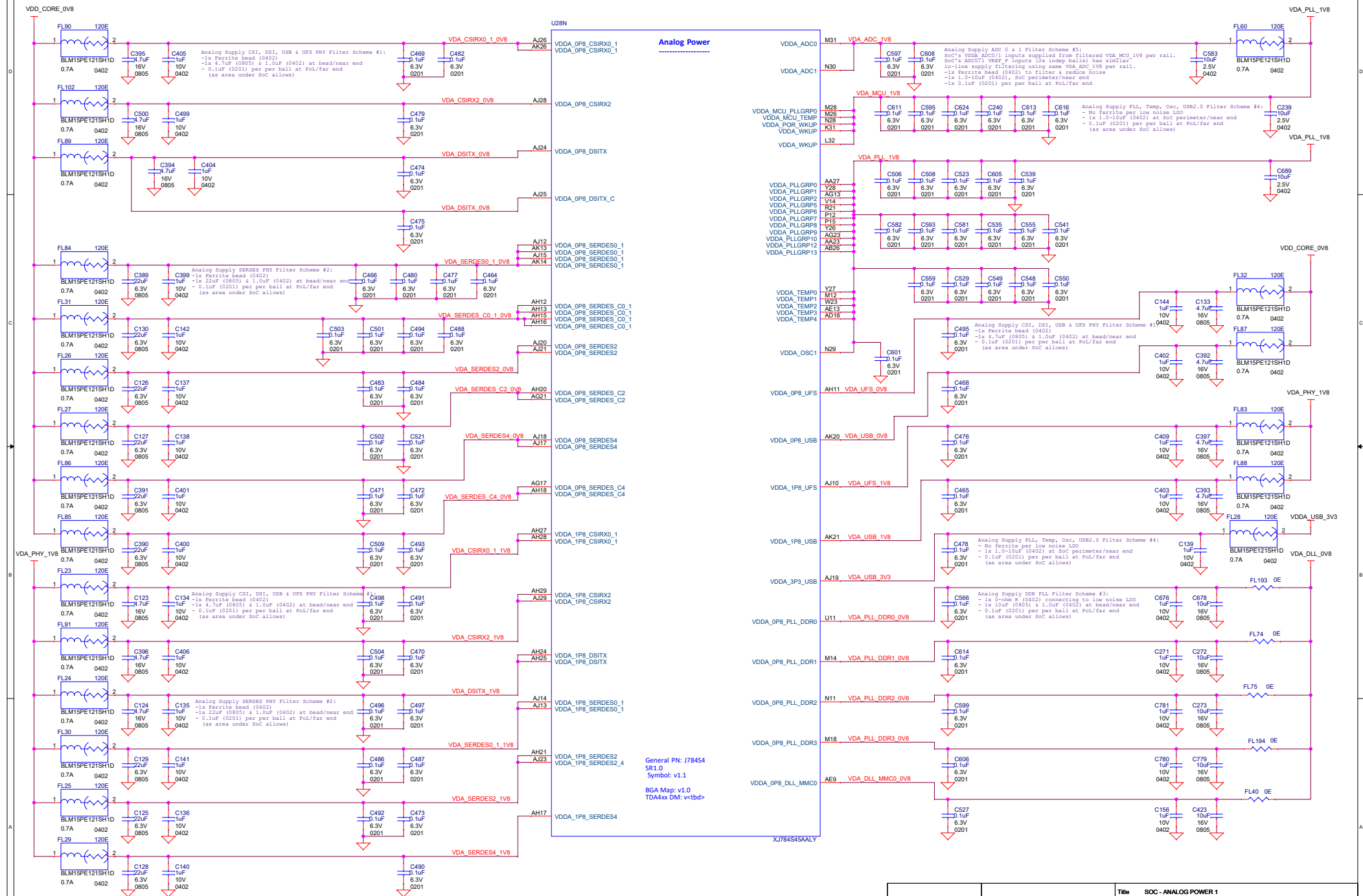
USB VBUS Resistor divider circuit



UFS FLASH



## ANALOG POWER 1



Project :

## AM69 Edge AI Kit



Title	SOC - ANALOG POWER 1
-------	----------------------

Size	DDG45454.001 SK AM30
------	----------------------

Date: Monday, May 05, 2025

Rev

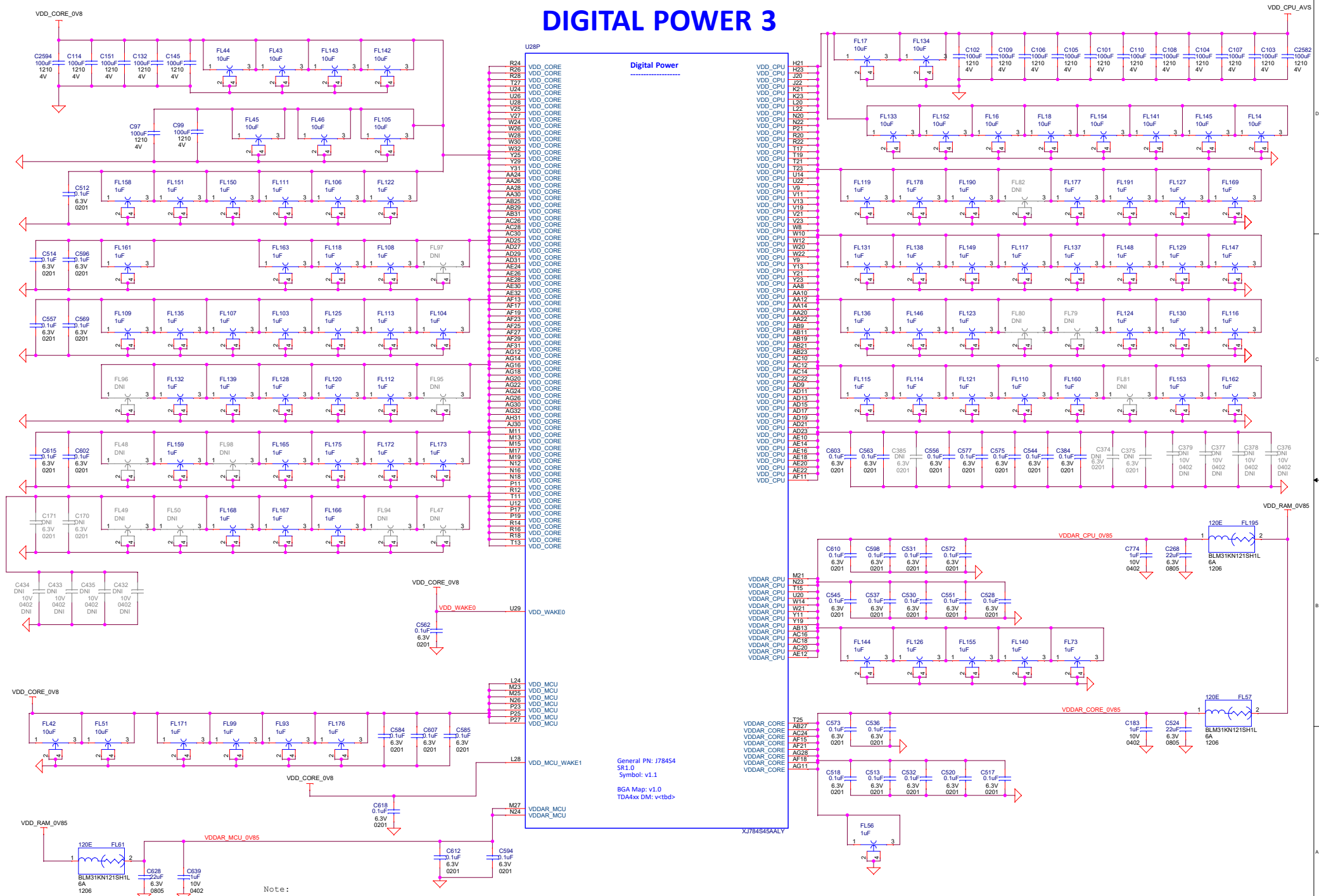
E4

## IO Power & Support



X.I784S45AAI Y

# DIGITAL POWER 3



Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this SK PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Project :

AM69 Edge AI Kit



Title	SOC - DIGITAL POWER 3
-------	-----------------------

Size	DDG45451.001 SK AN20
------	----------------------

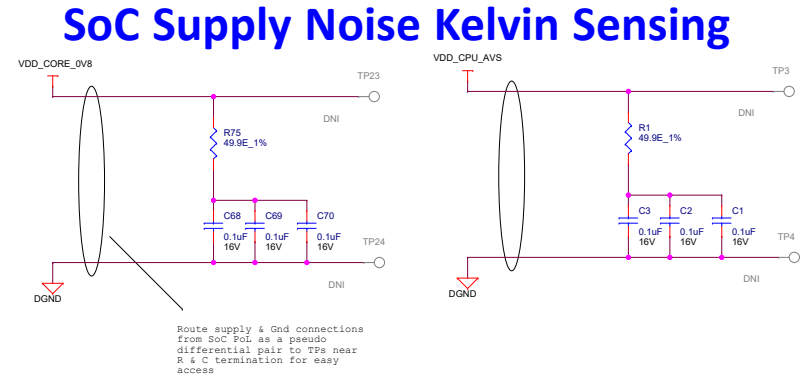
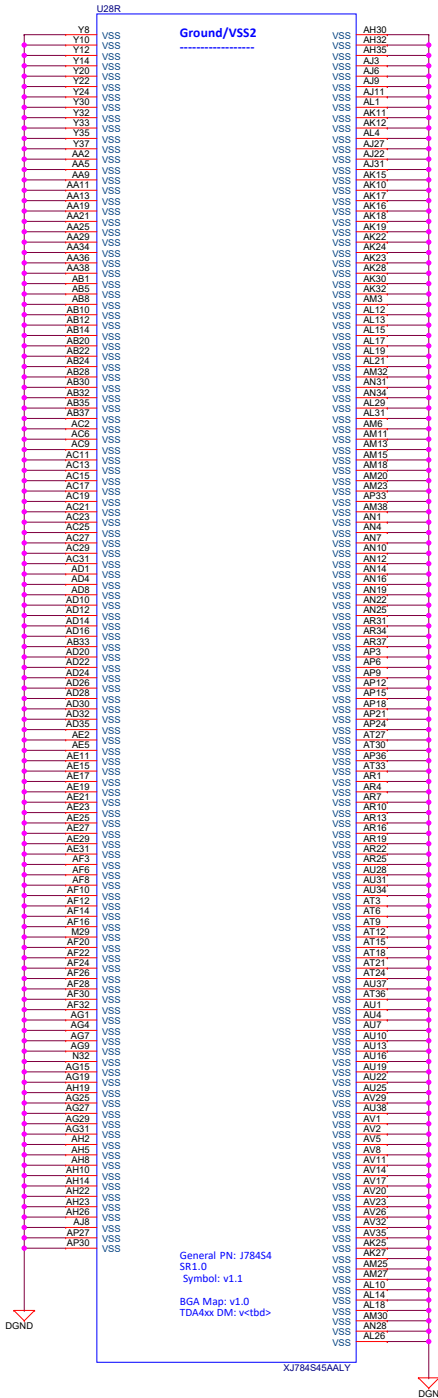
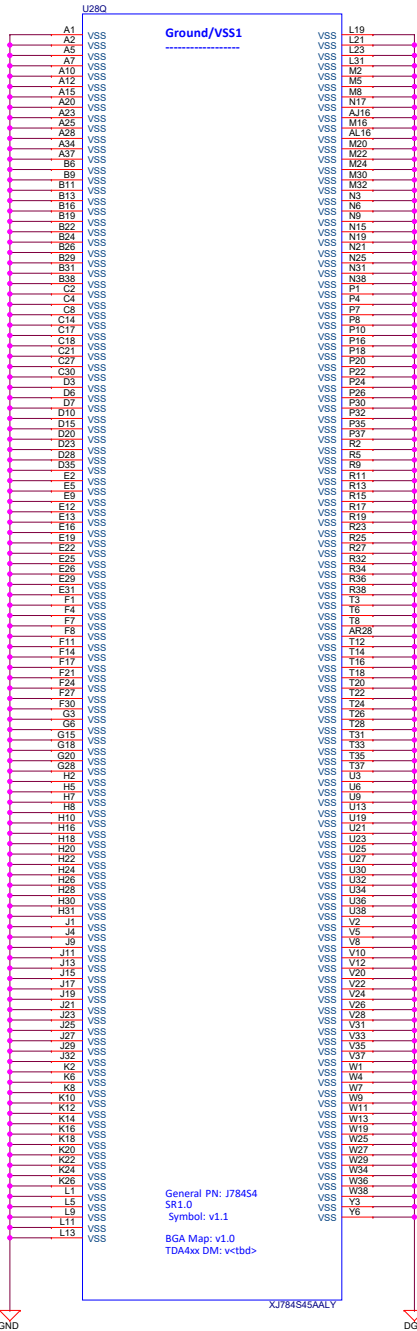
Date: Monday, May 05, 2025

Re

2

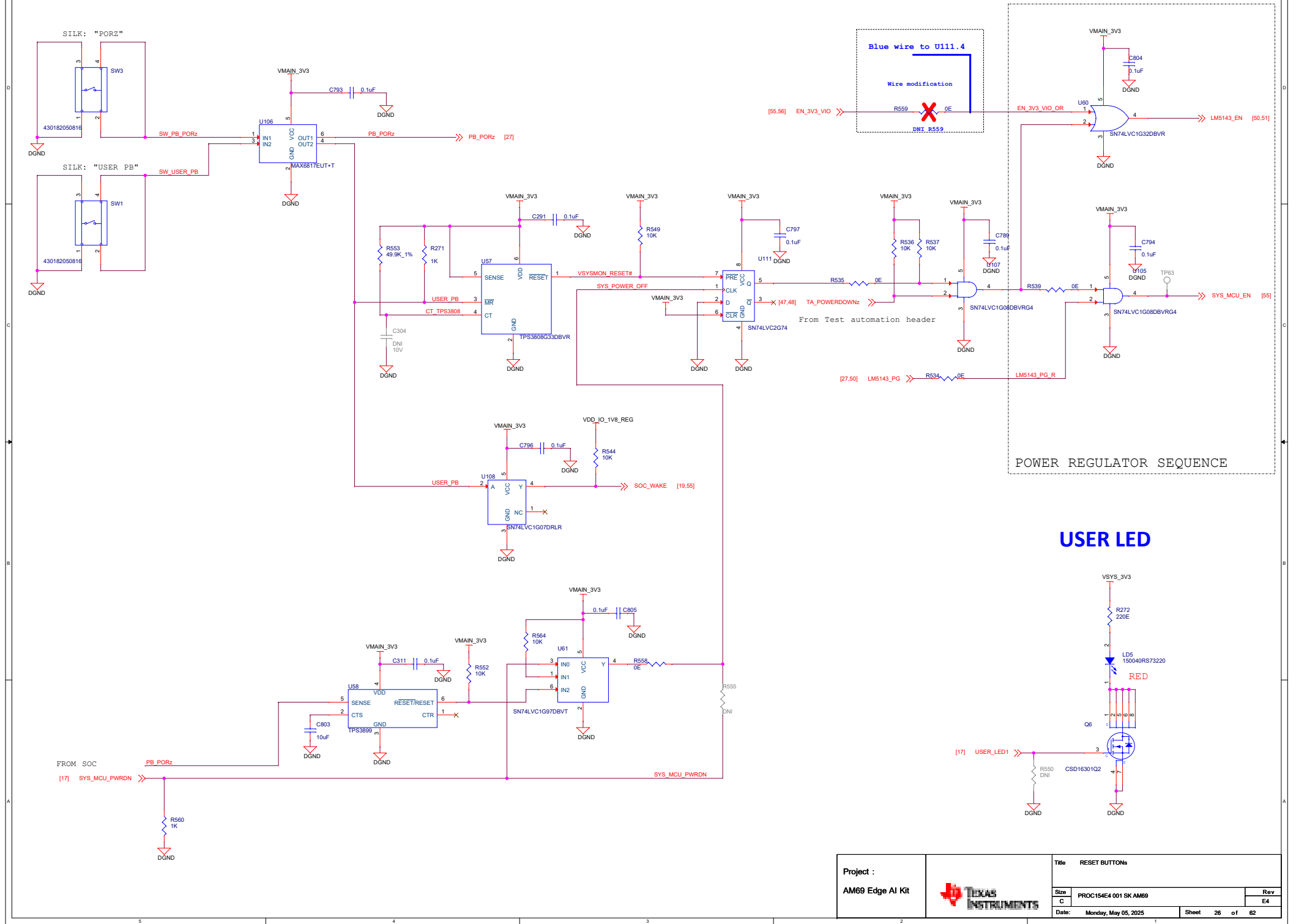


# SOC GROUND

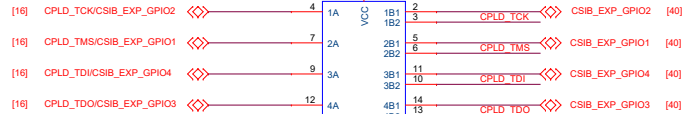
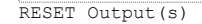


Project : AM69 Edge AI Kit		Title SOC - GROUND & KELVIN SENSING	
Rev E4		Size C	
Date: Monday, May 05, 2025		Sheet 25 of 62	

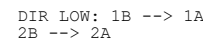
# RESET BUTTONs



Default termination on IOs is Pull down, when the CPLD is not programmed.

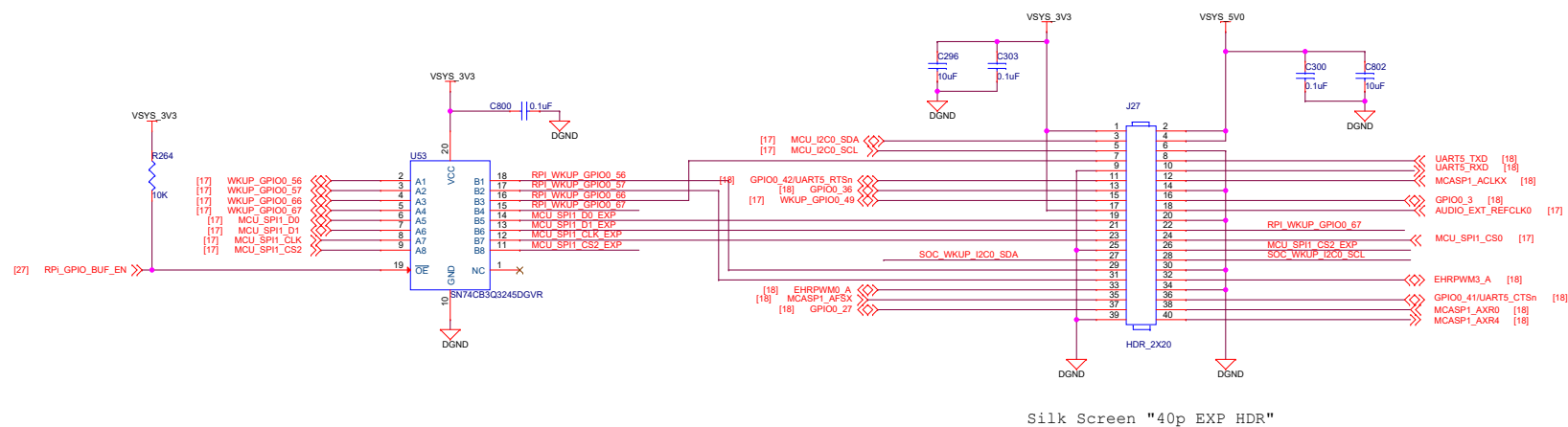



Note: Test Automation logic to set desired BOOTMODE.



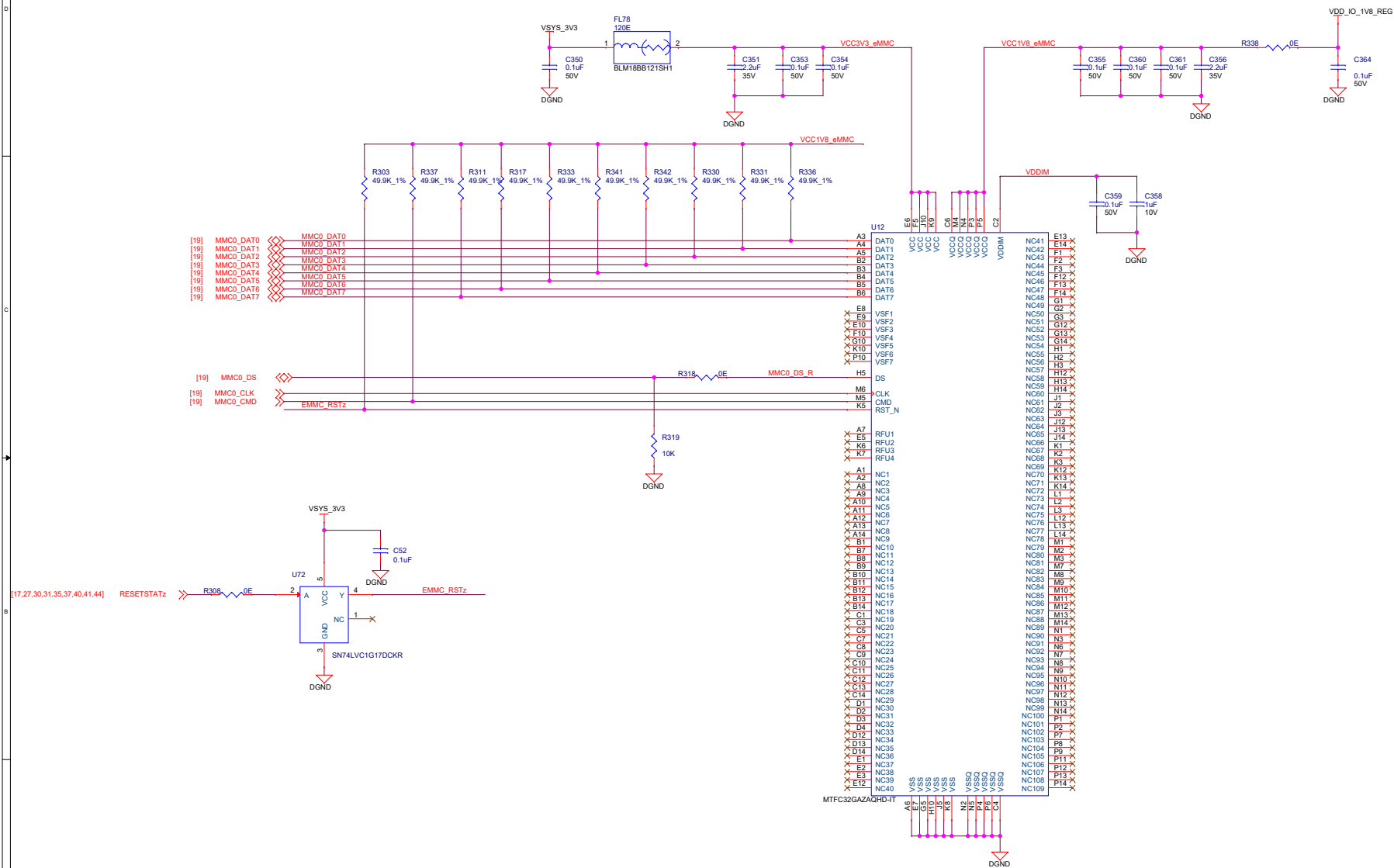
SW2.3	SW2.2	SW2.1	BOOTMODE
0	0	0	SD
0	0	1	NO Boot
0	1	0	Ethernet
0	1	1	USB
1	0	0	xSPI - 1S
1	0	1	UART
1	1	0	eMMC
1	1	1	xSPI SDFP

## 40Pin Expansion Header

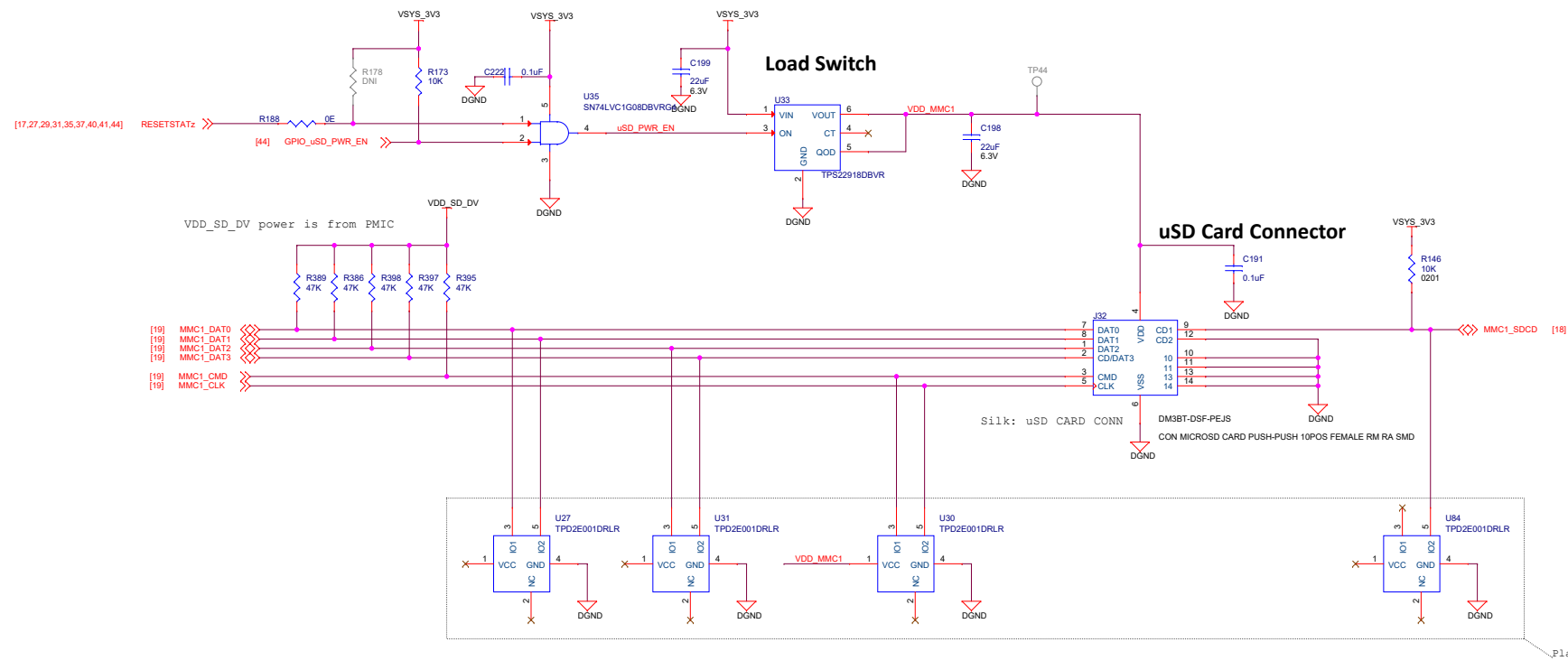


Project :  AM69 Edge AI Kit		Title BOARD ID EEPROM & 40 PIN EXP HEADER			
		Size C	PROC154E4 001 SK AM69	Rev	
				E4	
		Date: Monday, May 05, 2025		Sheet	28

## eMMC FLASH

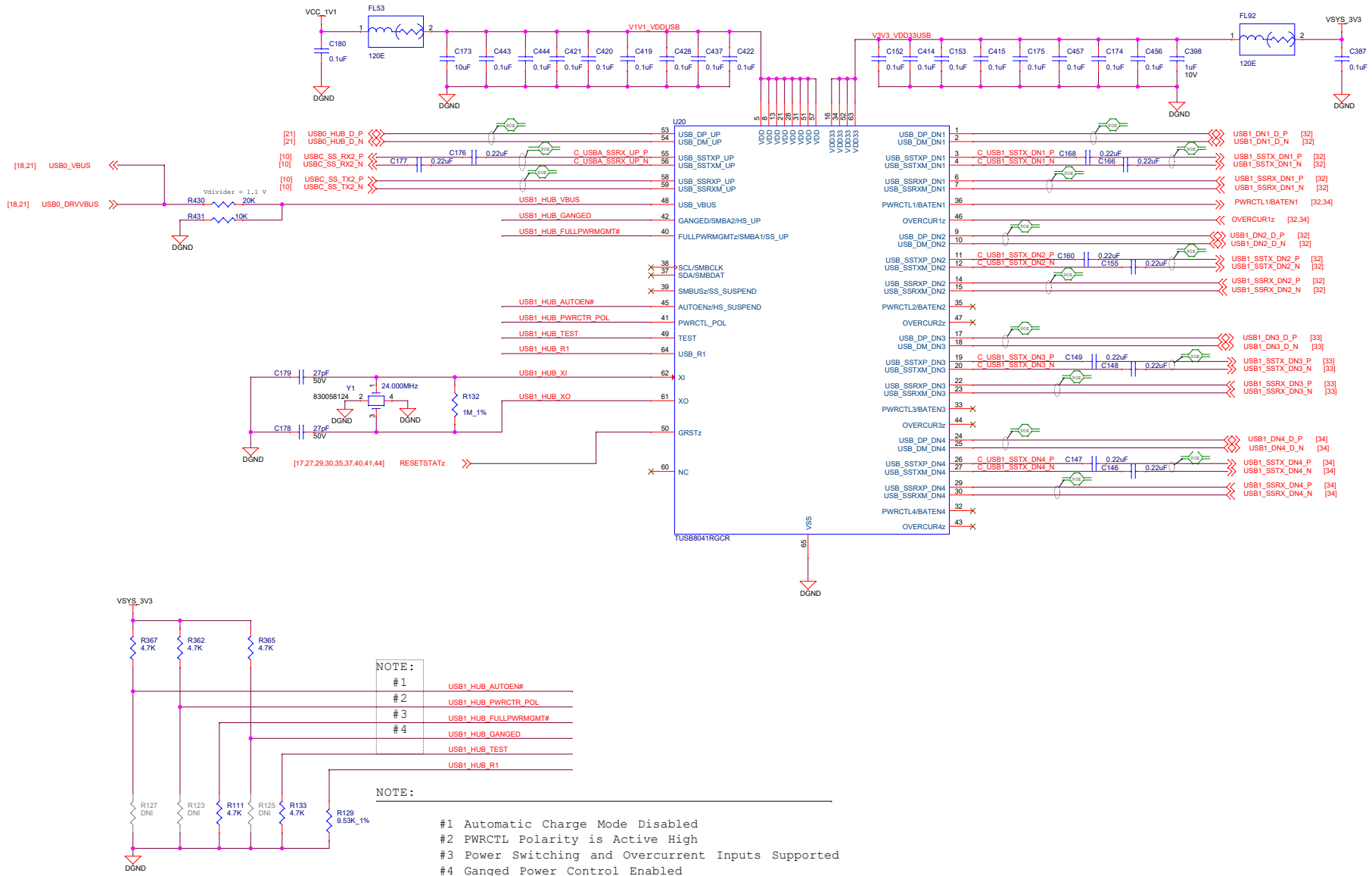


## Micro SD CARD INTERFACE

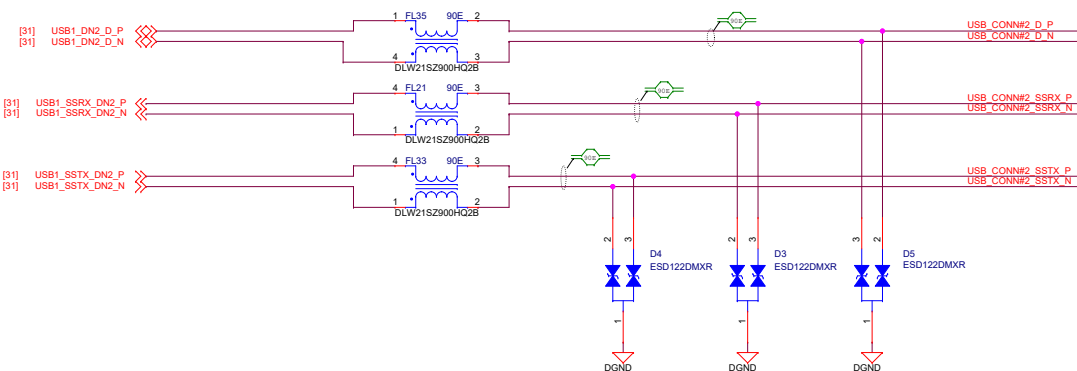
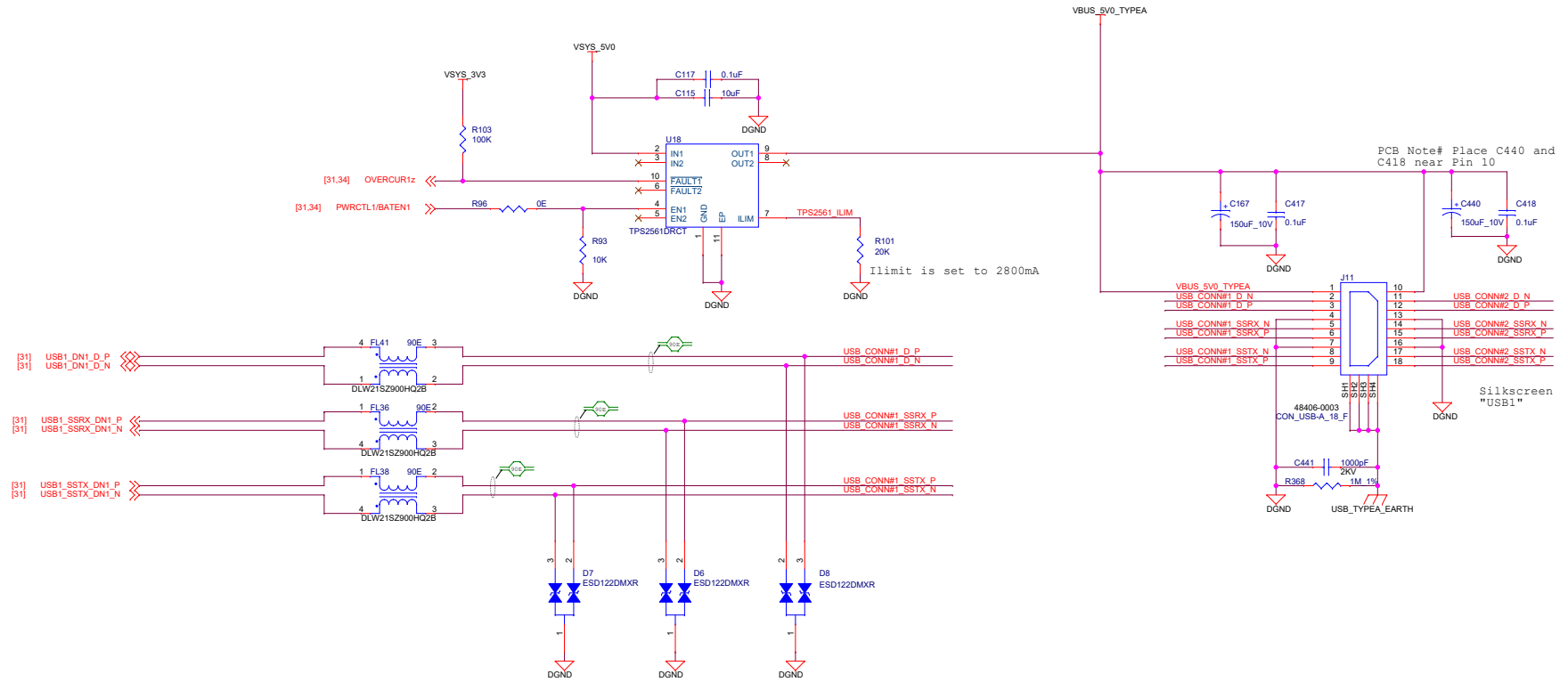


Place near SD Card Connector

# USB3.0 HUB

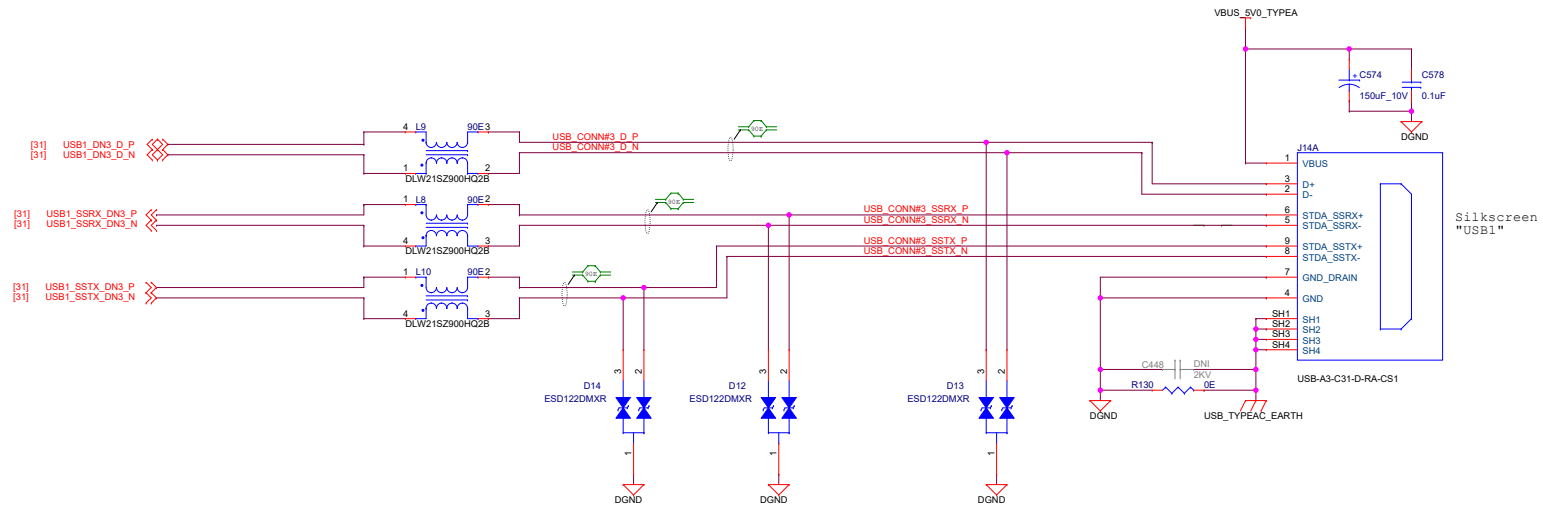


# USB 3.0 TYPE-A CONNECTORS - 1

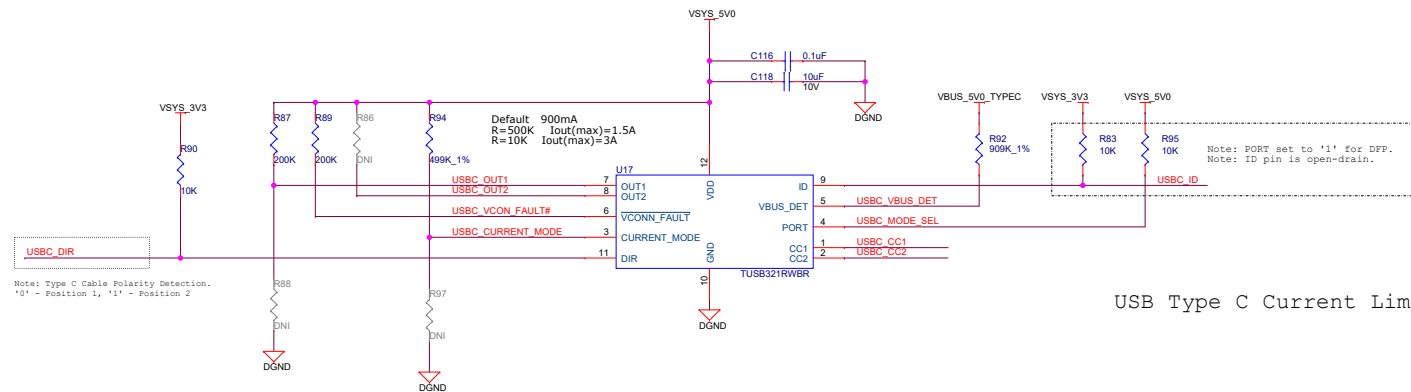




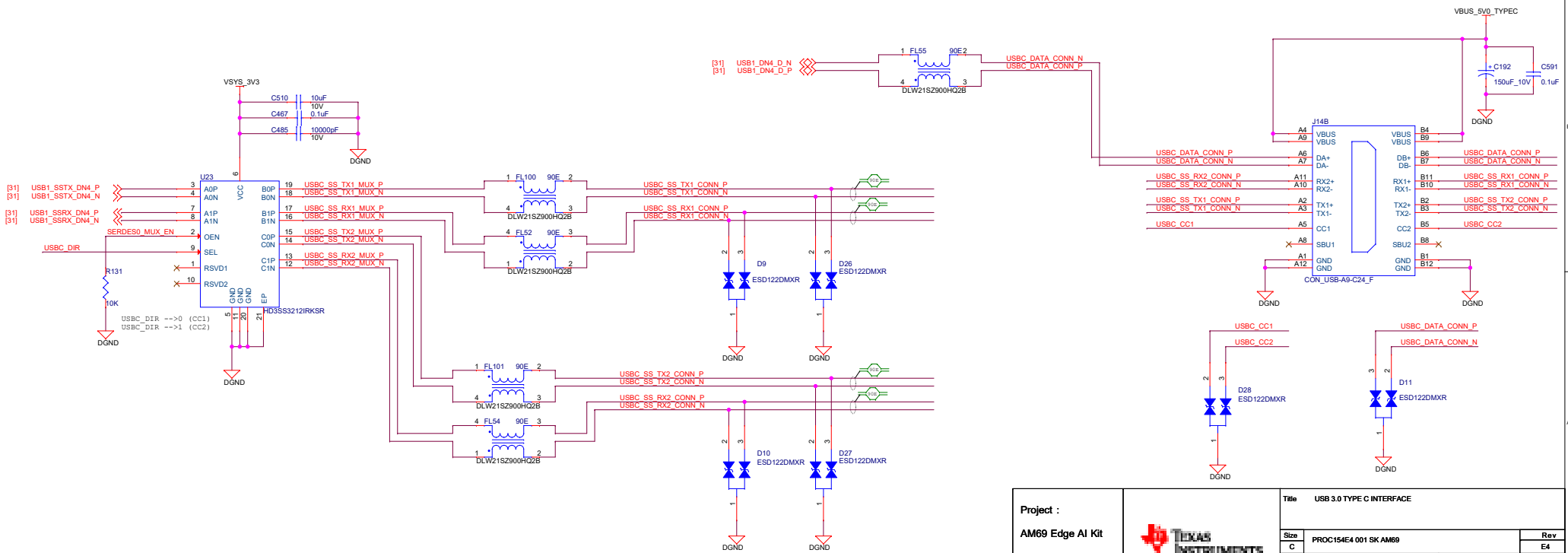
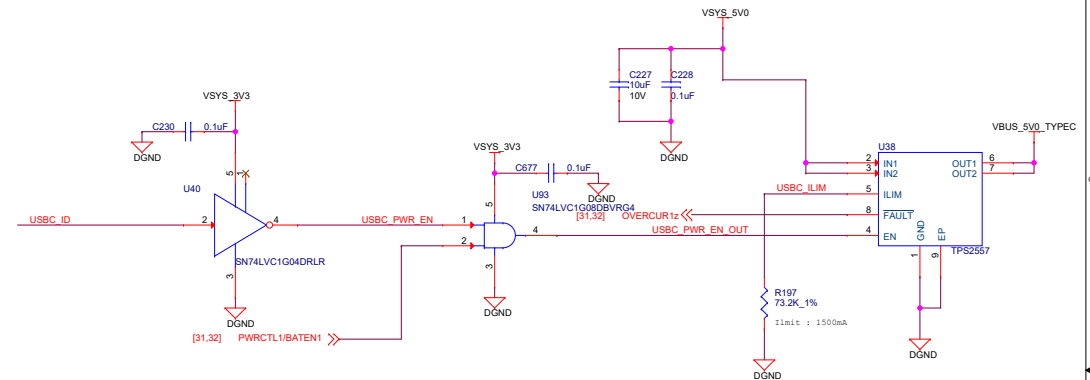
## USB 3.0 TYPE-A CONNECTORS - 2



## USB 3.0 TYPE C INTERFACE

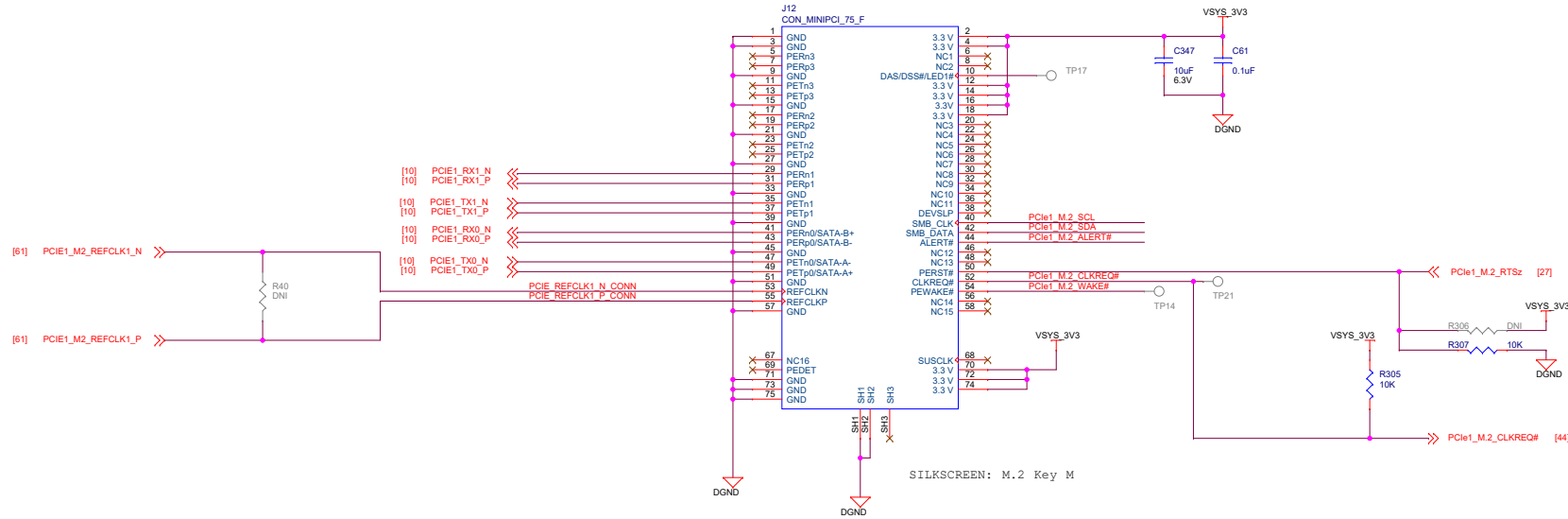


USB Type C Current Limit

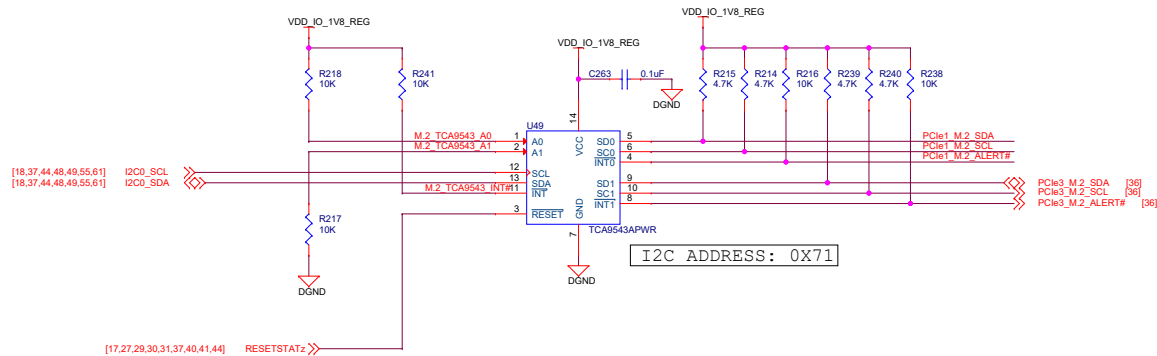


# PCIe\_M.2\_INTERFACE SSD

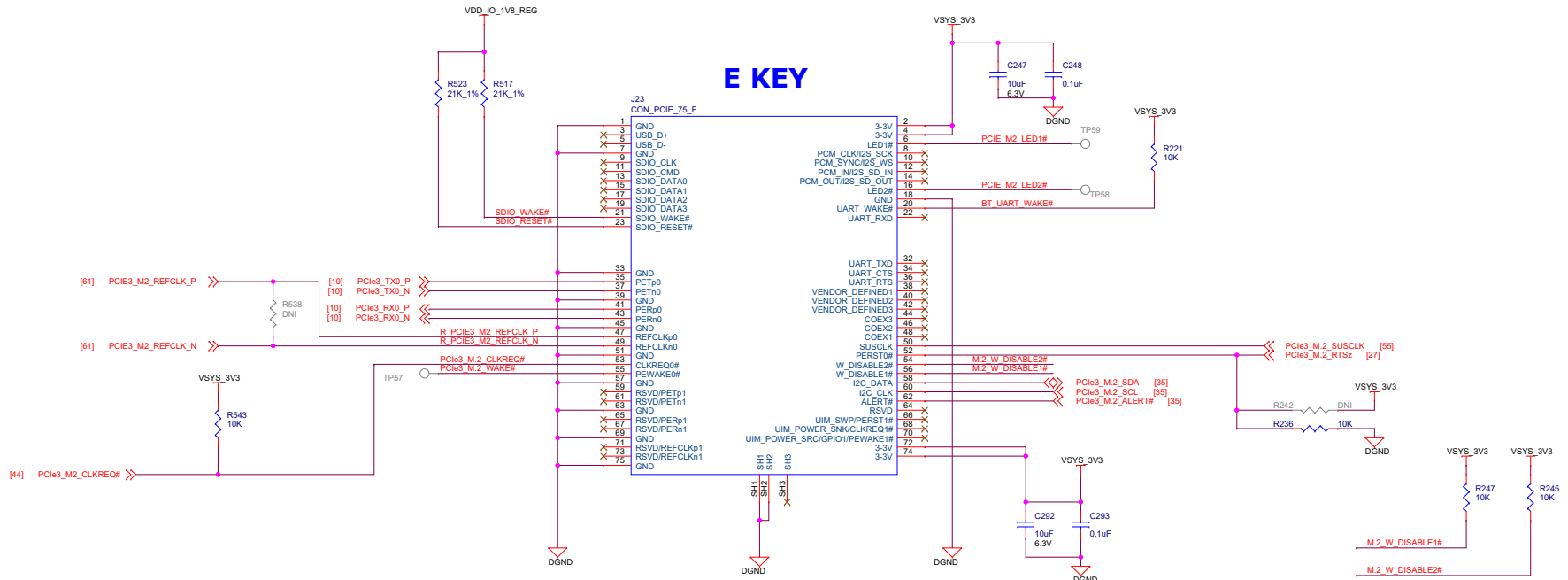
## M KEY



## 3.3V To 1V8 Level translator

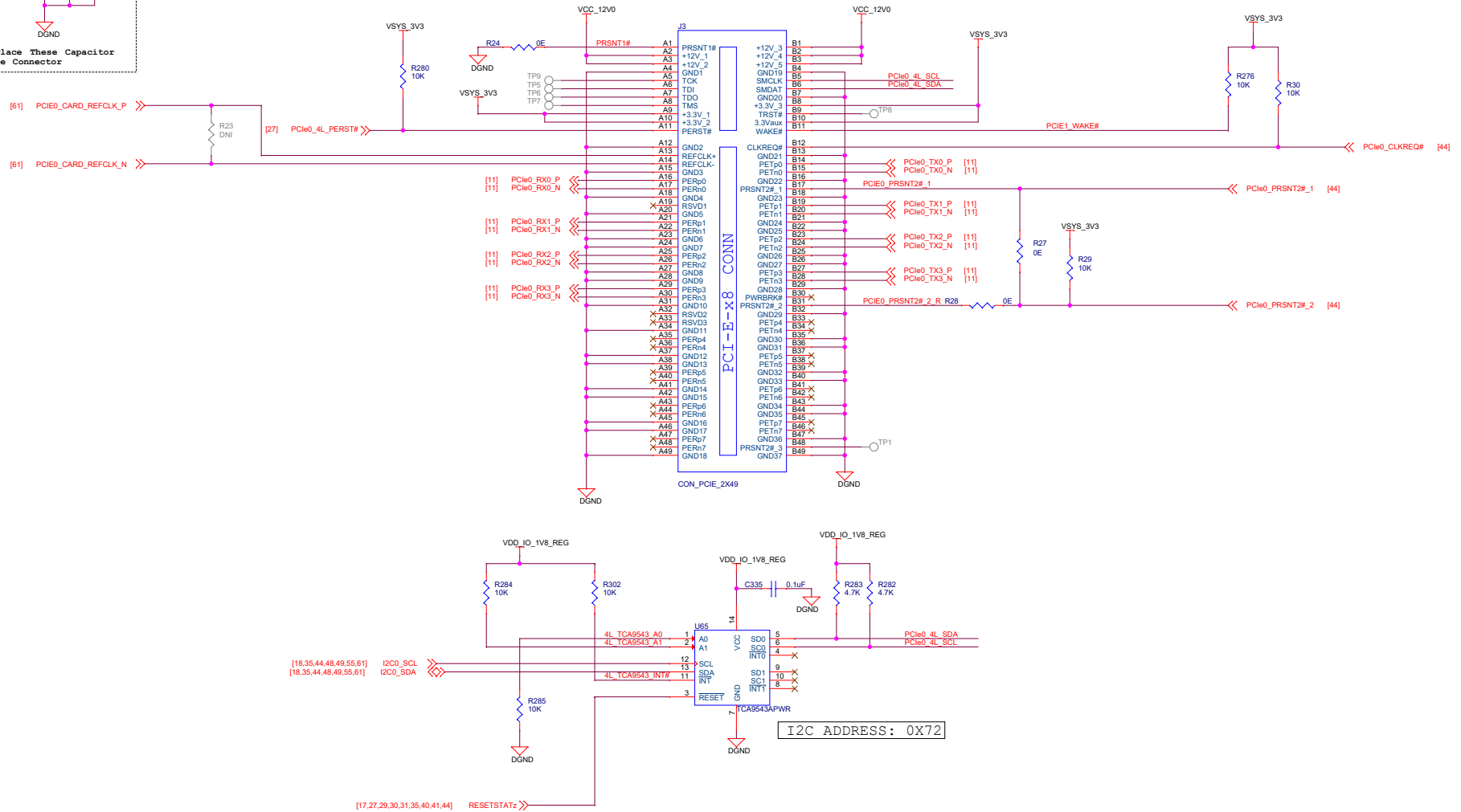
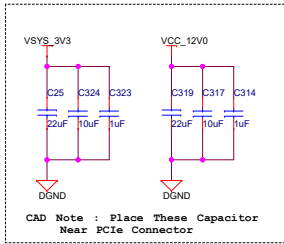


# PCIe\_M.2\_INTERFACE - SDIO



SILKSCREEN: M.2 Key E

# PCIe Card Slot



RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

Project :  
AM69 Edge AI Kit



Title	MCU GB ETHERNET
-------	-----------------

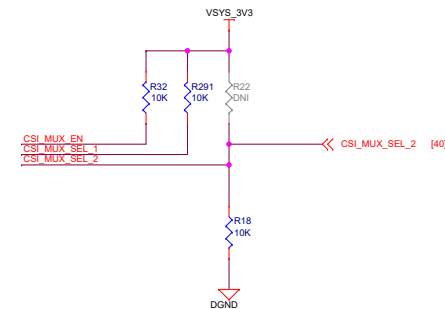
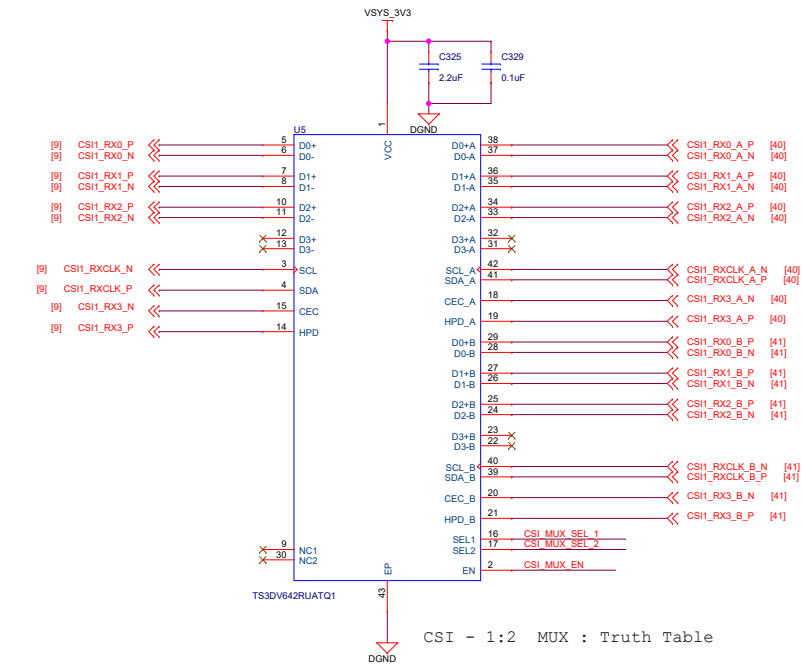
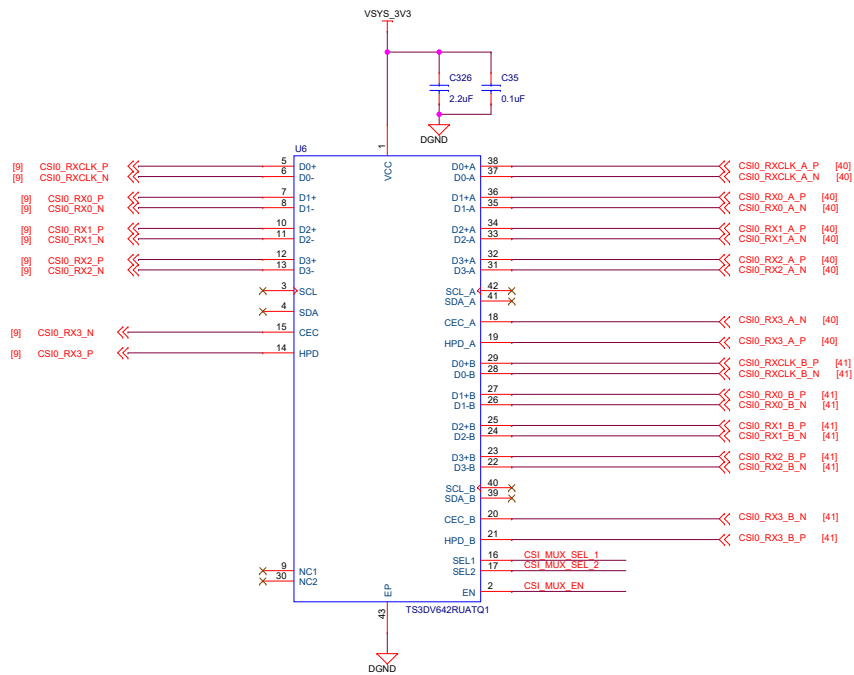
Size	DDG45454.004.0K AM30
------	----------------------

Date: Monday, May 05, 2025

Rev

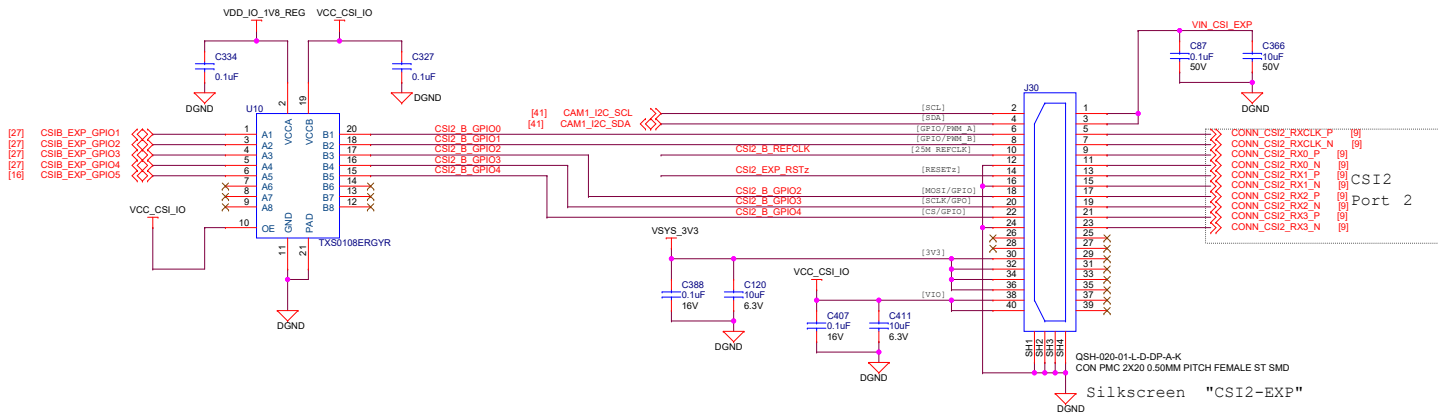
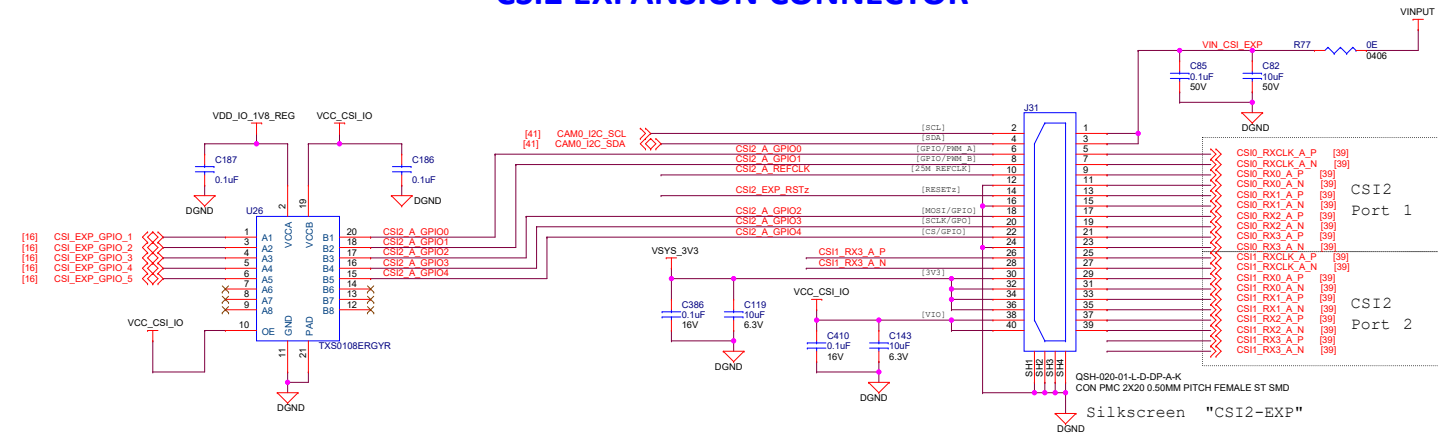
2

# CSI MUX - DATA

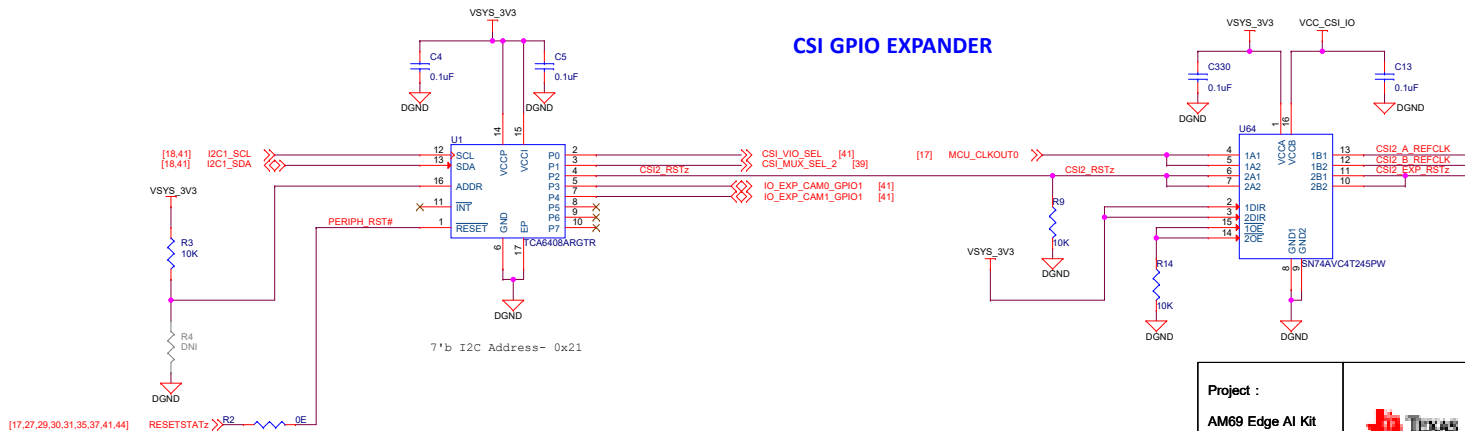


MUX_SEL_2	FUNCTION	
LOW	INPUT<-- A Port [CSI2 Connector]	(default)
HIGH	INPUT<--B port [FPC Camera Connector]	

# CSI2 EXPANSION CONNECTOR



## CSI GPIO EXPANDER



Project :  
AM69 Edge AI Kit



Title: CSI2 EXPANSION CONNECTOR

Size: PROC154E4 001 SK AM69

Date: Monday, May 05, 2025

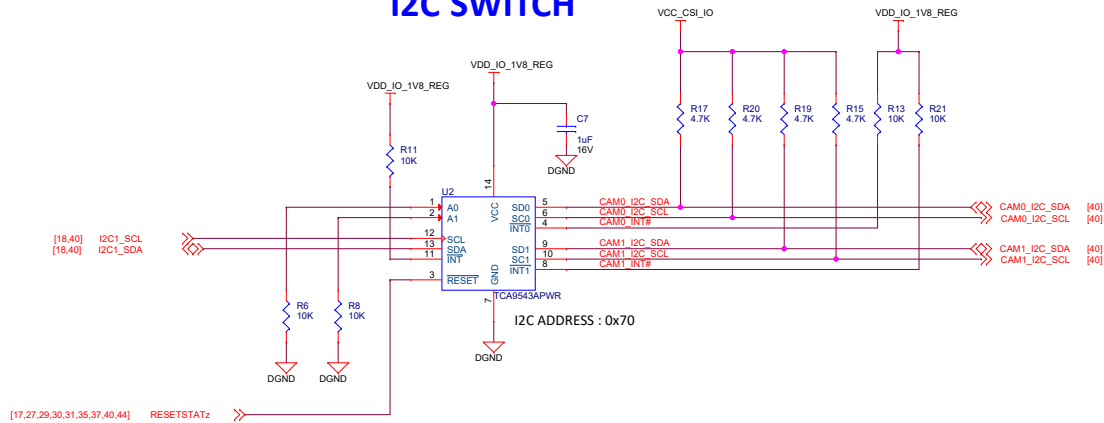
Rev: E4

Sheet: 40 of 62

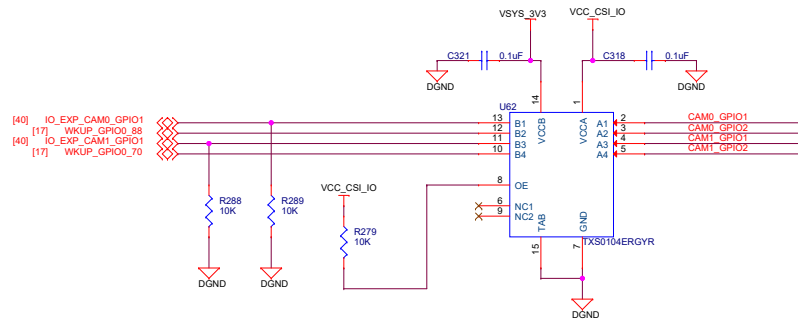


# CSI FPC CAMERA CONNECTORS

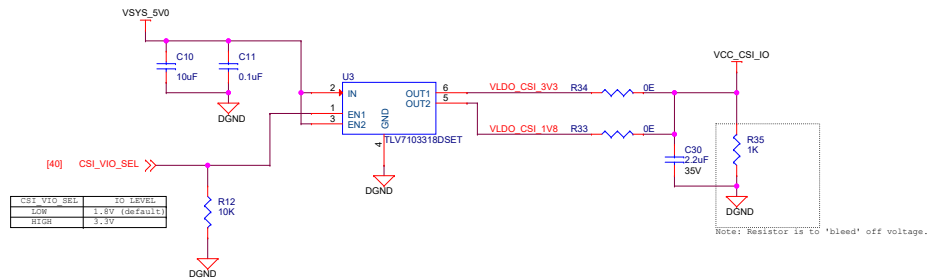
## I2C SWITCH



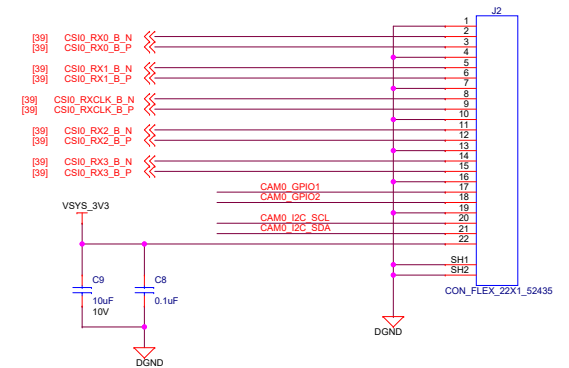
## GPIO LEVEL TRANSLATOR



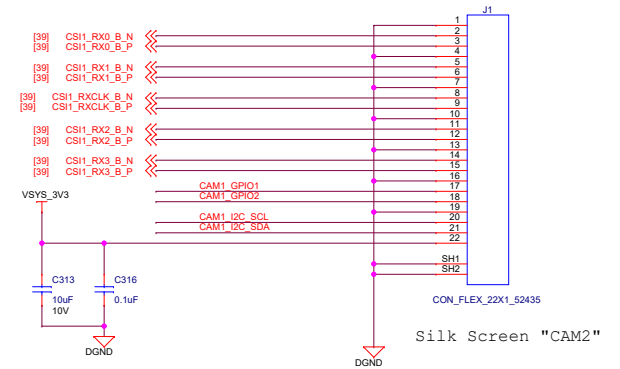
## CAMERA IO SUPPLY



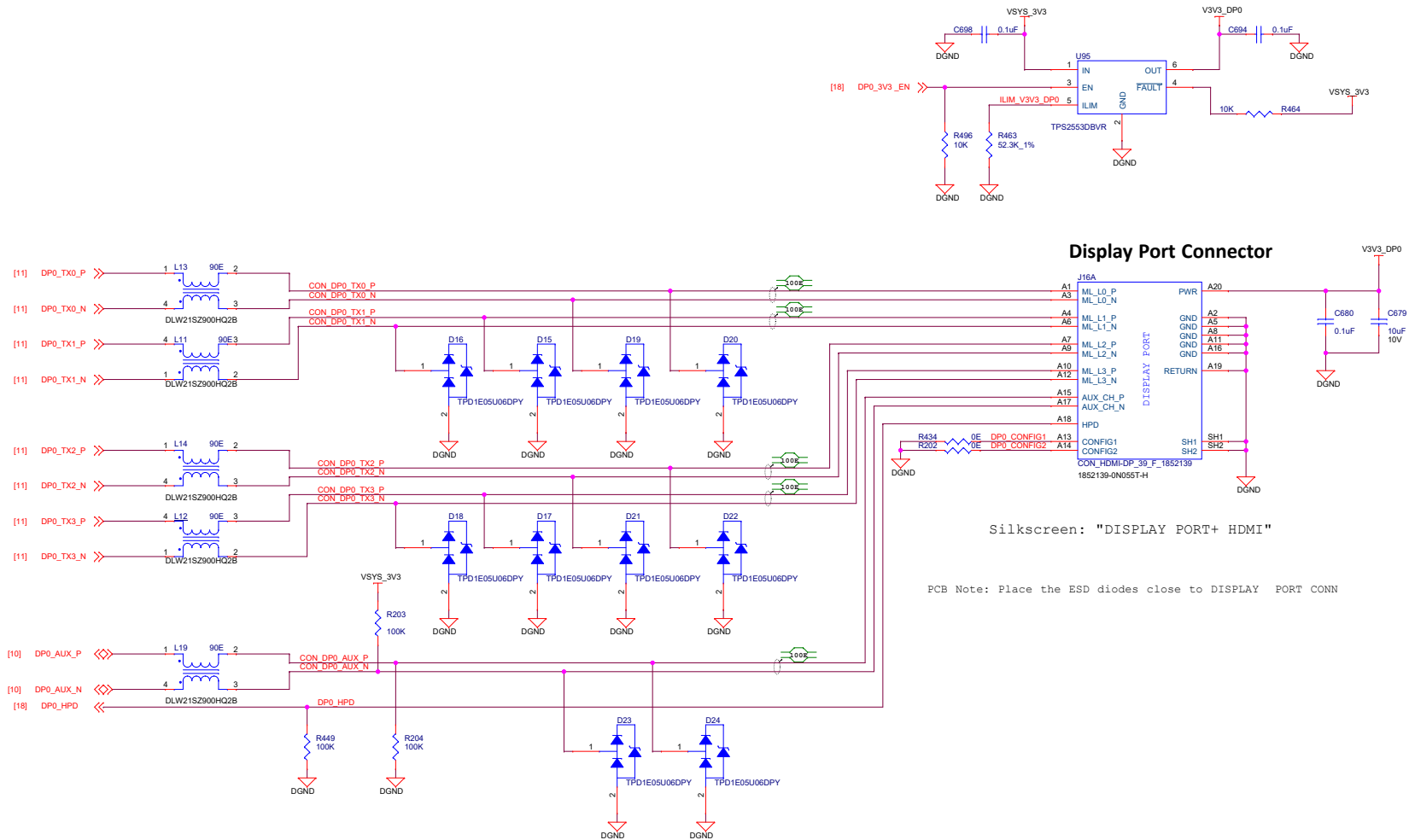
Silk Screen "CAM1"  
FPC Camera Connector -1



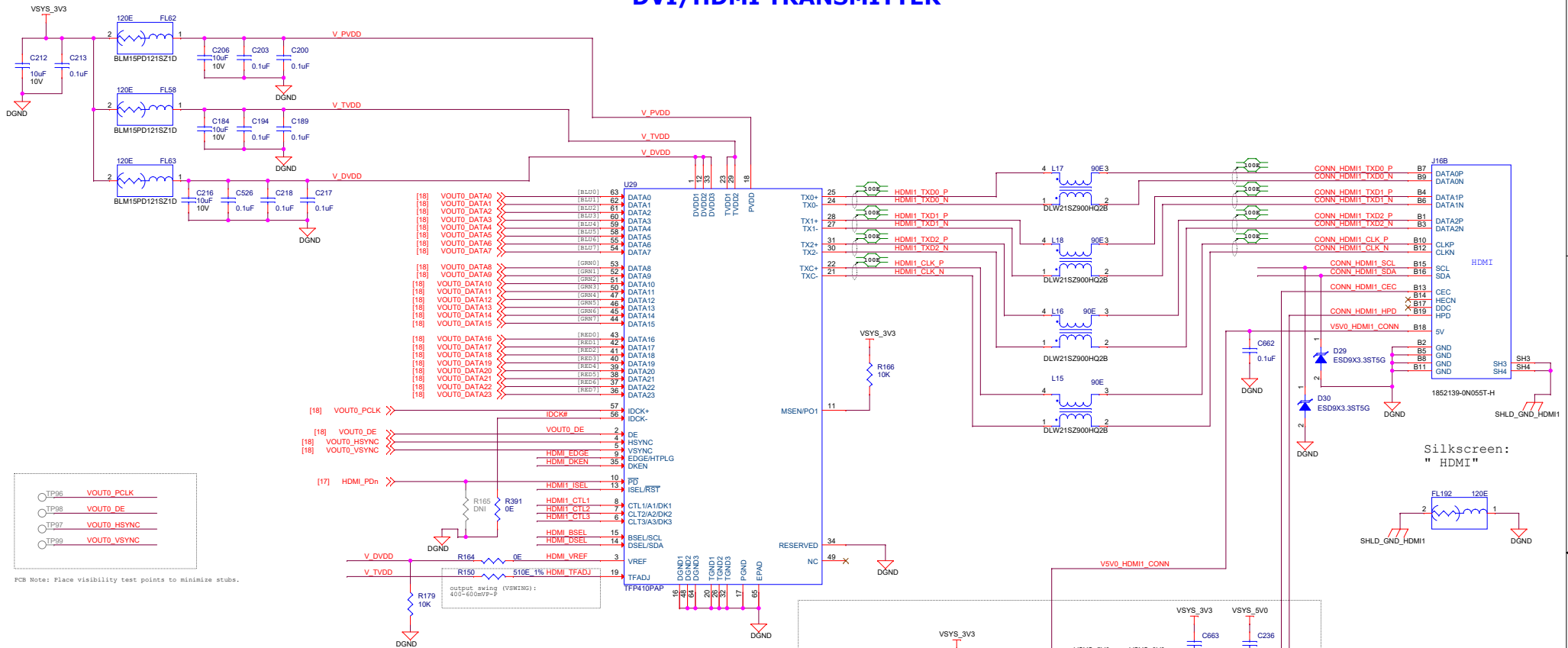
FPC Camera Connector -2



## DISPLAY PORT INTERFACE



# DVI/HDMI TRANSMITTER

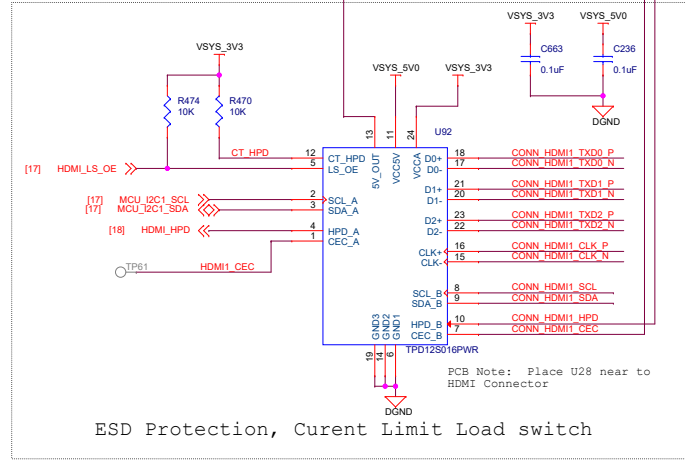


## DVI Configuration Settings

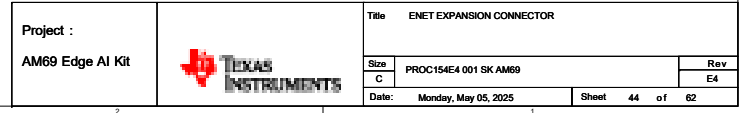
VREF	BSEL	EDGE	DSEL	BUS WIDTH	LATCH MODE	CLOCK MODE	CLOCK EDGE
0.55V-0.9V	1	0	0	24-bit	Single-ended	Falling	Single-ended
Default	1	1	0	24-bit	Single-ended	Raising	Single-ended

ISEL:- Low (default): I2C interface is disabled and chip configuration is specified by BSEL, DSEL, EDGE, VREF pins

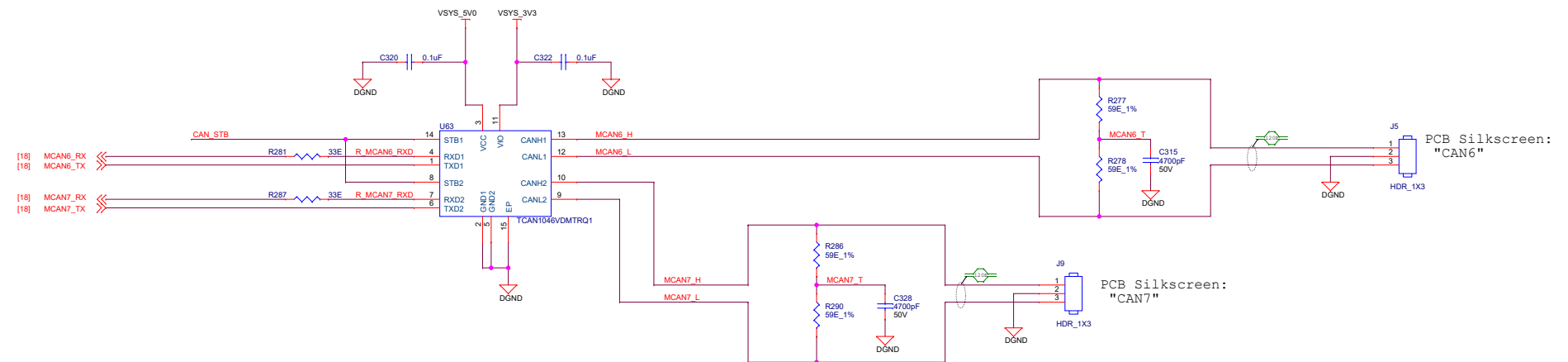
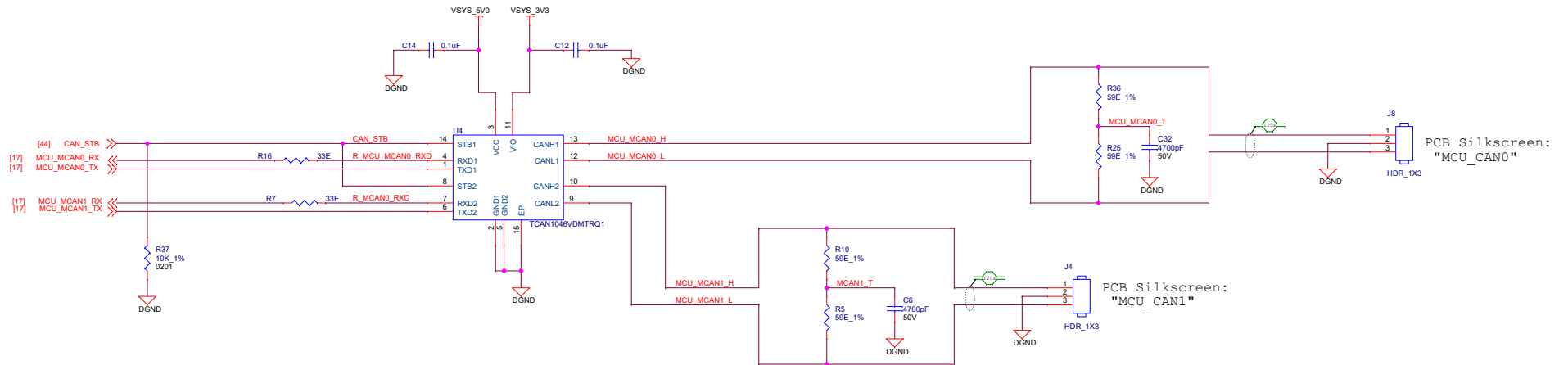
When ISEL: L, DSEL-H- enables de-skew function (default)



## Silkscreen "ENET-EXP"

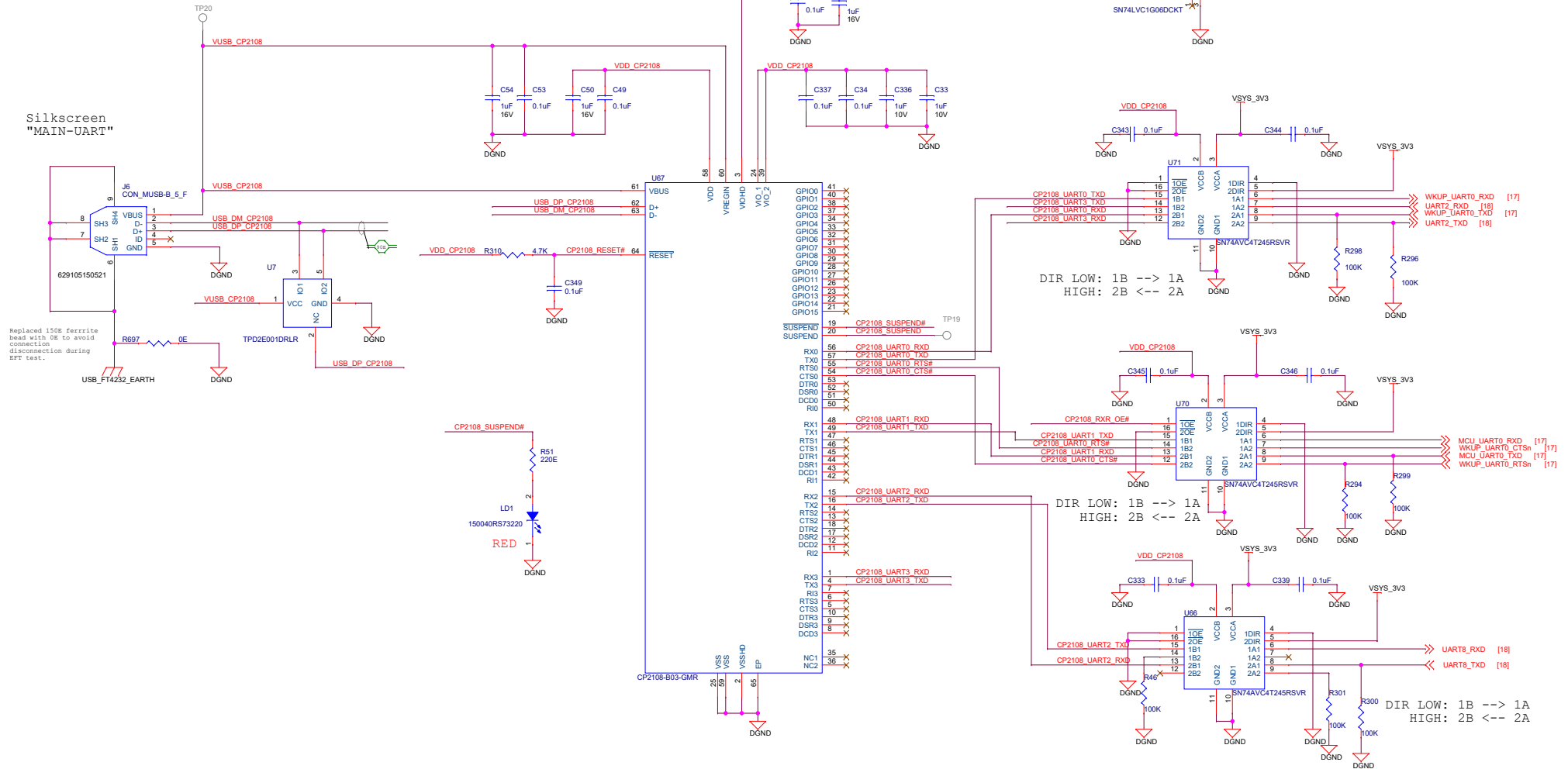


# CAN TRANSCEIVERS

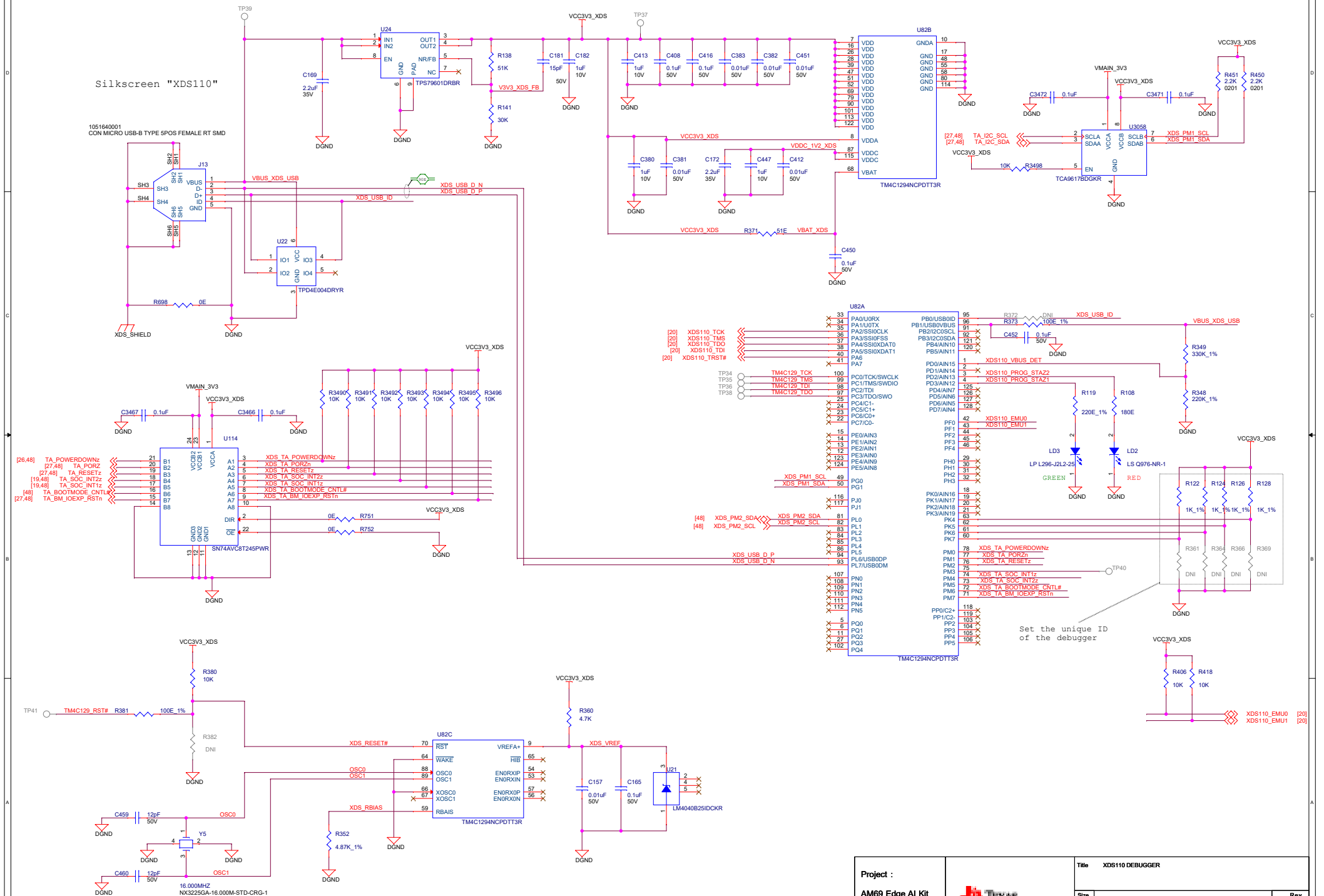


# QUAD PORT CONSOLE

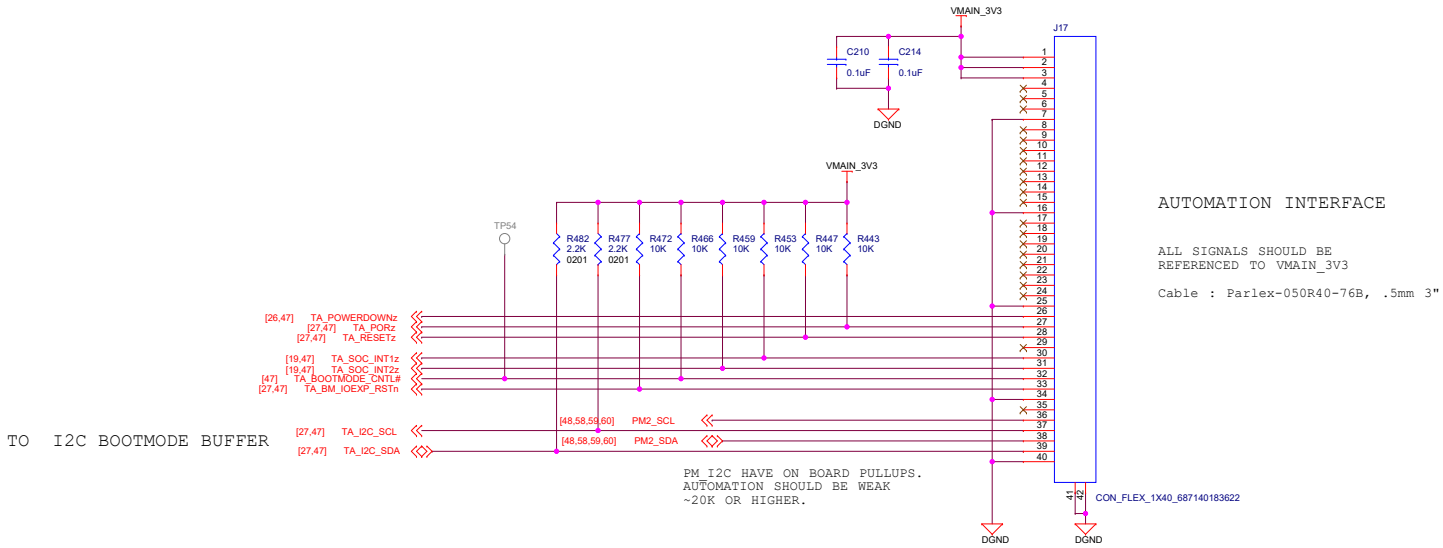
Silkscreen  
"MAIN-UART"



## XDS110 DEBUGGER

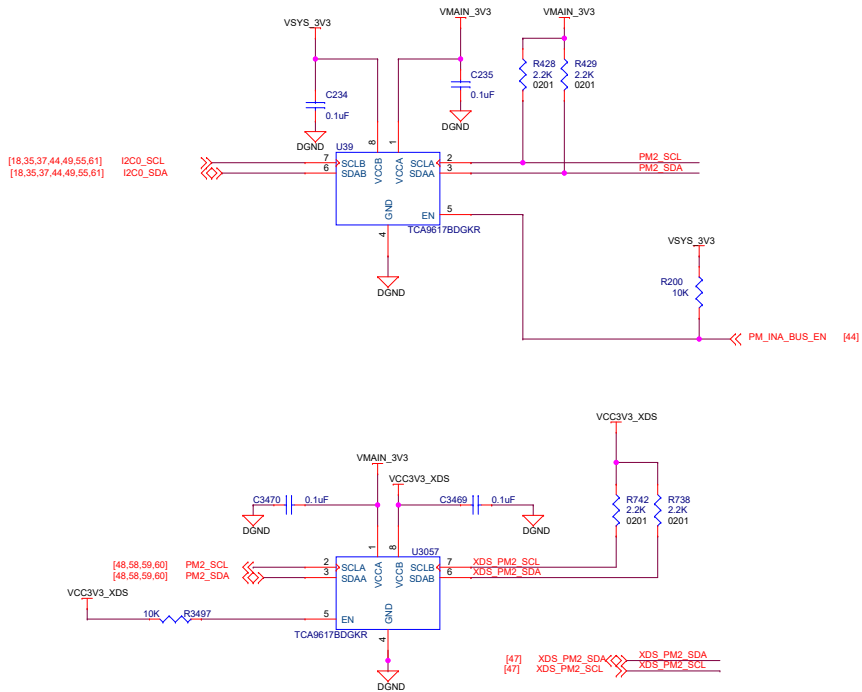


TEST AUTOMATION HEADER



AUTOMATION INTERFACE

ALL SIGNALS SHOULD BE  
REFERENCED TO VMAIN\_3V3  
Cable : Parlex-050R40-76B, .5mm 3"

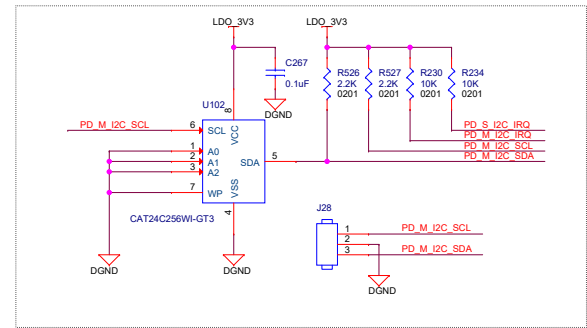


TEST AUTOMATION GPIO MAPPING

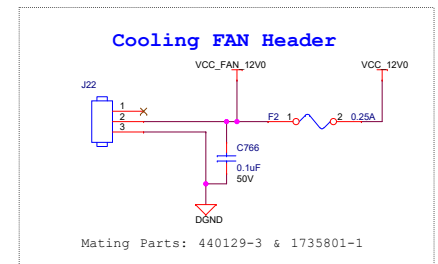
SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORz	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup



## EEPROM &amp; PROGRAMMING HEADER



## Power Input



SILK: POWER IN



Date: Monday, May 05, 2025

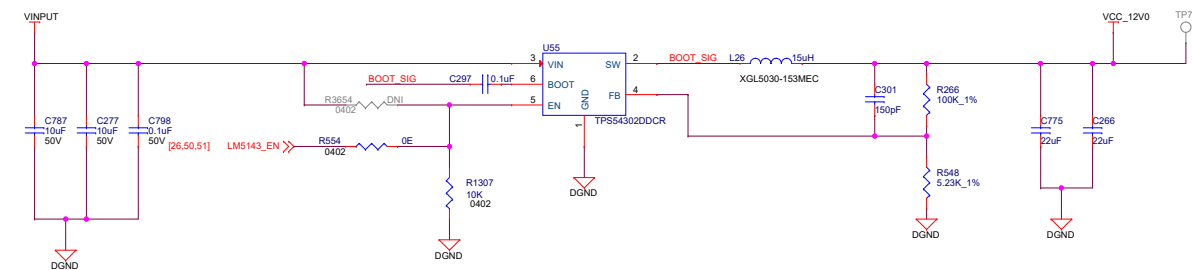
2



## POWER SUPPLY #2

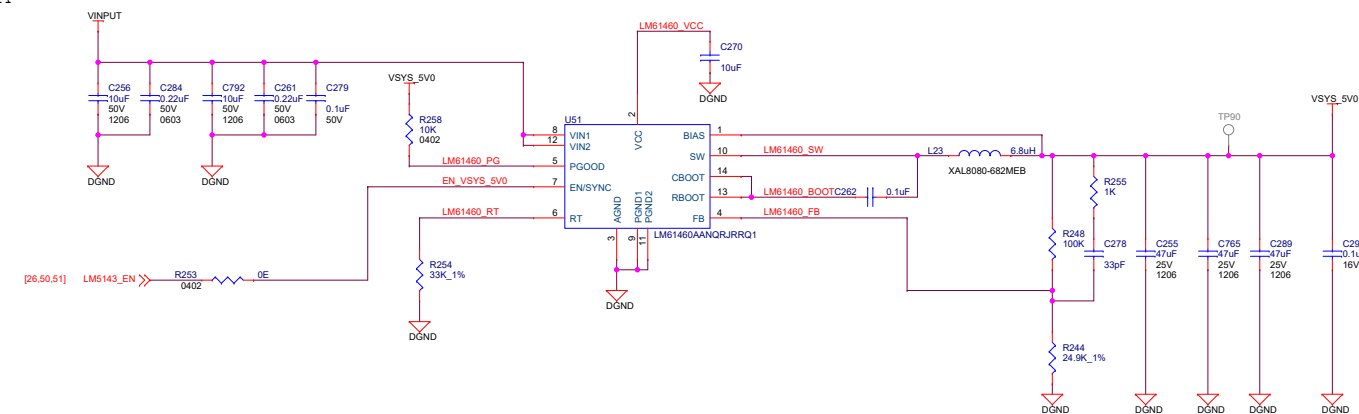
TI WEBENCH Simulation Inputs:  
 Vin (min) = 15V Vin (max) = 25V  
 Vout = 12V@3A  
 Ta = 25 deg

### 12V GENERATION



LM61460 5V BUCK REGULATOR  
 VinMin = 12V  
 VinMax = 25V  
 Vout = 5.0V  
 Iout = 6A

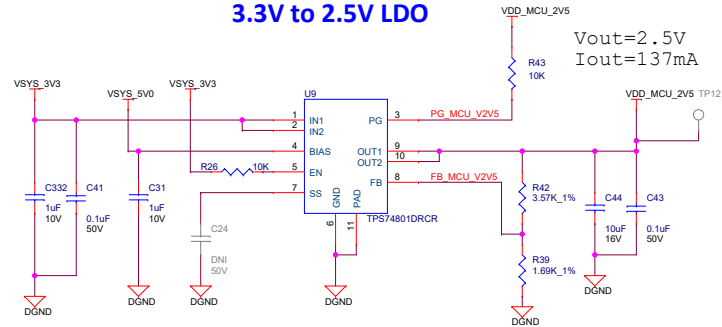
### 5V GENERATION



# POWER SUPPLY #3

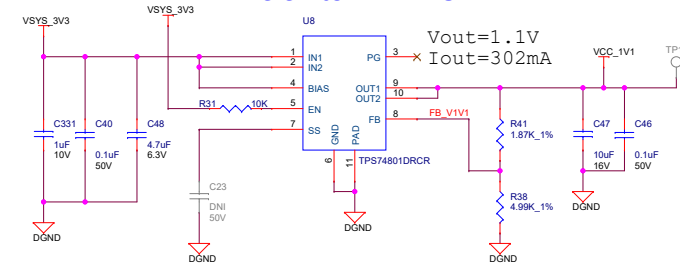
## ETHERNET POWER- MCU RGMII

### 3.3V to 2.5V LDO



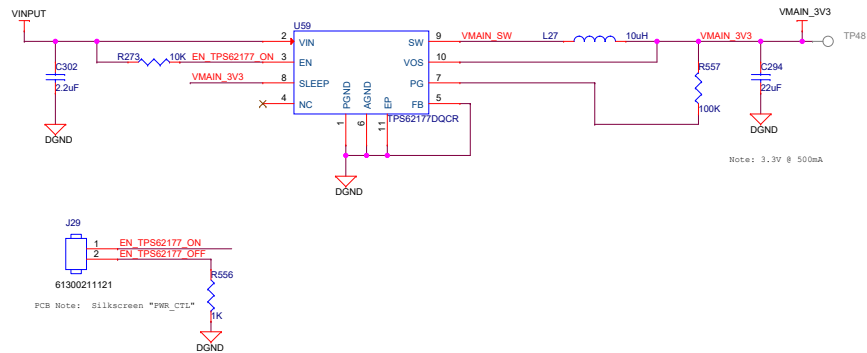
## USB HUB POWER & ETHERNET POWER - RGMII1

### 3.3V to 1.1V LDO

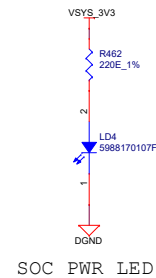


PCB NOTE: Keep 4.7uF capacitor close to BIAS pin

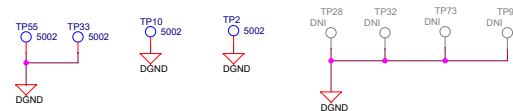
## SYSTEM MANAGEMENT 3.3V REGULATOR



## POWER INDICATION LED's



## GROUND TEST POINTS



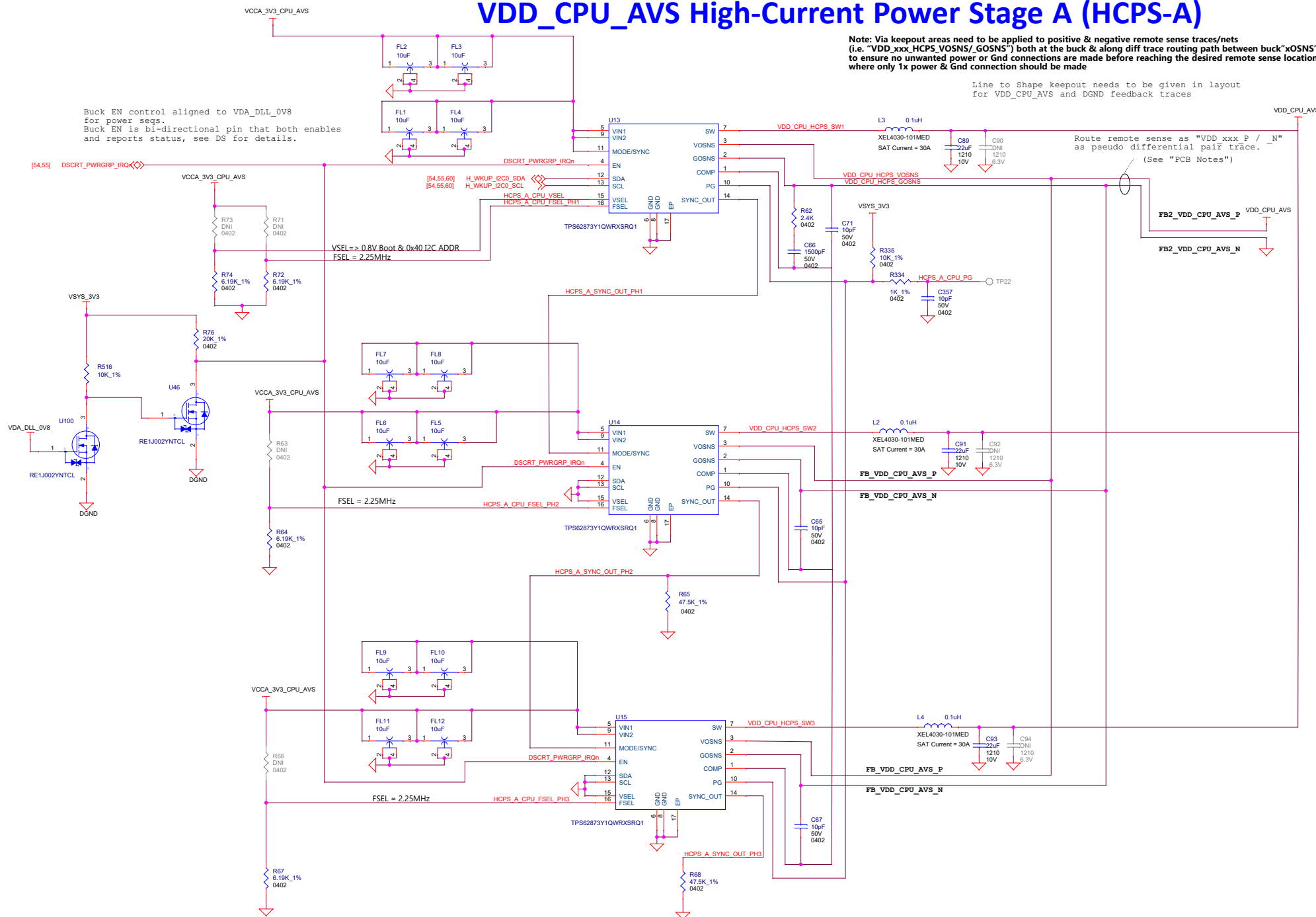
PCB NOTE: Spread the SMD test points Top and Bottom Side of PCB

# VDD\_CPU\_AVS High-Current Power Stage A (HCPS-A)

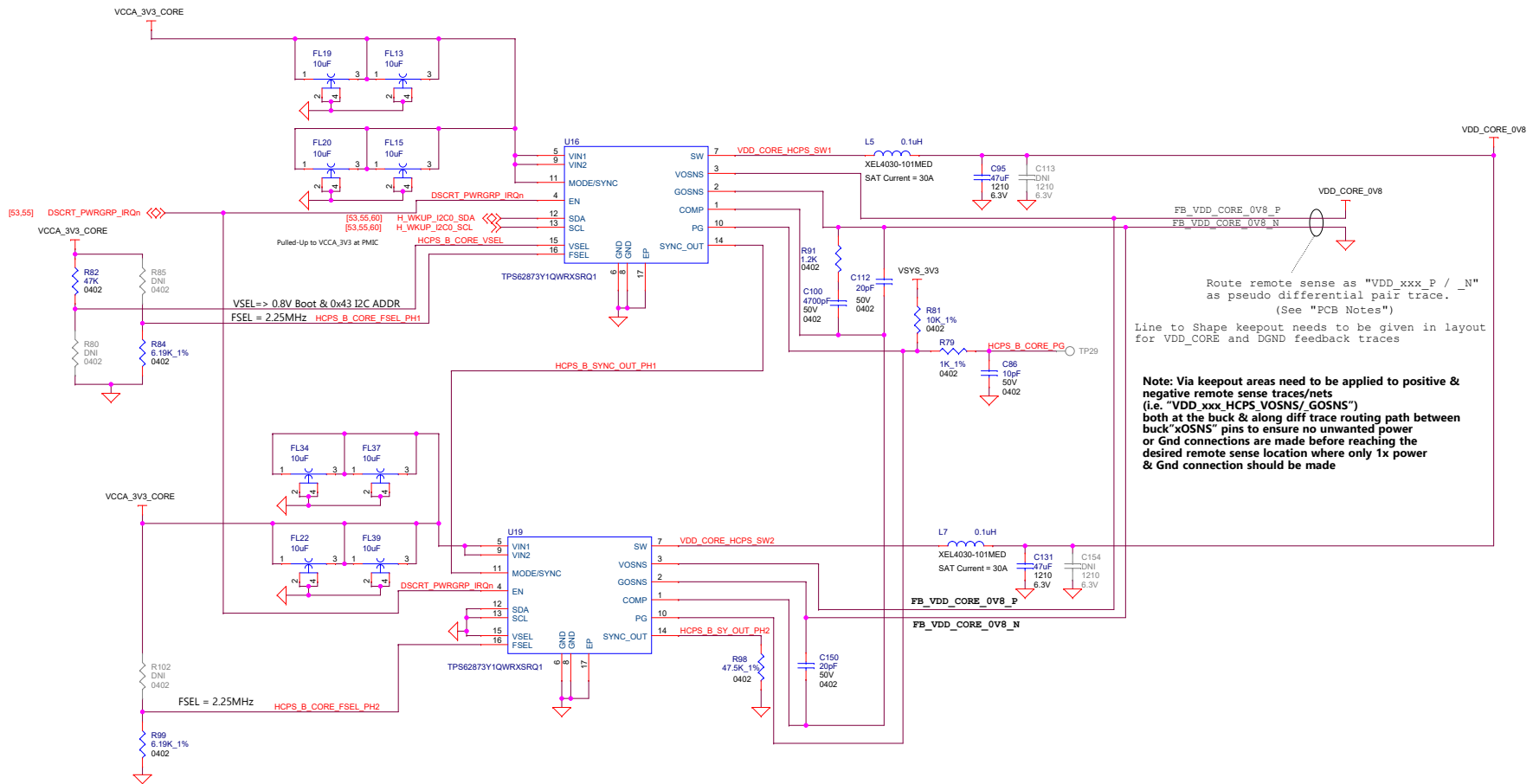
Note: Via keepout areas need to be applied to positive & negative remote sense traces/nets (i.e. "VDD\_XXX\_HCPS\_VOSNS"/\_GOSNS") both at the buck & along diff trace routing path between buck"xOSNS" pins to ensure no unwanted power or Gnd connections are made before reaching the desired remote sense location where only 1x power & Gnd connection should be made

Line to Shape keepout needs to be given in layout for VDD\_CPU\_AVS and DGND feedback traces

Buck EN control aligned to VDA\_DLL\_0V8 for power seqs.  
Buck EN is bi-directional pin that both enables and reports status, see DS for details.



## VDD\_CORE\_0V8 High-Current Power Stage A (HCPS-B)



Route remote sense as "VDD\_XXX P / \_N"  
as pseudo differential pair trace.  
(See "PCB Notes")

Line to Shape keepout needs to be given in layout  
for VDD\_CORE and DGND feedback traces

**Note:** Via keepout areas need to be applied to positive & negative remote sense traces/nets (i.e. "VDD\_XXX\_HCPS\_VOSNS/ GOSNS") both at the buck & along diff trace routing path between buck/xOSNS" pins to ensure no unwanted power or Gnd connections are made before reaching the desired remote sense location where only 1x power & Gnd connection should be made

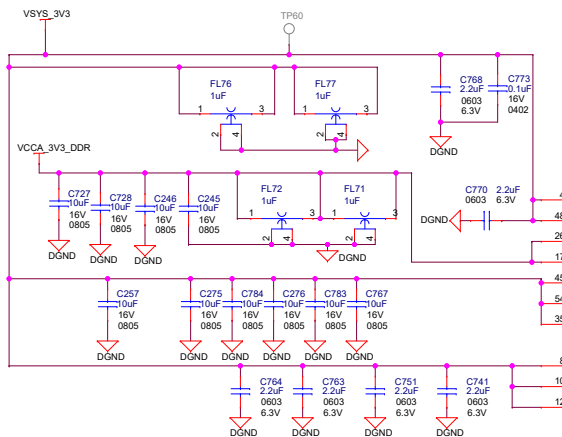
# PMIC

"PCB Notes":

- For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Use pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
  2. Ensure only 2x Point of Load (PoL) vias connect sense trace to Pwr & Gnd planes near the middle of SOC's power ball group.
  3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
  4. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible.

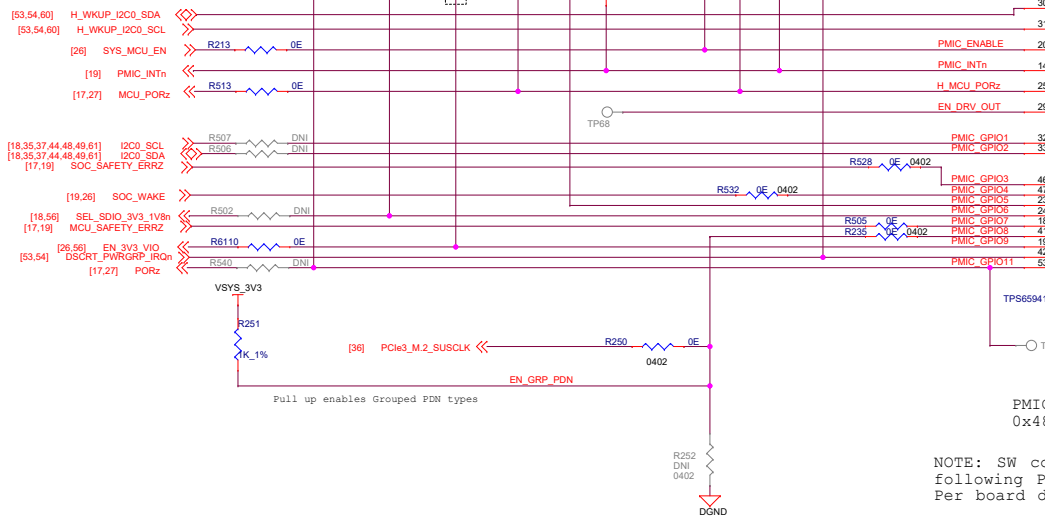
For single-phase Buck converter configs, route remote sense feedback as follows:

1. Use single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Ensure only 1x PoL via connects sense trace to Pwr plane near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
4. Trace widths = 4-8mil.



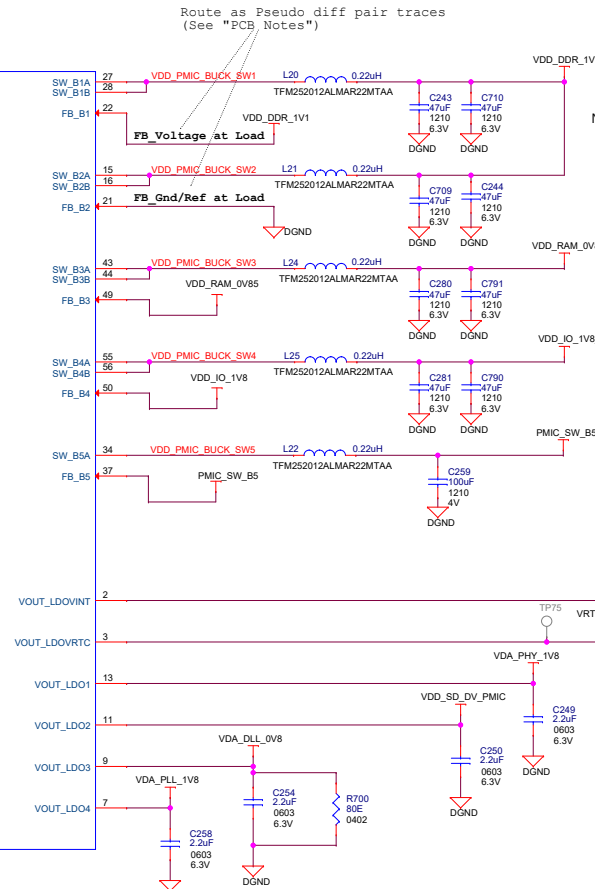
NOTE: 2x Options for disabling WDOG Timer:

- 1 - Install R699 as HW option
- 2 - System SW can use I2C write to PMIC register after SW boot.



PMIC-A uses default I2C ADDR:  
0x48, 0x49, 0x4A & 0x4B

NOTE: SW commands required to reassign following PMIC GPIO pin functions after SoC BOOT  
Per board design needs: GPIO #s 1 - 7.



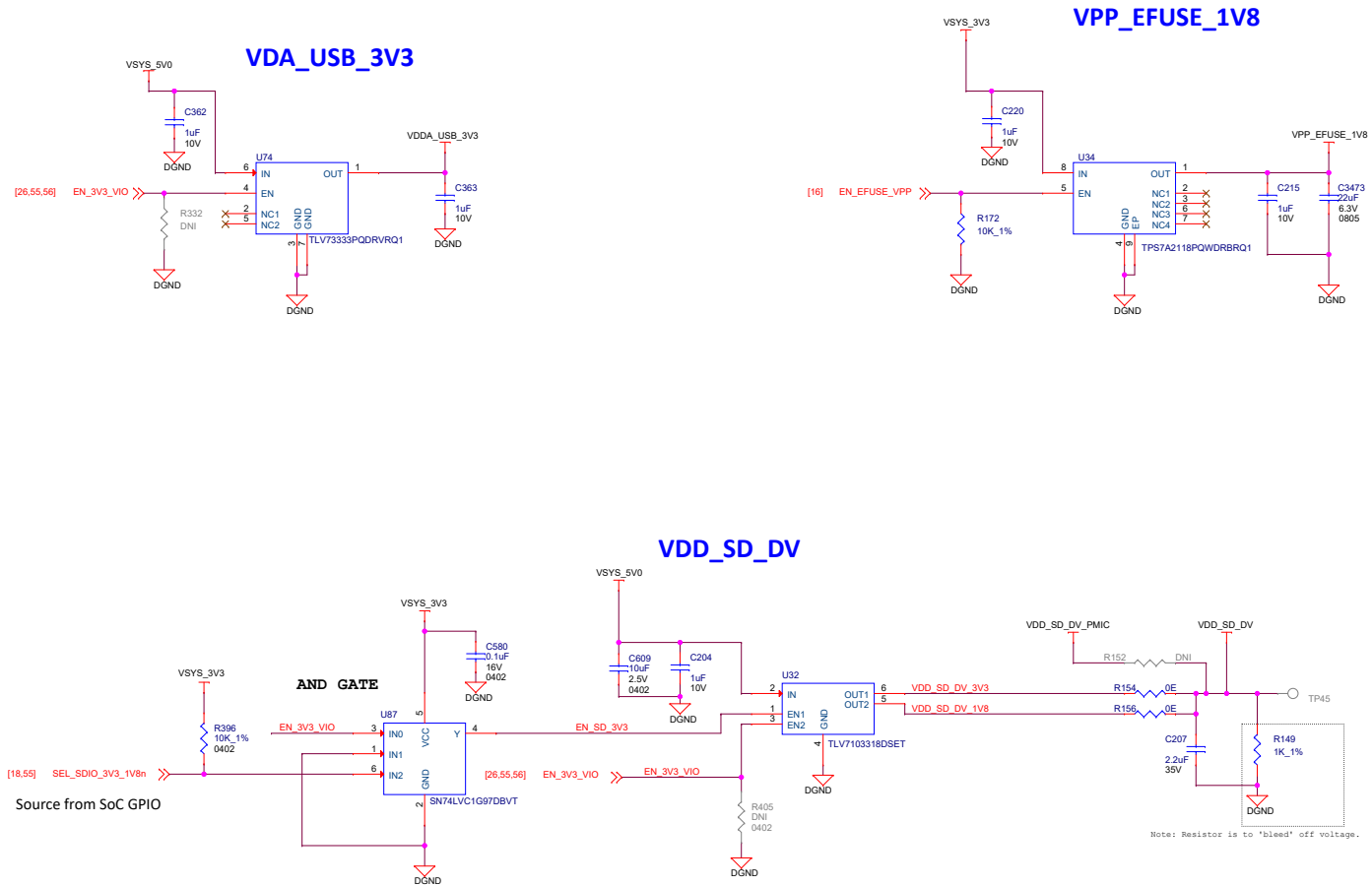
Note: Keepout needs to be provided for the VDD\_DDR\_1V1 and Gnd vias of the feedback pins connecting to the PMIC.

Line to Shape keepout needs to be given in layout for VDD\_DDR\_1V1 and DGND feedback traces

NOTE: 10mA bleed resistor added to ensure stable LDO operation when board Cz = ~30uF > LDO's max Cz = 20uF

Project :		Title PMIC	
AM69 Edge AI Kit		Size	
		C PROC154E4 001 SK AM69	
		Rev	
		E4	
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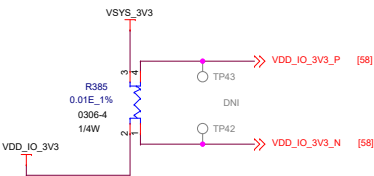
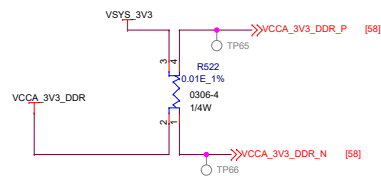
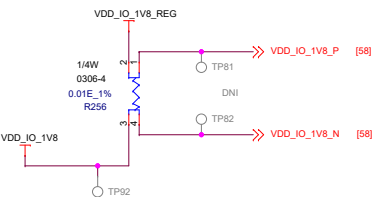
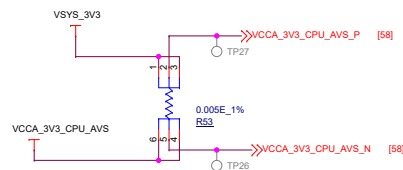
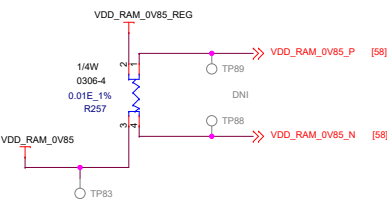
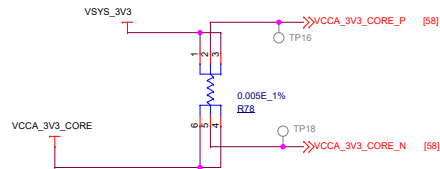
# LDOs



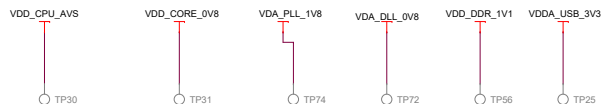


# SOC Current Sense Resistors

CORE, AVS and DDR input supply sense resistors



PCB Note: Place all SMT TPs  
on PCB top-side & on top of via at  
Bd-to-Bd connector



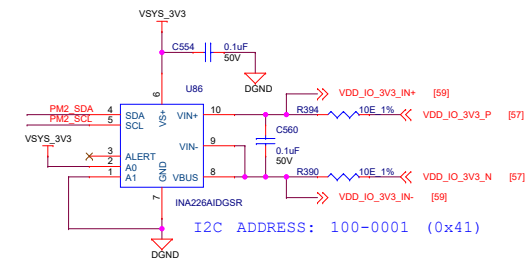
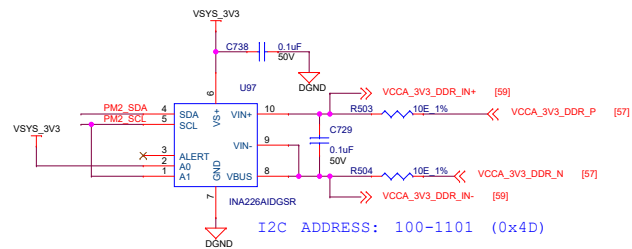
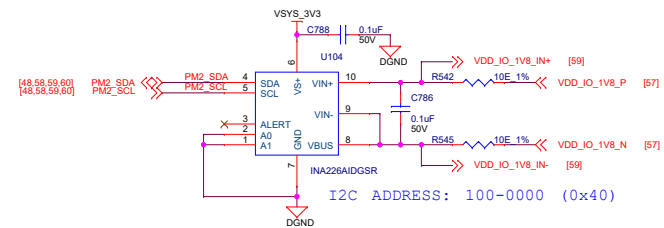
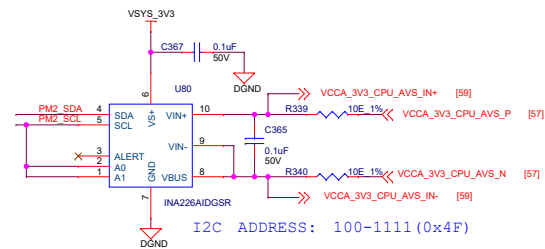
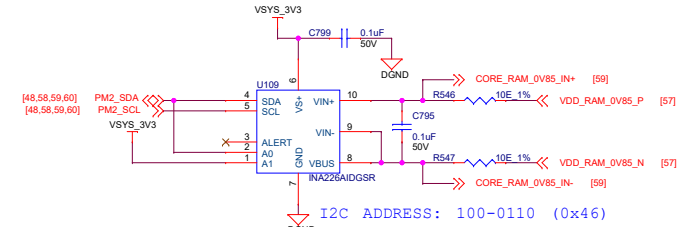
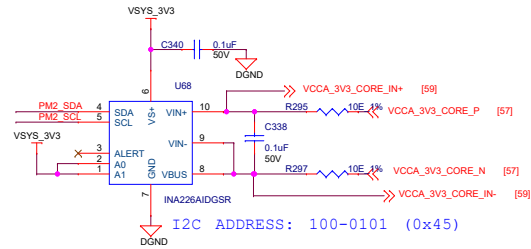
Project :  
AM69 Edge AI Kit



Title		SOC - CURRENT SENSE RESISTORS	
Size	PROC154E4 001 SK AM69		Rev
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Date:	Monday, May 05, 2025	Sheet	57 of 62

Note: The design supports current/voltage measurements using either INA226 or INA231. The SK will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

## CURRENT MONITORS - INA226



Project :  
AM69 Edge AI Kit



Title CURRENT MONITORS - INA226

Size PROC154E4 001 SK AM69

C

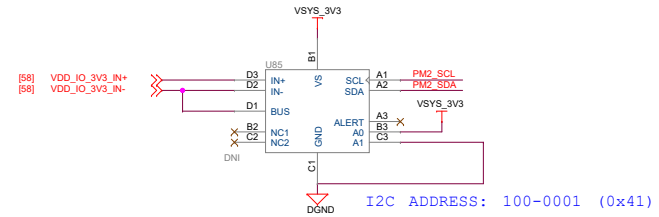
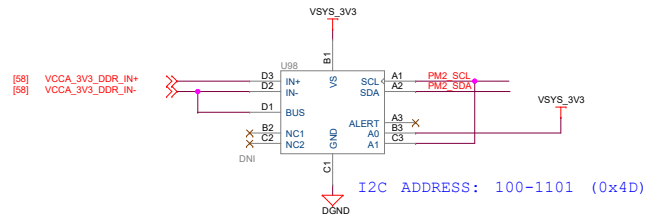
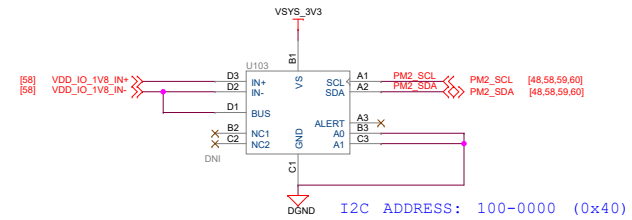
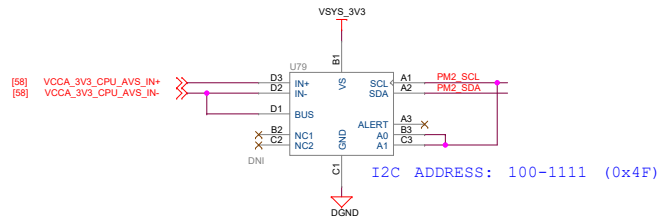
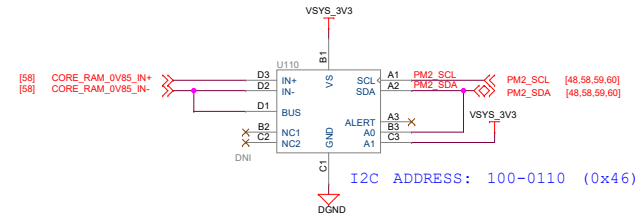
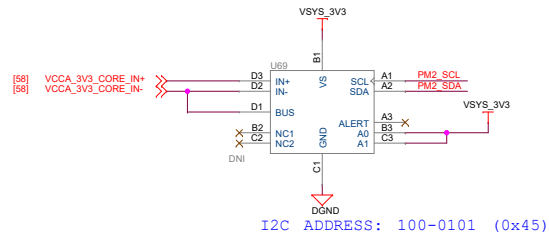
Date: Monday, May 05, 2025

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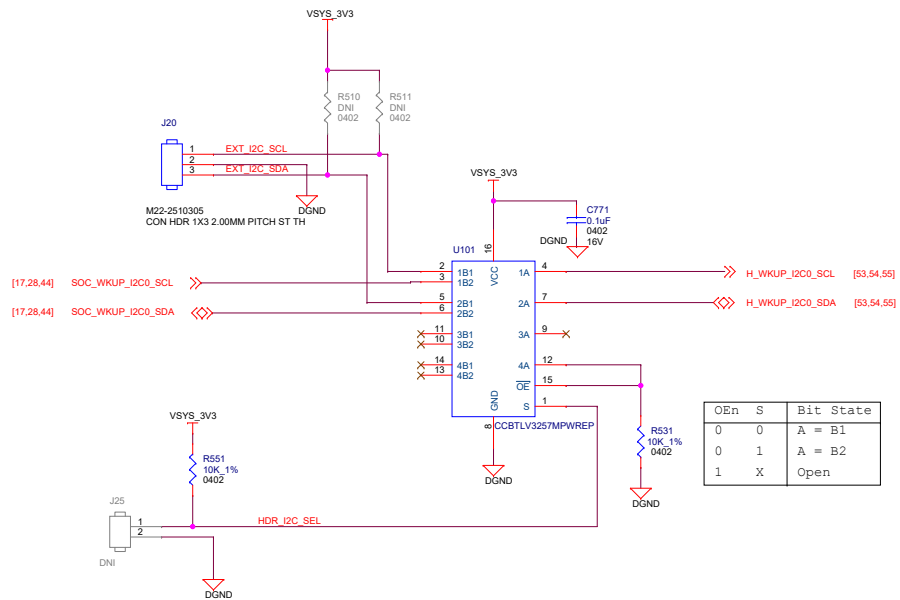
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Note: The design supports current/voltage measurements using either INA226 or INA231. The SK will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

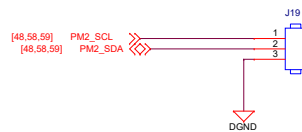
## CURRENT MONITORS - INA231



# PMIC Support Circuit



## EXT POWER MEASUREMENT



Project :

AM69 Edge AI Kit



Title PMIC SUPPORT CIRCUIT

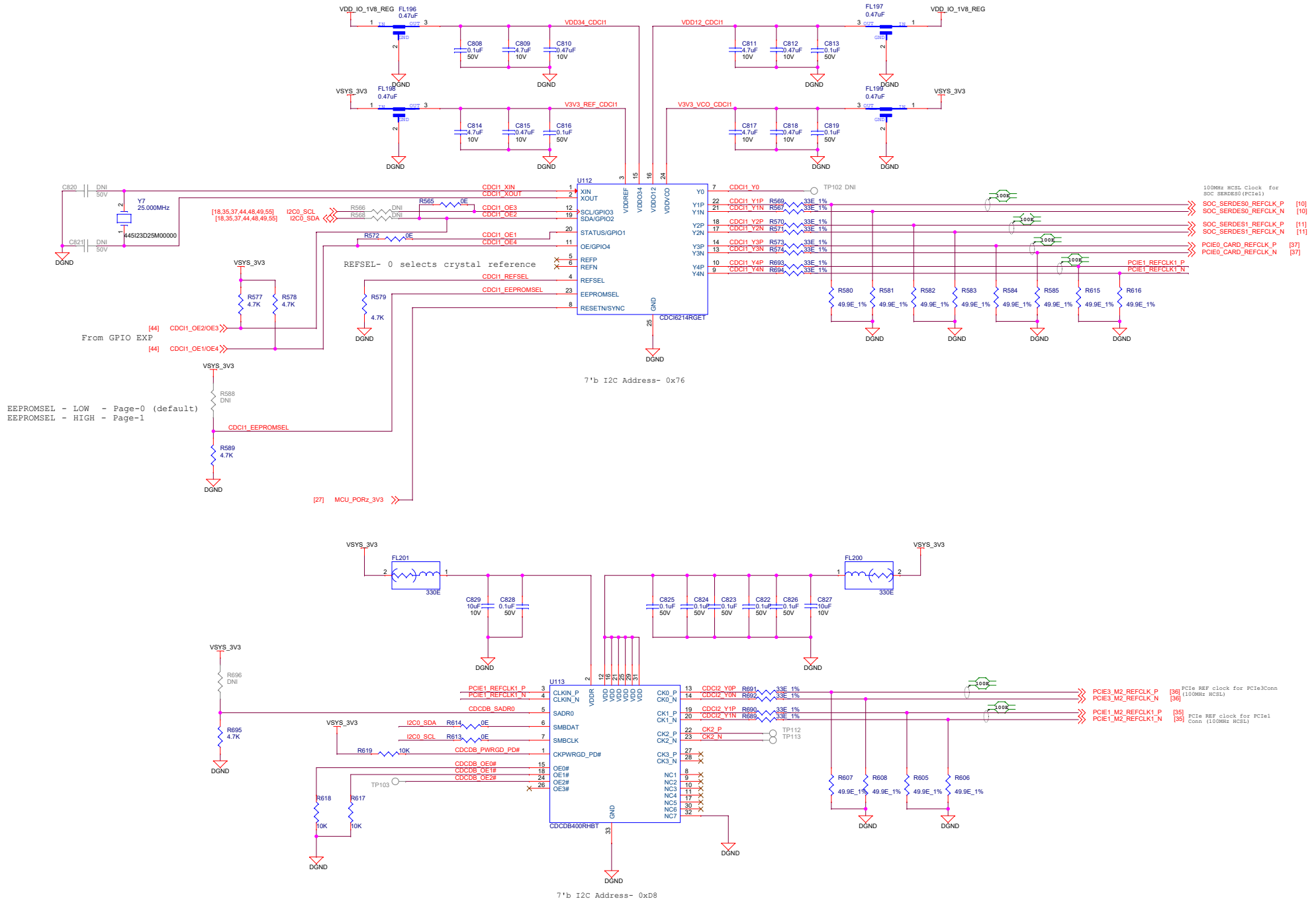
Size C

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# SERDES CLOCK GENERATORS



NOTES, HW & LABELS

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

LABELS

Board Serial No.



AM6-COMPROCEVM

Assembly Revision.

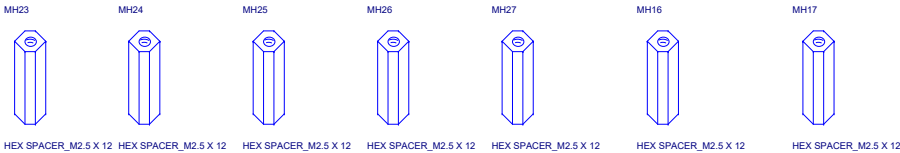


AM6-COMPROCEVM

SCREWS



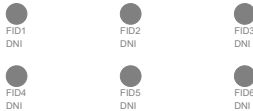
STANDOFFS



WASHER



FIDUCIALS



BARE PCB



SCREW & WASHER FOR PCIe M.2



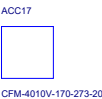
LOGOS



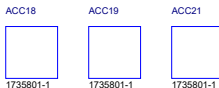
HEAT SINK



FAN



CRIMP PIN



CONN HOUSING



SCREW FOR FAN ASSEMBLY

