REVISIONS		
REV #	DESCRIPTION	DATE
REV #	CCN #	DDMMYY

FABRICATION NOTES:

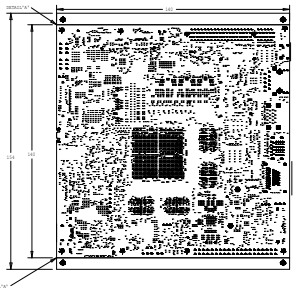
1. FABRICATE PCB IN ACCORDANCE WITH IPC-6012C, CLASS 2; PER IPC-6011. PCB SHALL BE MANUFACTURED USING 1-SPEED OR EQUIVALENT.
2. MATERIALS:
   1. LAMINATE AND PREPREG (R-TF368) TO BE IN ACCORDANCE WITH IPC-4101/126. (DK10.75 1.60)
   2. COPPER FOIL TO BE IN ACCORDANCE WITH IPC-MF-150, UNLESS OTHERWISE SPECIFIED, FOR OUTER LAYERS 1.45 OZ. COPPER WEIGHT IS TO BE CONSIDERED "FINISHED". THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 6012B TABLE NO.3-7 AND 3-8.
3. ALL HOLES SHALL BE LOCATED WITHIN 0.10MM DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.125MM.
4. BOW AND TWIST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTH.
5. CONDUCTOR WIDTH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCASE FOR MATCHING IMPEDANCE MISTRAL SHALL APPROVE THE MODIFIED WIDTHS AND SPACING. TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
6. AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
7. FINISH:
   1. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG, ELECTROLESS NICKEL/IMMERSION GOLD, ELECTROLESS NICKEL SHALL BE 3-6 MICRONS, TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.04-0.06 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
   2. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-SM-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. VIA HOLES ON BOARD SHALL BE TYPE VII FILLED AND CAP PLATED.
      ONLY SOLDERMASK IMAGES THAT ARE 0.08(0.003") PER SIDE SHALL BE REDUCED IF REQUIRED. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED. DEFAULT COLOUR OF SOLDER MASK SHALL BE BLUE.
   3. SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON ANY SOLDERMASK COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERMASK AREAS.
   4. SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 20UM [0.00079"].
   5. ALL HOLES SURROUNDED BY LAND <=0.010" SHALL BE COMPLAIN TO IPC4012, CLASS 2.
8. MARKING:
   1. BOARD SHALL MEET THE REQUIREMENTS OF UL-796K WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO,UL FILE NUMBER, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
9. TEST REQUIREMENTS:
   1. 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-D-356 NET LIST FOR OPENS AND SHORTS.
10. THIEVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
11. TEAR DROPS SHALL BE ADDED ON INTERNAL AND EXTERNAL LAYER FOR ALL THE VIA'S AND THROUGH HOLE PADS.
12. FINISHED PCB THICKNESS SHALL BE 0.080" +/-10%.
13. MIN TRACE WIDTH/SPACING ON BOARD IS 0.003"/0.003".
14. ALL THE IMPEDANCE SHALL BE MATCHED AS PER IMPEDANCE TABLE WITH +/-10% TOLERANCE.
15. ALL UNCONNECTED VIA'S SHALL BE SUPPRESSED IN INTERNAL LAYERS.
16. V-SCORE TO BE DONE AS PER DETAIL'A'.

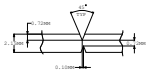
BACKDRILLED TO BE DONE FROM L04 TO L14.
BACKDRILLED TO BE DONE FROM L11 TO L16.

DRILL CHART: TOP TO BOTTOM

ALL UNITS ARE IN MILS

SYMBOL	FINISHED SIZE	TOLERANCE (MIN)	TOLERANCE (MAX)	PLATED	QTY
●	5.98	+2.0/-2.0	-	PLATED	64
●	7.99	+3.0/-3.0	-	PLATED	480
●	8.0	+3.0/-3.0	-	PLATED	5364
●	10.0	+3.0/-3.0	-	PLATED	335
●	14.0	+3.0/-3.0	-	PLATED	16
●	24.0	+3.0/-3.0	-	PLATED	20
●	28.0	+3.0/-2.0	-	PLATED	149
●	32.0	+3.0/-2.0	-	PLATED	2
●	22.0	+3.0/-3.0	-	PLATED	22
●	26.0	+3.0/-3.0	-	PLATED	13
●	60.0	+3.0/-3.0	-	PLATED	17
●	64.0	+2.0/-2.0	-	PLATED	28
●	84.0	+3.0/-3.0	-	PLATED	40
●	69.0	+3.0/-2.0	-	PLATED	2
●	66.0	+3.0/-3.0	-	PLATED	2
●	80.0	+3.0/-3.0	-	PLATED	4
●	116.0	+3.0/-3.0	-	PLATED	2
●	32.0	+3.0/-3.0	-	NON-PLATED	2
●	36.0	+2.0/-2.0	-	NON-PLATED	2
●	60.0	+3.0/-3.0	-	NON-PLATED	4
●	64.0	+2.0/-2.0	-	NON-PLATED	2
●	62.0	+2.0/-2.0	-	NON-PLATED	2
●	92.0	+2.0/-2.0	-	NON-PLATED	2
●	104.0	+3.0/-3.0	-	NON-PLATED	7
●	126.0	+3.0/-3.0	-	NON-PLATED	6
●	48.0x22.0	+3.0/-3.0	+3.0/-3.0	PLATED	4
●	48.0x24.0	+3.0/-3.0	+3.0/-3.0	PLATED	4
●	52.0x24.0	+3.0/-2.0	+3.0/-3.0	PLATED	2
●	62.0x24.0	+3.0/-3.0	+3.0/-3.0	PLATED	2
●	66.0x32.0	+3.0/-2.0	+3.0/-3.0	PLATED	2
●	68.0x39.0	+3.0/-3.0	+3.0/-3.0	PLATED	2
●	80.0x24.0	+3.0/-3.0	+3.0/-3.0	PLATED	2
●	84.0x32.0	+3.0/-3.0	+3.0/-3.0	PLATED	2





DETAIL-A(V-GROOVE DETAILS)
SCALE:NTS

LAYER STACKUP

LAYER NAME	FINISHED Cu	X-SECTION	DIELECTRIC THICKNESS [INCHES]
PRIMARY SIDE SILKSCREEN			
PRIMARY SIDE SOLDERMASK			
L01 PRIMARY SIDE	1.3loz		0.00440
L02 GROUND-PLANE-1	1oz.		0.00400
L03 INNER-SIGNAL-1	1oz.		0.00420
L04 GROUND-PLANE-2	1oz.		0.00400
L05 INNER-SIGNAL-2	1oz.		0.00420
L06 GROUND-PLANE-3	1oz.		0.00400
L07 INNER-SIGNAL-3	1oz.		0.00420
L08 POWER-PLANE-1	1oz.		0.00400
L09 POWER-PLANE-2	1oz.		0.00420
L10 INNER-SIGNAL-4	1oz.		0.00400
L11 GROUND-PLANE-4	1oz.		0.00420
L12 INNER-SIGNAL-5	1oz.		0.00400
L13 GROUND-PLANE-5	1oz.		0.00420
L14 GROUND-PLANE-6	1oz.		0.00400
L15 GROUND-PLANE-6	1oz.		0.00440
L16 SECONDARY SIDE	1.3loz		
SECONDARY SIDE SOLDERMASK			
SECONDARY SIDE SILKSCREEN			

IMPEDANCE SPECIFICATIONS

S1#	TYPE	LAYER	TRACEWIDTH(Mils)	SPACING(Mils)	IMPEDANCE(Ohms)	REF LAYER
01.	EDGE COUPLED MICROSTRIP	L1/L16	4.7	5.6	120	L3/L14
02.	EDGE COUPLED MICROSTRIP	L1/L16	4.7	5.6	100	L2/L15
03.	EDGE COUPLED MICROSTRIP	L16	6.3	5.7	90	L2/L15
04.	EDGE COUPLED MICROSTRIP	L1/L16	7.4	5.8	85	L2/L15
05.	EDGE COUPLED MICROSTRIP	L1	9	5	80	L2
06.	MICROSTRIP	L1	13	-	40	L2
07.	MICROSTRIP	L1/L16	9	-	50	L2/L15
08.	EDGE COUPLED STRIPLINE	L3,L5,L7, L10,L12,L14	3	5	100	L2/L4,L4/L6,L6/L8, L9/L11,L11/L13,L13/L15
09.	EDGE COUPLED STRIPLINE	L10,L12,L14	3.8	5	90	L9/L11,L11/L13,L13/L15
10.	EDGE COUPLED STRIPLINE	L14	4.3	5	85	L13/L15
11.	EDGE COUPLED STRIPLINE	L3,L5	5	5	80	L2/L4,L4/L6
12.	EDGE COUPLED STRIPLINE	L7	7.3	5.4	66	L6/L8
13.	EDGE COUPLED STRIPLINE	L3	3	15	132	L2/L4
14.	STRIPLINE	L3,L5,L7, L10,L12,L14	3.8	-	50	L2/L4,L4/L6,L6/L8, L9/L11,L11/L13,L13/L15
15.	STRIPLINE	L7	8	-	33	L6/L8
16.	STRIPLINE	L3	3	-	66	L2/L4
17.	STRIPLINE	L3,L5,L10	6	-	40	L2/L4,L4/L6,L9/L11
18.						

SIGNATURES	DATE
LAYOUT BY AG	211024
REVIEWED BY SA	211024
APPROVED BY AMB	211024

TEXAS INSTRUMENTS

PROC154E4

AM69 PROCESSOR STARTER KIT

SIZE		Rev
D		E4
SCALE: NONE		SHEET 1 OF 23