

AM625-Q1 / AM620-Q1 -LOW POWER STARTER KIT SK (EVM) With TPS6521920 PMIC

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Revision Number

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REV	E2A
VER	2.1

D-Note :-

SK/EVM is a device evaluation board or platform. The SK/EVM is not a reference design. In some cases the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SOC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata, and TRM when designing their custom board. The information found in the datasheet should always take precedence over the SK/EVM implementation.

R-Note:-

- * Verify the DNI components configuration with respect to the SK schematics (Use PDF) after completion of board design before board assembly.
- * A standard 5% tolerance resistor can be used for most of the series and parallel pull resistor.
- * Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build. (Refer FAQs listed for additional details)

KEY LINKS TO COLLATERALS

Hardware Design Guide : https://www.ti.com/lit/an/sprad05b/sprad05b.pdf
Schematic Design and Review Checklist : https://www.ti.com/lit/an/sprad21d/sprad21d.pdf
PMIC Power Solutions application note : https://www.ti.com/lit/an/slvafd0b/slvafd0b.pdf
DDR Board Design and Layout Guidelines : https://www.ti.com/lit/an/sprad06/sprad06.pdf
SKs (Starter Kits) for reference : SK-AM62B, SK-AM62B-P1, SK-AM62-LP, SK-AM62-SIP, SK-AM62A-LP, SK-AM62P-LP

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C		E2A
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REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
2.01	13 APR 2023	Drafted from E2 Schematics	Mistral Design Team	Deepak NS	Krishna Prasad A
2.02	13 APR 2023	Added M.2 screw and standoffs (9774015243R, MPMS 002 0005 PH , 3356) Changed the value of R339 resistor to 7.5K Chnaged the U14 part to TPD2E2U06DRL	Mistral Design Team	Deepak NS	Krishna Prasad A
2.1	24 MAY 2024	Updated SoC Part Number, Enabled Voltage ratings for all the capacitors and added Design Review notes Moved to DNI : R581, C5, C43, C41, C338, C376, C140, C416, Q4, U1, Y1 Moved to Mount : R324, 326, R323, R325, R321, R322, R320, R319, R661, R412, R496, R527, C533 C68 - 1uF changed to 2.2uF ; C533 - 0.1uF changed to 2.2uF ; C39 - 4.7uF changed to 1uF ; C40 - 0.1uF changed to 4.7uF ; C38,C384,C185,C192 - 1uF changed to 0.1uF ; C62,C53 - 9pF changed to 18pF ; C386,C186,C187 - 2.2uF changed to 1uF R124 - 10K_1% changed to Std 10K ; R91,R372,R371,R627,R628 - 22E_1% changed to 0E ; R51,R272,R400 - 49.9_1% changed to Std 10K ; R309 - 100K changed to Std 10K ; R630 - 2.2K changed to 1.5K ; R119,R147 - 3.4K_1% changed to 3.48K_1%	Mistral Design Team		

LINKS TO KEY FAQs

https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1279517/faq-am625-q1-or-am620-q1-custom-board-hardware-design-collaterals-to-get-started
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am62x-am62ax-am62px-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1337851/faq-am625-q1-am620-q1-custom-board-hardware-design---design-and-review-notes-for-reuse-of-sk-am62-lp-schematics
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1280721/faq-am625-am623-am625sip-am625-q1-am620-q1-custom-board-hardware-design---faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit

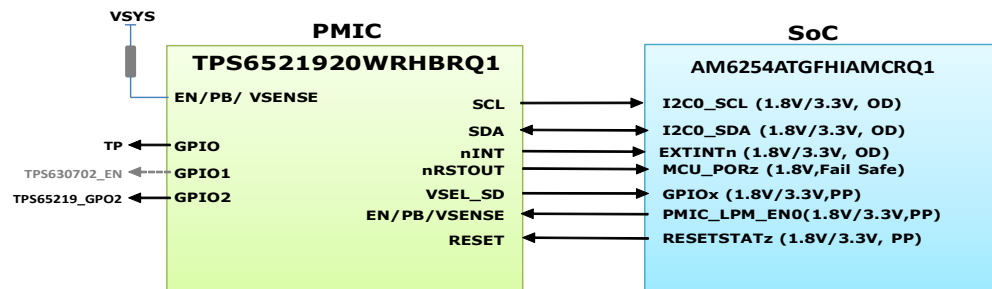
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Title REVISION HISTORY

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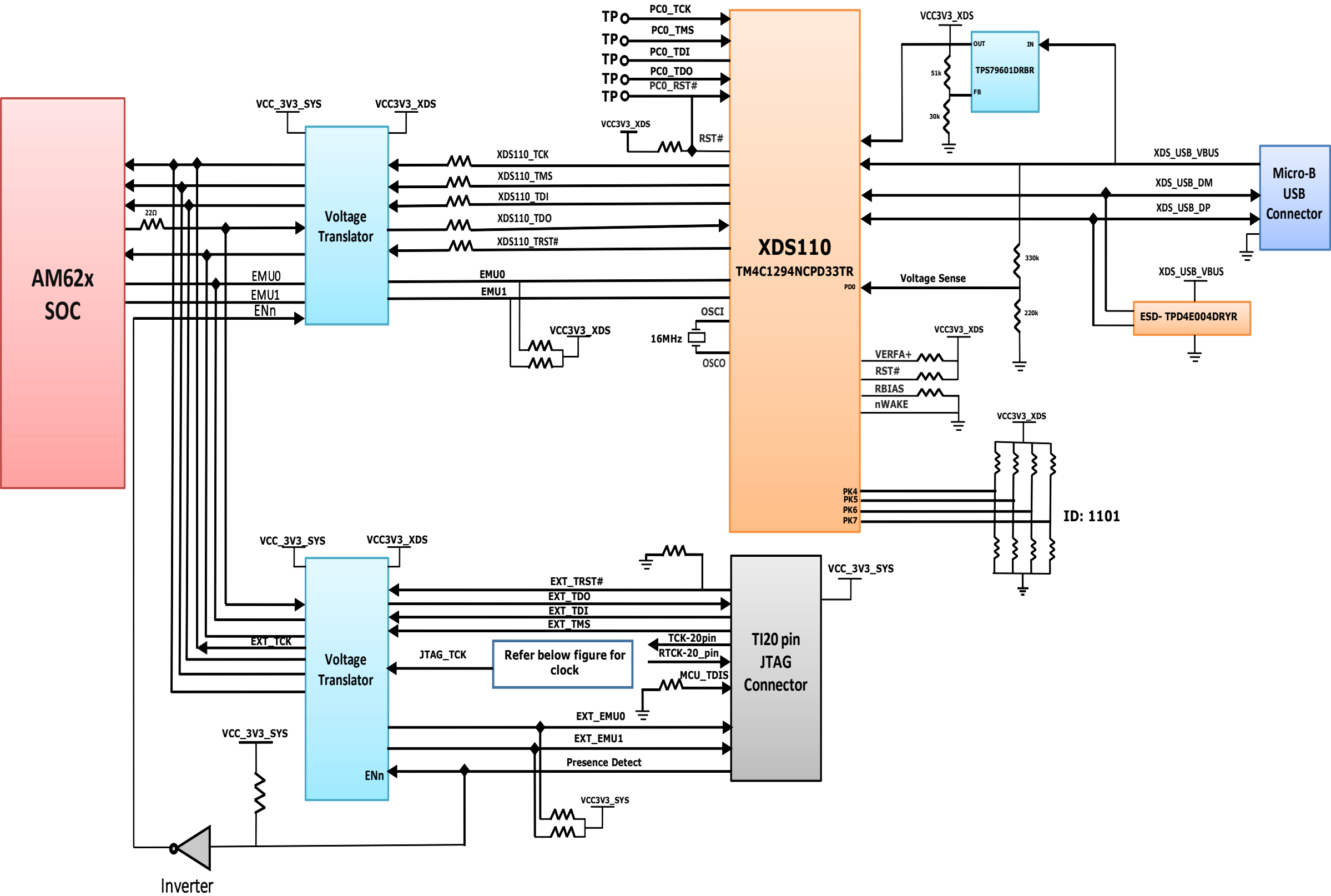
Rev E2.1



BLOCK DIAGRAM_XDS110

D-Note:-

Please follow SK-AM62P-LP implementations for latest updates on XDS110



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Title BLOCK DIAGRAM_XDS110

Size C
PROC124E2A AM62x-LOW POWER SKEVM

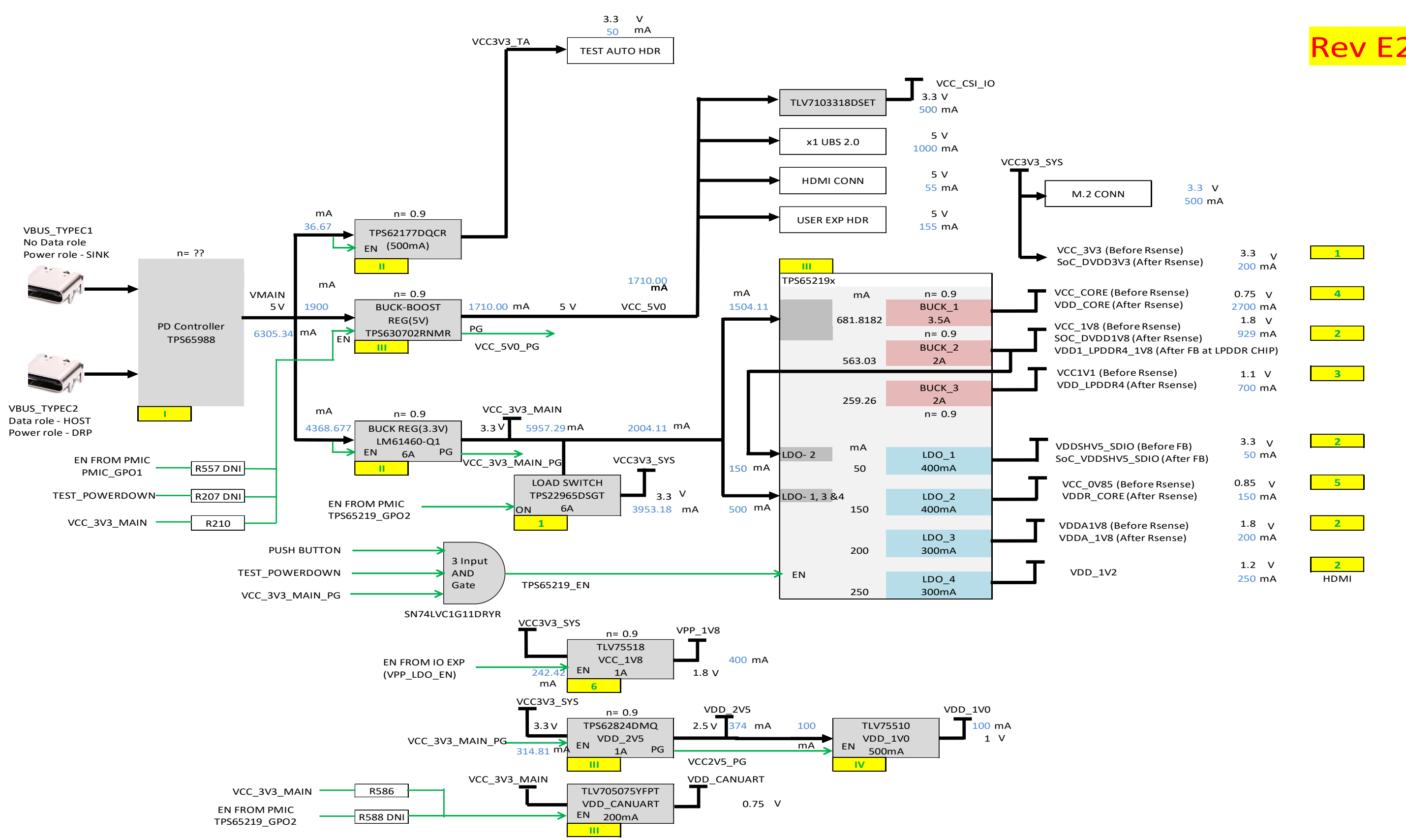
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POWER BLOCK DGM

Rev E2.1

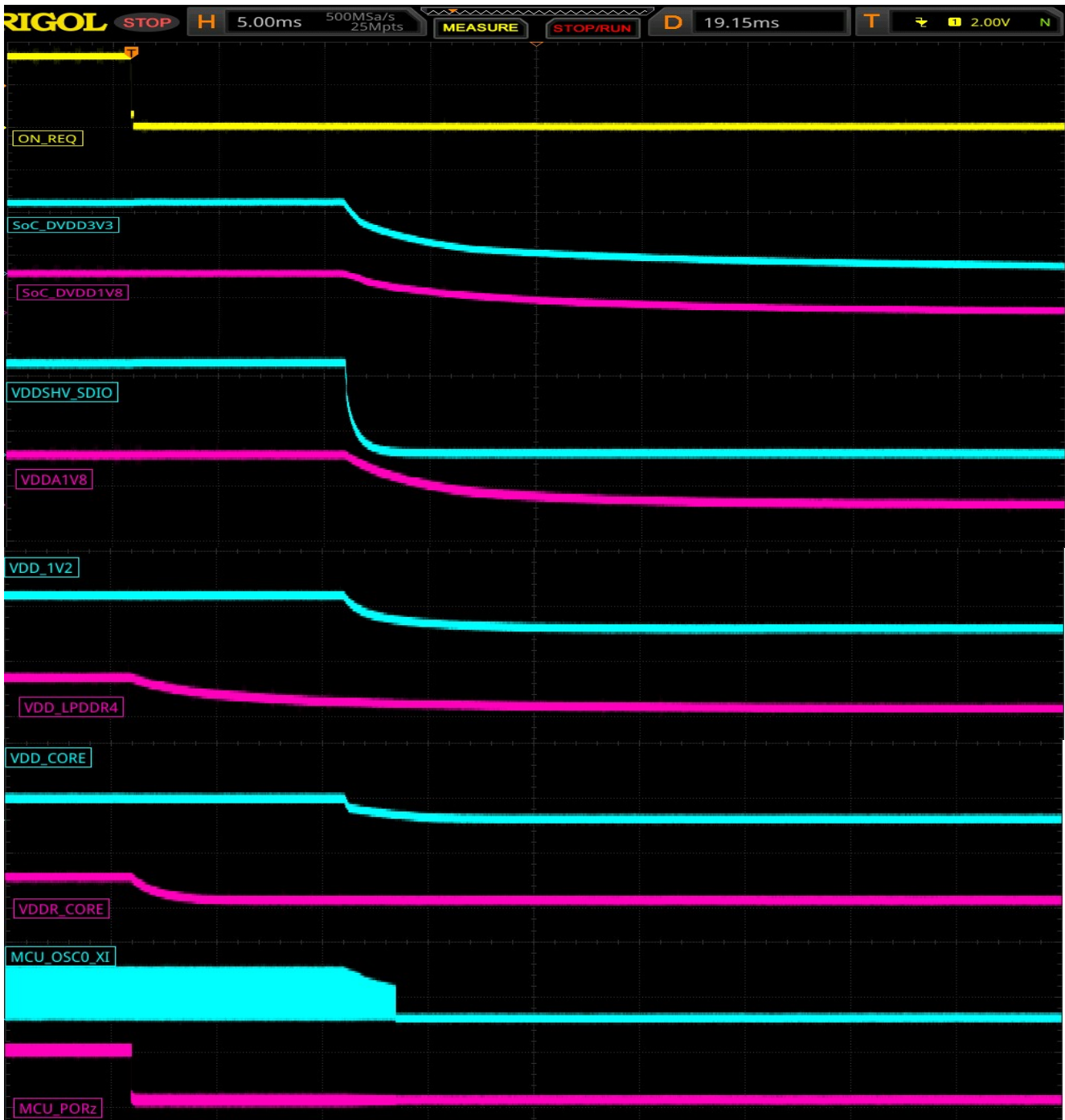


POWER SEQUENCE

POWER UP SEQUENCE



POWER DOWN SEQUENCE



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Title POWER SEQUENCE

Size C PROC124E2A AM62x-LOW POWER SKEVM

Rev E2A

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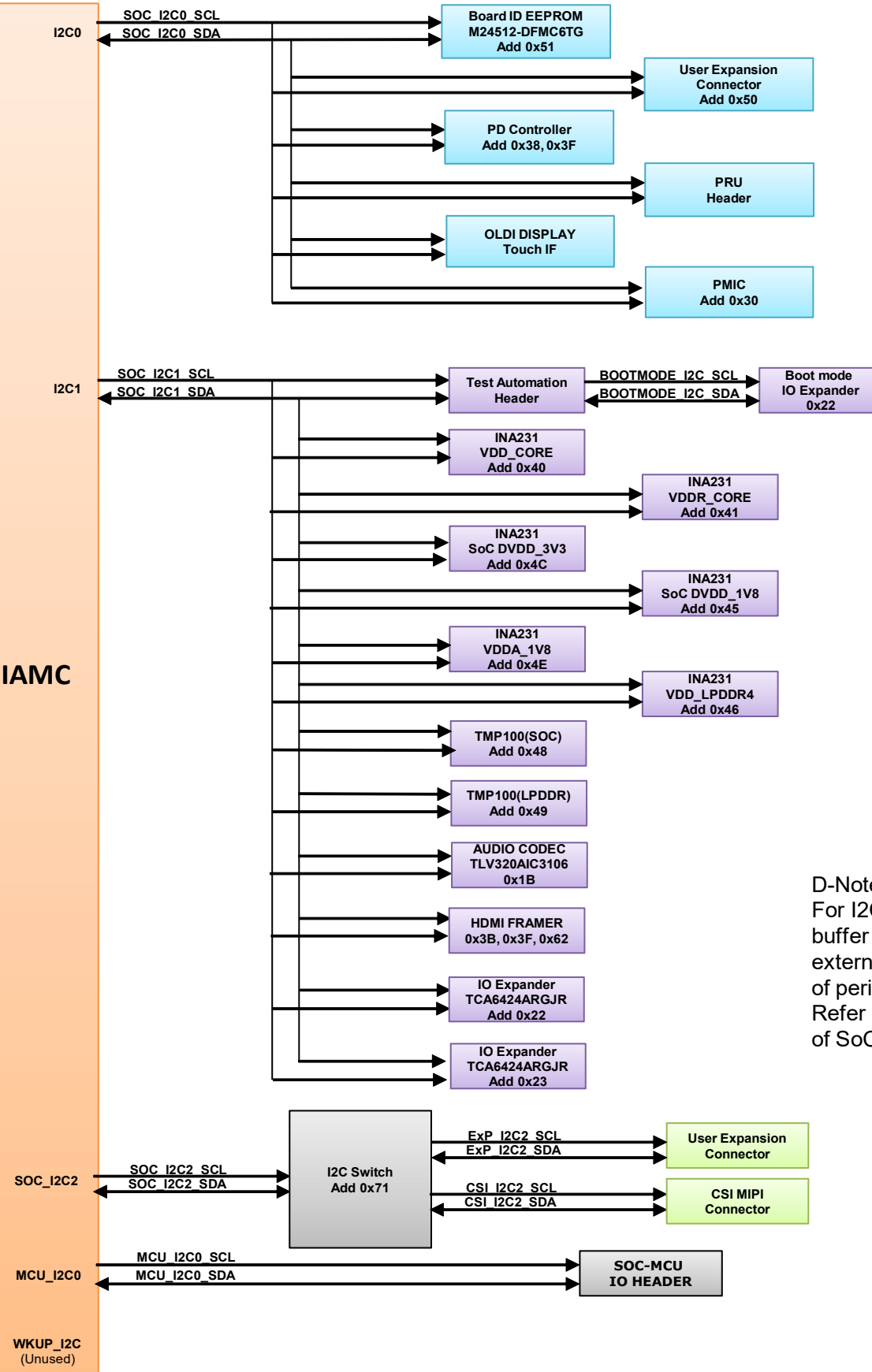
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I2C TREE

Rev E2.1

R-Note :-
Add - Indicates Address

AM6254ATGGHIAMC
SOC



R-Note :-
Refer below section of the data sheet
Timing and Switching Characteristics
I2C
Exceptions:

D-Note :-
For all emulated open-drain output
LVCMOS I2C interfaces. (I2C0, I2C1,
I2C2, I2C3) pullup resistors are
recommended
Location of the pullup is not a concern
It is recommended to connect the
pullups with the shortest possible stub.

D-Note :-
For I2C interfaces with open-drain output type
buffer (MCU_I2C0 and WKUP_I2C0), an
external pullup is recommended irrespective
of peripheral usage and IO configuration.
Refer Pin Connectivity Requirements section
of SoC data sheet

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Title I2C TREE		
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GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN	VOLTAGE CONNECTED
									ON SOC SIDE	ON SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC	ENABLE	MCU_GPIO0_0	MCU_SPI0_CS0	OUTPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn/PRU_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
	PRU Connector Interrupt									
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	MCU Header GPIO0_16	MCU_GPIO0_16	GPIO	MCU_GPIO0_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CANUART	SoC_DVDD3V3
7	MCU Header GPIO0_15	MCU_GPIO0_15	GPIO	MCU_GPIO0_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CANUART	SoC_DVDD3V3
8	PMIC Interrupt	PMIC_INT_B	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV3	SoC_DVDD3V3
9	IO Expander Interrupt		INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	SoC_DVDD3V3
10	TEST GPIO1 from Test Automation Connector/ User Interrupt Push Button									
11	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
12	CAN_FD_WKUP_SW signal from switch	ETH_CAN_INH_SOC	INTERRUPT	MCU_GPIO0_19	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
13	CAN_FD_WKUP_HDR_INH signal from header									
14	User EXP Conn GPIO	EXP_GPIO1_22	GPIO	GPIO1_22	UART0_CTSn	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	GPIO1_23	UART0_RTSn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
16	User Interrupt									
17	User EXP Conn GPIO	EXP_GPIO0_14_LT	GPIO	GPIO0_14	OSPI0_CSn3	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
18	PMIC Standby Enable	PMIC_STBY	ENABLE	MCU_GPIO0_22	PMIC_LPM_EN0	OUTPUT	HIGH	HIGH	VDDSHV_CANUART	SoC_DVDD3V3
19	User EXP Conn GPIO	EXP_EHRPWM1_B	GPIO	GPIO1_10	MCASP0_AXR0	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 01										
1	eMMC Reset control GPIO	GPIO_EMMC_RSTN	RESET	IO EXPANDER-P11		OUTPUT	HIGH	LOW		VCC_3V3_SYS
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P01		OUTPUT	HIGH	LOW		VCC_3V3_SYS
3	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P00		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	LOW		VCC_3V3_SYS
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER-P04		OUTPUT	LOW	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P06		OUTPUT	LOW	HIGH		VCC_3V3_SYS
8	Audio Codec Reset Control GPIO	GPIO_AUD_RSTN	RESET	IO EXPANDER-P10		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
10	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER-P02		INPUT	HIGH	LOW		VCC_3V3_SYS
11	SOC UART1 Mux Select	UART1_FET_BUF_EN	SELECT	IO EXPANDER-P12		OUTPUT	HIGH	LOW		VCC_3V3_SYS
12	BT UART WKUP Signal	BT_UART_WAKE_SOC	INTERRUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTN	RESET	IO EXPANDER-P14		OUTPUT	HIGH	LOW		VCC_3V3_SYS
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO0	INPUT/OUTPUT	IO EXPANDER-P15		NA	NA	NA		VCC_3V3_SYS
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER-P16		NA	NA	NA		VCC_3V3_SYS
16	OLDI Interrupt	GPIO_OLDI_INT	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	HDMI Interrupt	HDMI_INTN	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		INPUT	HIGH	LOW		VCC_3V3_SYS
19	MCASP1 Enable and Direction Control	MCASP1_FET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
20		MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
21		MCASP1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_SYS
22		UART1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC_3V3_SYS
23	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER - 02										
1	SoC SPI0 MUX Selection	SPI0_FET_SEL	ENABLE	IO EXPANDER-P20		OUTPUT	LOW	HIGH		VCC_3V3_SYS
2	SoC SPI0 MUX Enable	SPI0_FET_OE	CONTROL	IO EXPANDER-P21		OUTPUT	LOW	LOW		VCC_3V3_SYS
3	OLDI Reset	GPIO_OLDI_RSTn	RESET	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
5	CSI Regulator Enable (VCC_CSI_IO)	CSI_VLDO_SEL	ENABLE	IO EXPANDER-P26		OUTPUT	LOW	HIGH		VCC_3V3_SYS
6	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS
7	Wilink Enable	WL_LT_EN	ENABLE	IO EXPANDER-P10		OUTPUT	LOW	HIGH		VCC_3V3_SYS
8	CSI Reset control GPIO	CSI_RSTZ	RESET	IO EXPANDER-P11		OUTPUT	LOW	HIGH		VCC_3V3_SYS

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Title GPIO MAPPING TABLE

Size
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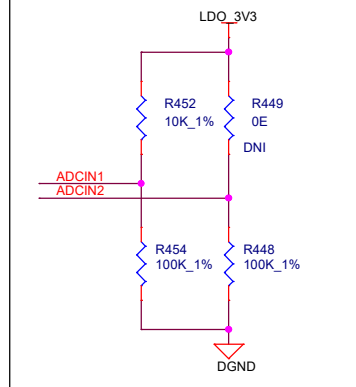
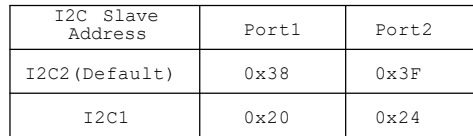
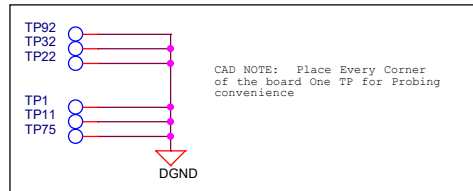
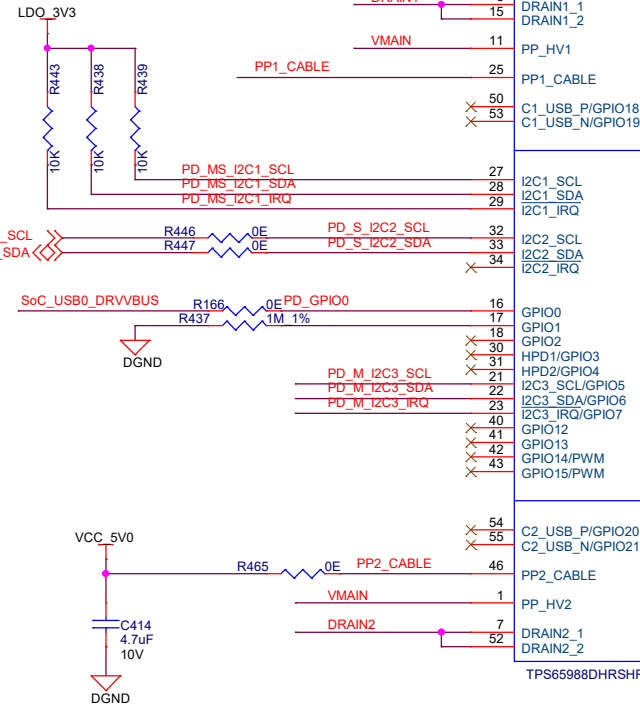
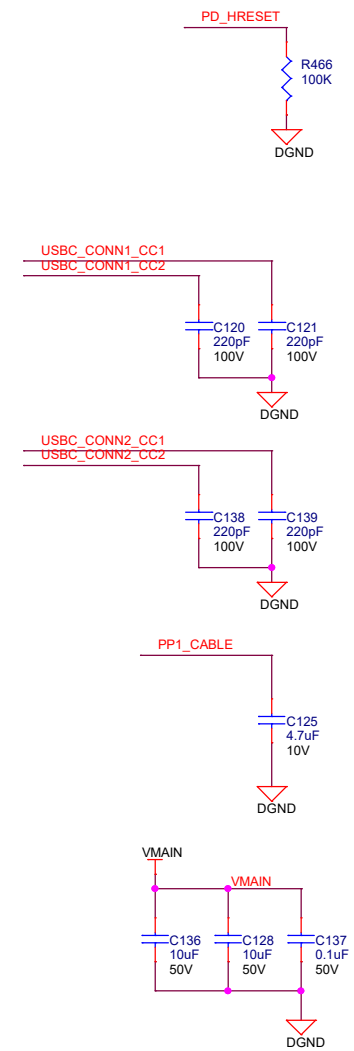
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USB TYPE-C PD CONTROLLER AND POWER SUPPLY

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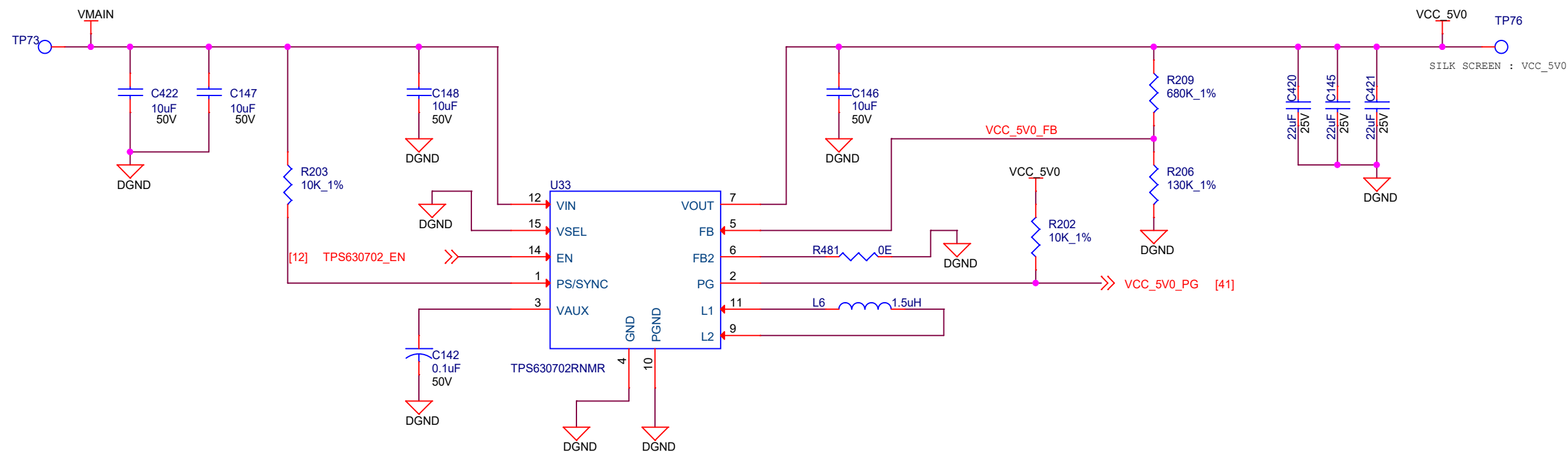
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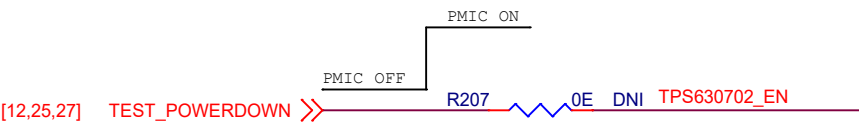
PERIPHERAL POWER SUPPLIES - 1

VinMin = 4.5V
VinMax = 15V
Vout = 5V @ 3.6A

D-Note :-
Add a Jumper or OR for isolation
or Current measurement for
preproduction board



D-Note :-
Power Cycle control from Test Automation



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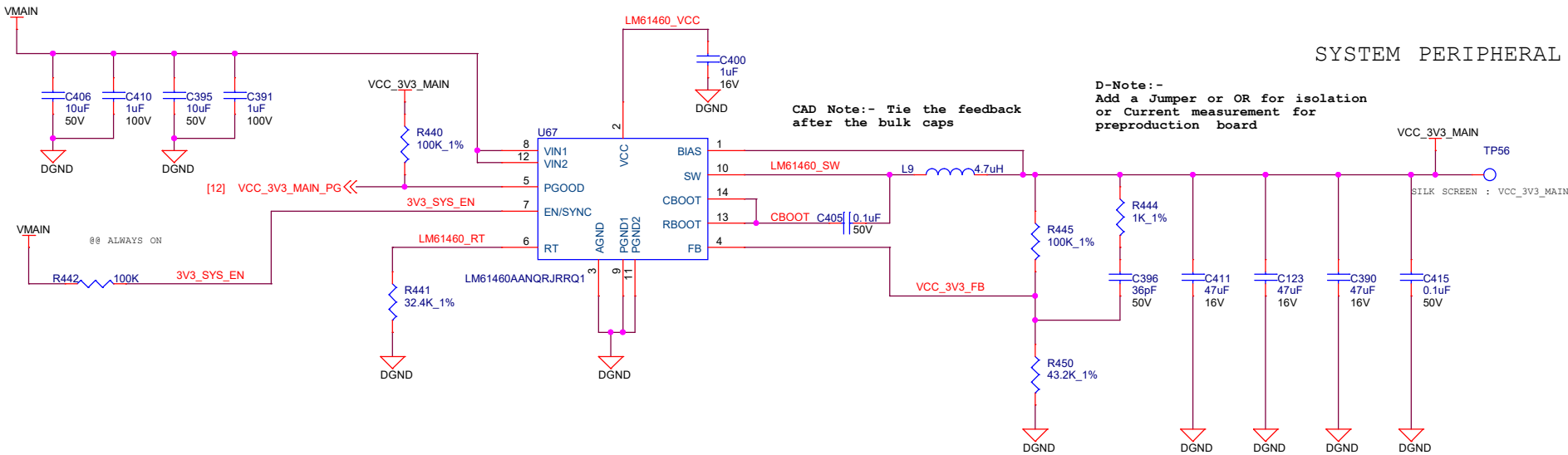


Title PERIPHERAL POWER SUPPLY -1		
Size B	Variant Name = PROC124E2A AM62x-LOW POWER SKEVM	Rev E2A
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PERIPHERAL POWER SUPPLIES - 2

VinMin = 4.5V
VinMax = 15V
Vout = 3.3V @ 6A

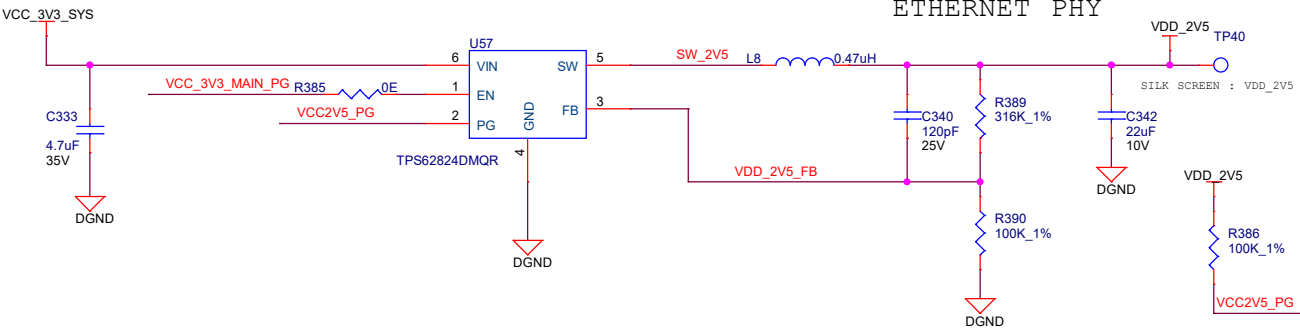
3.3V, 6.0 AMPS SUPPLY



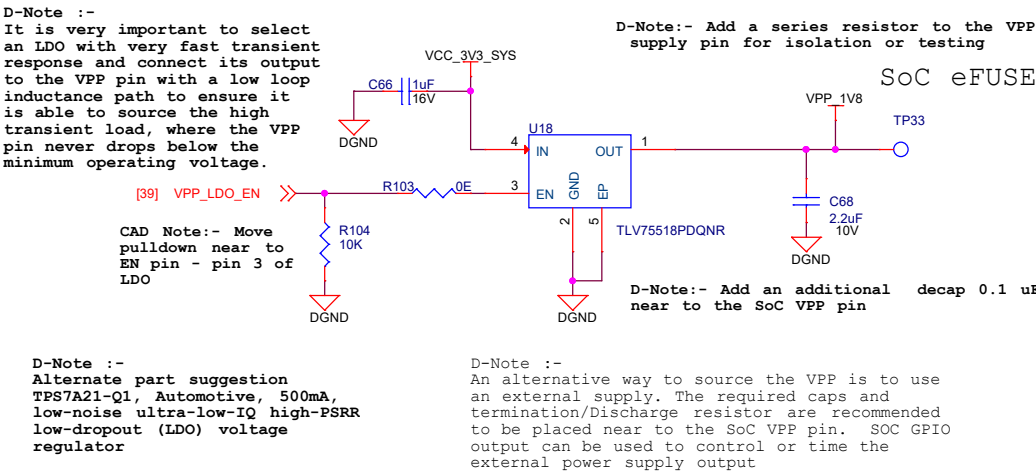
PERIPHERAL SUPPLY - ETHERNET PHY

2.5V, 1.0 AMP SUPPLY

ETHERNET PHY

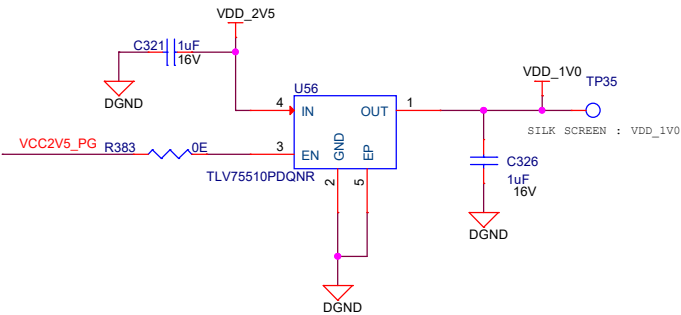


1.8V VPP, 0.5 AMP SUPPLY



PERIPHERAL SUPPLY - ETHERNET PHY

1.0V, 0.5 AMP



D-Note :-
Given the transient current requirement during eFuse programming, using load switch or FET switch may not be a recommended approach, It is recommended to use an LDO. A load or FET switch is likely to have too much voltage drop that can't be compensated like when using an LDO.

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Title PERIPHERAL POWER SUPPLY-2

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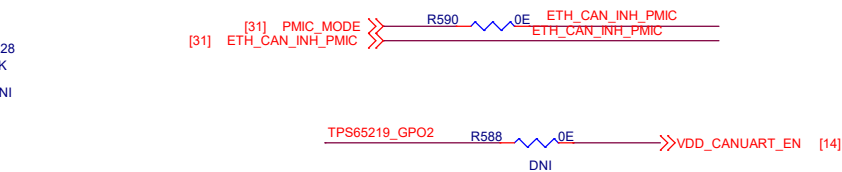
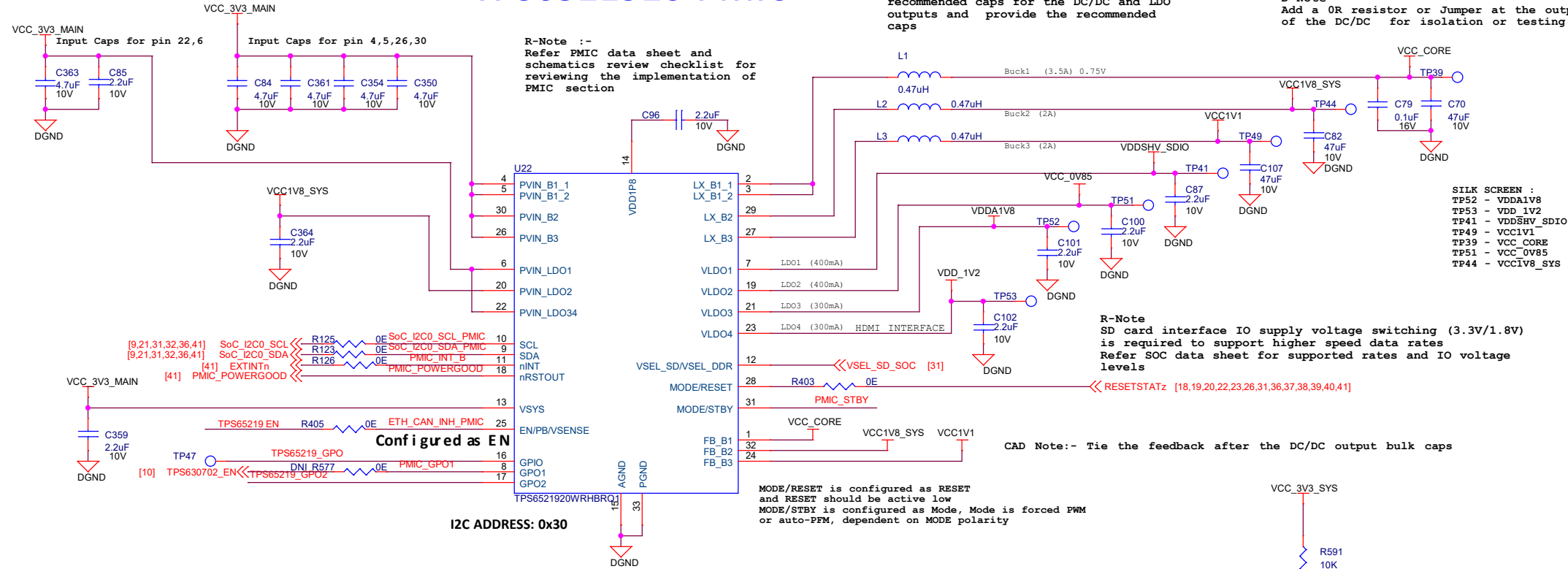
PMIC REGULATORS	VOLTAGE RAIL	CURRENT (mA)
BUCK 1	VCC_CORE(0.75V)	3500
BUCK 2	VCC_1V8	2000
BUCK 3	VDD_1V1	2000
LDO 1	VDDSHV_SDIO	400
LDO 2	VCC_0V85	400
LDO 3	VDDA1V8	300
LDO 4	VDD_1V2	300

D-Note :-
Show the bulk caps connection for each of the DC/DC inputs separately Add a 0.1 uF across the bulk caps PVIN_B1_1, PVIN_B1_2 can share the same bulk cap

SOC POWER SUPPLY PMIC TPS6521920 PMIC

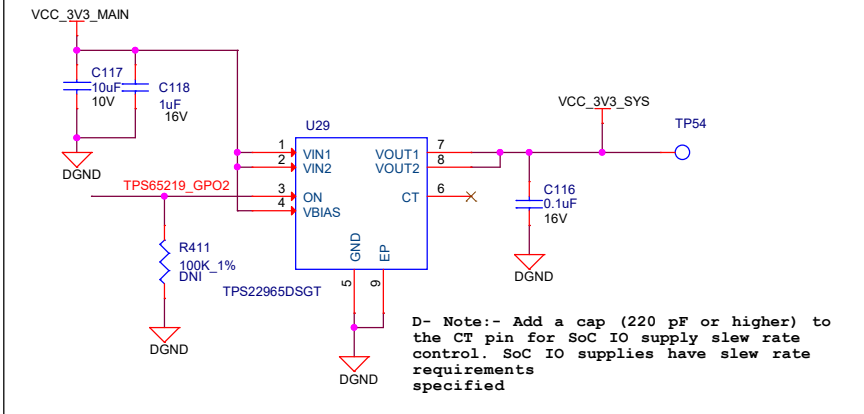
D-Note :-
Verify the PMIC data sheet for the recommended caps for the DC/DC and LDO outputs and provide the recommended caps

D-Note
Add a 0R resistor or Jumper at the output of the DC/DC for isolation or testing

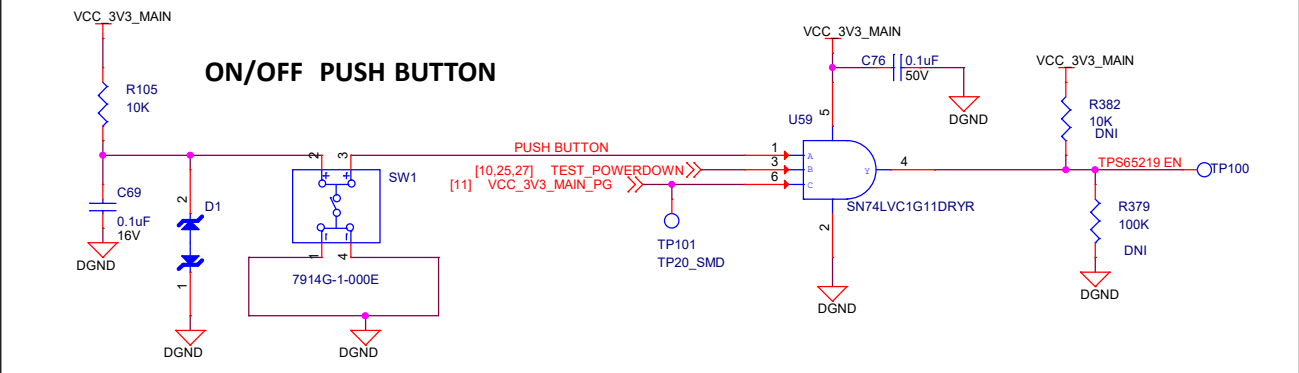


SOC 3.3V IO SUPPLY

VCC_3V3_SYS LOAD SWITCH



PMIC ON/OFF PUSH BUTTON LOGIC



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Title SOC POWER SUPPLY PMIC

Size C PROC124E2A AM62x-LOW POWER SKEVM

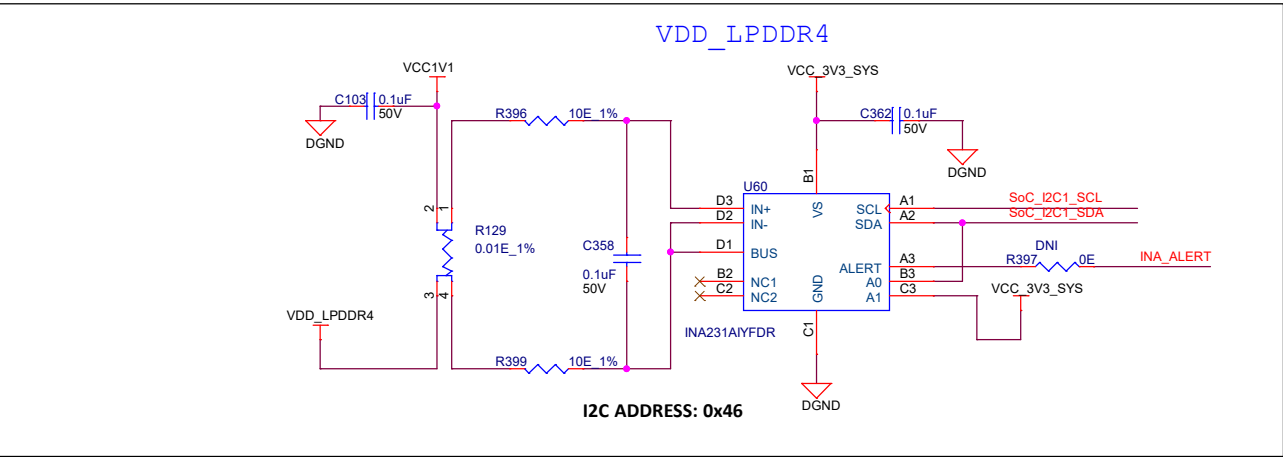
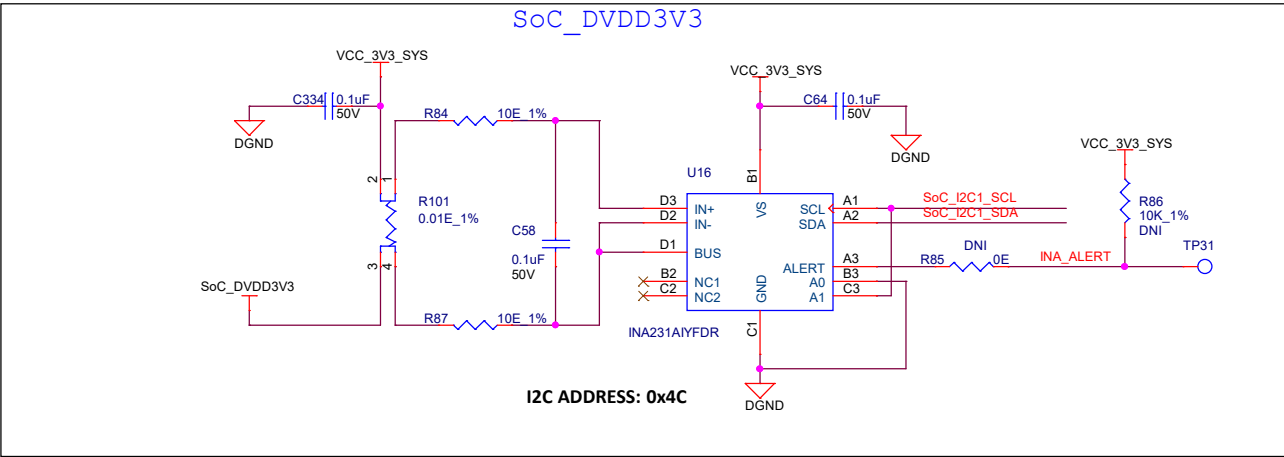
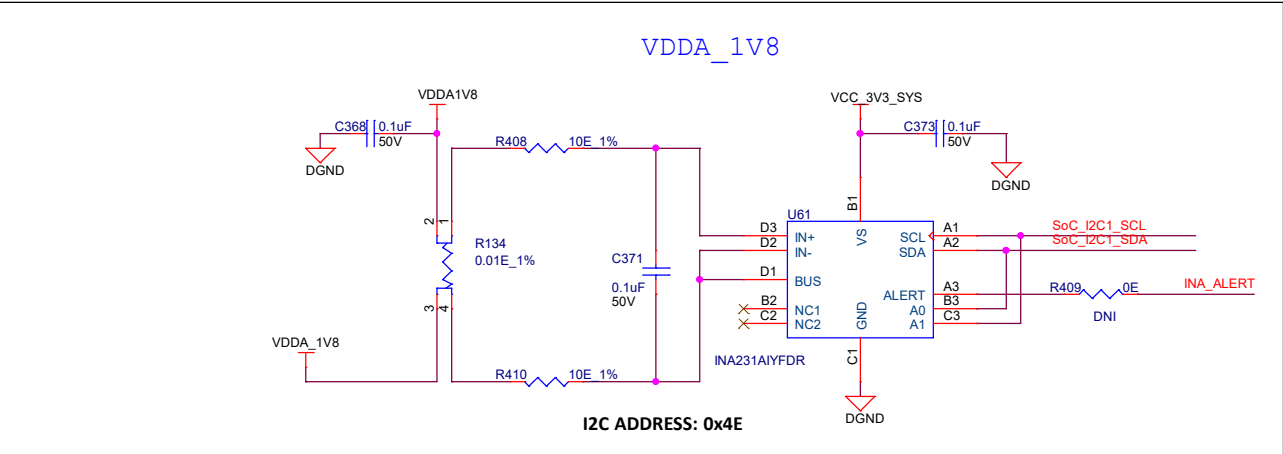
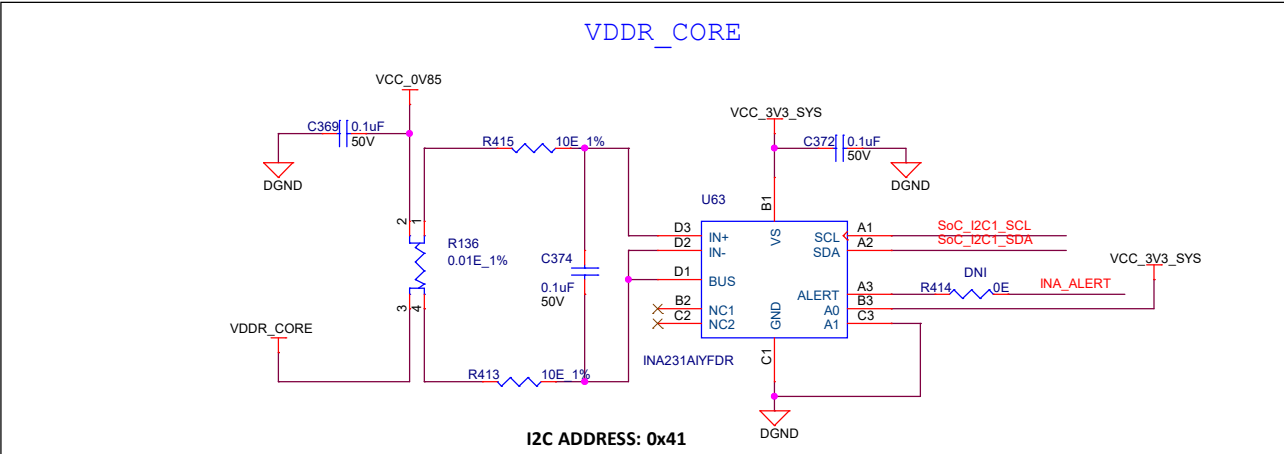
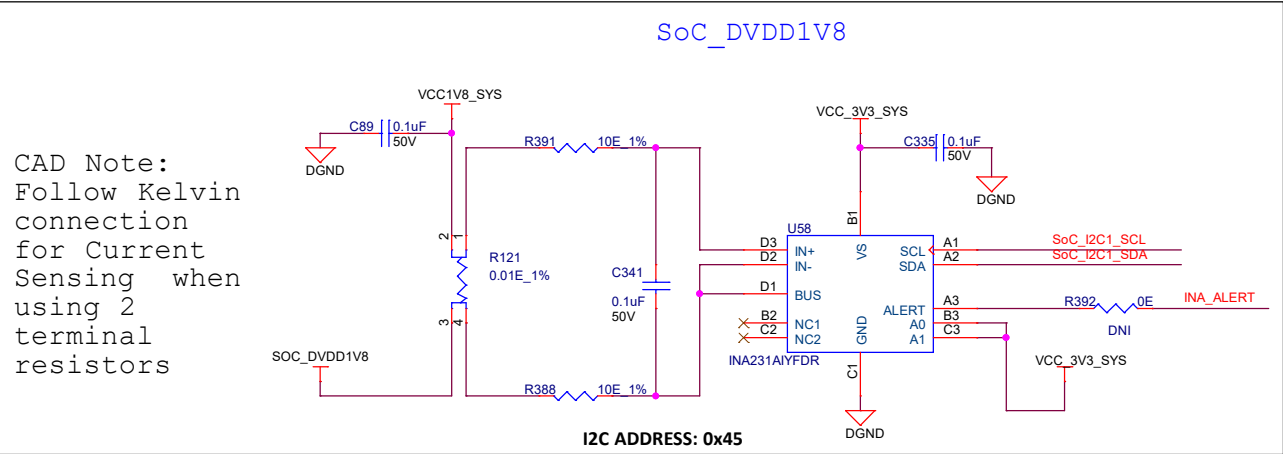
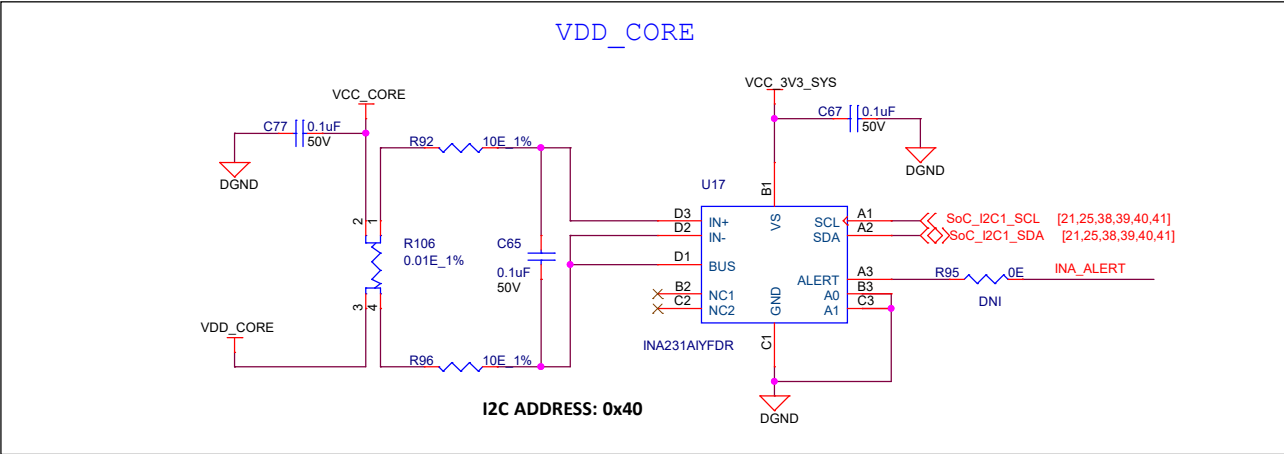
Date: Friday, May 24, 2024

Sheet 12 of 44

Rev E2A

CURRENT MONITORING DEVICES

D-Note:- Note the supply rail name change across the shunt when optimizing the design (Deleting the current sense resistor)



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4E
VCC1V1	VDD_LPDDR4	46

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Title CURRENT MONITORING DEVICES

Size C
PROC124E2A AM62x-LOW POWER SKEVM

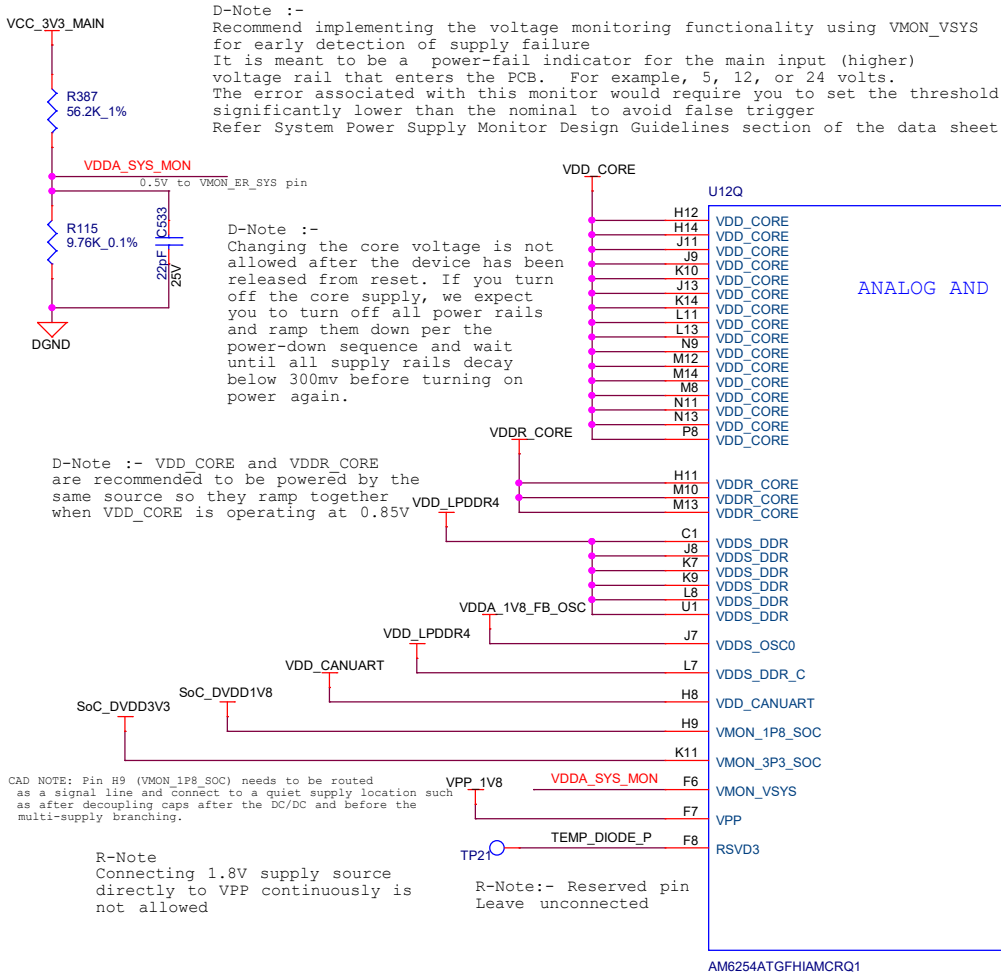
Rev E2A

Date: Friday, May 24, 2024

Sheet 13 of 44

SOC POWER

D-Note :-
Recommend implementing the voltage monitoring functionality using VMON_VSYS for early detection of supply failure
It is meant to be a power-fail indicator for the main input (higher) voltage rail that enters the PCB. For example, 5, 12, or 24 volts.
The error associated with this monitor would require you to set the threshold significantly lower than the nominal to avoid false trigger
Refer System Power Supply Monitor Design Guidelines section of the data sheet



D-Note :- VDD_CORE and VDDR_CORE are recommended to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85V

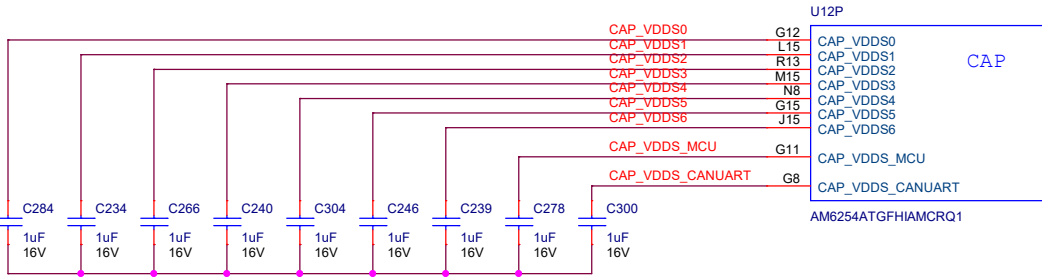
CAD NOTE: Pin H9 (VMON_1P8_SOC) needs to be routed as a signal line and connect to a quiet supply location such as after decoupling caps after the DC/DC and before the multi-supply branching.

R-Note
Connecting 1.8V supply source directly to VPP continuously is not allowed

R-Note:- Reserved pin
Leave unconnected

D-Note :-
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used.
It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized any time and the USB calibration procedure does not happen.
Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

D-Note :-
Refer Pin connectivity requirements to connect the CSIO supplies (analog and core) when CSIO interface is not used
Ferrite and Bulk Caps are optional when CSIO is not used and Boundary scan functionality is required

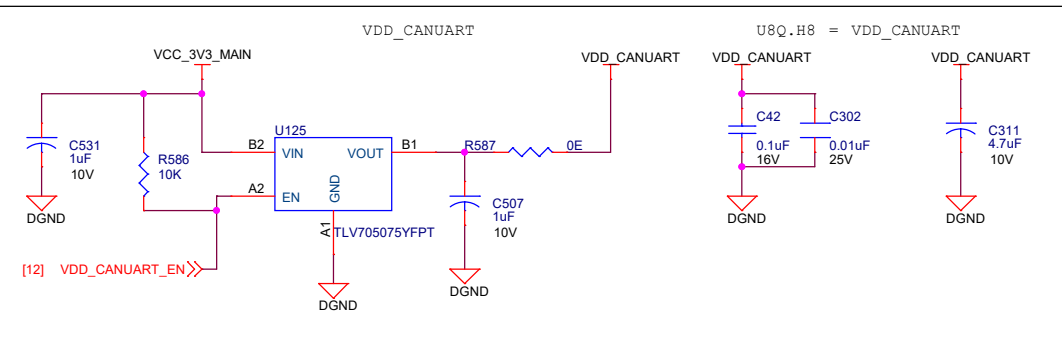
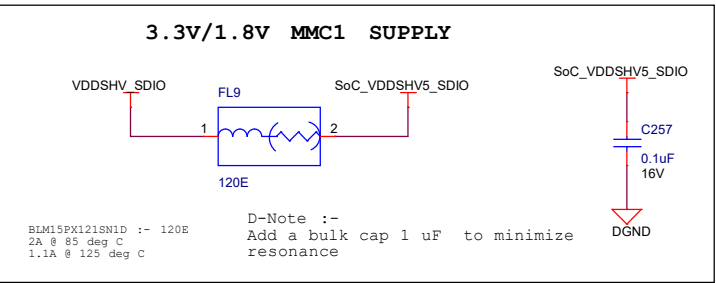
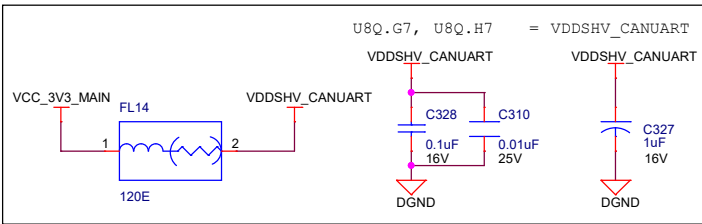
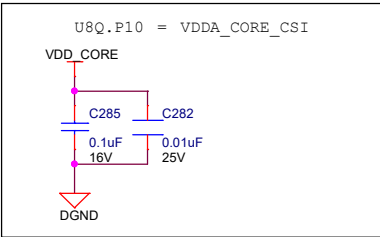
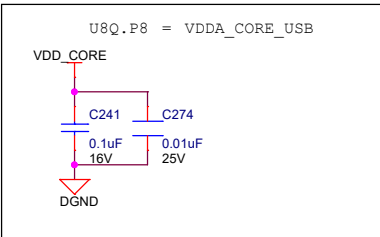
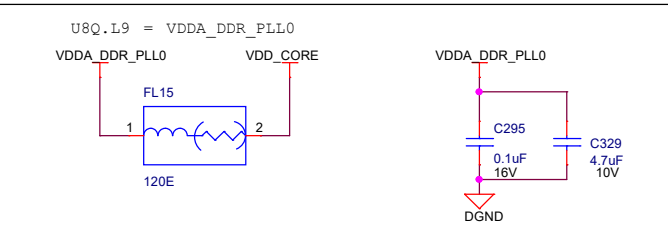
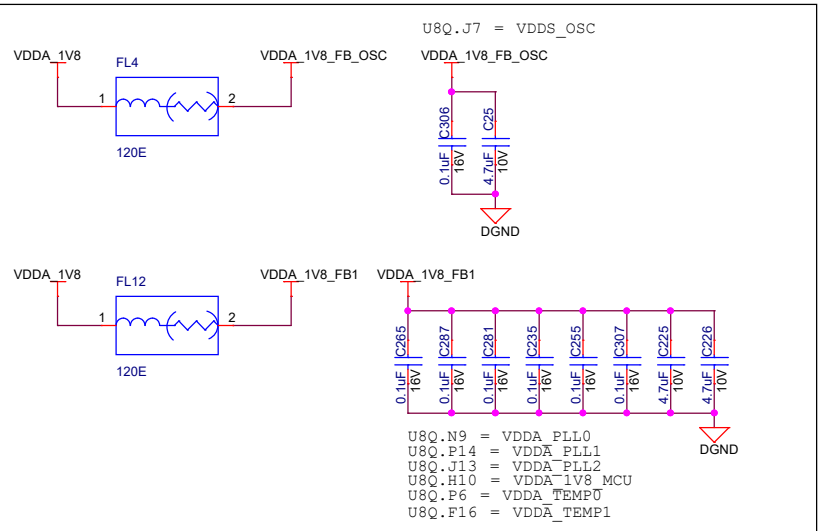
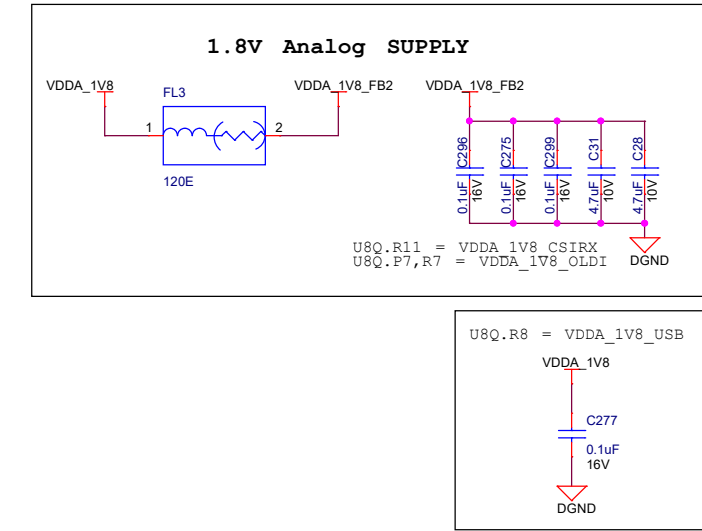


D-Note :-
Select cap with less the 1 ohm ESR
Ensure the PCB loop inductance is < 2.5 nH
Select 0201 package or smallest possible package
Refer SoC Data sheet

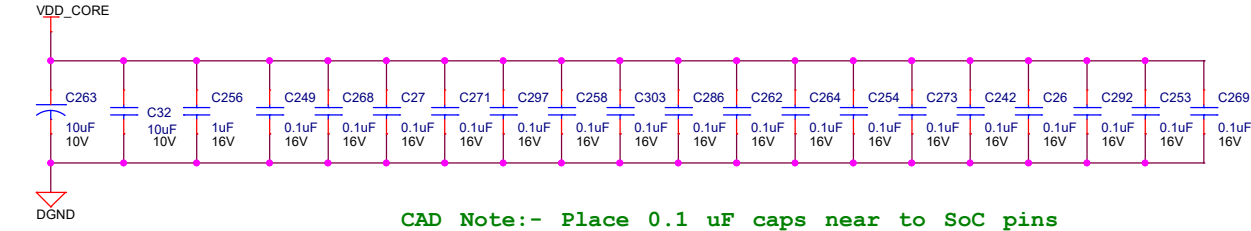
D-Note :-
Common SOC LVCMOS IO interface guidelines
1. Most of the SOC IOs are not fail-safe. No input should be applied before supply ramps.
2. SOC LVCMOS inputs have minimum slew rate requirements specified
3. SOC IO buffers are off during Reset. A pull is required near to the attached device being driven by the SOC IOs
4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull. When adding pull is not feasible, ensure the traces are routed away from noisy signals

D-Note :-
A Trace connected to SOC is effectively an antenna that will pick up noise. A potential will be generated on the signal when noise couples into the antenna. This potential will be largest on the highest impedance end of the signal. By placing a pull-up or pull-down near the SoC pin, we force the highest potential to the open-circuit end of the signal rather than the SoC end of the signal.

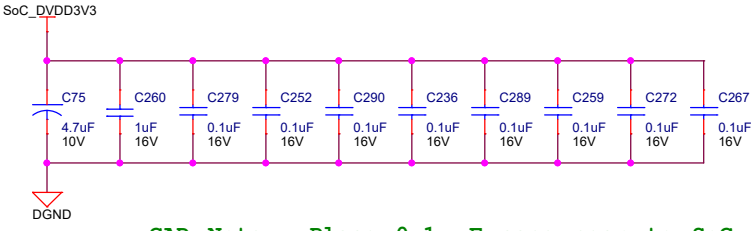
CORE SUPPLY



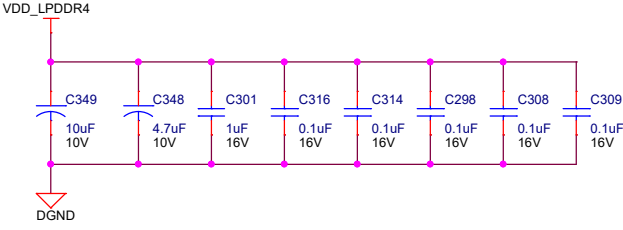
SOC POWER SUPPLIES - DECAPS



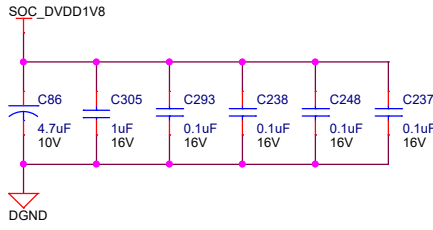
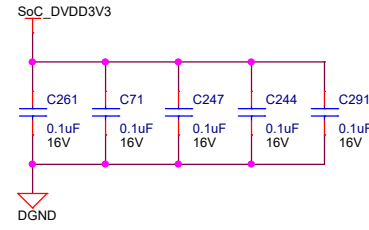
CAD Note:- Place 0.1 uF caps near to SoC pins



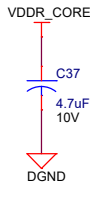
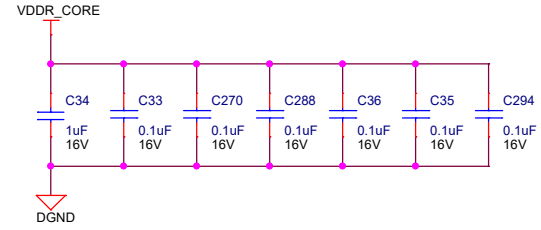
CAD Note:- Place 0.1 uF caps near to SoC pins



CAD Note:- Place 0.1 uF caps near to SoC pins

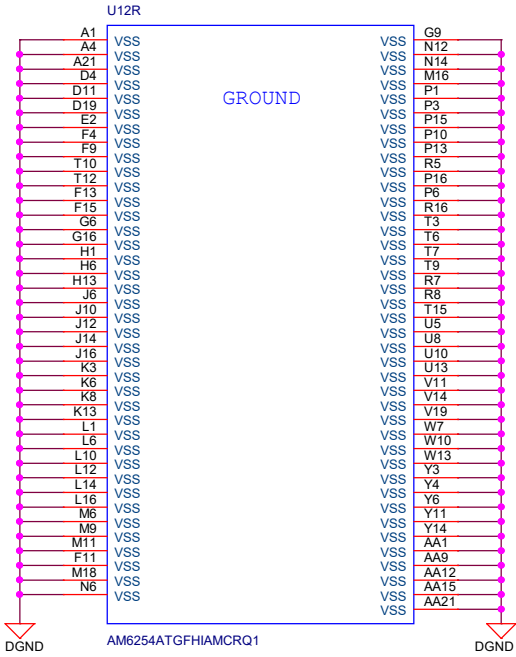


CAD Note:- Place 0.1 uF caps near to SoC pins



CAD Note:- Place 0.1 uF caps near to SoC pins

SOC VSS



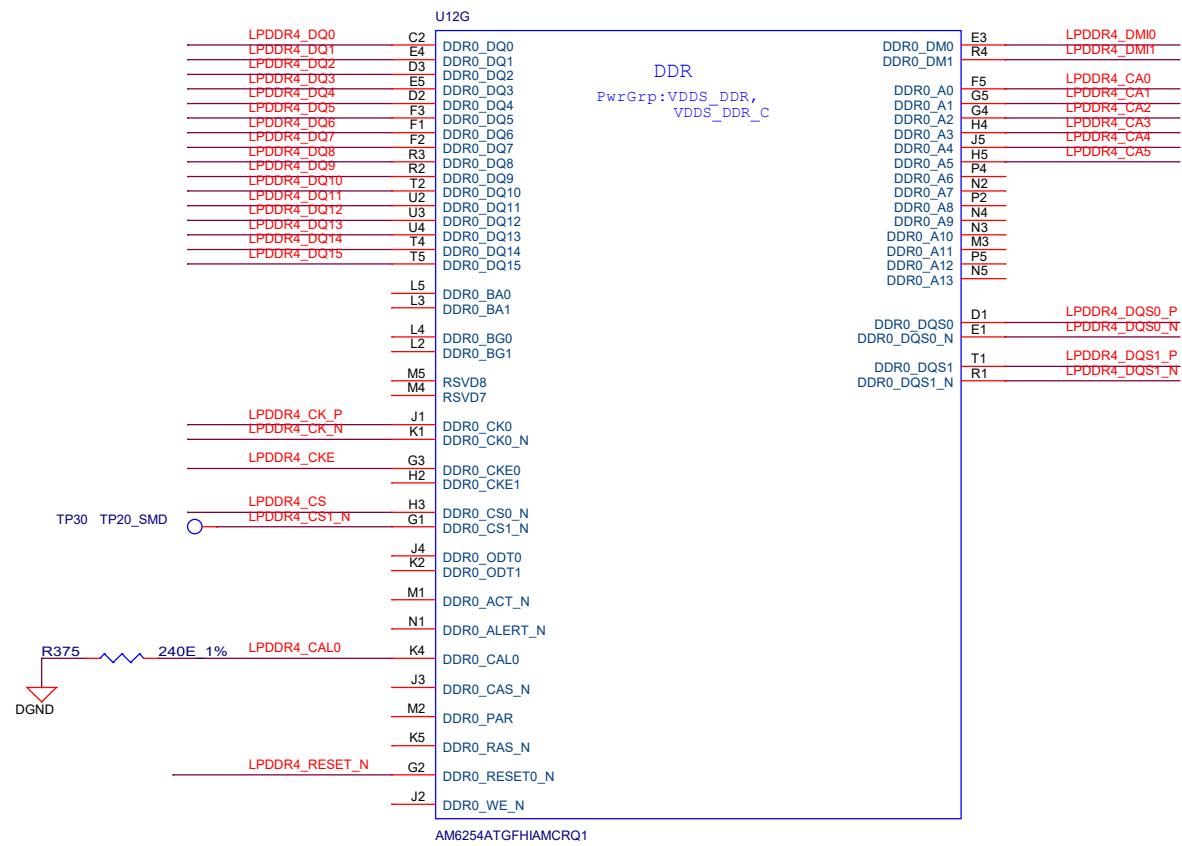
Designed for TI by Mistral Solutions Pvt Ltd



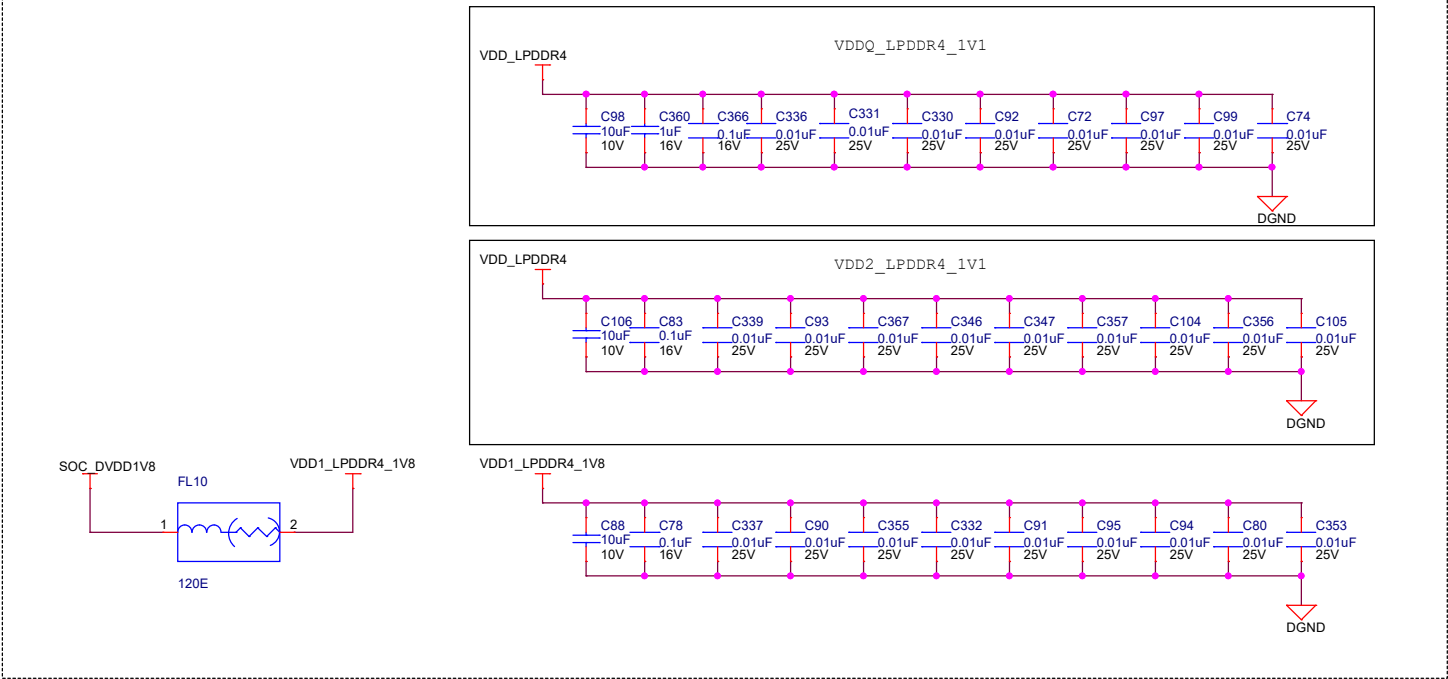
Title SOC POWER CAPS & SOC VSS

Size	Variant Name = PROC124E2A AM62x-LOW POWER SKEVM	Rev
C		
Date:	Friday, May 24, 2024	Sheet 15 of 44

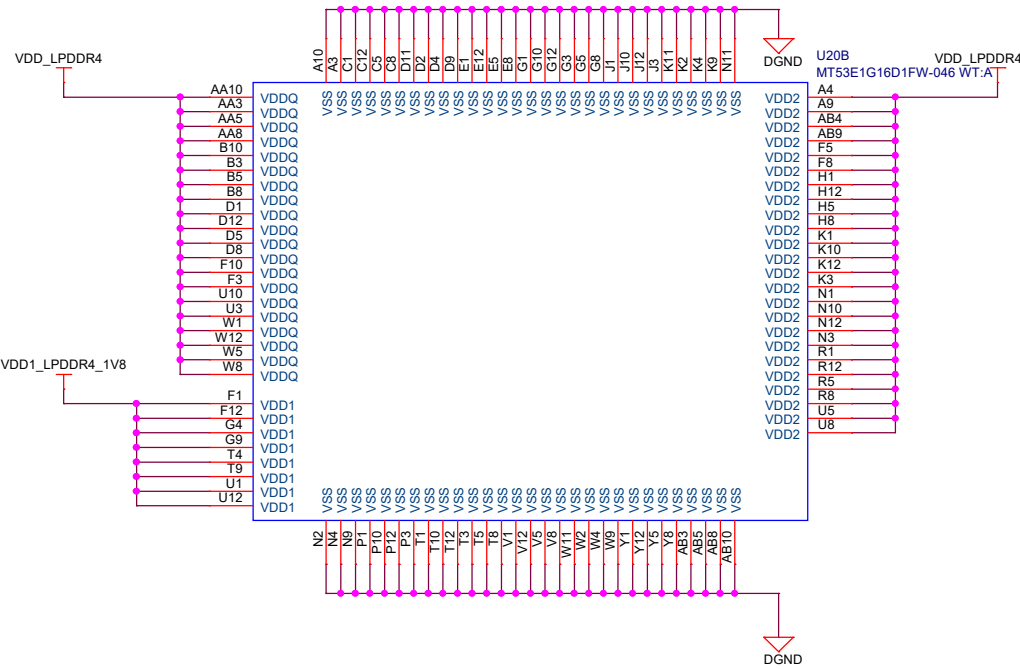
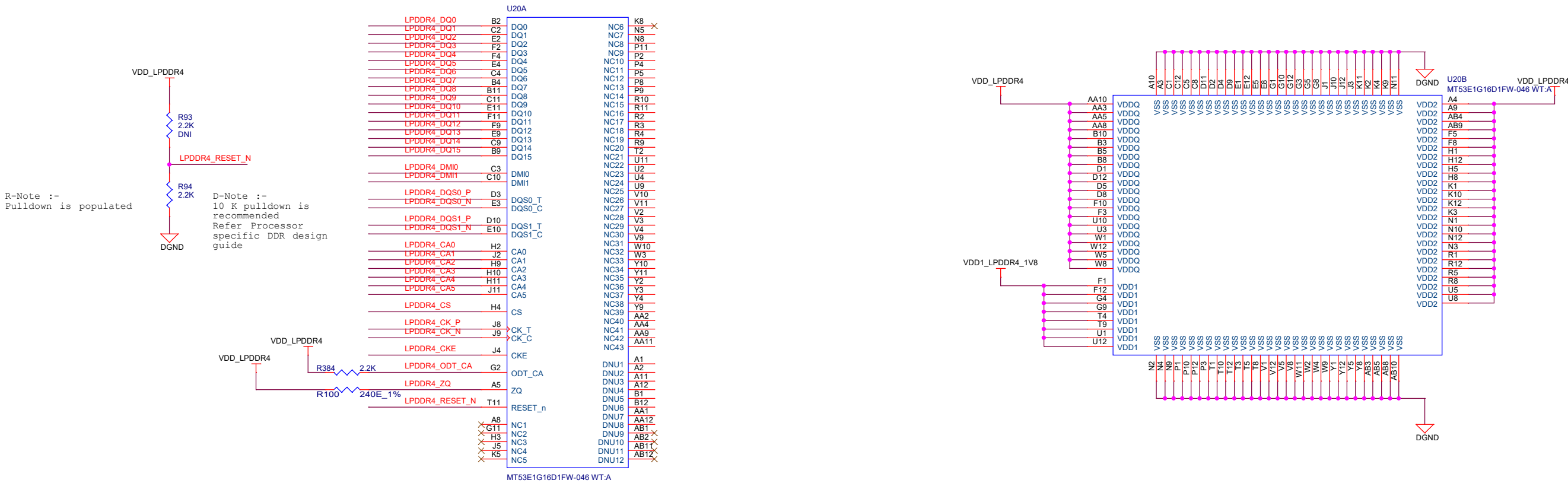
SOC LPDDR4 INTERFACE



LPDDR4 POWER DECAPS



LPDDR4 DEVICE



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Title SOC LPDDR4 INTERFACE

Size	Variant Name = PROC124E2A AM62x-LOW POWER SKEVM	Rev
C		E2A
Date:	Friday, May 24, 2024	Sheet 16 of 44

M.2 INTERFACE - SDIO



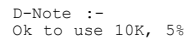
WILINK LEVEL TRANSLATORS



Design Note: WL_LT_EN = Active Hi



CAD Note:-
Place R1 & R2 close to each other to avoid stub.



SOC - MMC Interface

D-Note :-
OE provision on MMC0_CLK
Helps improve signal integrity

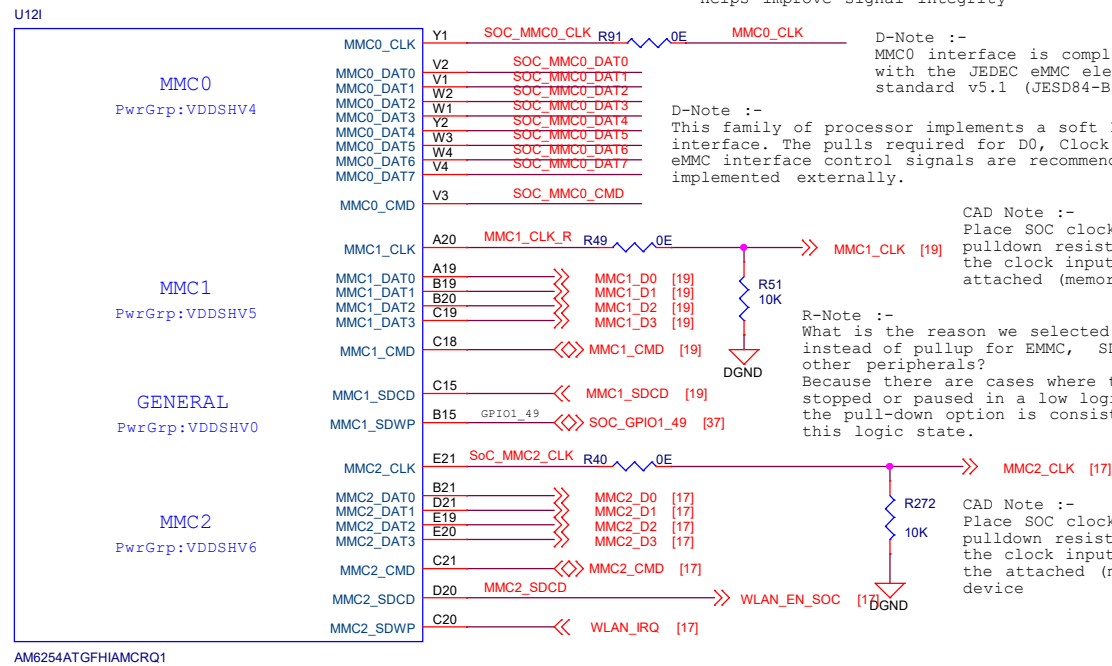
D-Note :-
MMC0 interface is compliant
with the JEDEC eMMC electrical
standard v5.1 (JESD84-B51)

D-Note :-
This family of processor implements a soft PHY for eMMC
interface. The pulls required for D0, Clock and other
eMMC interface control signals are recommended to be
implemented externally.

CAD Note :-
Place SOC clock output
pulldown resistor near to
the clock input pin of the
attached (memory) device

R-Note :-
What is the reason we selected pulldown
instead of pullup for EMMC, SD card or
other peripherals?
Because there are cases where the clock is
stopped or paused in a low logic state and
the pull-down option is consistent with
this logic state.

CAD Note :-
Place SOC clock output
pulldown resistor near to
the clock input pin of the
attached (memory) device

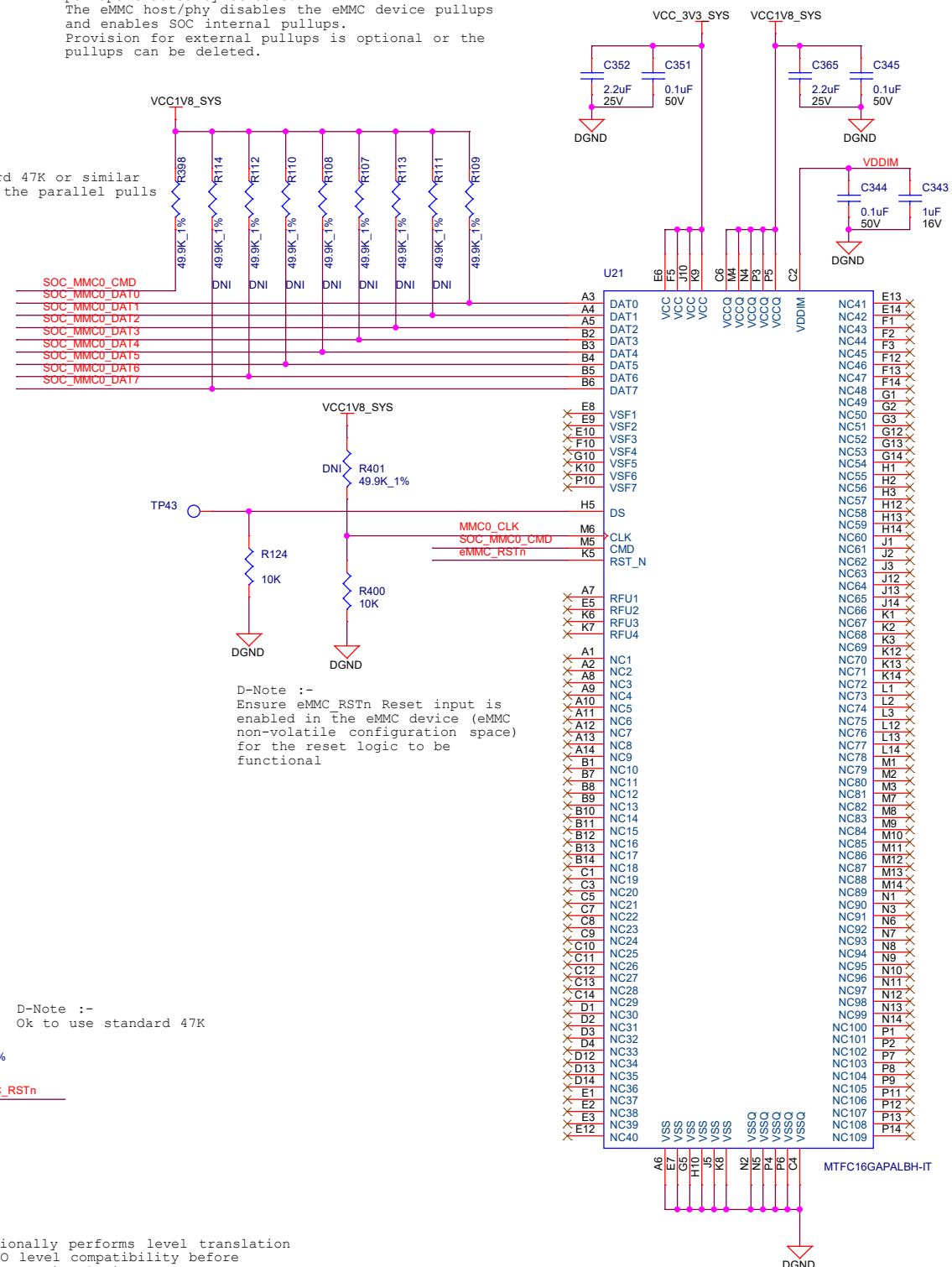


AM6254ATGFHAMCRQ1

eMMC FLASH

D-Note :-
For D7..D1 eMMC device is expected to have the
pullups enabled by default.
The eMMC host/phy disables the eMMC device pullups
and enables SOC internal pullups.
Provision for external pullups is optional or the
pullups can be deleted.

D-Note :-
Add additional decaps as required
Refer SK-AM62P-LP schematics



eMMC FLASH RESET

D-Note :-
The GPIO reset option makes it possible for
software to reset the attached device (eMMC or
OSPI or SD card or OLDI or EPHY) without
resetting the entire processor if there is a
case where the peripheral becomes unresponsive.

D-Note :-
Add a series resistor to the GPIO
input for isolation or testing
Refer SK-AM62P-LP schematics

D-Note :-
Ok to use standard 47K

D-Note :-
You could eliminate the GPIO option and only use
the reset output (Warm or Cold), where software
forces a warm reset if the peripheral becomes
unresponsive. However, this will reset the entire
device rather than trying to recover the specific
peripheral without resetting the entire device.

D-Note :-
In case ANDing logic is not used and the
processor Main Domain warm reset status output
(RESETSTATz) is used to reset the attached
device, ensure the IO voltage level of the
attached device matches the RESETSTATz IO
voltage level. A level translator is
recommended to match the IO voltage level. A
resistor divider could be used alternatively,
provided optimum impedance value of the
resistor divider is selected. If too high the
rise/fall time of the eMMC reset input could be
slow and introduce too much delay. If too low
it will cause the AM62x to source too much
steady-state current during normal operation.

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before
optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and
affect SOC operation

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Title eMMC FLASH INTERFACE

Size C PROC124E2A AM62x-LOW POWER SKEVM

Rev E2A

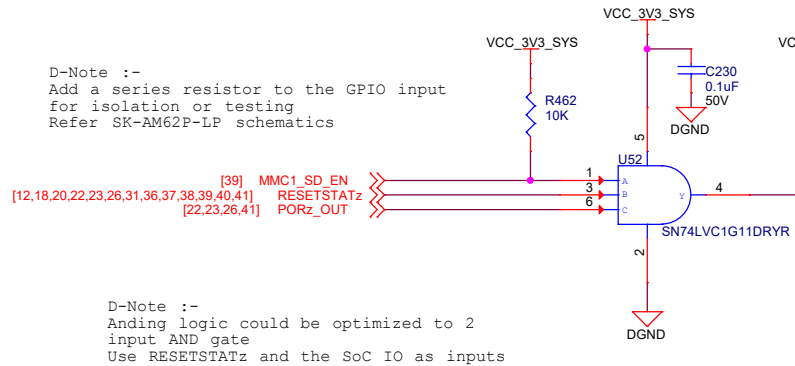
Date: Friday, May 24, 2024

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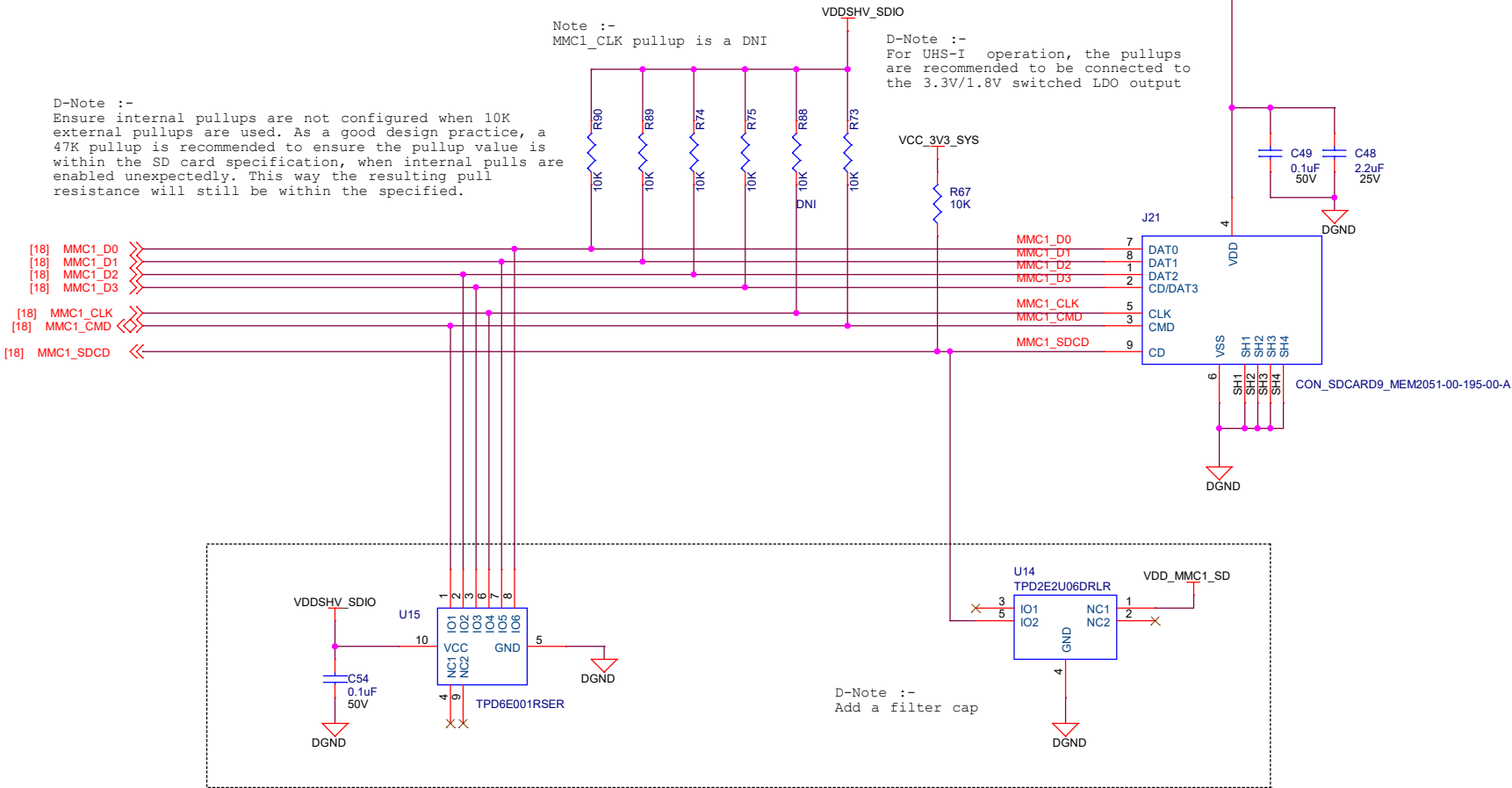
SD CARD INTERFACE

D-Note :-
This power switch, along with the power switch supply reset logic, and the host IO power supply circuit is required to support UHS-I SD Cards which begins communications using 3.3V signal levels and later change to 1.8V signal levels when changing to one of the faster data transfer speeds. Cycling power to the SD Card is the only way to put it back into 3.3V mode since SD Cards do not have a reset pin. The host IO power supply must power off/on and change voltage at the same time as the SD Card. These circuits and the software driver operating the signals sourcing these circuits ensure both devices are off, or on and operating at the same IO voltage at the same time.

SD CARD LOAD SWITCH RESET LOGIC



LOAD SWITCH



PIN			I/O	DESCRIPTION
NAME	DRL	DCK		
IO1	3	1	I/O	The IO1 and IO2 pins are an ESD protected channel. Connect these pins to the data line as close to the connector as possible.
IO2	5	2	I/O	
NC	1, 2	—	-	This pin is not connected and is left floating, grounded, or connected to VCC.
GND	4	3	G	The GND (ground) pin is connected to ground.

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Title SD CARD INTERFACE

Size C PROC124E2A AM62x-LOW POWER SKEVM

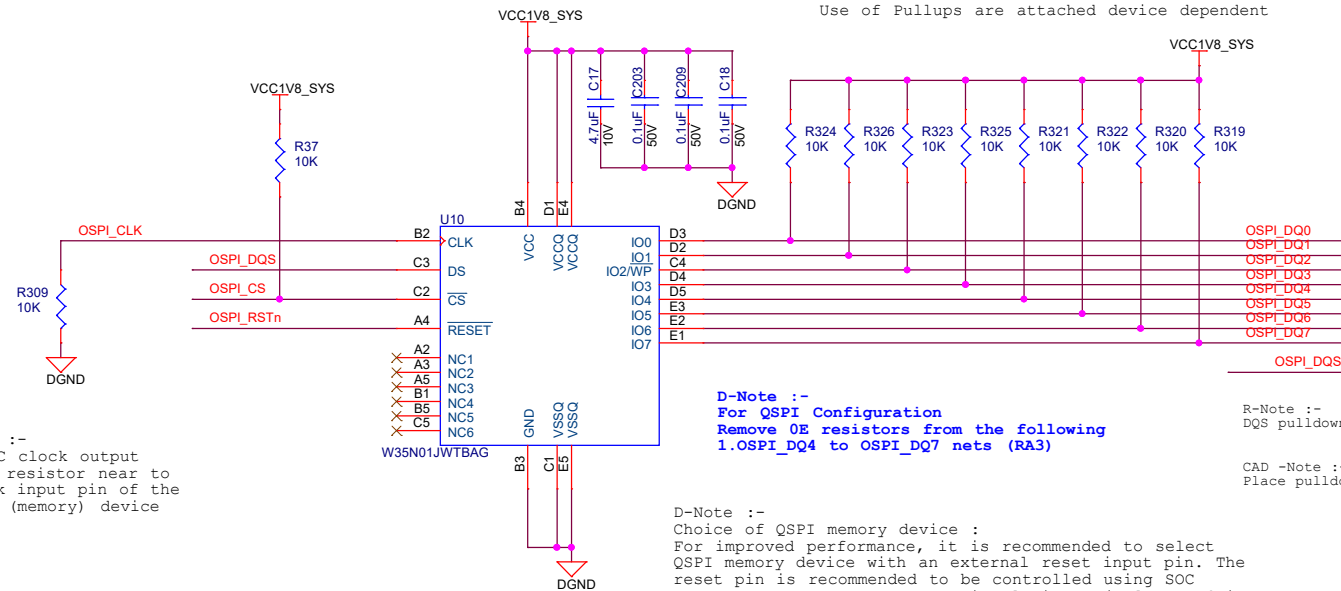
Rev E2A

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OSPI FLASH

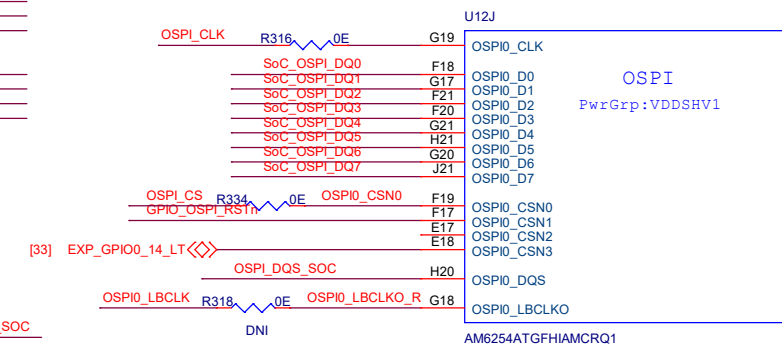
R-Note
SOC IO buffers are off during power-up. A pullup is recommended near to the attached device, to hold the attached device IOs in a known state. Use of Pullups are attached device dependent



D-Note :-
These 0R resistors are used for configuring QSPI and OSPI
This is optional during custom board design

D-Note :-
Connecting OSPI interface to multiple devices
is not recommended or supported

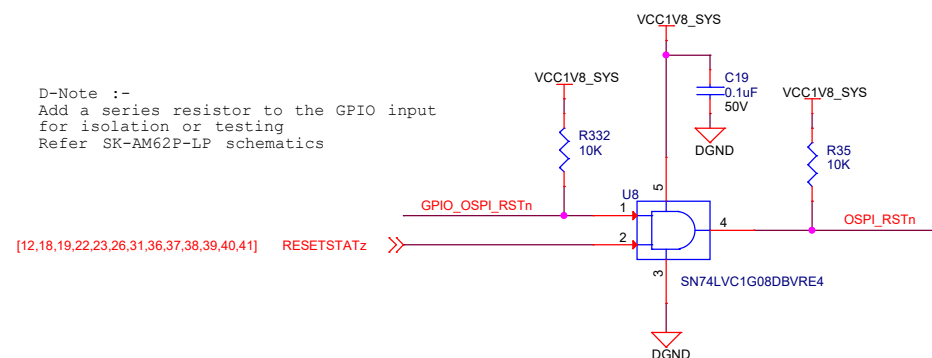
SOC OSPI INTERFACE



D-Note :-
External loopback clock series resistors
are DNI when DQS is connected

CAD Note:- Place R318 close to the SOC Ball with as little trace as possible

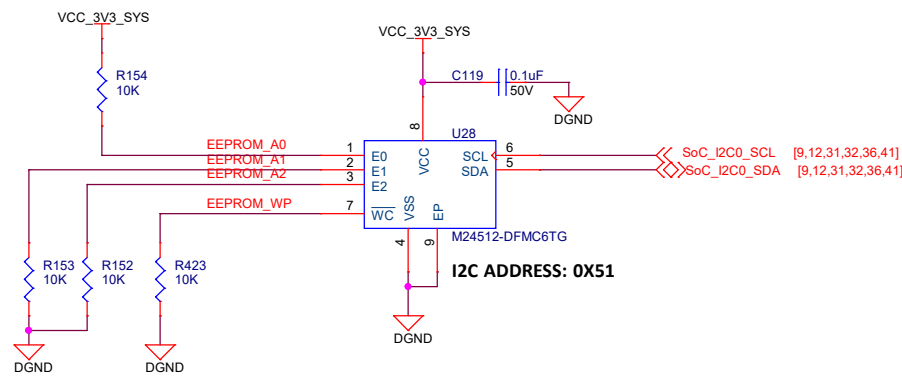
OSPI FLASH RESET



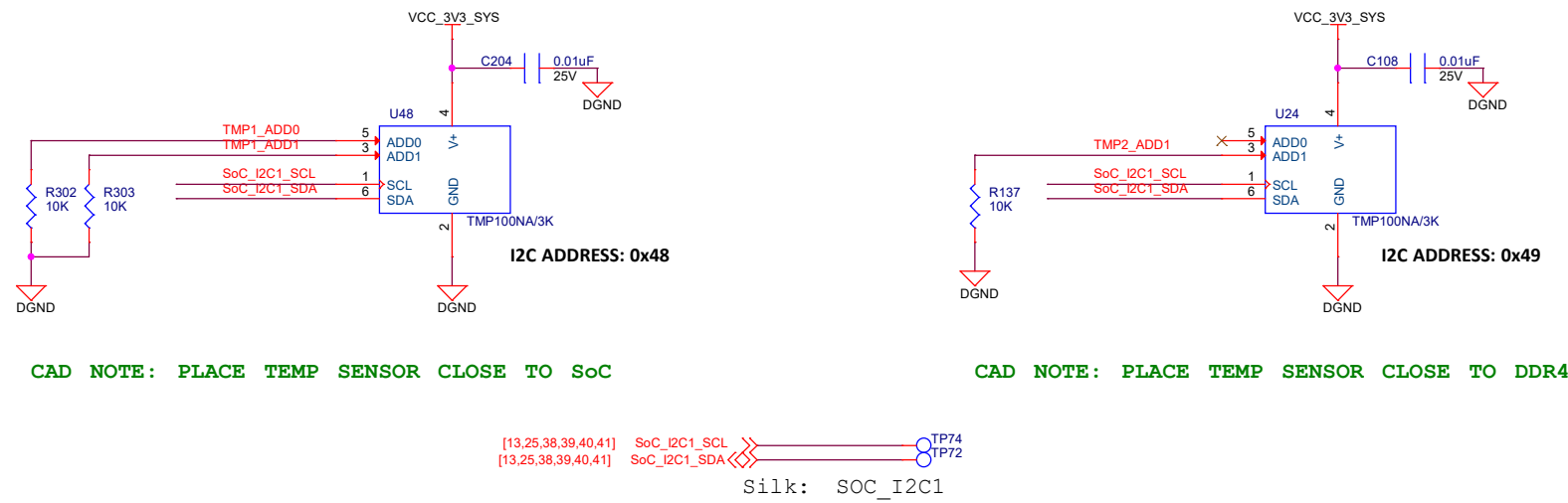
D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before
optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and
affect SOC operation



BOARD ID EEPROM



DIGITAL TEMPERATURE SENSORS



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Title BOARD ID EEPROM & TEMPERATURE SENSORS

Size C PROC124E2A AM62x-LOW POWER SKEVM

Rev E2A

Date: Friday, May 24, 2024

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CPSW3G RGMII 1 - ETHERNET PHY

D-Note :-
The caps and values used are as per the EPHY
data sheet recommendations.

D-Note :-
Refer to DP83867ERGZ-R-EVM when
using LAN Discrete Transformer
Module and RJ45 connector

R-Note :-
Ferrite is DNI

D-Note :-
Verify the power sequence
requirements for Two-Supply
Configuration and Three-Supply
Configuration

RJ45 CONNECTOR WITH INTEGRATED MAGNETICS

CON_RJ45-14_LPJG16314A4NL
Silk: RGMII-1

Note :-
Add a series resistor to the GPIO
input for isolation or testing
Refer SK-AM62P-LP schematics

Note :-
Pullup is enabled for GPIO input
RESETSTATz series resistor is DNI

D-Note
ANDing logic could be optimized to 2 input AND gate
Use RESETSTATz (or PORz_OUT) and the SoC IO as inputs

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before
optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and
affect SOC operation

PHY ADDRESS = 0000
Auto-negotiation Disabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

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Title CPSW RGMII_1 ETHERNET PHY

Size C
PROC124E2A AM62x-LOW POWER SKEVM

Rev E2A

Date: Friday, May 24, 2024

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Designed for TI by Mistral Solutions Pvt Ltd

D-Note :-
Refer to DP83867ERGZ-R-EVM when
using LAN Discrete Transformer
Module and RJ45 connector

R-Note :-
Ferrite is DNI

D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-
Provide provision for Series resistor based on EPHY for RX signals near to EPHY

D-Note :-
XI clock Input amplitude allowed is 1.8V
irrespective of the IO supply
Use a CAP DIVIDER when the clock amplified
is 3.3V

D-Note :-
Refer EPHY EVM for JTAG connections

[22] CPSW_RGMII_INTn CPSW_RGMII_INTn
 [22,31] SoC_RGMII_MDC R644 0E CPSW_RGMII2_MDC
 [22,31] SoC_RGMII_MDIO R646 0E CPSW_RGMII2_MDIO

Note :-
Add a isolation resistor to the GPIO input
for isolation or testing
Refer SK-AM62P-LP schematics

Note :-
Pullup is enabled for GPIO input
RESETSTATz series resistor is DNI

D-Note
 Anding logic could be optimized to 2 input AND gate
 Use RESETSTATz (or PORz OUT) and the SoC IO as inputs

D-Note :-
ANDING logic additionally performs level translation
Verify the Reset IO level compatibility before
optimizing the reset ANDING logic.
IO level mismatch could cause supply leakage and
affect SOC operation

```
PHY ADDRESS = 0001
Auto-negotiation Disabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns
```

Silk: RGMII-2



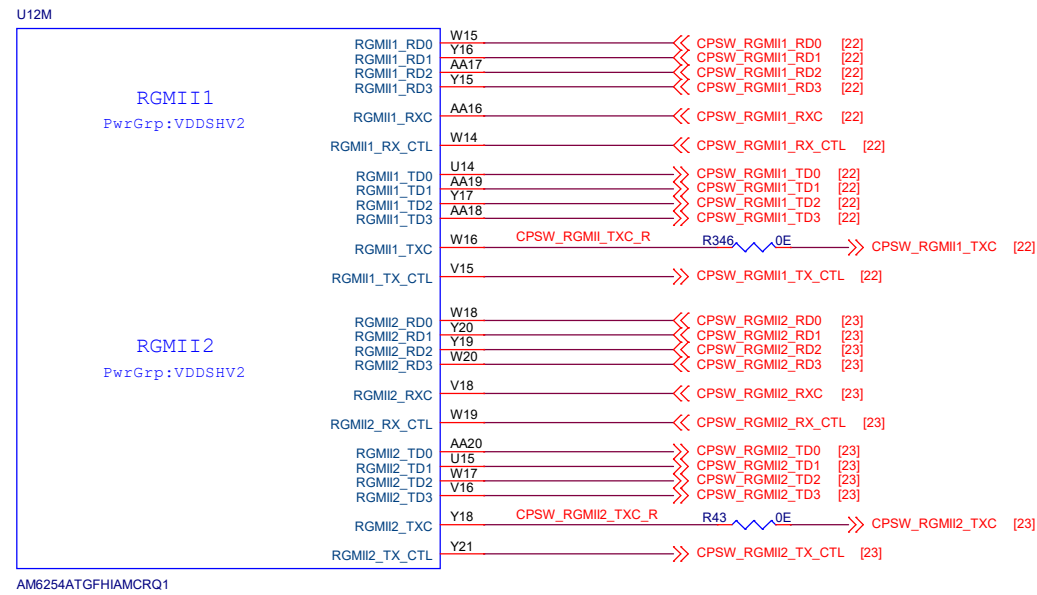
Title	CPSW RGMII_1 ETHERNET PHY
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Size	PROC124E2A AM62x-LOW POWER SKEVM
C	

Rev
E2A

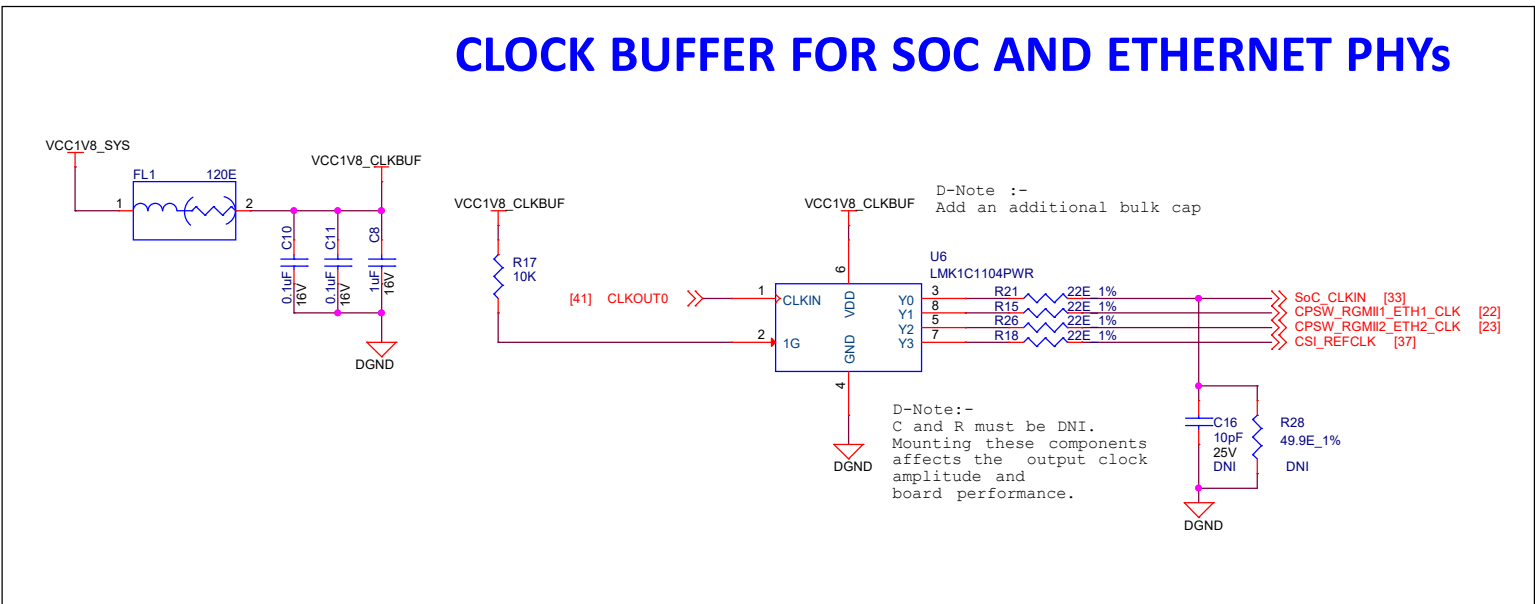
Date:	Friday, May 24, 2024	Sheet	23	of	44
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SOC MAC INTERFACE



D-Note :-
Add series resistors 22 R on the Ethernet
interface TX (TDx) signals near to the SoC

CLOCK BUFFER FOR SOC AND ETHERNET PHYs



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Title ETHERNET PHY CLOCK BUFFER & LED DRIVER

Size C PROC124E2A AM62x-LOW POWER SKEVM

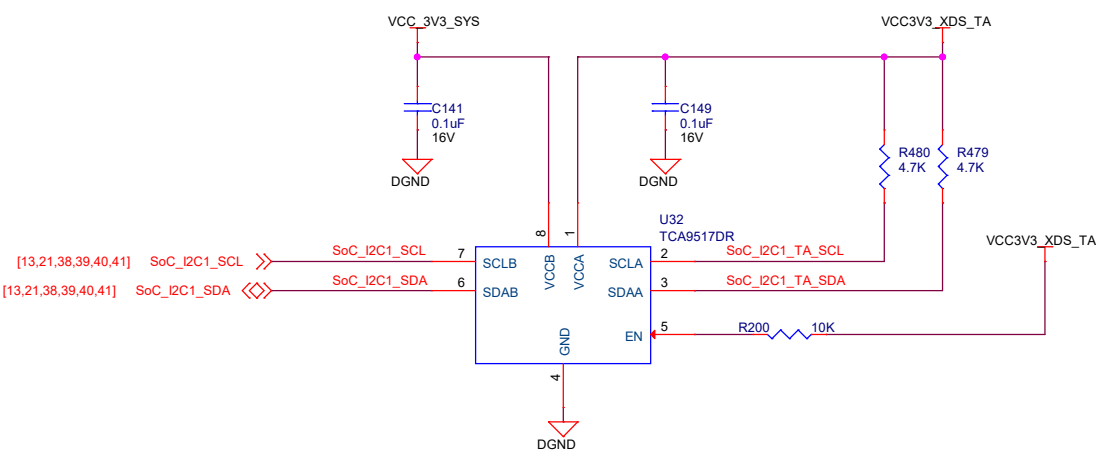
Rev E2A

Date: Friday, May 24, 2024

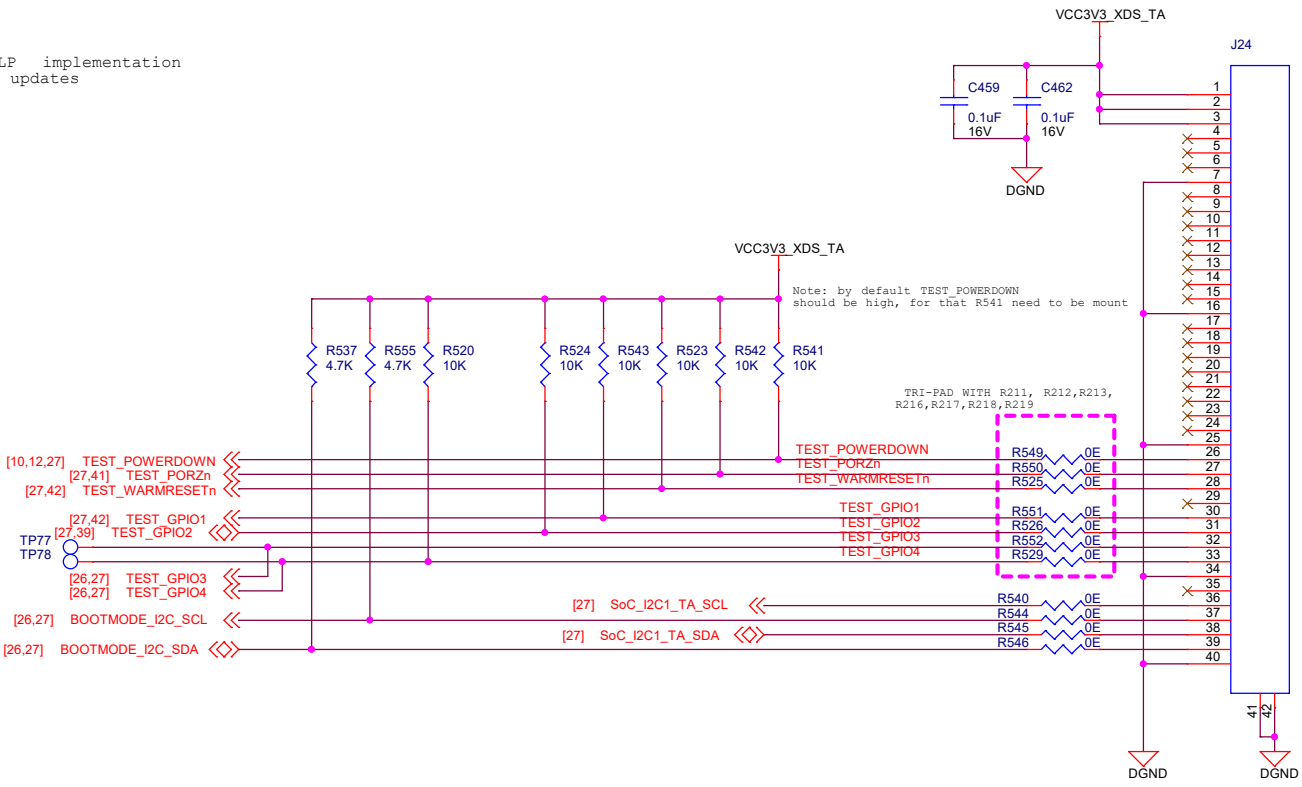
Sheet 24 of 44

40-PIN TEST AUTOMATION HEADER

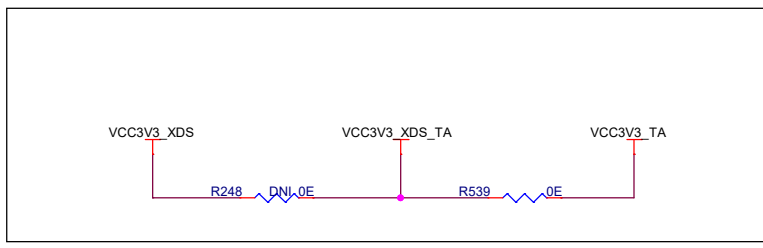
I2C BUS BUFFER



D-Note :-
Refer SK-AM62P-LP implementation
for the latest updates

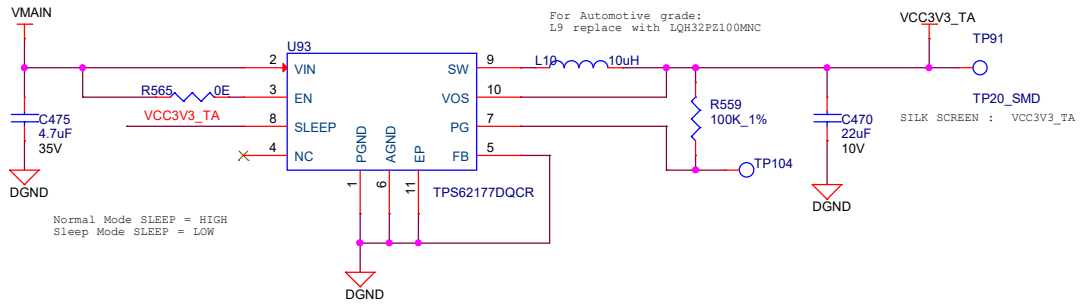


CON_FLEX_40X1_FH12A-40S-0.5SH
Silk: AUTOMATION HDR



TEST AUTOMATION BOARD POWER

VinMin = 4.75V
VinMax = 24V
Vout = 3.3V @ 0.5A



TEST AUTOMATION GPIO MAPPING

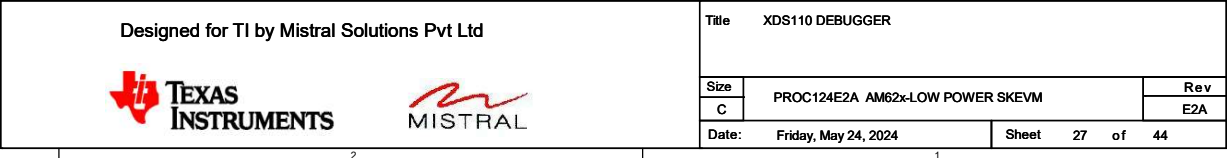
SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SOC_GPIO1_23 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

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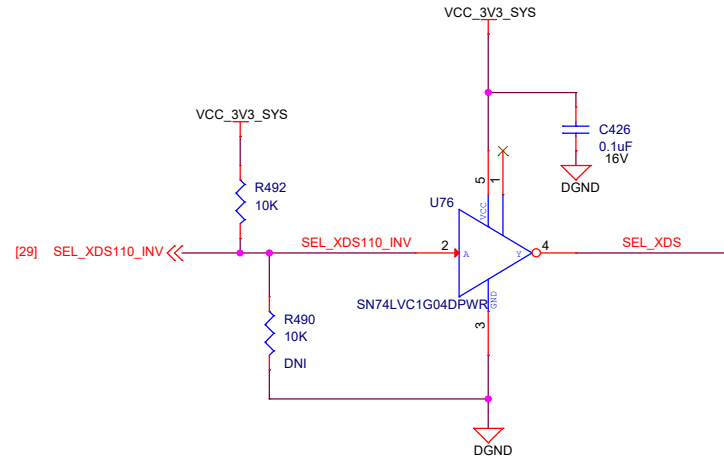
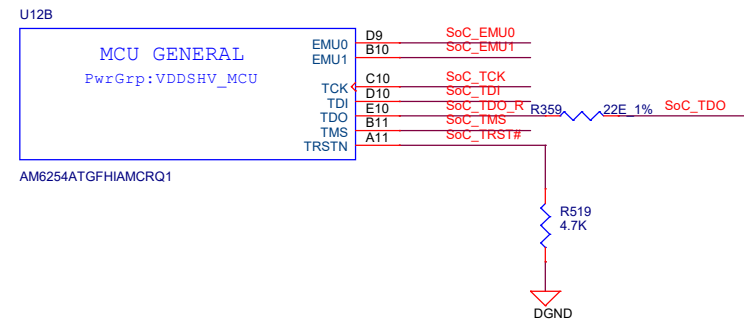


Title TEST AUTOMATION	
Size C	Rev E2A
PROC124E2A AM62x-LOW POWER SKEVM	
Date: Friday, May 24, 2024	Sheet 25 of 44

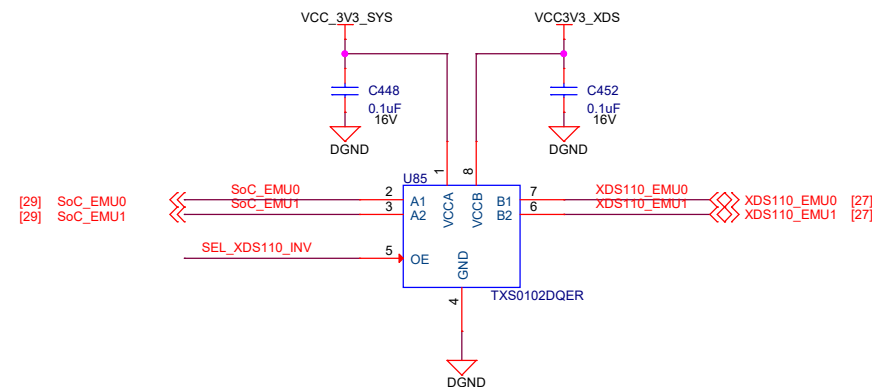
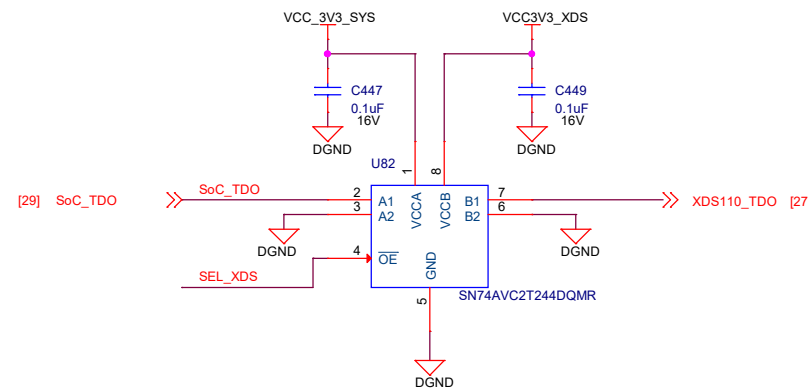
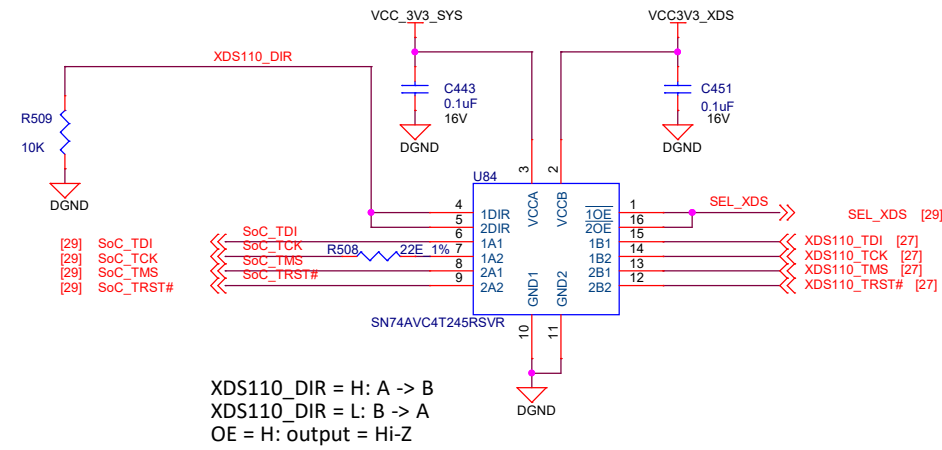
D-Note :-
Please follow SK-AM62P-LP EVM implementations for latest updates on XDS110



JTAG SOC SECTION



BUFFER XDS110



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Title JTAG BUFFER

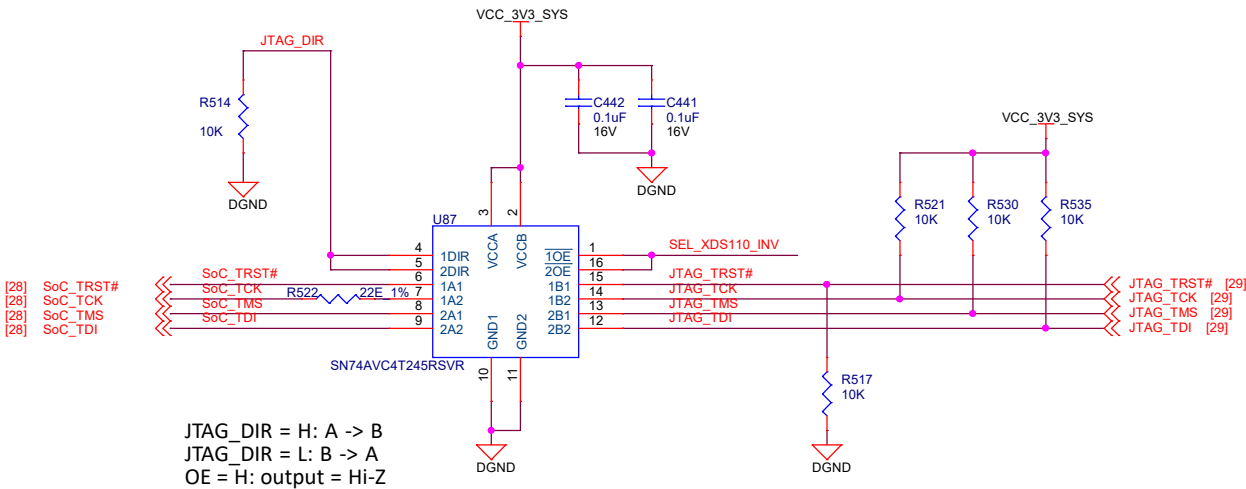
Size C
PROC124E2A AM62x-LOW POWER SKEVM

Rev E2A

Date: Friday, May 24, 2024

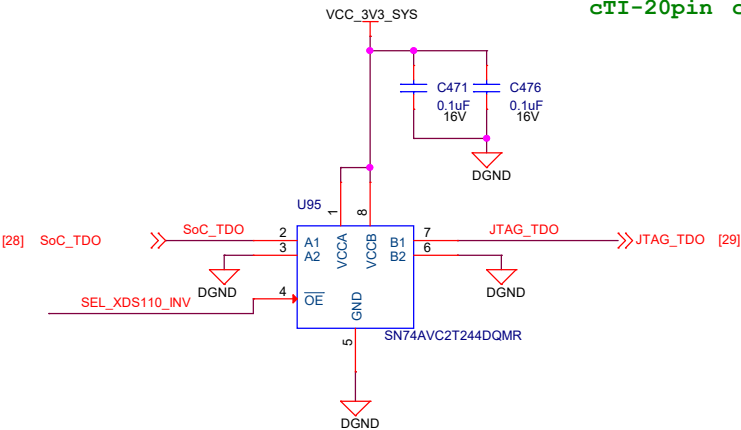
Sheet 28 of 44

cTI20 JTAG BUFFERS

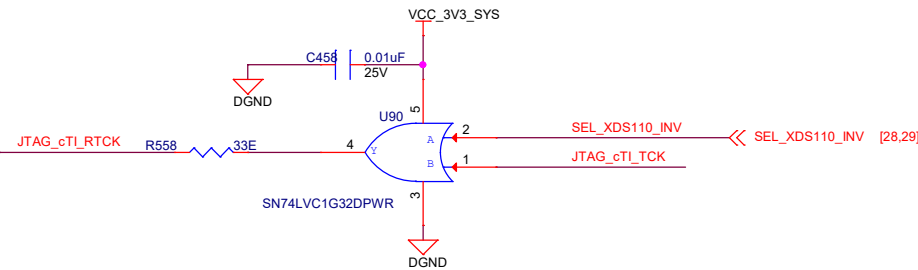
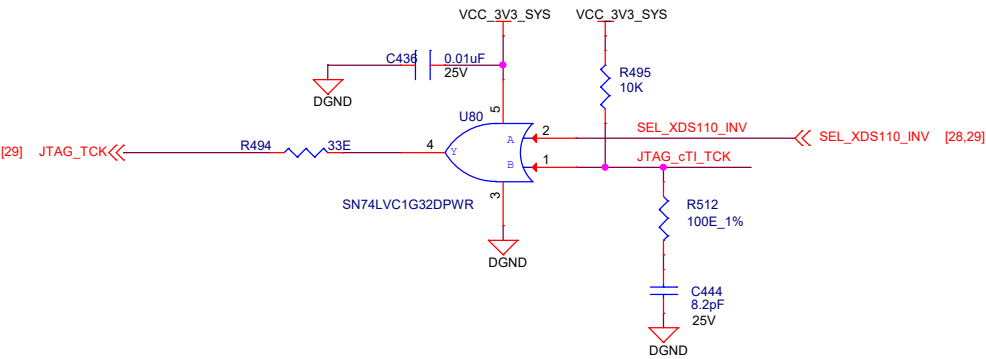


JTAG_DIR = H: A -> B
JTAG_DIR = L: B -> A
OE = H: output = Hi-Z

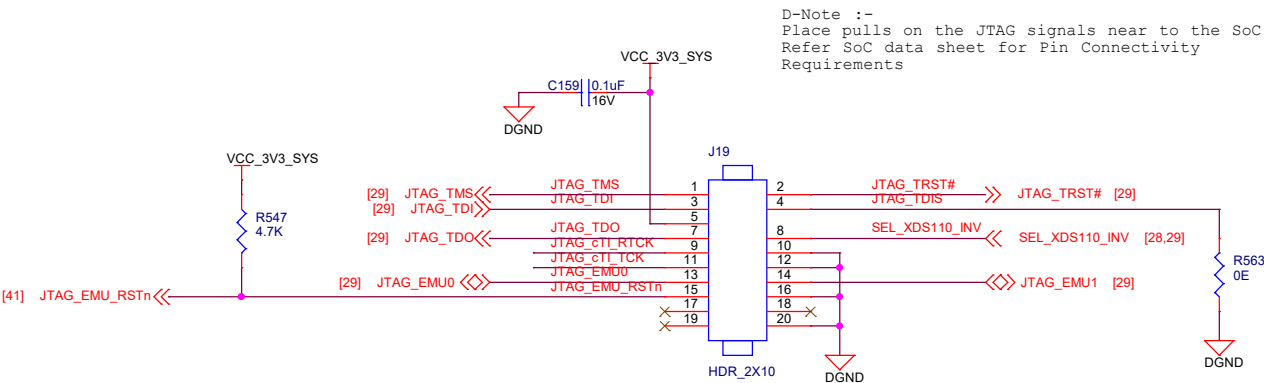
CAD NOTE: Buffers U99 and U101 need to be placed closer to the cTI-20pin connector J11 to reduce Stub length of the JTAG signals.



JTAG CLOCK BUFFER



JTAG 20 PIN cTI CONNECTOR

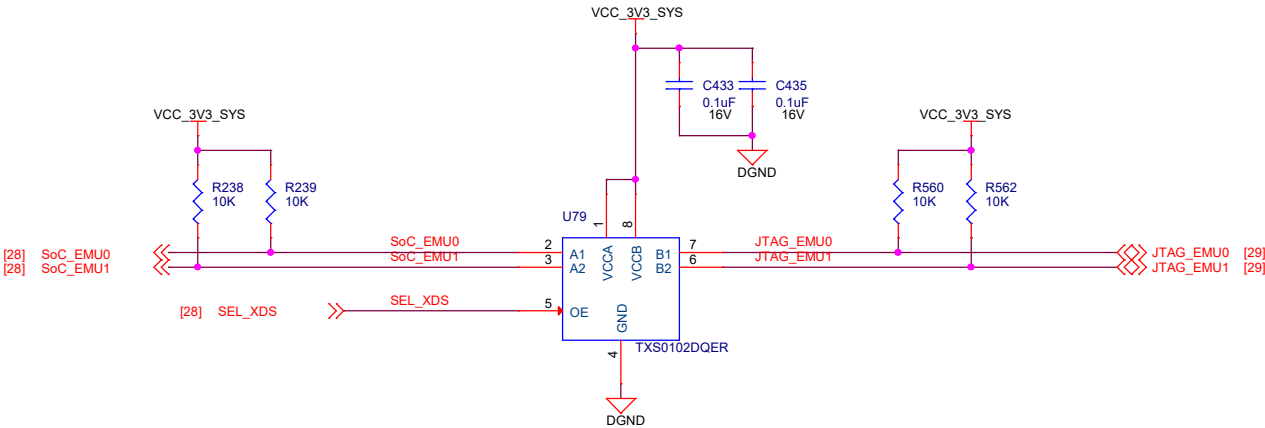


D-Note :-
Place pulls on the JTAG signals near to the SoC
Refer SoC data sheet for Pin Connectivity Requirements

Silk: cTI

D-Note :-
Add an external ESD protection to provide system level ESD protection when external connector is used for debug. Follow the connectivity table for connecting the required pulls for the SOC JTAG interface. Add Test points, and external ESD protection when JTAG connector is not used.

D-Note :-
TRSTn is the reset to the JTAG logic. For normal operation, this is pulled low, and thus the JTAG remains in reset as it is not being used. When a JTAG pod is connected, the pod will eventually drive this signal high to release the JTAG logic from reset and enable a JTAG connection.



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Title JTAG 20 PIN cTI CONNECTOR

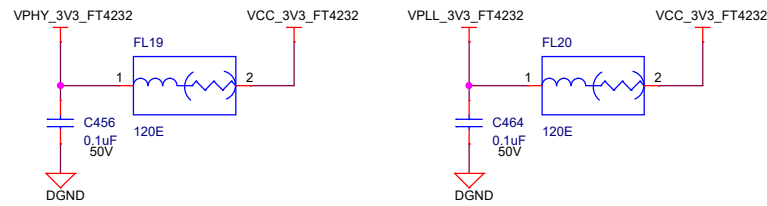
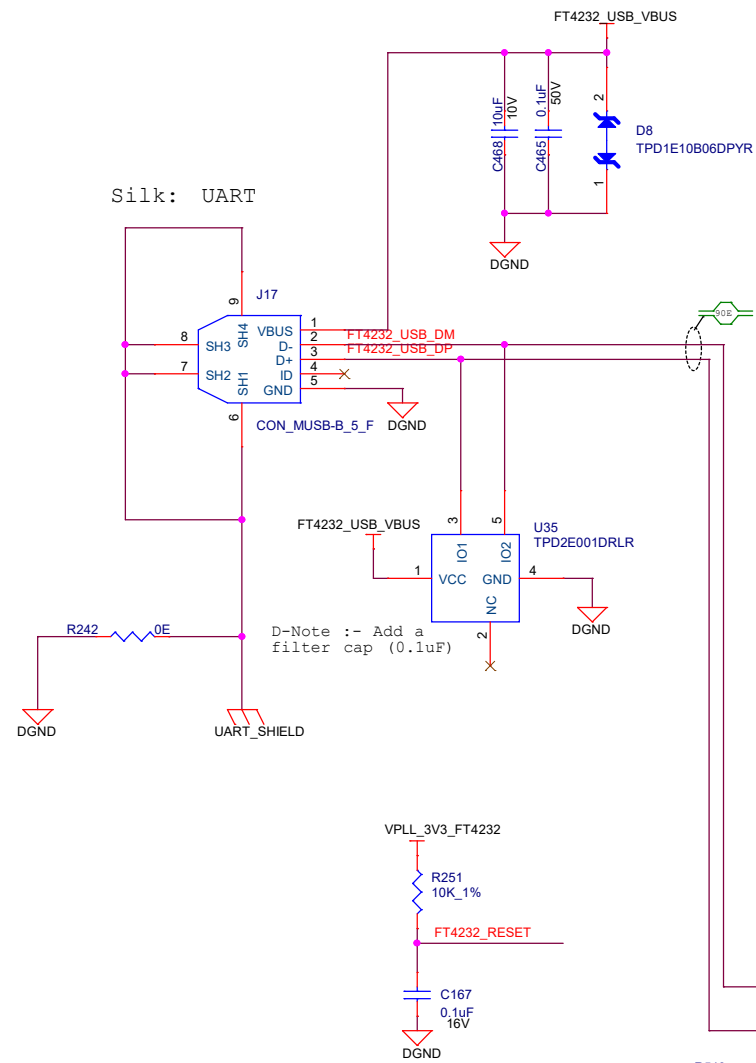
Size C PROC124E2A AM62x-LOW POWER SKEVM

Rev E2A

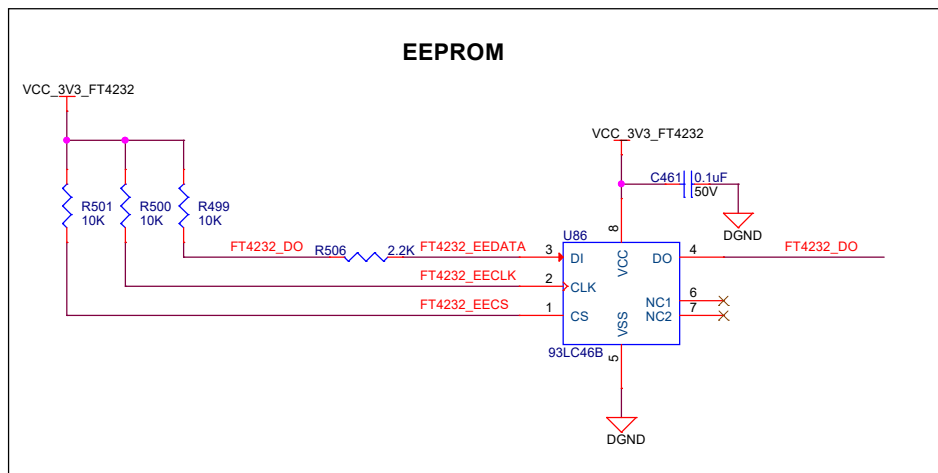
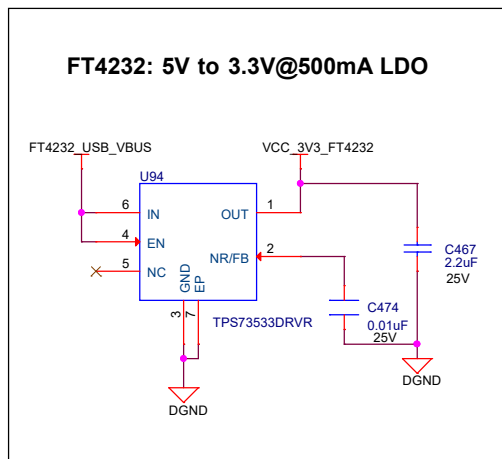
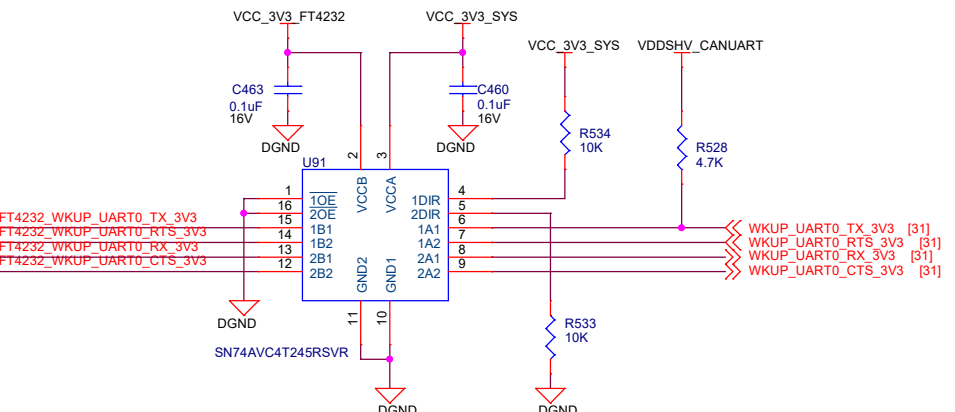
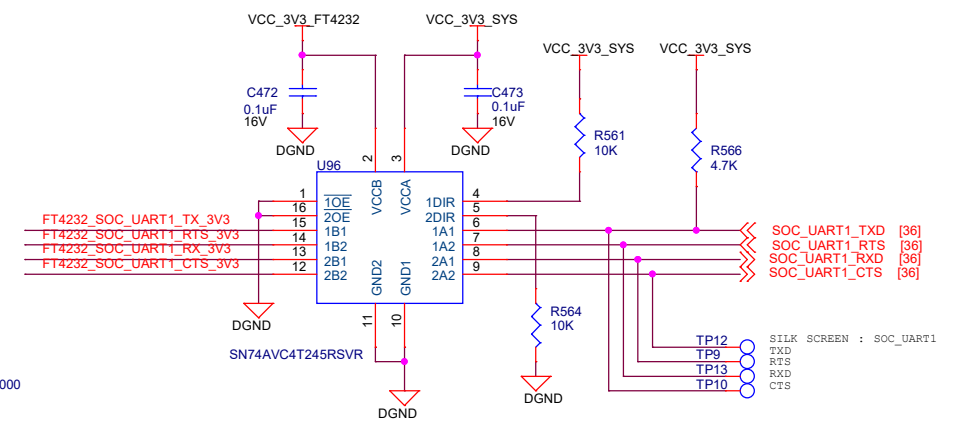
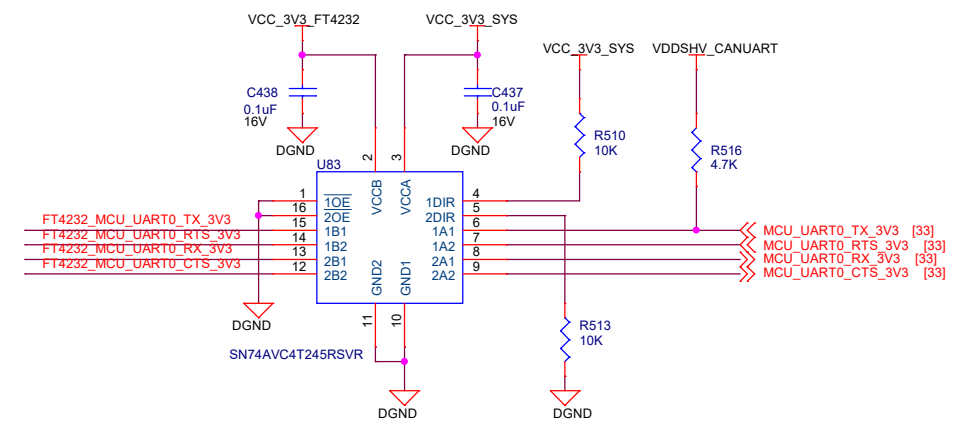
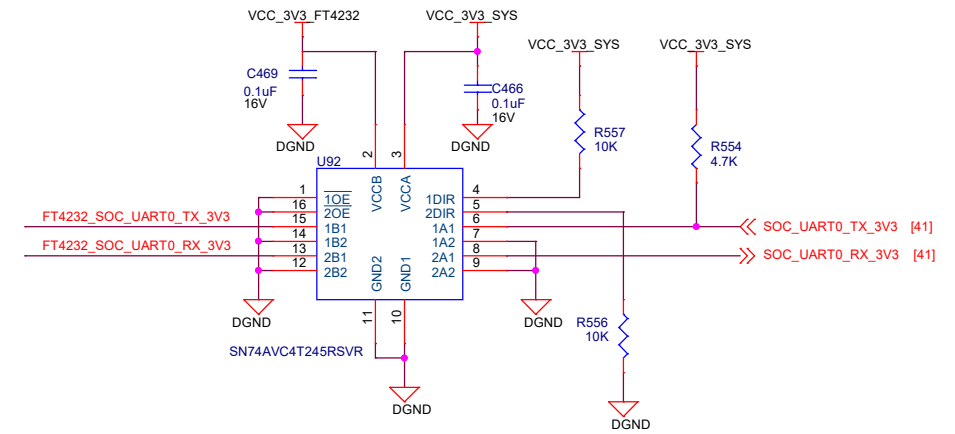
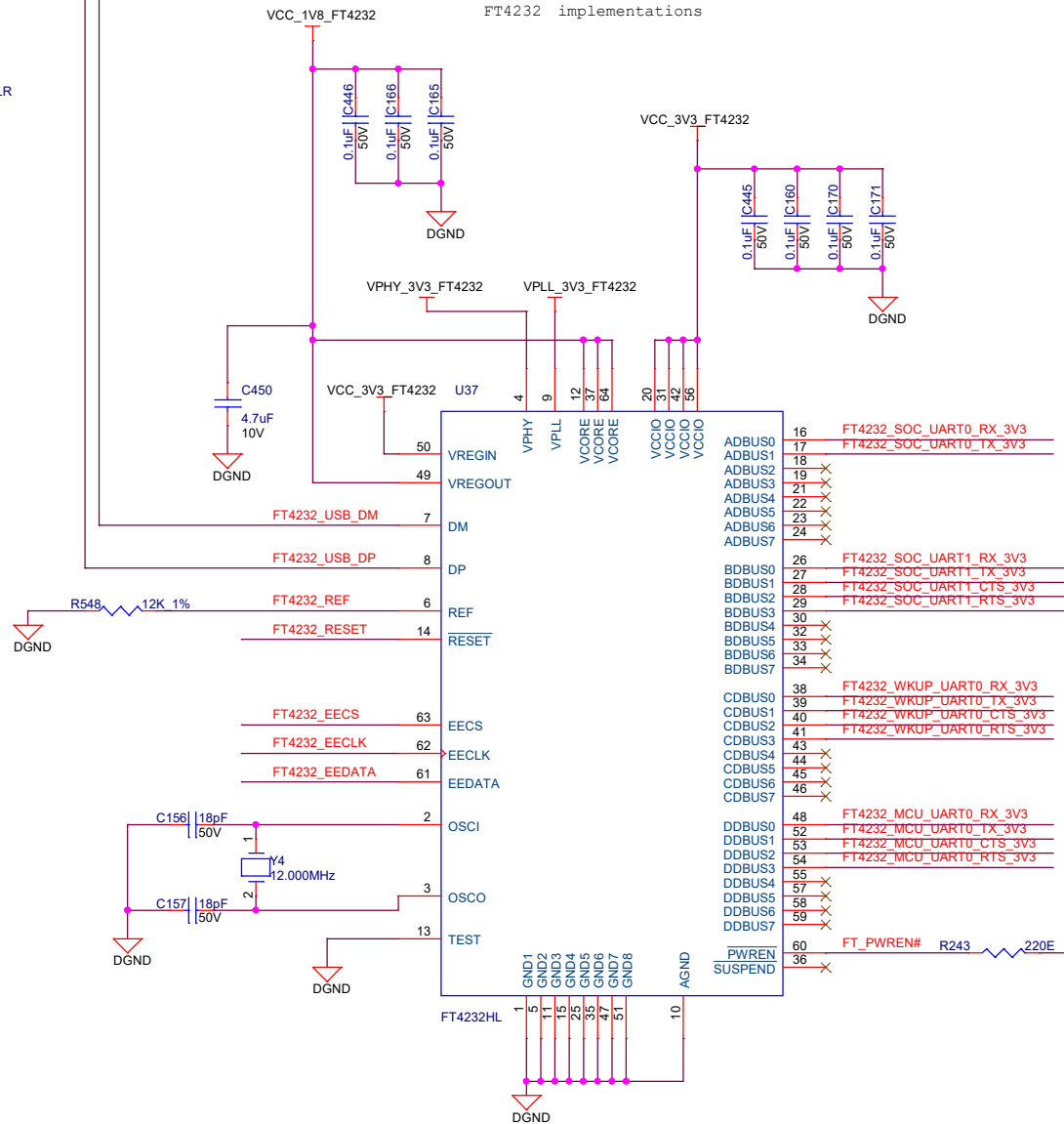
Date: Friday, May 24, 2024

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FT4232 UART



D-Note :-
Follow SK-AM62P-LP for latest
FT4232 implementations



R-Note :-
Verify the implementation with
the device manufacturer

Designed for TI by Mistral Solutions Pvt Ltd



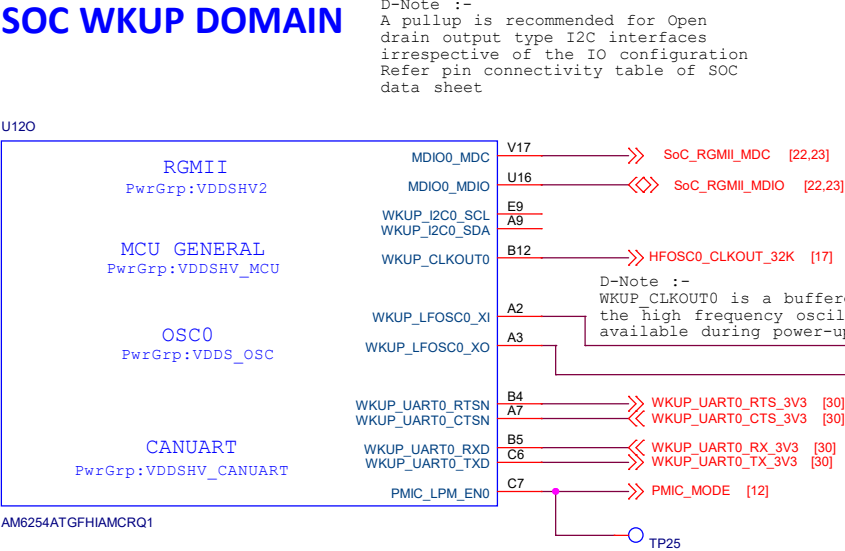
Title	FT4232 UART TO USB BRIDGE
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Size	PROC124E2A AM62x-LOW POWER SKEVM
C	

Date:	Friday, May 24, 2024	Sheet	30	of	44
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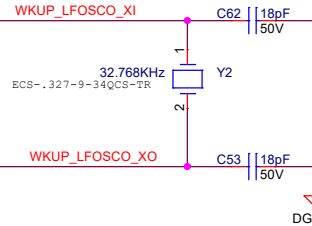
Rev
E2A

SOC WKUP DOMAIN



D-Note :-
A pullup is recommended for Open drain output type I2C interfaces irrespective of the IO configuration Refer pin connectivity table of SOC data sheet

D-Note :-
Open-drain output type buffer I2C interfaces have slow rate requirement when pulled to 3.3 V. An RC is recommended for slow rate control Refer SK-AM62P-LP schematics



D-Note :-
WKUP_CLKOUT0 is a buffered output of the high frequency oscillator (HFOSC0) available during power-up as default

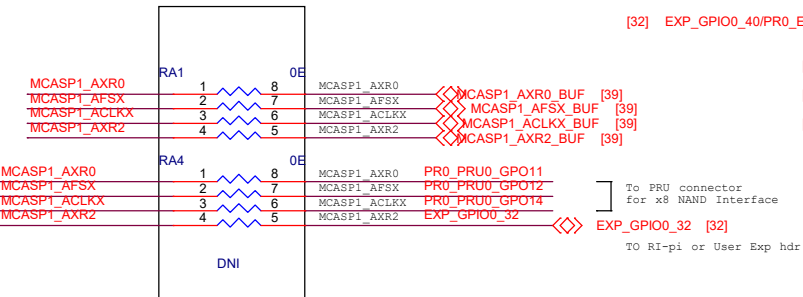
D-Note :-
Refer SoC data sheet for the recommended circuit configuration during preproduction PCB and the production PCB

D-Note :-
Shorting of bootmode inputs (IOs) is not recommended or allowed since the IOs have alternate functions that could be configured after boot Shorting the bootmode pins directly to VCC or ground directly is not recommended Connect each of the bootmode pins through separate resistor Choose the bootmode resistor value based on the use case (10K or similar)

D-Note :-
SOC IO buffers for signals used for GPMC interface are disabled during reset The required pulls for the interfaced signals are provided on the GPMC interface card

D-Note :-
When bootmode Isolation buffers are not used, connect the bootmode configuration resistors directly to the SOC bootmode input pins. Connect the SOC bootmode signal used for alternate function to the attached device through 0R for isolation or testing.

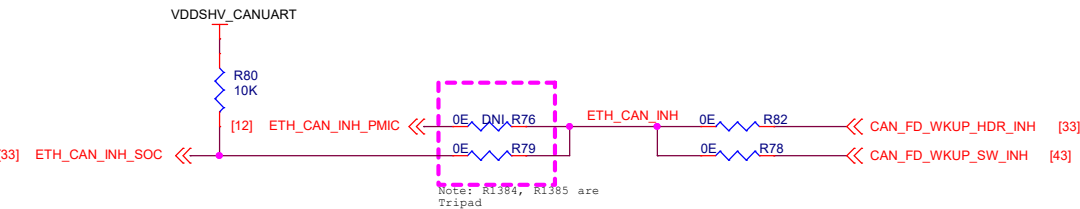
Cad Note: Place such that stubs are minimum. use TRIPAD ACTION



D-Note :-
Add a 22R at the output of MCASP1_ACLKX near to the SOC

[32] EXP_GPIO0_40/PRU_ECAP0_IN_APWM_OUT
[32] EXP_GPIO0_36
[32] EXP_GPIO0_38
[32] EXP_GPIO0_39
[32] EXP_GPIO0_33
[32] EXP_GPIO0_32

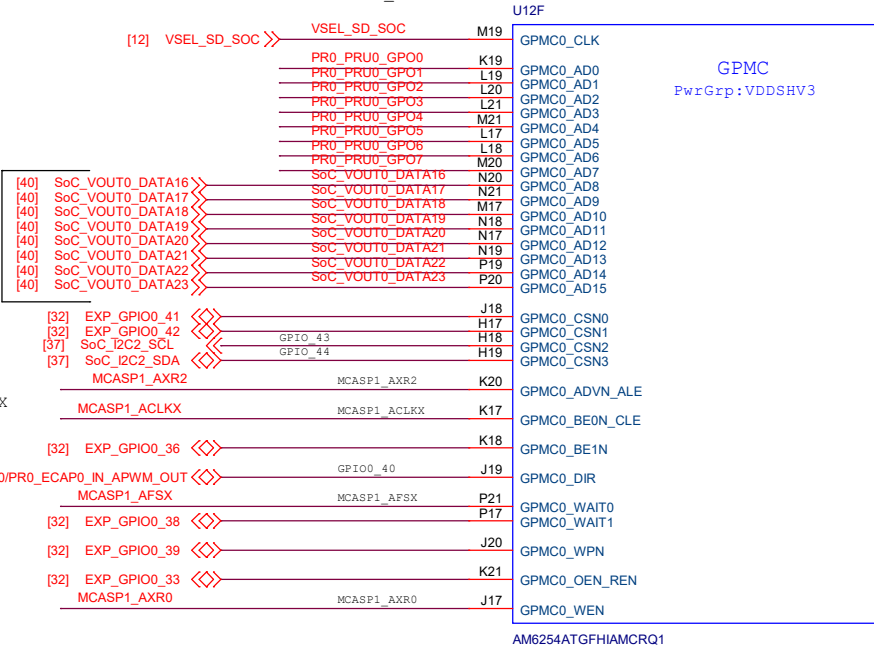
To PRU connector for x8 NAND interface
TO RI-pi or User Exp hdr



D-Note :-
WKUP LFOSC0 has limited use case. Provide provision to ground Xi when not used. Refer SOC data sheet

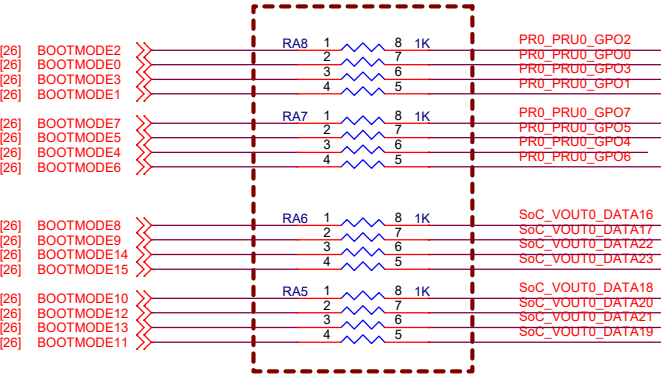
D-Note :-
The only LFOSC0 register bits that should be changed by the customer are BP_C, PD_C, and CTRLMMR_WKUP_LFXOSC_TRIM[18:16], where PD_C is reset (0) to enable the oscillator and the BP_C bit is only set (1) to place the oscillator in bypass mode when using an LVCMOS clock source. The CTRLMMR_WKUP_LFXOSC_TRIM[18:16] bits are set based on the actual capacitance load applied to the crystal, as defined by the Load Capacitance Equation. The load capacitance range of the crystal will be half of the recommended capacitor value range since there are connected in series with the crystals resonate circuit.

SOC GPMC INTERFACE



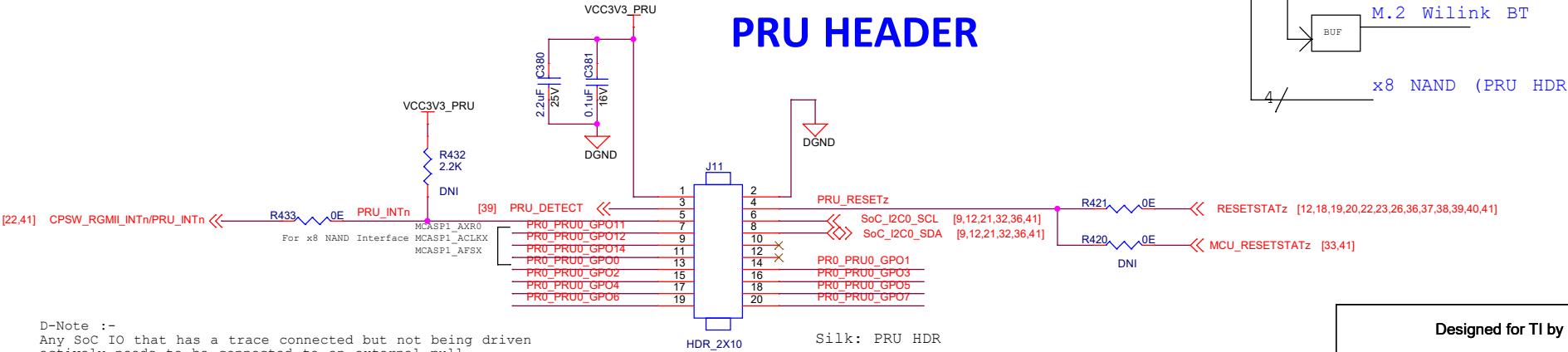
D-Note
Add a series resistor 0R when used as GPMC0_CLK

BOOTMODE PINS



R-Note :- Resistors are used to isolate the BOOTMODE control logic after the value is latched

PRU HEADER

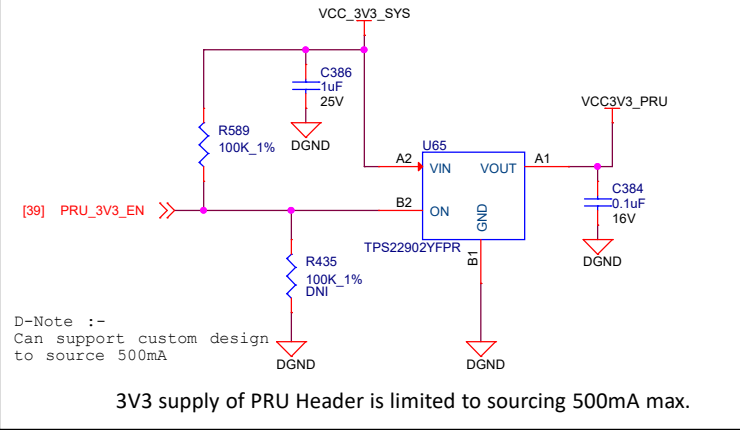


D-Note :-
Any SoC IO that has a trace connected but not being driven actively needs to be connected to an external pull. When adding pull is not feasible, ensure the traces are routed away from noisy signals

D-Note:- Processor IOs connected to PRU Header are not fail-safe. No external input shall be driven when Starter Kit is not powered-up.

Silk: PRU HDR

POWER SWITCH FOR PRU HEADER



D-Note :-
Can support custom design to source 500mA

3V3 supply of PRU Header is limited to sourcing 500mA max.

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Title PRU HEADER

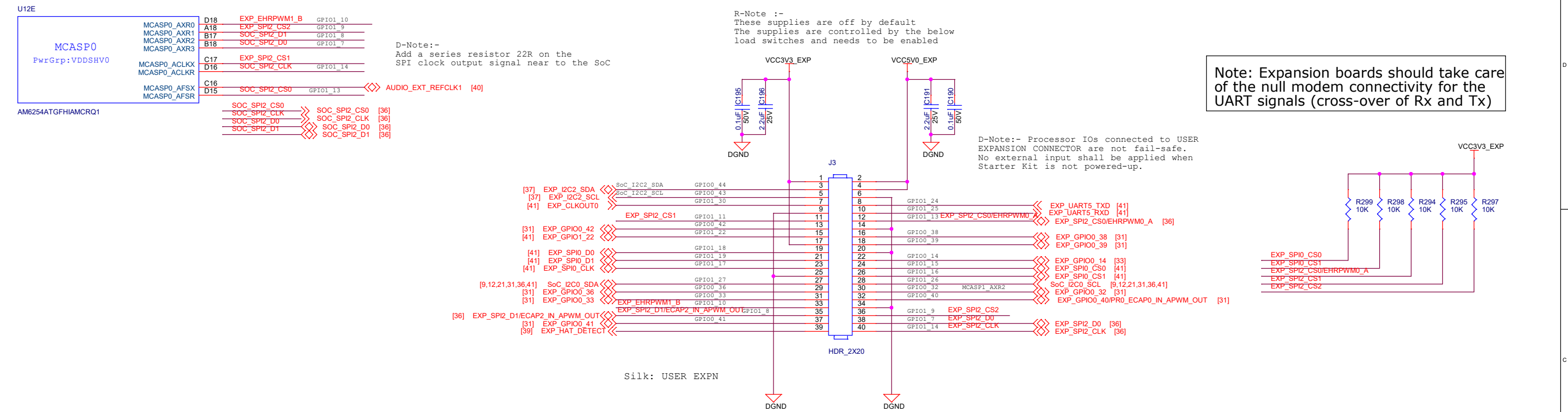
Size PROC124E2A AM62x-LOW POWER SKEVM

Rev E2A

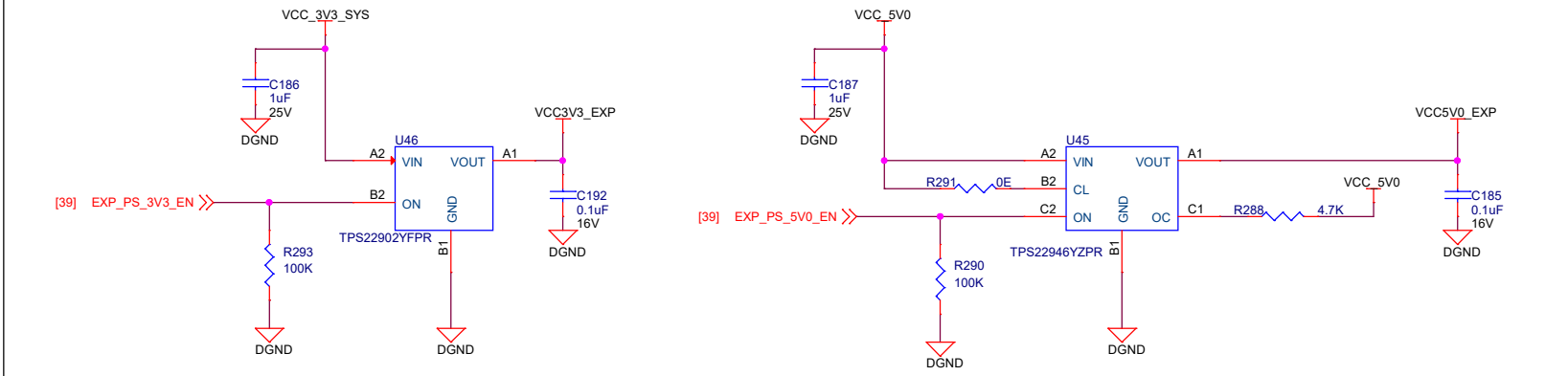
Date: Friday, May 24, 2024

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USER EXPANSION CONNECTOR



LOAD SWITCHES FOR USER EXPANSION CONNECTOR



D-NOTE :-

AM62x Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

D-Note :-
A pullup is recommended for Open drain output type I2C interfaces irrespective of the IO configuration
Refer pin connectivity table of SOC data sheet

D-Note :-
Open-drain output type buffer I2C interfaces have slew rate requirement when pulled to 3.3 V
An RC is recommended for slew rate control
Refer SK-AM62P-LP schematics

D-Note :-
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO

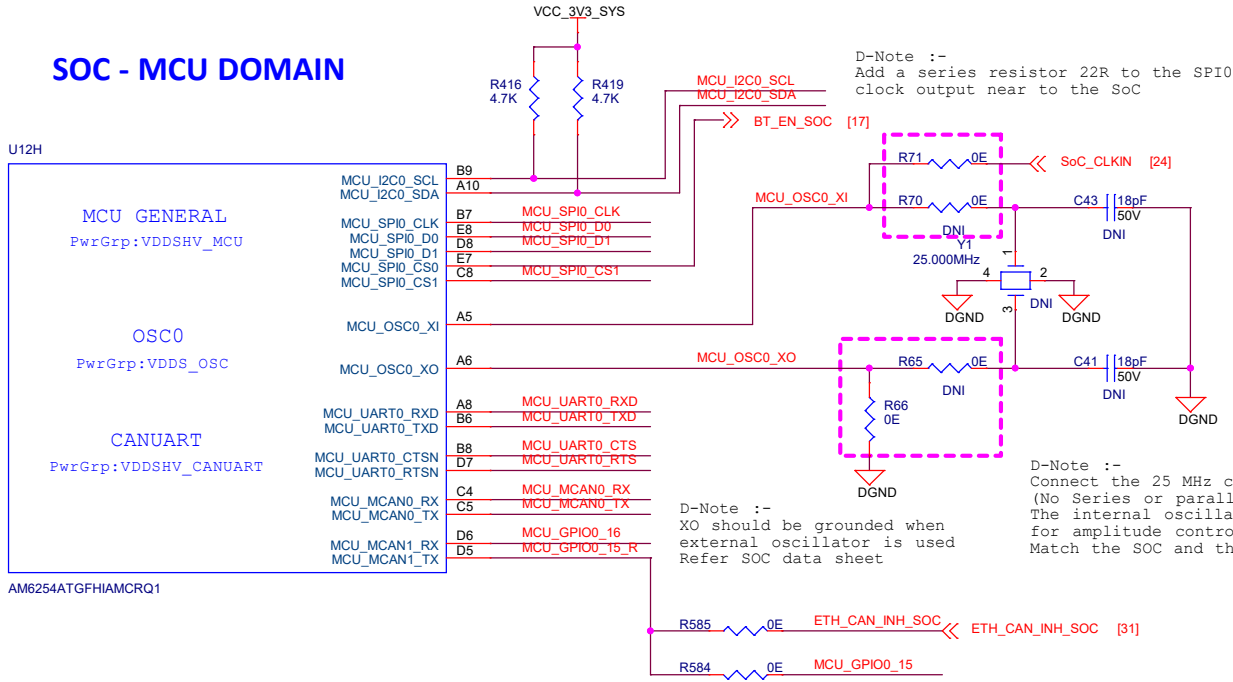
D-Note :-
No HFOSC0 registers are required to be changed. These registers should remain in their default state.
Select the appropriate crystal circuit components that are compliant to the values defined in the MCU_OSC0 Crystal Circuit Requirements table.
Read the Load Capacitance and Shunt Capacitance sections to select the appropriate crystal circuit components.

D-Note :-
Refer Applications, Implementation, and Layout section of the data sheet for clock routing guidelines as below:
Clock Routing Guidelines
Oscillator Routing

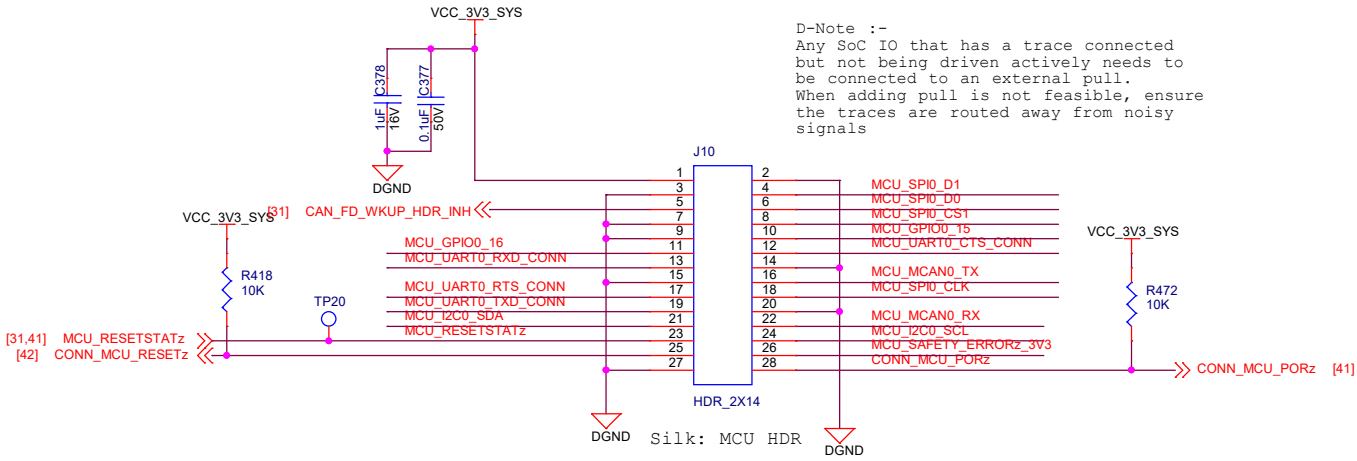
D-Note :-
MCU_OSC0 has been validated only with a 25 MHz clock source, so that is the only frequency supported.
The datasheet shows MCU_OSC0 not starting until after the core voltage because there are some cases where the oscillator may not start until VDD_CORE is valid. In most cases it will start as early as VDDDS_OSC0, but this may not always be the case. This diagram in the datasheet is showing the maximum start-up time, which must include the case where the delay is based on VDD_CORE being valid.

D-Note :-
Connect the 25 MHz crystal directly to the SOC Xi and Xo pins
(No Series or parallel resistors are recommended).
The internal oscillator implements AGC (Automatic Gain Control) for amplitude control
Match the SOC and the EPHY crystal specs

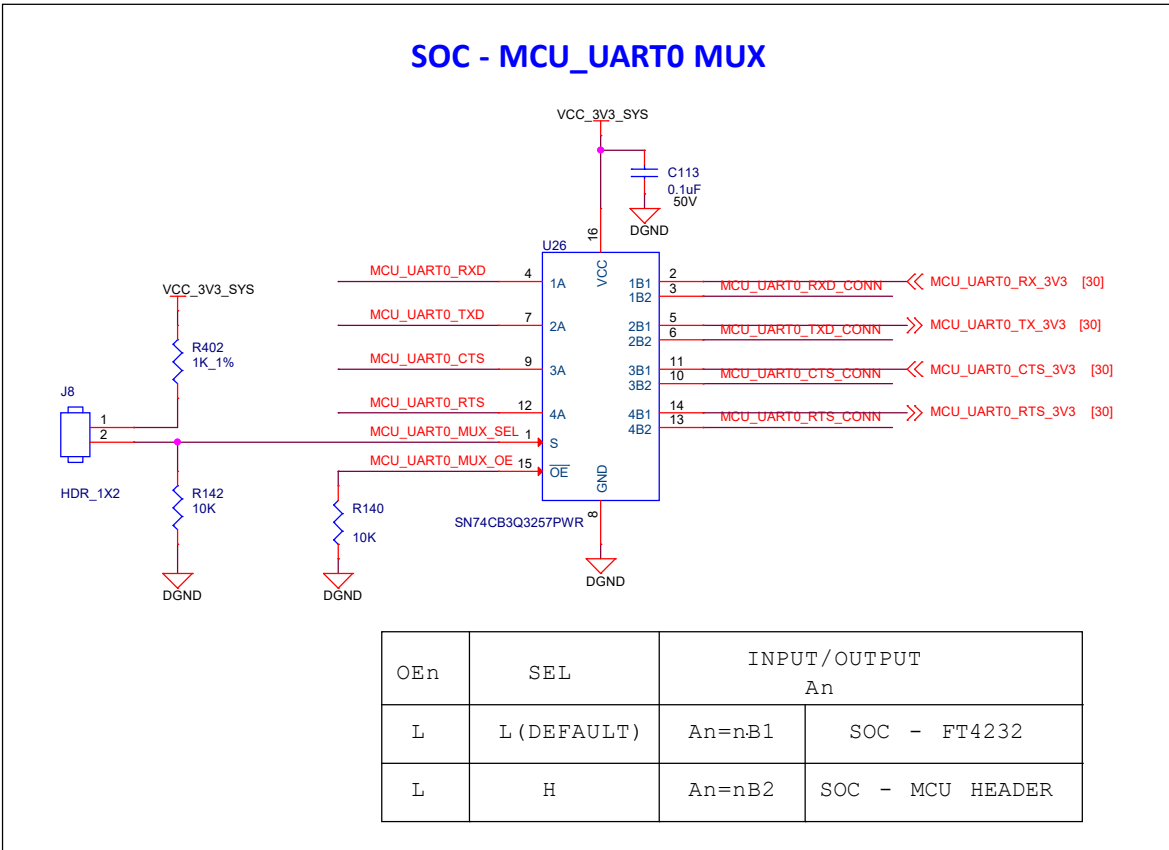
SOC - MCU DOMAIN



SOC-MCU HEADER



SOC - MCU_UART0 MUX



OEn	SEL	INPUT/OUTPUT	
		An	An
L	L (DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER

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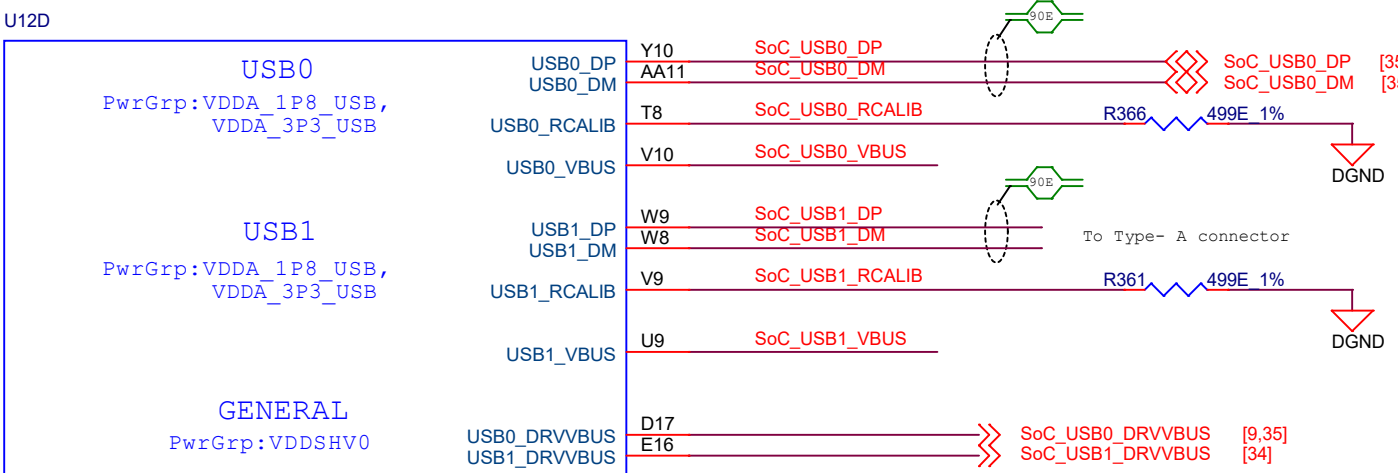
Title MCU HEADER

Size C
C PROC124E2A AM62x-LOW POWER SKEVM
Date: Friday, May 24, 2024

Rev E2A

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USB1 - USB 2.0 TYPE-A



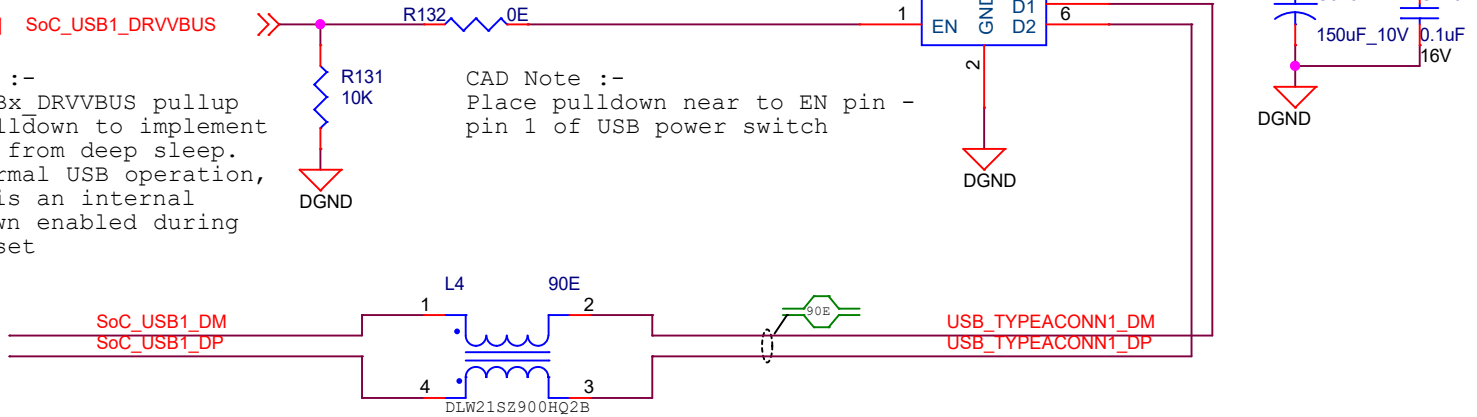
AM6254ATGFHAMCRQ1

To Type- C connector
Port: 2 of PD Controller

D-Note :-
DNI USBx_DRVVBUS pullup
and pulldown to implement
wakeup from deep sleep.
For Normal USB operation,
there is an internal
pulldown enabled during
SOC reset

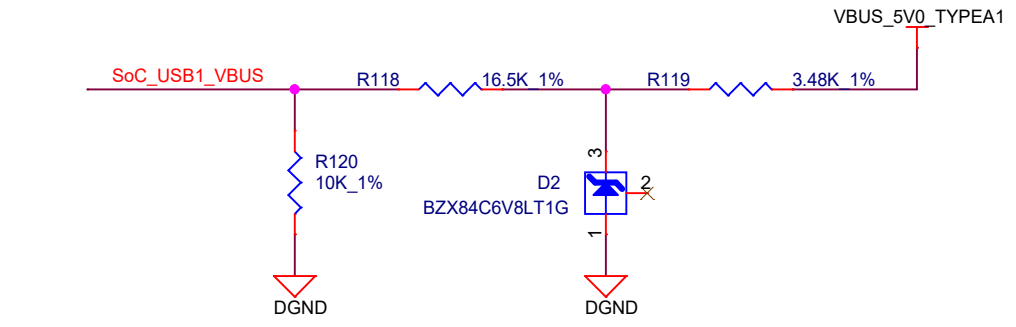
CAD Note :-
Place pulldown near to EN pin -
pin 1 of USB power switch

D-Note :-
Use power switch with OC indication
Example TPS2051
Connect OC output of the power switch to
SoC IO for USB VBUS over load detection
Refer SK-AM62P-LP schematics

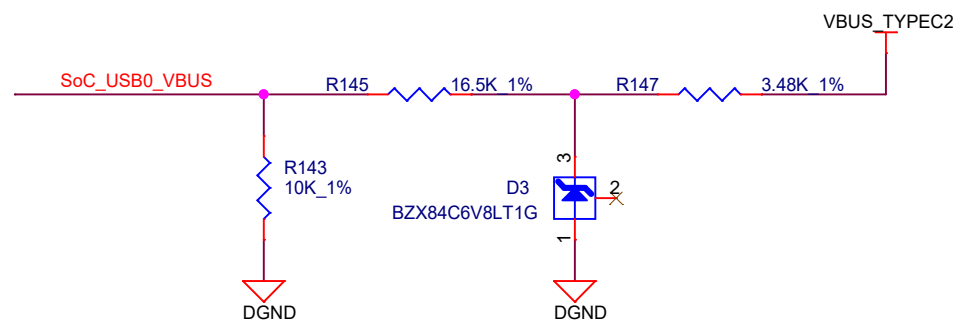


Silk: TYPE-A

D-Note :-
Provide provision to bypass
the CMC using OR resistor
for performance testing



D-Note:- Refer USB VBUS Design Guidelines section of SoC data sheet



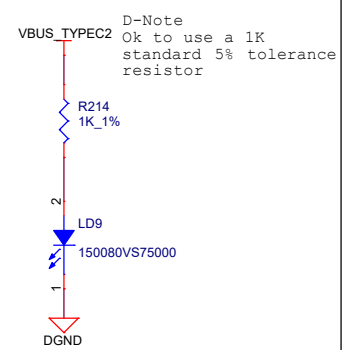
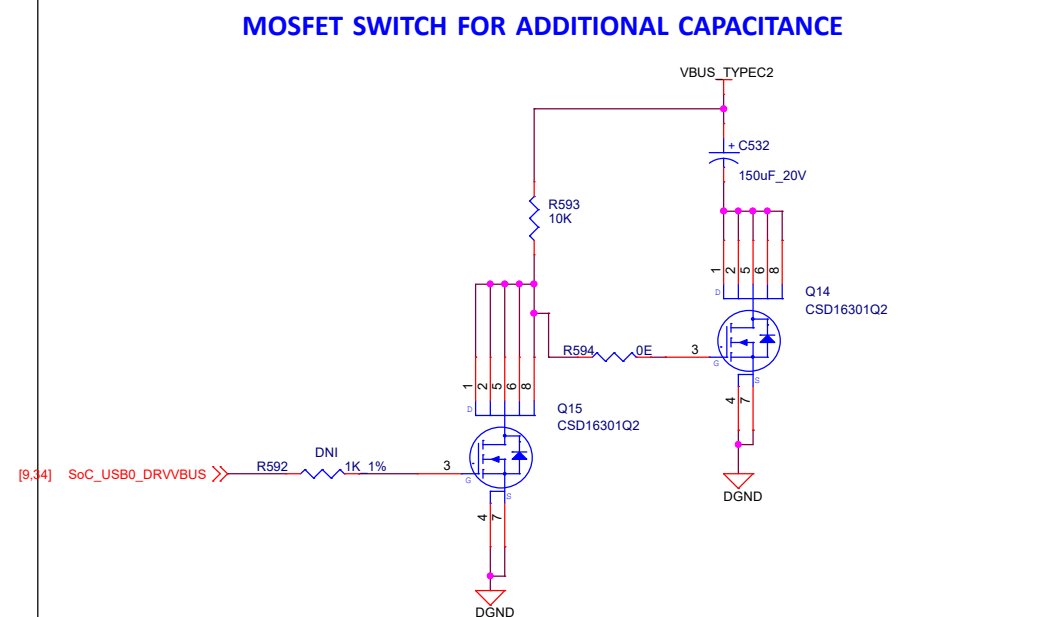
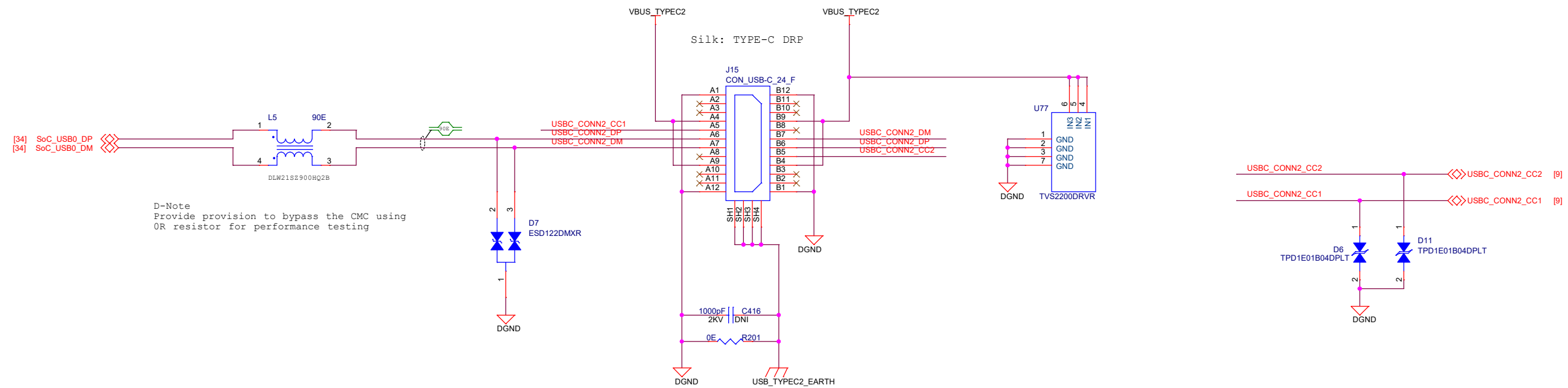
D-Note:- VBUS connection is optional for Host configuration

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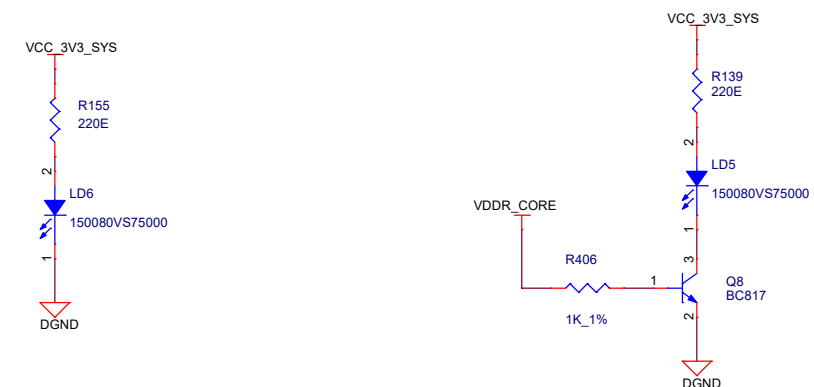


Title USB 2.0 TYPE-A		
Size B	PROC124E2A AM62x-LOW POWER SKEVM	Rev E2A
Date: Friday, May 24, 2024	Sheet 34 of 44	

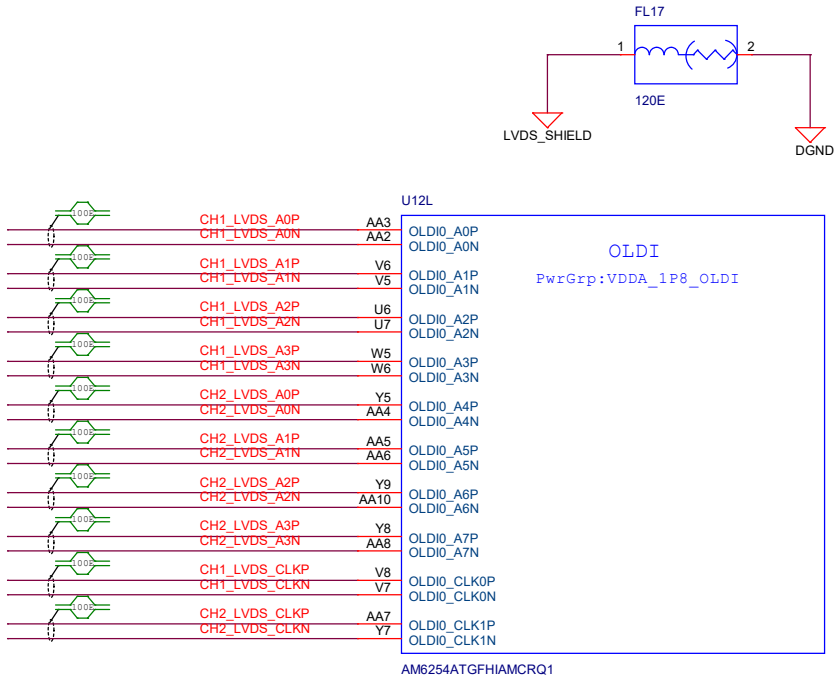
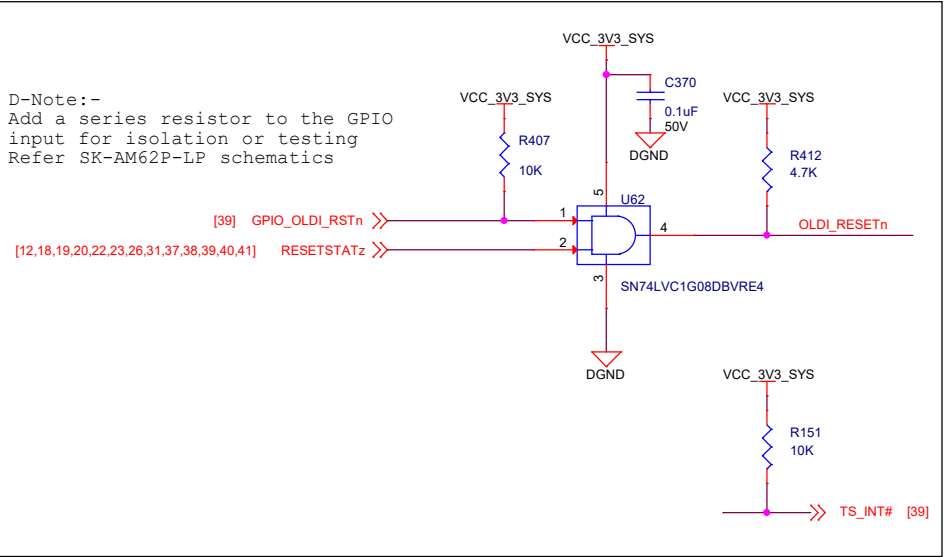
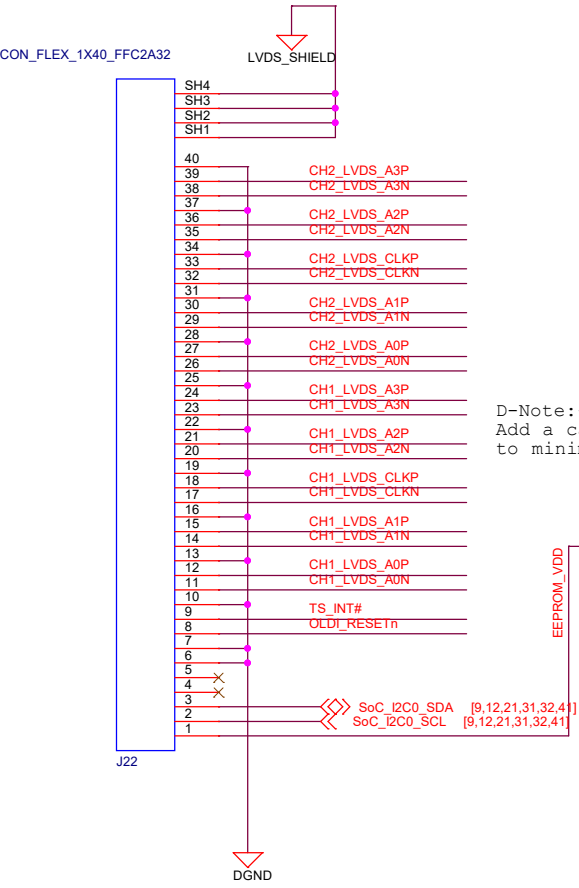
USB 2.0 TYPE-C DRP



R-Note :-
This is a supply negotiation
indicator.
On indicates success.

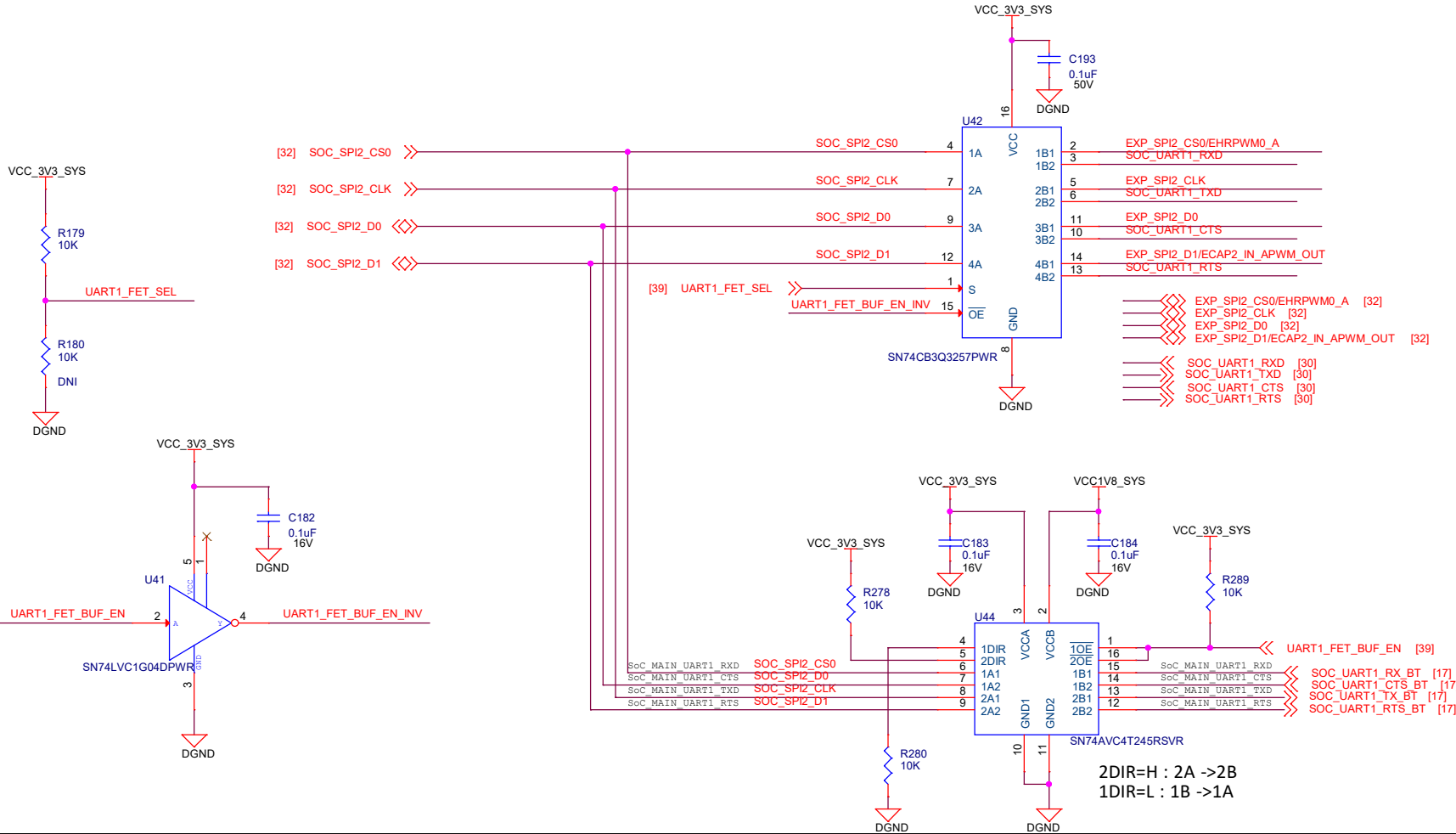


OLDI DISPLAY INTERFACE



D-Note :-
Refer Device Comparison for information on the AMC package device that supports OLDI interface

SoC UART1 FET SWITCH & BUFFER



OEn	SEL	INPUT/OUTPUT An	
L	L	An=nB1	USER EXPANSION CONNECTOR
L	H (DEFAULT)	An=nB2	SOC - FT4232

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Title OLDI DISPLAY INTERFACE

Size C
PROC124E2A AM62x-LOW POWER SKEVM

Rev E2A

Date: Friday, May 24, 2024

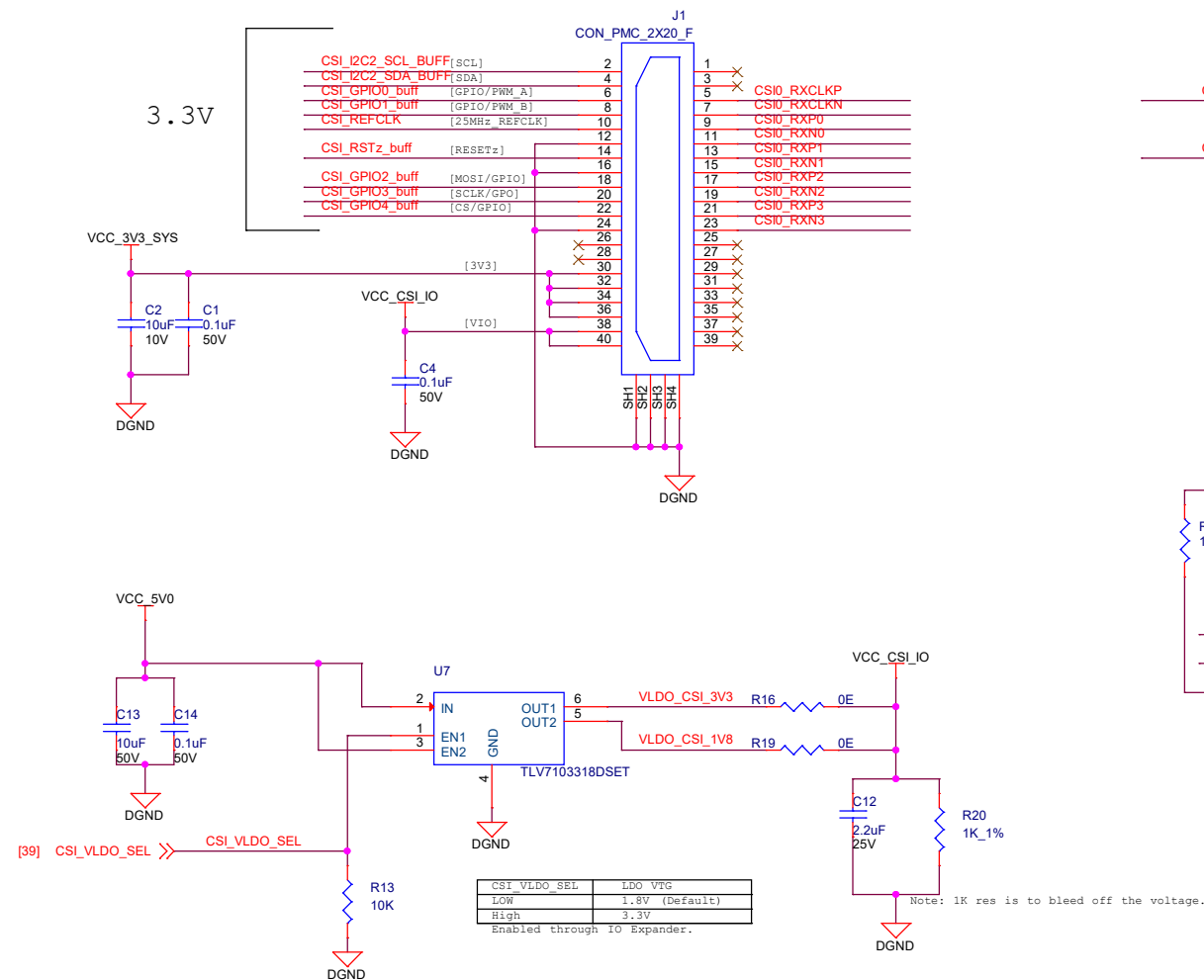
Sheet 36 of 44

CSI INTERFACE

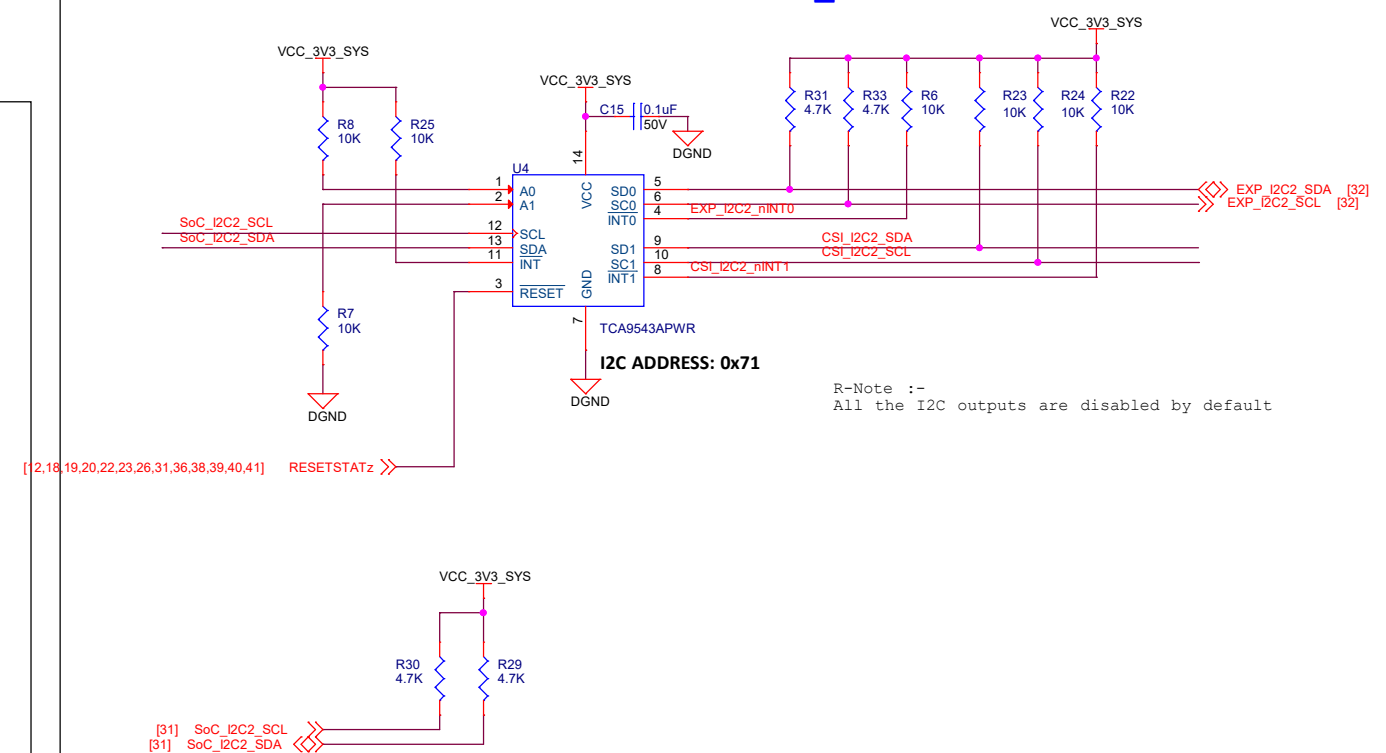
R-Note :-
Based on End product requirement, interface
the CSI signals to respective attach devices

MIPI Connector

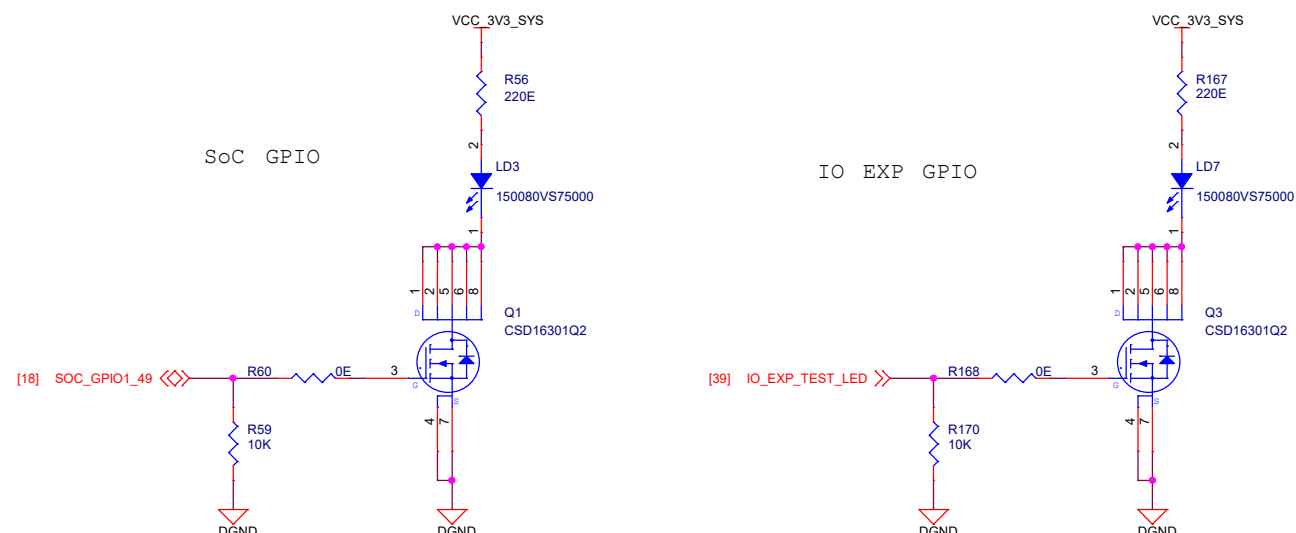
Silk: CSI0 EXP



I2C SWITCH FOR SoC_I2C2



USER TEST LEDS



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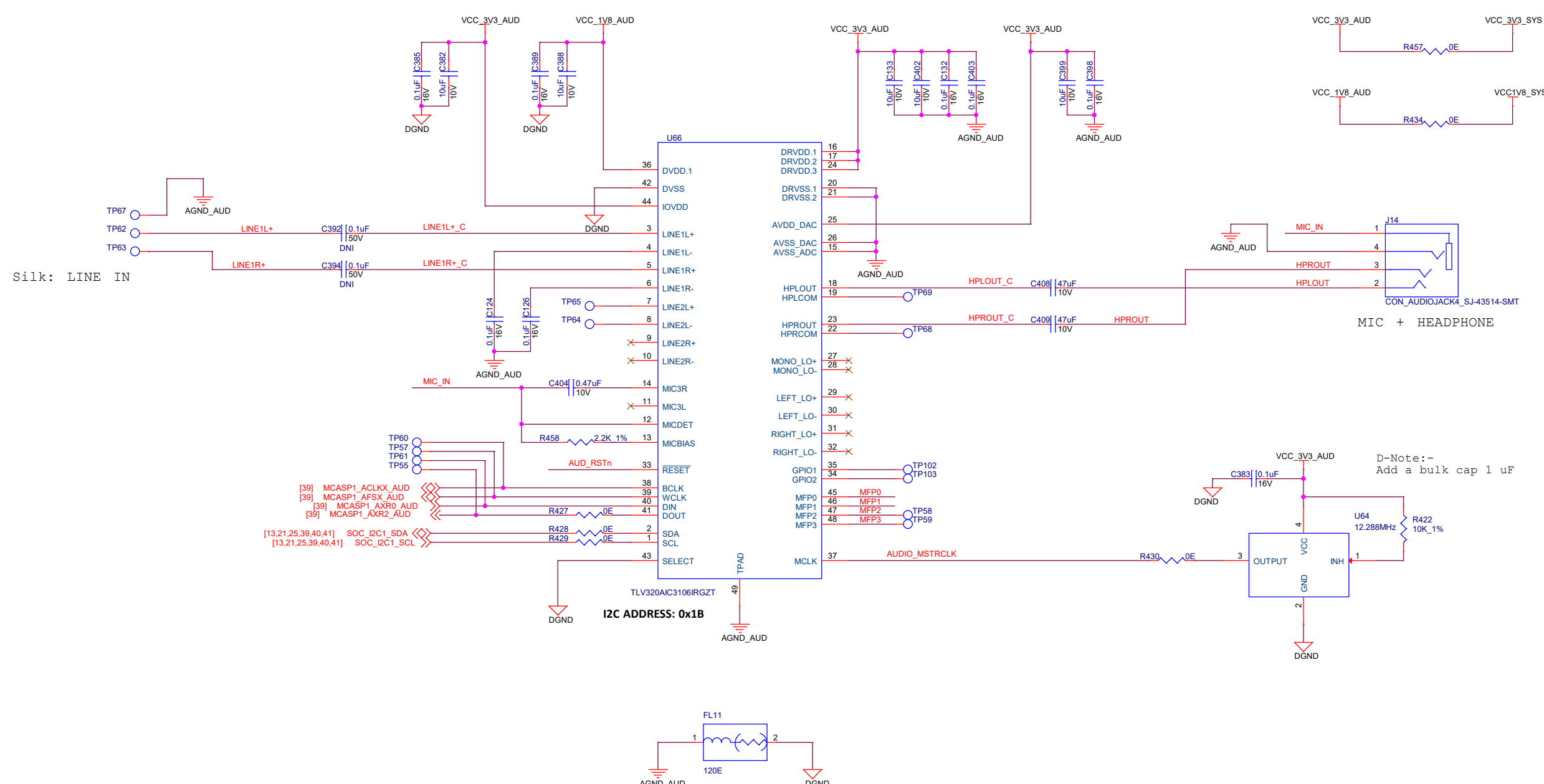


Title	CSI INTERFACE & USER TEST LEDS
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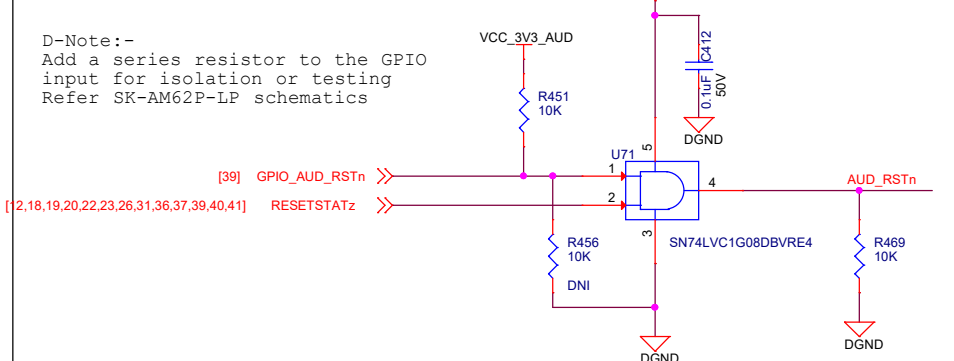
Size	PROC124E2A AM62x-LOW POWER SKEVM
C	

Date:	Friday, May 24, 2024	Sheet	37	of	44
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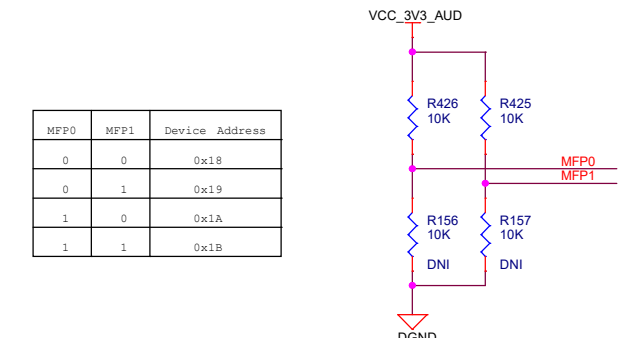
AUDIO CODEC



AUDIO CODEC RESET



CODEC I2C ADDRESS SELECTION

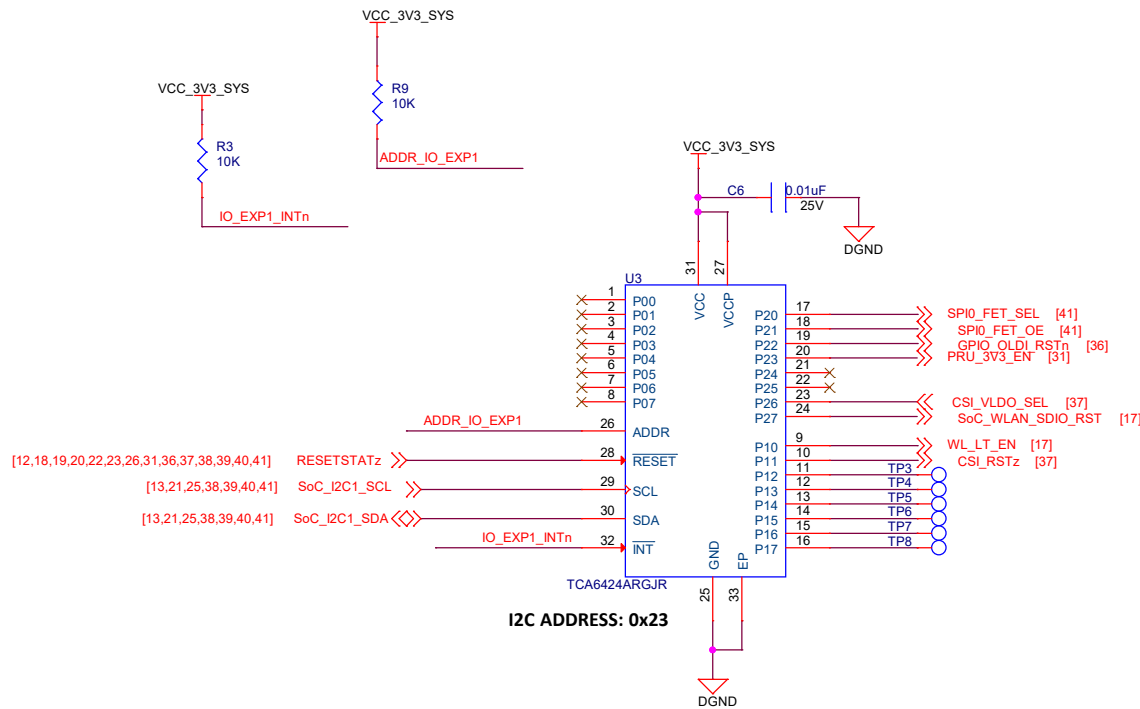
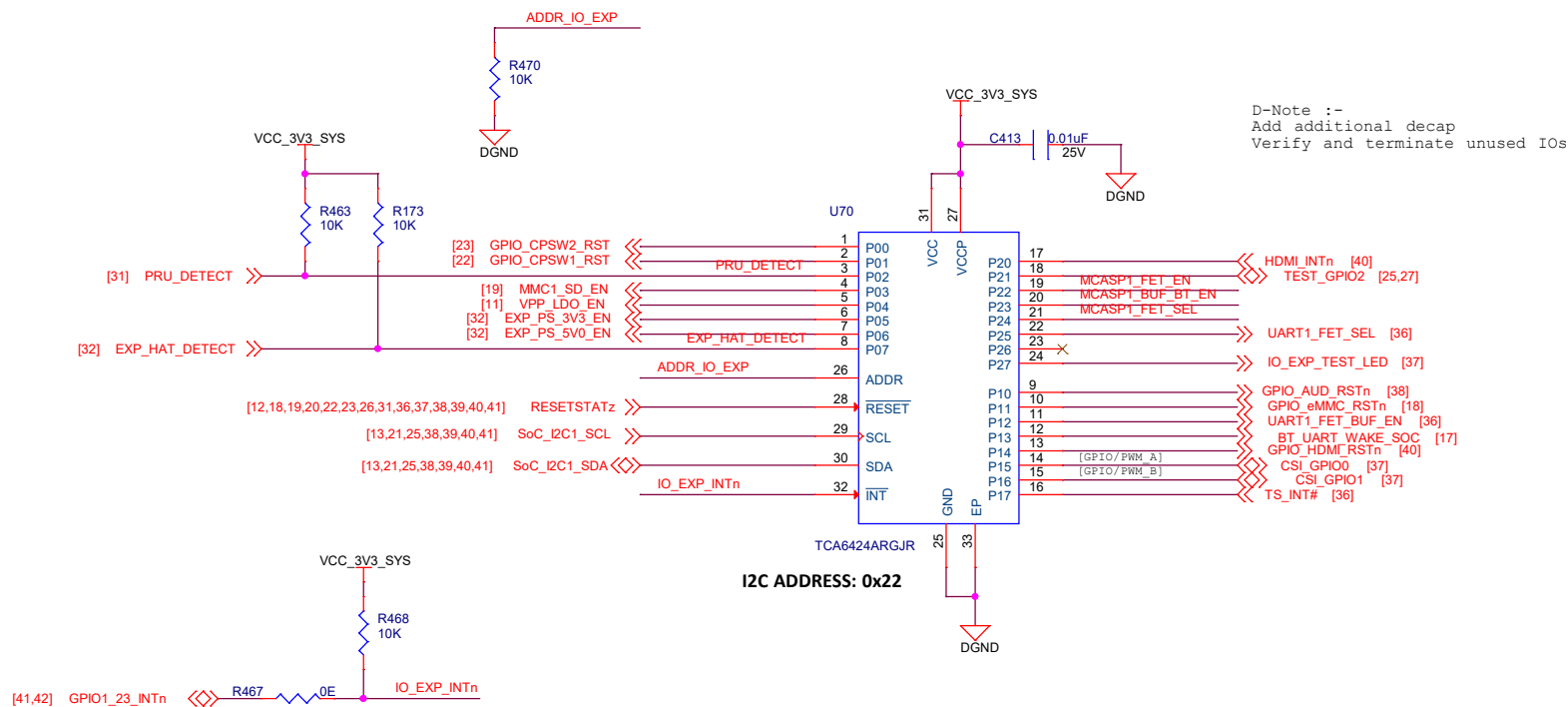


Designed for TI by Mistral Solutions Pvt Ltd

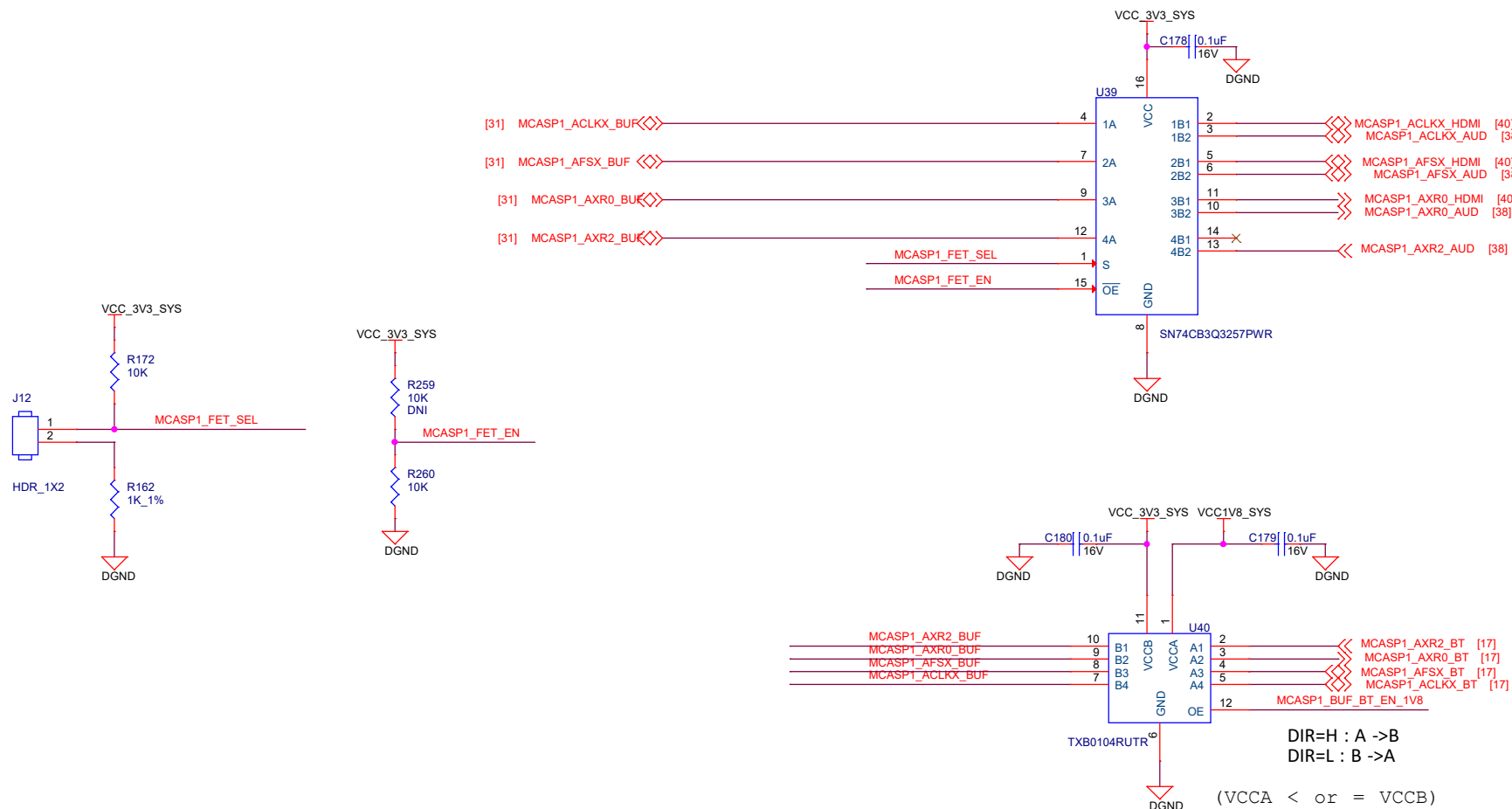


Title		AUDIO CODEC	
Size	C	PROC124E2A AM62x-LOW POWER SKEVM	Rev E2A
Date:	Friday, May 24, 2024	Sheet 38 of 44	

IO EXPANDER



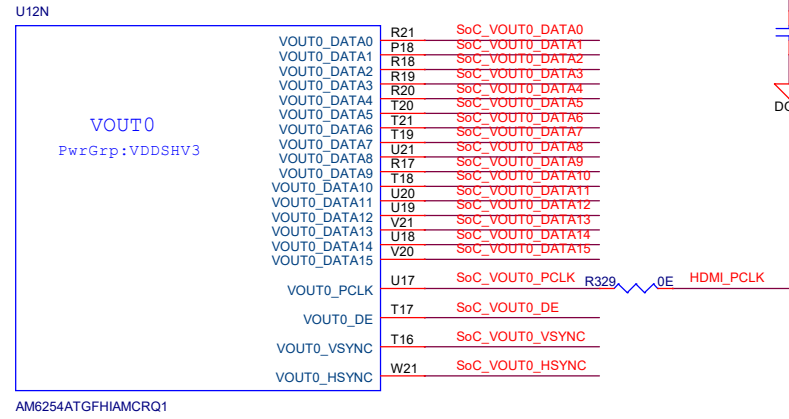
McASP1 FET SWITCH & BUFFER



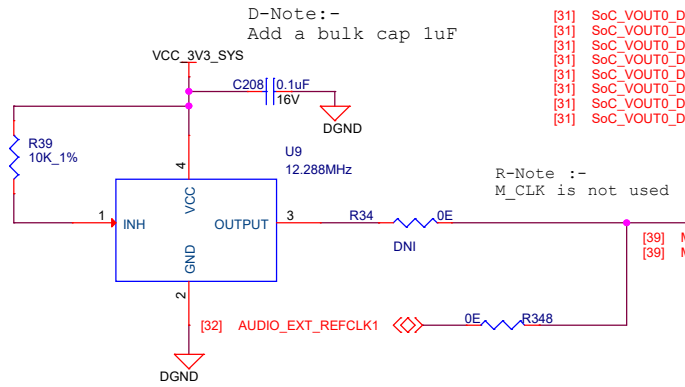
OEn	SEL	INPUT/OUTPUT	
		An=nB2	An
L	H (DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

HDMI INTERFACE

R-Note :-
Verify the implementation with
the device manufacturer

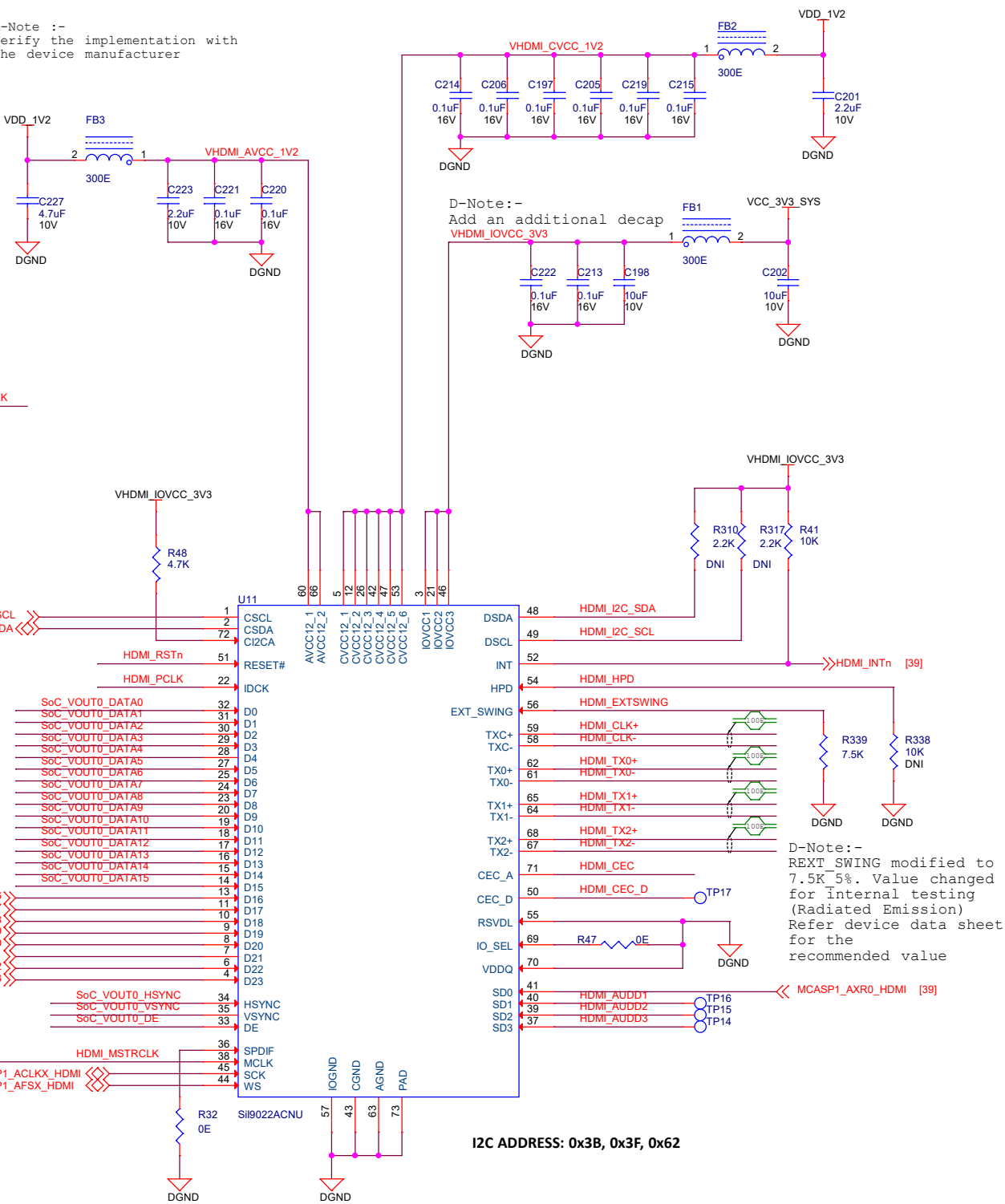


```
Input Mode - RGB888
Clock Mode - 1x
Data Bus Width - 24
(8 bits for Red and Blue and 8 bits for Green)
```

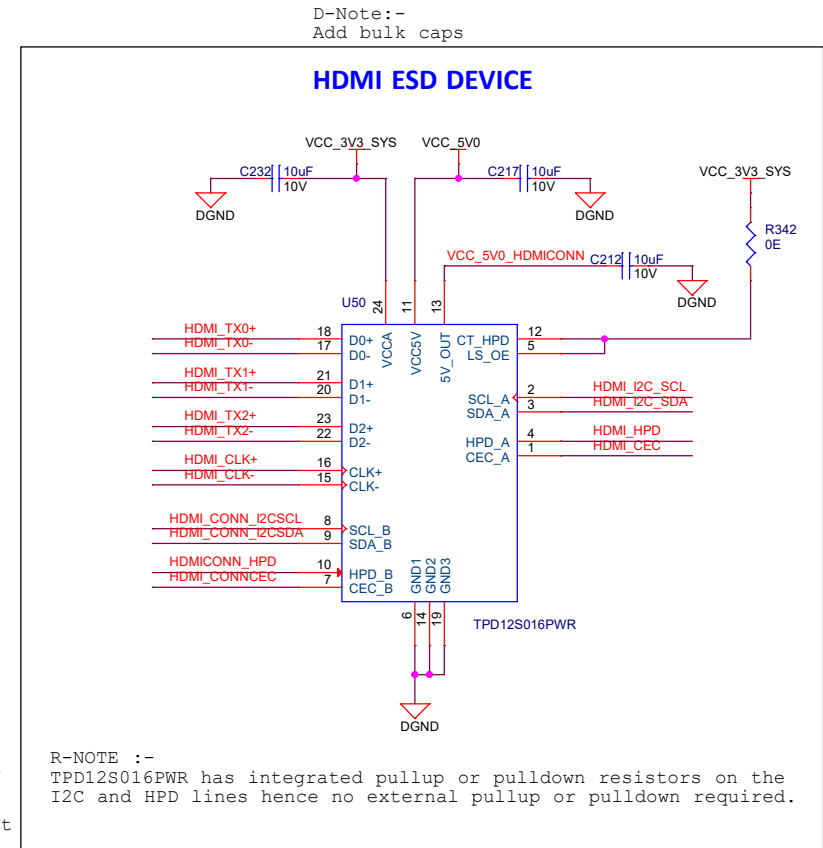


D-Note:-
Add a bulk cap 1uF

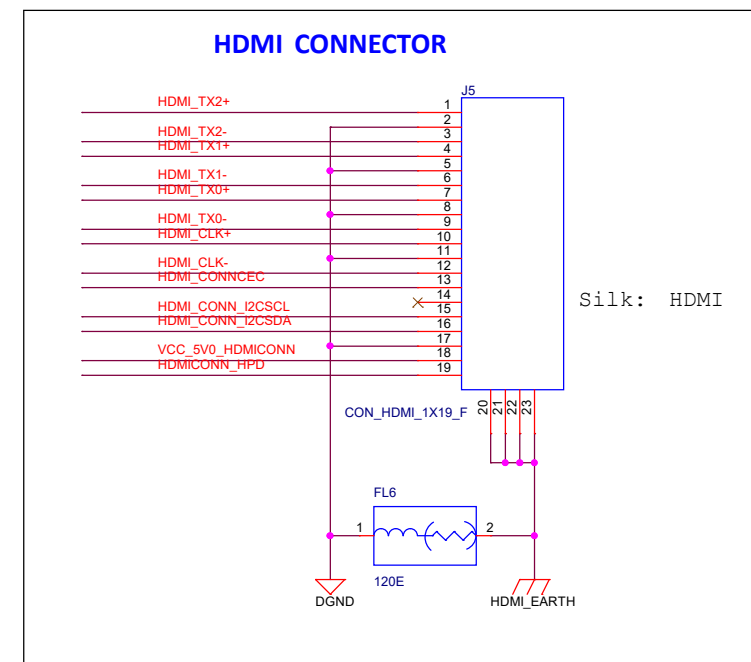
R-Note :-
M_CLK is not used



I2C ADDRESS: 0x3B, 0x3F, 0x62



R-NOTE :-
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.



Silk: HDMI

Designed for TI by Mistral Solutions Pvt Ltd



Title	HDMI INTERFACE
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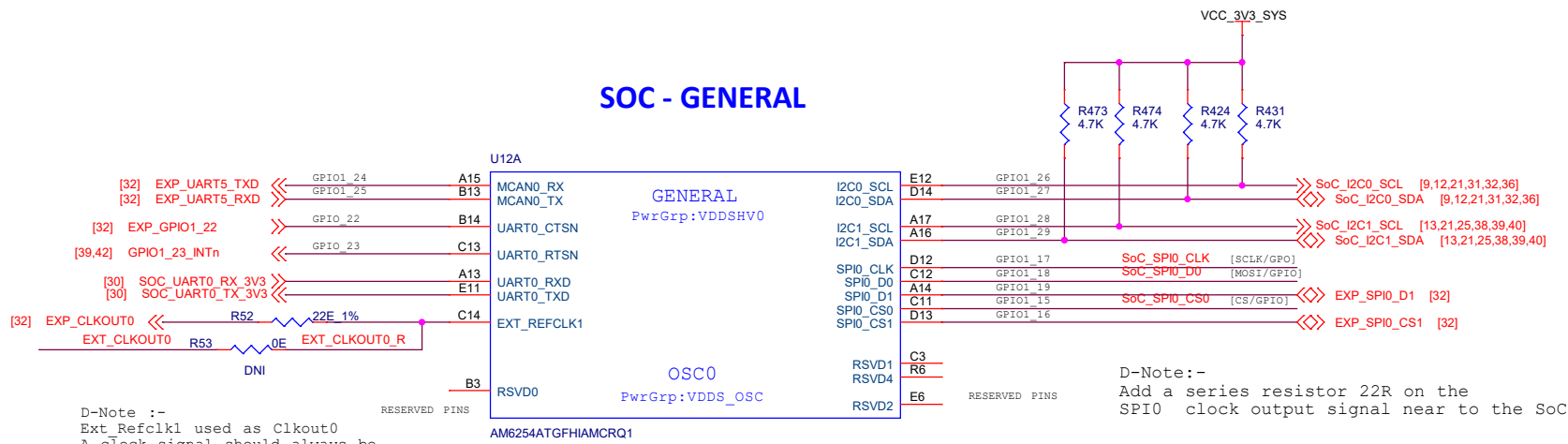
Size	PROC124E2A AM62x-LOW POWER SKEVM
C	

Rev
E2A

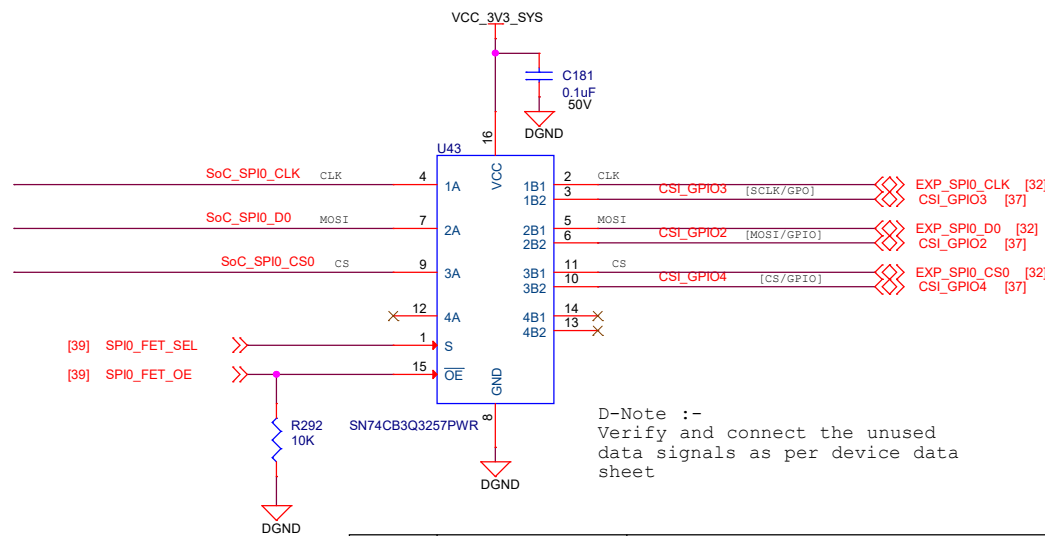
Date: Friday, May 24, 2024

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SOC - GENERAL

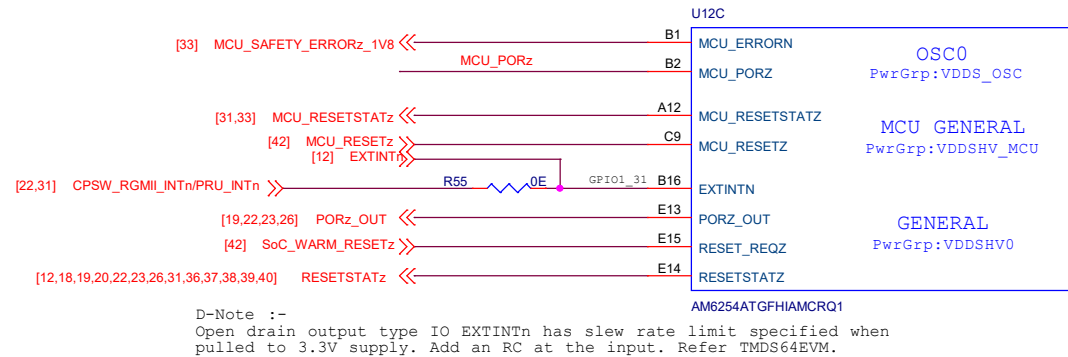


SoC SPI0 FET SWITCH

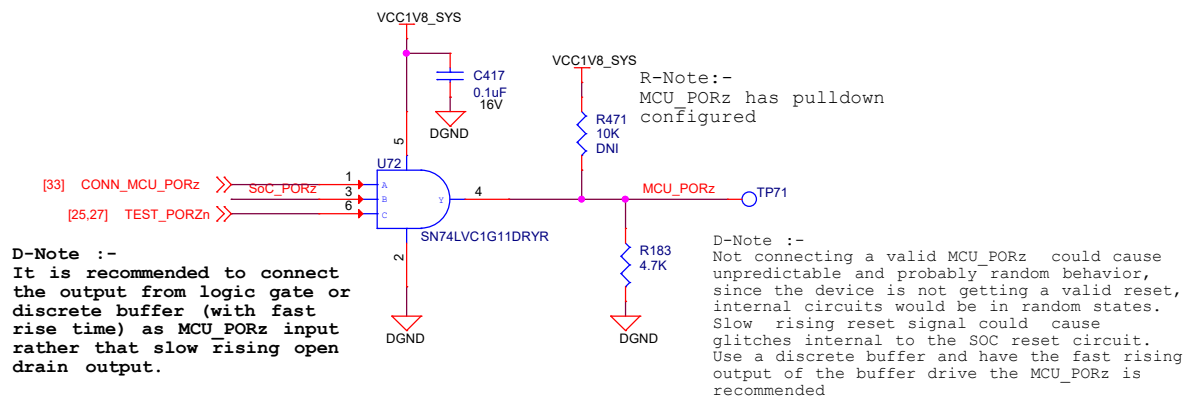


SOC - RESET

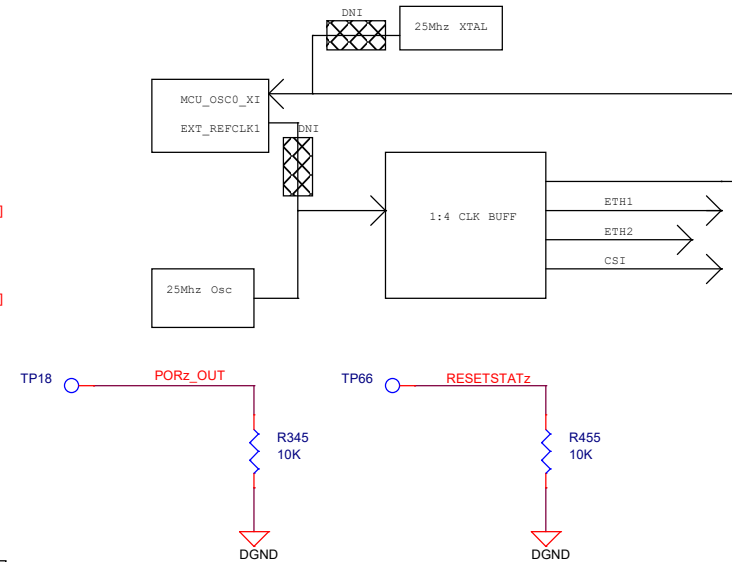
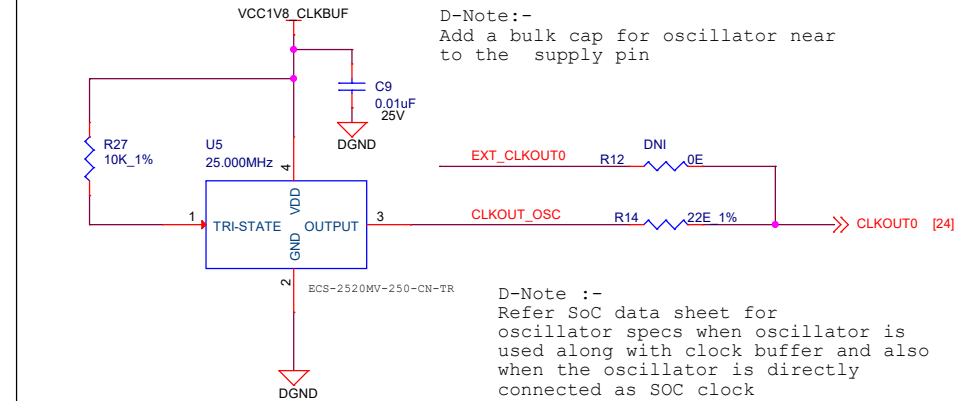
D-Note :-
Provide provision for a pulldown
Populate when attached device is connected
Refer SOC data sheet pin connectivity requirements



MCU POWER ON RESET



OSCILLATOR



D-Note :-
Pull-down resistor on PORz_OUT and RESETSTATz is provided to hold the attached device in reset condition during SOC reset and power-up

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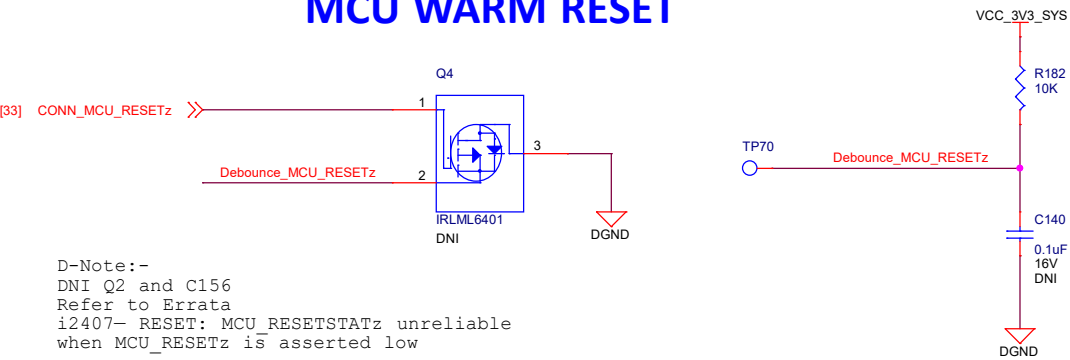


Title OSCILLATOR

Size	Rev
C	E2A
Date: Friday, May 24, 2024	Sheet 41 of 44

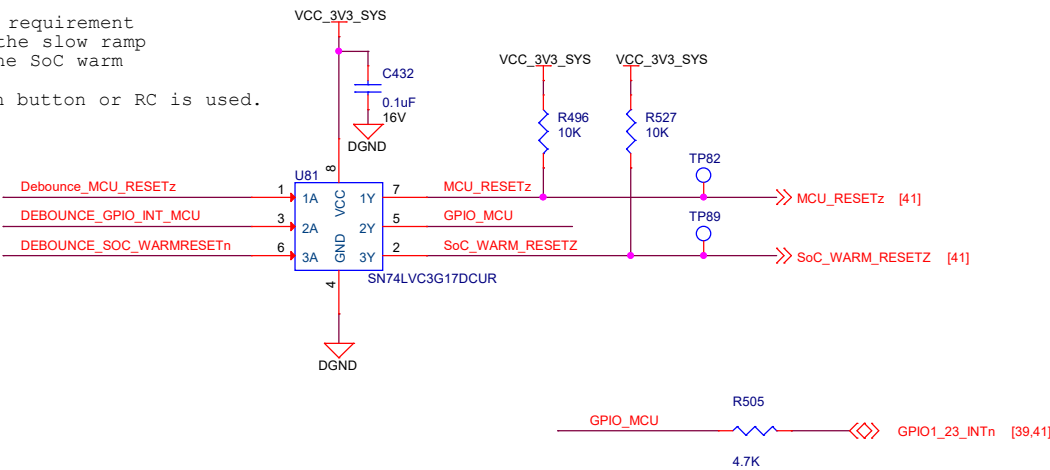
EXTERNAL RESET INPUT AND SCHMITT TRIGGER DEBOUNCE LOGIC

MCU WARM RESET

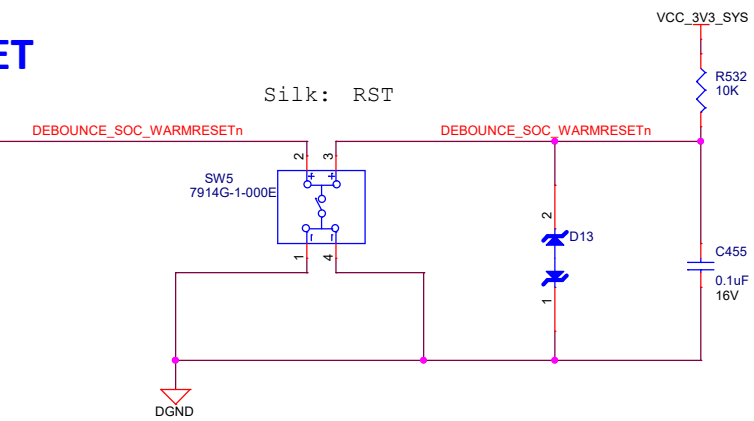
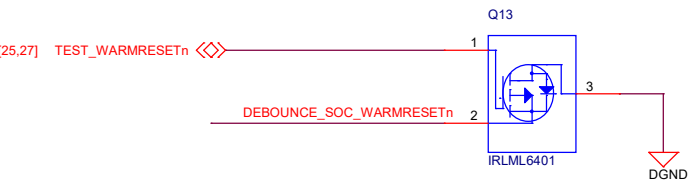


D-Note:-
LVCMOS inputs have slew rate requirement
Schmitt trigger is used for the slow ramp
pushbutton RC connected to the SoC warm
reset inputs
This is recommended when push button or RC is used.

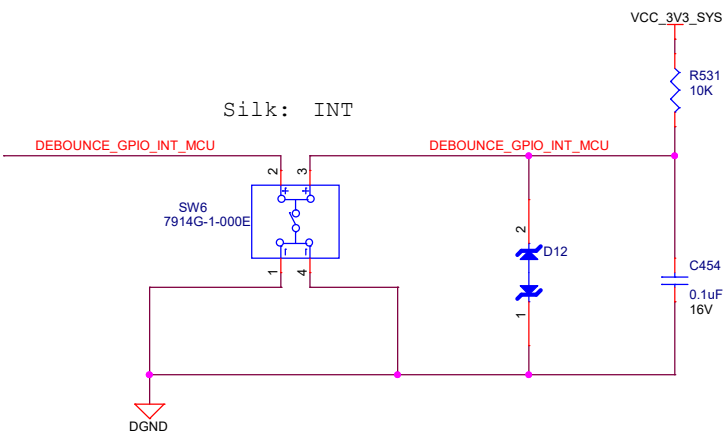
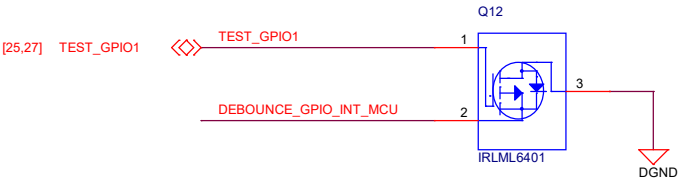
DEBOUNCE CIRCUIT



SOC WARM RESET



USER INTERRUPT



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Title RESET

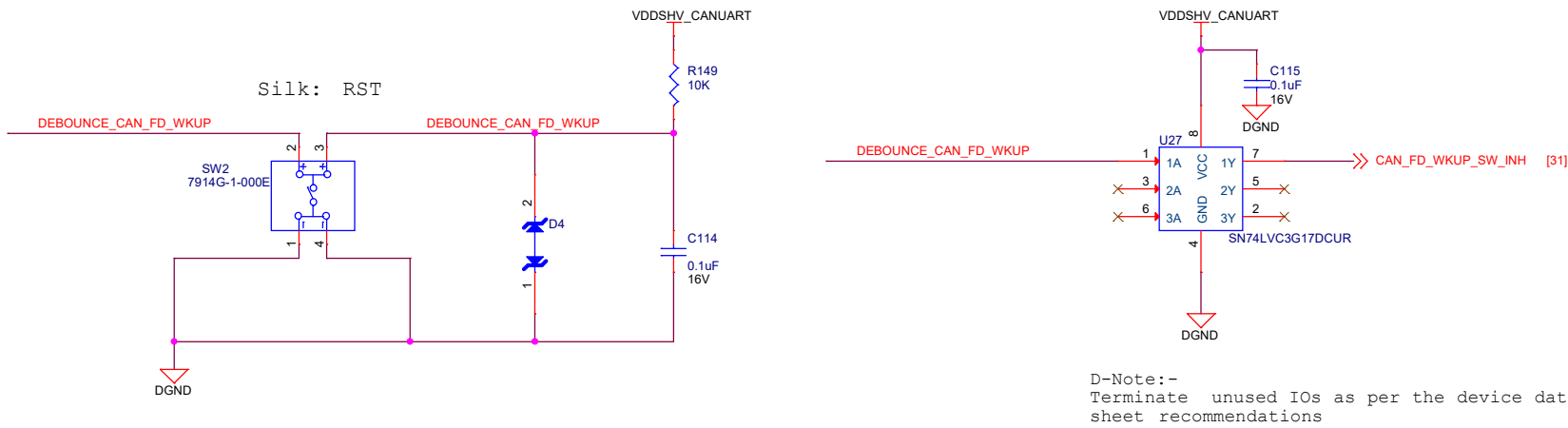
Size C PROC124E2A AM62x-LOW POWER SKEVM

Rev E2A

Date: Friday, May 24, 2024

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CAN-FD FAST WAKE UP SW



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Title CAN FD WKUP SW

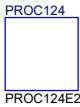
Size	Rev
C	E2A
Date: Friday, May 24, 2024	Sheet 43 of 44

MOUNTING HARDWARE

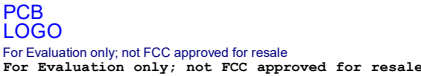
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

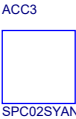
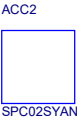
BARE PCB



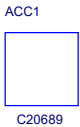
LOGOs



JUMPERS



AM62x LOW POWER SOCKET



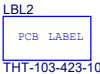
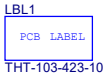
FIDUCIALS



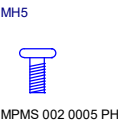
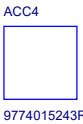
LABELS

Board Serial No.

Assembly Revision



SCREW & WASHER FOR PCIe M.2



R-Note:-
Refer STRAP CONFIGURATION OF ETHERNET PHYS
page from SK-AM64B schematics

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Title HARDWARE SCHEMATICS

Size C PROC124E2A AM62x-LOW POWER SKEVM

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