

FUSION2 SERIAL CAPTURE BOARD

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| | |
|-----|-----|
| REV | E4 |
| VER | 0.5 |

REVISION HISTORY

| VER # | DATE | DESCRIPTION OF CHANGES | AUTHOR | REVIEWED BY | APPROVED BY |
|---------|----------------|--|---------------------|-------------|-------------|
| 0.1 | 11th AUG 2022 | Drafted from Rev E2 | Mistral Design Team | | |
| 0.2 | 24th AUG 2022 | Updated 12V regulator section | Mistral Design Team | | |
| 0.3 | 14th OCT 2022 | Updated 971 PART number to DS90UB971RHBRQ1 | Mistral Design Team | | |
| 0.4 | 123h JUNE 2023 | Updated R233 part value 4.87K to 402E | Mistral Design Team | | |
| E4(0.5) | 26th JUL 2024 | Drafted from Rev E3 Fix for the U36 P-Channal MOSFET Direction Dual footprint provision for the RADAR input connectors - J3,J6,J9,J12. Alternate inductor added for the L29. GPIO option provided for HUB 1,2 and 3 GPIO4 GPIO option provided for Serializer GPIO3 | Mistral Design Team | | |
| | | | | | |

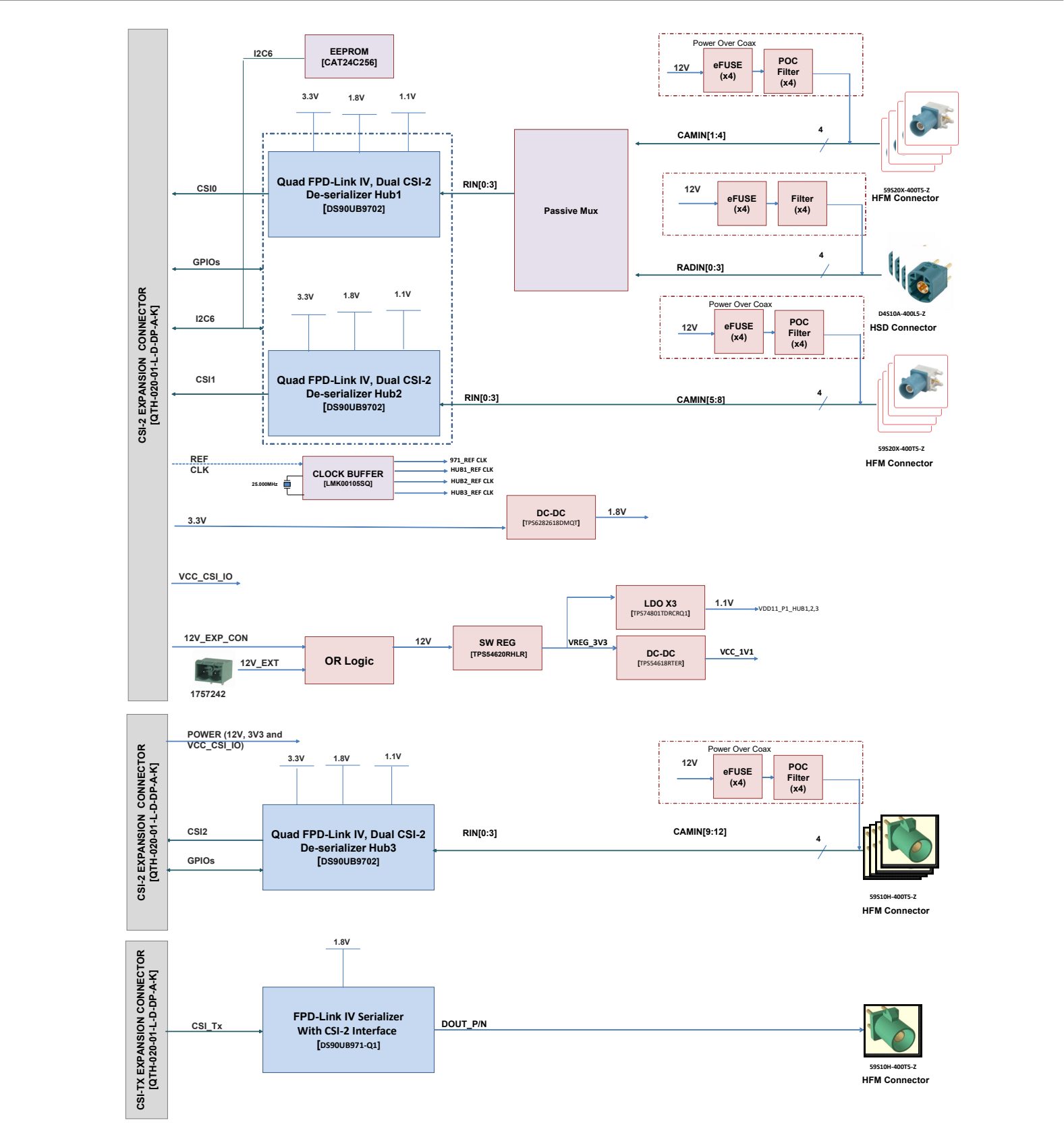
Project :

J7 EVM

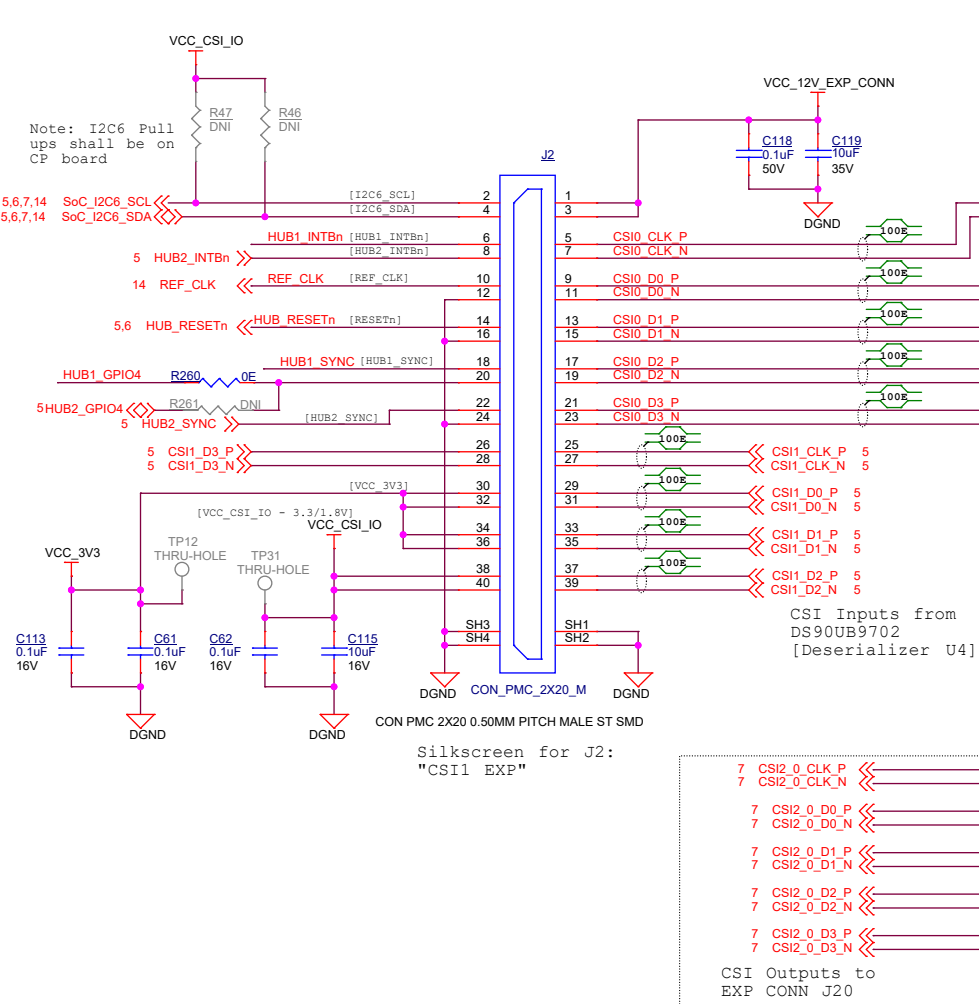


| | | | |
|-------|------------------------------|------------------|---------|
| Title | | REVISION HISTORY | |
| Size | PROC082 001 J7EXP0A01EVM | | Rev |
| C | | | E4 |
| Date: | Thursday, September 10, 2020 | Sheet | 2 of 16 |

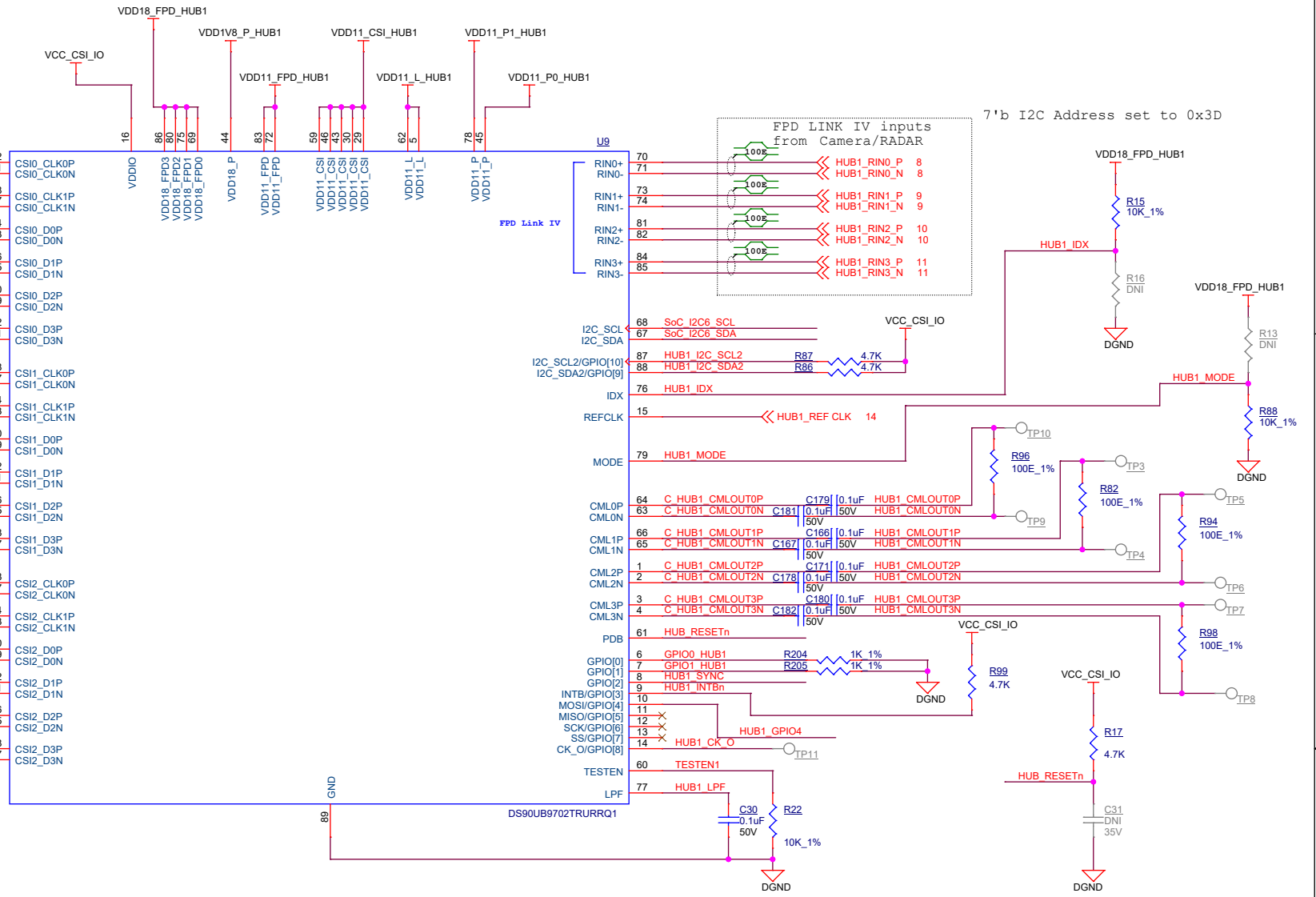
BLOCK DIAGRAM(TBU)



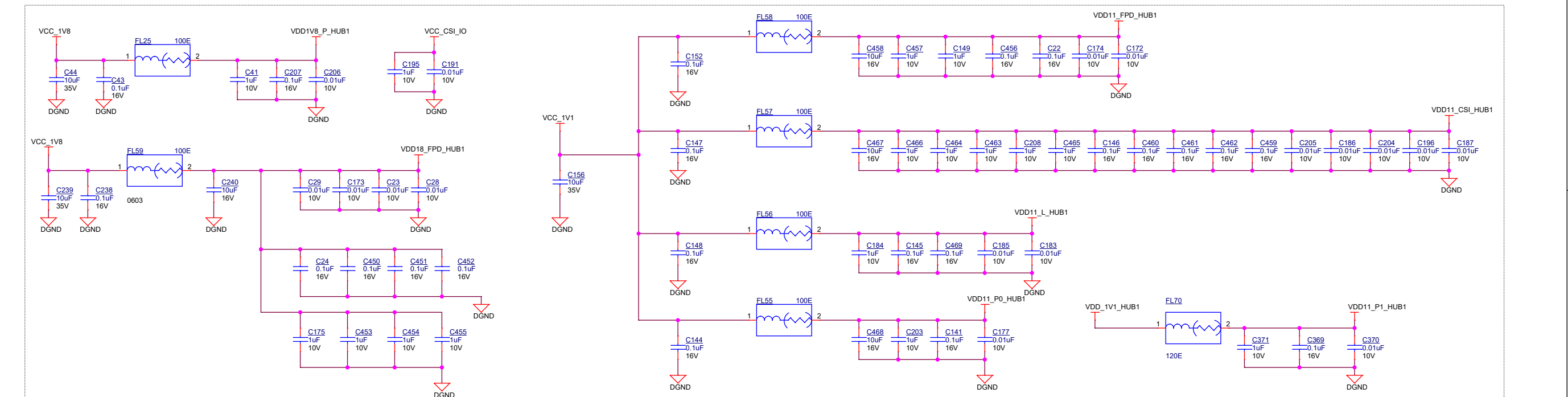
Expansion Connector 1



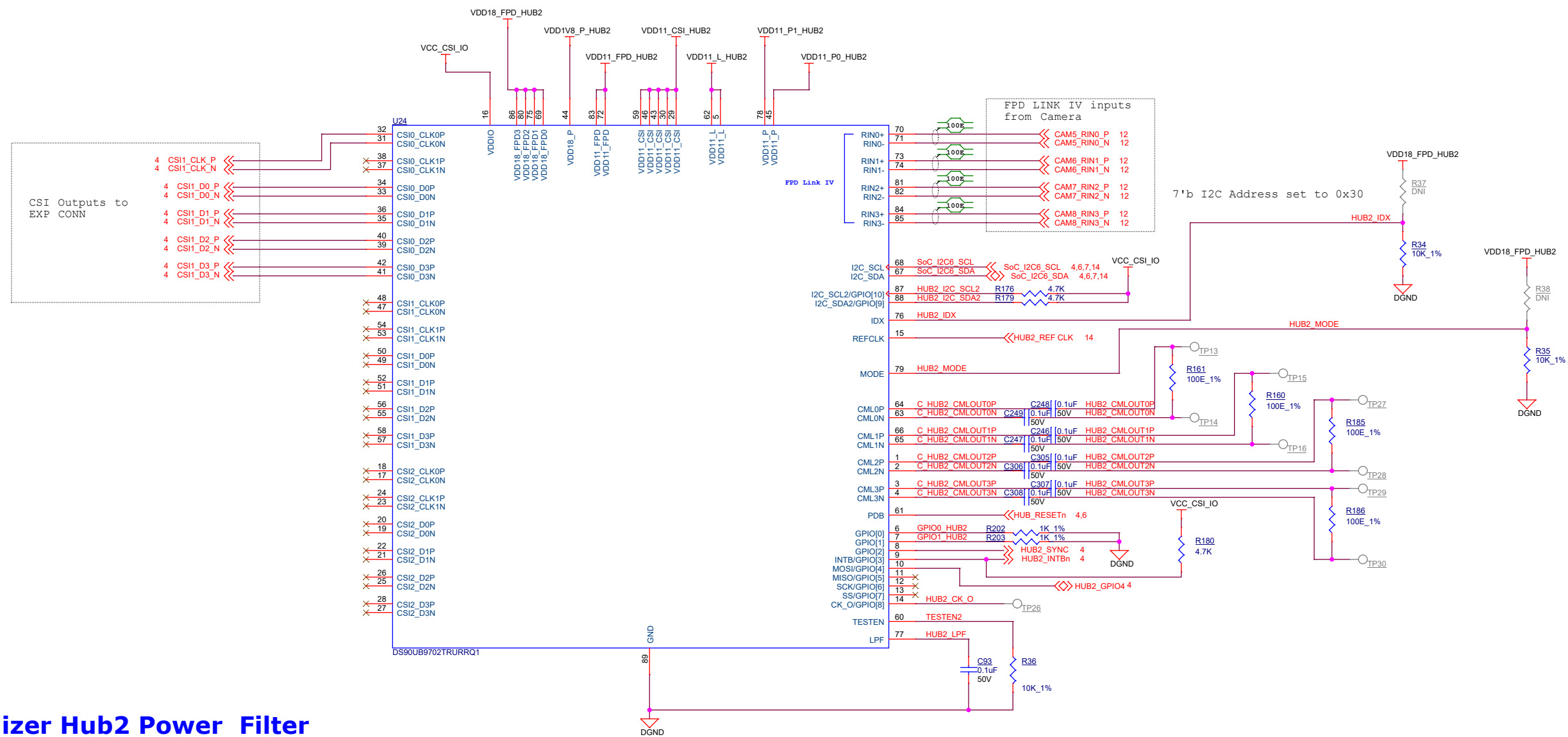
FPD Link IV to CSI-2 De-Serializer Hub-1



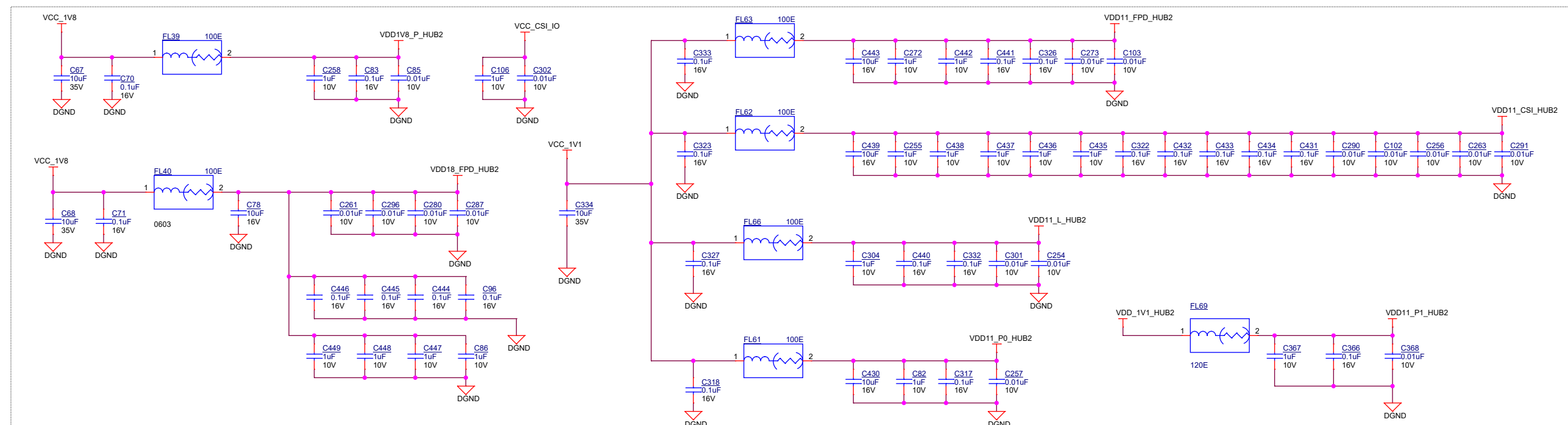
De-Serializer Hub1 Power Filter



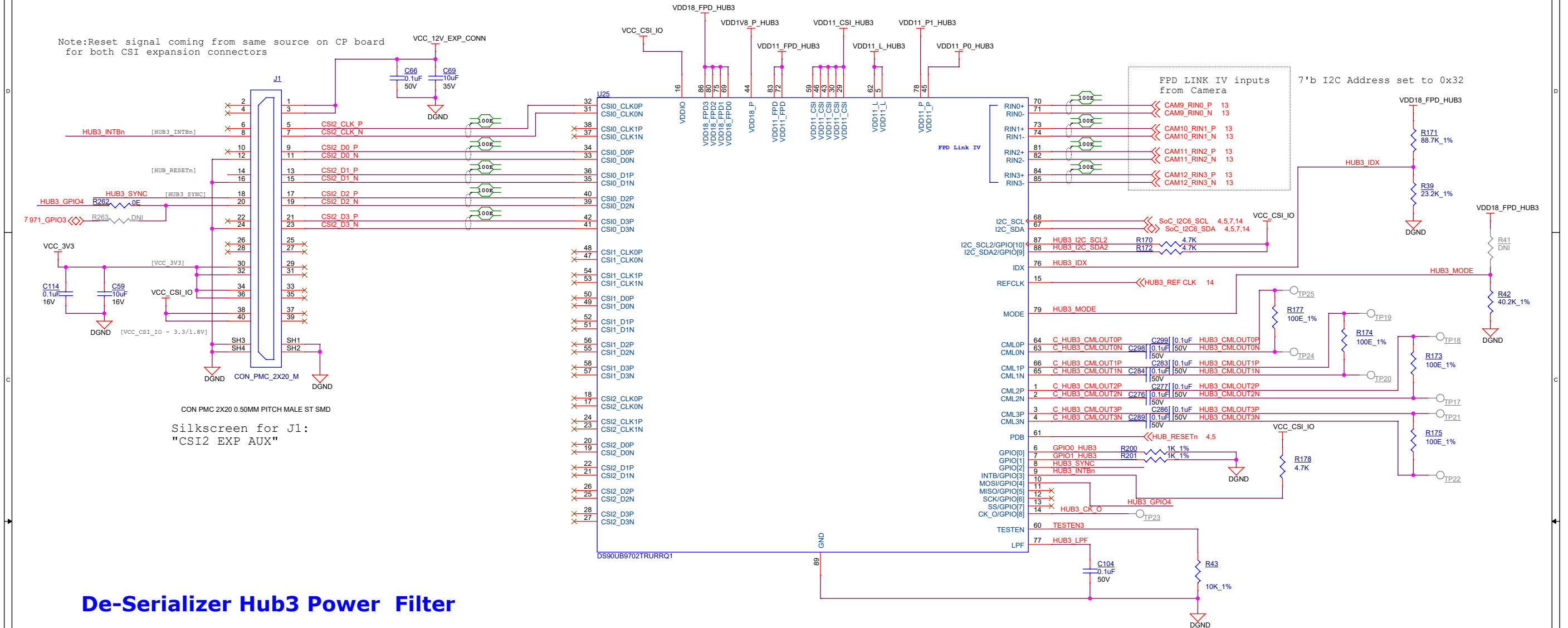
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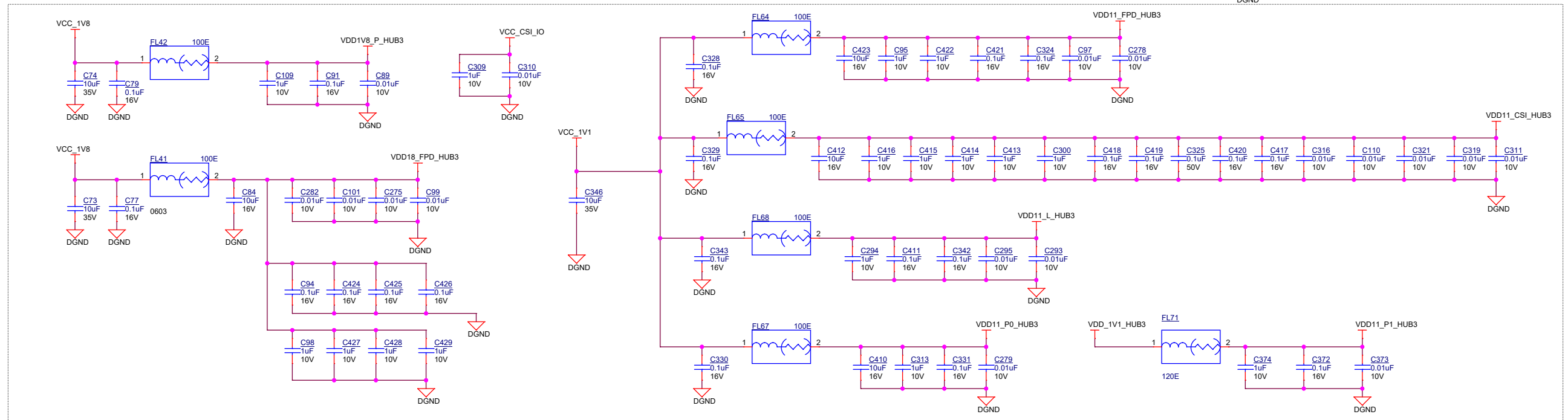
De-Serializer Hub2 Power Filter



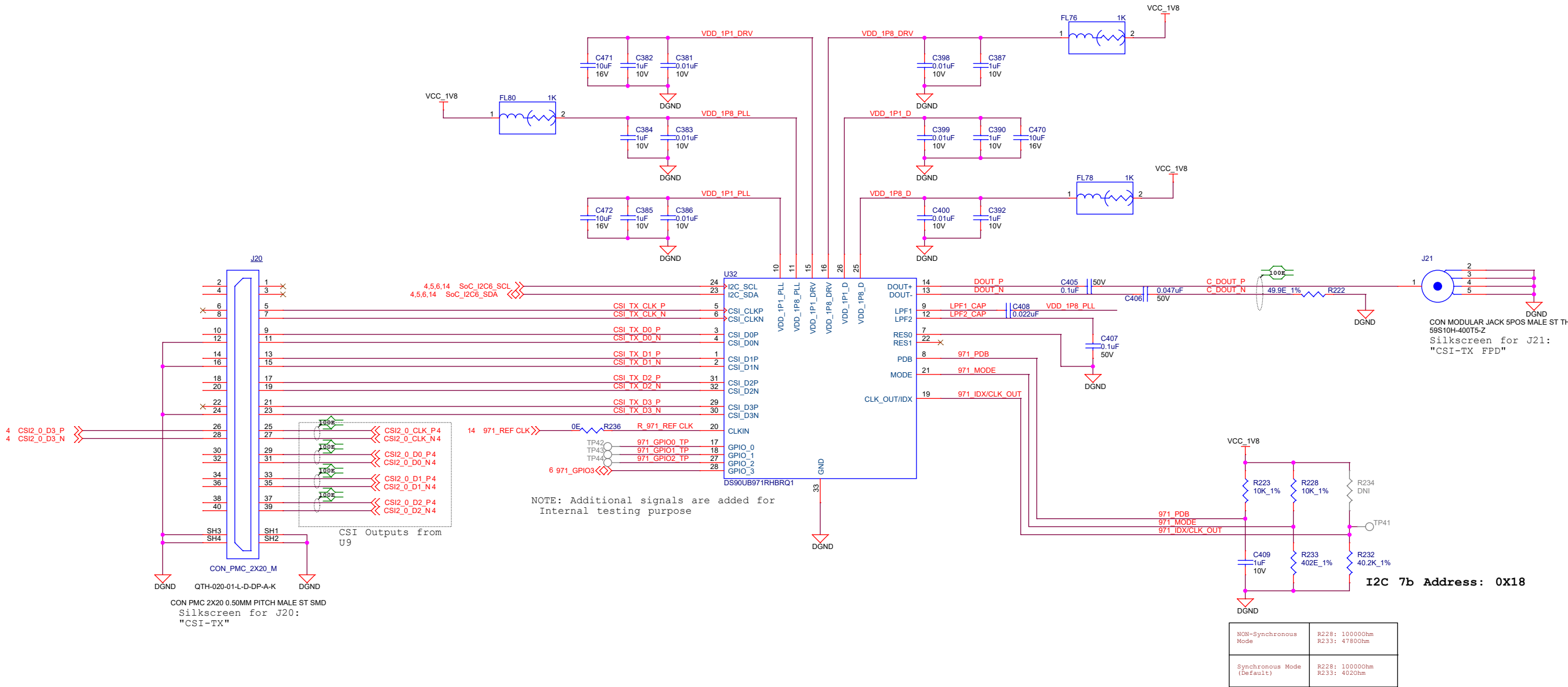
FPD Link IV to CSI-2 De-Serializer Hub - 3



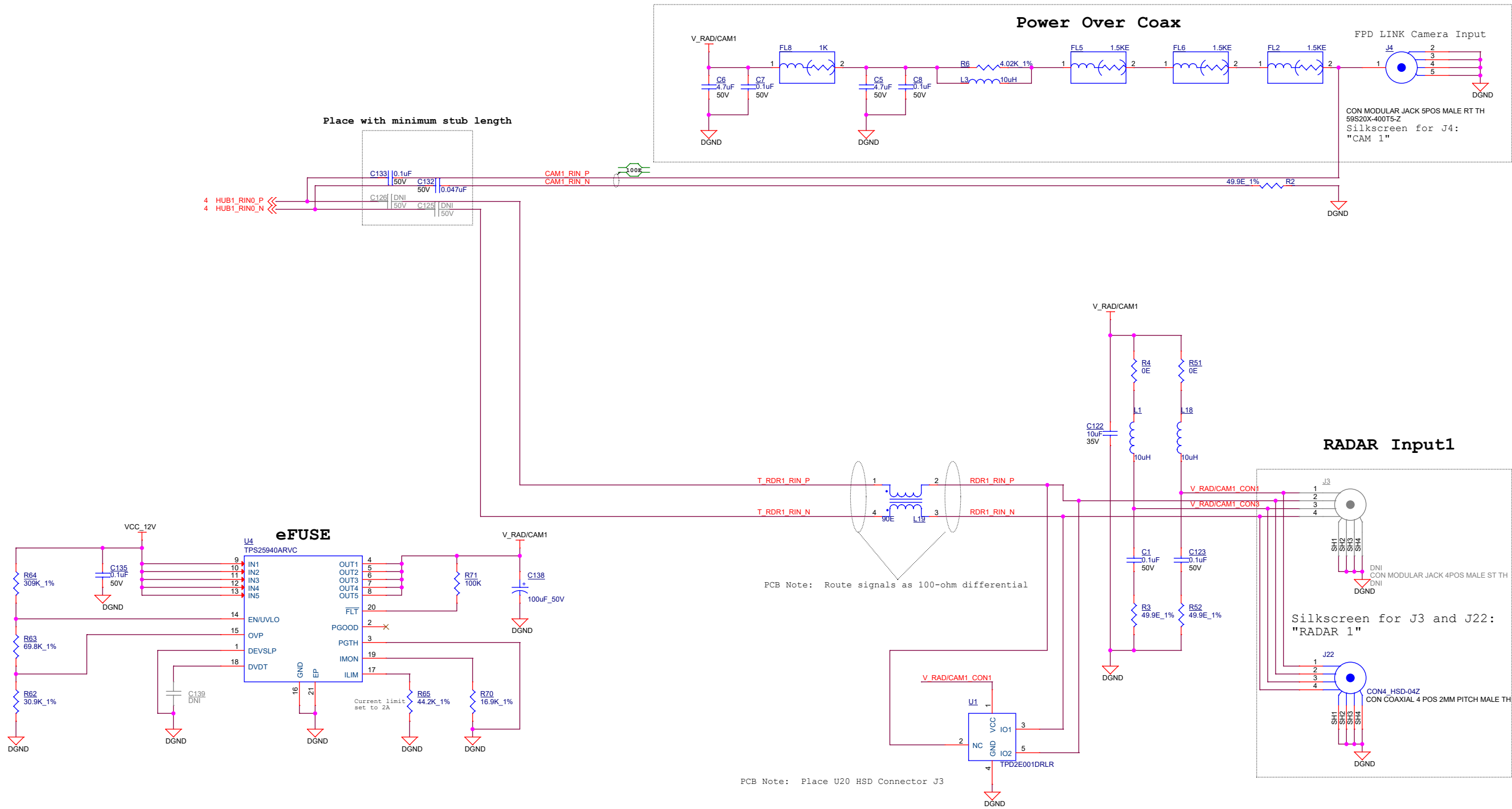
De-Serializer Hub3 Power Filter



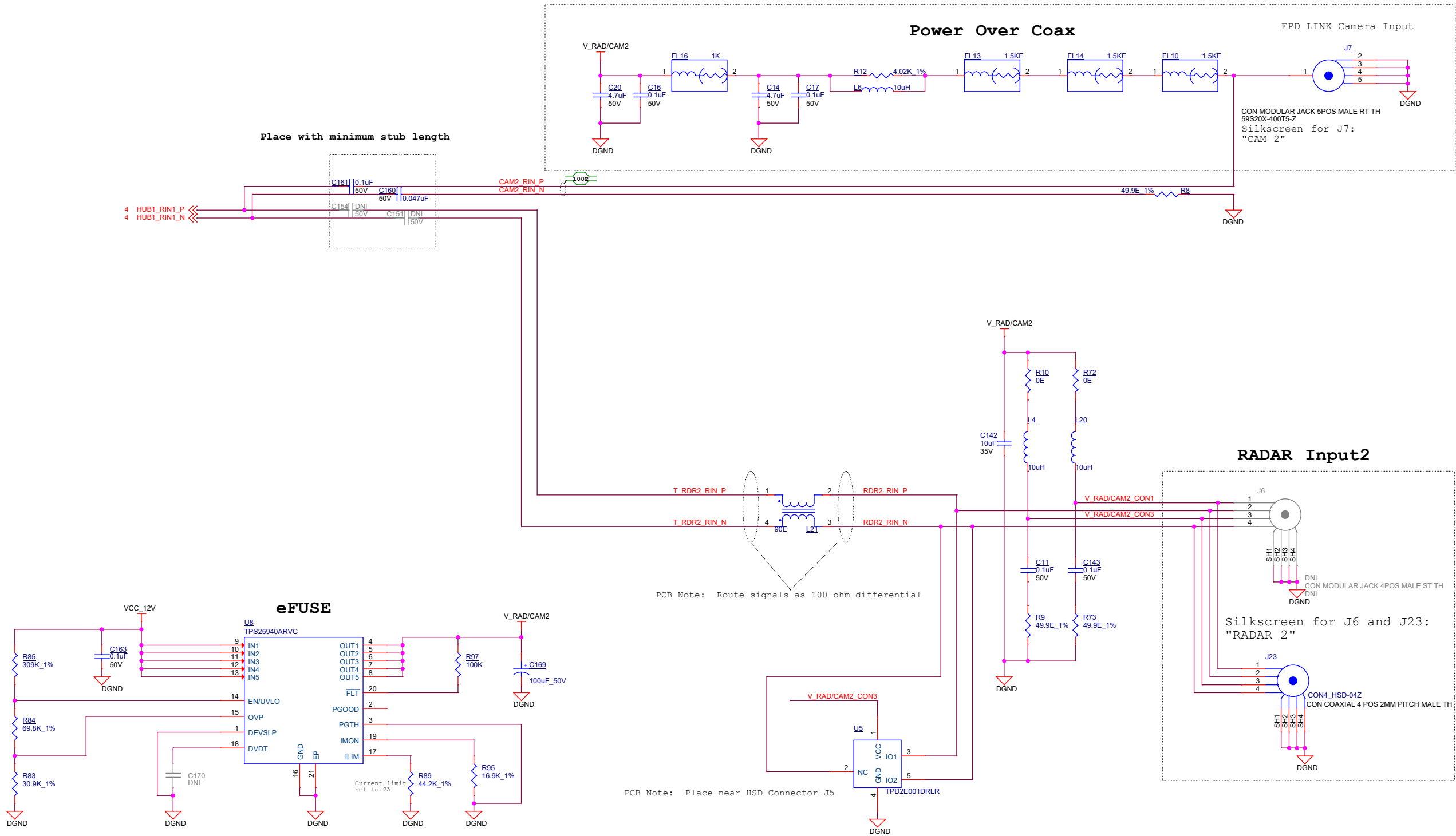
CSI to FPD Link IV Serializer 971'



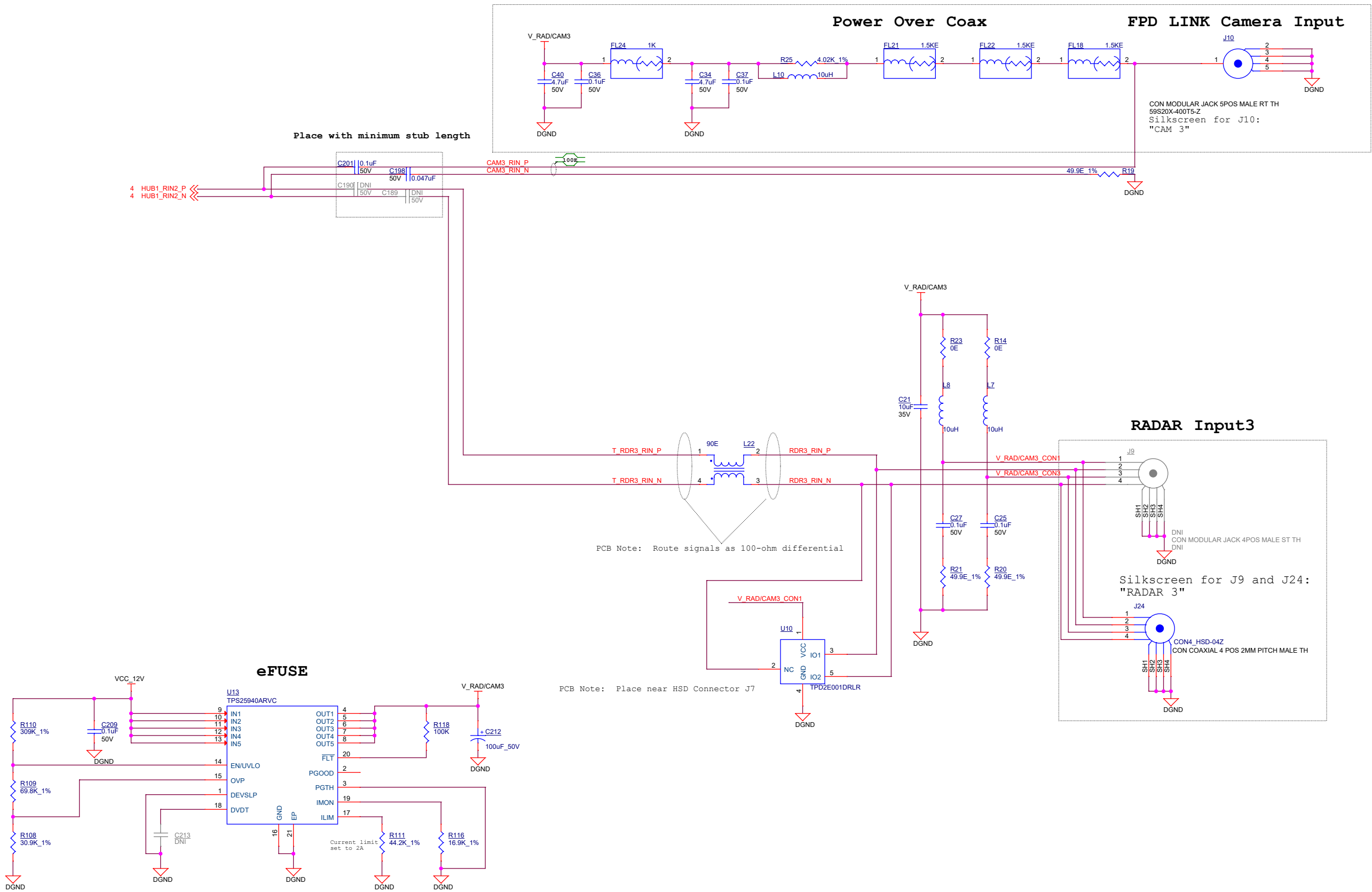
FPD Link Camera/RADAR Input1



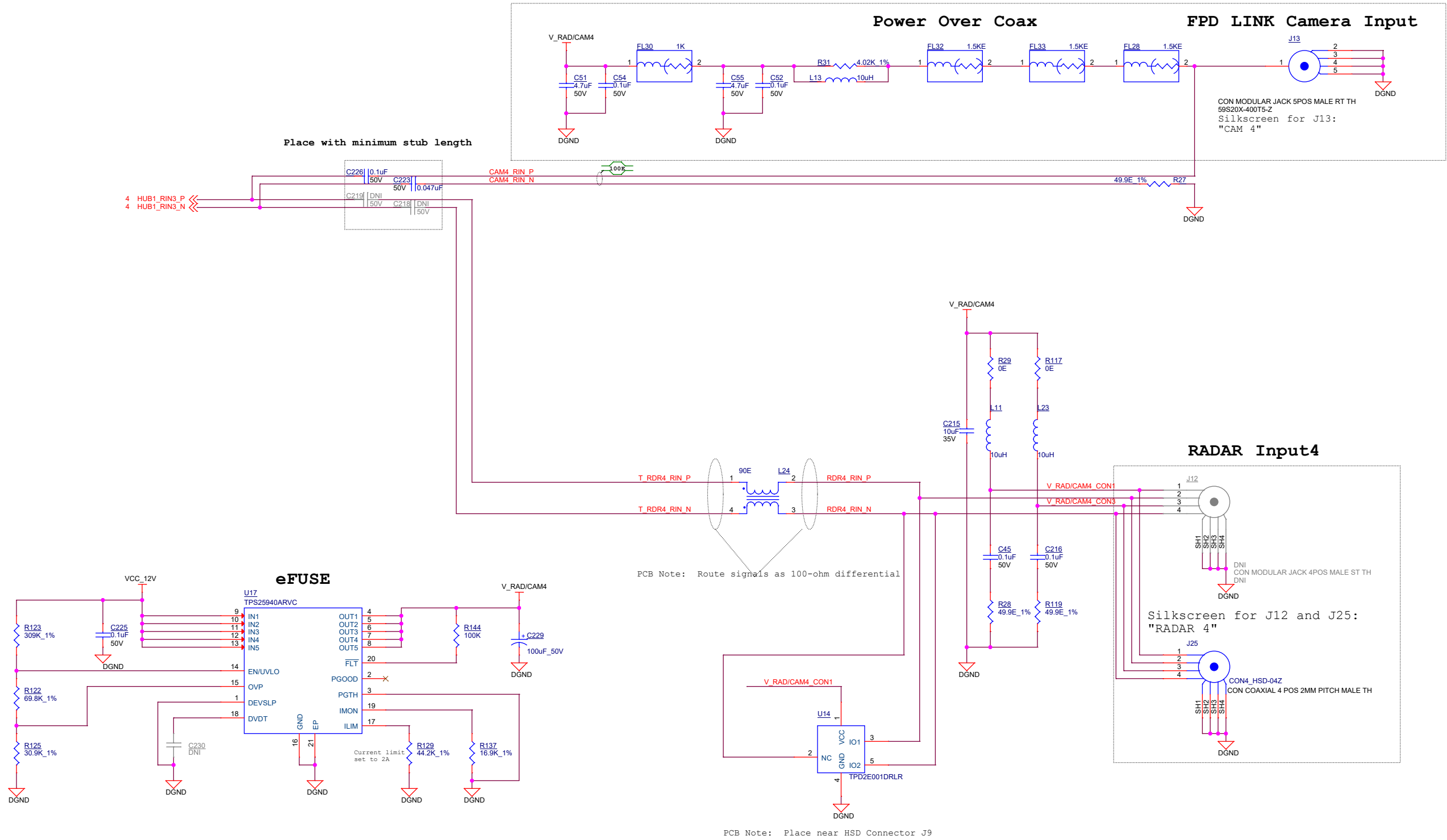
FPD Link Camera/RADAR Input2



FPD Link Camera/RADAR Input3

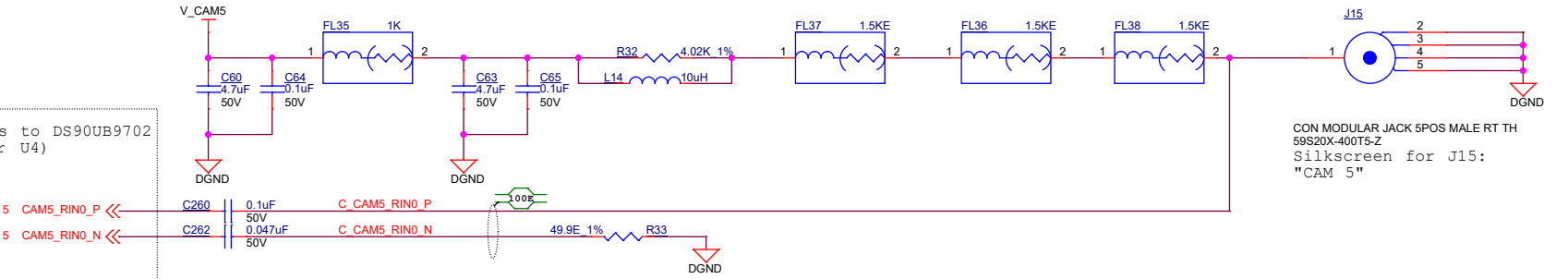


FPD Link Camera/RADAR Input4

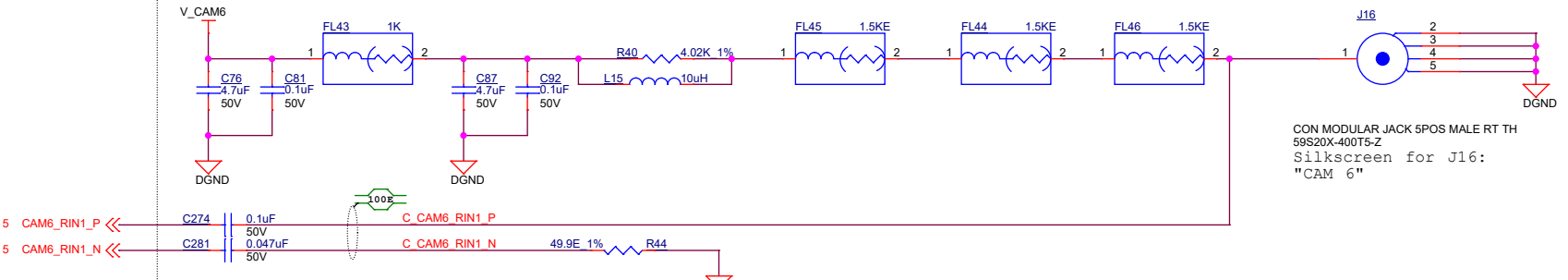


FPD Link Camera Inputs 5-8

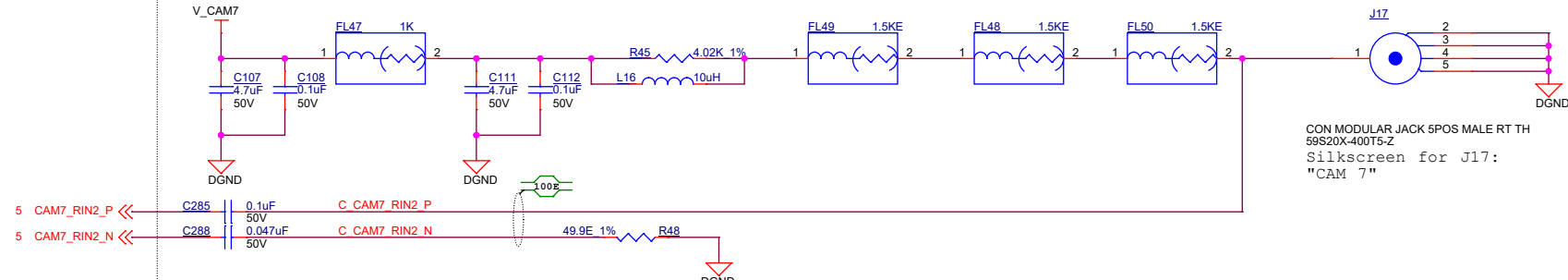
Power Over Coax



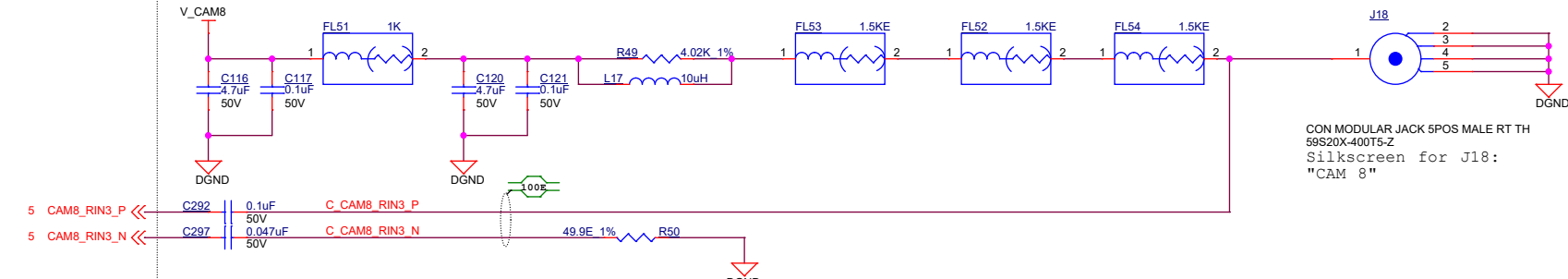
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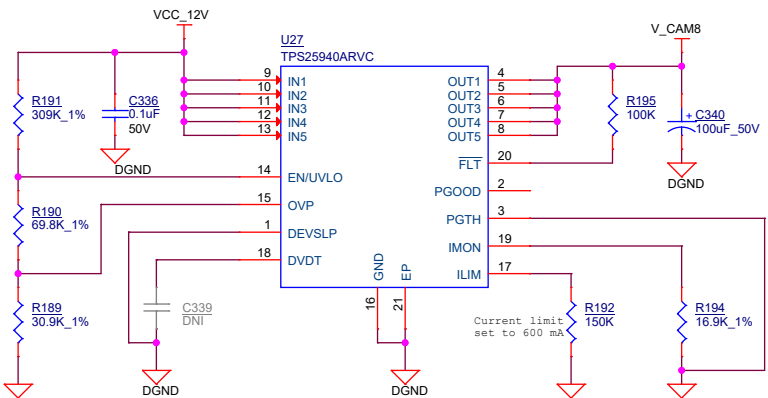
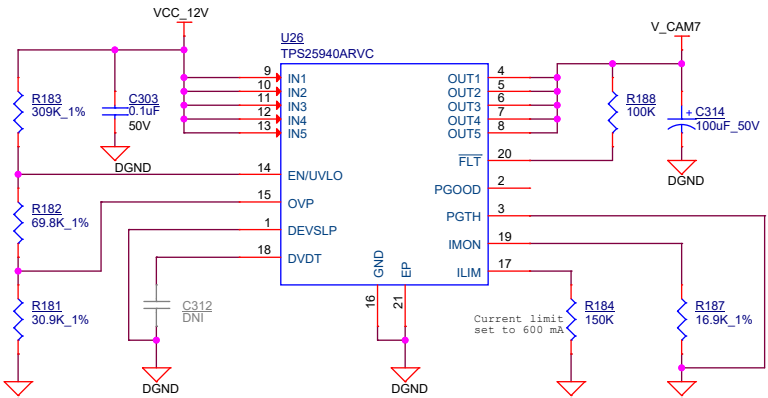
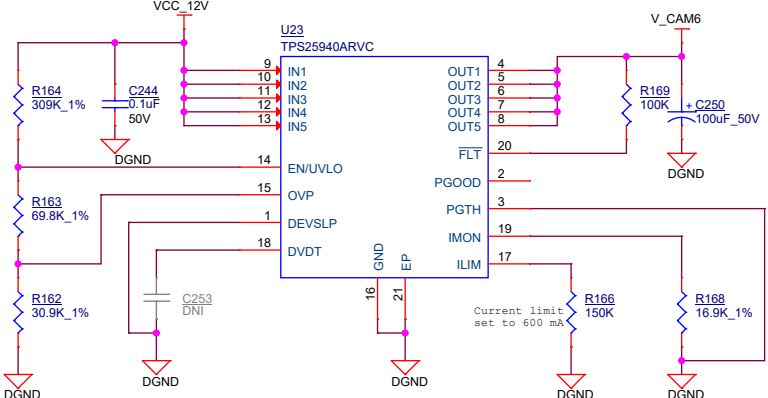
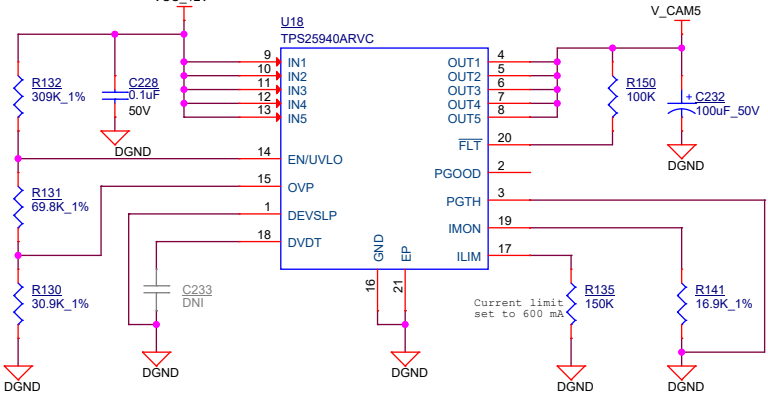
Power Over Coax



Power Over Coax

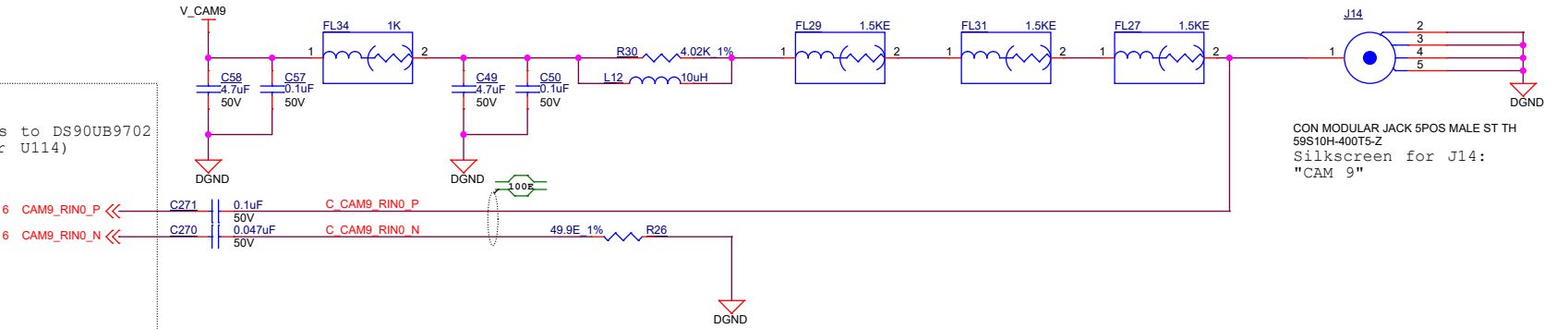


eFUSE

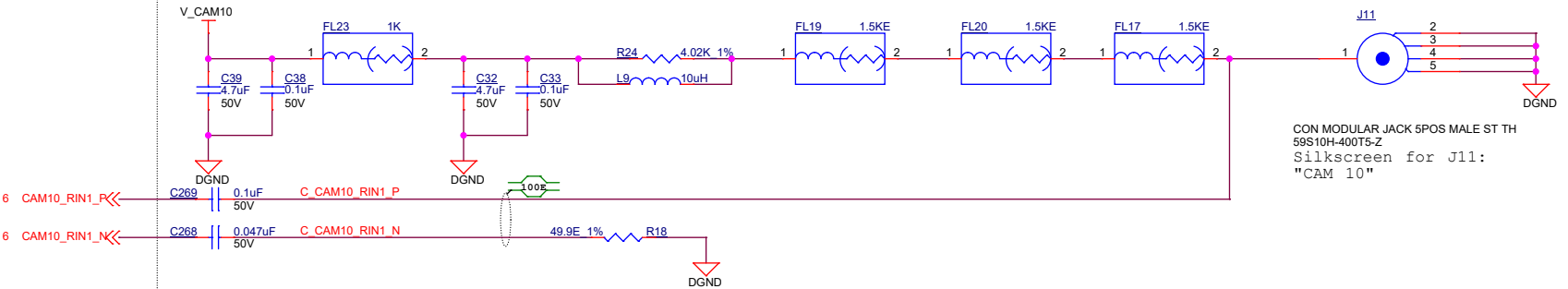


FPD Link Camera Inputs 9-12

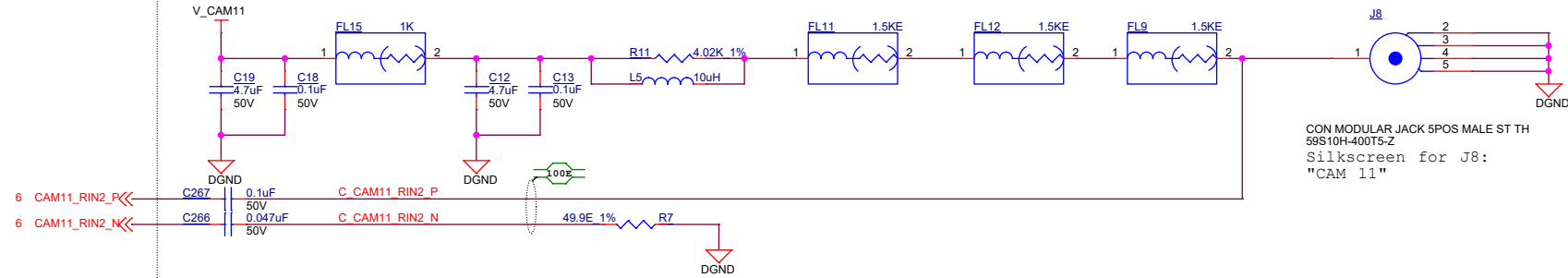
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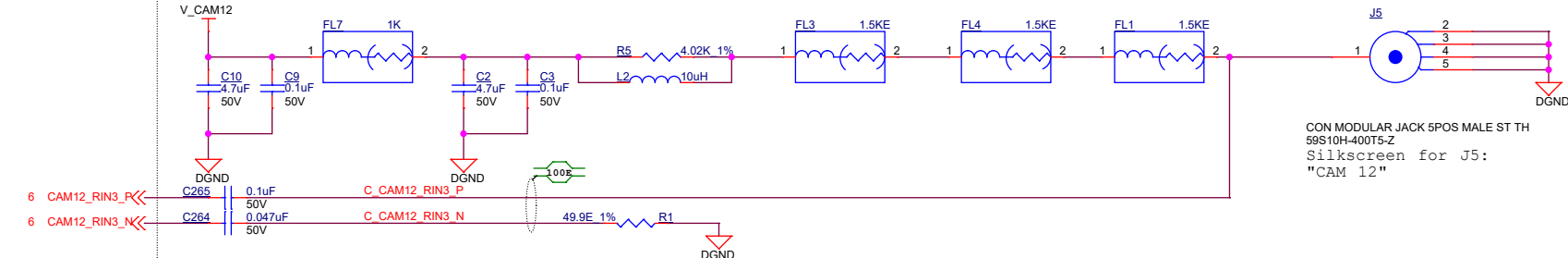
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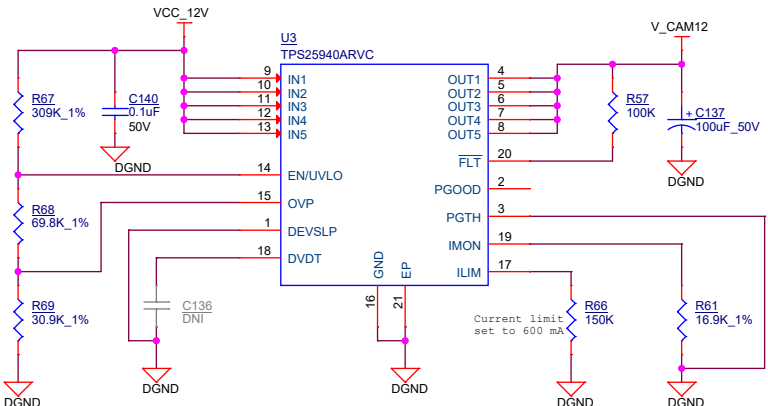
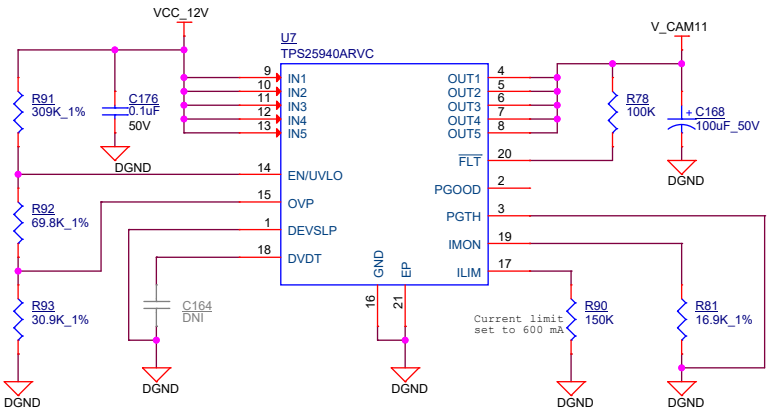
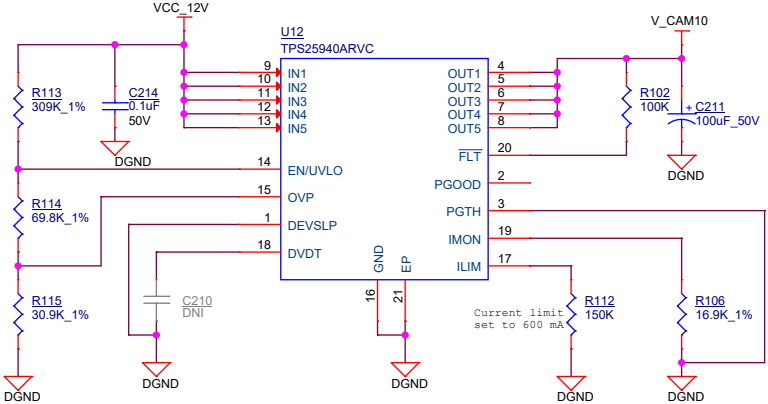
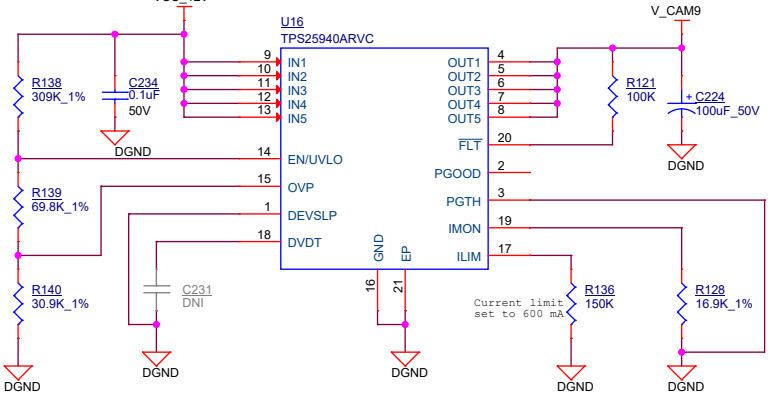
Power Over Coax



Power Over Coax

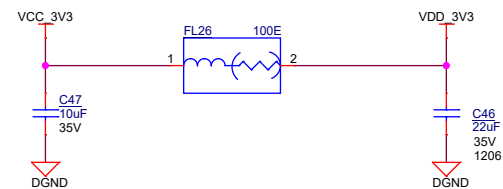
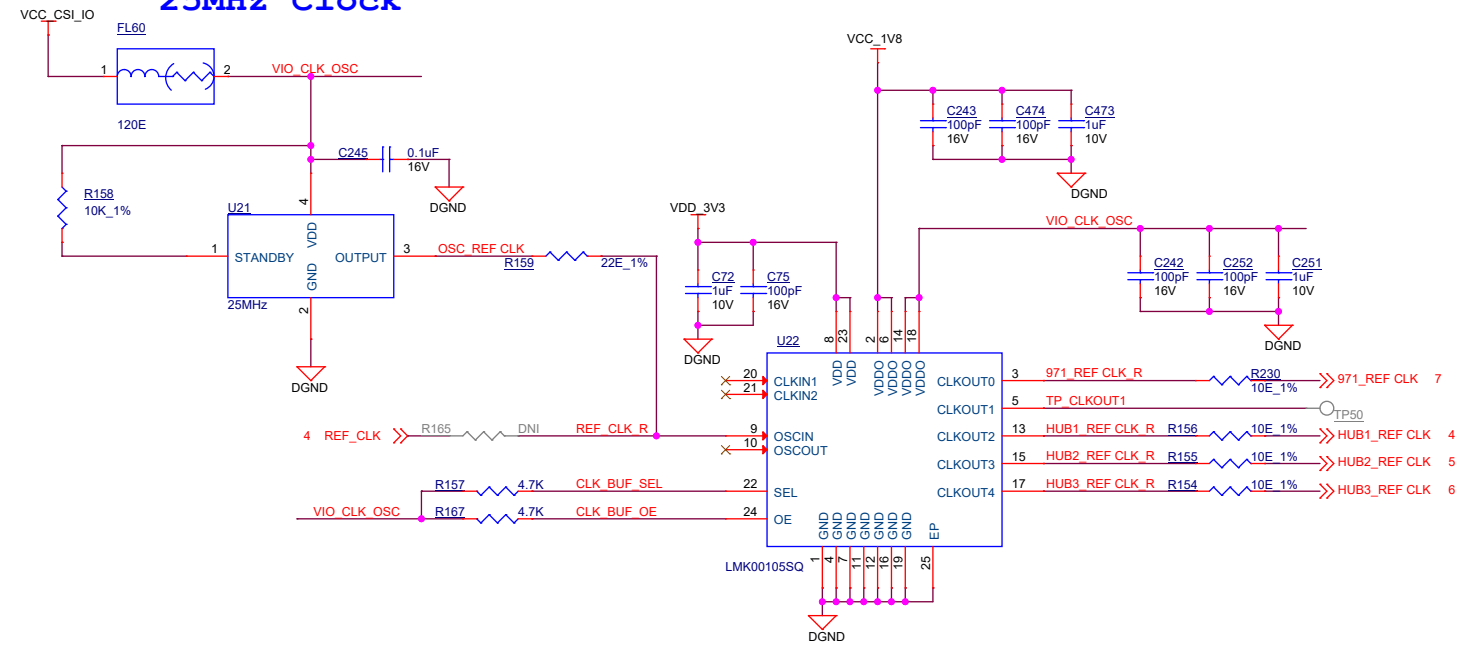


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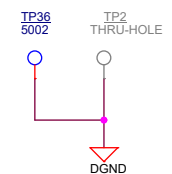


Clock Buffer

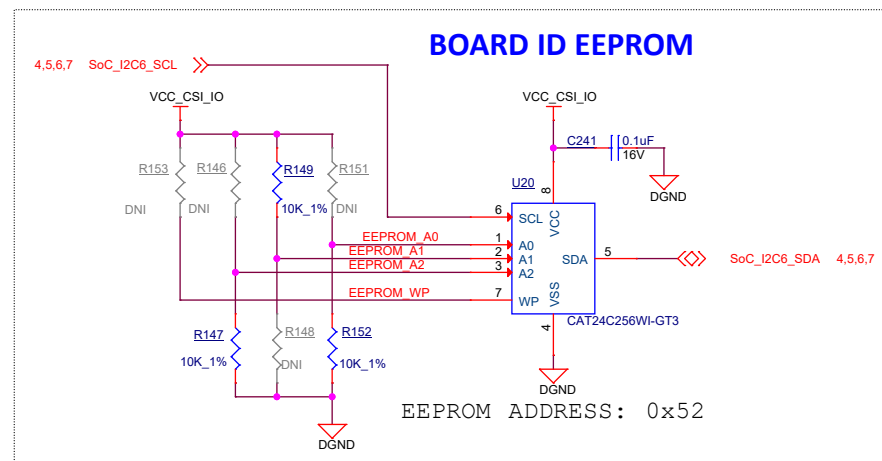
25MHz Clock



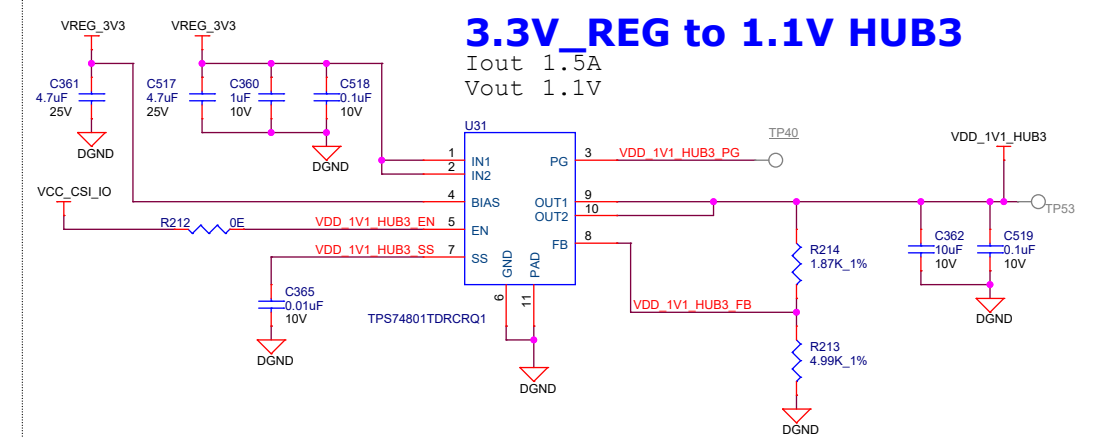
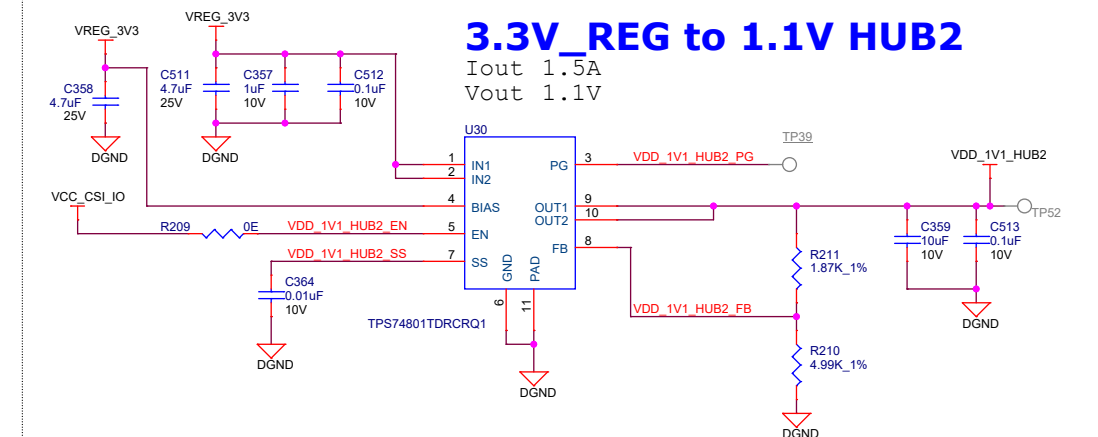
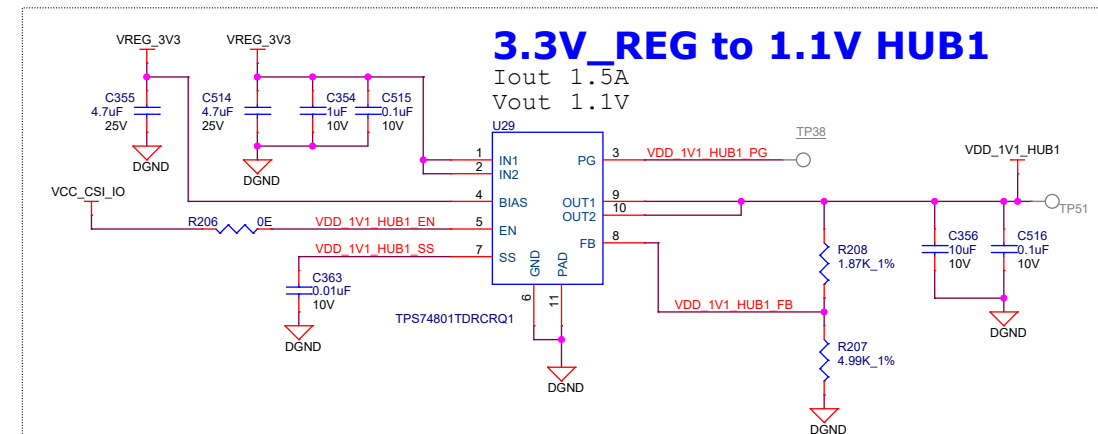
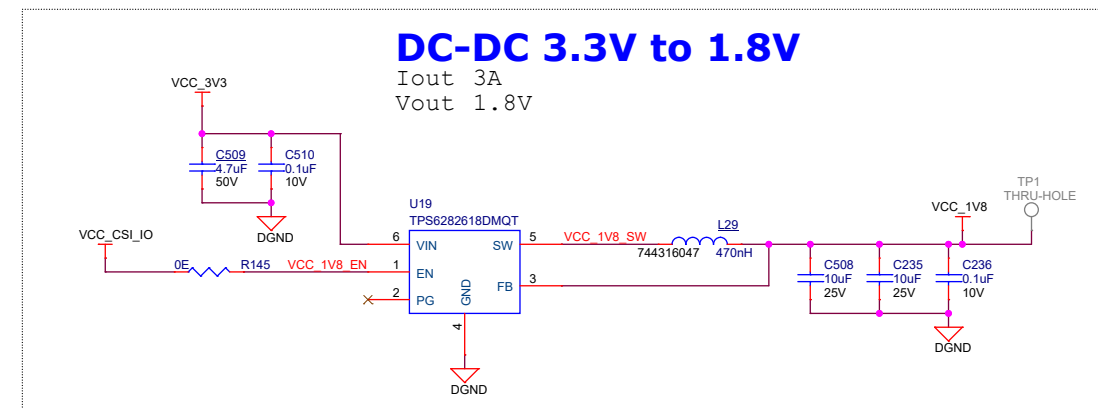
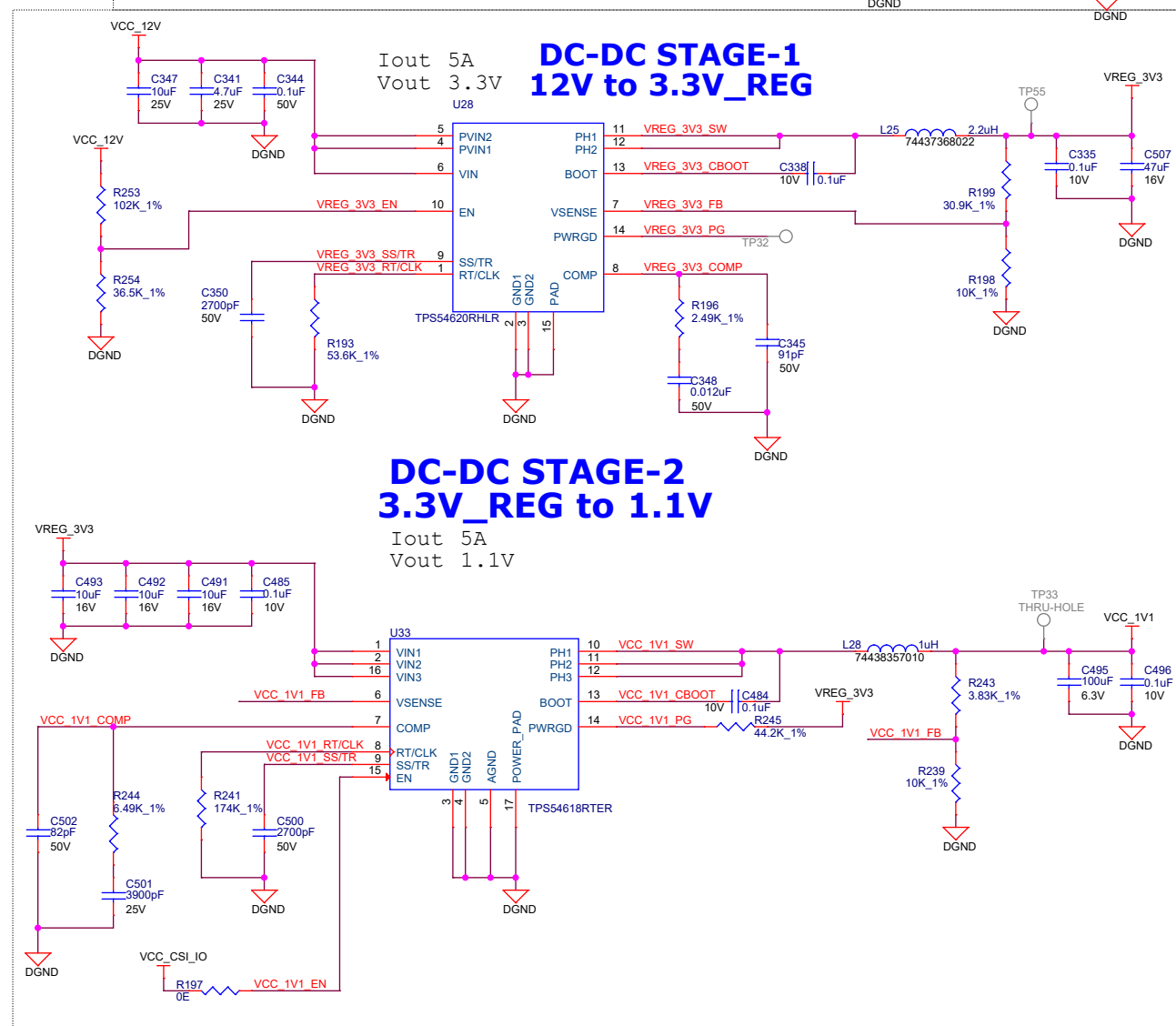
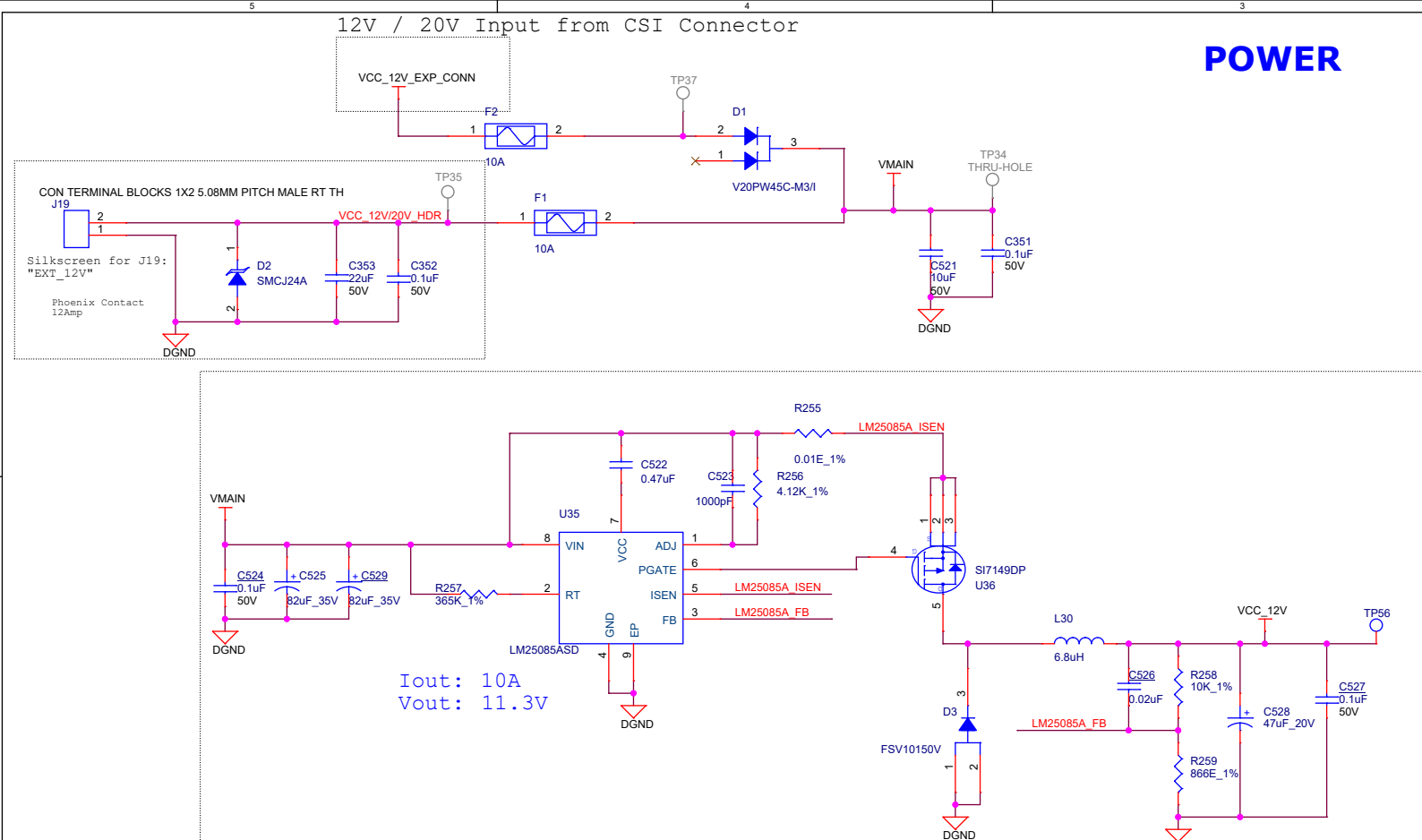
GROUND TEST POINTS



BOARD ID EEPROM



POWER

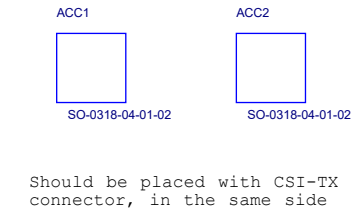


HARDWARE SCHEMATICS

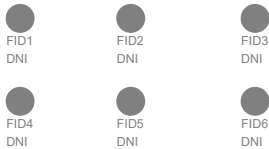
ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

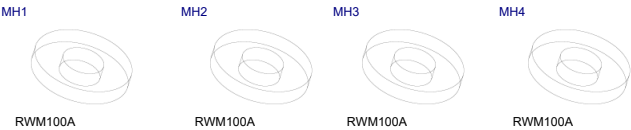
SUPPORT FOR CSI-TX CABLE



FIDUCIALS



WASHERS



LABELS

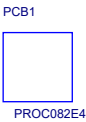
Board Serial No.



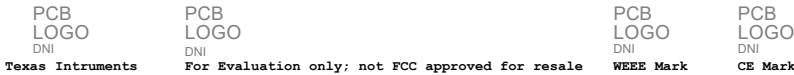
Assembly Revision.



BARE PCB



LOGOs



Project :

J7 EVM



Title
HARDWARE SCHEMATICS

Size
C PROC082 001 J7EXPA01EVM

Date: Thursday, September 19, 2024

Sheet 16 of 16

Rev

E4