

AM62P STARTER KIT EVM

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BOARD REVISION	E2
SCHEMATIC VERSION	3.5

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D-Note:

SK/EVM is a device evaluation board or platform. The SK/EVM is not a reference design. In some cases the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SOC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata, and TRM when designing their custom board. The information found in the datasheet should always take precedence over the SK/EVM implementation.

R-Note:

- * Verify the DNI components configuration with respect to the SK schematics (Use PDF) after completion of board design before board assembly
- * A standard 5% tolerance resistor can be used for most of the series and parallel pull resistor
- * Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build.(Refer FAQs listed for additional details)

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REVISION HISTORY

	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	0.01	20 FEB 2023	Initial Draft derived from AM62A SK - PROC135E3 schematics	Mistral Design Team	Nishant	
	0.02	23 FEB 2023	Updated power section & PMIC part as per PDN	Mistral Design Team	Nishant	
	0.03	24 FEB 2023	1. Added pullups on XDS110 side for Test Automation signals 2. Added 5V0 sourcing caps to meet USB Specifications	Mistral Design Team	Nishant	
	0.04	27 FEB 2023	Replaced parts : LPDDR4 (8 GB), eMMC (32 GB with H5400 support), OSPI (512 Mb NOR Flash)	Mistral Design Team	Nishant	
	0.06	01 MAR 2023	Replaced parts : LPDDR4 (8 GB), eMMC (32 GB with H5400 support), OSPI (512 Mb NOR Flash) Added DSI, OLDI, GPMC (x8) connectors & updated respective net connections	Mistral Design Team	Nishant	
	0.07	03 MAR 2023	Updated PMIC local caps, GPIO connections & assembly variants	Mistral Design Team	Nishant	
	0.08	08 MAR 2023	1. Updated INA section to include INA228 as default with footprint support for INA231 2. INA Kelvin sense resistors moved to PMIC sheet as per modular design requirement	Mistral Design Team	Nishant	
	0.09	15 MAR 2023	1. Updated TI review comments 2. Updated PMIC connections as per PDN v1.5	Mistral Design Team	Nishant	
	0.10	16 MAR 2023	Added separate dual LDO for VDDSHV_SDIO, 5V0 headers for OLDI & DSI daughter cards	Mistral Design Team	Nishant	
	0.11	20 MAR 2023	1. Updated PMIC Enable & GPIO connections 2. Modified RC shield connections for RGMII1, RGMII2 & USB Type A connectors	Mistral Design Team	Nishant	
	0.12	22 MAR 2023	1. Updated TI review comments on PD Controller 2. Replaced HDMI EXT_SWING resistor with 7.5K_5% ohms	Mistral Design Team	Nishant	
	0.13	28 MAR 2023	Added extra local caps to PMIC Switching outputs as recommended in datasheet	Mistral Design Team	Nishant	
	0.14	04 APR 2023	Modified SoC decaps & added RC circuit for I2C	Mistral Design Team	Nishant	
	0.15	07 APR 2023	1. Added series resistors for RGMII TX signals 2. Swapped DDR DQ & DMI bits	Mistral Design Team	Nishant	
	0.16	18 APR 2023	1. Updated Internal and review comments from TI 2. Replaced Oscillator with new LMK6CE series (BAW), OLDI and DSI Connector.	Mistral Design Team	Nishant	Ajit MB
	0.18	03 MAY 2023	Modified the 3T decaps as 4 pin IC's and updated a few review comments from TI	Mistral Design Team	Nishant	
	0.19	10 MAY 2023	Modified the 2T current sense resistor parts to 4T sense similar to AM62A SK	Mistral Design Team	Nishant	
	0.20	16 MAY 2023	1. Replaced USB Type A load switch (with OC) & ESD protection device 2. Added capacitor to CT pin of VCC_3V3_SYS & VDD_MMC1 load switches	Mistral Design Team	Nishant	Ajit MB
	0.21	24 MAY 2023	1. VMON connection modified for PMIC to meet threshold of 3.3V 2. Part References Back annotated from PCB file	Mistral Design Team	Nishant	
	0.23	21 AUG 2023	1. Corrected power architecture & sequencing diagrams 2. Baselined	Mistral Design Team	Nishant	Ajit MB
E1-1	1.1	03 OCT 2023	1. Modified WD_DISABLE pull to VCC_3V3_MAIN 2. Modified PMIC_RSTOUT pull to VCC_3V3_SYS 3. Changed Assembly instruction for R280 to Mount 4. Changed the PMIC VSENSE voltage from VMAIN to VBUS_TYPEC1 and VBUS_TYPEC2 (dual input) and implemented ORing diode.	Mistral Design Team	Nishant	Ajit MB
	1.2	05 OCT 2023	Few circuits marked DNI as captured in change list document	Mistral Design Team	Nishant	Ajit MB
	1.3	07 NOV 2023	Changed R91 and R127 to 3.48k_1%	Mistral Design Team	Nishant	Ajit MB
	2.0	21 NOV 2023	Baselined	Mistral Design Team	Nishant	Ajit MB
E1-2	2.1	21 MAR 2024	1. Implemented the modular approach 2. R114, R116 value has been changed from 0E to 100E 3. C572 has been added.	Mistral Design Team	Pandiyarajan	Ajit MB
	2.2	21 MAY 2024	1. Implemented the review comments shared by TI 2. Updated R528 from 10K to 47K 3. Load switch(U134) and its corresponding components were added for the 15W source power sensing implementation 4. SoC_I2C0_SCL, SoC_I2C0_SDA and PD_I2C1_IRQ were swapped from I2C2 port of the PD controller (U103) to I2C1 port	Mistral Design Team	Pandiyarajan	Ajit MB
	2.3	05 JUN 2024	1. Enabled Voltage ratings for all the capacitors and added Design notes 2. R133, R643 - 0E changed to 22E; 3. C273 - 4.7uF changed to 1uF; C276 - 1uF changed to 4.7uF; C178, C180 - 1uF changed to 0.1uF; C40, C43 - 12pF changed to 18pF 4. R652, R653 (22E) added to EXP_SPI0_CLK, SOC_SPI2_CLK respectively	Mistral Design Team	Pandiyarajan	Ajit MB
	2.4	12 JUN 2024	1. Oscillator(U7) and clock buffer(U8) has been powered up from VDDA_1V8 to VDDA1V8 2. R169 has been made as DNI; R59 changed from 51k_1% to 51.7k_1% 3. R39 and C12 removed 4. R654, C577 added to PMIC_INT 5. R655 added to MCASP1_ACLKX	Mistral Design Team	Pandiyarajan	Ajit MB
	2.5	12 NOV 2024	1.C578 decap has been added the VDD_MMC0 pin 2.FL10 has been removed and VDD_MMC0 is directly shorted with VDDR_CORE	Mistral Design Team	Pandiyarajan	Ajit MB

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E2	3.1	03 DEC 2024	FL7 has been removed and VDDA_DLL_MMC0 has been shorted with VDDR_CORE	Mistral Design Team	Pandiyarajan	
	3.2	23 DEC 2024	C579, C580 decaps added to SOC_DVDD1V8 rail	Mistral Design Team	Pandiyarajan	
	3.3	17 FEB 2025	C578 removed; C566, C269 and C46 have been DNI'd	Mistral Design Team	Pandiyarajan	
	3.4	10 APR 2025	Updated PMIC part number	Mistral Design Team	Pandiyarajan	
	3.5	30 OCT 2025	Updated SoC part number	Mistral Design Team	Pandiyarajan	

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KEY LINKS TO COLLATERALS

Hardware Design Guide : https://www.ti.com/lit/an/sprada9/sprada9.pdf
Schematic Design and Review Checklist : https://www.ti.com/lit/an/sprad21d/sprad21d.pdf
DDR Board Design and Layout Guidelines : https://www.ti.com/lit/an/sprad66a/sprad66a.pdf
SKs (Starter Kits) for reference : SK-AM62B, SK-AM62B-P1, SK-AM62-LP, SK-AM62-SIP, SK-AM62A-LP, SK-AM62P-LP

LINKS TO KEY FAQs

(10) [FAQ] AM62P / AM62P-Q1 Custom board hardware design - Collaterals to Get started - Processors forum - Processors - TI E2E support forums
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am62x-am62ax-am62px-custom-board-hardware-design--collaterals-for-reference-during-schematic-design-and-schematics-review
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1340906/faq-am62p-am62p-q1---custom-board-hardware-design---Design-and-review-notes-for-reuse-of-sk-am62p-lp-schematics
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1306030/faq-am62p-am62p-q1-custom-board-hardware-design--faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit

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Title LINKS TO KEY COLLATERALS AND FAQs

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BLOCK DIAGRAM - AM62P SKEVM

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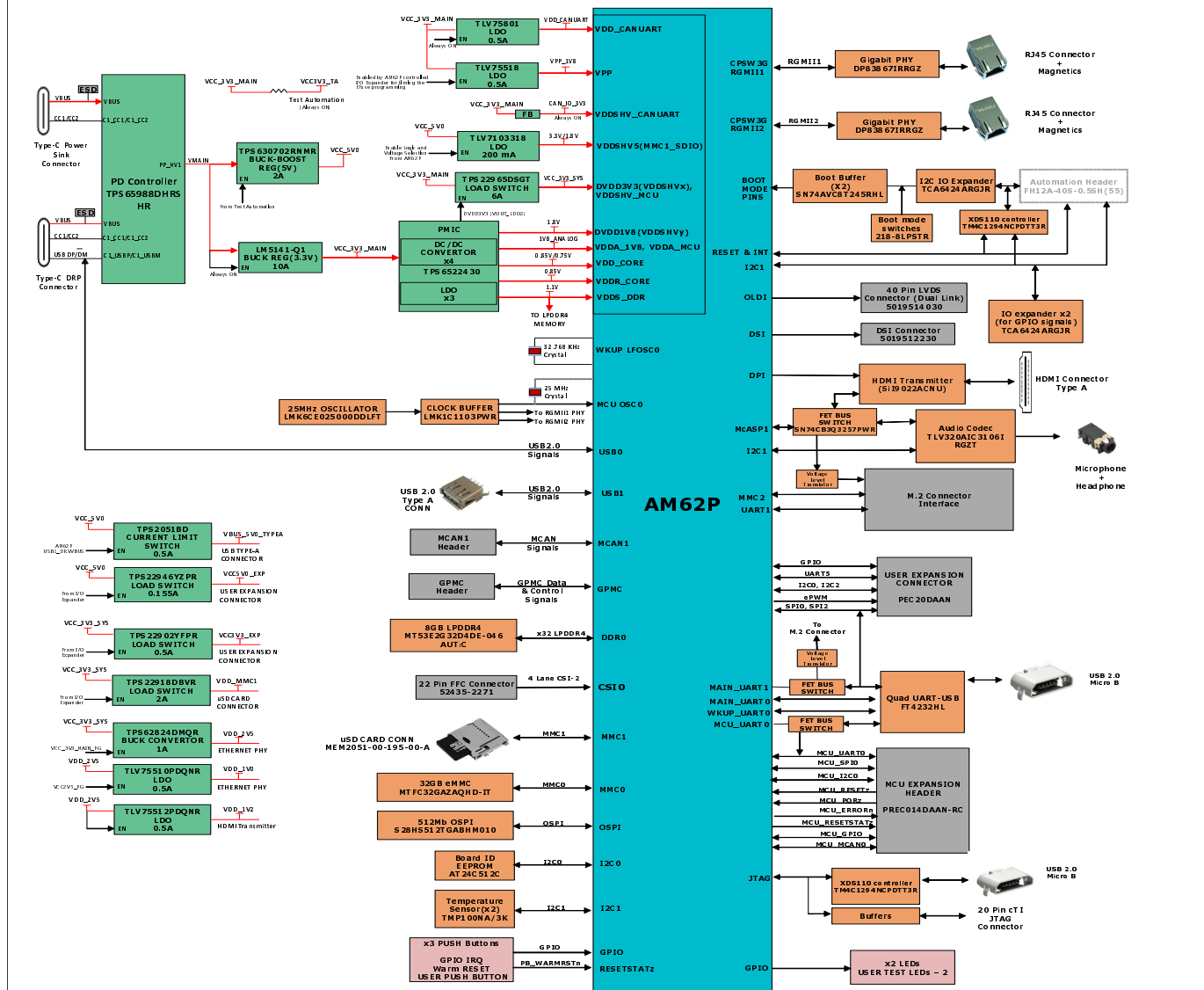
1. Pins AA25 and B25 (OBSCCLK) of the SoC are Main Domain Observation Clock outputs for testing and debugging purposes only.
Add a TP near to the SoC and a provision to isolate the signal for testing whenever possible.
2. Pin E10 (MCU_OBSCLK) of the SOC is MCU Domain Observation Clock output for testing and debugging purposes only.
Add a TP near to the SoC and provision to isolate the signal for testing whenever possible.

D-Note:

Drive strength configuration is currently not supported. The drive strength must remain in the default state since this is the only condition used during timing closure of the peripherals. The devices are set to maximum drive strength. Please refer to the IBIS model to find the drive strength of the I/Os.

D-Note:

Refer Device Comparison section of the processor data sheet for supported cores, peripherals and memory size.



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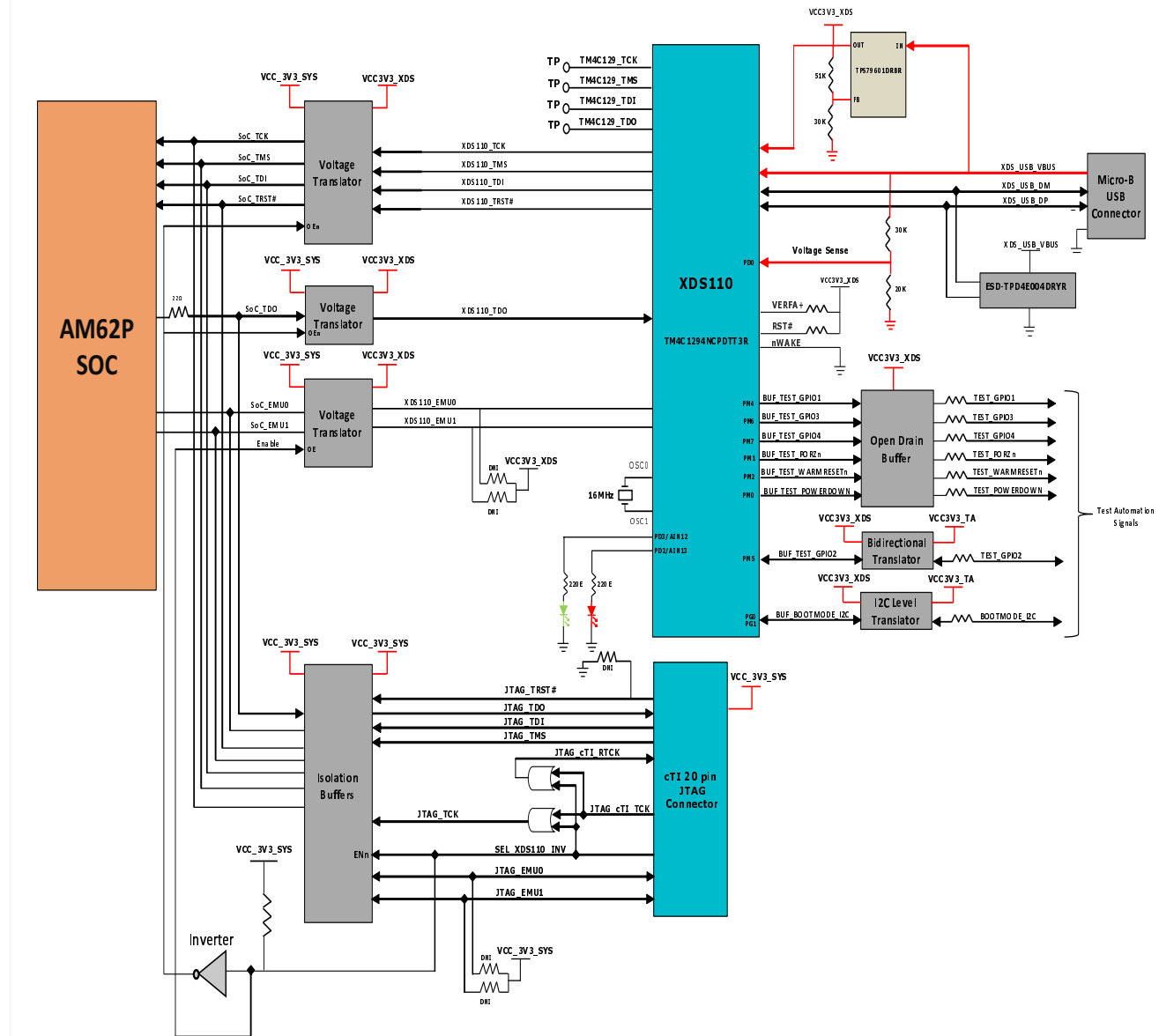
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BLOCK DIAGRAM - XDS110 DEBUGGER



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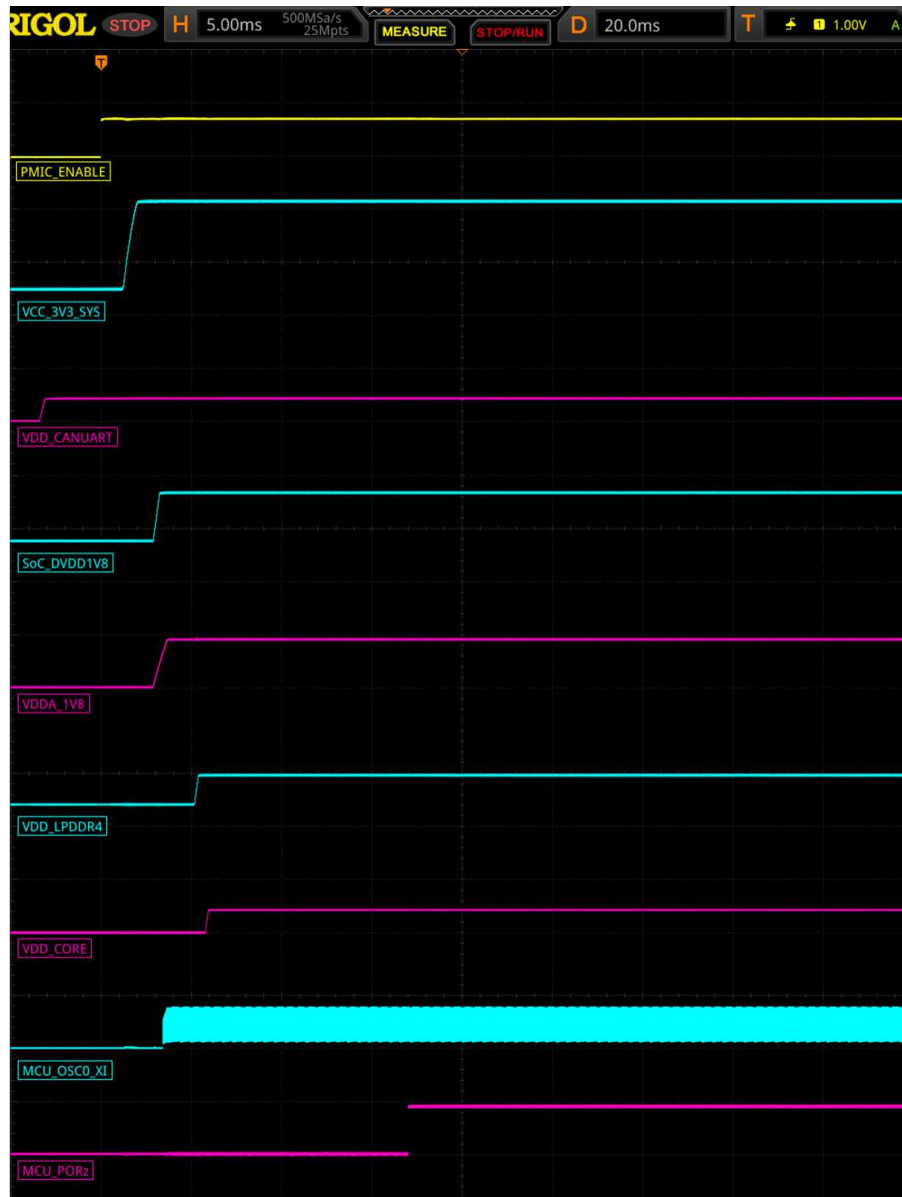
Title BLOCK DIAGRAM_XDS110

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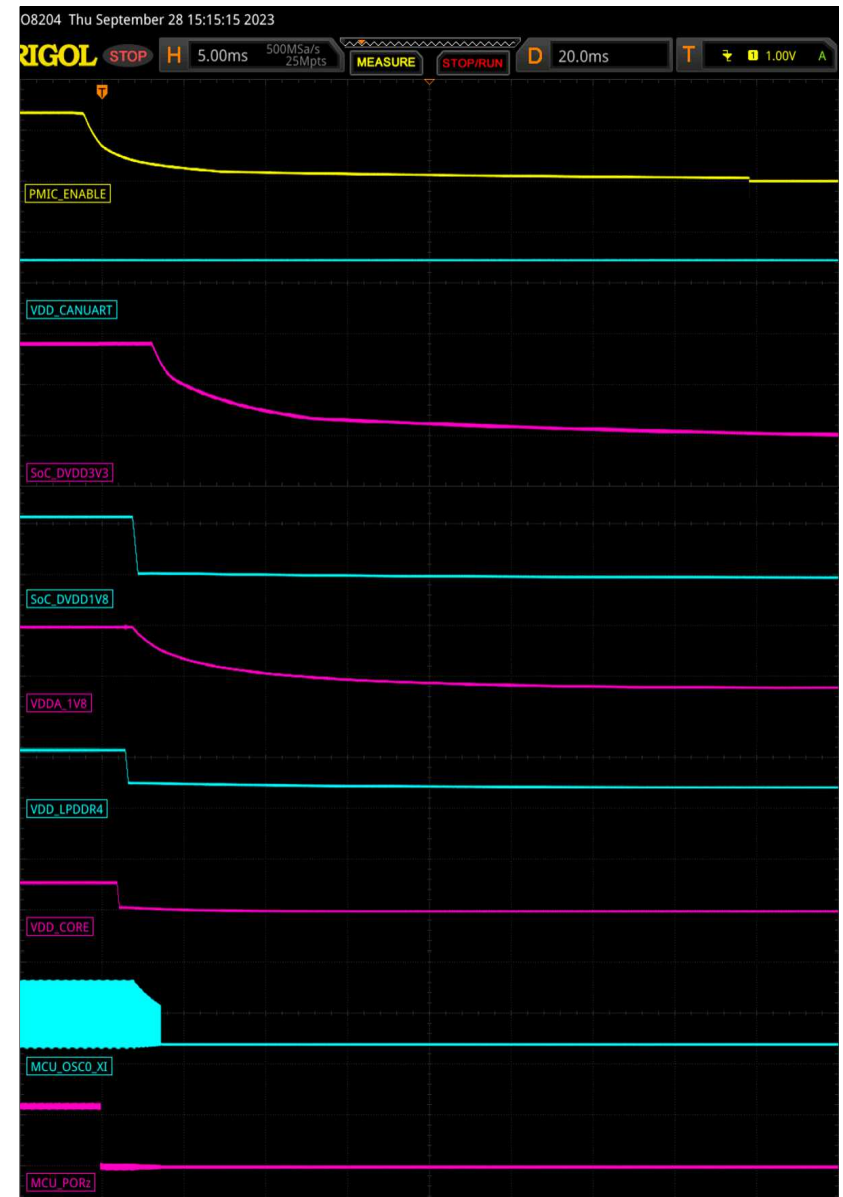
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POWER ARCHITECTURE BLOCK DIAGRAM

POWER UP SEQUENCE



POWER DOWN SEQUENCE

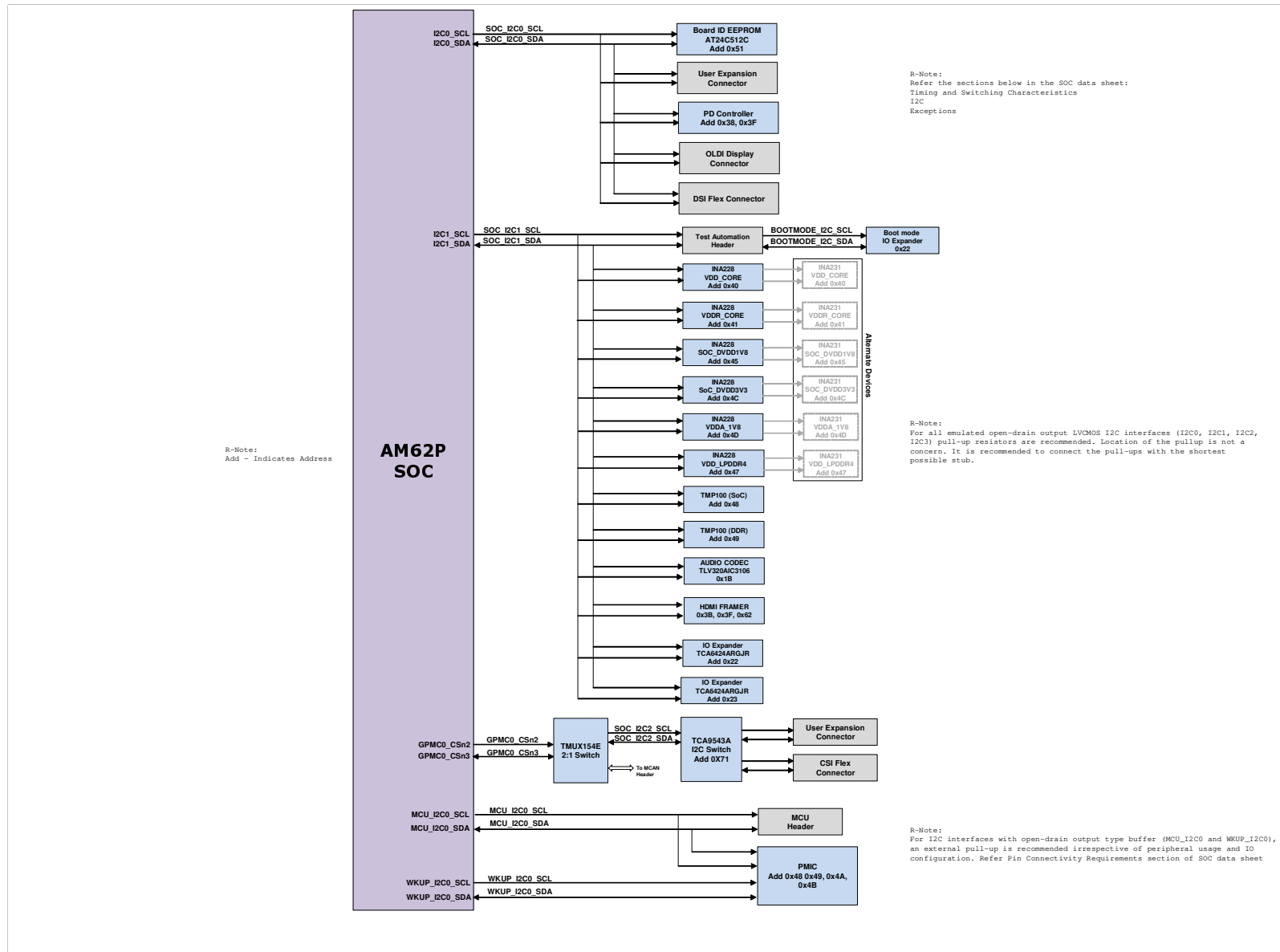


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I2C TREE



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GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE RAIL CONNECTED ON KEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SD_CD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_VDD01V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_VDD01V8
3	MCU Interrupt	MCU_INTn	INTERRUPT	MCU_GPIO0_0	MCU_SPIO_CS0	INPUT	HIGH	LOW	VDDSHV_MCU	SoC_VDD03V3
4	CP5W Ethernet PHY Interrupt	CP5W_ETH_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_VDD01V3
5	OSPI Reset Control GPIO	GPIO0_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn2	OUTPUT	HIGH	LOW	VDDSHV1	SoC_VDD01V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_VDD01V8
7	MCU Header GPIO0_16	MCU_GPIO0_16	GPIO	MCU_GPIO0_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CAN UA RT	CAN_IO_3V3
8	MCU Header GPIO0_15	MCU_GPIO0_15	GPIO	MCU_GPIO0_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CAN UA RT	CAN_IO_3V3
9	PMC Interrupt	PMC_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_VDD03V3
10	CAN-FD fast wake up signal from switch	CAN_FD_WKUP_SW_INH	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CAN UA RT	CAN_IO_3V3
11	CAN-FD fast wake up signal from MCU header	CAN_FD_WKUP_HDR_INH								
12	User test LED control signal	SOC_GPIO1_49	ENABLE	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_VDD03V3
13	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	GPIO1_23	UART0_RTSn	INPUT	HIGH	LOW	VDDSHV0	SoC_VDD01V3
14	User Interrupt									
15	Low power mode enable	PMC_LPM_EN0	ENABLE	MCU_GPIO0_22	PMC_LPM_EN0	OUTPUT	HIGH	LOW	VDDSHV_CAN UA RT	CAN_IO_3V3
16	SD Card I/O Voltage Selection	VSEL_SD_SOC	SELECTION	GPIO0_31	GPIO0_CLK	OUTPUT	NA	NA	VDDSHV3	SoC_VDD03V3
IO EXPANDER – 01										
1	Interrupt from DLDI display	OLDI_INT#	INTERRUPT	IO EXPANDER-P00		INPUT	HIGH	LOW		VCC_3V3_SYS
2	x8 NAND Card Presence Detect	x8_NAND_DETECT	DETECTION	IO EXPANDER-P01		INPUT	HIGH	LOW		VCC_3V3_SYS
3	UART1 FET selection control	UART1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P02		OUTPUT	HIGH	-		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
5	SOC eFuse Voltage (VP=1.8V) Regulator Enable	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	NA	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	SOC UART1 Mux Select	UART1_FET_BUF_EN	ENABLE	IO EXPANDER-P06		OUTPUT	HIGH	LOW		VCC_3V3_SYS
8	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
9	DSI Display GPIO0	DSI_GPIO0	GPIO	IO EXPANDER-P10		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
10	DSI Display GPIO1	DSI_GPIO1	GPIO	IO EXPANDER-P11		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
11	OLDI to HDMI Card Device ID interrupt	OLDI_EDID	INTERRUPT	IO EXPANDER-P12		INPUT	HIGH	LOW		VCC_3V3_SYS
12	BT UART WKUP Signal	BT_UART_WAKE_SOC_3V3	INTERRUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	USB Type A overcurrent indicator	USB_TYPEA_OC_INDICATION	INTERRUPT	IO EXPANDER-P14		INPUT	HIGH	LOW		VCC_3V3_SYS
14	Raspberry Pi Camera CS0 GPIO1	CS1_GPIO0	INPUT/OUTPUT	IO EXPANDER-P15		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
15	Raspberry Pi Camera CS0 GPIO2	CS1_GPIO1	INPUT/OUTPUT	IO EXPANDER-P16		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
16	WLAN Alert Interrupt	WLAN_ALERTn	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO1 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC_3V3_SYS
19	MCASP1 Enable and Direction Control	MCASP1_FET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
20		MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
21		MCASP1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	-		VCC_3V3_SYS
22	DSI to HDMI Card Device ID interrupt	DSI_EDID	INTERRUPT	IO EXPANDER-P25		INPUT	HIGH	LOW		VCC_3V3_SYS
23	Power Delivery I2C Interrupt Request	PD_IDC_IRQ	INTERRUPT	IO EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_SYS
24	User Test LED 2	IO_EXP2_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER – 02										
1	M2 module Bluetooth LDO Enable	BT_EN_SOC	ENABLE	IO EXPANDER-P00		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
2	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P01		OUTPUT	LOW	HIGH		VCC_3V3_SYS
3	M2 Interface Level Translator Enable	WL1T_EN	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
4	SoC I2C2 & MCAN MUX Selection	SoC_I2C2_MCAN_SEL	CONTROL	IO EXPANDER-P20		OUTPUT	HIGH	-		VCC_3V3_SYS
5	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER-P21		OUTPUT	HIGH	LOW		VCC_3V3_SYS
6	CP5W Ethernet PHY-1 Reset Control GPIO	GPIO_CP5W1_RST	RESET	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS
7	CP5W Ethernet PHY-2 Reset Control GPIO	GPIO_CP5W2_RST	RESET	IO EXPANDER-P23		OUTPUT	HIGH	LOW		VCC_3V3_SYS
8	DLDI display Reset control GPIO	GPIO_OLDI_RSTn	RESET	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC_3V3_SYS
10	eMMC Reset control GPIO	GPIO_eMMC_RSTn	RESET	IO EXPANDER-P26		OUTPUT	HIGH	LOW		VCC_3V3_SYS
11	WLAN Reset control GPIO	SOC_WLAN_S0IO_RST	RESET	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS

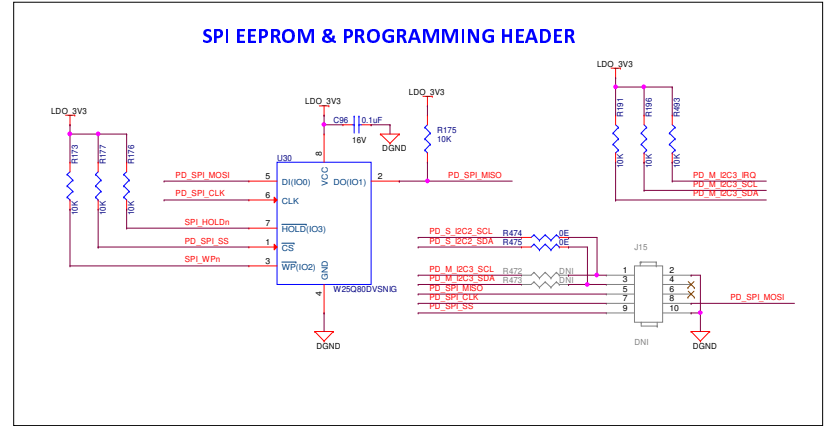
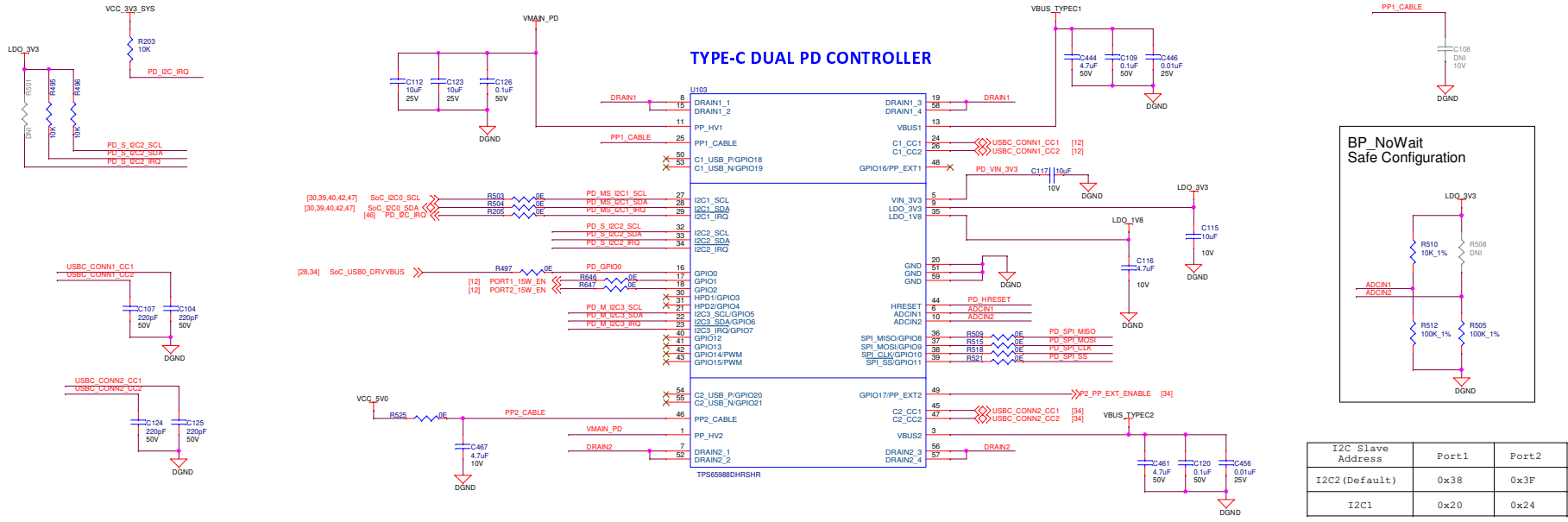
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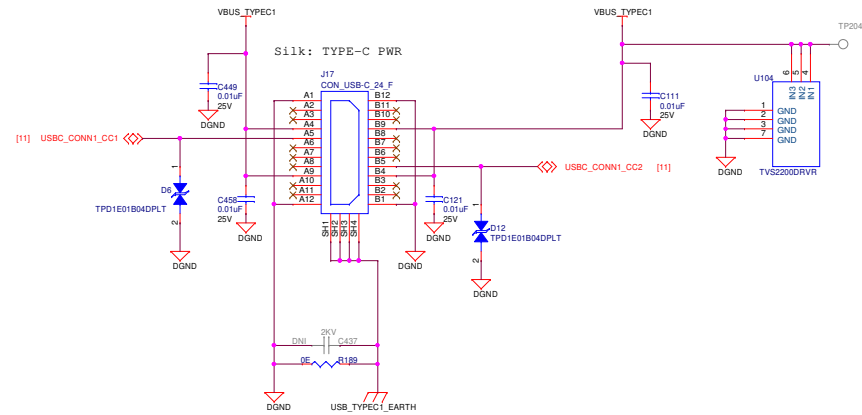
Title GPIO MAPPING TABLE

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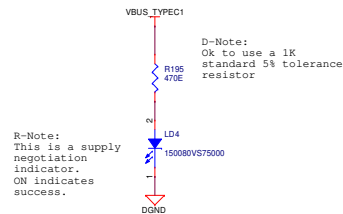
USB TYPE-C PD CONTROLLER AND POWER SUPPLY



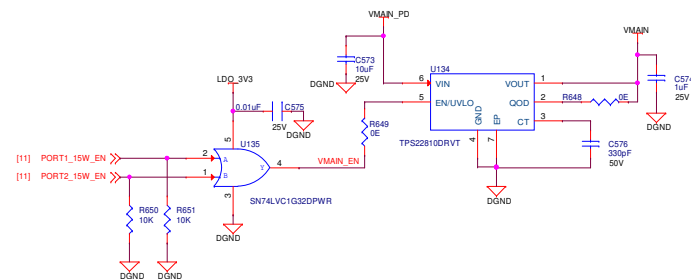
USB TYPE-C POWER CONNECTOR



POWER INDICATION LED: VBUS_TYPEC1



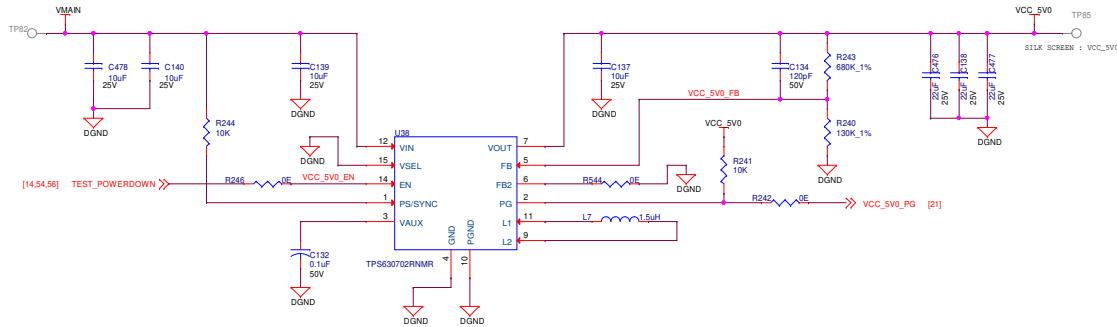
LOAD SWITCH FOR VMAIN



PRE REGULATOR POWER SUPPLY-1

VinMin = 4.5V
VinMax = 15V
Vout = 5V @ 2A

D-Note:
Add a Jumper or 0 R for isolation or current measurement
for pre-production board.



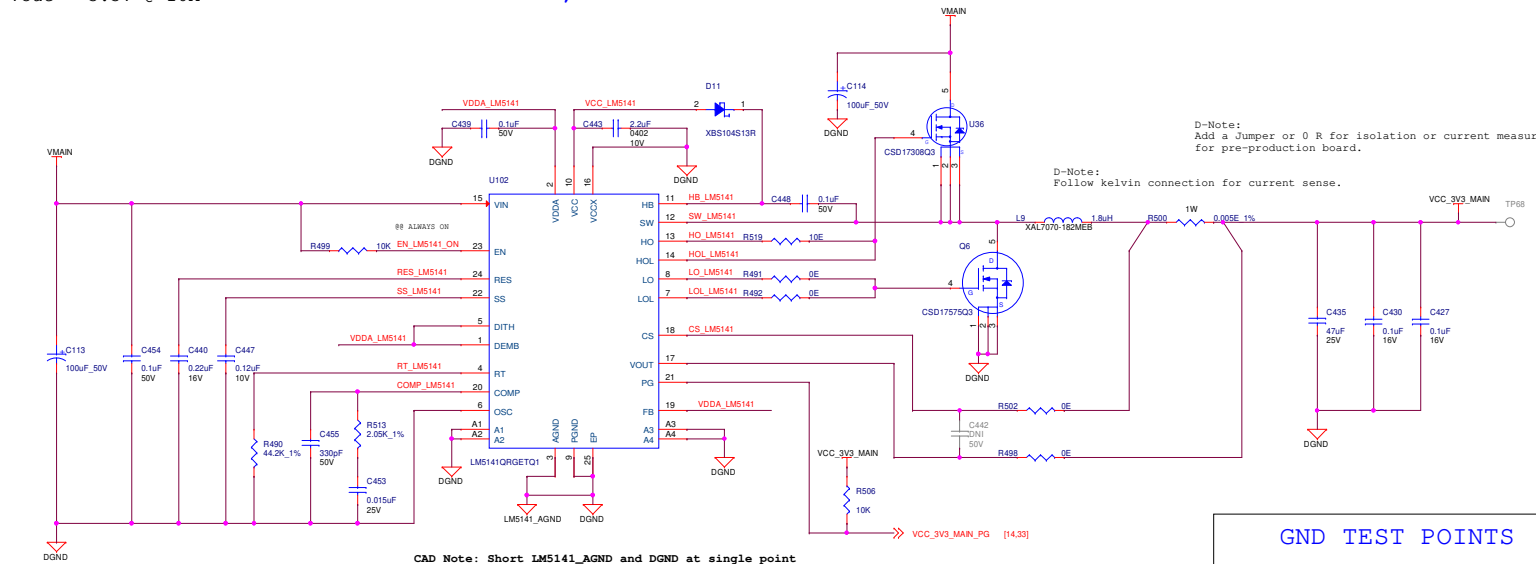
PRE REGULATOR POWER SUPPLY-2

3.3V, 10.0 AMPS SUPPLY

VinMin = 4.5V
VinMax = 15V
Vout = 3.3V @ 10A

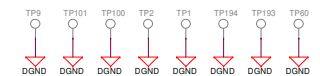
D-Note:
Add a Jumper or 0 R for isolation or current measurement
for pre-production board.

D-Note:
Follow kelvin connection for current sense.



CAD Note: Short LM5141_AGND and DGND at single point

GND TEST POINTS



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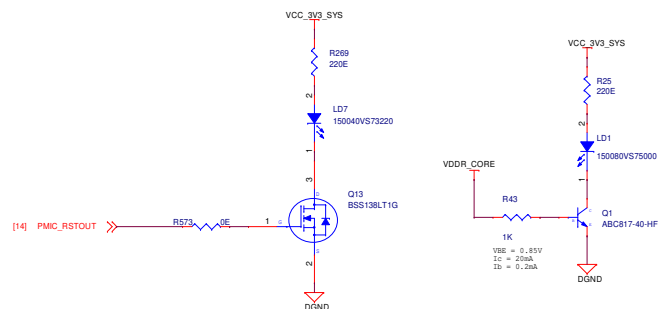


Title PRE-REGULATOR POWER SUPPLY

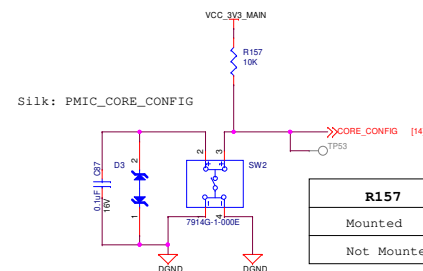
Size	Rev
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PMIC POWER INDICATION LED



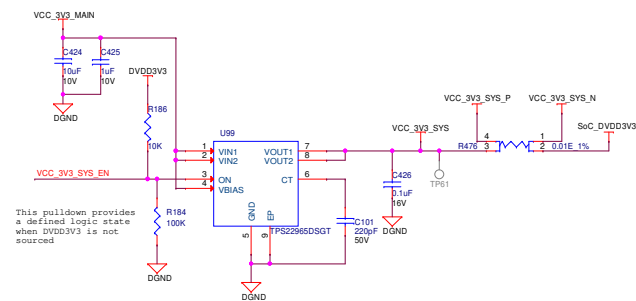
PMIC PUSH BUTTON LOGIC



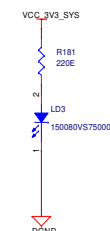
R157	VDD_CORE VOLTAGE
Mounted	0.85 V (DEFAULT)
Not Mounted	0.75 V

Note: When R157 is DNI, Push Button (SW2) becomes operational through internal pullup on PMIC GPIO3

VCC_3V3_SYS LOAD SWITCH

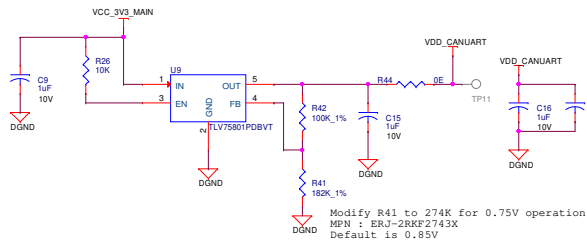


POWER RAIL LED

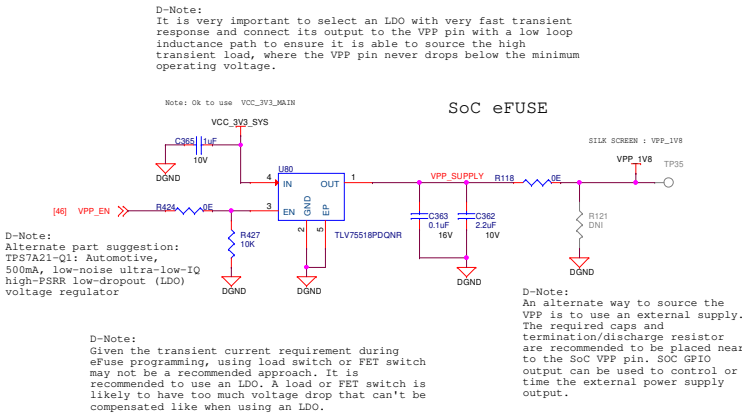


SOC POWER SUPPLIES - LDOs

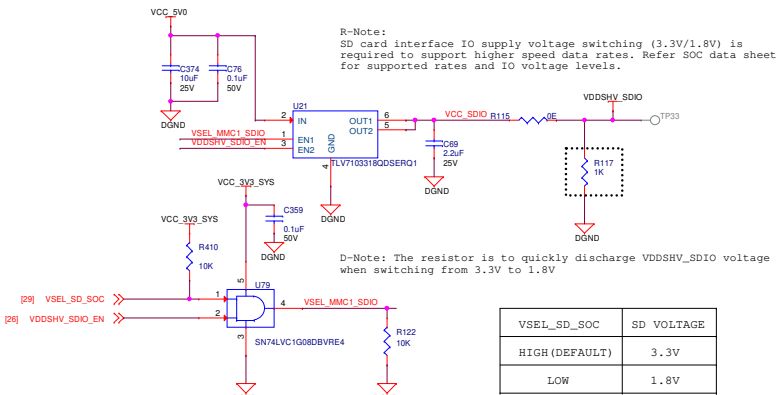
CANUART SUPPLY



1.8V VPP (eFUSE), 0.5AMPS SUPPLY



3.3V/1.8V SD CARD IO SUPPLY



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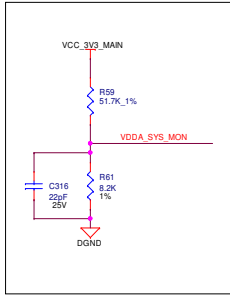


Title SOC POWER SUPPLIES - LDOs FOR CANUART, VPP AND SD CARD IO

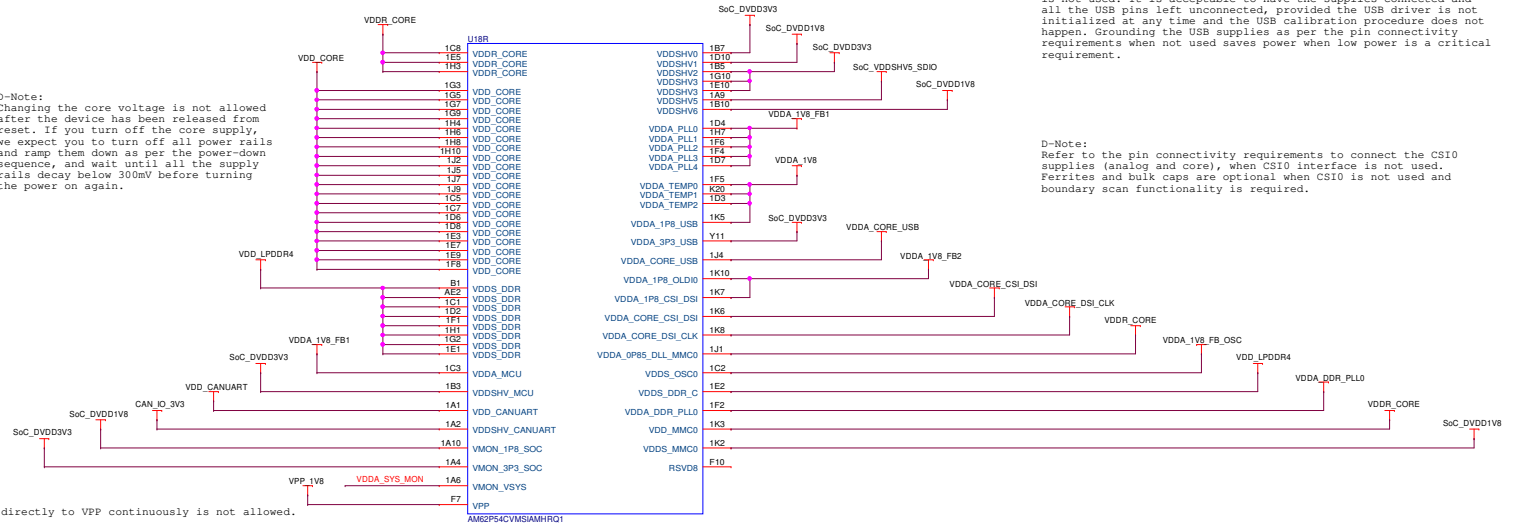
Size	PROC164E2	Rev
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SOC POWER SUPPLIES AND SUPPLY RAILS

D-Note: Recommend implementing the voltage monitoring functionality using VMON_VSYS for early detection of supply failure. It is meant to be a power-fail indicator for the main input (higher) voltage rail that enters the PCB. For example, 5, 12, or 24 volts. The error associated with this monitor would require you to set the threshold significantly lower than the nominal to avoid a false trigger. Refer to System Power Supply Monitor Design Guidelines section of the data sheet.



D-Note: Changing the core voltage is not allowed after the device has been released from reset. If you turn off the core supply, we expect you to turn off all power rails and ramp them down as per the power-down sequence, and wait until all the supply rails decay below 300mV before turning the power on again.



D-Note:
Connecting 1.8V supply source directly to VPP continuously is not allowed.

D-Note:

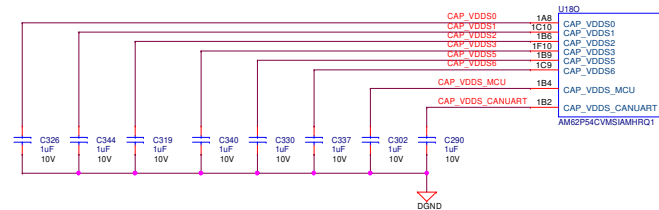
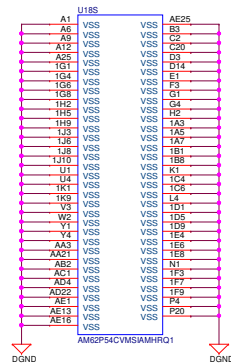
Common SoC LVMCMOS IO Interface Guidelines:

1. Most of the SoC IOs are not fail-safe. No input should be applied before supply ramps.
2. SoC LVMCMOS inputs have minimum slew rate requirements specified.
3. SoC IO buffers are off during Reset. A pull is required near to the attached device being driven by the SoC IOs.

Any SoC IO that has a trace connected and not being actively driven needs a parallel pull. When adding a pull is not feasible, ensure the trace is routed away from noisy signals.

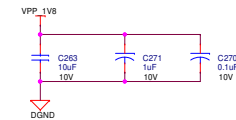
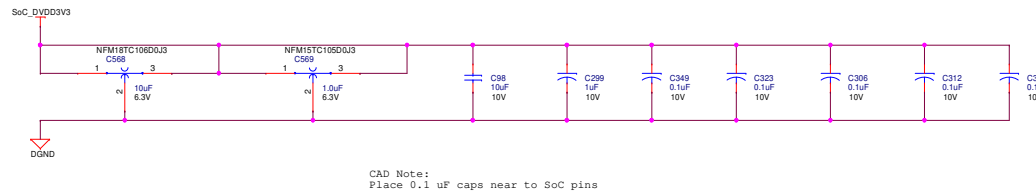
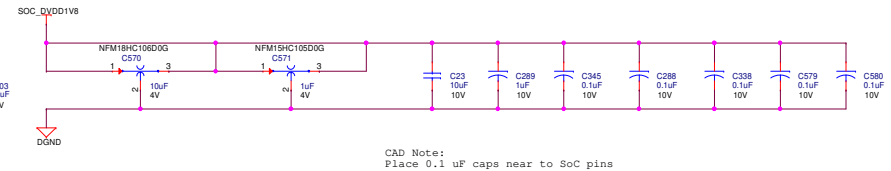
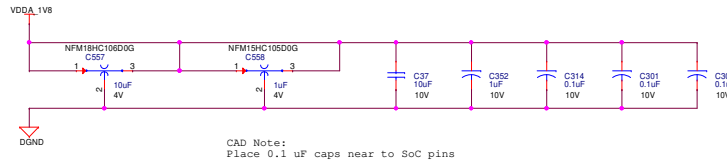
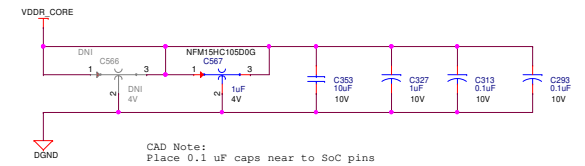
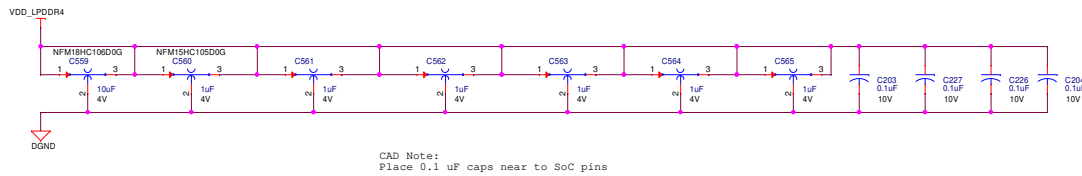
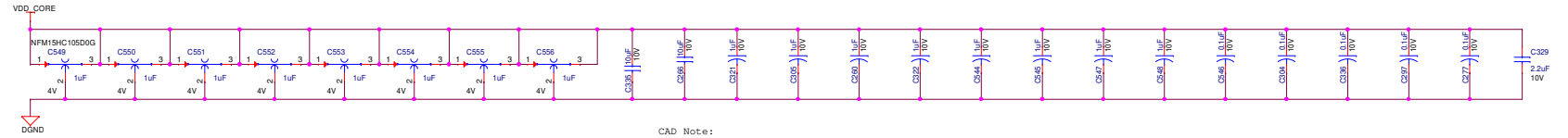
D-Note:
A trace connected to the SoC is effectively an antenna that will pick up noise. A potential will be generated on the signal when noise couples into the antenna. This potential will be largest on the highest impedance end of the signal. By placing a pull-up or pull-down near the SoC pin, we force the highest potential to the open-circuit end of the signal rather than the SoC end of the signal.

SOC VSS



D-Note:
Select capacitors with ESR < 1 ohm. Ensure the PCB loop inductance is < 2.5 nH. Select 0201 package or the smallest possible package. Refer to the SOC data sheet.

SOC POWER SUPPLIES - DECAPS 1



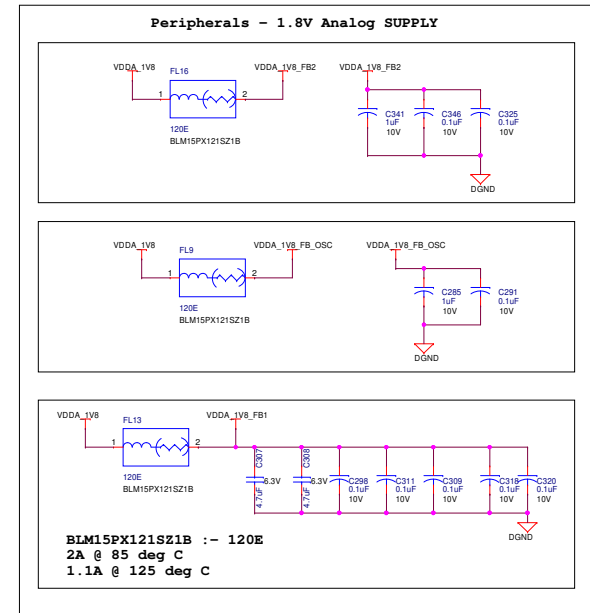
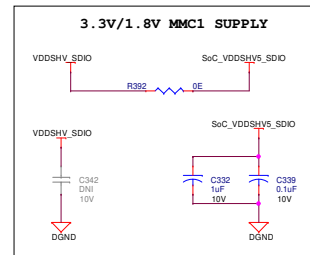
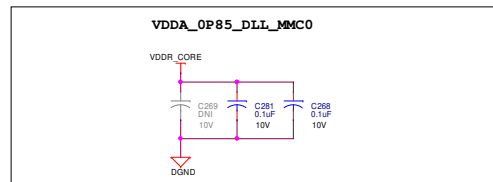
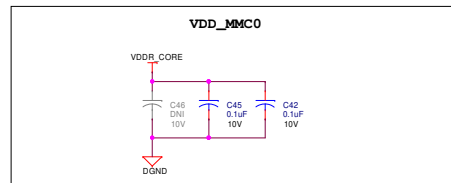
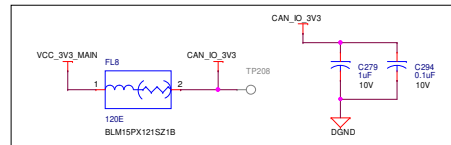
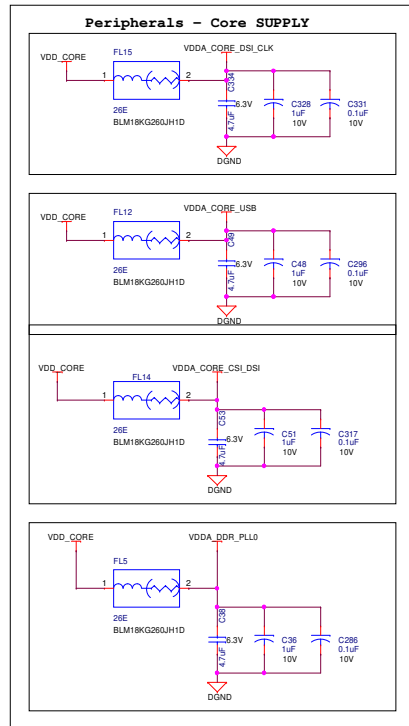
R-Note:
Usage of 3 terminal capacitors optimizes the usage of bulk capacitors and minimizes the PCB inductance.

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Title		
SOC POWER SUPPLIES - DECAPS 1		
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SOC POWER SUPPLIES - DECAPS 2

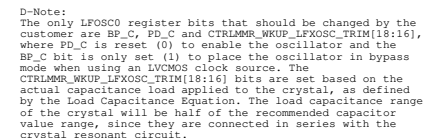
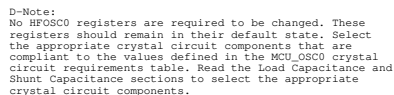


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Title		SOC POWER SUPPLIES - DECAPS 2	
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D-Note:
SoC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SoC IO.

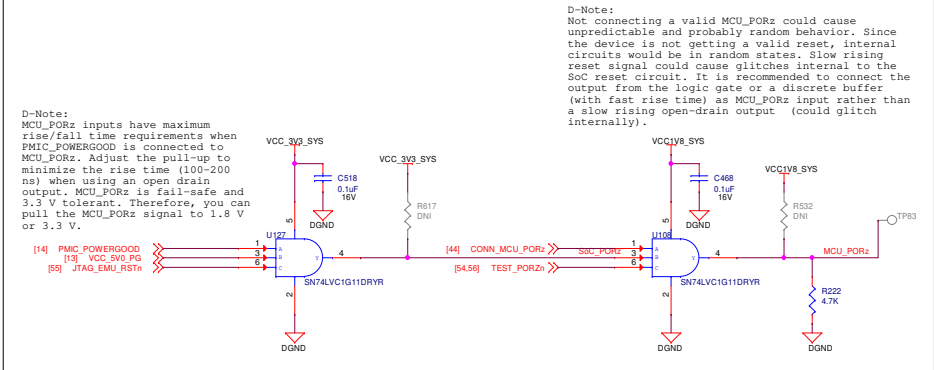


D-Note:
Refer to the SoC data sheet for the oscillator specs, when oscillator is used along with the clock buffer and also when the oscillator is directly connected as SoC clock.

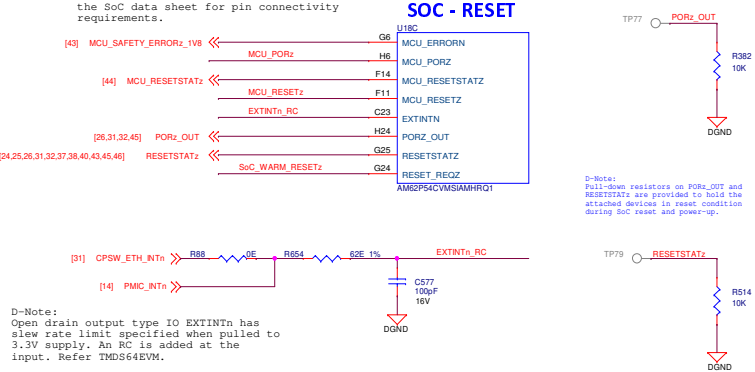
D-Note:
R27 pull-down is populated when SoC clock is used. The pull-down holds the buffer input low until the SoC clock output is configured.

SOC RESET

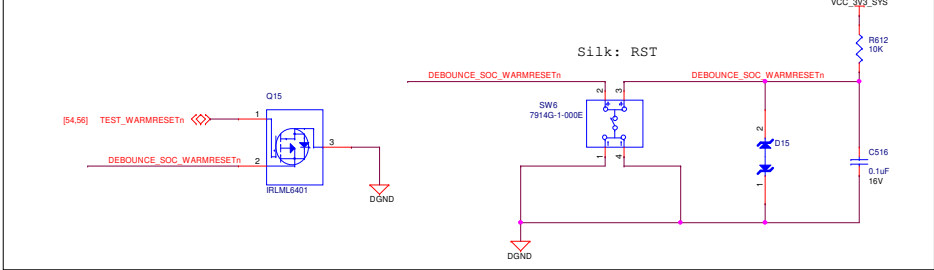
MCU POWER ON RESET



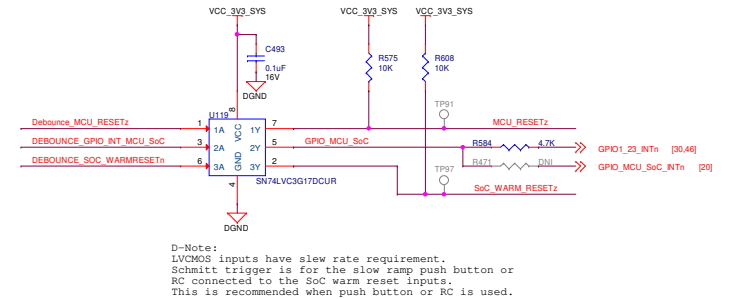
D-Note:
Provide a provision for a pull-down. Populate when attached device is connected. Refer to the SoC data sheet for pin connectivity requirements.



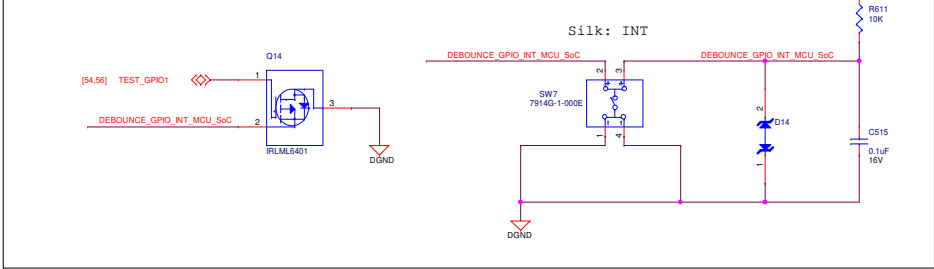
SOC WARM RESET PUSH BUTTON



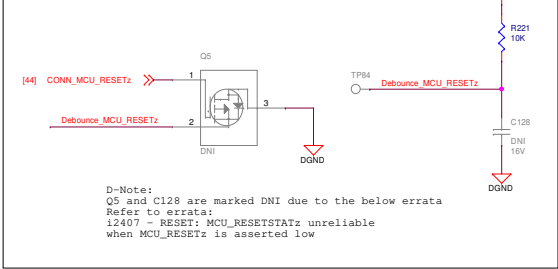
RESET & INT DEBOUNCE CIRCUIT



USER INTERRUPT PUSH BUTTON



SOC MCU WARM RESET



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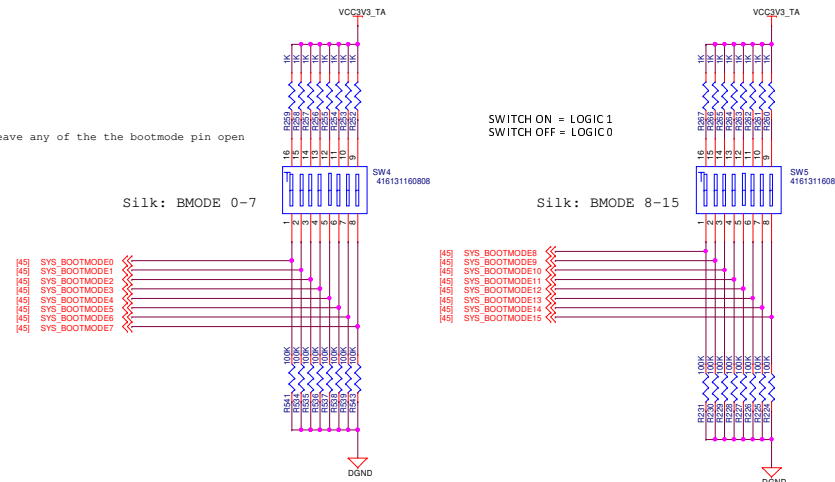


Title			SOC RESET	
Size	PROC164E2		Rev	
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BOOT MODE CONFIGURATION RESISTORS AND SWITCHES

D-Note: VCC3V3_TA supply is used for test automation.
Connect SoC_DVDD3V3 in the custom board design when buffers are not used

D-Note:
It is not recommended to leave any of the the bootmode pin open including reserved pins.

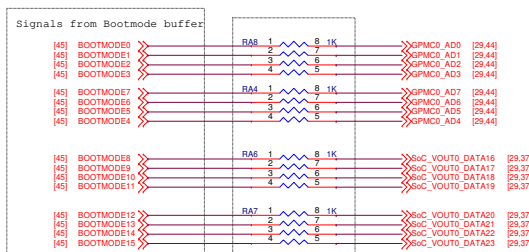


BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. USB0 MS

D-Note:
1. Dip switches are optional and are used on the SK for ease of configuration. A pull-up or pull-down resistor can be used to set the bootmode configuration. Provide provisions for pull-up and pull-down resistors for the bootmode pins that have configuration capability.
2. When DIP switches are used on a custom board, an external ESD protection may be required if the DIP switches are expected to be configured in an uncontrolled ESD environment.
3. When DIP switches are used, reduce the resistor values used for the divider to 47k and 470R ohms for maintaining the ratio.

BOOTMODE PINS



D-Note :
Connect SYS_BOOTMODE signals from BOOT mode configuration resistors and switches section when bootmode buffers are not used

D-Note:
1. 1k resistor at the output of the buffer is recommended when the bootmode pins are used for alternate functions.
2. When bootmode isolation buffers are not used, connect the bootmode configuration resistors directly to the SoC bootmode input pins. Connect the SOC bootmode signal used for alternate function to the attached device through OR for isolation or testing.

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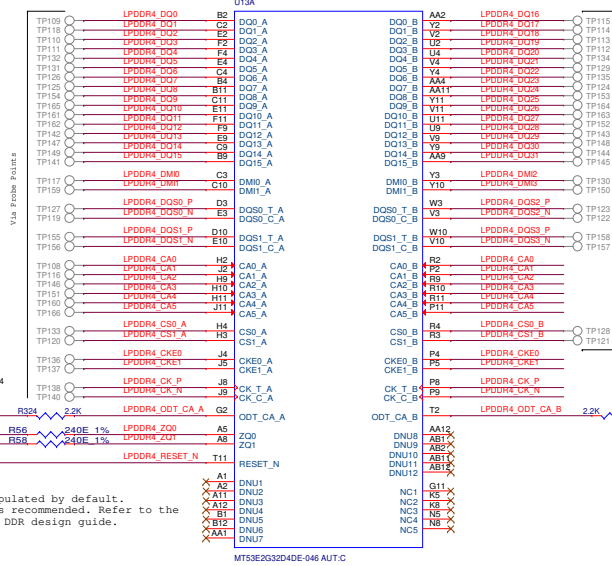


Title BOOT MODE CONFIGURATION RESISTORS AND SWITCHES

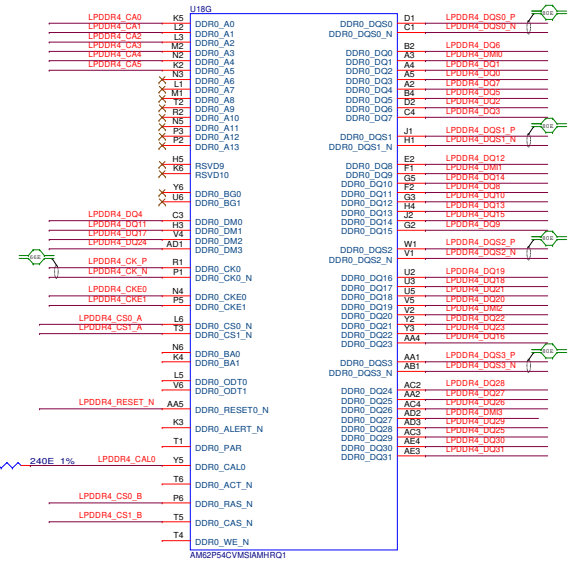
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LPDDR4 DEVICE

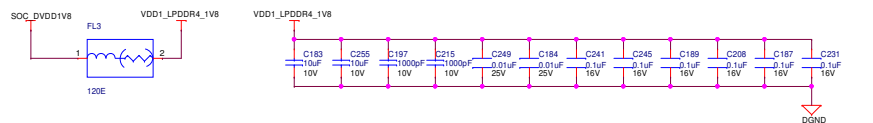
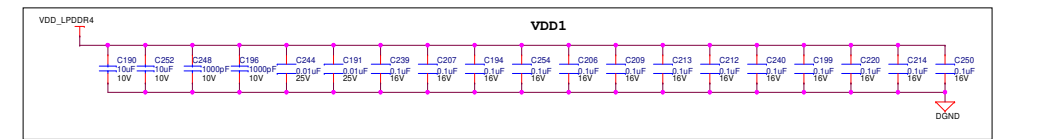
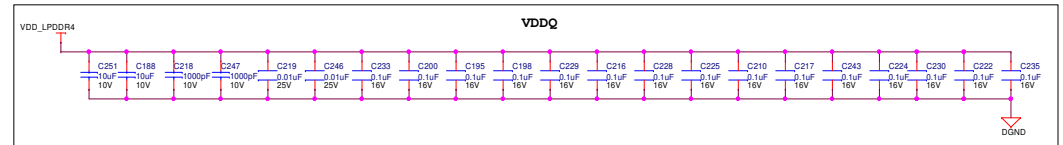
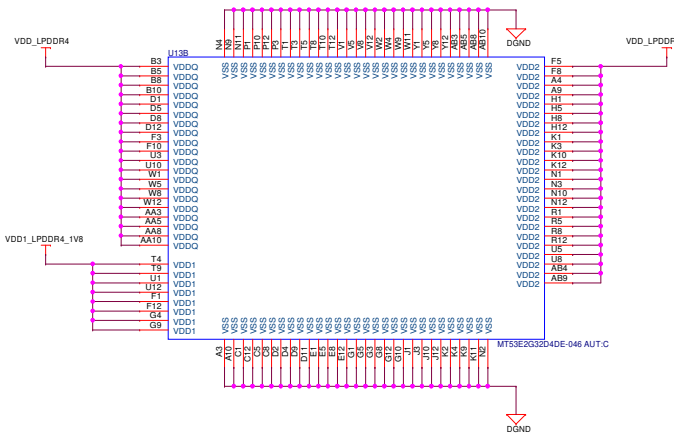
Silk: LPDDR4



SOC LPDDR4 INTERFACE



LPDDR4 POWER DECAPS



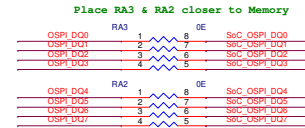
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Title Soc DDR and LPDDR4 DEVICE INTERFACE

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R-Note: These 0 ohm resistors are for configuring OSPI & QSPI. These are specific to the SK and optional if the interface is fixed.



R-Note:
DQS pulldown is enabled.

SOC OSPI INTERFACE

D-Note : Recommended OE provision on
OSPIO clock for signal integrity



Place R396 close
to the SoC

pad R421 & R417
avoid stubs

CAD Note:
Place R400 close to the SOC Ball
with as little trace as possible

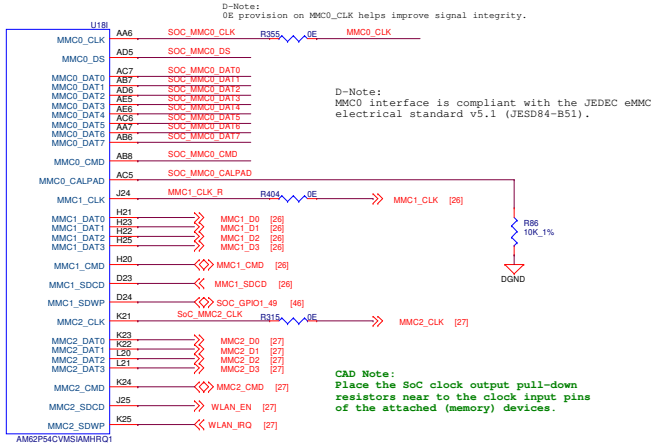
AM62P

D-Note:
ANDing logic additionally performs level translation. Verify the reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch could cause supply leakage and affect SoC operation.

eMMC INTERFACE

D-Note:
This family of processor implements a hard and dedicated PHY for eMMC interface.

SOC - MMC Interface



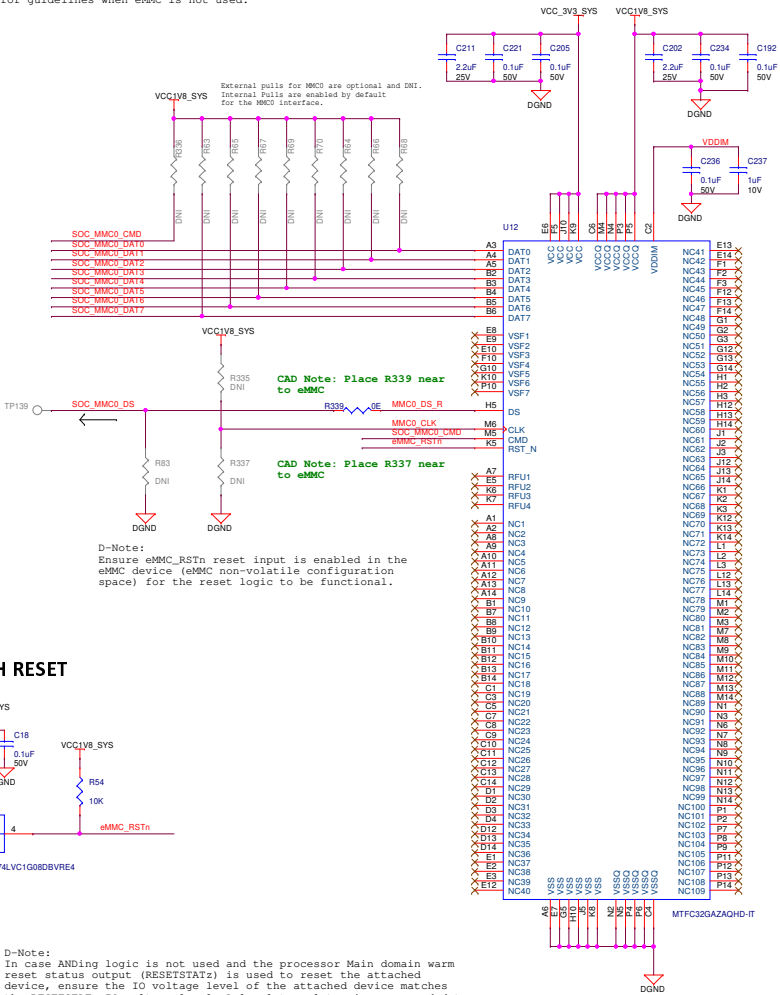
R-Note:
What is the reason we selected pull-down instead of pull-up for eMMC, SD card or other peripherals?
Because there are cases where the clock is stopped or paused in a low logic state and the pull-down option is consistent with this logic state.

D-Note:
1. You could eliminate the GPIO option and only use the reset output (warm or cold), where the software forces a warm reset, if the peripheral becomes unresponsive. However, this will reset the entire device rather than trying to recover the specific peripheral without resetting the entire device.
2. The GPIO reset option makes it possible for the software to reset the attached device (eMMC or OSPI or SD card or OLDIO or EPHY) without resetting the entire processor, if there is a case where the peripheral becomes unresponsive.

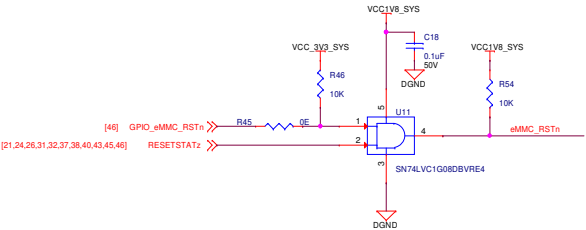
D-Note:
ANDing logic additionally performs level translation. Verify the reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch could cause supply leakage and affect SoC operation.

D-Note:
The pulls required for D0-D7, clock and other eMMC interface control signals are enabled internal to the SoC during reset and are eMMC JEDEC standard compliant. External pull-up is optional and can be deleted on the custom board. Refer to the pin connectivity table for guidelines when eMMC is not used.

eMMC FLASH



eMMC FLASH RESET



D-Note:
In case ANDing logic is not used and the processor Main domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level. A resistor divider could be used alternatively, provided optimum impedance value of the resistor divider is selected. If it is too high, the rise/fall time of the eMMC reset input could be slow and introduce too much delay. If it is too low, it will cause the AM62x to source too much steady-state current during normal operation.

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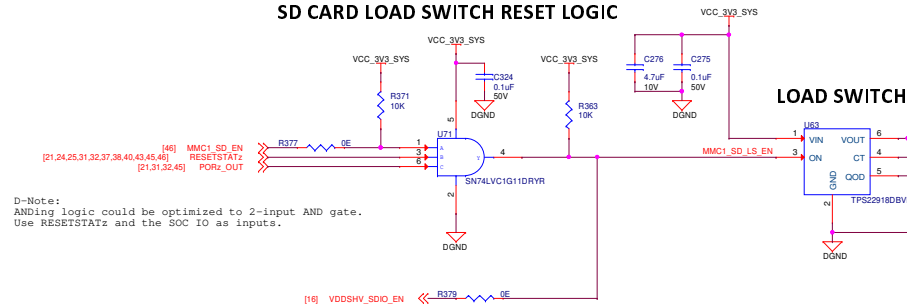


Title SOC MMC0[0:2] INTERFACE and eMMC FLASH + RESET

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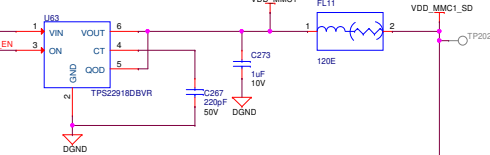
SD CARD INTERFACE

SD CARD LOAD SWITCH RESET LOGIC



D-Note:
ANDing logic could be optimized to 2-input AND gate.
Use RESETSTATz and the SOC IO as inputs.

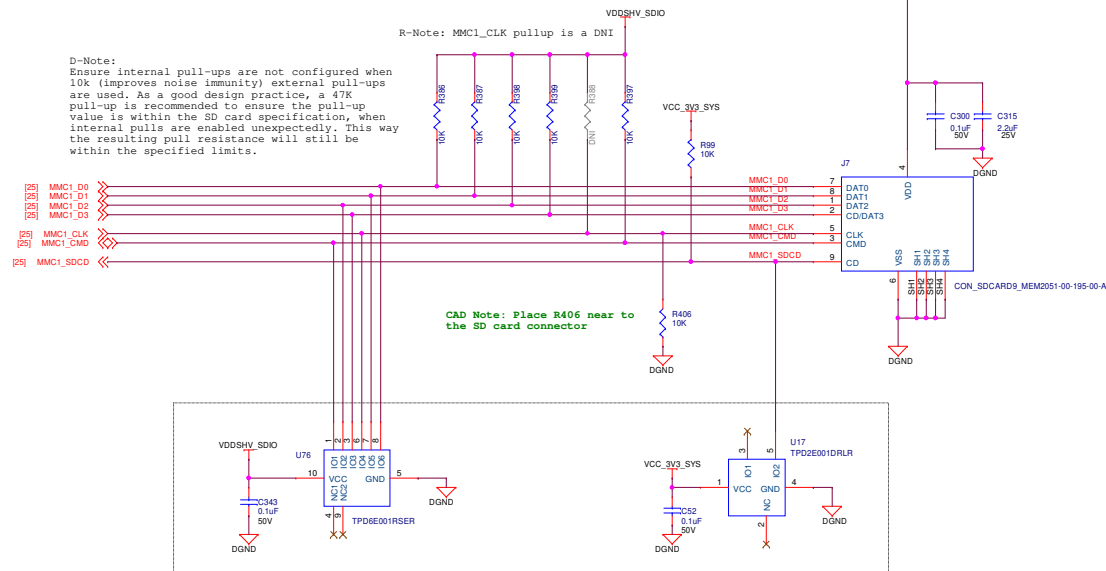
LOAD SWITCH



D-Note:
For UHS-I operation, the pullups are recommended to be connected to the 3.3 V/1.8 V switched LDO output.

D-Note:
Ensure internal pull-ups are not configured when 10k (improves noise immunity) external pull-ups are used. As a good design practice, a 47K pull-up is recommended to ensure the pull-up value is within the SD card specification, when internal pulls are enabled unexpectedly. This way the resulting pull resistance will still be within the specified limits.

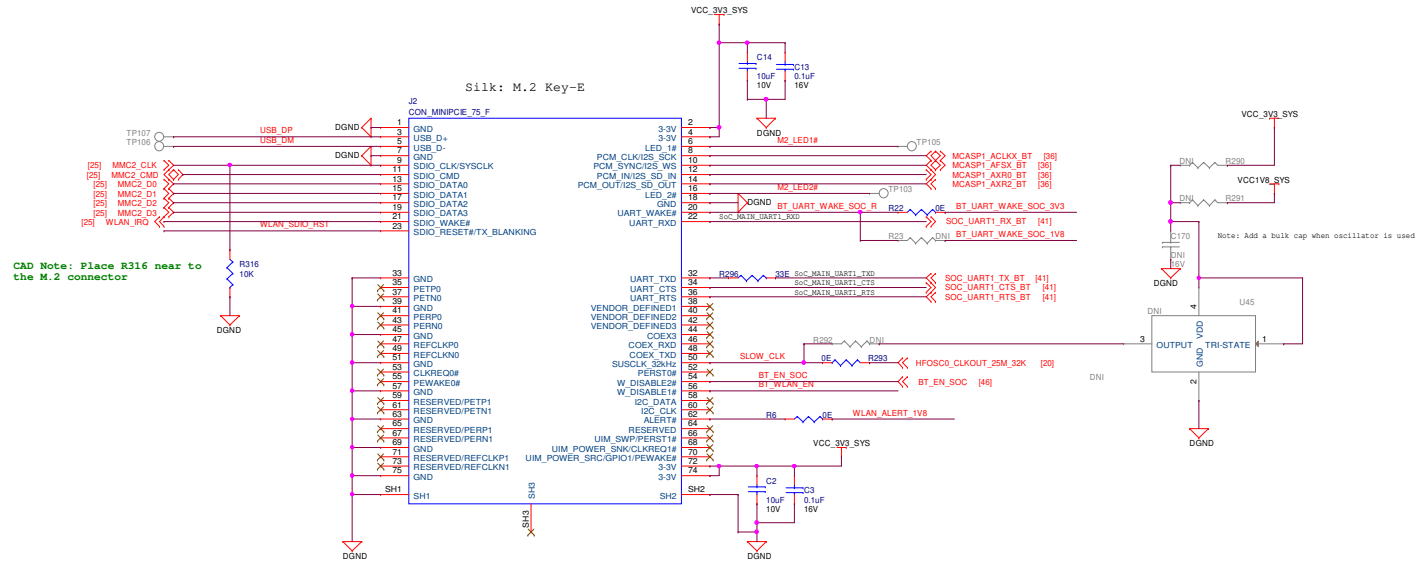
R-Note: MMC1_CLK pullup is a



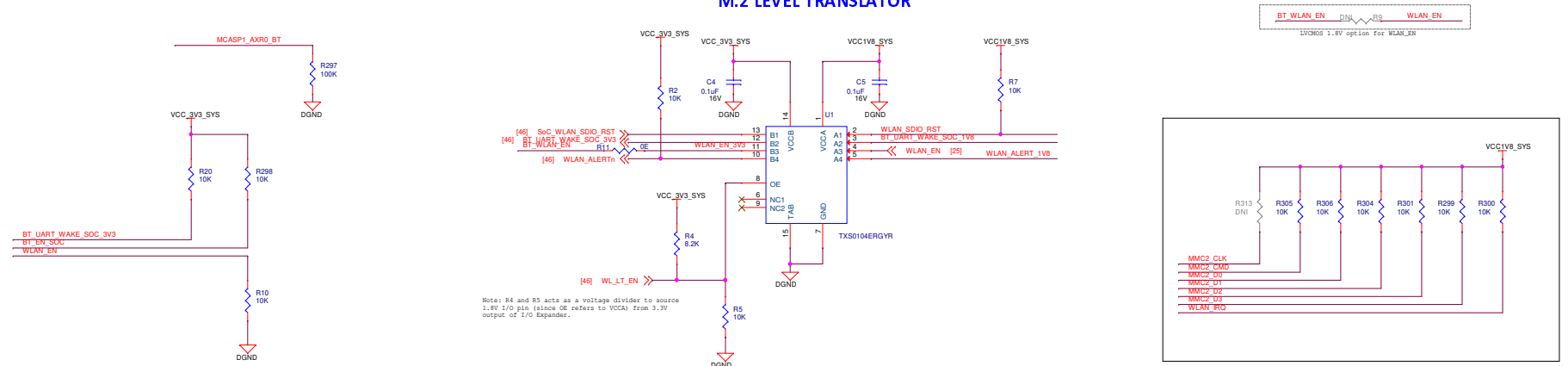
CAD Note: Place R406 near to the SD card connector

D-Note: Place near to SD Card Connector

M.2 INTERFACE - SDIO



M.2 LEVEL TRANSLATOR



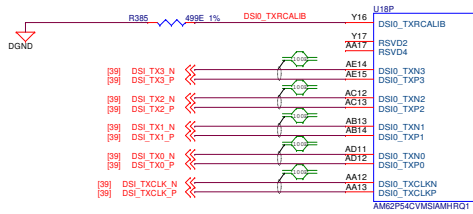
Designed for TI by Mistral Solutions Pvt Ltd



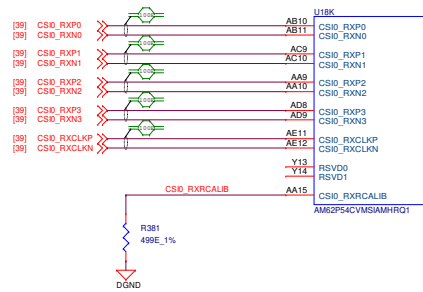
Title M.2 INTERFACE AND CONNECTOR

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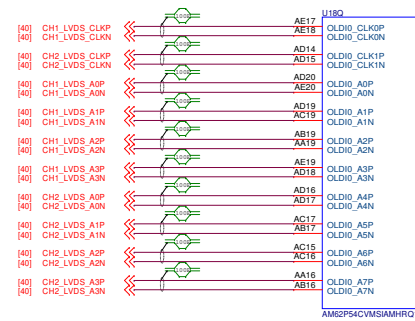
SOC - DSI



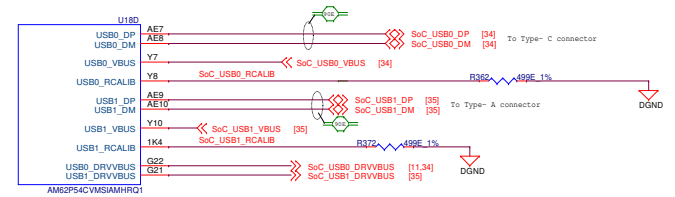
SOC - CSI



SOC - OLDI



SOC - USB



D-Note:
DNI USBx_DRVVBUS pull-up and pull-down to implement wake-up from deep sleep.
For Normal USB operation, there is an internal pull-down enabled during SoC reset.

SOC - ETHERNET INTERFACE



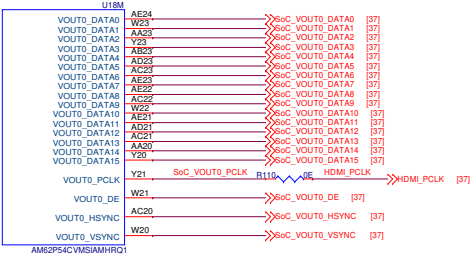
SOC - GPMC INTERFACE

D-Note:
Shorting of bootmode inputs (IOs) is not recommended or allowed, since the IOs have alternate functions that could be configured after booting. Shorting the bootmode pins directly to VCC or ground is not recommended. Connect each of the bootmode pins through separate resistor. Choose the bootmode resistor value based on the use case (10K or similar).

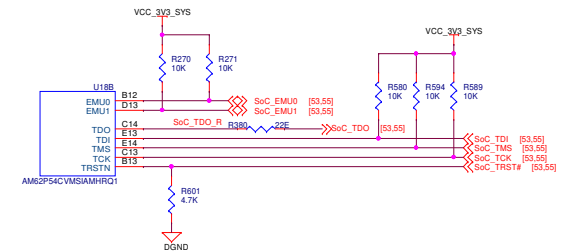
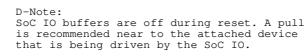
D-Note:
SoC IO buffers used for GPMC interface signals are disabled during reset. The required pulls for the interfaced signals are provided on the GPMC interface card.



SOC - VIDEO OUTPUT



SOC - JTAG



D-Note:
EXT_REFCLK1 is used as CLKOUT0. A clock signal should always be connected point-to-point without any branches. When connecting CLKOUT0 to more than one (multiple) clock inputs, use a buffer with one input and multiple outputs.

D-Note:
SoC Io is recon that is

CPSW3G RGMII_1 ETHERNET PHY

D-Note:
The caps and values used are as per the EPHY data sheet recommendations.

R-Note:
Ferrite is DNI

R-Note:
Verify the power sequence requirements for two-supply configuration and three-supply configuration.

R-Note:
Refer to DP83867ERG2-R-EVM when using LAN Discrete Transformer Module and RJ45 connector.

RJ45 CONNECTOR WITH INTEGRATED MAGNETICS

D-Note:
Provide provision for series resistor based on EPHY for RX signals near to the EPHY.

D-Note:
Allowed amplitude for XI clock input is 1.8 V irrespective of the IO supply. Use a CAP DIVIDER when the clock amplified is 3.3 V.

D-Note:
Refer to the EPHY EVM for JTAG connection.

D-Note:
ANDing logic could be optimized to a 2-input AND gate. Use RESETSTATz (or PORz_OUT) and the SoC IO as inputs.

Note:
Verify the resistor mounting configuration for resistors that are marked as DNI

D-Note:
ANDing logic additionally performs level translation. Verify the reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch could cause supply leakage and affect SoC operation.

PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

Designed for TI by Mistral Solutions Pvt Ltd

TEXAS INSTRUMENTS

MISTRAL

Title CPSW3G RGMII_1 ETHERNET PHY

Size PROC164E2

C

Date Thursday, October 30, 2025

Sheet 31 of 56

Rev E2

```
PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns
```

Designed for TI by Mistral Solutions Pvt Ltd



Title	CPSW3G RGMII 1 ETHERNET PHY
-------	-----------------------------

Size	BB0010150
------	-----------

C	PROC164E2
---	-----------

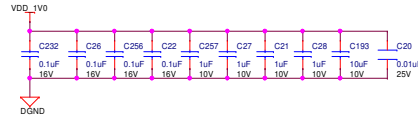
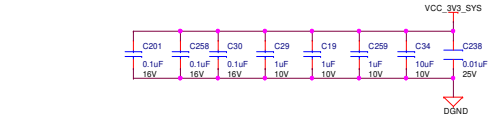
Date: Thursday, October 30, 2025	Sheet 31 of 58
----------------------------------	----------------

Rev

E2

CPSW3G RGMII_2 ETHERNET PHY

D-Note:
The caps and values used are as per the EPHY data sheet recommendations.



D-Note:
Refer to DP83867ERG2-R-EVM when using LAN Discrete Transformer Module and RJ45 connector.

D-Note:
Provide provision for series resistor based on EPHY for RX signals near to the EPHY.

D-Note:
Allowed amplitude for XI clock input is 1.8 V irrespective of the IO supply. Use a CAP DIVIDER when the clock amplified is 3.3 V.

D-Note:
Refer to the EPHY EVM for JTAG connection.

[30,31] SoC_RGMII_MDC
[30,31] SoC_RGMII_MDIO

CAD NOTE: TP19 is a via probe point

TP19

TP20

TP21

TP22

TP23

TP24

TP25

TP26

TP27

TP28

TP29

TP30

TP31

TP32

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TP276

TP277

TP278

TP279

TP280

TP281

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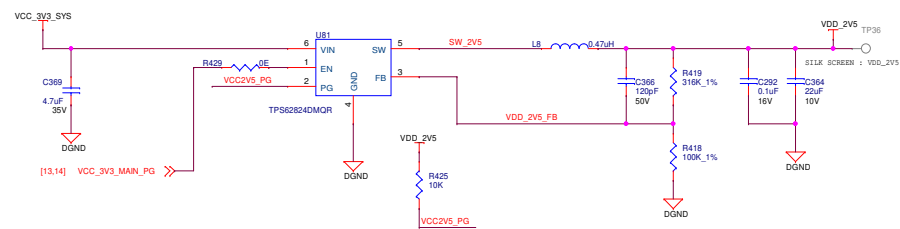
TP291

TP292

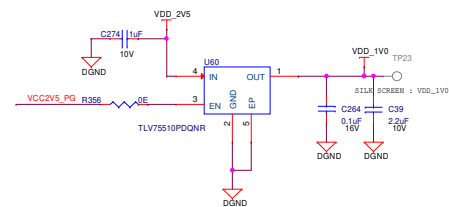
TP293

POWER SUPPLIES FOR ETHERNET PHY

2.5V (ETHERNET PHY), 1.0AMPS SUPPLY



1.0V (ETHERNET PHY), 0.5AMPS SUPPLY



Designed for TI by Mistral Solutions Pvt Ltd



Title POWER SUPPLIES FOR ETHERNET PHY

Size PROC164E2

C

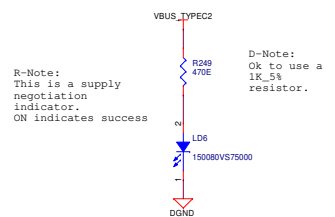
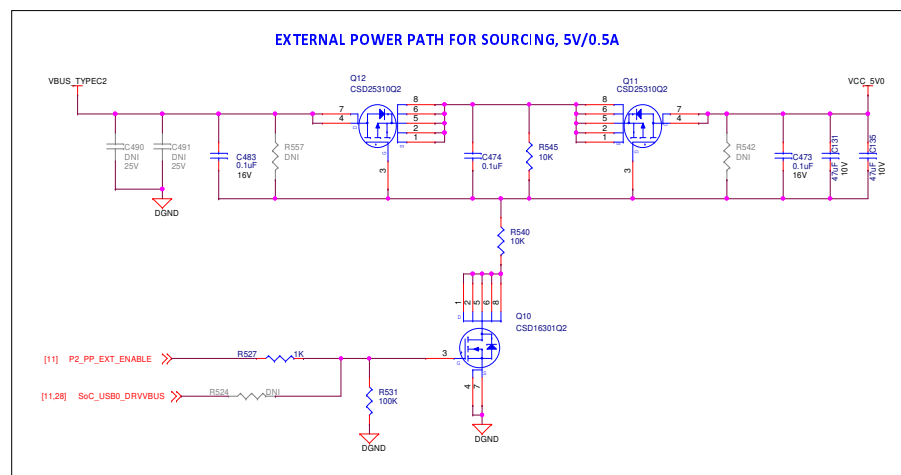
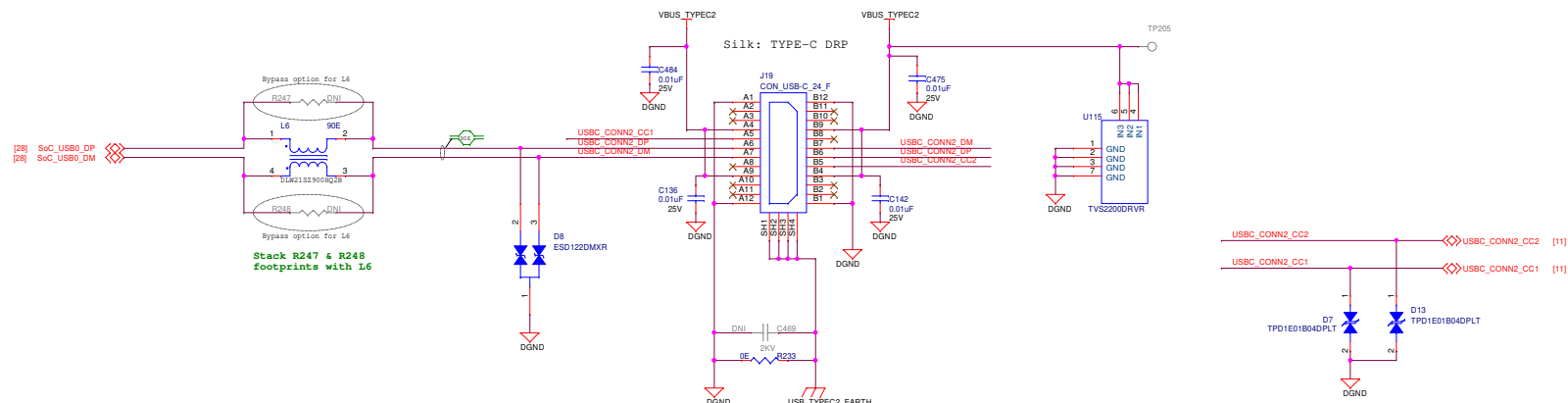
Date: Thursday, October 30, 2025

Sheet 33 of 58

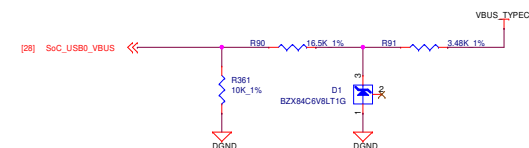
Rev

E2

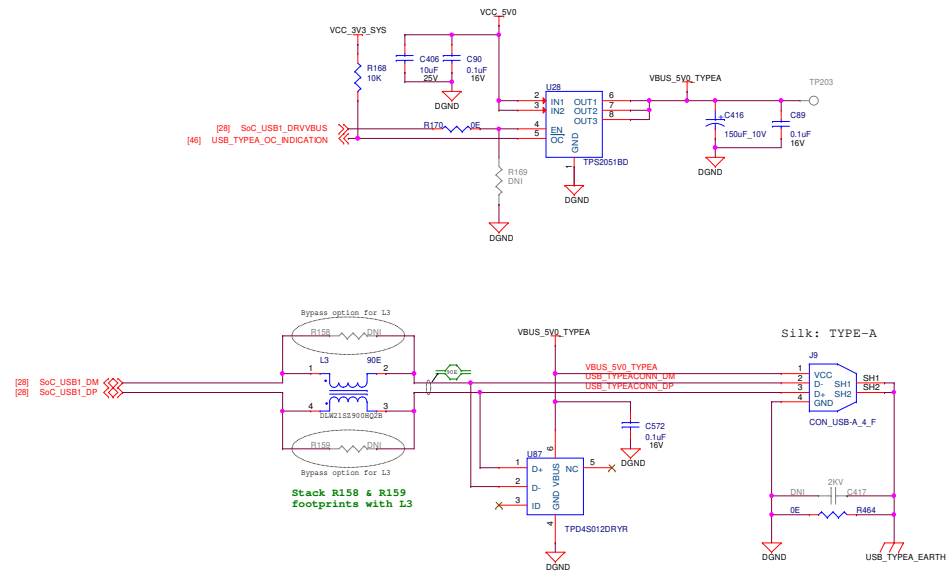
USB0 TYPE-C DRP



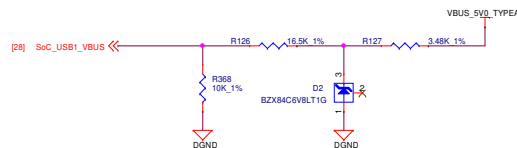
D-Note:
Refer to the USB VBUS Design Guidelines section of the SoC data sheet.



USB1 TYPE-A



D-Note:
 Refer to the USB VBUS Design Guidelines section of the SoC data sheet.



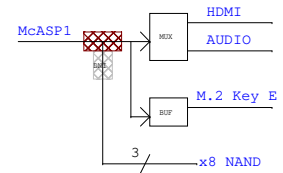
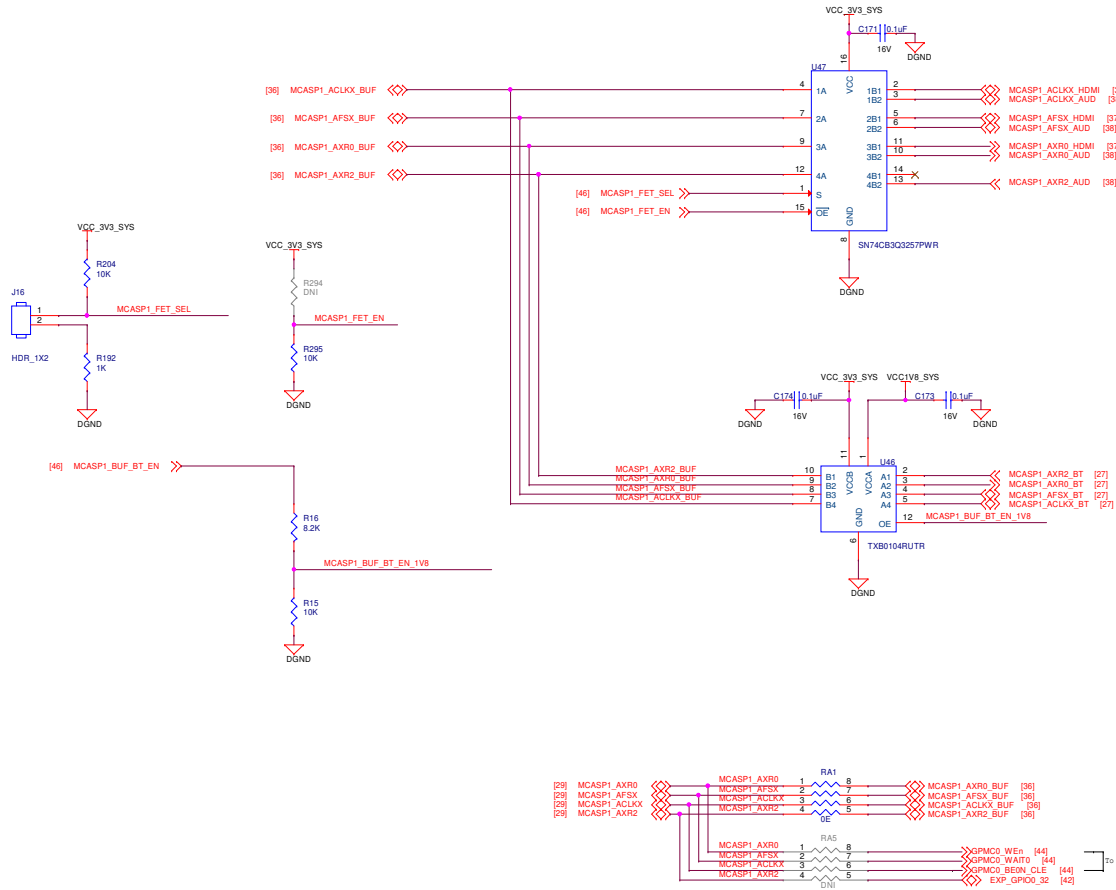
Designed for TI by Mistral Solutions Pvt Ltd



Title USB1 TYPE-A CONNECTOR, VBUS DIVIDER & POWER SWITCH

Size	Rev
C	PROC164E2
Date:	Thursday, October 30, 2025
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SOC MAIN McASP1 FET BUS SWITCH & VOLTAGE LEVEL TRANSLATOR



AUDIO CODEC

Silk: LINE IN

I2C ADDRESS: 0x18

TLV320AIC3106RQZT

CODEC I2C ADDRESS SELECTION

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B

AUDIO CODEC RESET

DESIGNED FOR TI BY MISTRAL SOLUTIONS PVT LTD

TEXAS INSTRUMENTS

MISTRAL

Title: AUDIO CODEC

Size: C

Proc: 164E2

Date: Thursday, October 30, 2025

Sheet: 38 of 58

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B

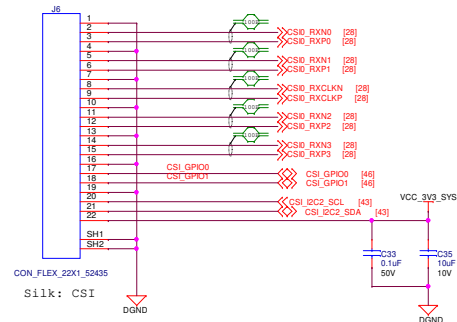


Size	PROC164E2
...	...

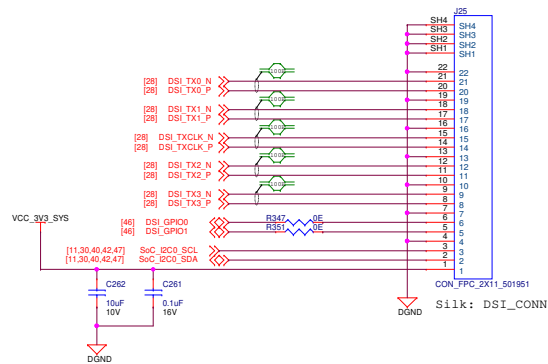
Date: Thursday, October 1, 2009

Sheet 38 of 58

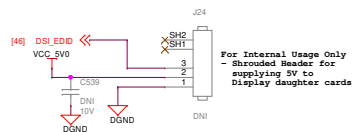
CSI INTERFACE



DSI INTERFACE



ADD ON CARD HEADER

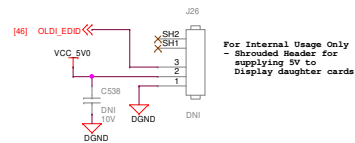


Designed for TI by Mistral Solutions Pvt Ltd



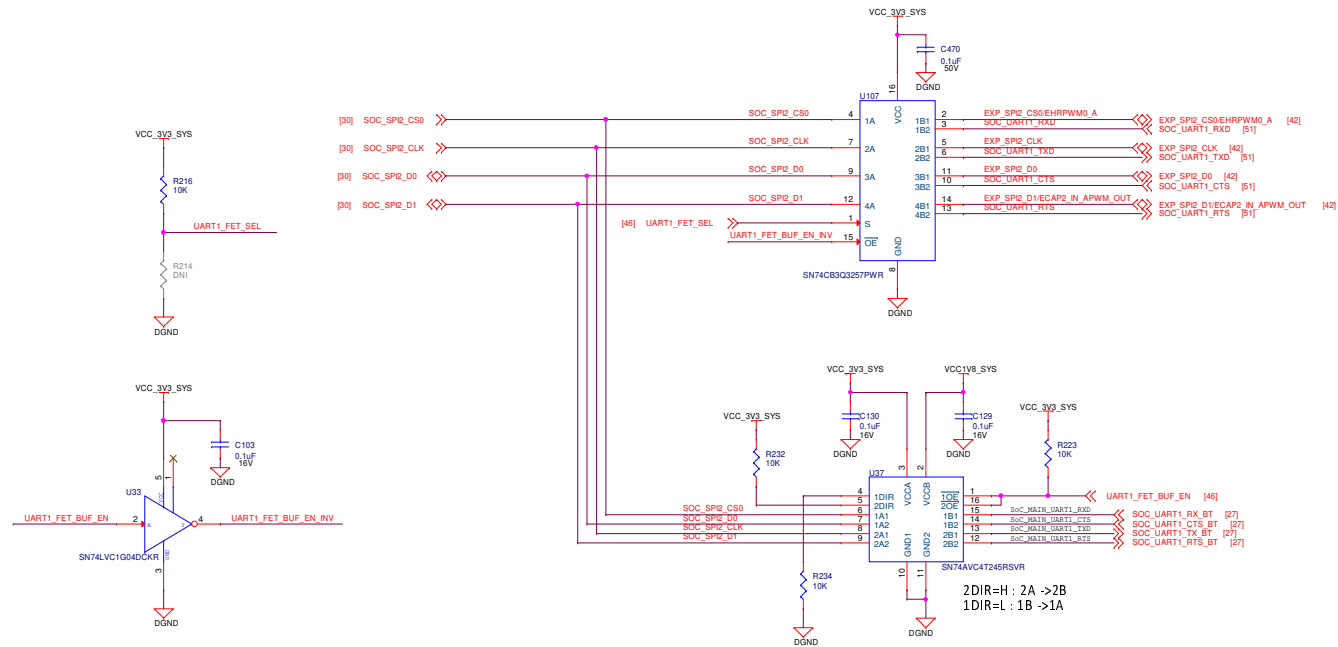
Title CSI AND DSI LCD INTERFACE CONNECTOR

Size	Rev
C	PROC164E2
Date:	Thursday, October 30, 2025
Sheet	39 of 58

[illegible]

Sheet 40 of 58

SOC MAIN UART1 - FET SWITCH & VOLTAGE LEVEL TRANSLATOR



OEn	SEL	INPUT/OUTPUT An	
L	L	An=nB1	SOC - EXP CONN
L	H (DEFAULT)	An=nB2	SOC - FT4232

Designed for TI by Mistral Solutions Pvt Ltd



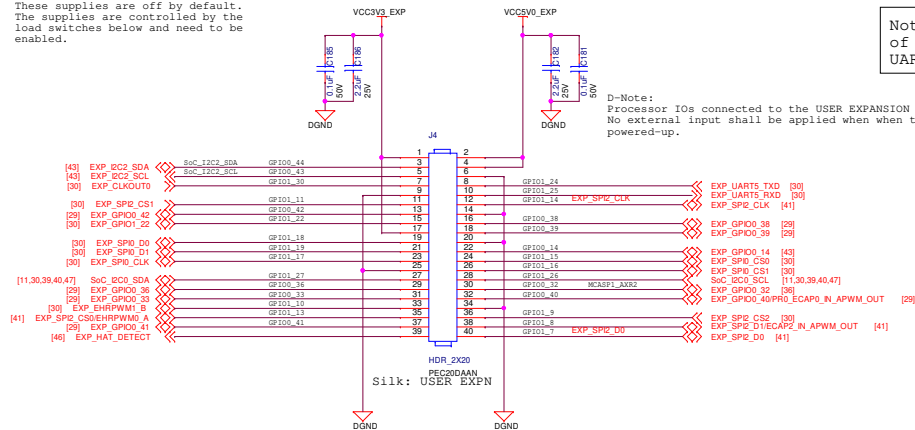
Title SOC MAIN UART1 - FET SWITCH & LEVEL TRANSLATOR 1

Size	Rev
C	E2

Date: Thursday, October 30, 2025 Sheet 41 of 58

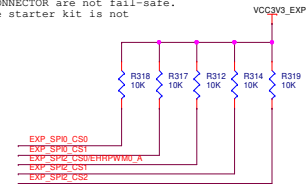
USER EXPANSION CONNECTOR

D-Note:
These supplies are off by default.
The supplies are controlled by the
load switches below and need to be
enabled.

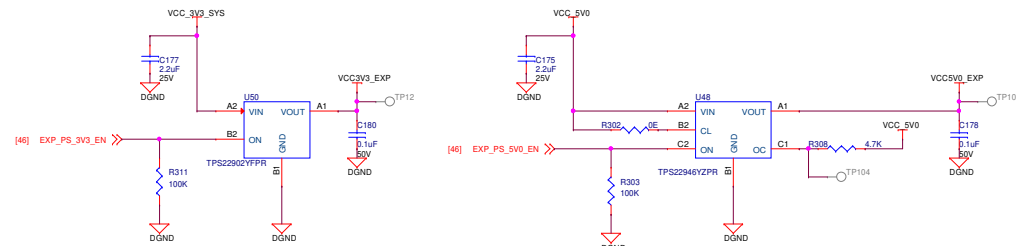


Note: Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)

D-Note:
Processor I/Os connected to the USER EXPANSION CONNECTOR are not fail-safe.
No external input shall be applied when the starter kit is not powered-up.



LOAD SWITCHES FOR USER EXPANSION CONNECTOR



D-Note:

AM62P Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62P Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

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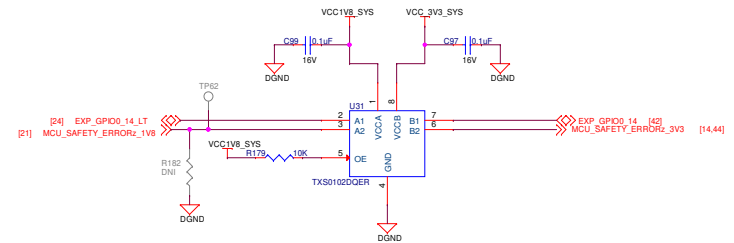
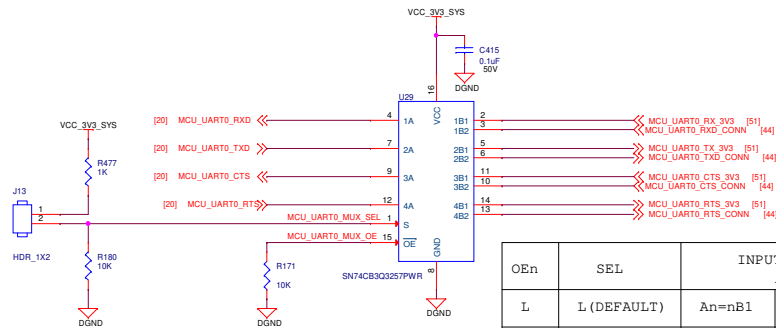
Title USER EXPANSION CONNECTOR

Size	Rev
C	E2
Date:	Thursday, October 30, 2025

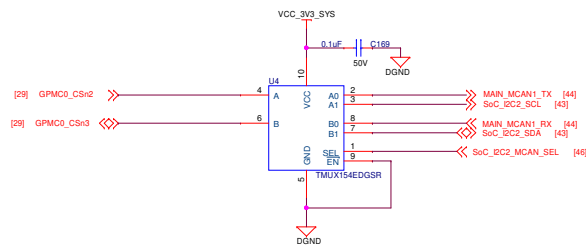
Sheet 42 of 58

MCU HEADER FET SWITCH AND LEVEL TRANSLATOR

SoC MCU UART0 FET BUS SWITCH

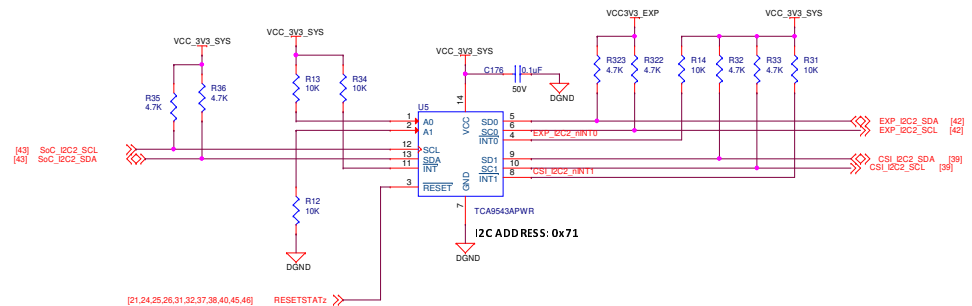


SOC I2C2/MCAN1 MUX



I2C SWITCH FOR SoC MAIN I2C2

D-Note: Both the I2C outputs are off during power-up.
The required I2C output needs to be configured.

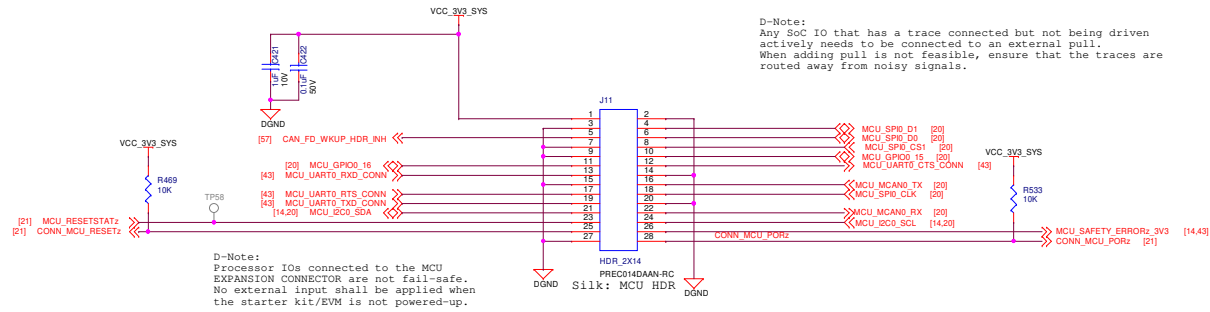


Designed for TI by Mistral Solutions Pvt Ltd

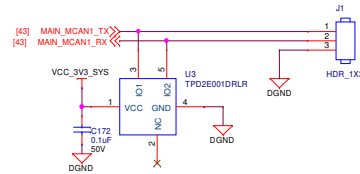


Title	
MCU HEADER FET SWITCH & LEVEL TRANSLATOR, I2C SWITCH AND MUX	
Size	Rev
C	PROJ164E2
Date:	Sheet
Thursday, October 30, 2025	43 of 58

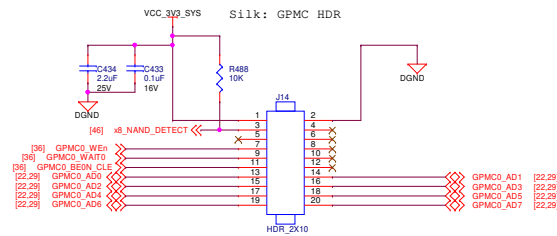
MCU EXPANSION HEADER



MCAN1 HEADER



GPMC HEADER



NOTE: J4, J11 & J14 will be used together when plugging in GPMC NAND (x8) Board

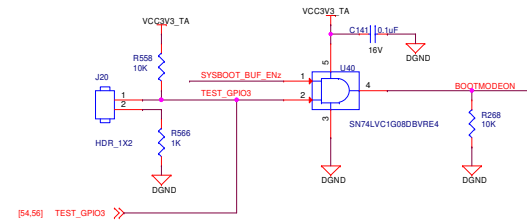
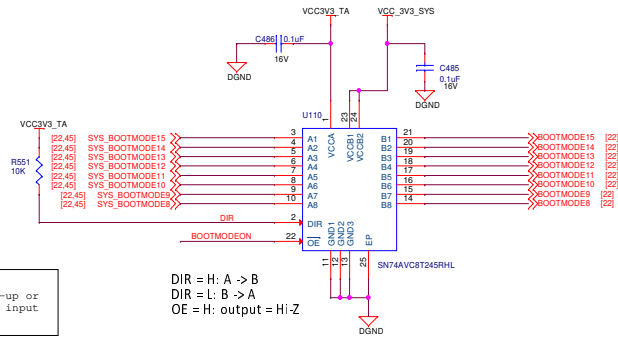
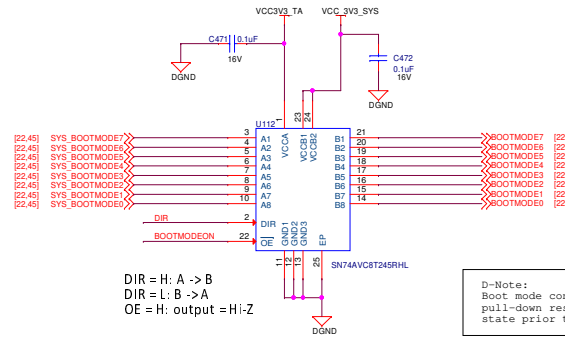
Designed for TI by Mistral Solutions Pvt Ltd



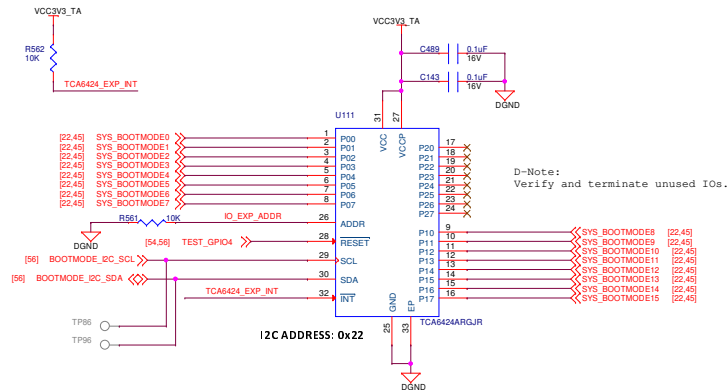
Title		
MCU HEADER, EXTERNAL MCAN CONNECTOR AND GPMC HEADER		
Size	Rev	
C	PROC164E2	E2
Date:	Thursday, October 30, 2025	Sheet 44 of 58

BOOTMODE BUFFERS AND IO EXPANDERS

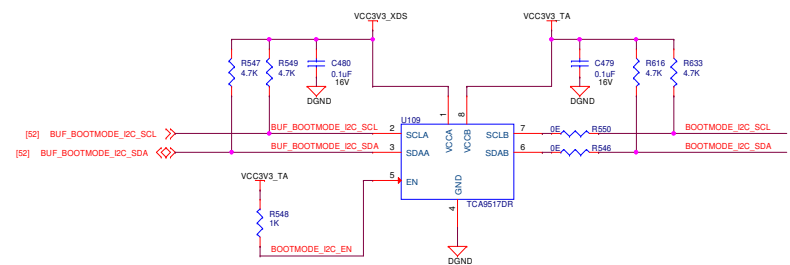
BOOT MODE BUFFERS



BOOTMODE IO EXPANDER



BOOTMODE I2C BUS BUFFER



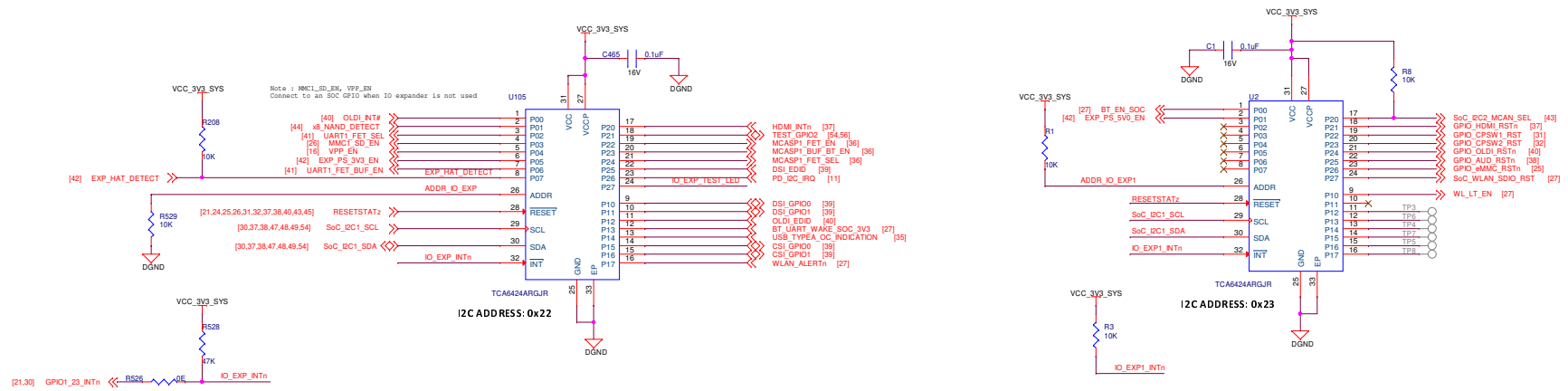
Designed for TI by Mistral Solutions Pvt Ltd



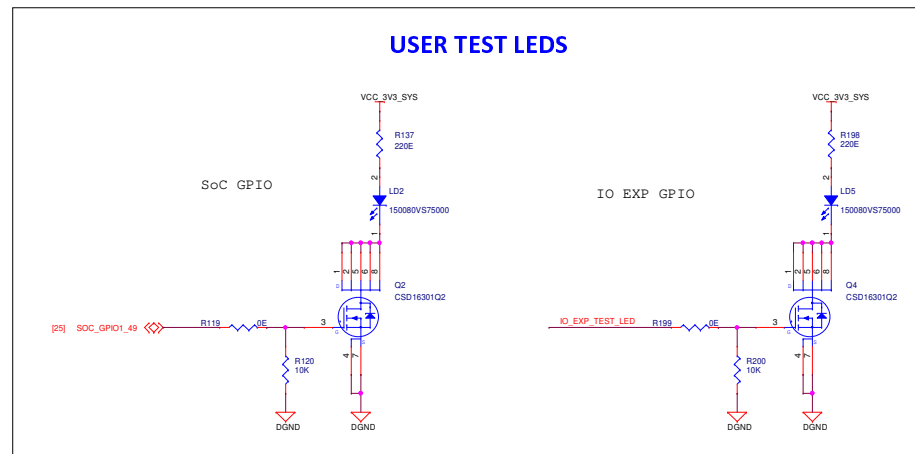
Title BOOTMODE BUFFERS AND IO EXPANDERS

Size	Rev
C	PROC164E2
Date:	Thursday, October 30, 2025
Sheet	45 of 58

IO EXPANDER



USER TEST LEDS



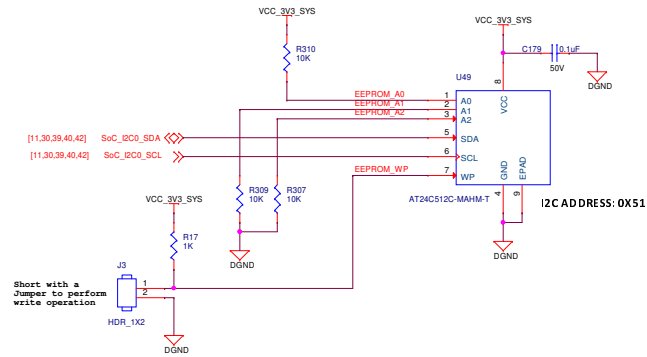
Designed for TI by Mistral Solutions Pvt Ltd



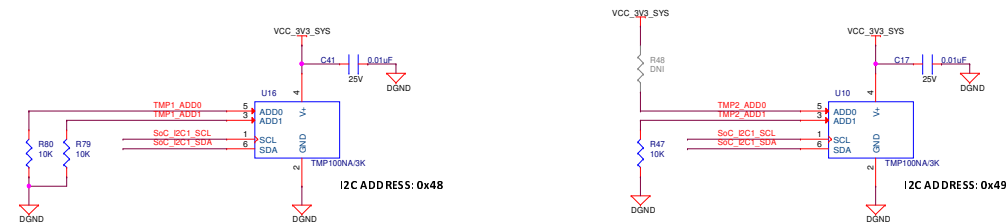
Title IO EXPANDER & USER TEST LED

Size	Rev
C	PROC164E2
Date:	Thursday, October 30, 2025
Sheet	46 of 58

BOARD ID EEPROM



DIGITAL TEMPERATURE SENSORS



CAD NOTE: PLACE TEMP SENSOR CLOSE TO SoC

CAD NOTE: PLACE TEMP SENSOR CLOSE TO LPDDR4

[30,37,38,46,48,49,54] SoC_I2C1_SCL
[30,37,38,46,48,49,54] SoC_I2C1_SDA
Silk: SOC_I2C1

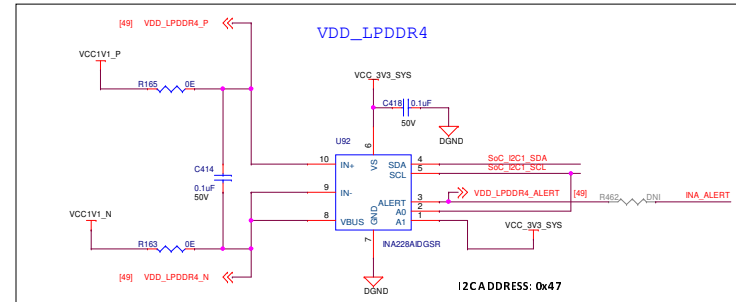
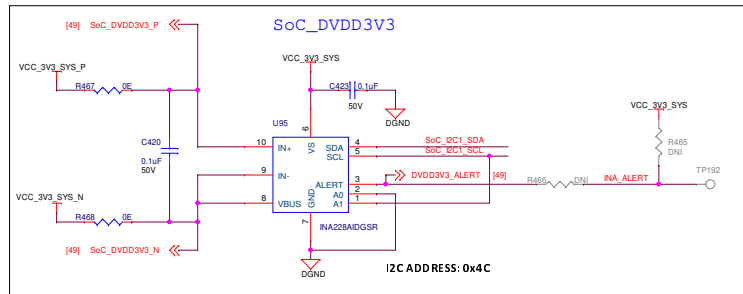
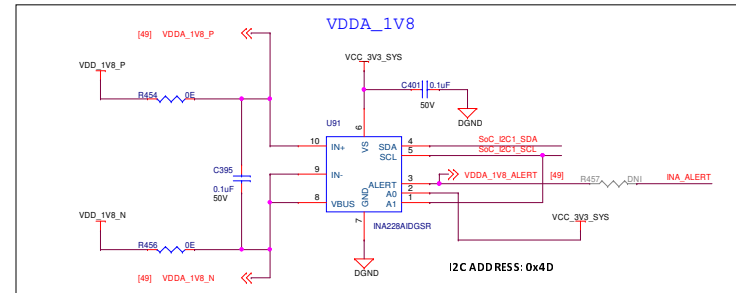
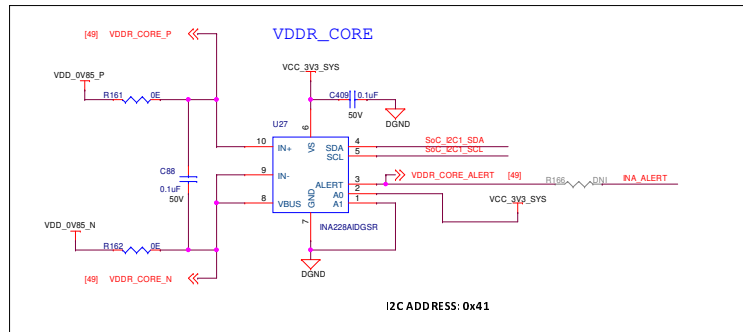
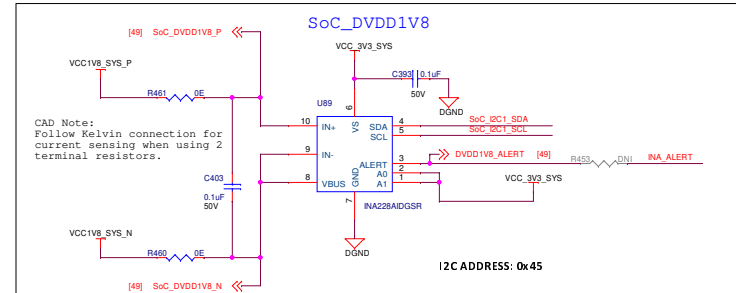
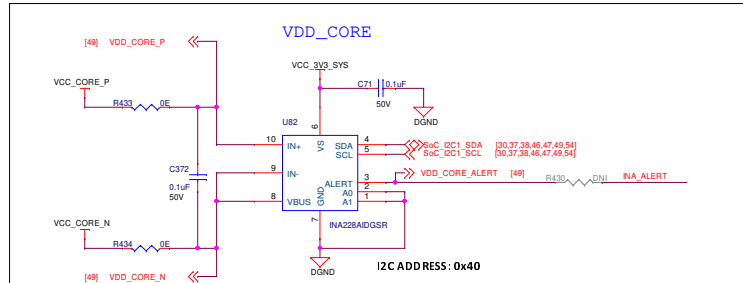
Designed for TI by Mistral Solutions Pvt Ltd



Title BOARD ID EEPROM & TEMPERATURE SENSORS

Size	Rev
C	E2
Date: Thursday, October 30, 2025	Sheet 47 of 58

CURRENT MONITORING DEVICES - 1



Note: The design supports current/voltage measurements using either INA228 or INA231. INA228 will be populated on the the SK (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_OV85	VDDR_CORE	41
VCC3V3_SYS	SoC_DVDD3V3	4C
VCC1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

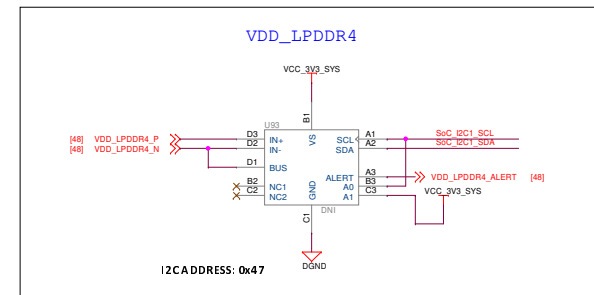
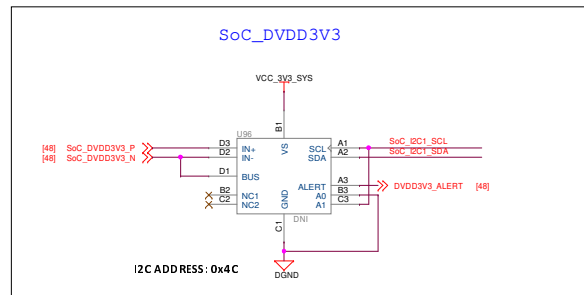
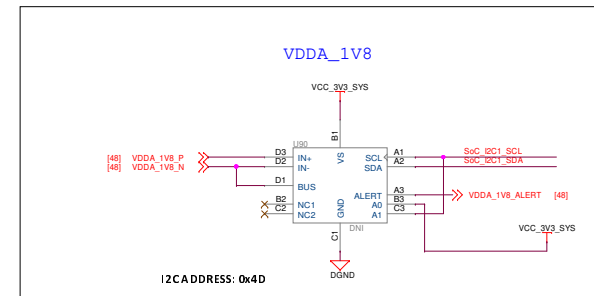
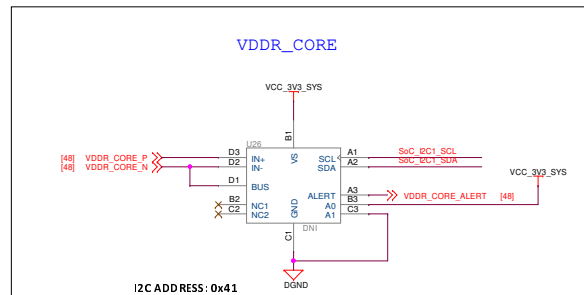
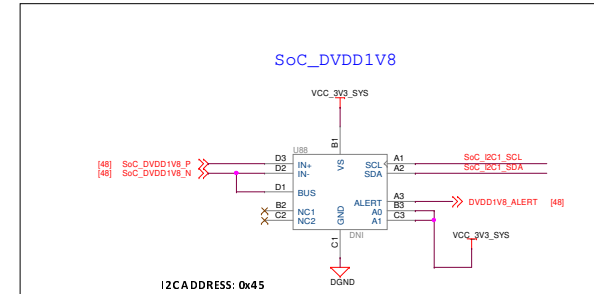
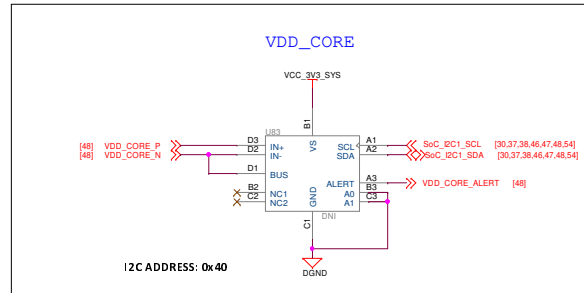
Designed for TI by Mistral Solutions Pvt Ltd



Title CURRENT MONITORING DEVICES - 1

Size	Rev
C	E2
Date: Thursday, October 30, 2025	Sheet 46 of 58

CURRENT MONITORING DEVICES - 2



Note: The design supports current/voltage measurements using either INA228 or INA231.
INA228 will be populated on the the SK
(Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_OV85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

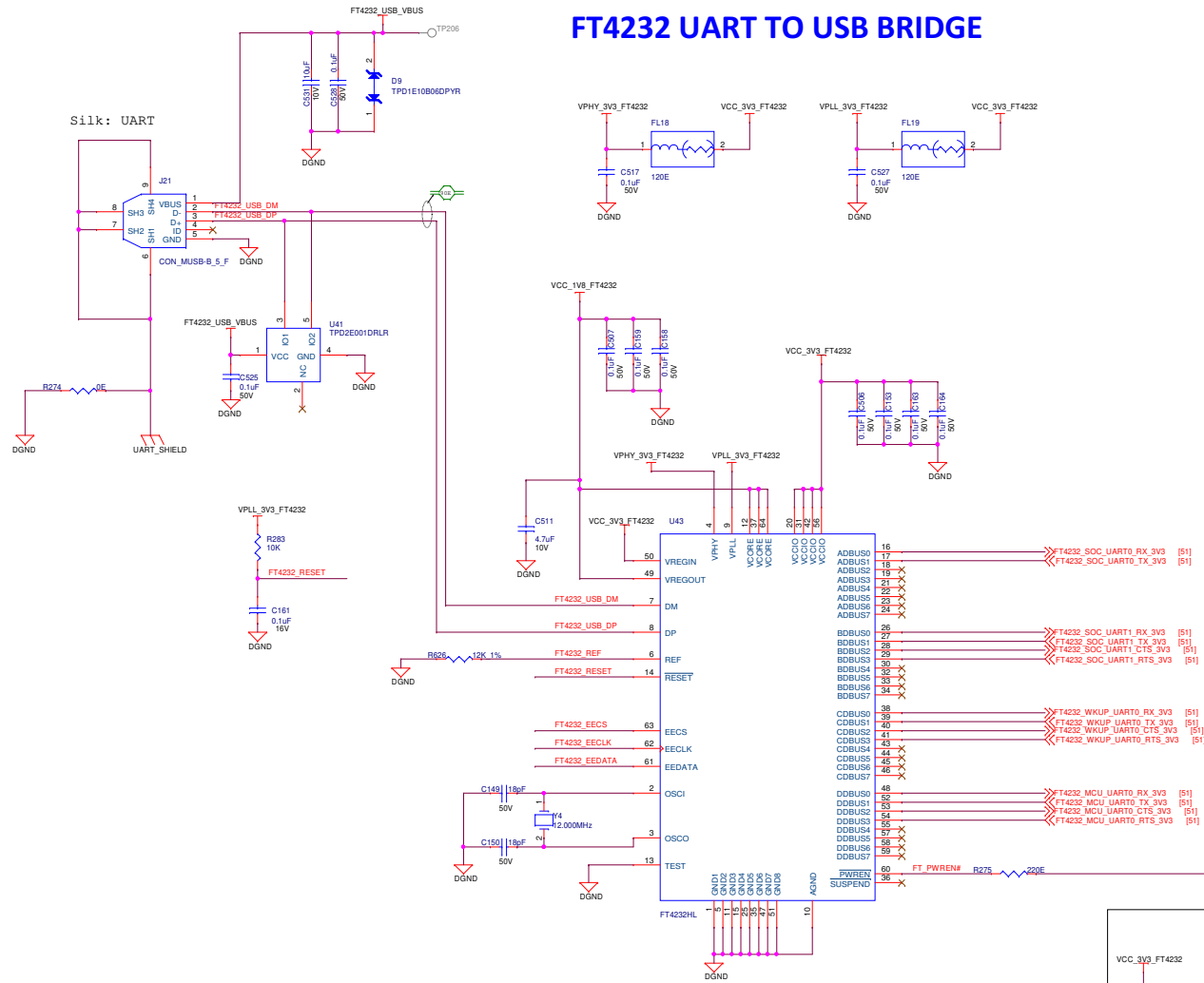
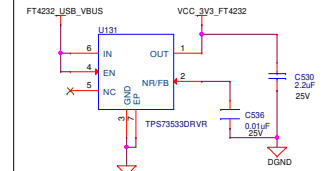
Designed for TI by Mistral Solutions Pvt Ltd



Title CURRENT MONITORING DEVICES - 2

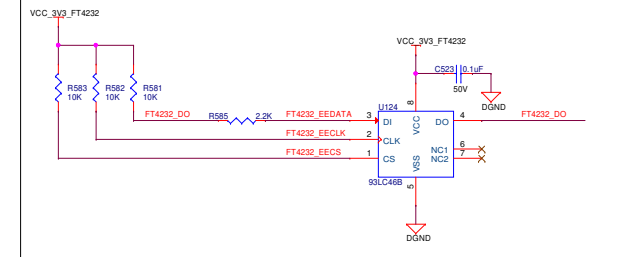
Size	Rev
C	PROC164E2
Date:	Thursday, October 30, 2025
Sheet	49 of 58

FT4232 UART TO USB BRIDGE

**FT4232: 5V to 3.3V@500mA LDO**

R-Note:
Verify the implementation with
the device manufacturer.

EEPROM



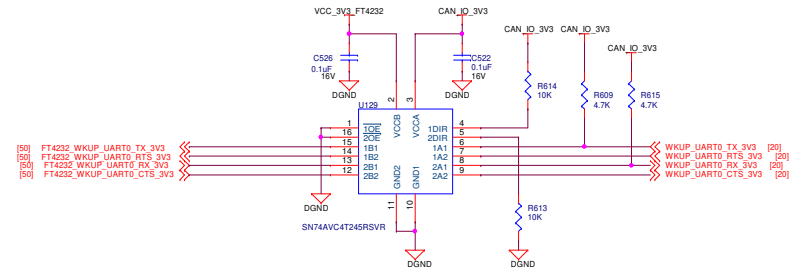
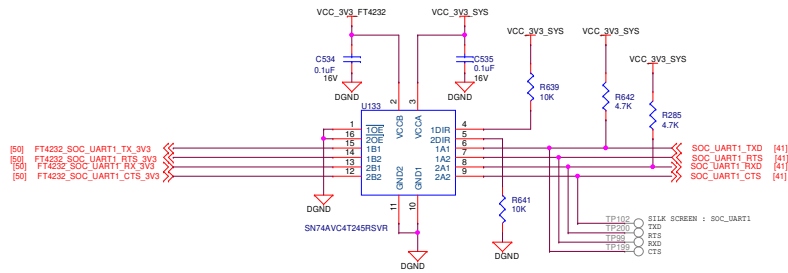
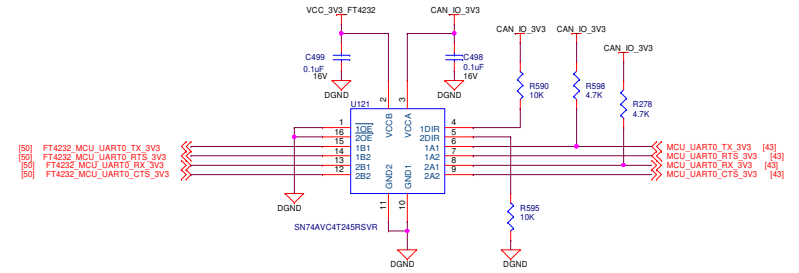
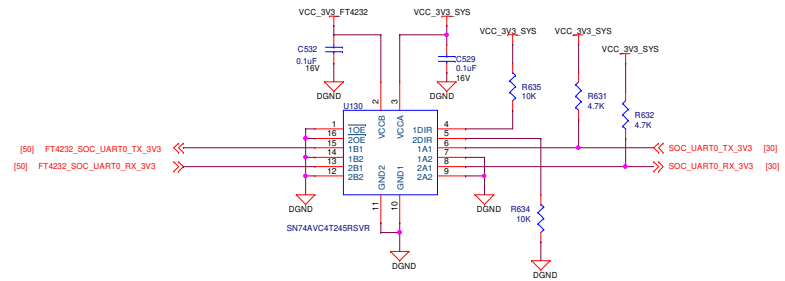
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Title	FT4232 UART TO USB BRIDGE
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FT4232 UART BUFFERS



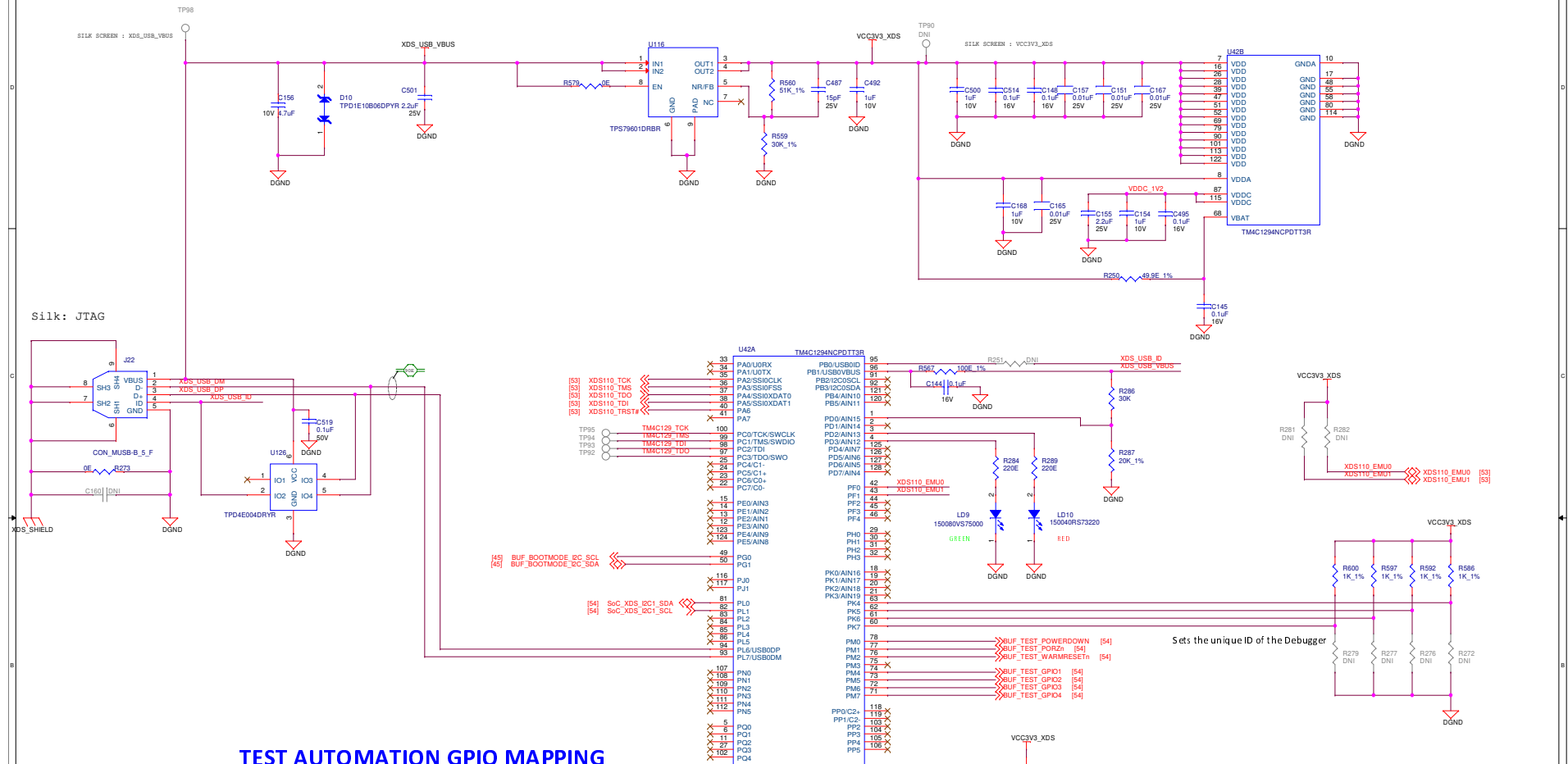
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Title FT4232 UART BUFFERS

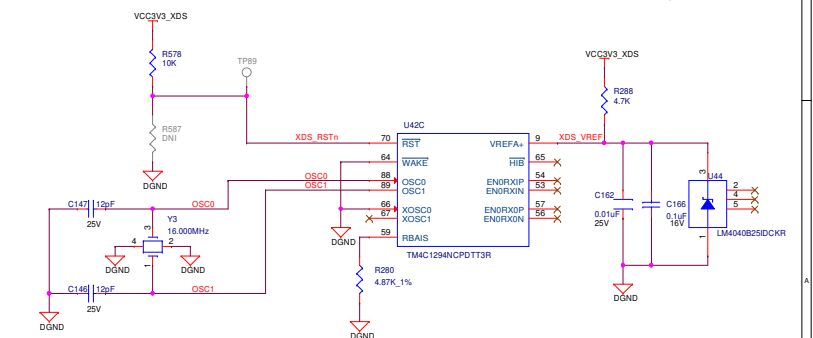
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XDS110 DEBUGGER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPI01	Used to Generate the interrupt on SOC_GPI00_90 Pin	OUTPUT	External Pullup
TEST_GPI02	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPI03	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPI04	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup



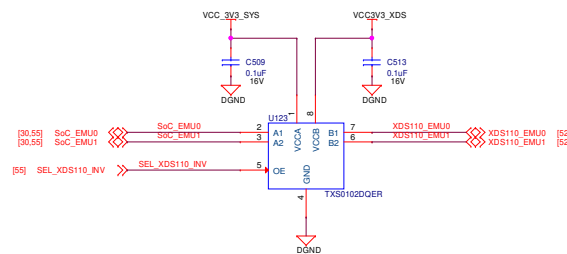
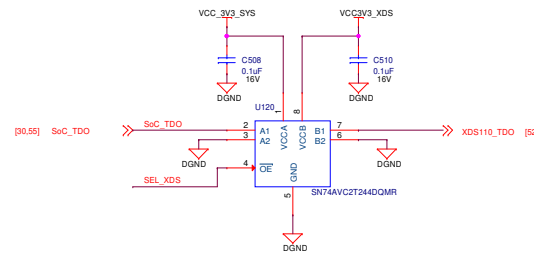
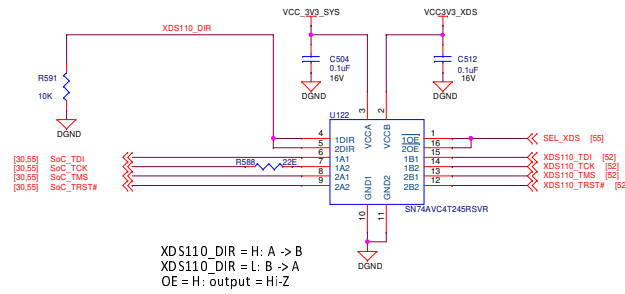
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Title	XDS110 DEBUGGER
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XDS110 JTAG BUFFER



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Title XDS110 JTAG BUFFER

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D



B



<p>TA Header Configuration</p> <p>Mount : R201, R202, R479</p> <p>Demount: R483, R576, R577</p>
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Designed for TI by Mistral Solutions Pvt Ltd		Title		XDS110 TEST AUTOMATION BUFFERS	
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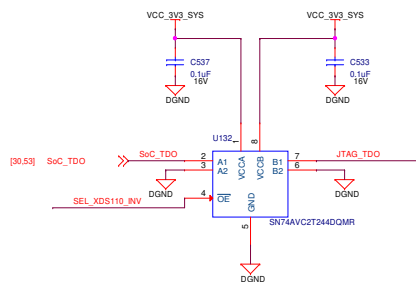


MISTRA

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[illegible]

JTAG_DIR = H: A -> B
JTAG_DIR = L: B -> A
OE = \bar{H} : output = Hi-Z



D-Note:
Place pulls on the JTAG signals near to the SoC.
Refer to the SoC data sheet for pin connectivity requirements.

VCC_JV3_SYS
R655
4.7k

[P1] _JTAG_EMU_RSTn

C152 0.1uF
18V
GNDN

Silk: cTI

J23

JTAG_TMS 1
JTAG_TDI 3
JTAG_TDO 9
JTAG_CTI_PCLK 7
JTAG_CTI_TCK 11
JTAG_CTI_TCK 13
_JTAG_EMU_RSTn 15
16
17
18

2
4
8
10
12
14
16
18

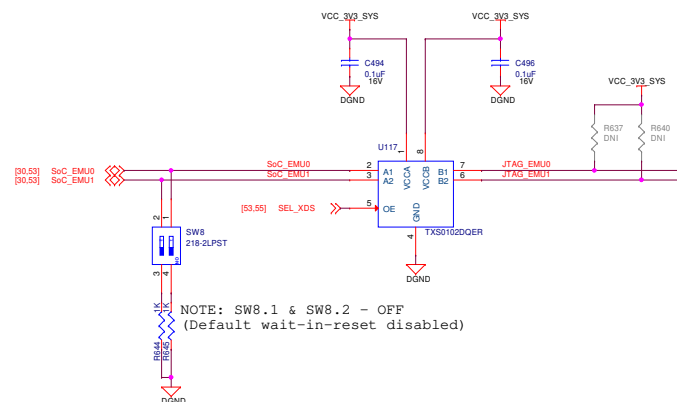
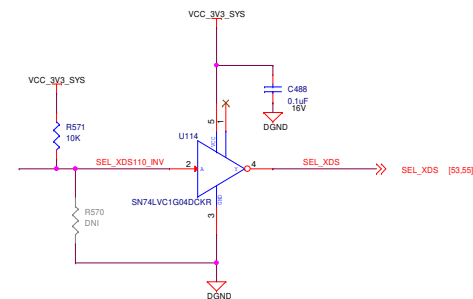
JTAG_TRSTn
JTAG_TUS
SEL_XDS10_INV [S3]
JTAG_EMU1

HDR 2X10
GNDN

R638
OE
GNDN

D-Note:
TRSTn is the reset to the JTAG logic. For normal operation, this is reset LOW, and thus the JTAG remains in reset as it is not being used. When a JTAG pod is connected, the pod will eventually drive this signal HIGH to release the JTAG logic from reset and enable a JTAG connection.

D-Note:
Add an external ESD protection to provide system level ESD protection, when the external connector is used for debugging. Follow the connectivity table for connecting the required pulls for the SoC JTAG interface. Add test points and external ESD protection when JTAG connector is not used.



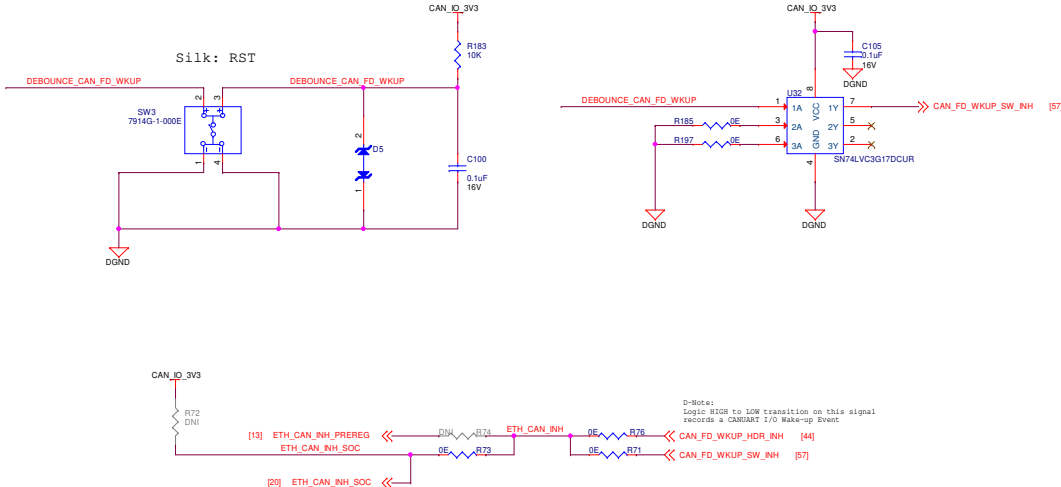
NOTE: SW8.1 & SW8.2 - OFF
(Default wait-in-reset disabled)

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CAN-FD FAST WAKE UP SW



MOUNTING HARDWARE

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled boards are wrapped in ESD Covers(individual) and packed securely before shipment.

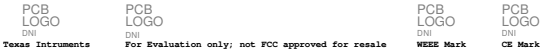
BARE PCB



AM62P SOCKET



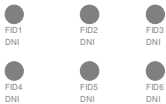
LOGOs



JUMPERS



FIDUCIALS



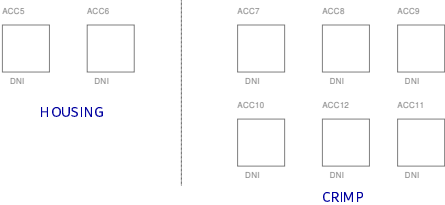
LABELS



SCREW & WASHER FOR PCIe M.2



HOUSING & CRIMP FOR DSI AND OLDI HEADER



D-Note:
Refer to the STRAP CONFIGURATION OF ETHERNET PHYS page from SK-AM64B schematics.

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Title ASSEMBLY NOTES AND MOUNTING HARDWARE

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