

# AM62A7 / AM62A3 LOW POWER STARTER KIT SK (EVM)

## WITH TPS65931211-Q1 PMIC

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#### Revision Number

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VER	1.1

#### D-Note :-

SK/EVM is a device evaluation board or platform. The SK/EVM is not a reference design. In some cases the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SOC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata, and TRM when designing their custom board. The information found in the datasheet should always take precedence over the SK/EVM implementation.

#### R-Note :-

- \* Verify the DNI components configuration with respect to the SK schematics (Use PDF) after completion of board design before board assembly
- \* A standard 5% tolerance resistor can be used for most of the series and parallel pull resistor
- \* Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build. (Refer FAQs listed for additional details)

### KEY LINKS TO COLLATERALS

<b>Hardware Design Guide :</b> <a href="https://www.ti.com/lit/an/sprad85/sprad85.pdf">https://www.ti.com/lit/an/sprad85/sprad85.pdf</a>
<b>Schematic Design and Review Checklist :</b> <a href="https://www.ti.com/lit/an/sprad21d/sprad21d.pdf">https://www.ti.com/lit/an/sprad21d/sprad21d.pdf</a>
<b>PMIC Power Solutions Application Note :</b> <a href="https://www.ti.com/lit/po/slvt204/slvt204.pdf">https://www.ti.com/lit/po/slvt204/slvt204.pdf</a>
<b>DDR Board Design and Layout Guidelines :</b> <a href="https://www.ti.com/lit/an/sprad66a/sprad66a.pdf">https://www.ti.com/lit/an/sprad66a/sprad66a.pdf</a>
SKs (Starter Kits) for reference : SK-AM62B, SK-AM62B-P1, SK-AM62-LP, SK-AM62-SIP, SK-AM62A-LP, SK-AM62P-LP

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REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	09 AUG 2023	Drafted from "PROC135E3_SCH" document.	Mistral Design Team	Nishant	Ajit MB
0.2	18 AUG 2023	Updated SoC, eMMC & PMIC Part Number	Mistral Design Team	Nishant	Ajit MB
1.0	21 AUG 2023	Baselined and Released	Mistral Design Team	Nishant	Ajit MB
1.1	11 JUNE 2024	Updated SoC Pin name (VMON_VSYS), Enabled Voltage ratings for all the capacitors and added Design Review notes  Moved to DNI : C33, C36, C291, C177, R272, U56, Y1  Moved to Mount : C556, R295, R296, R297, R299, R300, R301, R302, R303, R505, R534  C290 - 1uF changed to 2.2uF; C288,C184,C181,C39 - 1uF changed to 0.1uF; C45,C42 - 9pF changed to 18pF; C182,C179 - 2.2uF changed to 1uF; C40 - 4.7uF changed to 1uF; C38 - 0.1uF changed to 4.7uF  R350 - 2.2K changed to 10K; R125,R135 - 3.4K_1% changed to 3.48K_1%; R343 - 22E changed to 0E; R315,R242,R371 - 49.9K_1% changed to 10K; R368 - 10K_1% changed to Std 10K; R311 - 100K changed to Std 10K; R342,R341,R586,R584 - 22E_1% changed to 0E; R331,R344,R328 - 499E_0.1% changed to 499_1%; R451 - 10K changed to 47K; R351,R611 - 11K_1% changed to 10K_1%.	Mistral Design Team		

LINKS TO KEY FAQs

<a href="https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1203305/faq-am62a7-and-am62a7-q1-custom-board-hardware-design-collaterals-to-get-started">https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1203305/faq-am62a7-and-am62a7-q1-custom-board-hardware-design-collaterals-to-get-started</a>
<a href="https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1203441/faq-am62a3-and-am62a3-q1-custom-board-hardware-design-collaterals-to-get-started">https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1203441/faq-am62a3-and-am62a3-q1-custom-board-hardware-design-collaterals-to-get-started</a>
<a href="https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1306030/faq-am62p-am62p-q1-custom-board-hardware-design--faq-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit">https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1306030/faq-am62p-am62p-q1-custom-board-hardware-design--faq-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit</a>
<a href="https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1340905/faq-am62a7-am62a7-q1-am62a3-am62a3-q1---custom-board-hardware-design---guidelines-for-reuse-of-sk-am62a-lp-schematics">https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1340905/faq-am62a7-am62a7-q1-am62a3-am62a3-q1---custom-board-hardware-design---guidelines-for-reuse-of-sk-am62a-lp-schematics</a>
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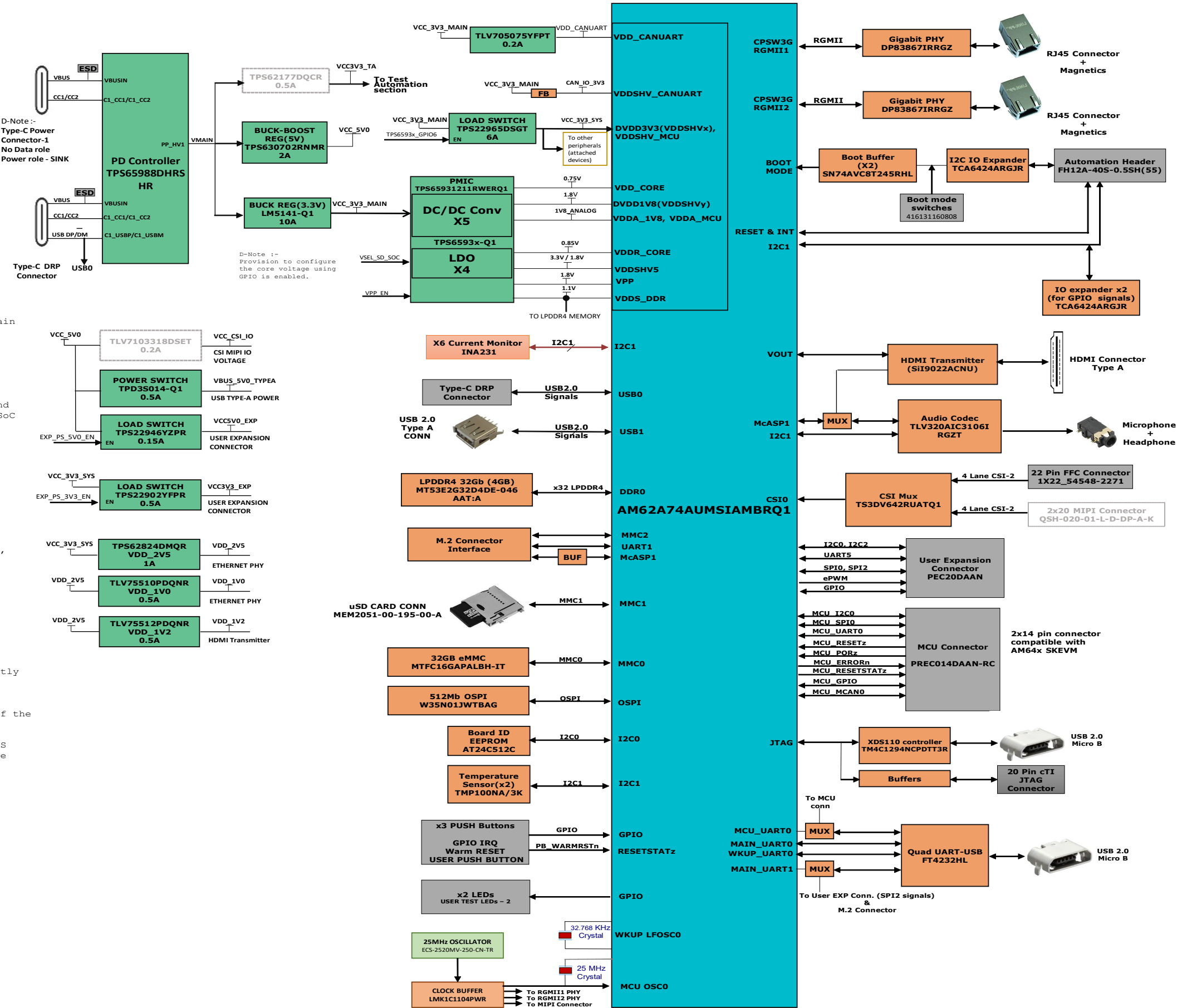
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# BLOCK DIAGRAM SK-AM62A-LP

D-Note :-  
Pins (OBSCLK) D17 and R20 of the SoC are main domain Observation clock output for test and debug purposes only.  
Add a TP near to the SoC and provision to isolate the signal for testing whenever possible  
Pin (MCU\_OBSCLK) C11 of the SOC are MCU Domain Observation clock output for test and debug purposes only. Add a TP near to the SoC and provision to isolate the signal for testing whenever possible.

D-Note :-  
Refer Device Comparison section of the processor data sheet for supported cores, peripherals and memory size

D-Note :-  
Drive strength configuration is currently not supported.  
The drive strength must remain in the default state since this is the only condition used during timing closure of the peripherals.  
The devices are set to maximum drive strength. Please reference to the IBIS model to find the drive strength of the IOs.



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Title BLOCK DIAGRAM AM62A\_ SKEVM

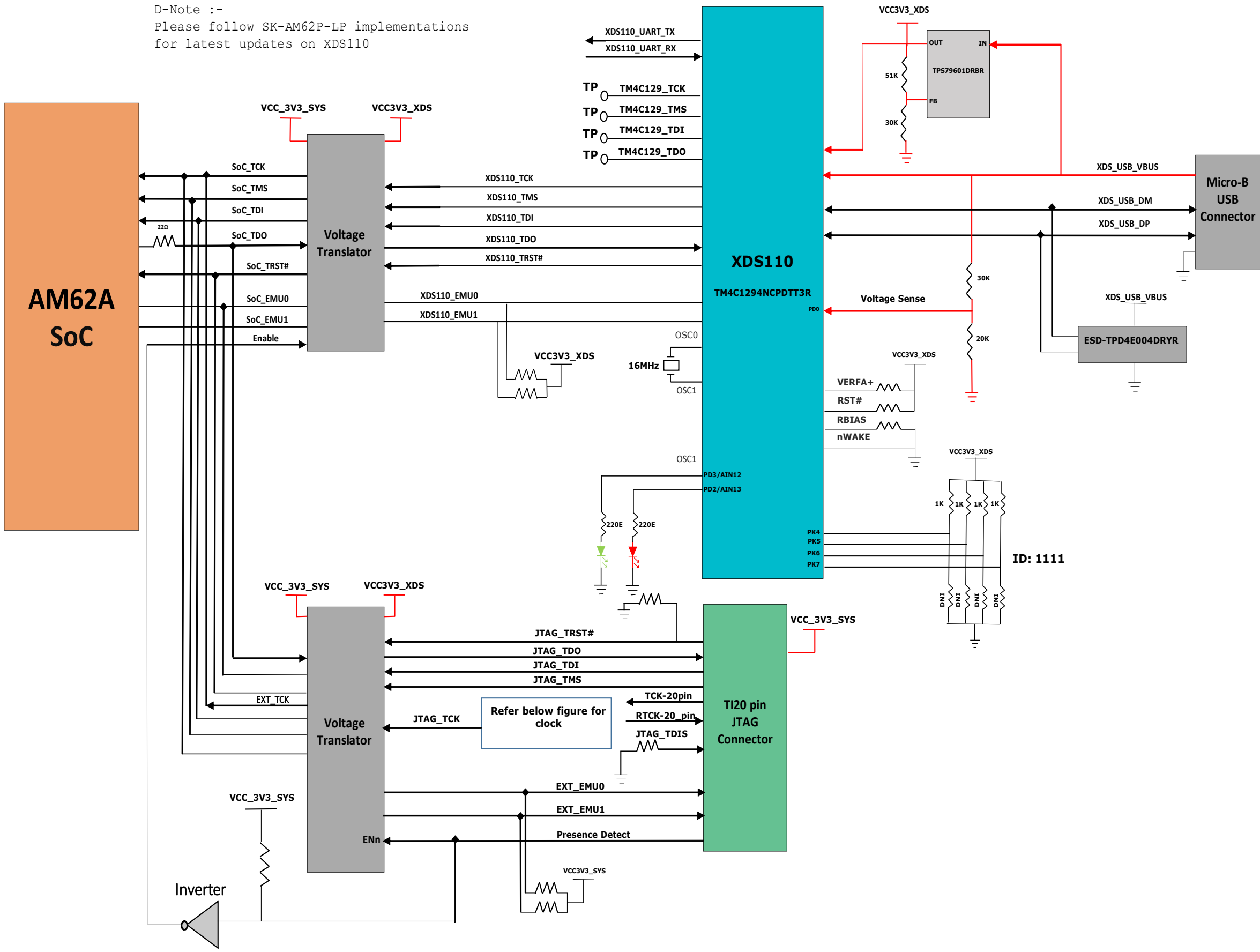
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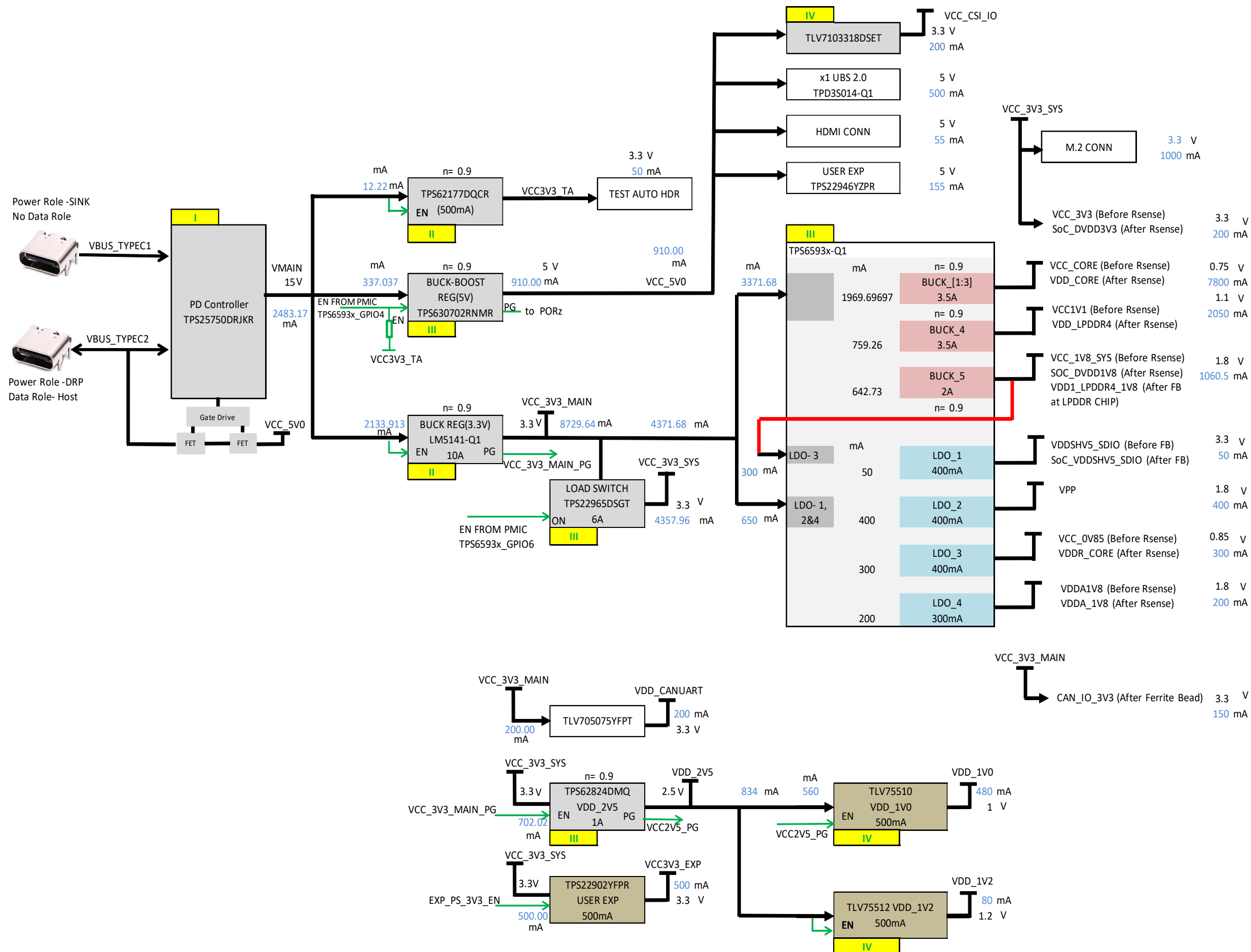
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Rev A

BLOCK DIAGRAM\_XDS110

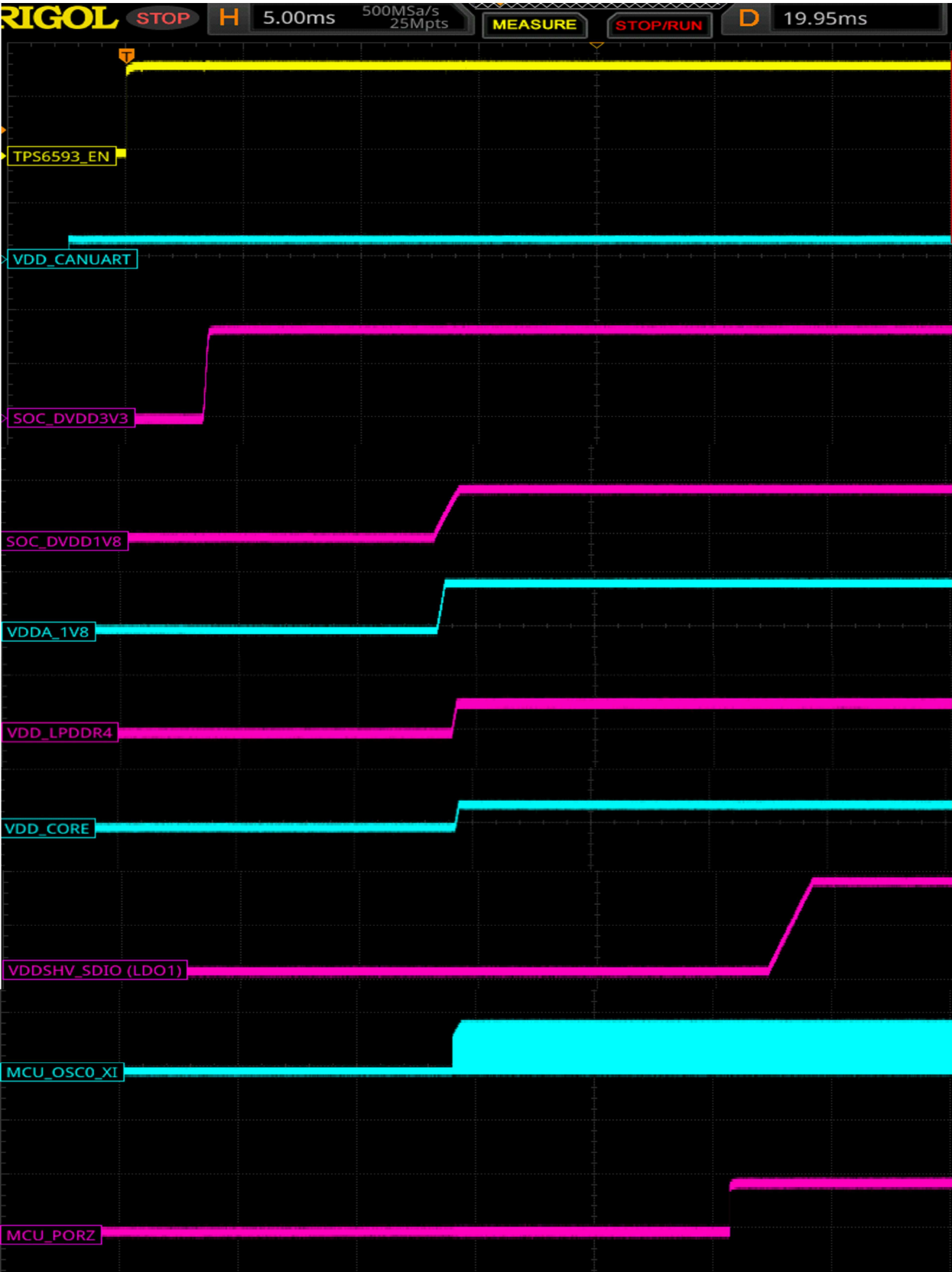


## POWER BLOCK DGM





POWER SEQUENCE



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Title POWER SEQUENCE

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Rev A

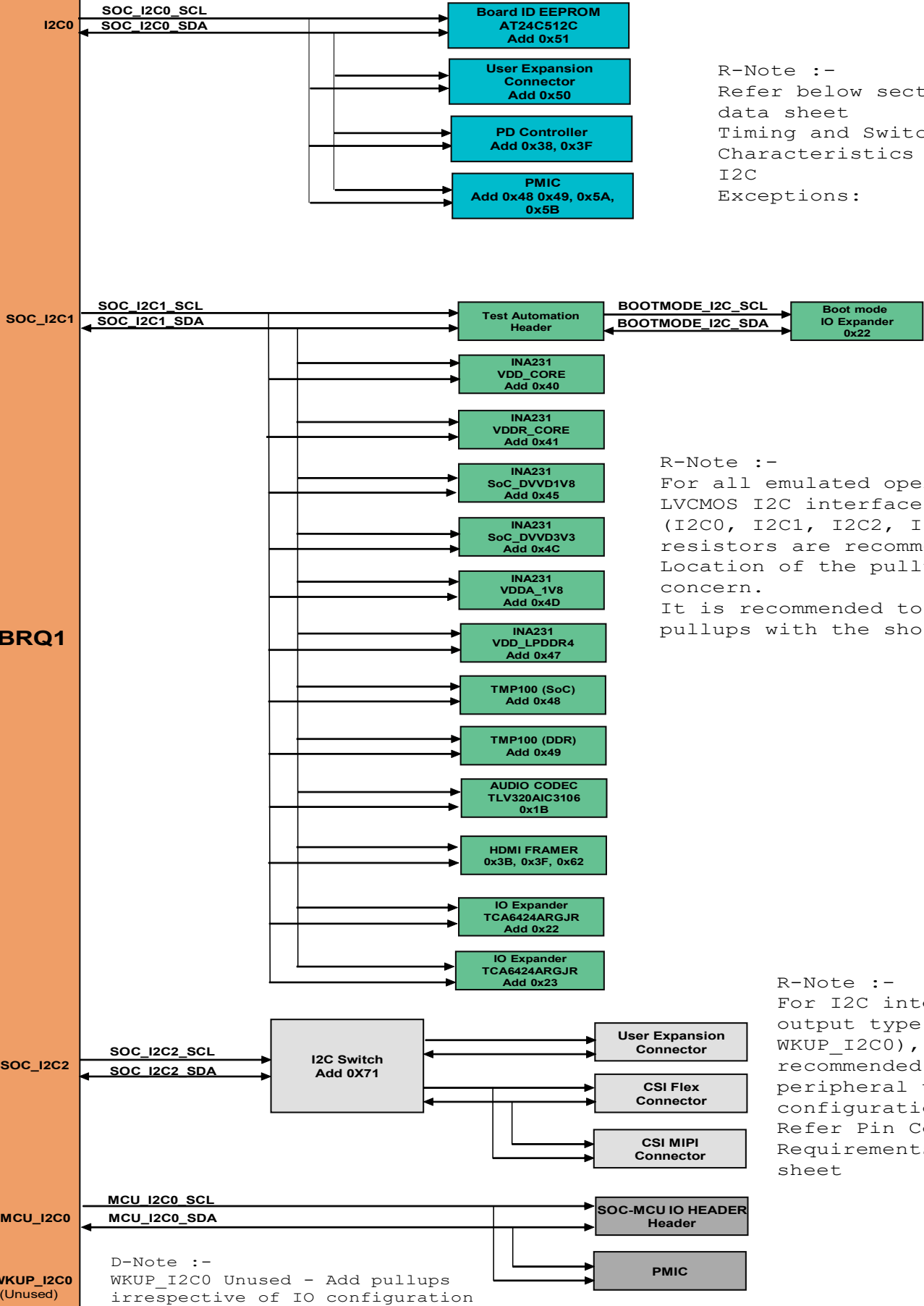
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I2C TREE

R-Note  
Add - Indicates  
Address

AM62A74AUMSIAMBRQ1  
SoC



R-Note :-  
Refer below section of the SOC  
data sheet  
Timing and Switching  
Characteristics  
I2C  
Exceptions:

R-Note :-  
For all emulated open-drain output  
I<sup>2</sup>C interfaces.  
(I2C0, I2C1, I2C2, I2C3) pullup  
resistors are recommended  
Location of the pullup is not a  
concern.  
It is recommended to connect the  
pullups with the shortest possible stub

R-Note :-  
For I2C interfaces with open-drain  
output type buffer (MCU\_I2C0 and  
WKUP\_I2C0), an external pullup is  
recommended irrespective of  
peripheral usage and IO  
configuration.  
Refer Pin Connectivity  
Requirements section of SOC data  
sheet

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Title		I2C TREE	
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GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE RAIL CONNECTED ON SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC	ENABLE	MCU_GPIO0_0	MCU_SPIO_CS0	OUTPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	MCU Header GPIO0_16	MCU_GPIO0_16	GPIO	MCU_GPIO0_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
7	MCU Header GPIO0_15	MCU_GPIO0_15	GPIO	MCU_GPIO0_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
8	PMIC Interrupt	PMIC_INT_B	INTERRUPT	GPIO0_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV3	SoC_DVDD3V3
9	CAN-FD fast wake up signal from switch	CAN_FD_WKUP_SW_INH	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
10	CAN-FD fast wake signal from MCU header	CAN_FD_WKUP_HDR_INH								
11	Interrupt signal from Automotive Ethernet ADD-ON board	CPSW_ETH2_INH								
12	User test LED control signal	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	Watchdog trigger input signal for Watchdog Trigger mode	PMIC_WDOG_TRIGG	ENABLE	MCU_GPIO0_19	WKUP_I2C0_SCL	INPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
14	WKUP Signal from RGMII2	CPSW_ETH2_WAKE	INTERRUPT	MCU_GPIO0_20	WKUP_I2C0_SDA	INPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
15	User EXP Conn GPIO	EXP_GPIO1_22	GPIO	GPIO1_22	UART0_CTSn	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	GPIO1_23	UART0_RTSn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
17	User Interrupt									
18	User EXP Conn GPIO	EXP_GPIO0_14_LT	GPIO	GPIO0_14	OSPI0_CSn3	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
19	PMIC Standby Disable	PMIC_LPM_EN0	ENABLE	MCU_GPIO0_22	PMIC_LPM_EN0	OUTPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
20	User EXP Conn GPIO	EXP_EHRPWM1_B	GPIO	GPIO1_10	MCASP0_AXR0	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 01										
1	Ethernet Daughter Card plug in detect	RGMII2_BRD_CONN_DET	DETECTION	IO EXPANDER-P00		INPUT	HIGH	LOW		VCC_3V3_SYS
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P01		OUTPUT	HIGH	LOW		VCC_3V3_SYS
3	M.2 module Bluetooth LDO Enable	BT_EN_SOC	ENABLE	IO EXPANDER-P02		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	NA	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P06		OUTPUT	LOW	HIGH		VCC_3V3_SYS
8	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
9	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	IO EXPANDER-P10		OUTPUT	HIGH	LOW		VCC_3V3_SYS
10	eMMC Reset control GPIO	GPIO_EMMC_RSTn	RESET	IO EXPANDER-P11		OUTPUT	HIGH	LOW		VCC_3V3_SYS
11	SOC UART1 Mux Select	UART1_FET_BUF_EN	ENABLE	IO EXPANDER-P12		OUTPUT	HIGH	LOW		VCC_3V3_SYS
12	BT UART WKUP Signal	BT_UART_WAKE_SOC_3V3	INTERRUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER-P14		OUTPUT	HIGH	LOW		VCC_3V3_SYS
14	Raspberry Pi Camera CSIO GPIO1	CSI_GPIO0	INPUT/OUTPUT	IO EXPANDER-P15		NA	NA	NA		VCC_3V3_SYS
15	Raspberry Pi Camera CSIO GPIO2	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER-P16		NA	NA	NA		VCC_3V3_SYS
16	WLAN Alert Interrupt	WLAN_ALERTn	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC_3V3_SYS
19	MCASP1 Enable and Direction Control	MCASP1_FET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
20		MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
21		MCASP1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	-		VCC_3V3_SYS
22		UART1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P25		OUTPUT	HIGH	-		VCC_3V3_SYS
23	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	INTERRUPT	IO EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_SYS
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER – 02										
1	SoC SPI0 MUX Selection	SPIO_FET_SEL	CONTROL	IO EXPANDER-P20		OUTPUT	LOW	-		VCC_3V3_SYS
2	SoC SPI0 MUX Enable	SPIO_FET_OE	ENABLE	IO EXPANDER-P21		OUTPUT	LOW	LOW		VCC_3V3_SYS
3	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	CSI flex and mipi MUX Selection	CSI_SEL2	CONTROL	IO EXPANDER-P23		OUTPUT	HIGH	-		VCC_3V3_SYS
5	CSI MUX Enable	CSI_EN	ENABLE	IO EXPANDER-P24		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
6	Auto PHY mode config	AUTO_100M_1000M_CONFIG	CONTROL	IO EXPANDER-P25		OUTPUT	NA	NA		VCC_3V3_SYS
7	CSI I/O Voltage Select(VCC_CSI_IO)	CSI_VLDO_SEL	CONTROL	IO EXPANDER-P26		OUTPUT	LOW	-		VCC_3V3_SYS
8	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	Wilink Enable	WL_LT_EN	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
10	CSI Reset Control GPIO	CSI_RSTz	RESET	IO EXPANDER-P11		OUTPUT	LOW	LOW		VCC_3V3_SYS

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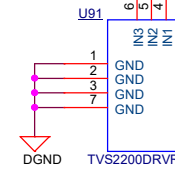
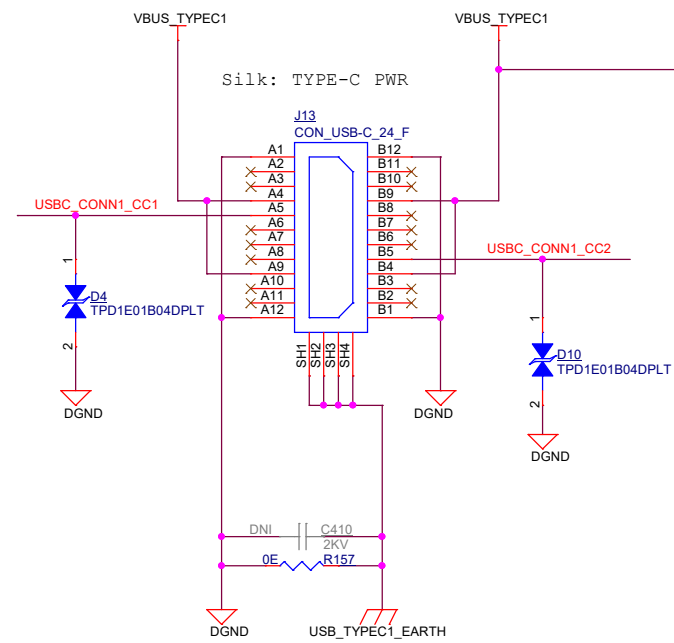


Title GPIO MAPPING TABLE

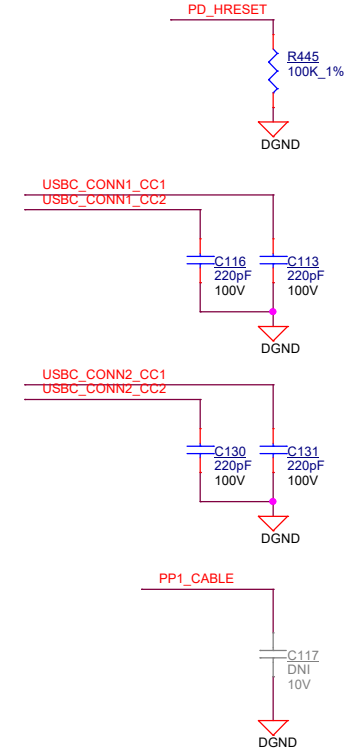
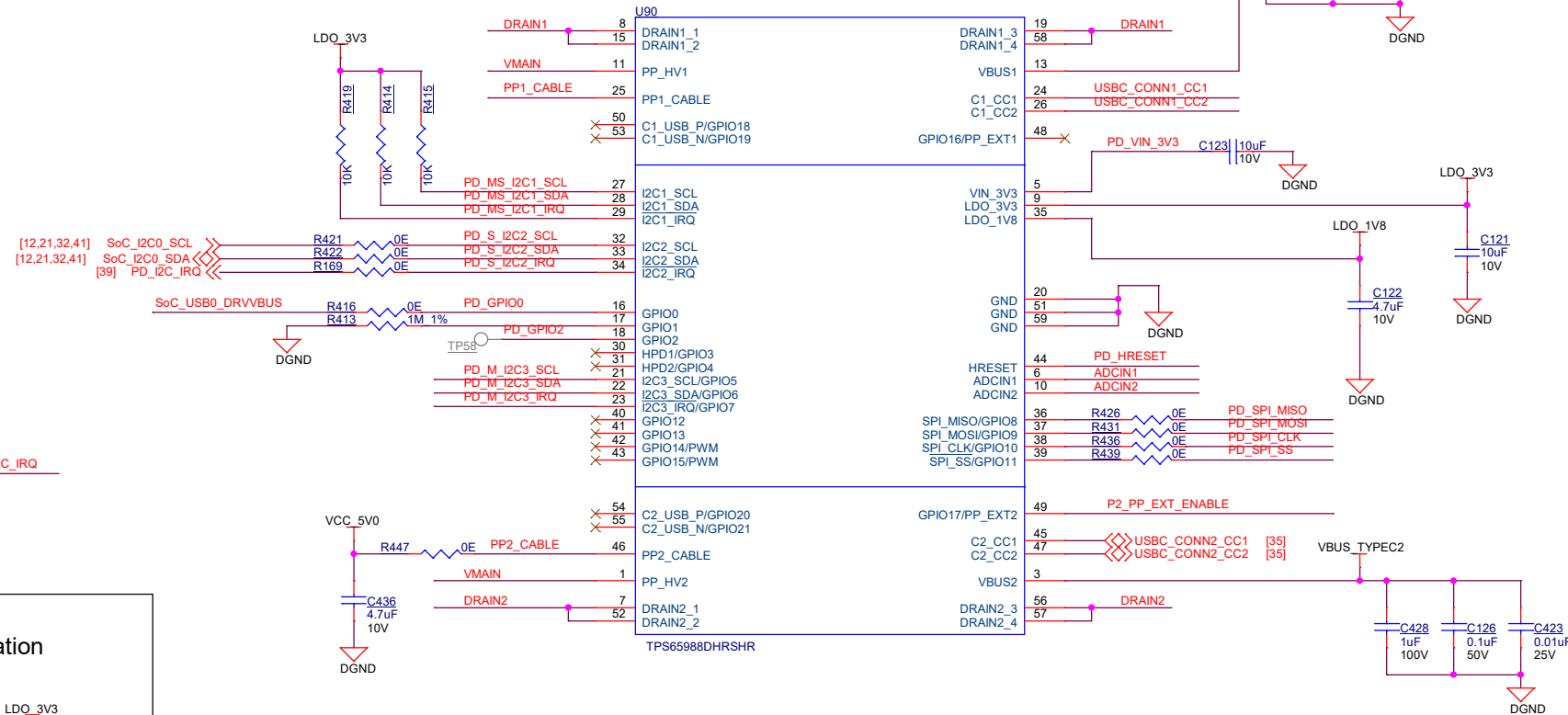
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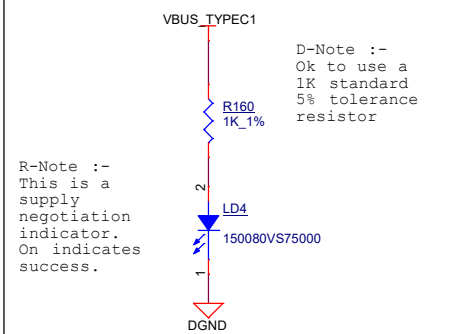
## USB TYPE-C PD CONTROLLER AND POWER SUPPLY



## TYPE-C DUAL PD CONTROLLER

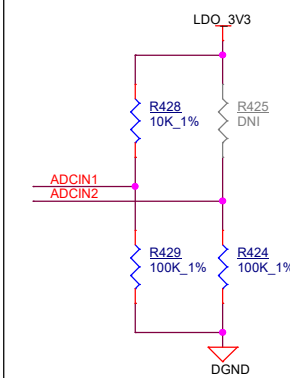


**POWER INDICATION LED: VBUS\_TYPEC1**

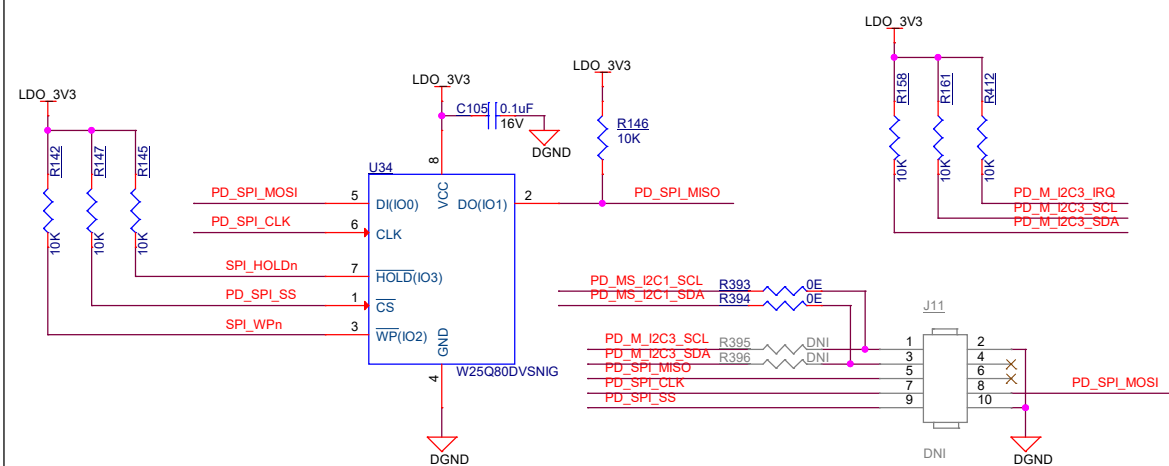


I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

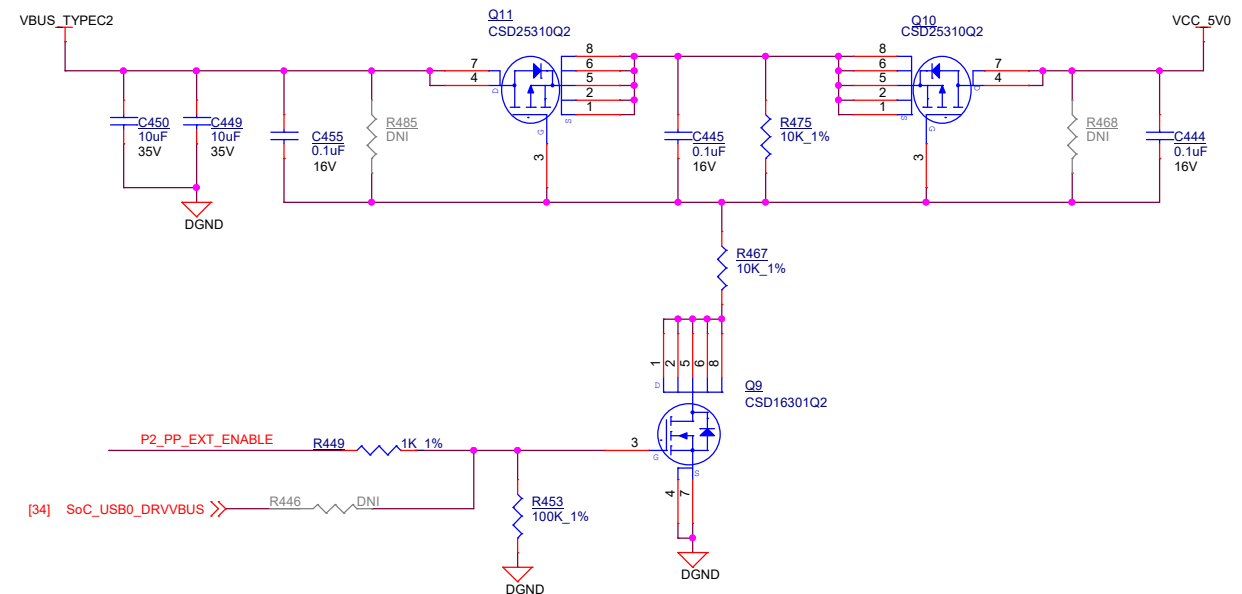
BP\_NoWait  
Safe Configuration



## SPI EEPROM & PROGRAMMING HEADER



## EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



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Title	USB TYPE-C
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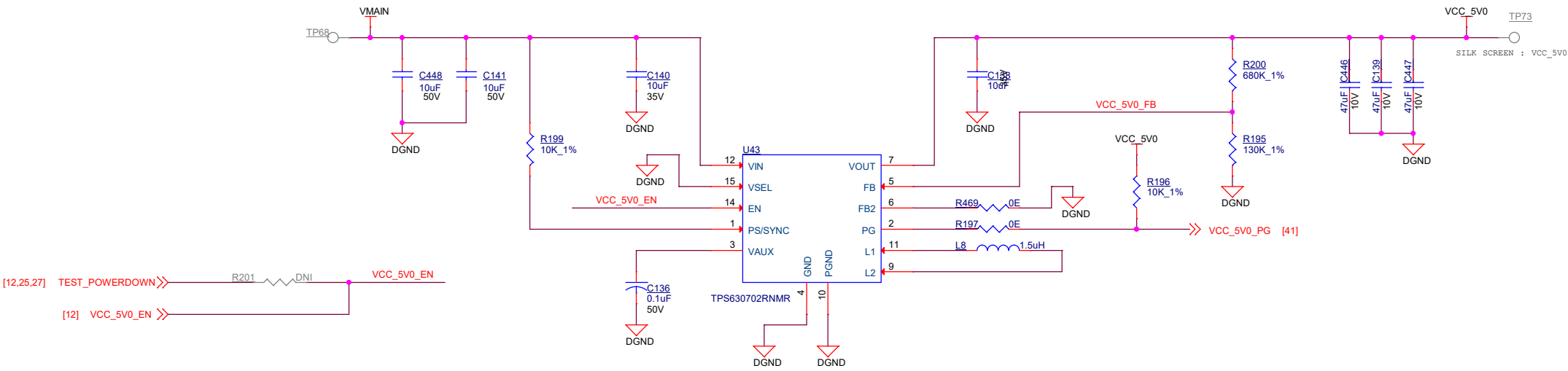
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PERIPHERAL POWER SUPPLIES - 1

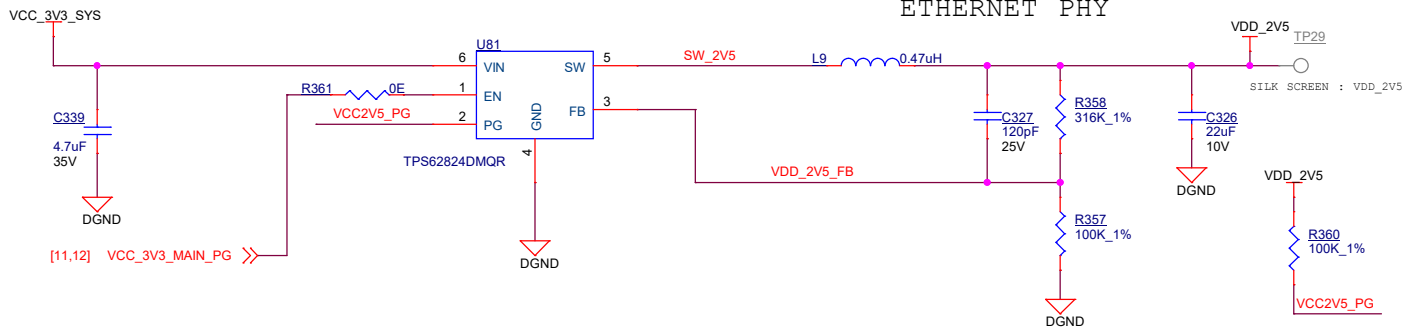
VinMin = 4.5V  
VinMax = 15V  
Vout = 5V @ 2A

D-Note :-  
Add a Jumper or OR for isolation  
or Current measurement for  
preproduction board



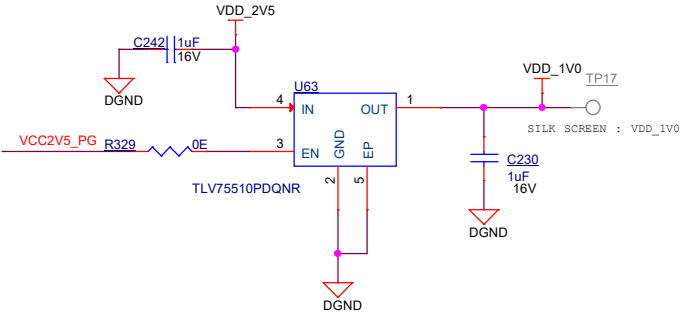
2.5V, 1.0 AMP SUPPLY

ETHERNET PHY



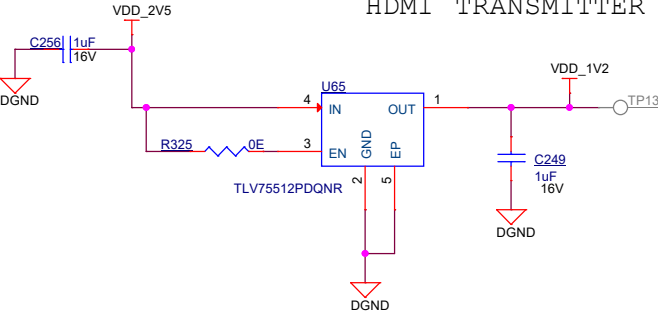
PERIPHERAL SUPPLY - ETHERNET PHY

1.0V, 0.5 AMP SUPPLY



1.2V, 0.5 AMP SUPPLY

HDMI TRANSMITTER



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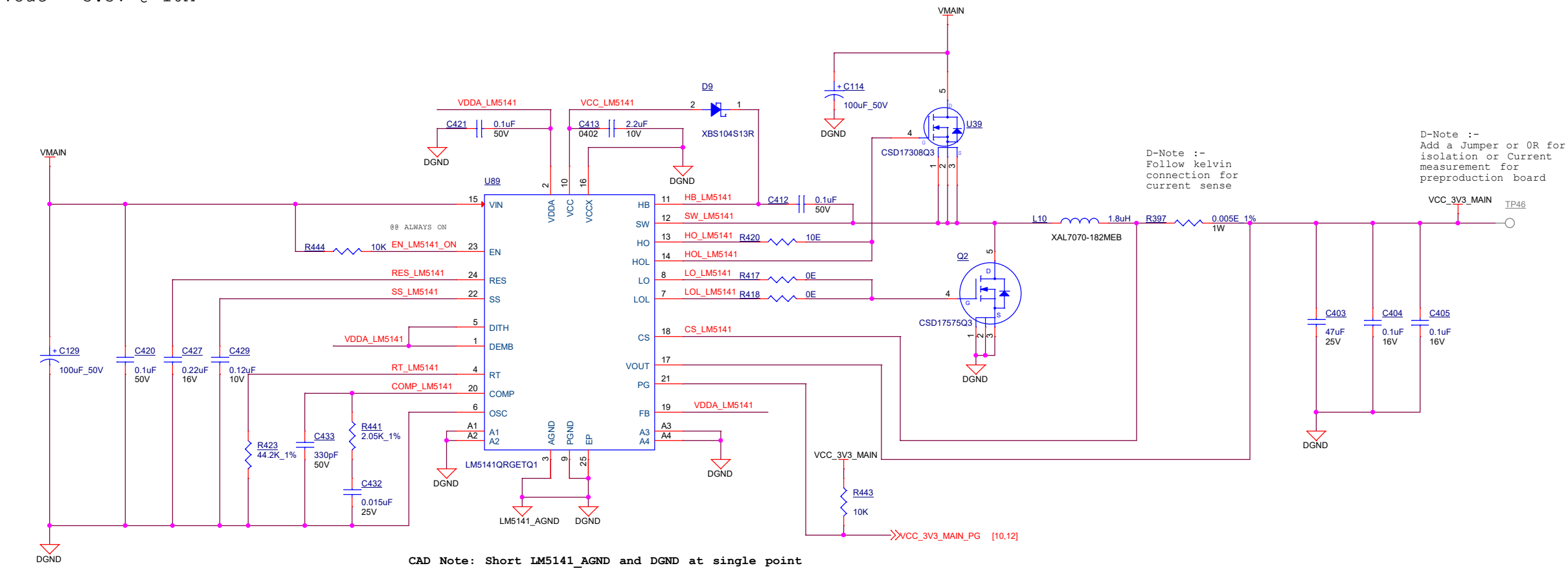
Title PERIPHERAL POWER SUPPLY -1

Size	Rev
C	A
Date:	Tuesday, June 11, 2024
Sheet	10 of 44

# PERIPHERAL POWER SUPPLIES - 2

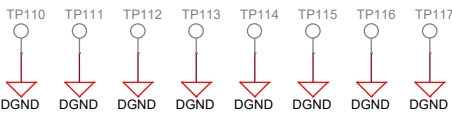
3.3V, 10.0 AMPS SUPPLY

VinMin = 4.5V  
VinMax = 15V  
Vout = 3.3V @ 10A



[33] ETH\_CAN\_INH\_PREREG >> DNI R81 EN\_LM5141\_ON

## GND TEST POINTS



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Title PERIPHERAL POWER SUPPLY-2

Size C  
PROC135A

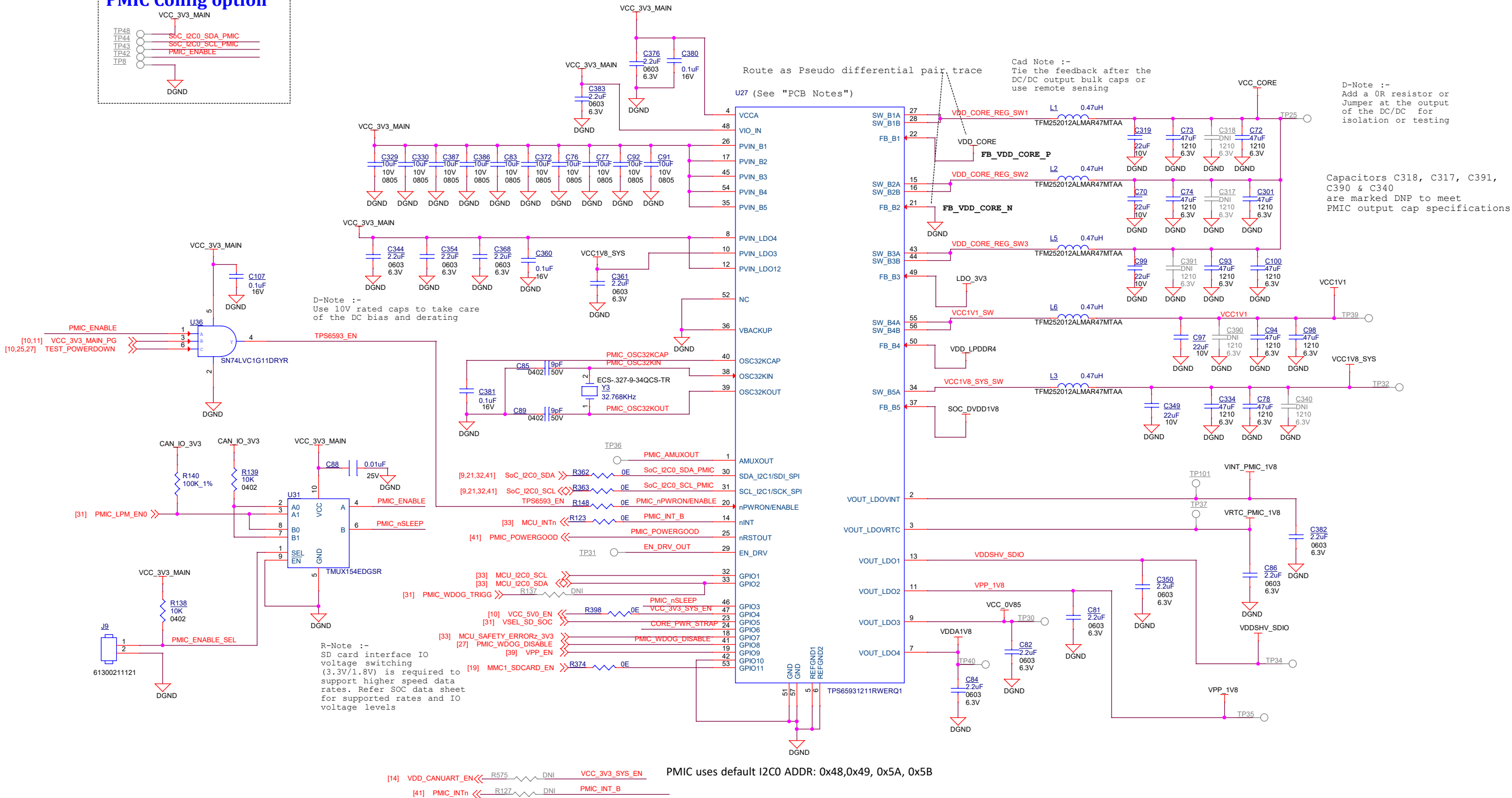
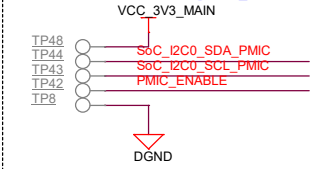
Date: Tuesday, June 11, 2024

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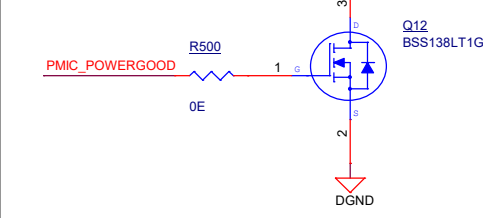
# SOC POWER SUPPLY PMIC

## PMIC Config option

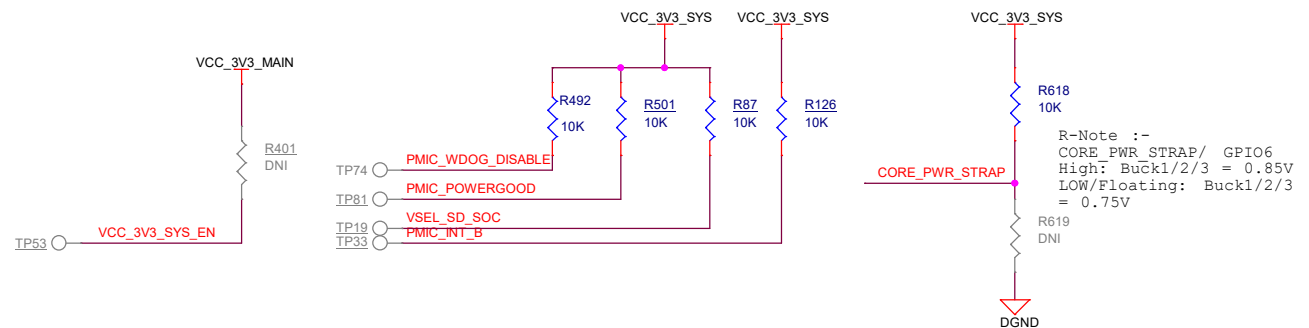
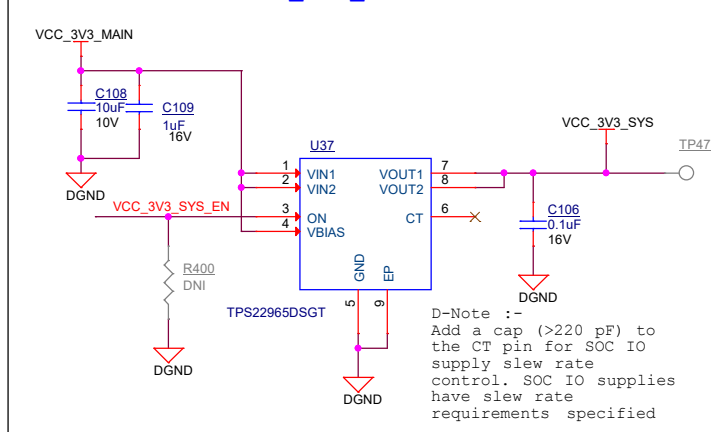


PMIC uses default I2C0 ADDR: 0x48, 0x49, 0x5A, 0x5B

## POWER INDICATION LED



## VCC\_3V3\_SYS LOAD SWITCH



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Title SOC POWER SUPPLY PMIC

Size PROC135A

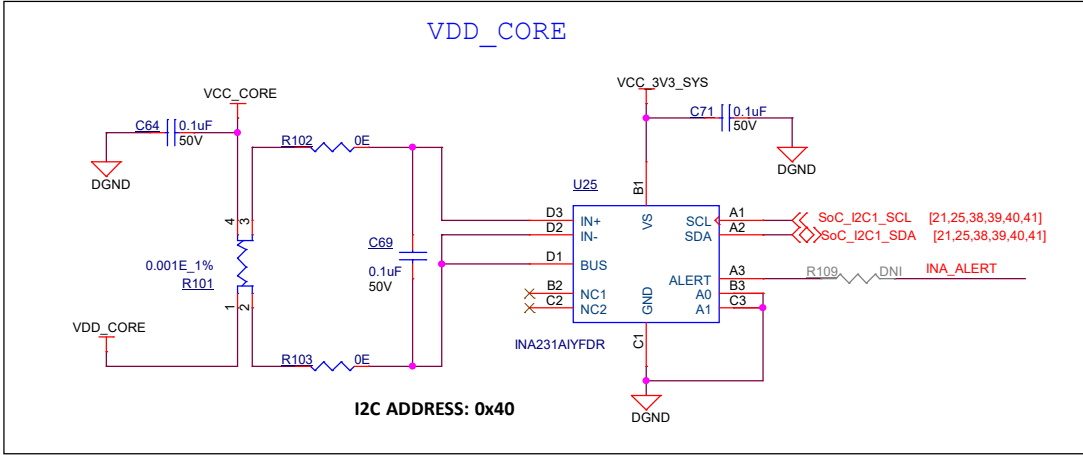
C

Date: Tuesday, June 11, 2024

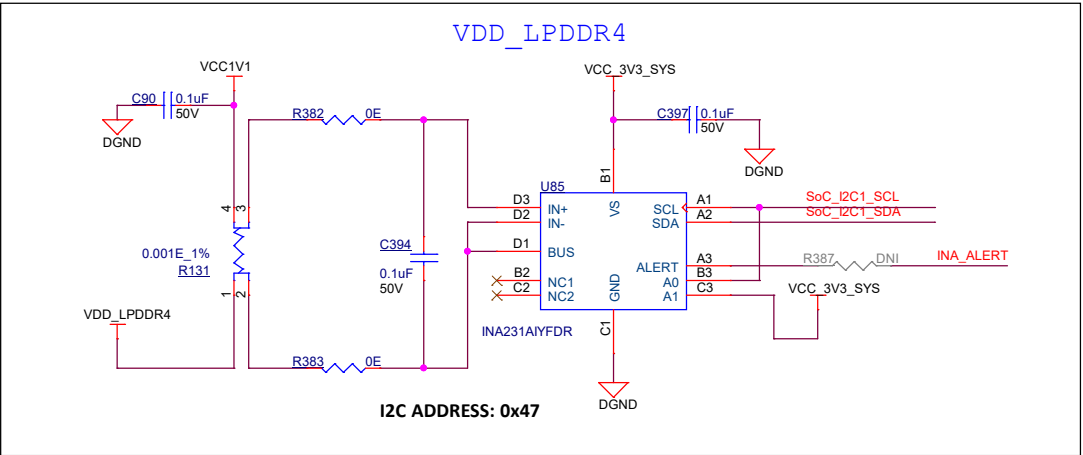
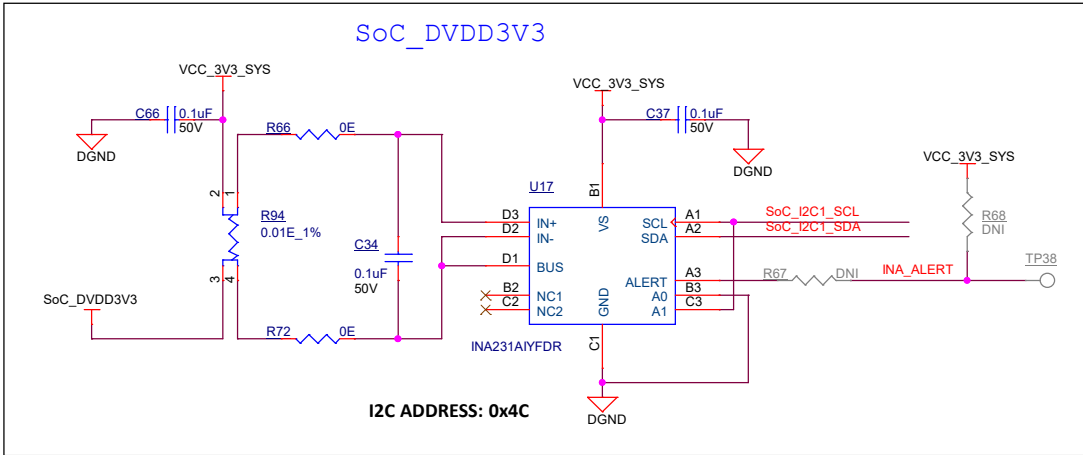
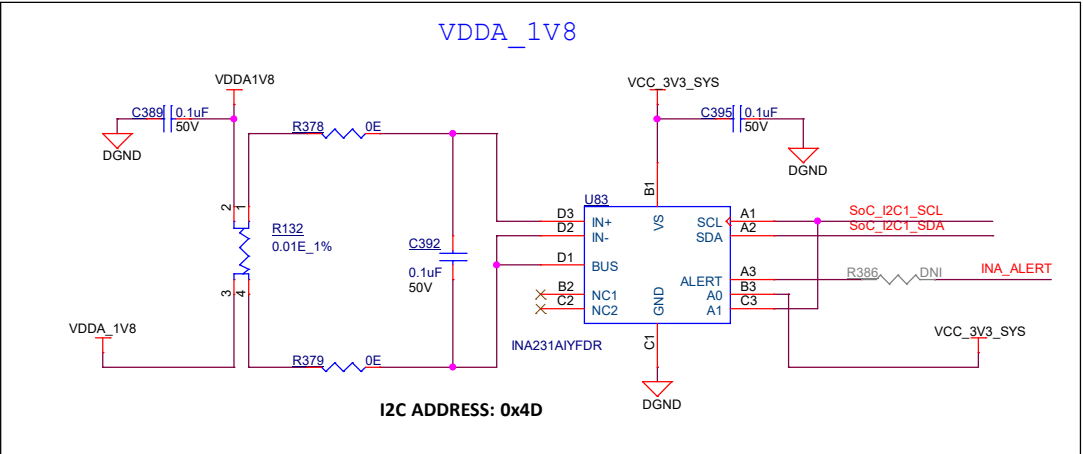
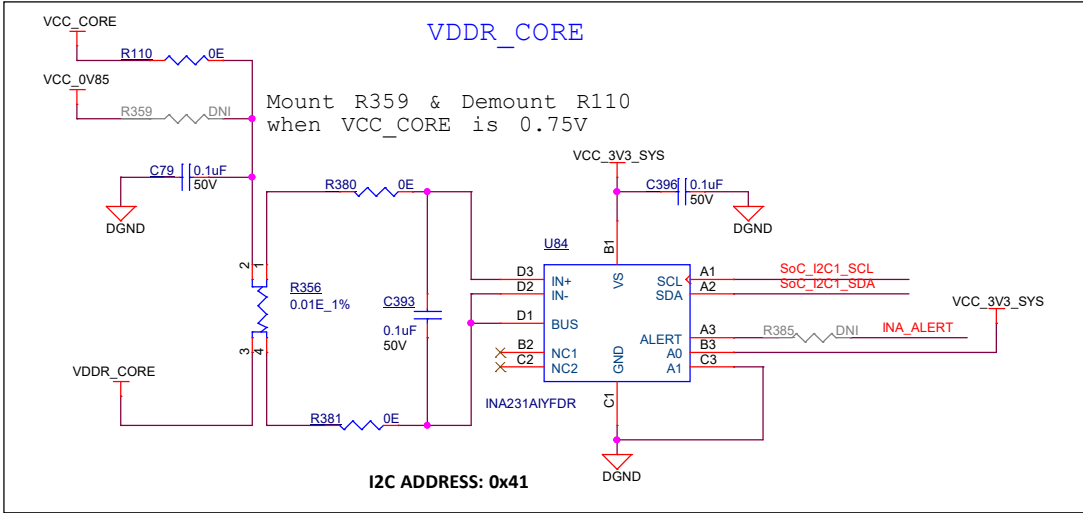
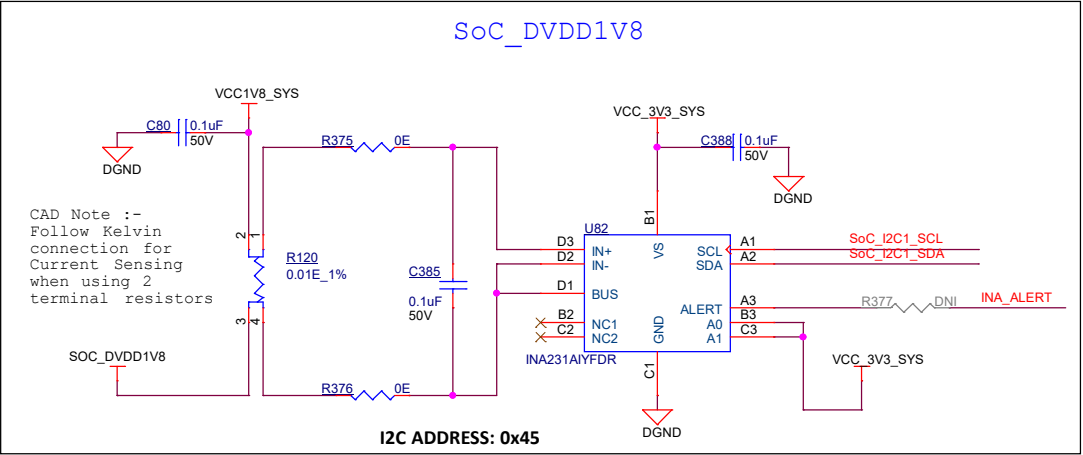
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# CURRENT MONITORING DEVICES



D-Note :-  
Note the supply rail name change across  
the shunt when optimizing the design  
(Deleting the current sense resistor)



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

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Title CURRENT MONITORING DEVICES

Size  
C PROC135A

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SOC POWER

D-Note :-  
Recommend implementing the voltage monitoring functionality using VMON\_VSYS for early detection of supply failure. It is meant to be a power-fail indicator for the main input (higher) voltage rail that enters the PCB. For example, 5, 12, or 24 volts. The error associated with this monitor would require you to set the threshold significantly lower than the nominal to avoid false trigger. Refer System Power Supply Monitor Design Guidelines section of the data sheet

D-Note :-  
Changing the core voltage is not allowed after the device has been released from reset. If you turn off the core supply, we expect you to turn off all power rails and ramp them down per the power-down sequence and wait until all supply rails decay below 300mv before turning on power again

D-Note :-  
VDD\_CORE and VDDR\_CORE are recommended to be powered by the same source so they ramp together when VDD\_CORE is operating at 0.85V\_

D-Note :-  
Add a filter cap. Refer SOC data sheet section System Power Supply Monitor Design Guidelines

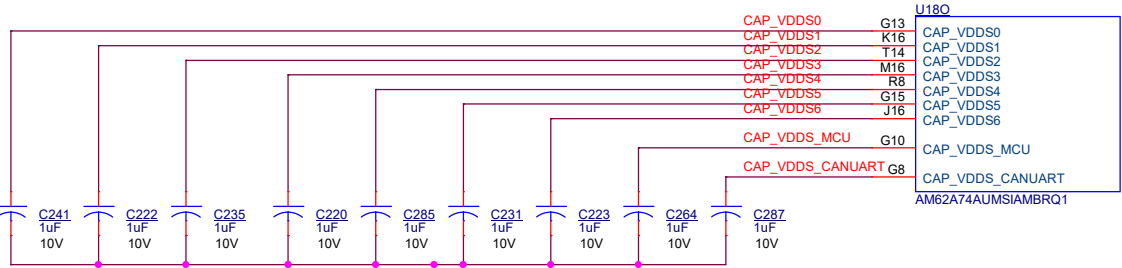
D-Note :-  
Connecting 1.8V supply source directly to VPP continuously is not allowed

D-Note :-  
It is very important to select an LDO with very fast transient response and connect its output to the VPP pin with a low loop inductance path to ensure it is able to source the high transient load, where the VPP pin never drops below the minimum operating voltage.

D-Note :-  
Refer Pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies (analog and core) when CSIO interface is not used  
Ferrite and Bulk Caps are optional when CSIO is not used and Boundary scan functionality is required

R-Note :-  
Reserved pins Leave unconnected

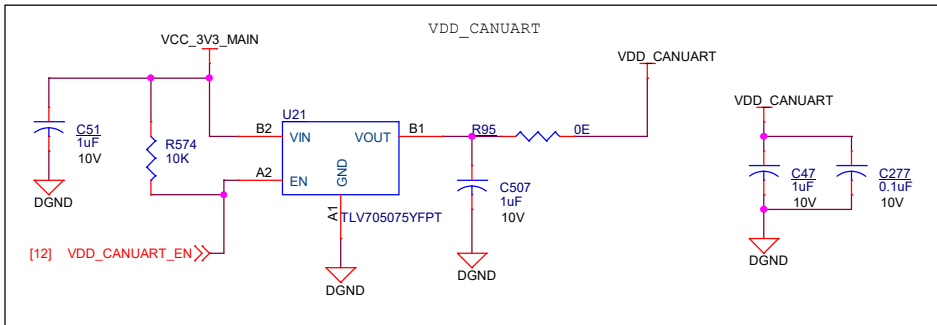
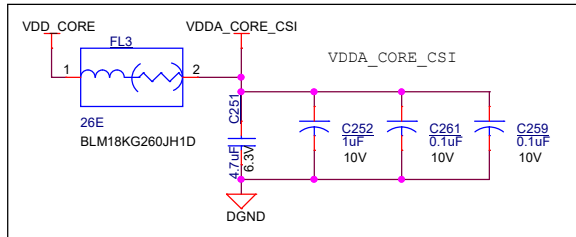
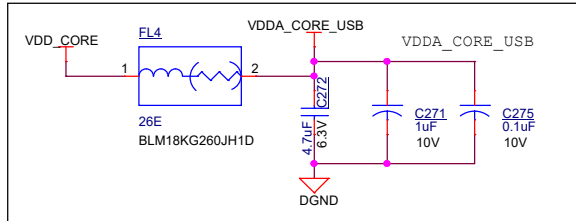
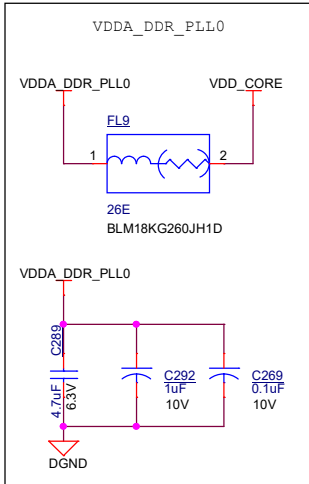
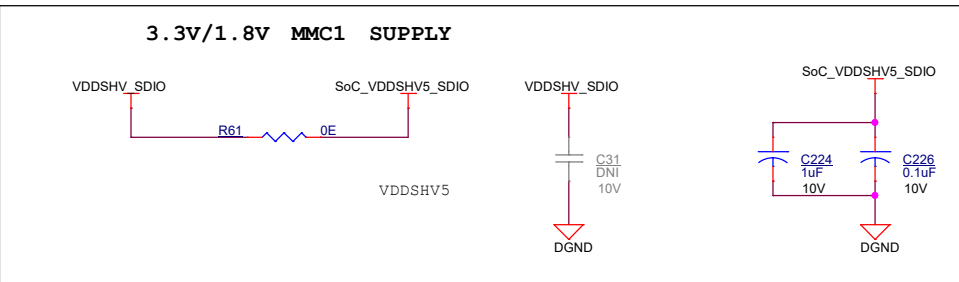
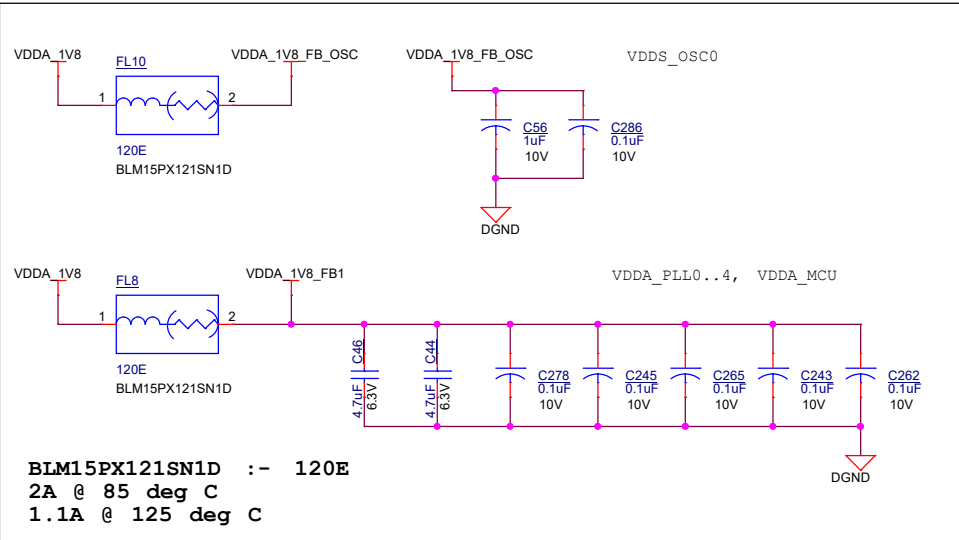
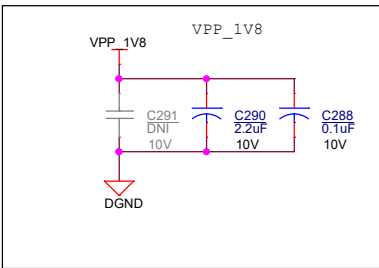
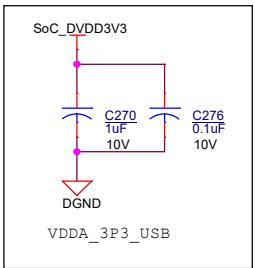
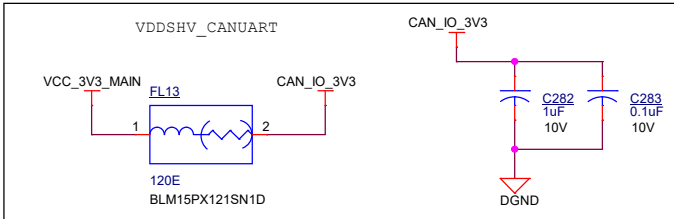
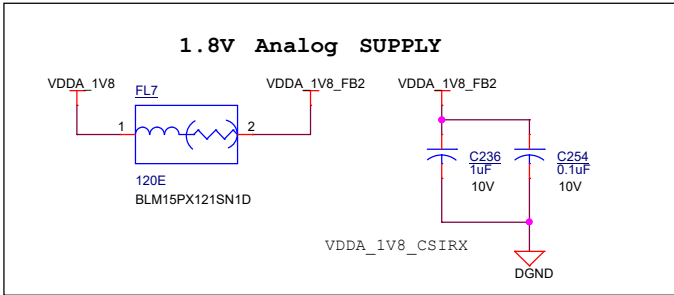
D-Note :-  
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized any time and the USB calibration procedure does not happen. Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.



D-Note :-  
Select capacitor with ESR < 1 Ohm  
Ensure the PCB loop inductance is < 2.5 nH  
Select 0201 package or smallest possible package  
Refer SOC Data sheet

D-Note :-  
Common SOC LVCMOS IO interface guidelines  
1. Most of the SOC IOs are not fail-safe. No input should be applied before supply ramps.  
2. SOC LVCMOS inputs have minimum slew rate requirements specified  
3. SOC IO buffers are off during Reset. A pull is required near to the attached device being driven by the SOC IOs  
4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull.  
When adding pull is not feasible, ensure the traces are routed away from noisy signals

D-Note :-  
A Trace connected to SOC is effectively an antenna that will pick up noise. A potential will be generated on the signal when noise couples into the antenna. This potential will be largest on the signal when the highest impedance end of the signal. By placing a pull-up or pull-down near the SoC pin, we force the highest potential to the open-circuit end of the signal rather than the SoC end of the signal.



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Title SOC POWER

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PROC135A

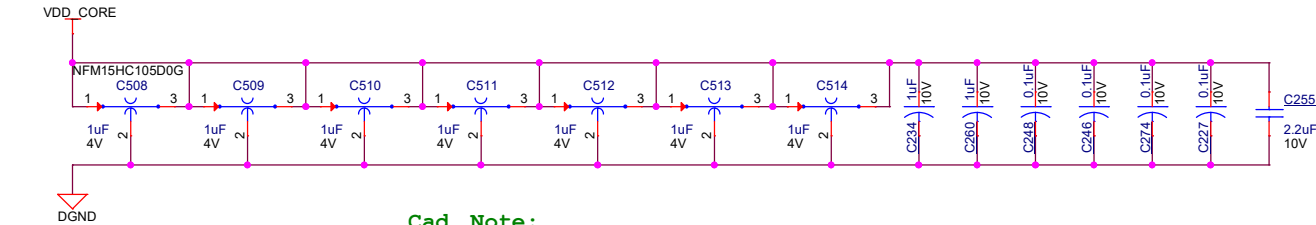
Date: Tuesday, June 11, 2024

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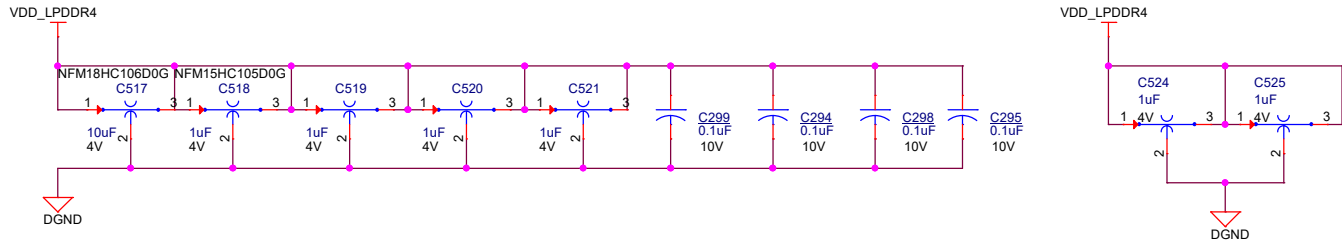
Rev A



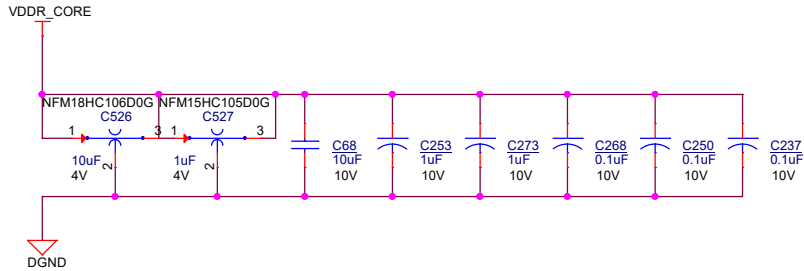
SOC POWER SUPPLIES - DECAPS



Cad Note:  
Place 0.1 uF caps near to SoC pins



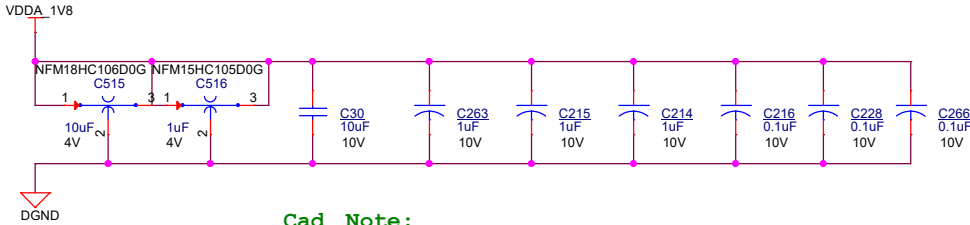
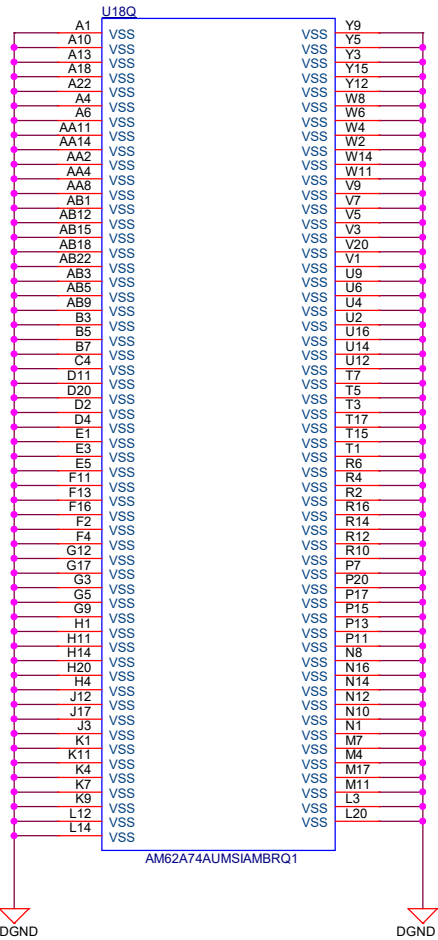
Cad Note:  
Place 0.1 uF caps near to SoC pins



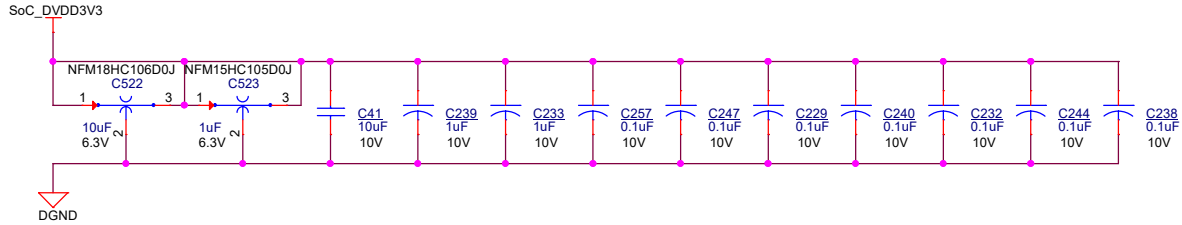
Cad Note:  
Place 0.1 uF caps near to SoC pins

R-Note :-  
Use of 3 terminal caps optimizes  
use of bulk caps and minimizes the  
PCB inductance

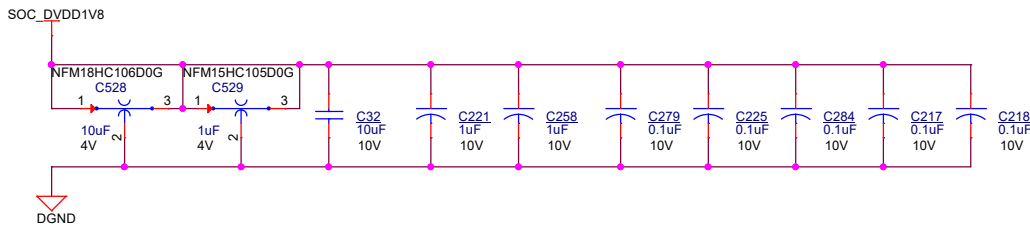
SOC VSS



Cad Note:  
Place 0.1 uF caps near to SoC pins



Cad Note:  
Place 0.1 uF caps near to SoC pins



Cad Note:  
Place 0.1 uF caps near to SoC pins

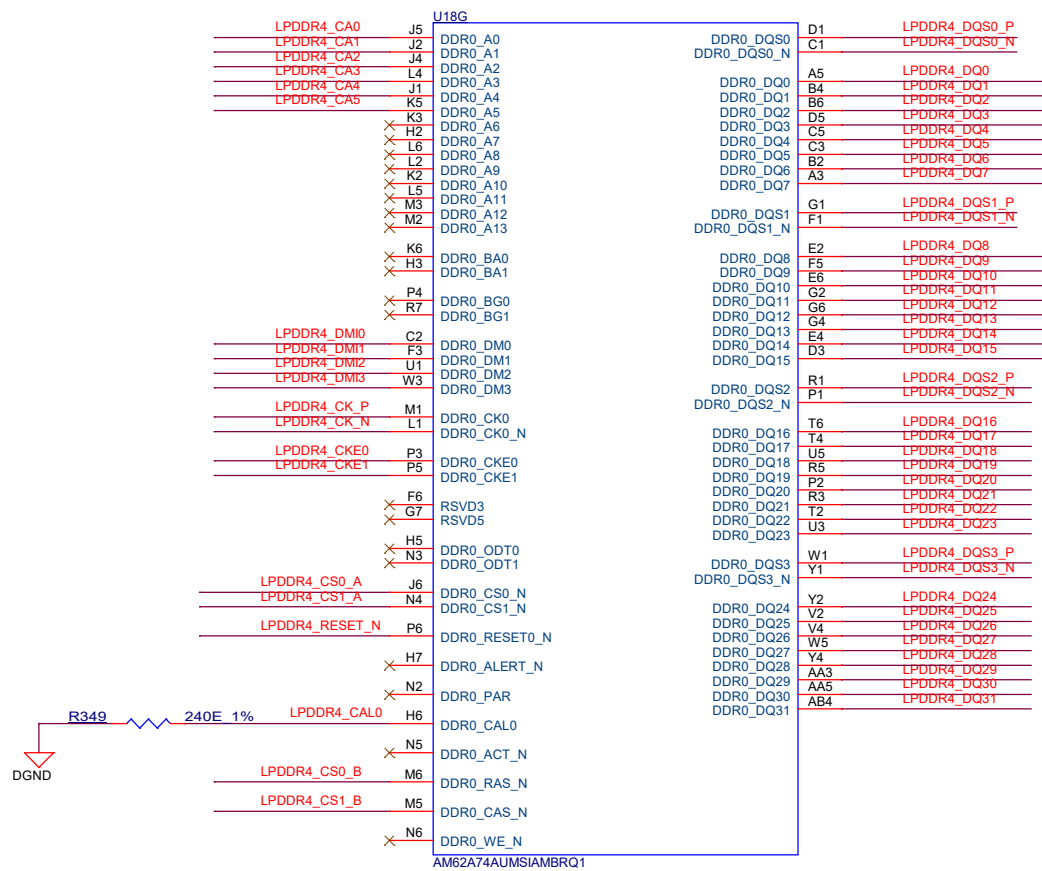
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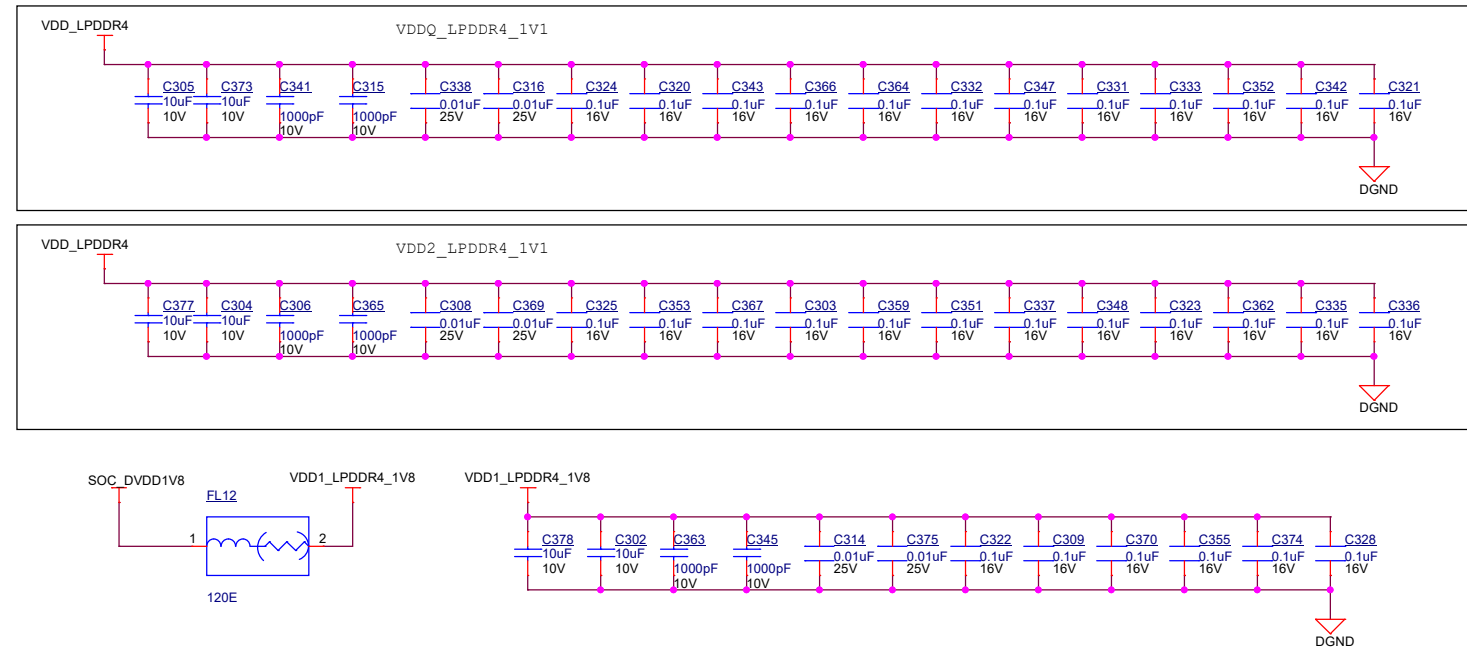
Title SOC POWER CAPS & SOC VSS

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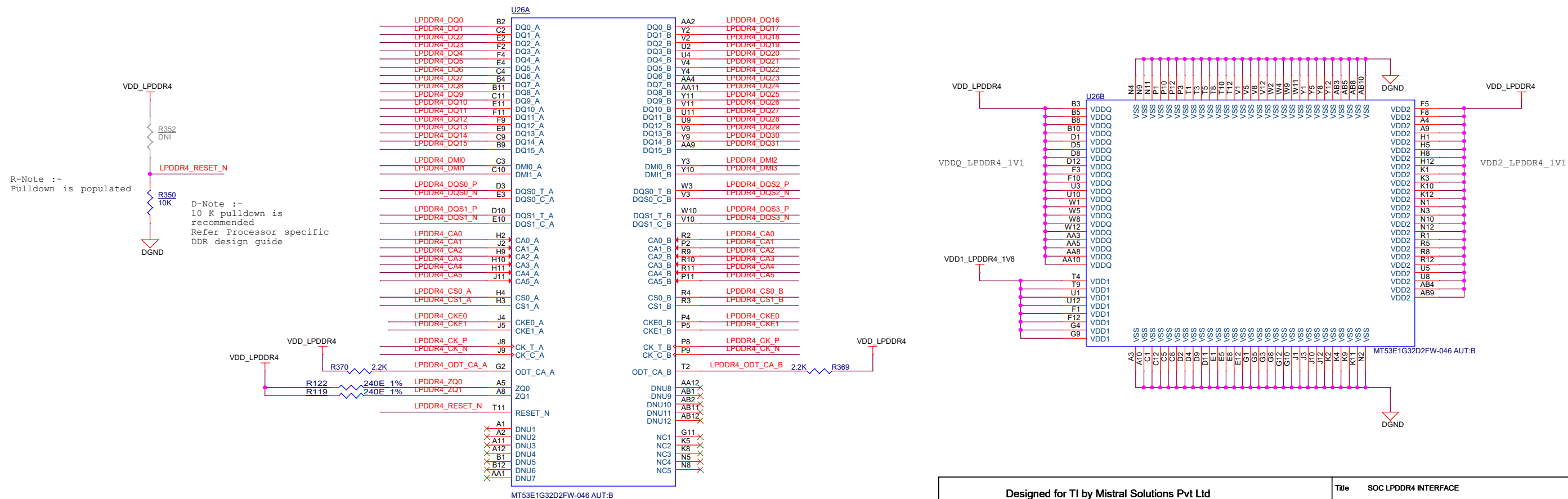
# SOC LPDDR4 INTERFACE



## LPDDR4 POWER DECAPS



## LPDDR4 DEVICE



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Title SOC LPDDR4 INTERFACE

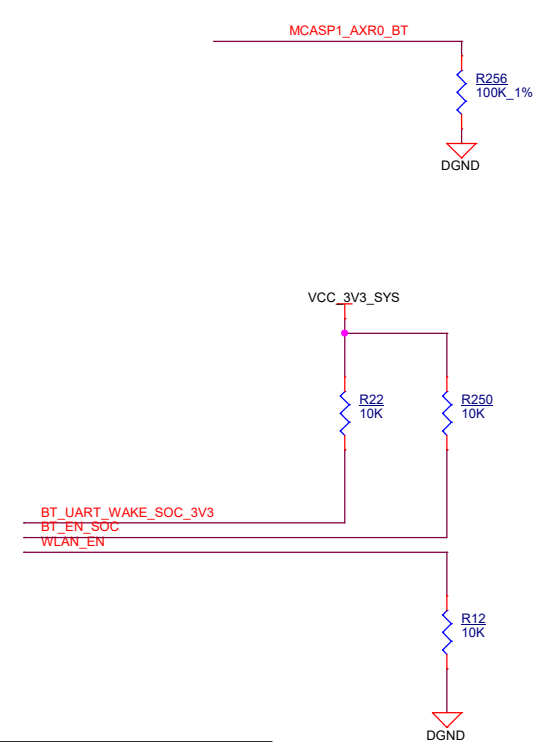
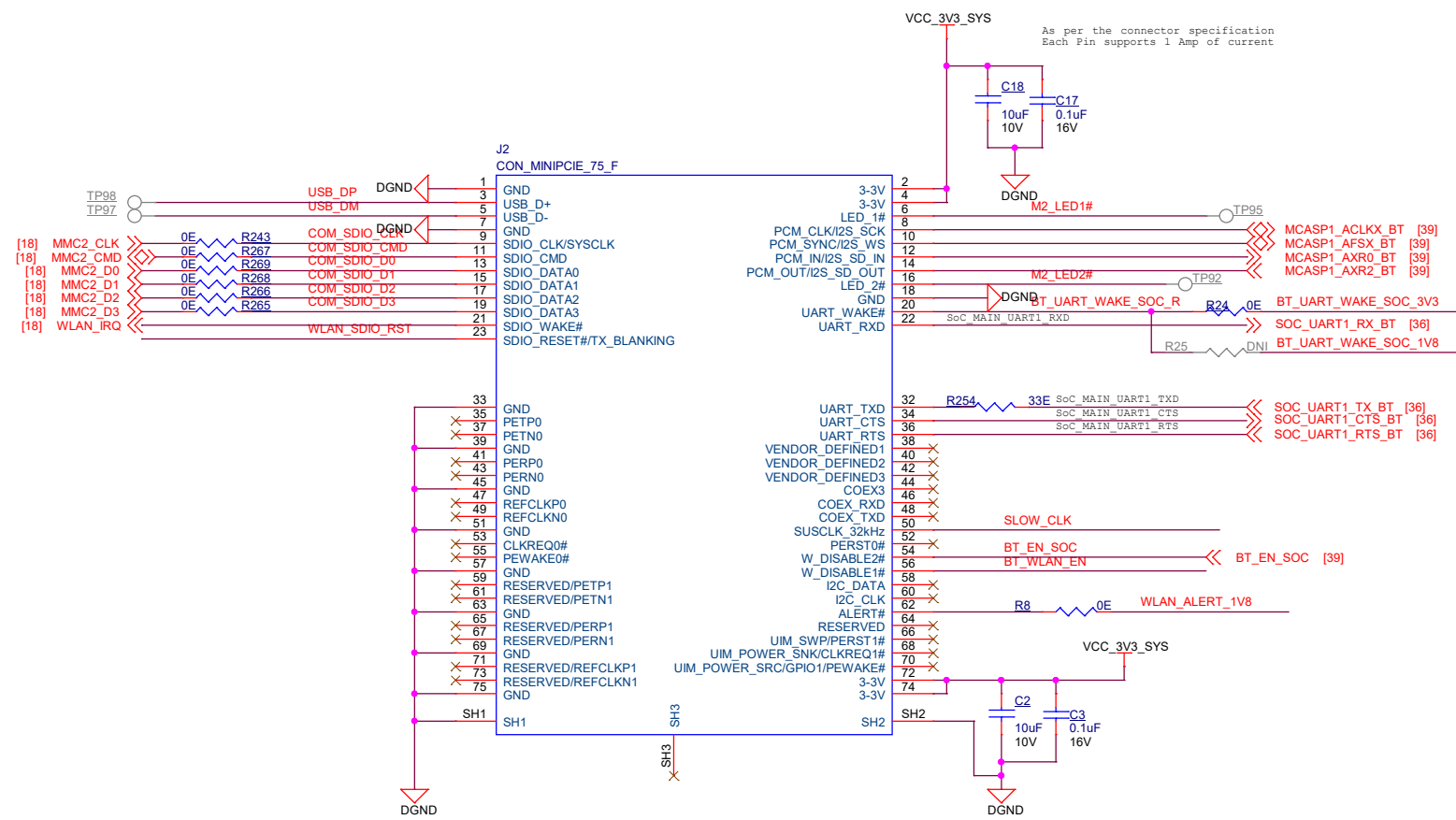
Size  
C PROC135A

Date: Tuesday, June 11, 2024

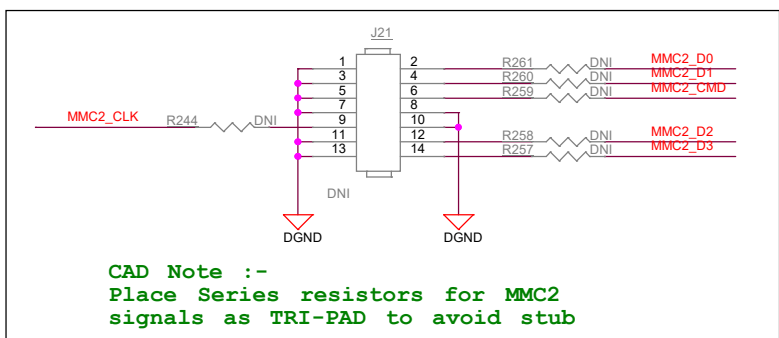
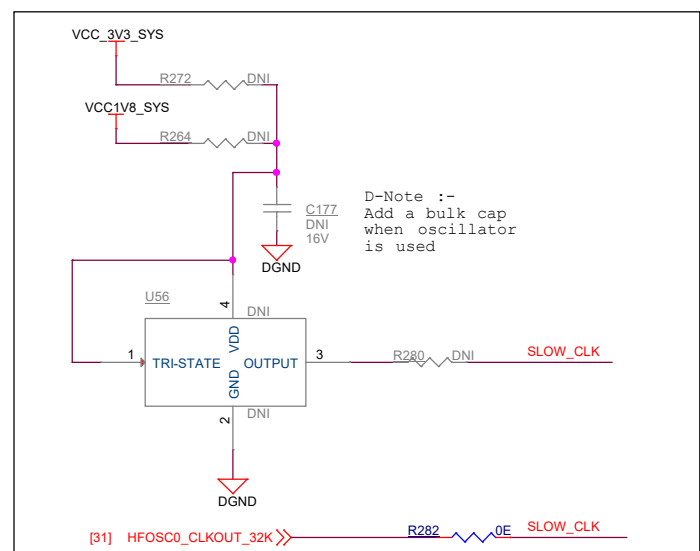
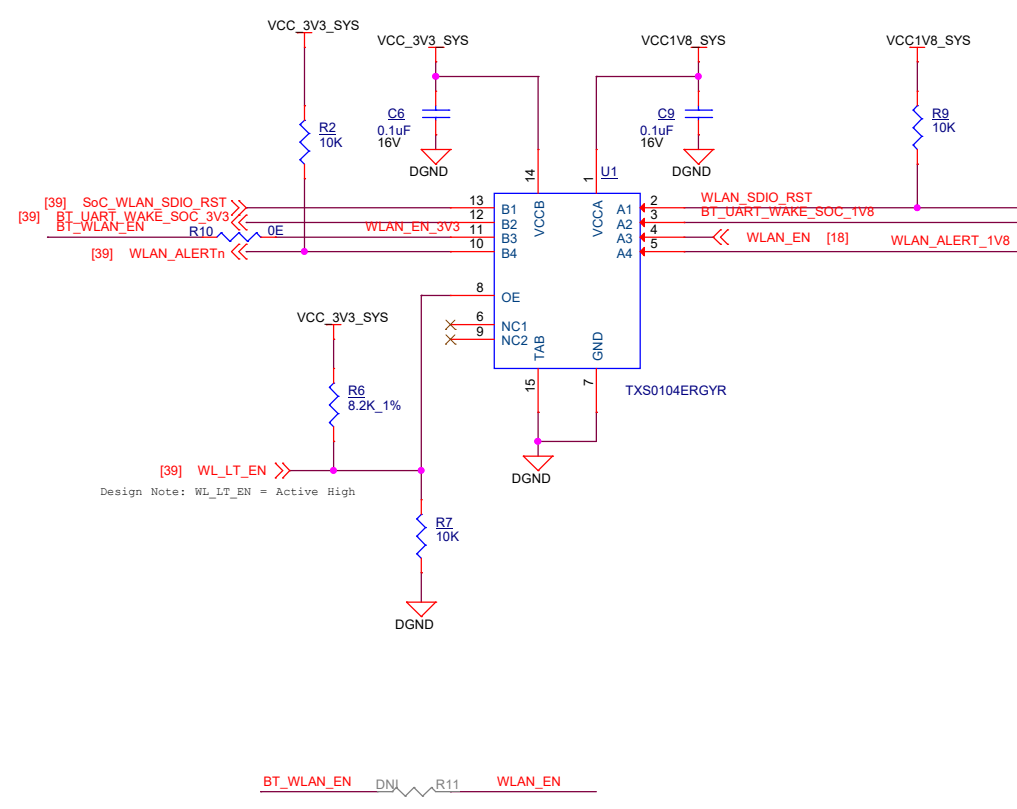
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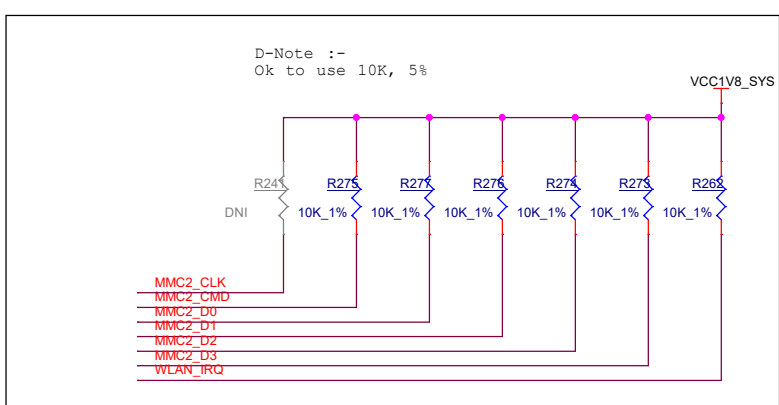
M.2 INTERFACE - SDIO



M.2 LEVEL TRANSLATOR



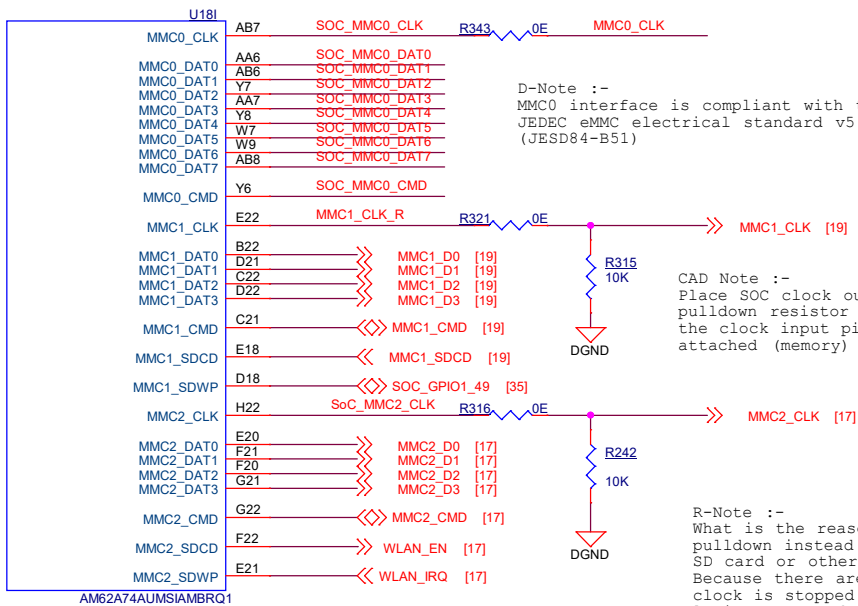
CAD Note :-  
Place Series resistors for MMC2 signals as TRI-PAD to avoid stub



D-Note :-  
Ok to use 10K, 5%

Cad Note :-  
Place R1 & R2 close to each other to avoid stub.

# SOC - MMC Interface



D-Note :-  
OE provision on MMC0\_CLK  
helps improve signal integrity

D-Note :-  
MMC0 interface is compliant with the  
JEDEC eMMC electrical standard v5.1  
(JESD84-B51)

CAD Note :-  
Place SOC clock output  
pulldown resistor near to  
the clock input pin of the  
attached (memory) device

R-Note :-  
What is the reason we selected  
pulldown instead of pullup for EMMC,  
SD card or other peripherals?  
Because there are cases where the  
clock is stopped or paused in a low  
logic state and the pull-down option  
is consistent with this logic state.

D-Note :-  
Ensure eMMC\_RSTn Reset input is enabled  
in the eMMC device (eMMC non-volatile  
configuration space) for the reset  
logic to be functional

D-Note :-  
The GPIO reset option makes it possible  
for software to reset the attached  
device (eMMC or OSPI or SD card or OLDIO  
or EPHY) without resetting the entire  
processor if there is a case where the  
peripheral becomes unresponsive.

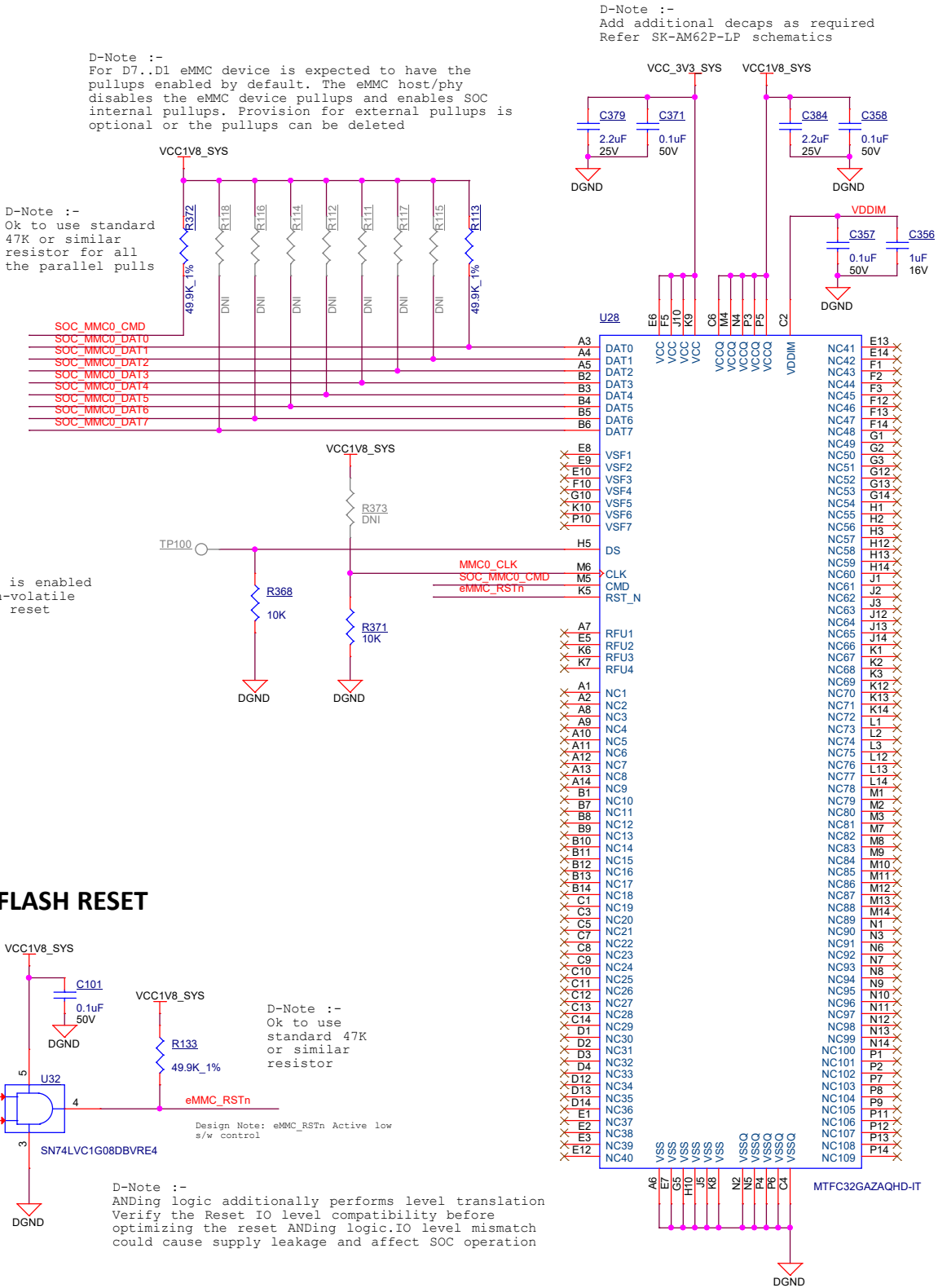
D-Note :-  
You could eliminate the GPIO option and only use the  
reset output ( Warm or cold), where software forces a  
warm reset if the peripheral becomes unresponsive.  
However, this will reset the entire device rather than  
trying to recover the specific peripheral without  
resetting the entire device.

D-Note :-  
Add a series resistor to the SOC GPIO  
input for isolation or testing. Refer  
SK-AM62P-LP schematics

D-Note :-  
In case ANDING logic is not used and the processor  
Main Domain warm reset status output (RESETSTATz)  
is used to reset the attached device, ensure the  
IO voltage level of the attached device matches  
the RESETSTATz IO voltage level. A level  
translator is recommended to match the IO voltage  
level. A resistor divider could be used  
alternatively, provided optimum impedance value of  
the resistor divider is selected. If too high the  
rise/fall time of the eMMC reset input could be  
slow and introduce too much delay. If too low it  
will cause the AM62x to source too much  
steady-state current during normal operation.

D-Note :-  
This family of processor implements a soft PHY  
for eMMC interface. The pulls required for D0,  
Clock and other eMMC interface control signals  
are recommended to be implemented externally.

# eMMC FLASH



D-Note :-  
Add additional decaps as required  
Refer SK-AM62P-LP schematics

D-Note :-  
For D7..D1 eMMC device is expected to have the  
pullups enabled by default. The eMMC host/phy  
disables the eMMC device pullups and enables SOC  
internal pullups. Provision for external pullups is  
optional or the pullups can be deleted

D-Note :-  
Ok to use standard  
47K or similar  
resistor for all  
the parallel pulls

D-Note :-  
Ok to use  
standard 47K  
or similar  
resistor

D-Note :-  
ANDING logic additionally performs level translation  
Verify the Reset IO level compatibility before  
optimizing the reset ANDing logic. IO level mismatch  
could cause supply leakage and affect SOC operation

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Title eMMC FLASH INTERFACE

Size PROC135A

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# SD CARD INTERFACE

D-Note :-  
This power switch, along with the reset logic, and the host IO power supply circuit is required to support UHS-I SD Cards which begins communications using 3.3V signal levels and later change to 1.8V signal levels when changing to one of the faster data transfer speeds. Cycling power to the SD Card is the only way to put it back into 3.3V mode since SD Cards do not have a reset pin. The host IO power supply must power off/on and change voltage at the same time as the SD Card. These circuits and the software driver operating the signals sourcing these circuits ensure both devices are off, or on and operating at the same IO voltage at the same time.

D-Note :-  
ANDing logic could be optimized to 2 input AND gate  
Use RESETSTATz and the SOC IO as inputs

## SD CARD LOAD SWITCH RESET LOGIC

## LOAD SWITCH

D-Note :-  
CT - Add a 220 pF or higher cap for SD card supply slew rate control

D-Note :-  
For UHS-I operation, the pullups are recommended to be connected to the 3.3V/1.8V switched LDO output

R-Note :-  
MMC1\_CLK pullup is a DNI

D-Note :-  
Ensure internal pullups are not configured when 10K external pullups are used. As a good design practice, a 47K pullup is recommended to ensure the pullup value is within the SD card specification, when internal pulls are enabled unexpectedly. This way the resulting pull resistance will still be within the specified.

CAD Note :-  
Place near SD Card Connector

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Title SD CARD INTERFACE

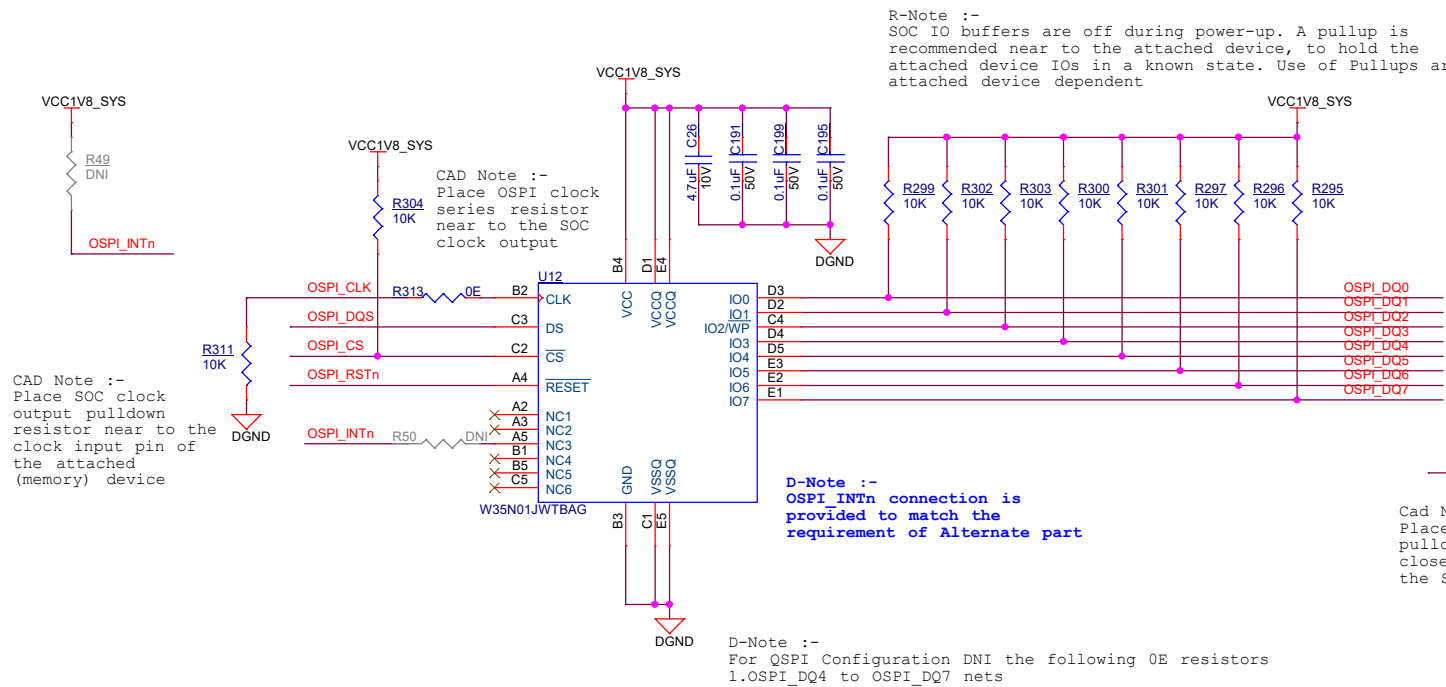
Size PROC135A

Date: Tuesday, June 11, 2024

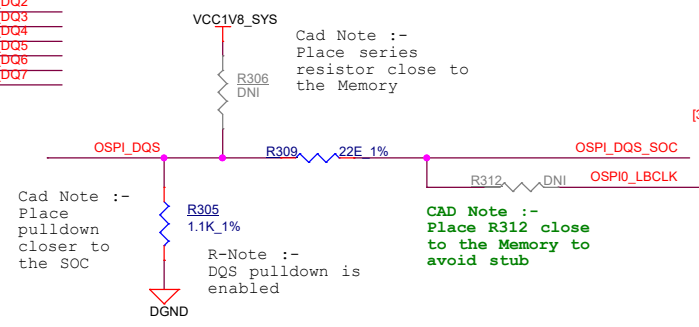
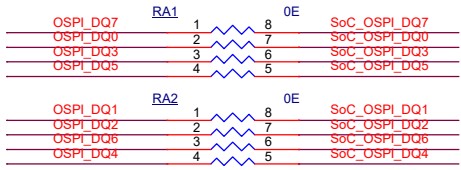
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Rev A

OSPI FLASH

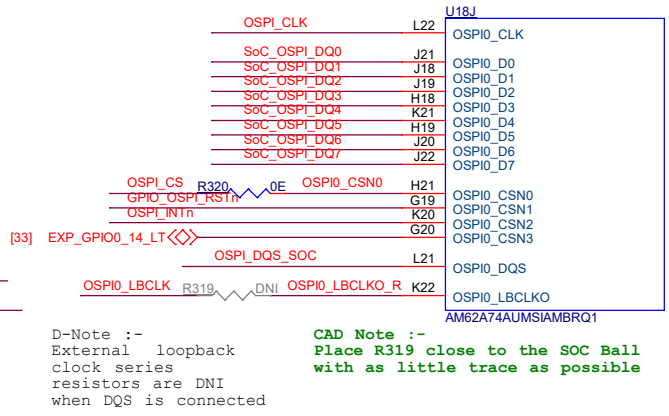


R-Note :-  
These 0 resistors are used for configuring QSPI and OSPI  
This is optional during custom board design

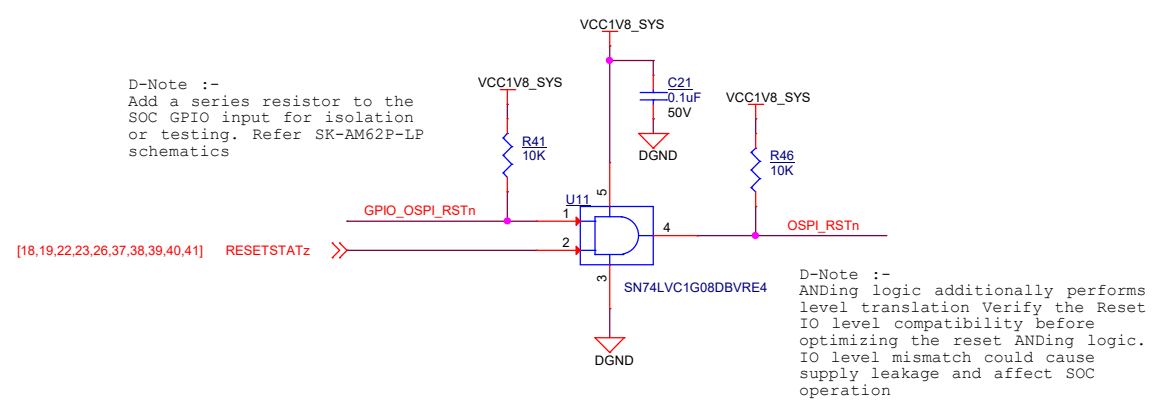


D-Note :-  
Connecting OSPI interface to multiple devices is not recommended or supported

SOC OSPI INTERFACE

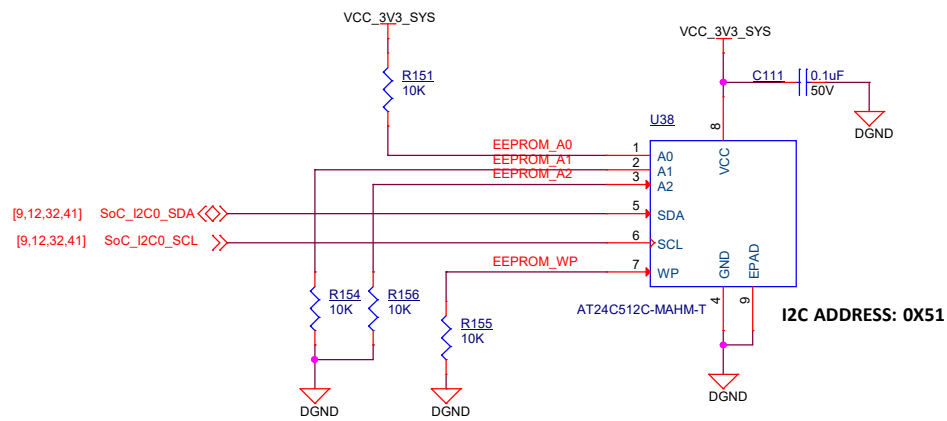


OSPI FLASH RESET

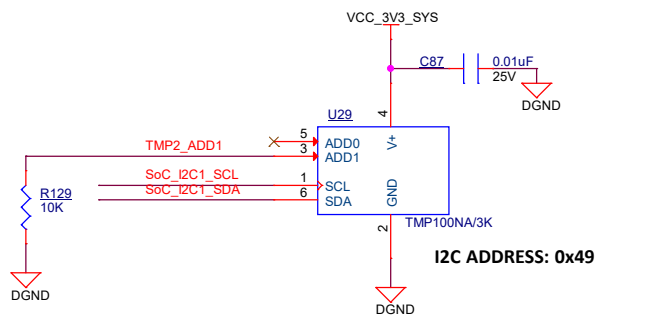
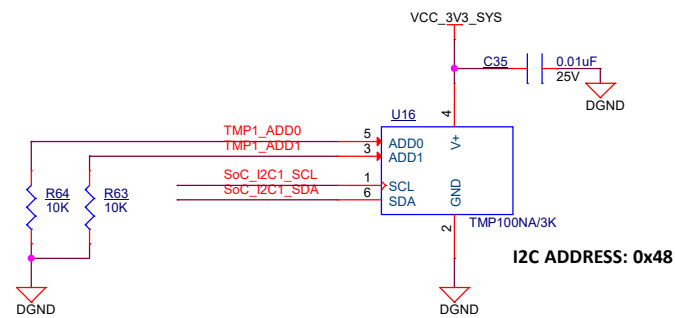




BOARD ID EEPROM



DIGITAL TEMPERATURE SENSORS



CAD NOTE: PLACE TEMP SENSOR CLOSE TO SoC

CAD NOTE: PLACE TEMP SENSOR CLOSE TO LPDDR4

[13,25,38,39,40,41] SoC\_I2C1\_SCL >> TP49

[13,25,38,39,40,41] SoC\_I2C1\_SDA << TP50

Silk: SOC\_I2C1

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Title BOARD ID EEPROM & TEMPERATURE SENSORS

Size C

PROC135A

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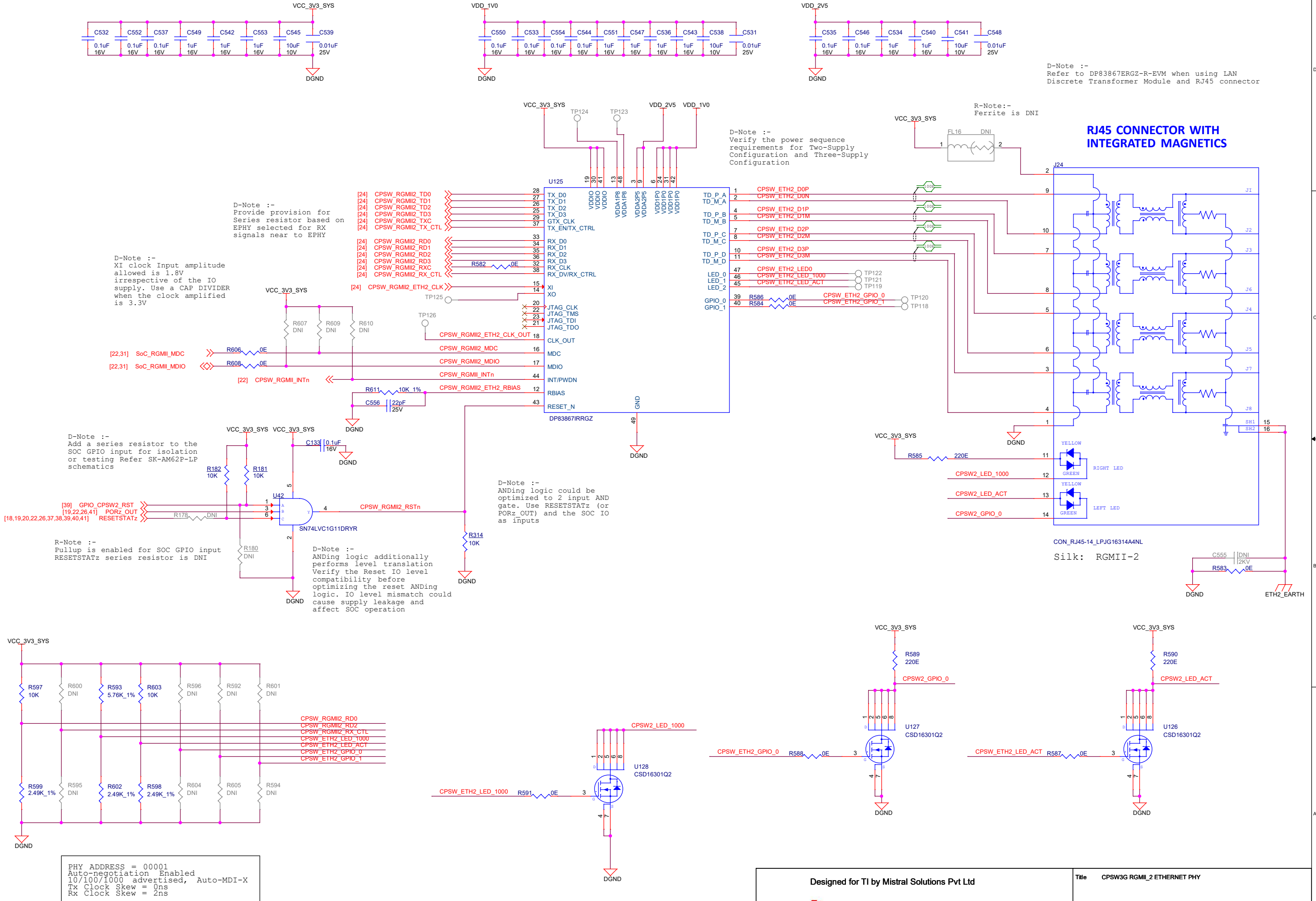
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CPSW3G RGMII 2 - ETHERNET PHY

D-Note :-  
The caps and values used are  
as per the EPHY data sheet  
recommendations.

D-Note :-  
Refer to DP83867ERGZ-R-EVM when using LAN  
Discrete Transformer Module and RJ45 connector

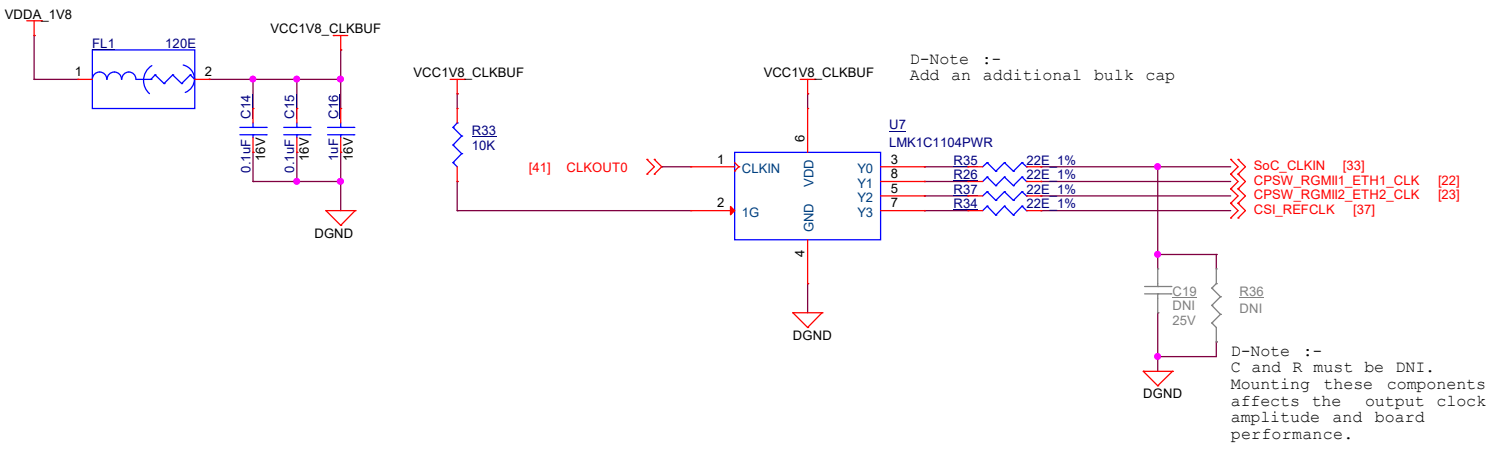


SOC MAC INTERFACE



D-Note :-  
Add series resistors 22 Ohm on the Ethernet interface TX (TDx) signals near to the SOC

CLOCK BUFFER FOR SOC AND ETHERNET PHYS

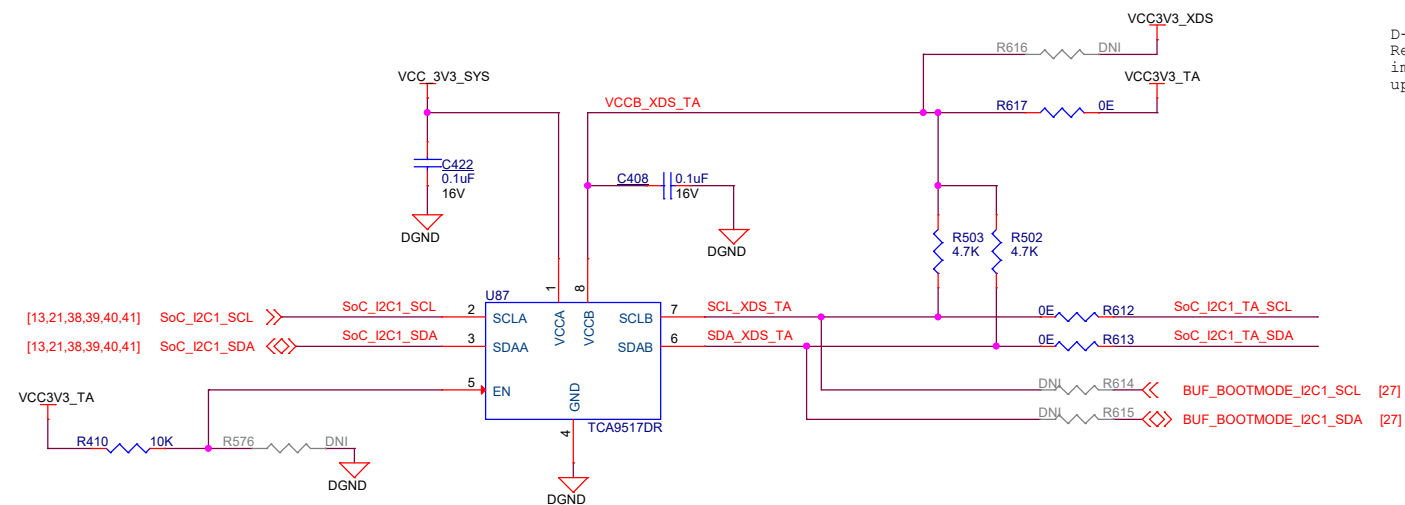


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Title			SOC MAC INTERFACE, CLOCK BUFFER FOR SOC AND ETHERNET PHYS
Size	PROC135A		Rev
C			A
Date:	Tuesday, June 11, 2024	Sheet	24 of 44

## I2C BUS BUFFER



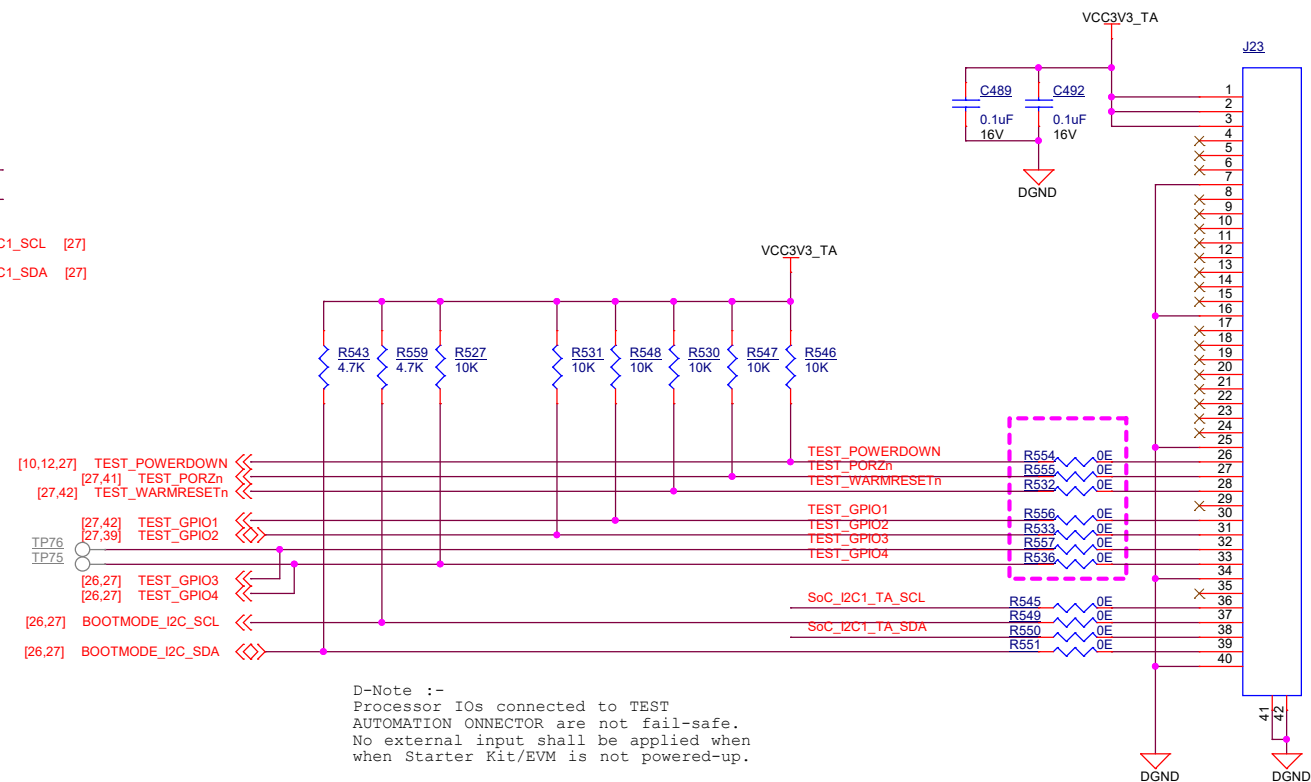
```

XDS110 Configuration
Mount      : R614, R615, R616
Demount    : R612, R613, R617

```

D-Note :-  
Refer SK-AM62P-LP  
implementation for the latest  
updates

## 40-PIN TEST AUTOMATION HEADER

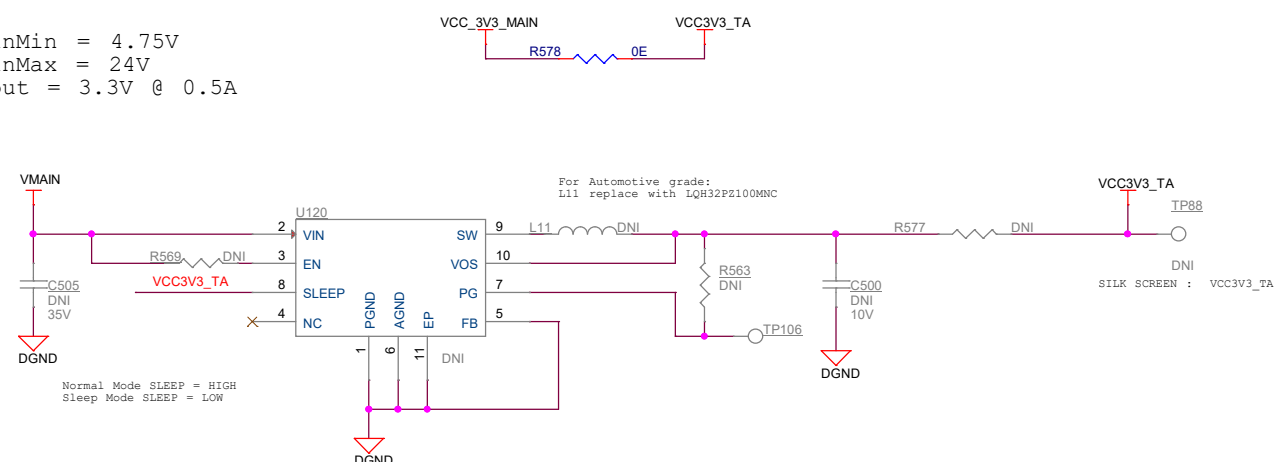


D-Note :-  
Processor IOs connected to TEST  
AUTOMATION CONNECTOR are not fail-safe.  
No external input shall be applied when  
when Starter Kit/EVM is not powered-up.

Silk: AUTOMATION HDR

## TEST AUTOMATION BOARD POWER

```
VinMin = 4.75V
VinMax = 24V
Vout = 3.3V @ 0.5A
```

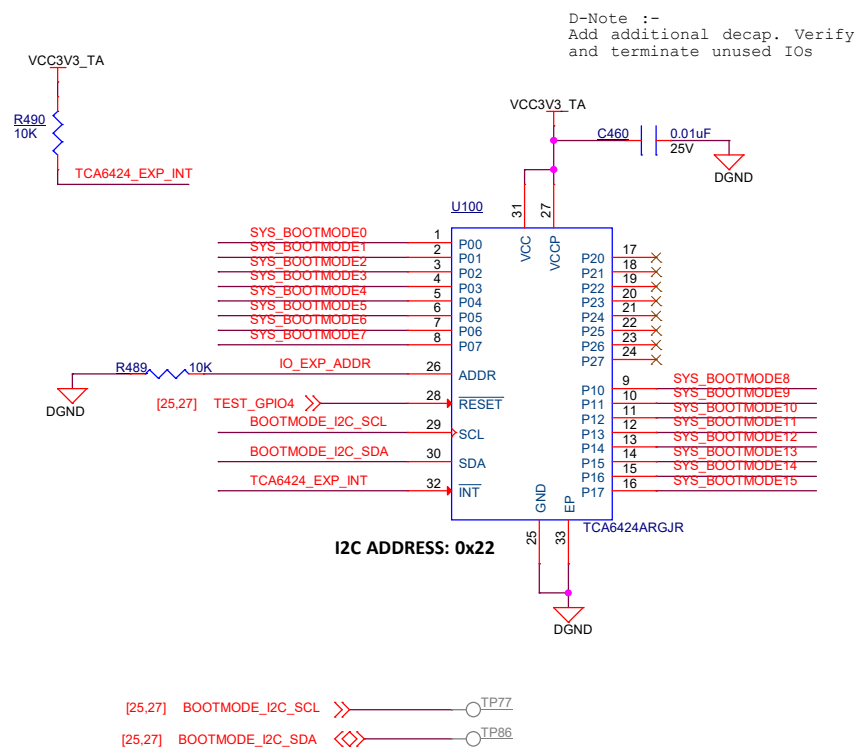


## TEST AUTOMATION GPIO MAPPING

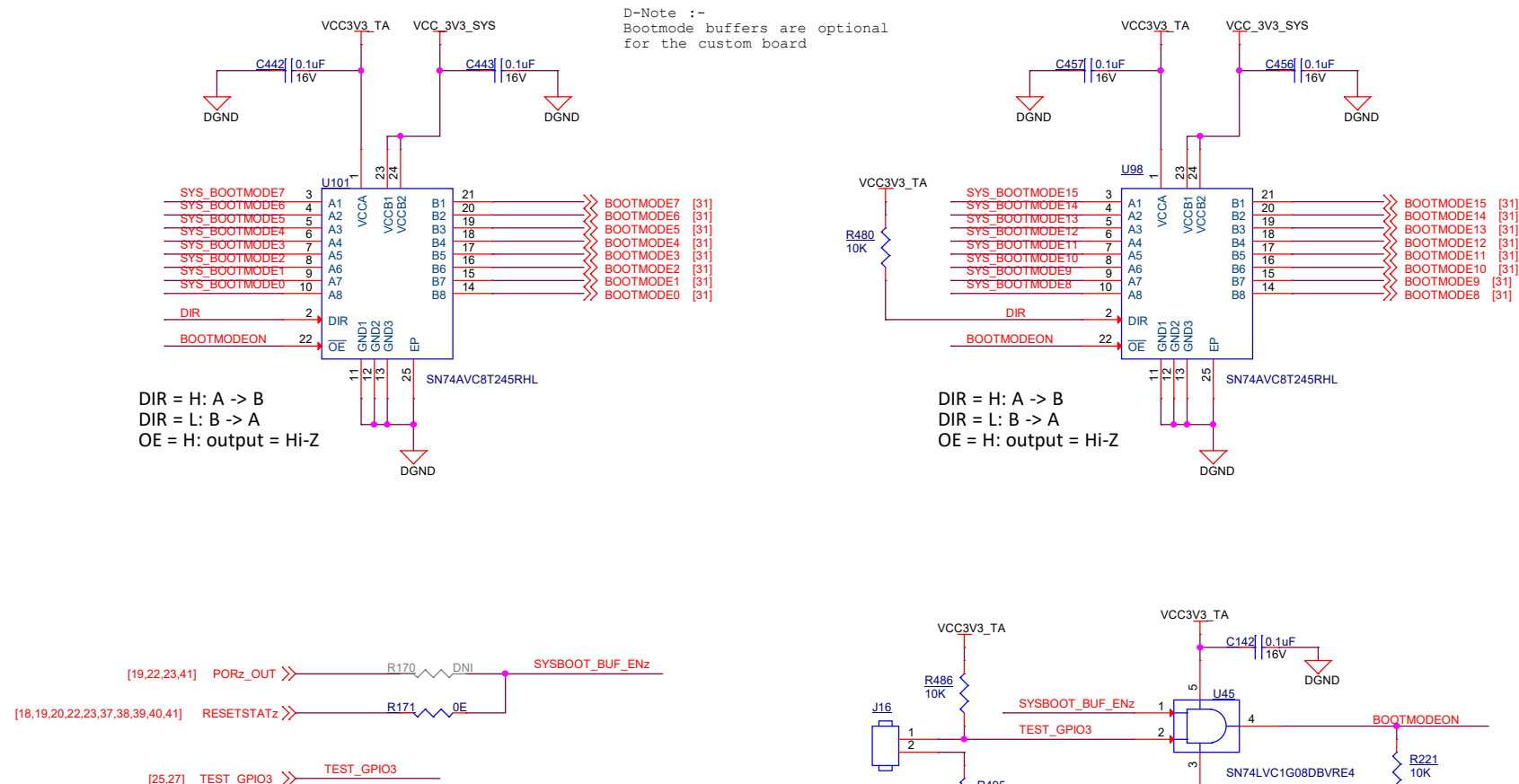
SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SOC_GPIO1_23 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup



## BOOTMODE IO EXPANDER

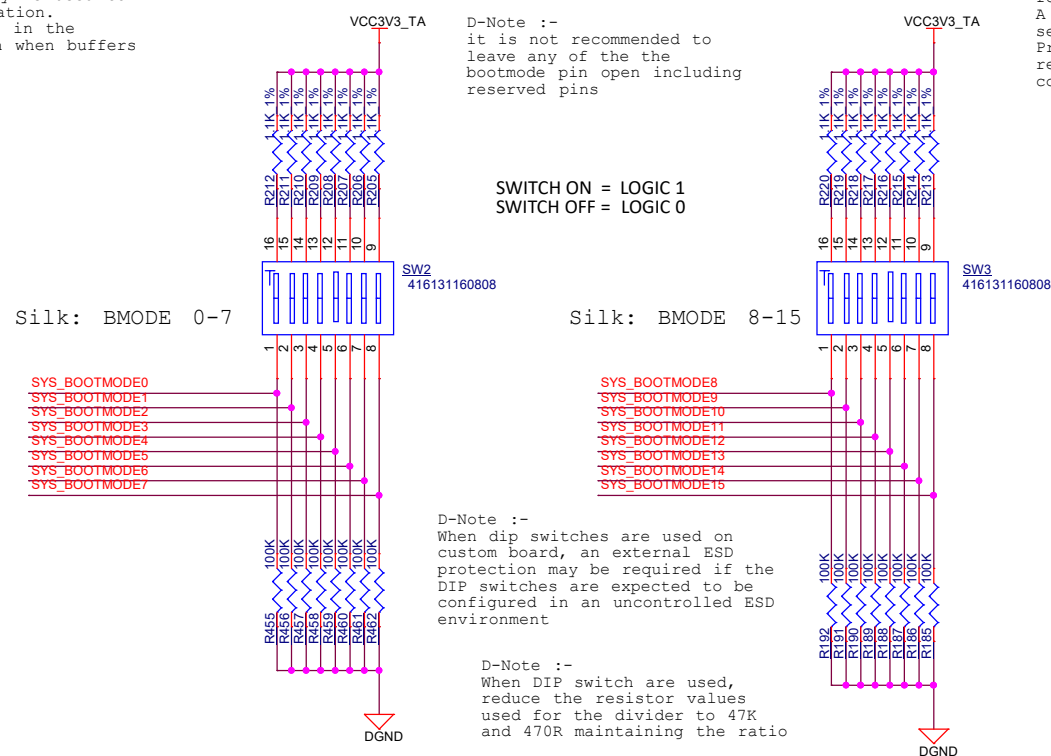


## BOOT MODE BUFFERS



## BOOTMODE CONFIGURATION RESISTORS AND BOOTMODE SWITCHES

D-Note :-  
VCC3V3 XDS\_TA supply is used to support test automation. Connect SOC DVDD3V3 in the custom board design when buffers are not used



### BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. USB0 MS

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Title BOOT MODE BUFFER & SWITCHES

Size  
C PROC135A

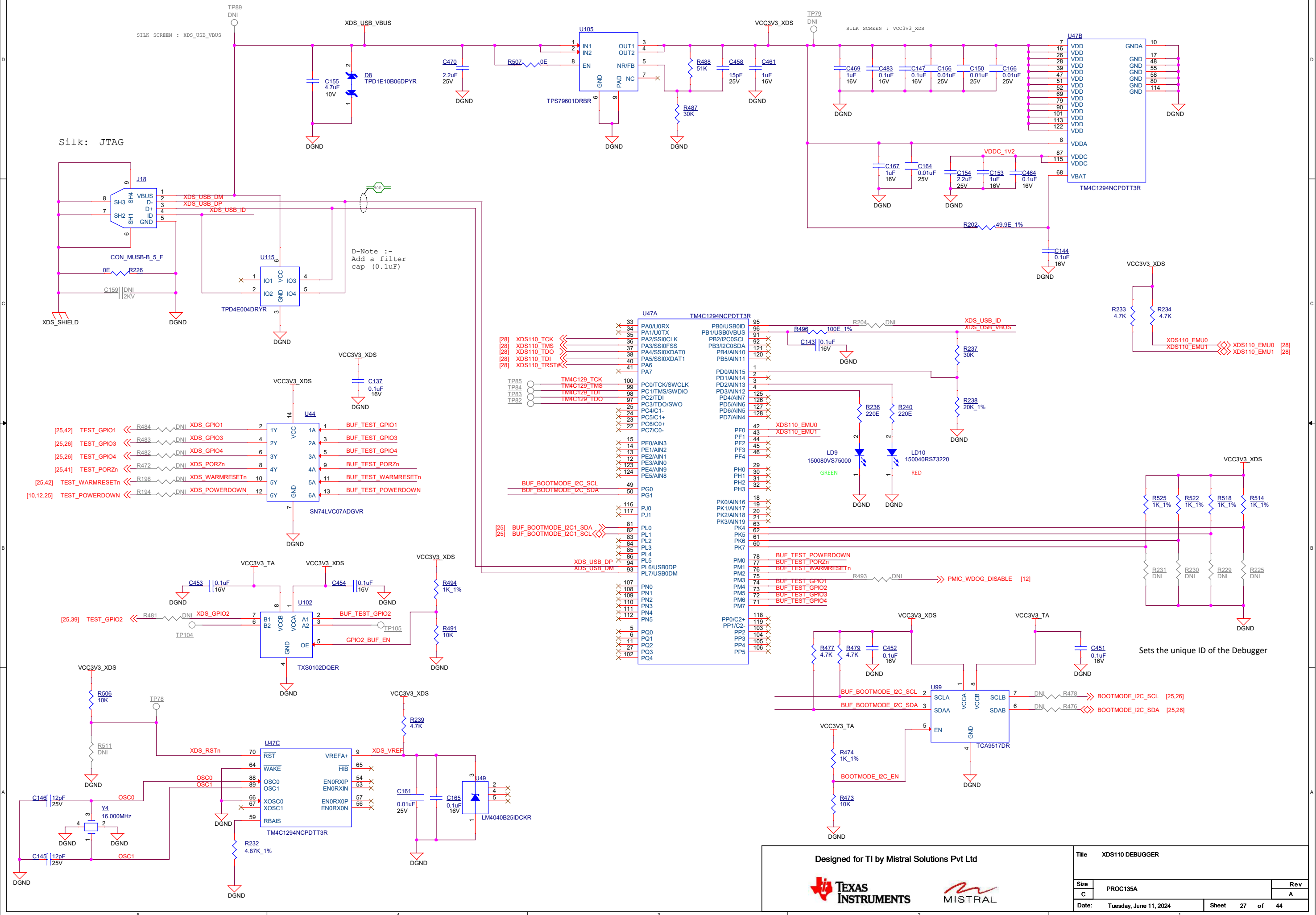
Rev  
A

Date: Tuesday, June 11, 2024

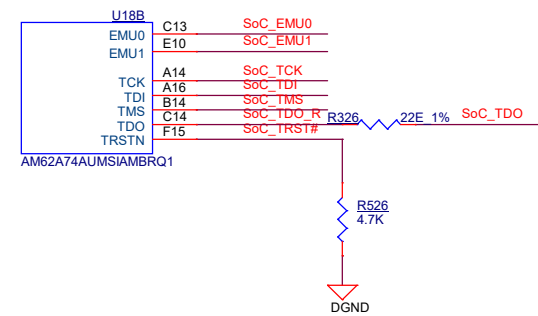
Sheet 26 of 44



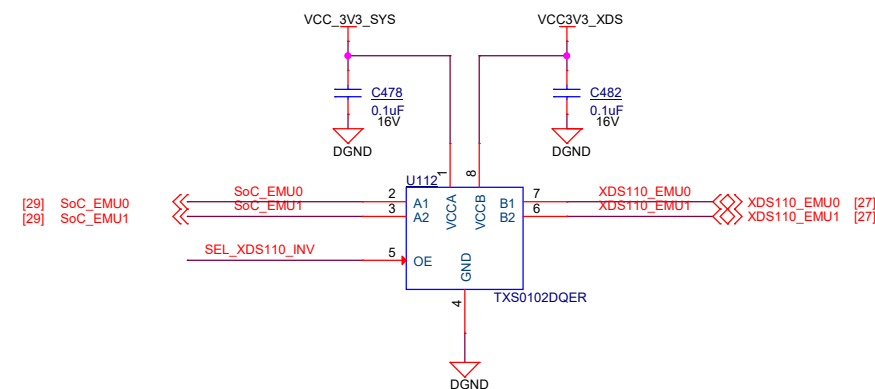
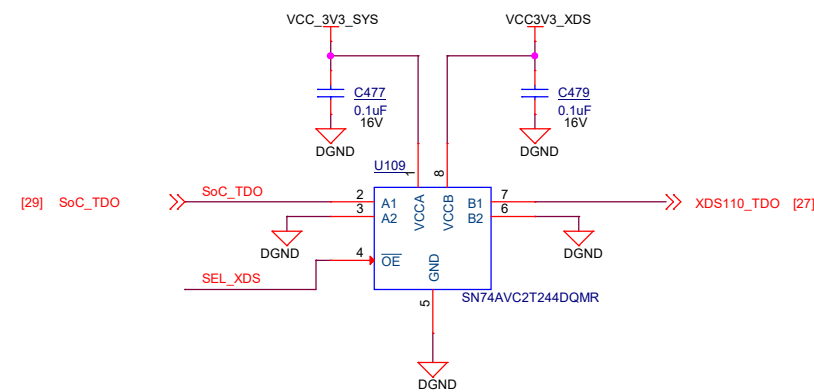
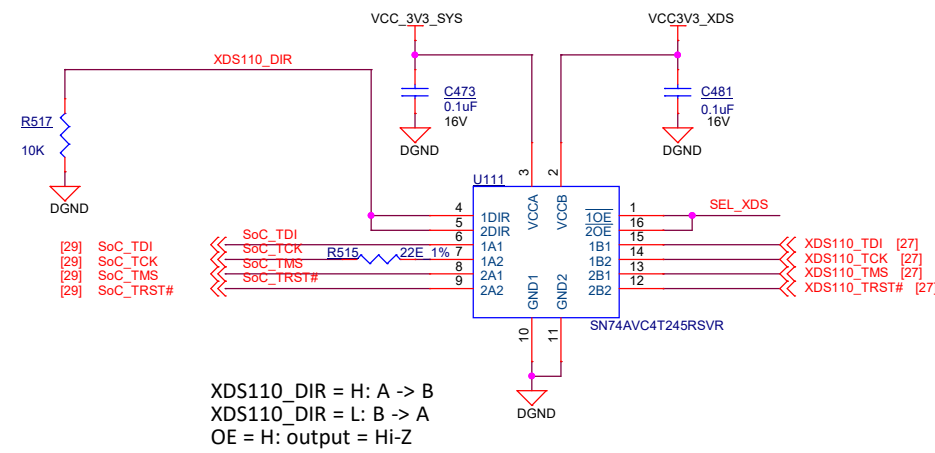
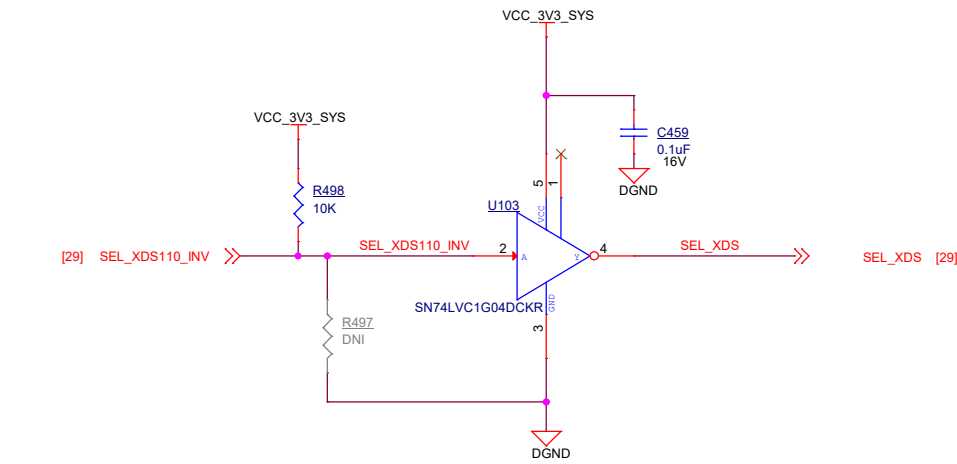
D-Note :-  
Please follow SK-AM62P-LP  
implementations for latest  
updates on XDS110



## SOC JTAG INTERFACE



## BUFFER XDS110



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Title JTAG BUFFER

Size  
C PROC135A

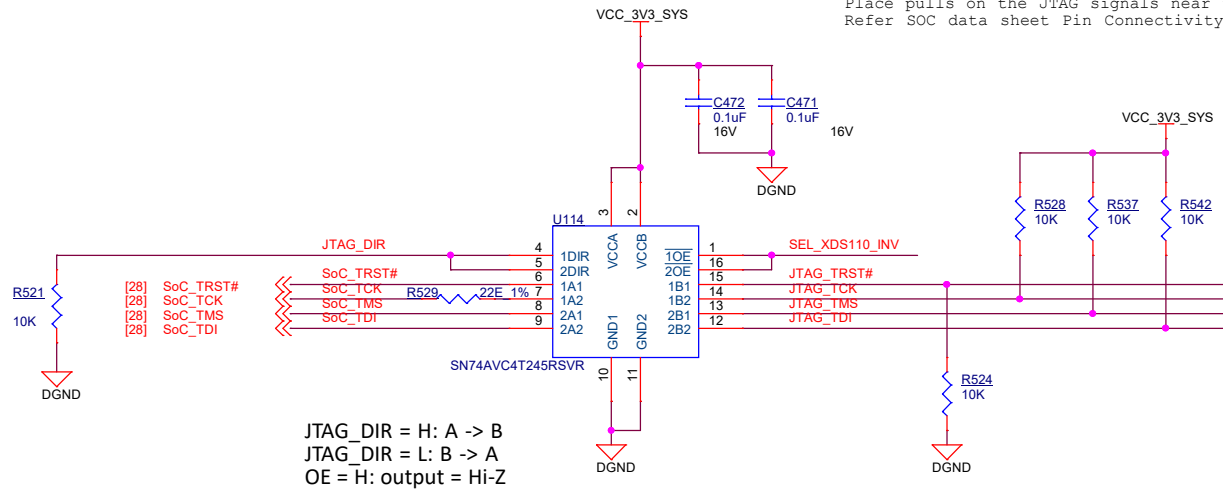
Rev  
A

Date: Tuesday, June 11, 2024

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cTI20 JTAG BUFFERS

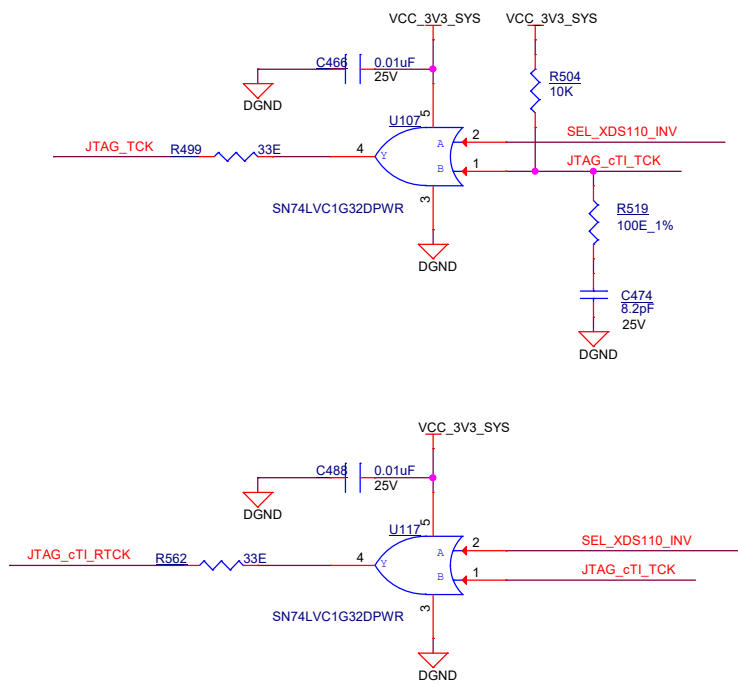
D-Note :-  
Place pulls on the JTAG signals near to the SOC  
Refer SOC data sheet Pin Connectivity Requirements section



JTAG\_DIR = H: A -> B  
JTAG\_DIR = L: B -> A  
OE = H: output = Hi-Z

CAD NOTE: Buffers U114 and U122  
need to be placed closer to the  
cTI-20pin connector J19 to reduce Stub length of the JTAG signals.

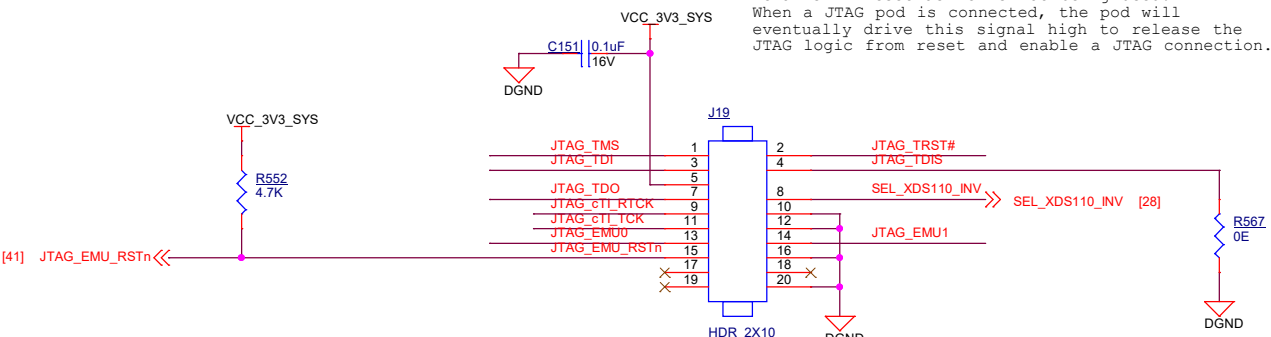
JTAG CLOCK BUFFER



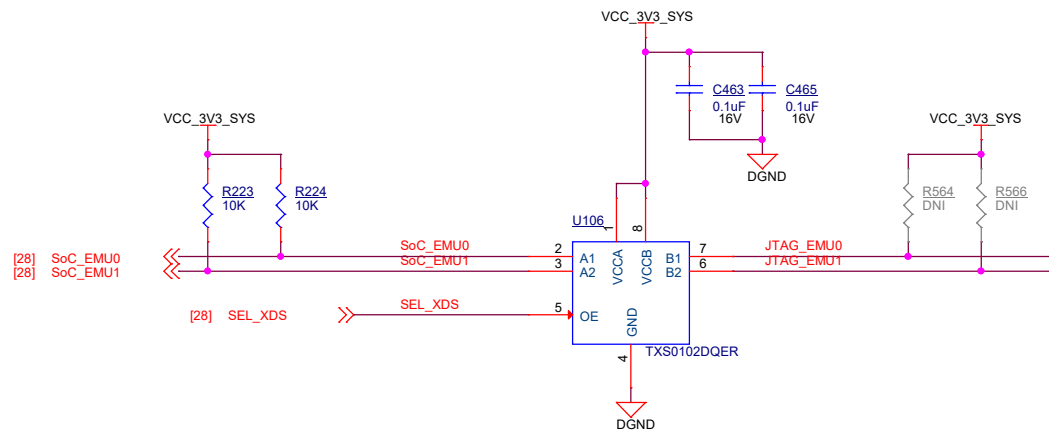
D-Note :-  
Add an external ESD protection to provide  
system level ESD protection when external  
connector is used for debug  
Add Test points and ESD protection when  
JTAG connector is not used

JTAG 20 PIN cTI CONNECTOR

D-Note :-  
TRSTn is the reset to the JTAG logic. For normal  
operation, this is pulled low, and thus the JTAG  
remains in reset as it is not being used.  
When a JTAG pod is connected, the pod will  
eventually drive this signal high to release the  
JTAG logic from reset and enable a JTAG connection.



Silk: cTI



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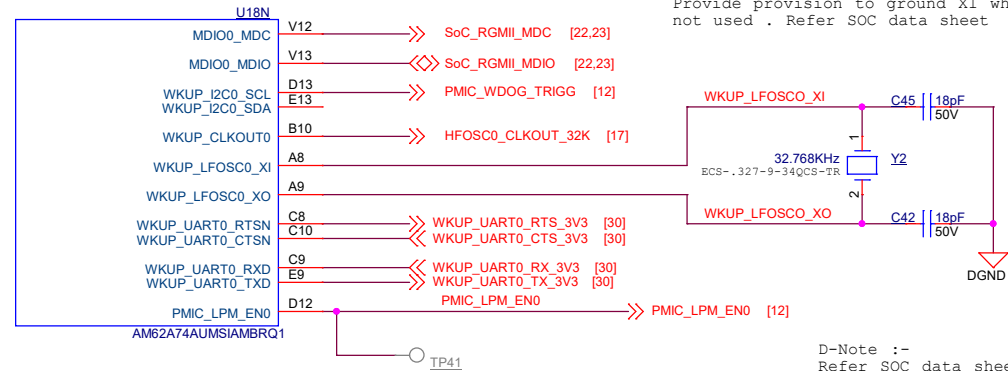


Title		JTAG 20 PIN cTI CONNECTOR	
Size	PROC135A	Rev	A
Date:	Tuesday, June 11, 2024	Sheet	29 of 44



## SOC WKUP DOMAIN

D-Note :-  
Open-drain output type buffer I2C interfaces A pullup is recommended for Open-drain output type I2C interfaces irrespective of the IO configuration Refer pin connectivity table of SOC data sheet



D-Note :-  
WKUP LFOSCO has limited use case.  
Provide provision to ground XI when  
not used . Refer SOC data sheet

D-Note :-  
The only LFOSC0 register bits that should be changed by the customer are BP\_C, PD\_C, and CTRLMMR WKUP\_LFXOSC\_TRIM[18:16], where PD\_C is reset (0) to enable the oscillator and the BP\_C bit is only set (1) to place the oscillator in bypass mode when using an LVCMOS clock source. The CTRLMMR WKUP\_LFXOSC\_TRIM[18:16] bits are set based on the actual capacitance load applied to the crystal, as defined by the Load Capacitance Equation. The load capacitance range of the crystal will be half of the recommended capacitor value range, since there are connected in series with the crystals resonate circuit.

D-Note :-  
Open-drain output type buffer I2C interfaces have slew rate requirement when pulled to 3.3 V. An RC is recommended for slew rate control. Refer SK-AM62P-LP schematics

D-Note :-  
SOC IO buffers used for GPMC interface signals are disabled during reset. The required pulls for the interfaced signals are provided on the GPMC interface card

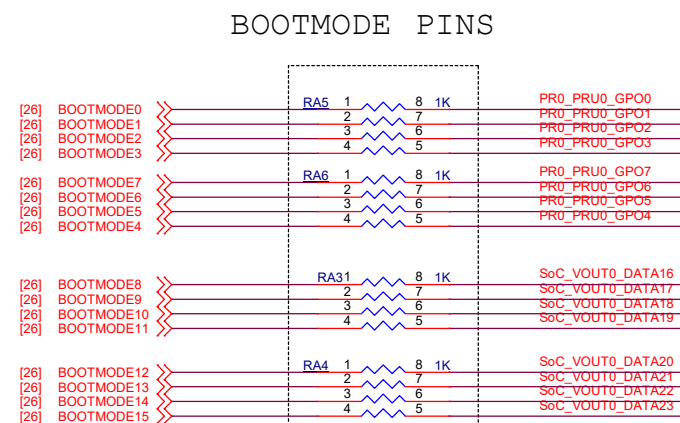
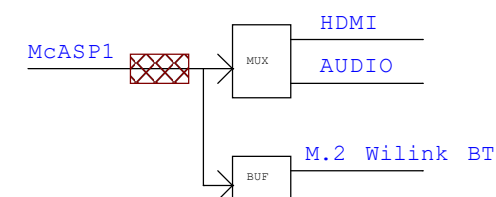
D-Note :-  
Shorting of bootmode inputs (IOs) is not recommended or allowed since the IOs have alternate functions that could be configured after boot. Shorting the bootmode pins directly to VCC or ground directly is not recommended. Connect each of the bootmode pins through separate resistor. Choose the bootmode resistor value based on the use case (10K or similar)

D-Note :-  
Refer SOC data sheet for the recommended circuit configuration during preproduction PCB and the production PCB

D-Note :-  
Reduce the series resistor value when buffer is not used to OR  
This resistor is used to isolate the alternate function during testing

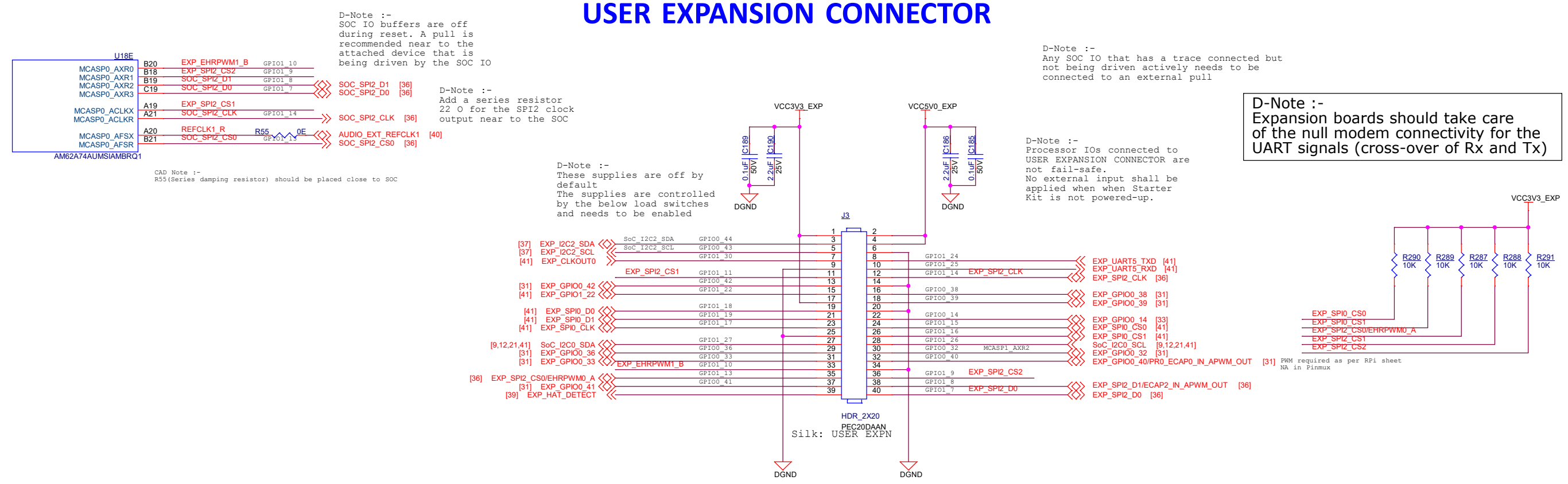


D-Note :-  
Add a 22R at the  
output of MCASP1\_ACLKX  
near to the SOC

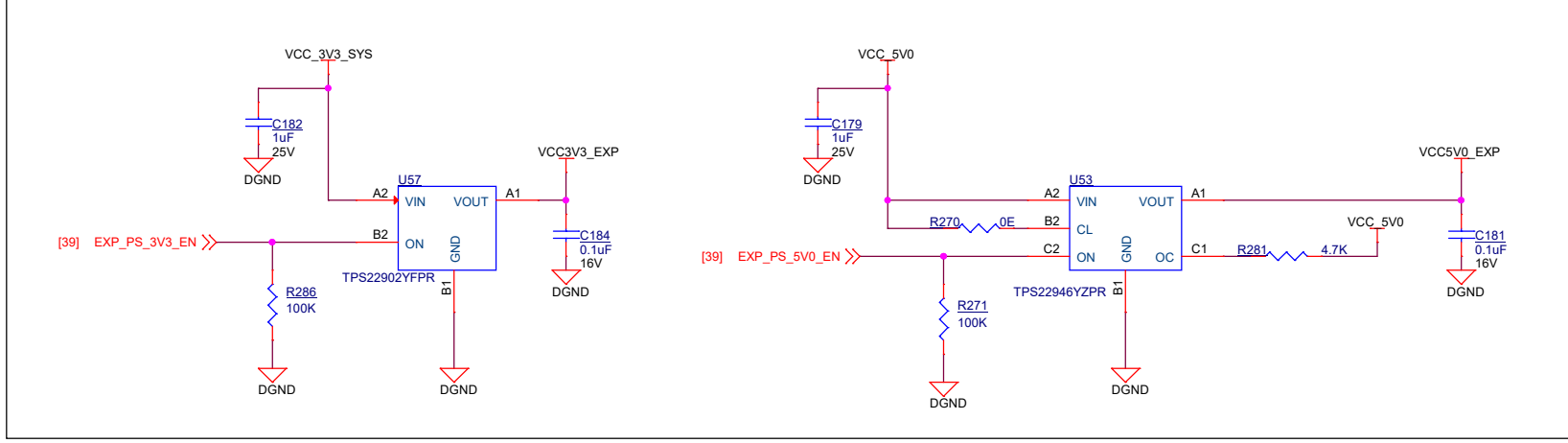


D-Note :-  
1K Resistors are used to  
isolate the BOOTMODE control logic  
after the value is latched

# USER EXPANSION CONNECTOR



## LOAD SWITCHES FOR USER EXPANSION CONNECTOR



### R-Note :-

AM62A Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62A Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

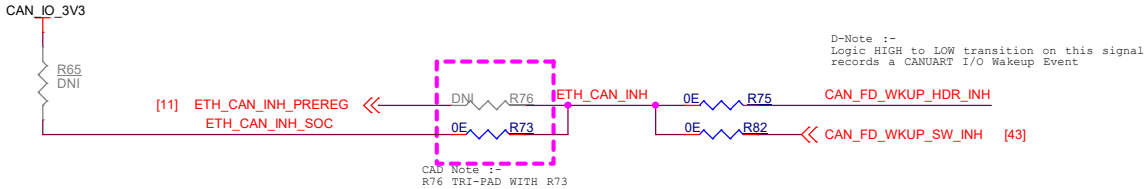
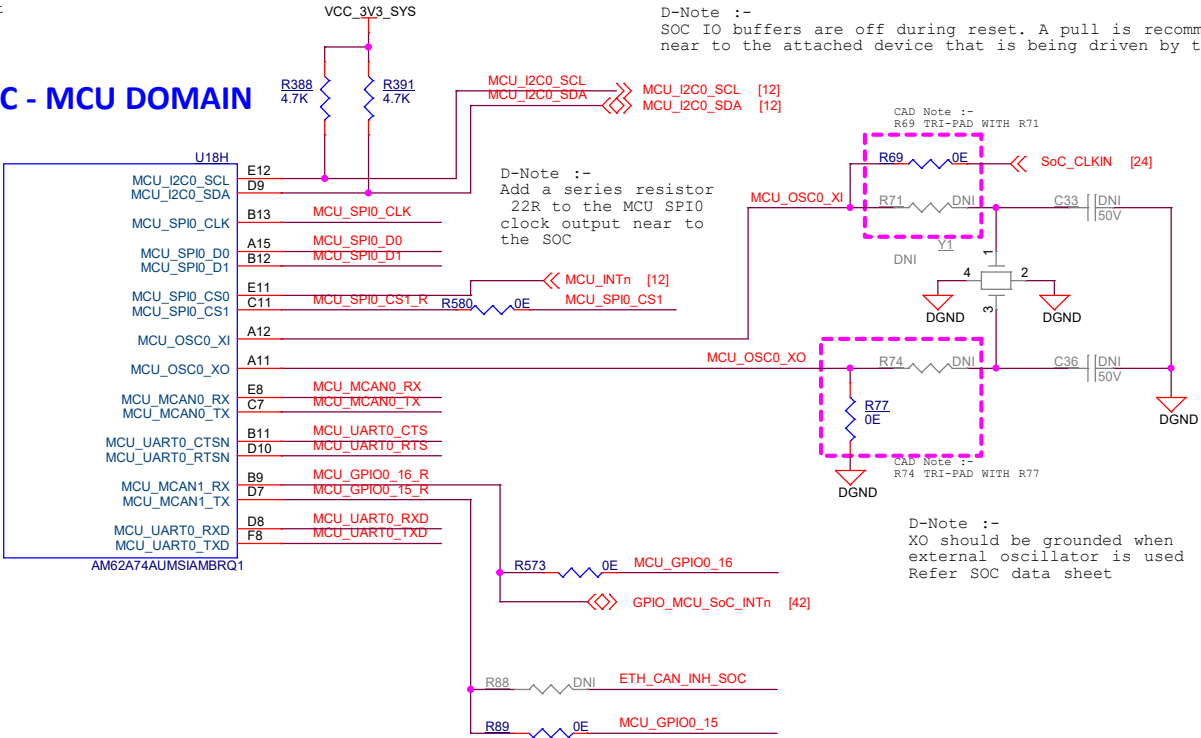


D-Note :-  
A pullup is recommended for Open-drain output type I2C interfaces irrespective of the IO configuration Refer pin connectivity table of SOC data sheet

D-Note :-  
Open-drain output type buffer I2C interfaces have slew rate requirement when pulled to 3.3 V An RC is recommended for slew rate control. Refer SK-AM62P-LP schematics

D-Note :-  
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO

SOC - MCU DOMAIN



D-Note :-  
Connect the 25 MHz crystal directly to the SOC Xi and Xo pins (No Series or parallel resistors are recommended). The internal oscillator implements AGC (Automatic Gain Control) for amplitude control. Match the SOC and the EPHY crystal specs

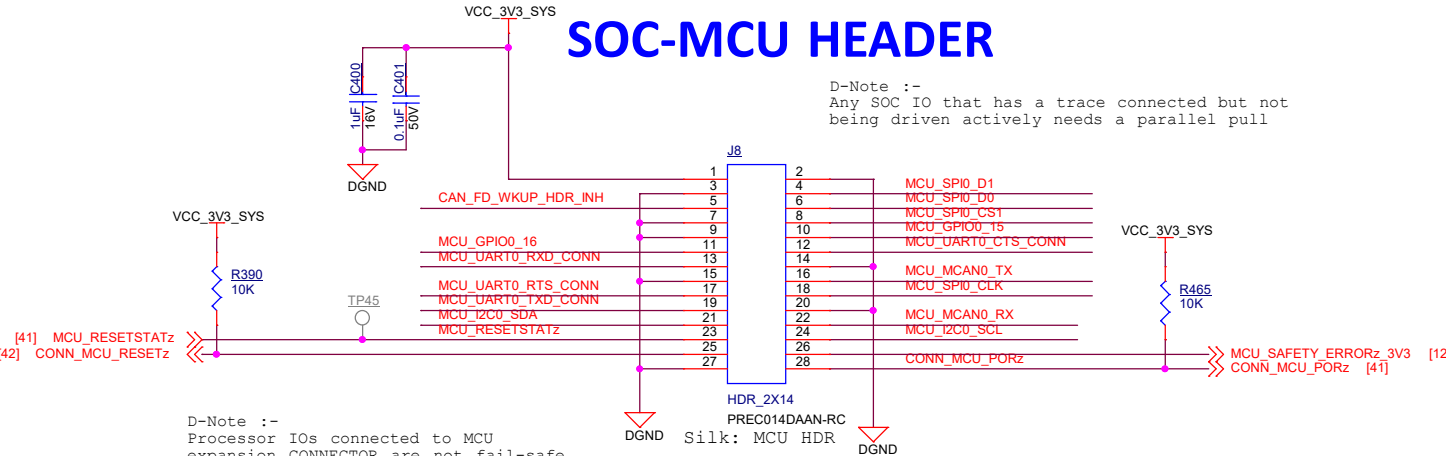
D-Note :-  
Refer Applications, Implementation, and Layout section of the data sheet for clock routing guidelines as below:  
Clock Routing Guidelines  
Oscillator Routing

D-Note :-  
No HFOSC0 registers are required to be changed. These registers should remain in their default state. Select the appropriate crystal circuit components that are compliant to the values defined in the MCU\_OSC0 Crystal Circuit Requirements table. Read the Load Capacitance and Shunt Capacitance sections to select the appropriate crystal circuit components.

D-Note :-  
MCU\_OSC0 has been validated only with a 25 MHz clock source, so that is the only frequency supported. The datasheet shows MCU\_OSC0 not starting until after the core voltage because there are some cases where the oscillator may not start until VDD\_CORE is valid. In most cases it will start as early as VDDSD0, but this may not always be the case. This diagram in the datasheet is showing the maximum start-up time, which must include the case where the delay is based on VDD\_CORE being valid.

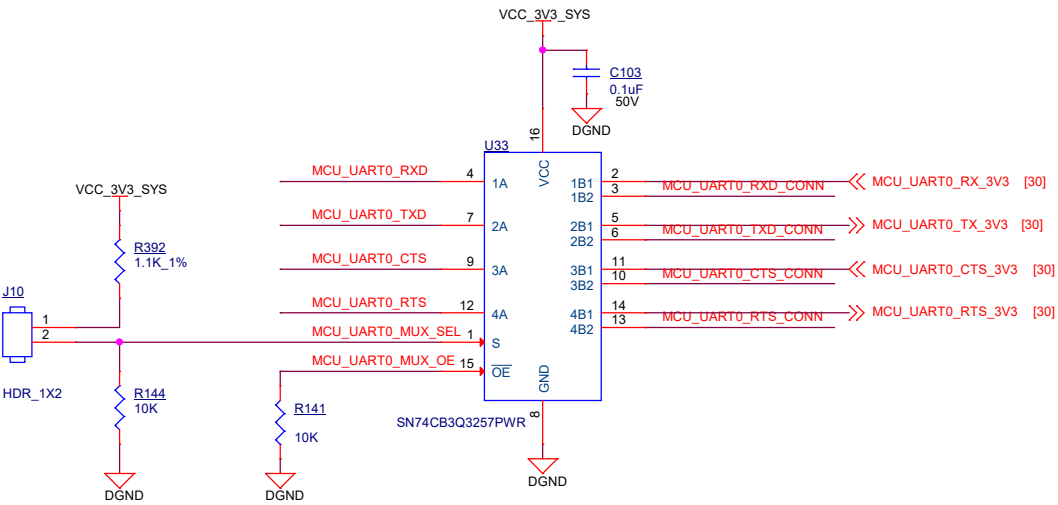
SOC-MCU HEADER

D-Note :-  
Any SOC IO that has a trace connected but not being driven actively needs a parallel pull



D-Note :-  
Processor IOs connected to MCU expansion CONNECTOR are not fail-safe. No external input shall be applied when Starter Kit/EVM is not powered-up.

SOC-MCU\_UART0 MUX



OEn	SEL	INPUT/OUTPUT	
		An	An
L	L (DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER

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Title MCU HEADER

Size PROC135A

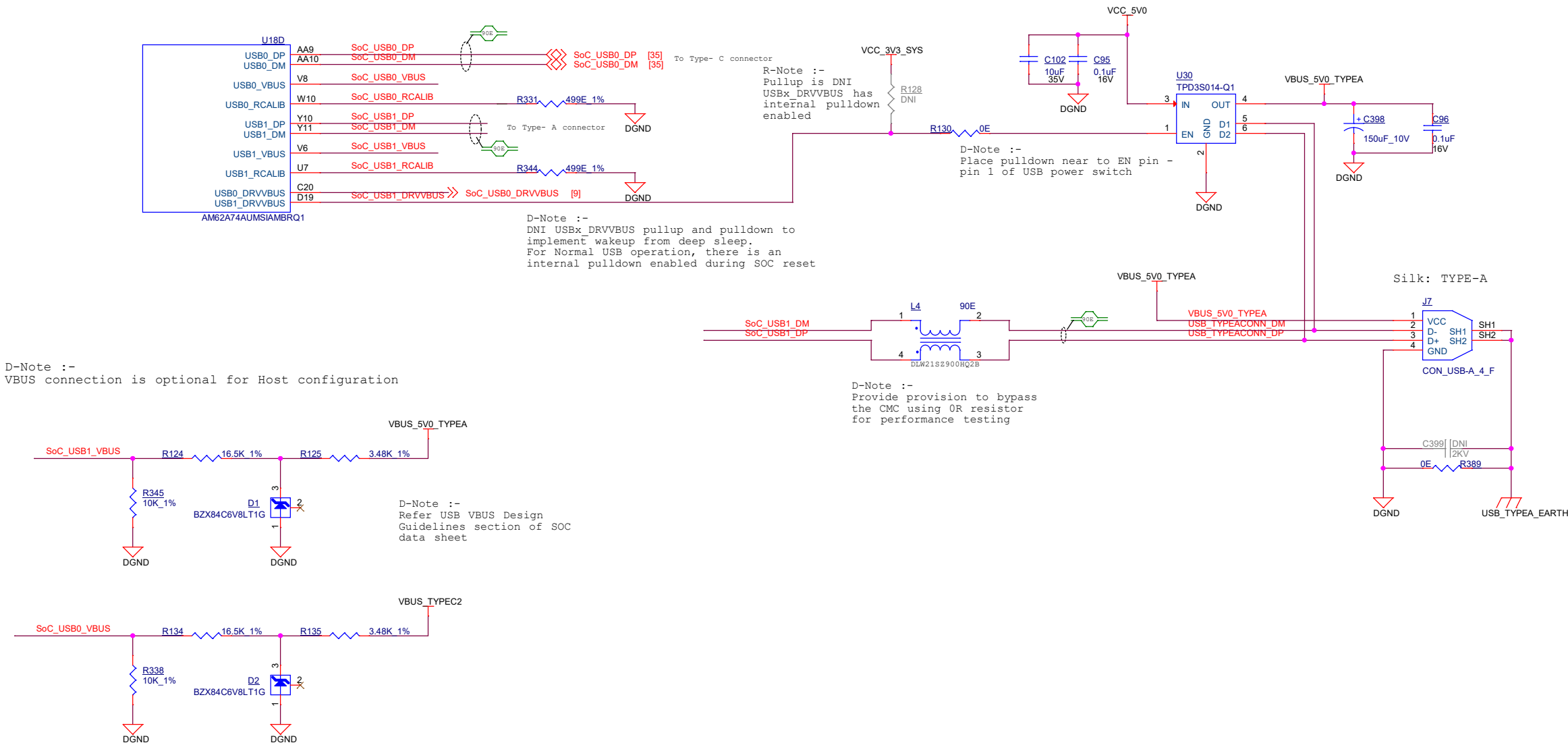
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USB1 - USB 2.0 TYPE-A

D-Note :-  
Use power switch with OC indication  
Example TPS2051  
Connect to a SOC IO for OC detection  
Refer SK-AM62P-LP schematics



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Title USB1 TYPE-A

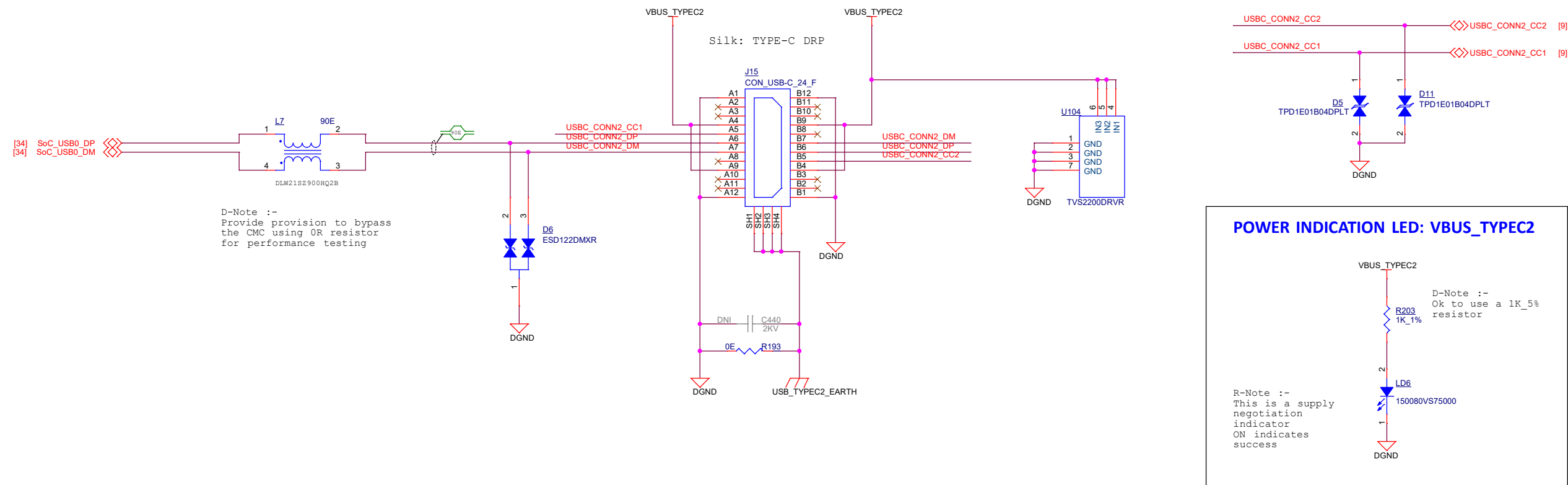
Size PROC135A

Date: Tuesday, June 11, 2024

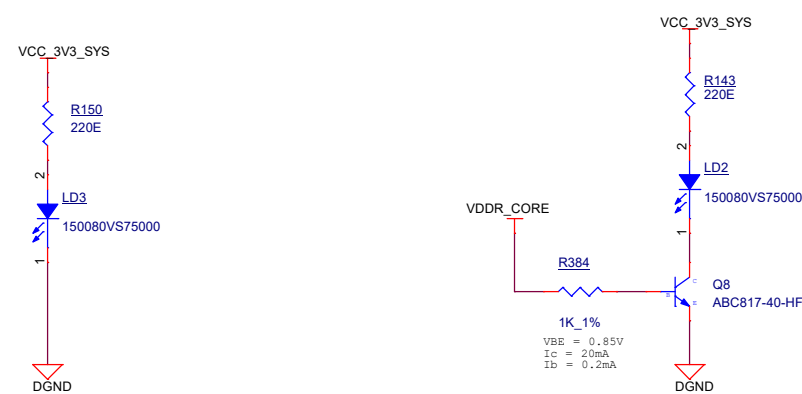
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Rev A

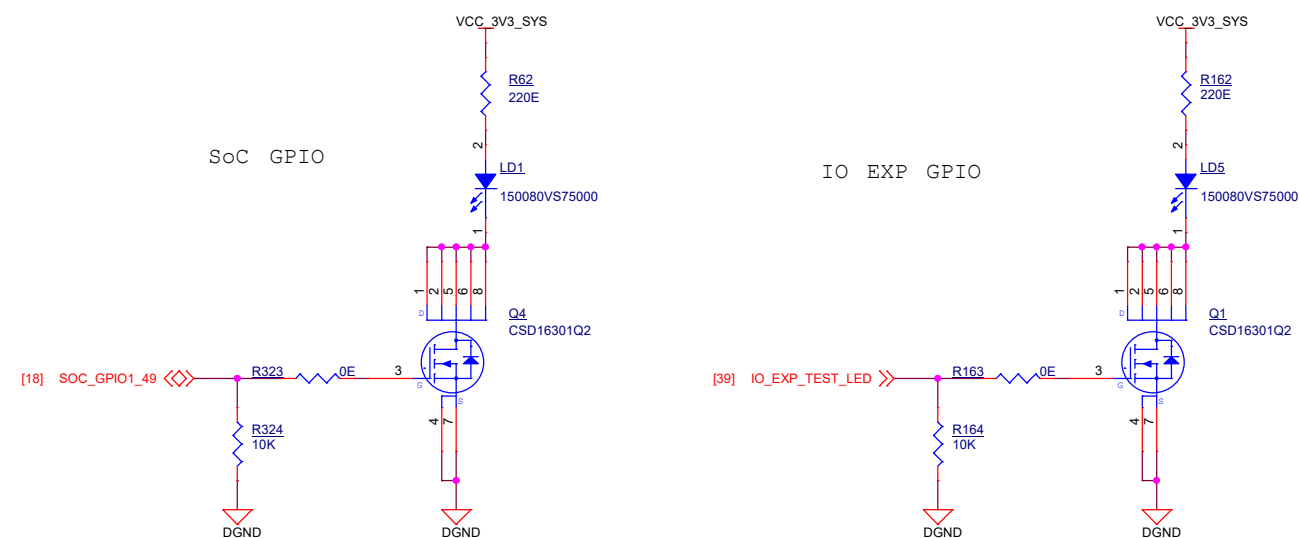
# USB0 TYPE-C DRP



## POWER RAIL LEDS



## USER TEST LEDS



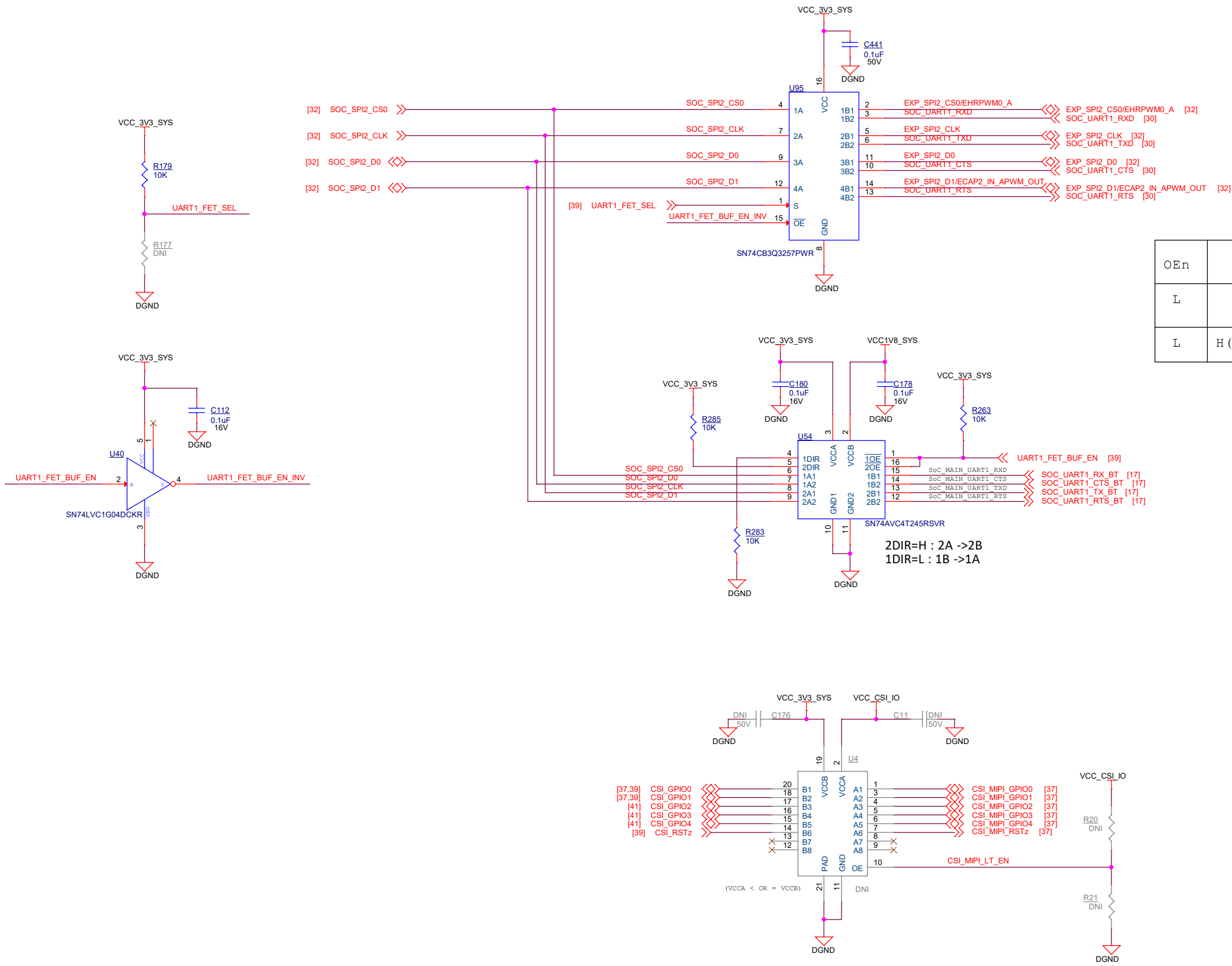
Designed for TI by Mistral Solutions Pvt Ltd



Title USB0 TYPE-C DRP & USER TEST LED

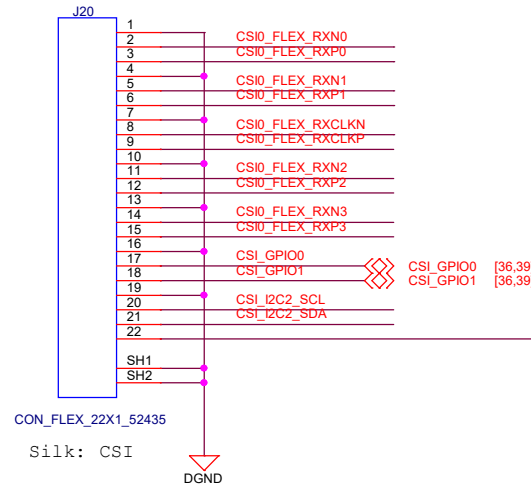
Size	Rev
C	A
Date: Tuesday, June 11, 2024	Sheet 35 of 44

SoC UART1 FET SWITCH & BUFFER

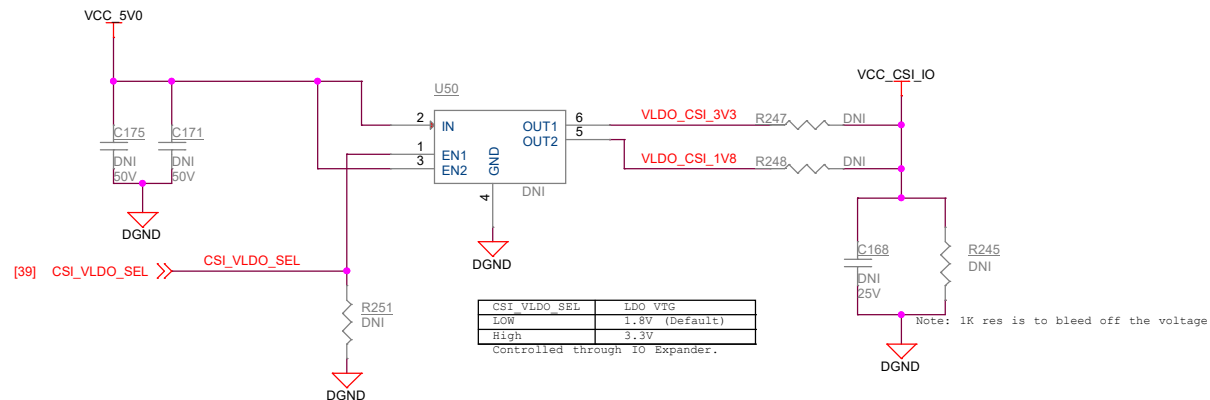
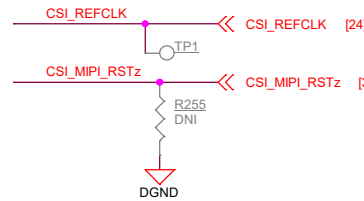
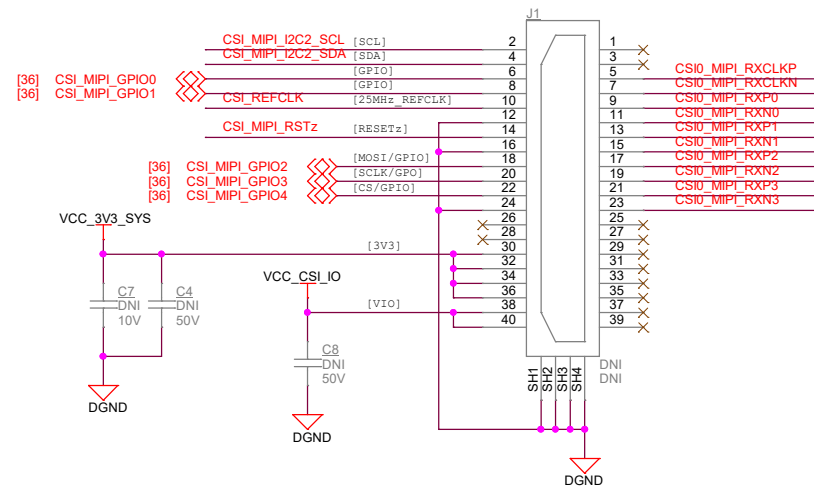


OEn	SEL	INPUT/OUTPUT	
		An=nB1	An
L	L	An=nB1	SOC - USER EXPANSION CONNECTOR
L	H (DEFAULT)	An=nB2	SOC - FT4232

## CSI INTERFACE



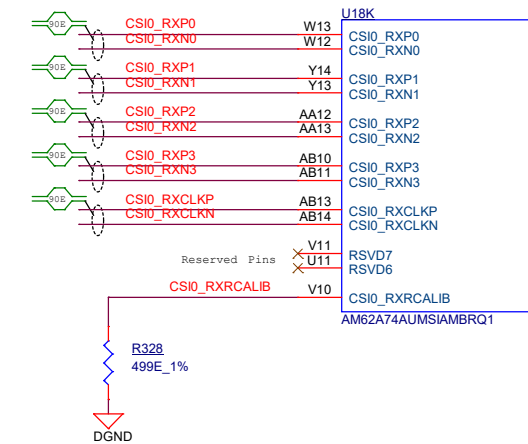
## MIPI CONNECTOR



CSI_VLDO_SEL	LDO_VTO
LOW	1.8V (Default)
High	3.3V

Controlled through IO Expander.

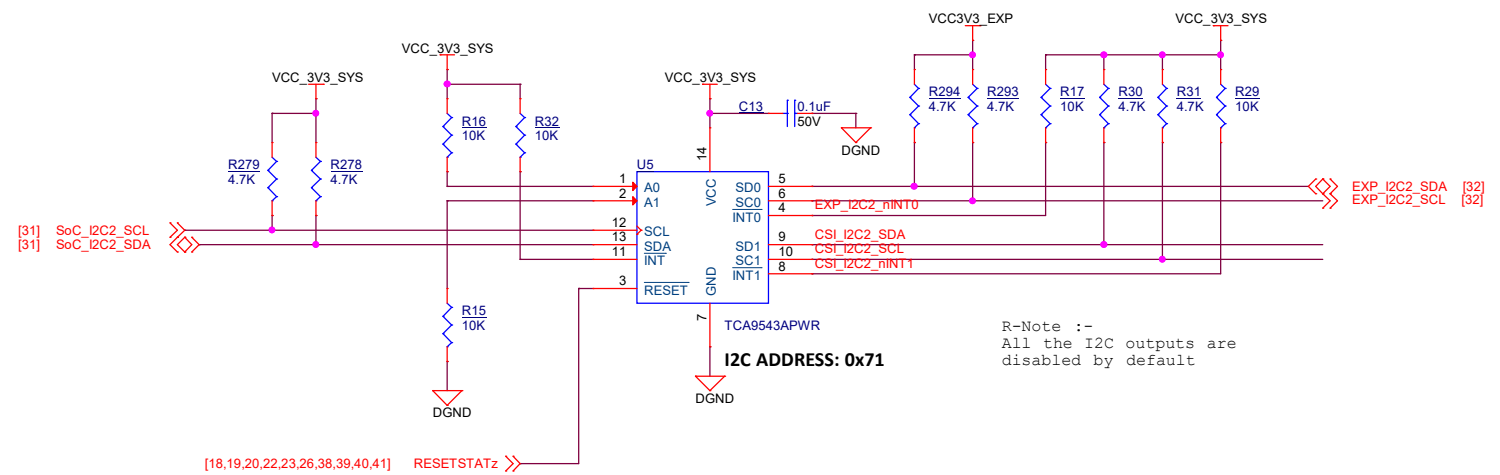
## SOC CSI INTERFACE



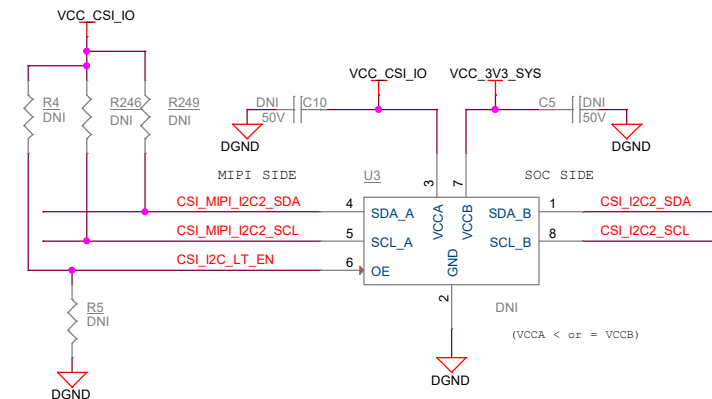
CSI - 1:2 MUX : Truth Table

MUX_SEL_2	FUNCTION
LOW	INPUT<--A port [CSI-2 Connector - J1]
HIGH	INPUT<--B port [Flex Camera Connector - J20] (default)

## I2C SWITCH FOR SoC\_I2C2



R-Note :-  
All the I2C outputs are disabled by default



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Title CSI INTERFACE

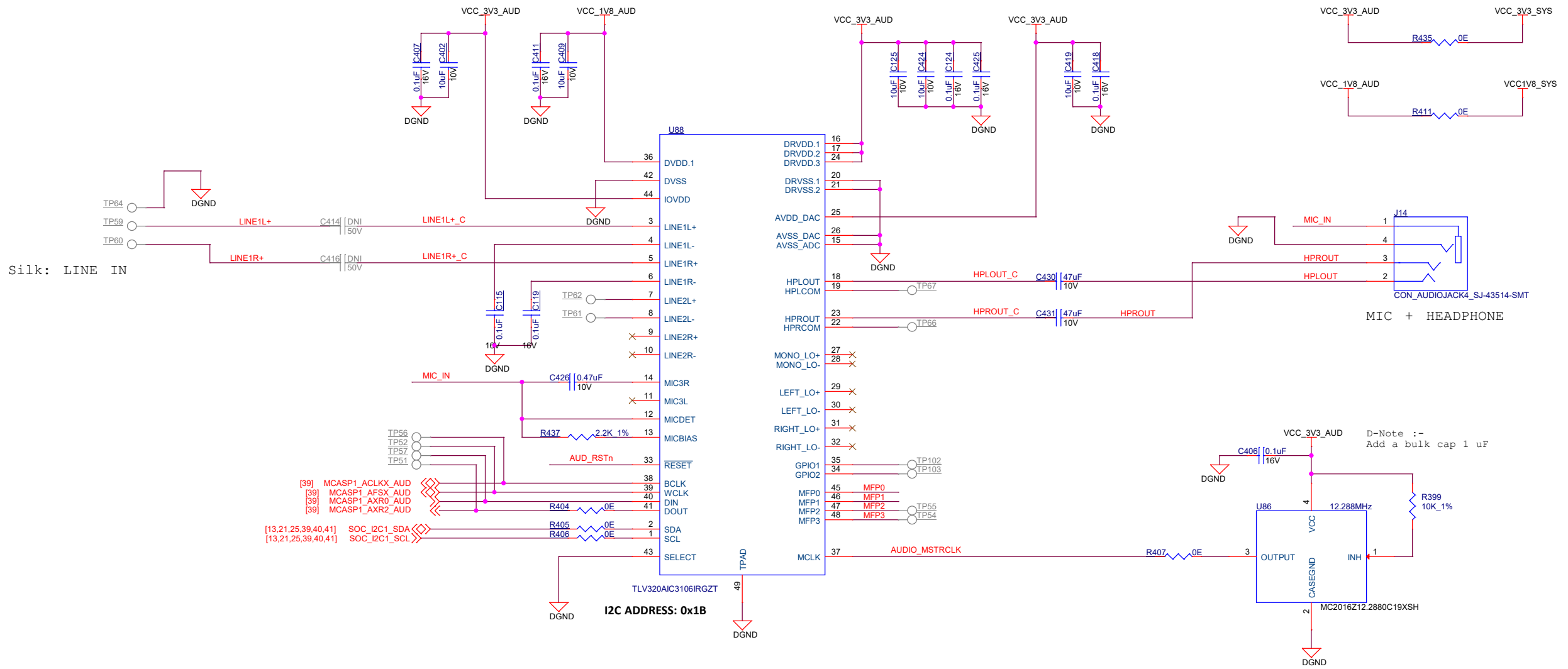
Size PROC135A

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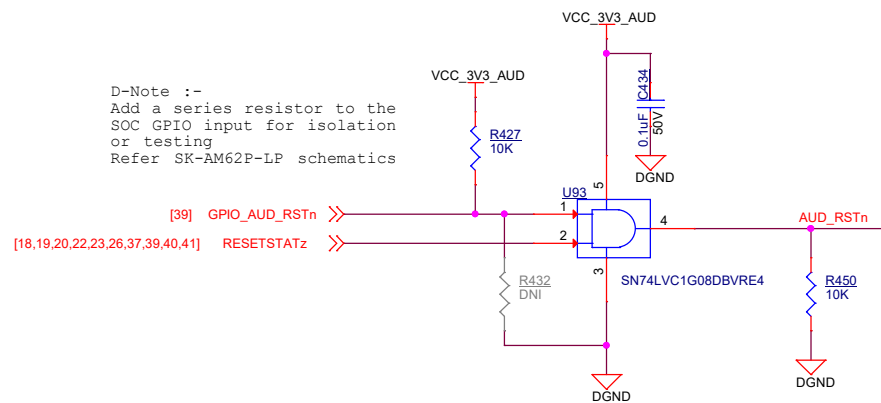
Rev A

## AUDIO CODEC

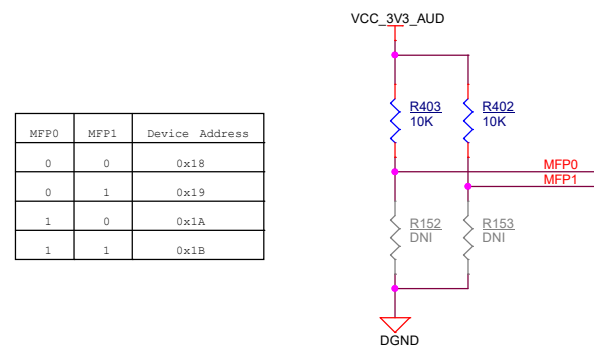


## AUDIO CODEC RESET

D-Note :-  
Add a series resistor to the  
SOC GPIO input for isolation  
or testing  
Refer SK-AM62P-LP schematics



## CODEC I2C ADDRESS SELECTION



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Title	AUDIO CODEC
-------	-------------

Size	PROC135A
C	

Date: Tuesday, June 11, 2024

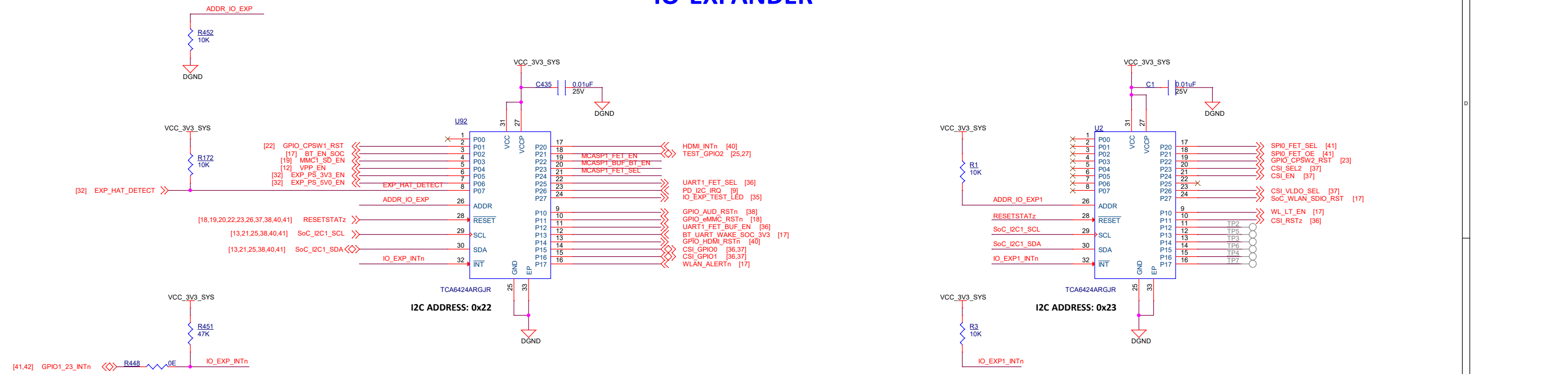
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Rev
A

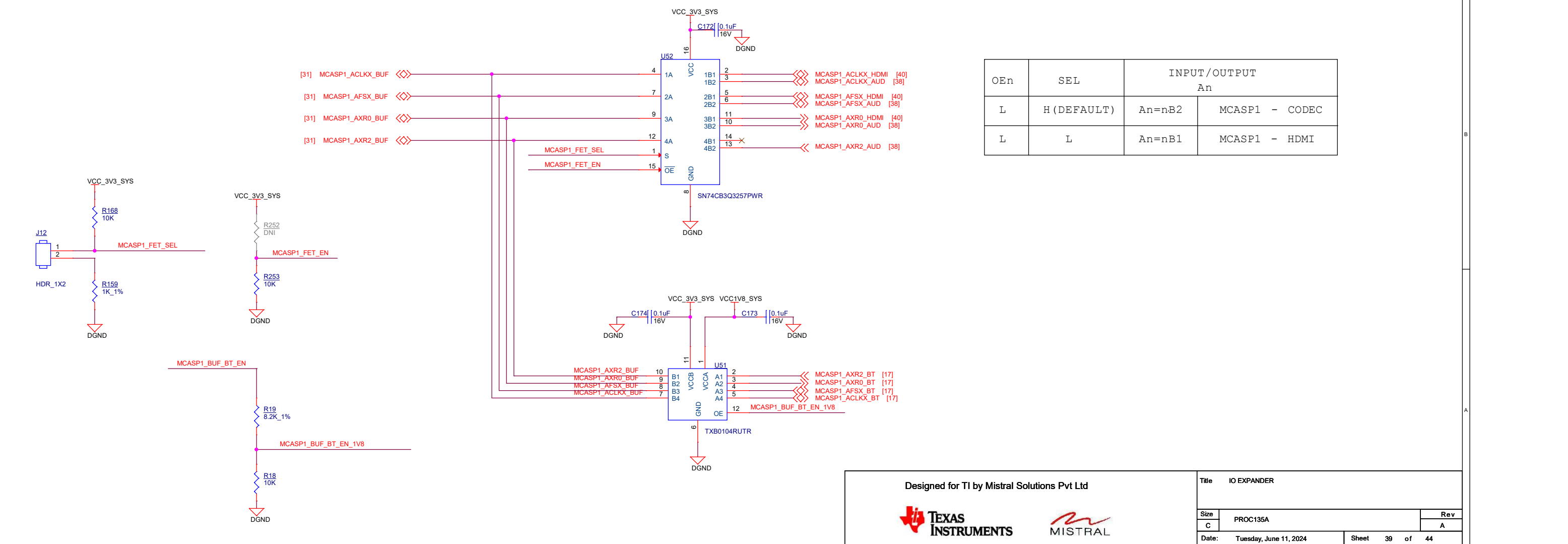
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IO EXPANDER



McASP1 FET SWITCH & BUFFER



OEn	SEL	INPUT/OUTPUT	
		An	
L	H (DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

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Title IO EXPANDER

Size C  
PROC135A

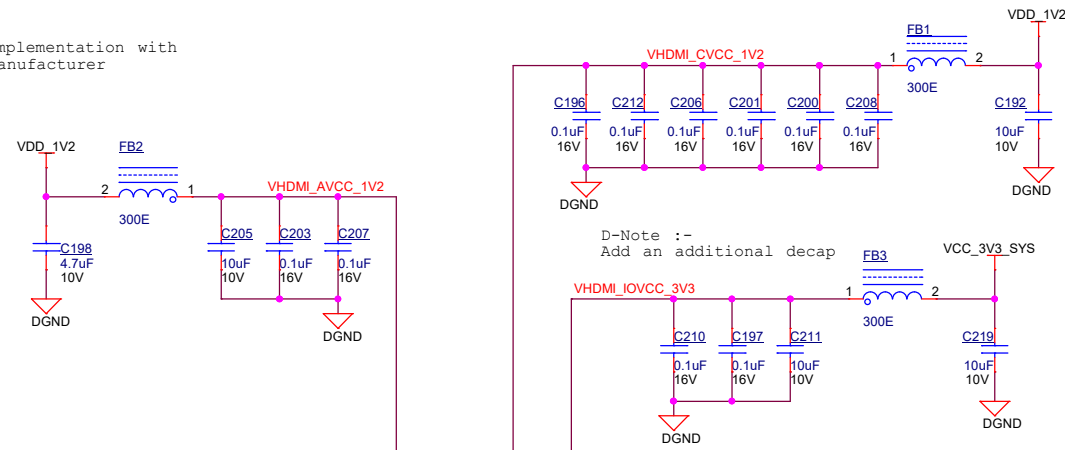
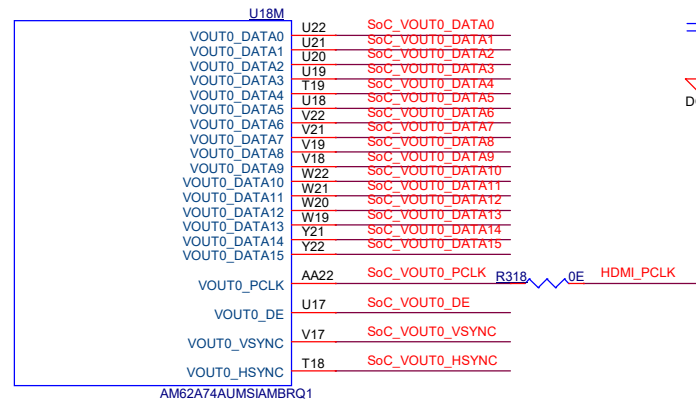
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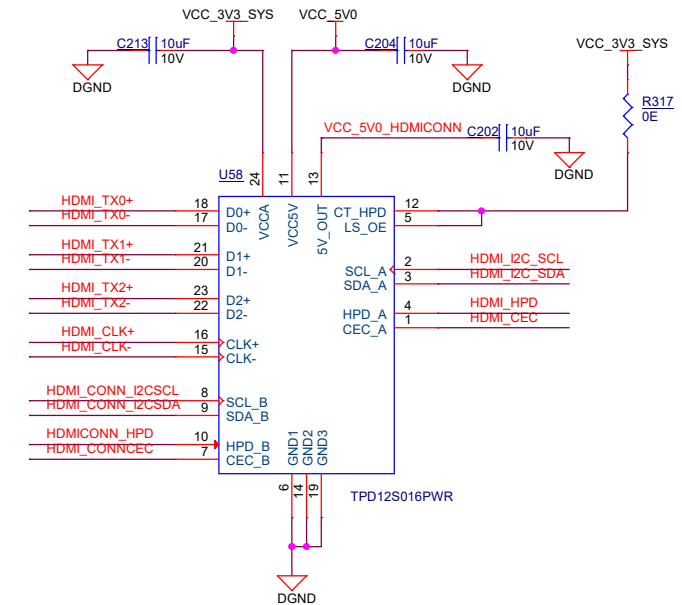
# HDMI INTERFACE

R-Note :-  
Verify the implementation with  
the device manufacturer



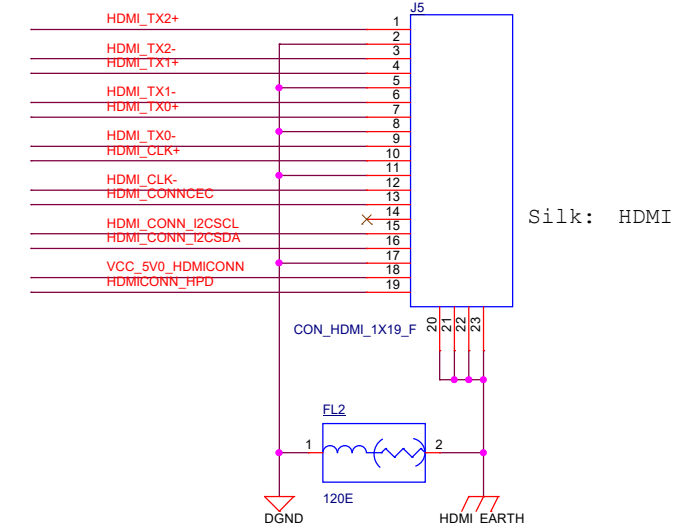
D-Note :-  
Add a bulk caps

## HDMI ESD DEVICE



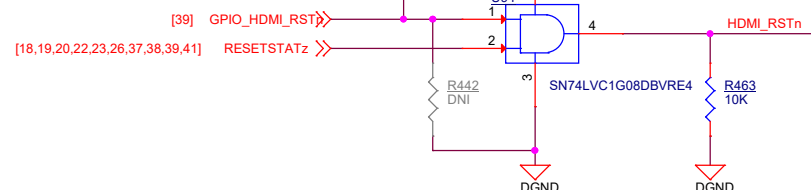
R-Note :-  
TPD12S016PWR has integrated pullup or pulldown resistors on the  
I2C and HPD lines hence no external pullup or pulldown required.

## HDMI CONNECTOR



## HDMI RESET

D-Note :-  
Add a series resistor to the  
SOC GPIO input for isolation  
or testing  
Refer SK-AM62P-LP schematics



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Title HDMI INTERFACE

Size PROC135A

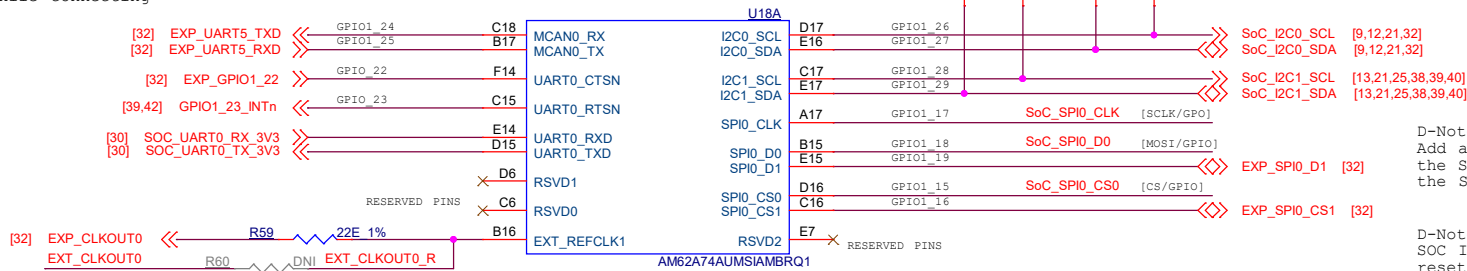
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Rev A

D-Note :-  
The TXD and RXD net names for UART  
are reverse with respect to  
MCAN(Refer pin attributes section of  
the data sheet)  
Take note while connecting

## SOC - GENERAL

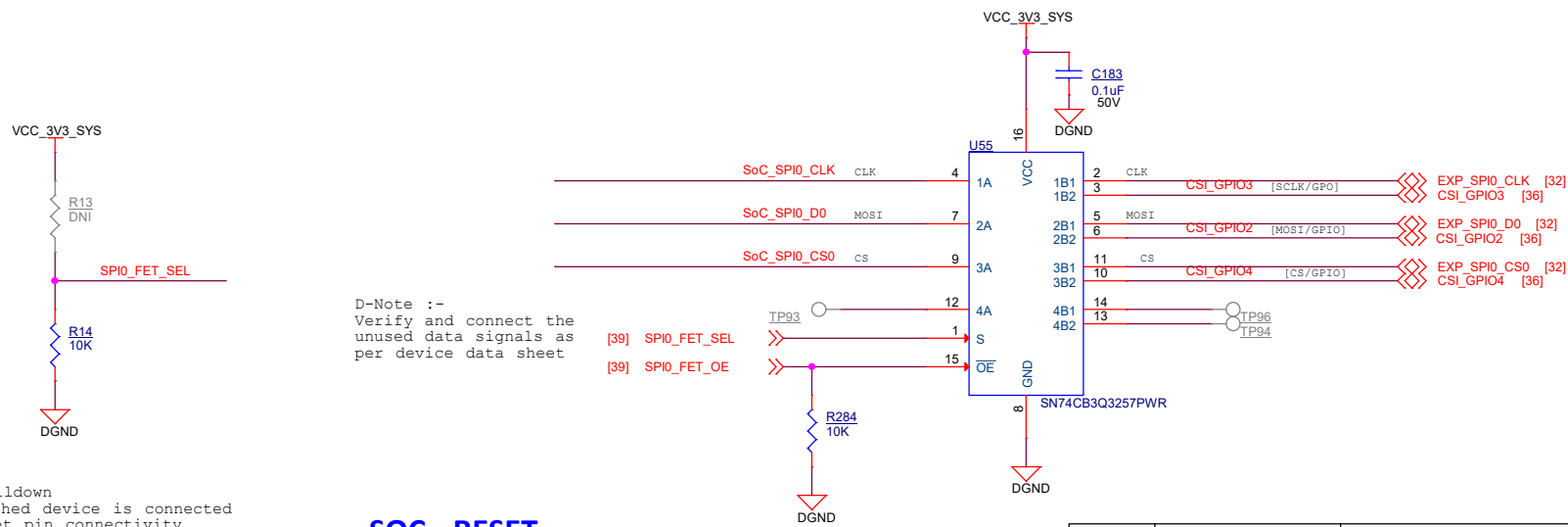


D-Note :-  
Ext Refclk1 used as Clkout0  
A clock signal should always be connected  
point to point without any branches. When  
connecting Clkout0 to more than one  
(multiple) clock inputs, use a buffer with  
one input and multiple outputs.

D-Note :-  
Add a series resistor 22R for  
the SPI0 clock output near to  
the SOC

D-Note :-  
SOC IO buffers are off during  
reset. A pull is recommended  
near to the attached device that  
is being driven by the SOC IO

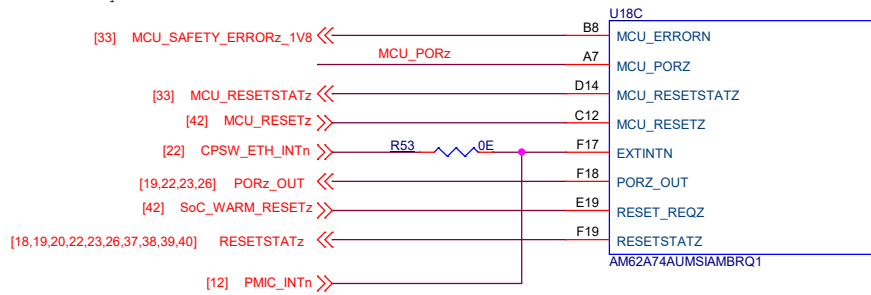
## SoC SPI0 FET SWITCH



D-Note :-  
Verify and connect the  
unused data signals as  
per device data sheet

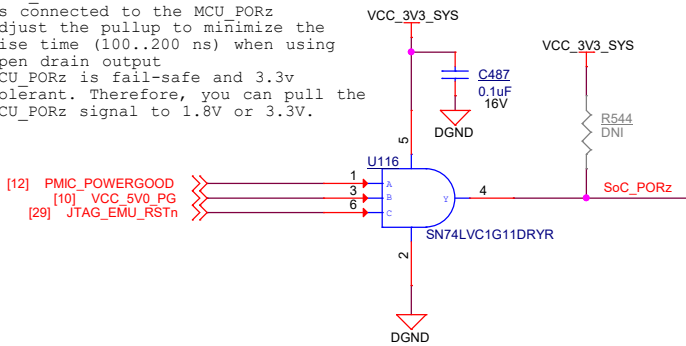
D-Note :-  
Provision for a pulldown  
Populate when attached device is connected  
Refer SOC data sheet pin connectivity  
requirements

## SOC - RESET



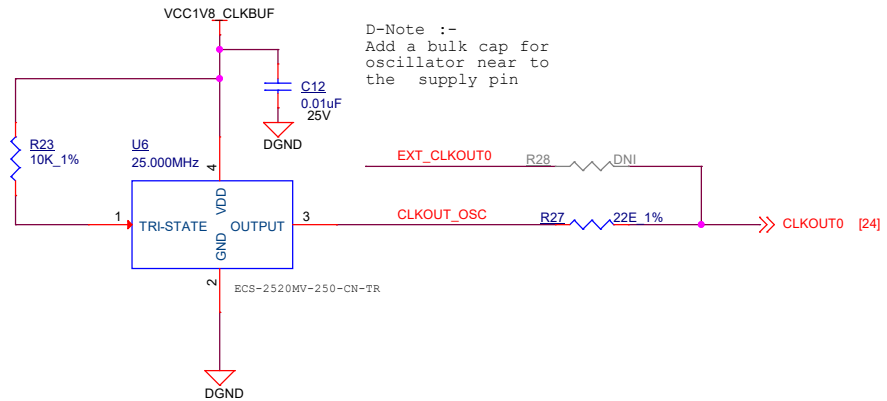
D-Note :-  
Open drain output type IO EXTINTn has slew rate limit specified when  
pulled to 3.3V supply. Add an RC at the input. Refer TMDs64EVM.

D-Note :-  
MCU\_PORz input have a maximum  
rise/fall time requirements when  
PMIC\_POWERGOOD  
is connected to the MCU\_PORz  
Adjust the pullup to minimize the  
rise time (100..200 ns) when using  
open drain output  
MCU\_PORz is fail-safe and 3.3v  
tolerant. Therefore, you can pull the  
MCU\_PORz signal to 1.8V or 3.3V.

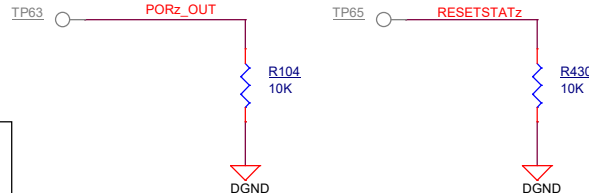
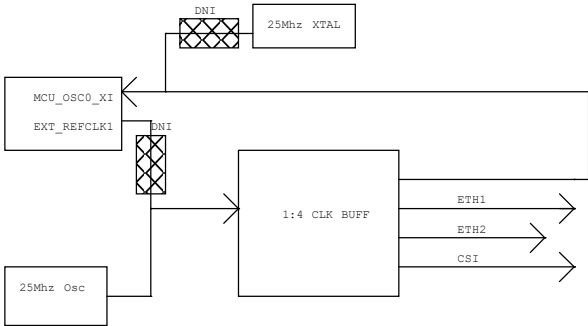


## OSCILLATOR

D-Note :-  
Refer SOC data sheet  
for oscillator specs

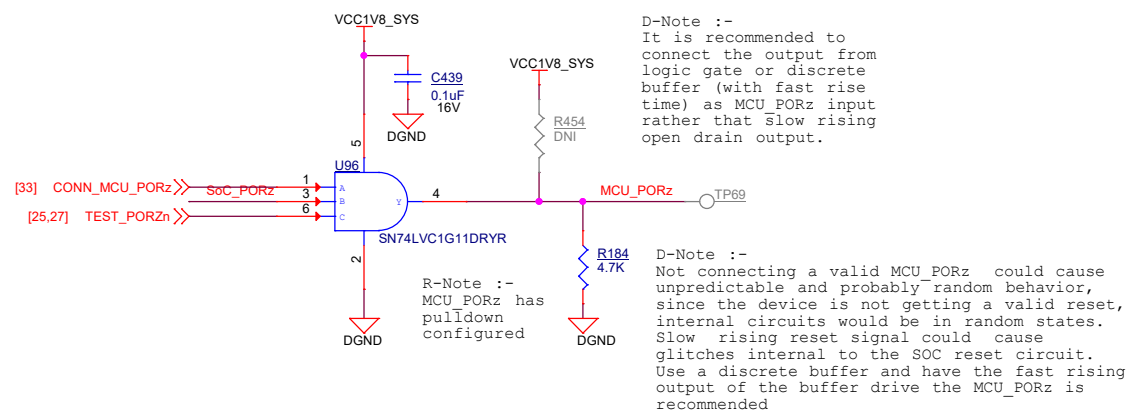


D-Note :-  
Add a bulk cap for  
oscillator near to  
the supply pin



D-Note :-  
Pull-down resistor on PORz\_OUT and  
RESETSTATz is provided to hold the  
attached device in reset condition  
during SOC reset and power-up

## MCU POWER ON RESET



D-Note :-  
It is recommended to  
connect the output from  
logic gate or discrete  
buffer (with fast rise  
time) as MCU\_PORz input  
rather than slow rising  
open drain output.

R-Note :-  
MCU\_PORz has  
pulldown  
configured

D-Note :-  
Not connecting a valid MCU\_PORz could cause  
unpredictable and probably random behavior,  
since the device is not getting a valid reset,  
internal circuits would be in random states.  
Slow rising reset signal could cause  
glitches internal to the SOC reset circuit.  
Use a discrete buffer and have the fast rising  
output of the buffer drive the MCU\_PORz is  
recommended

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Title OSCILLATOR

Size PROC135A

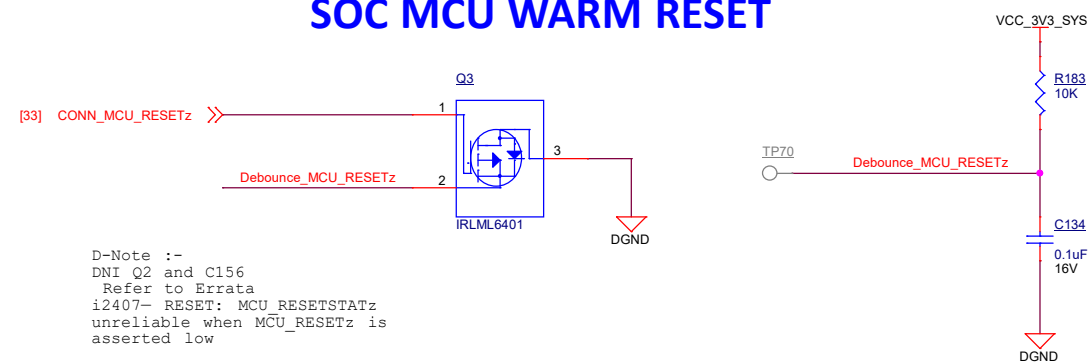
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Rev A

## EXTERNAL RESET INPUT AND SCHMITT TRIGGER DEBOUNCE LOGIC

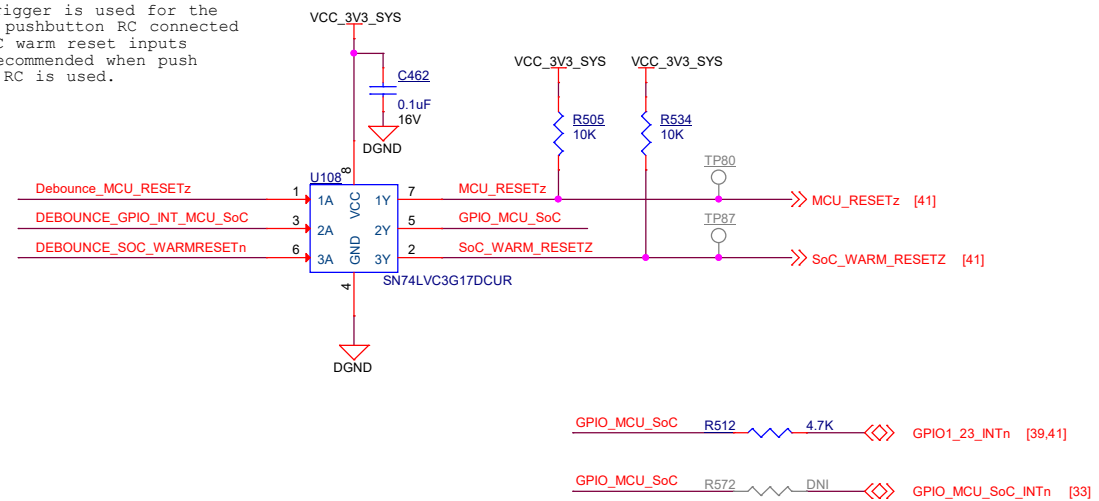
## SOC MCU WARM RESET



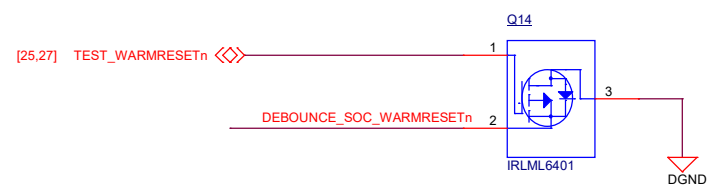
D-Note :-  
DNI Q2 and C156  
Refer to Errata  
i2407- RESET: MCU\_RESETSTATz  
unreliable when MCÜ\_RESETz is  
asserted low

## DEBOUNCE CIRCUIT

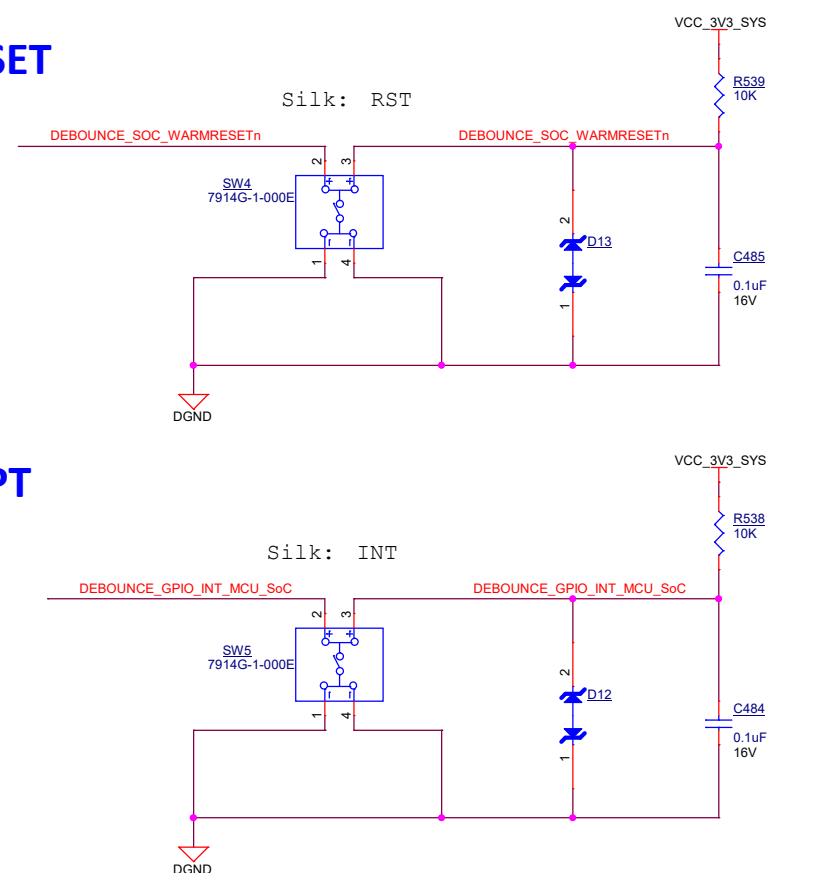
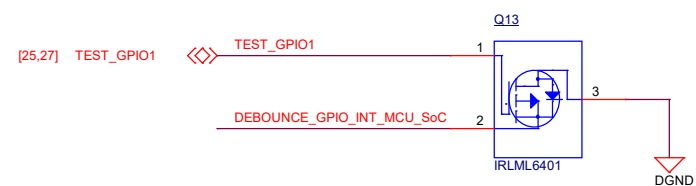
D-Note :-  
LVC MOS inputs have slew rate specifications  
Schmitt trigger is used for the slow ramp pushbutton RC connected to the SOC warm reset inputs  
This is recommended when push button or RC is used.



## SOC WARM RESET



## USER INTERRUPT



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Title	RESET
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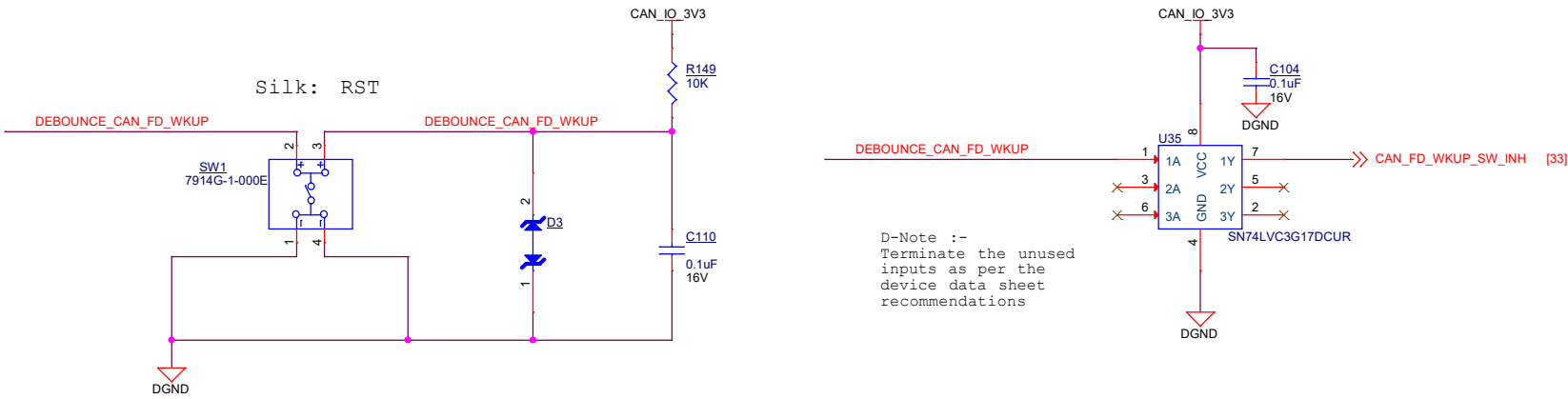
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C	

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A

CAN-FD FAST WAKE UP SW



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MOUNTING HARDWARE

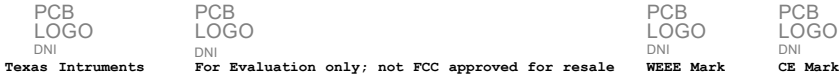
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB



LOGOs



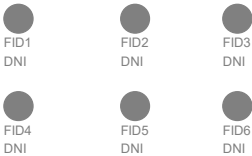
AM62A SOCKET



JUMPERS



FIDUCIALS



LABELS



SCREW & WASHER FOR PCIe M.2



D-Note :-  
Refer STRAP CONFIGURATION OF  
ETHERNET PHYS page from  
SK-AM64B schematics

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Title     HARDWARE SCHEMATICS

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