

AM263P CC
PROC159B(001)

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REVISION HISTORY

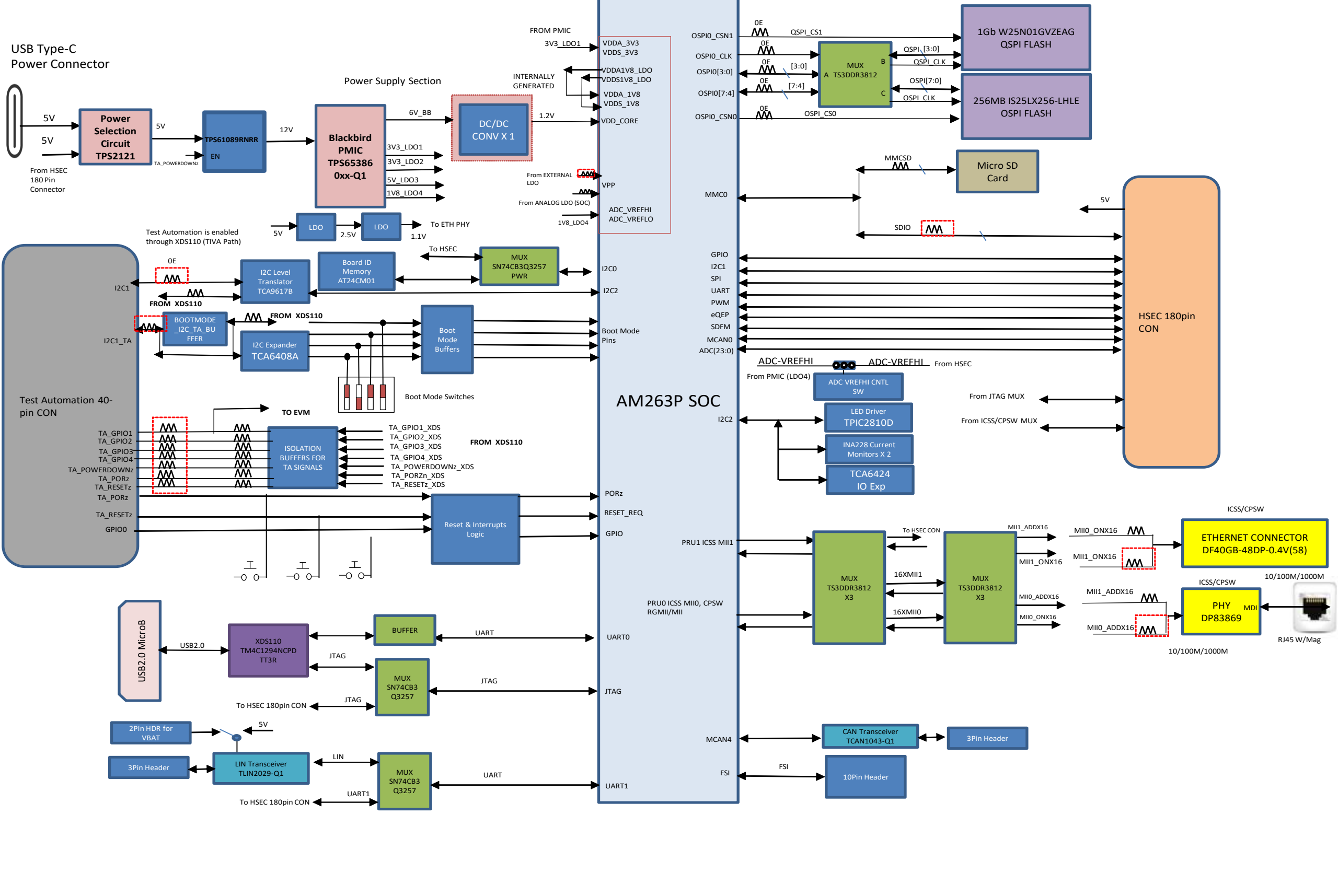
VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	3 FEB 2025	Drafted from REV A Schematics. Changed Boost converter U5 with part# TPS61089RNRR and changed Q21 (OSPI Reset) from N Channel Fet to P channel FET. Changed U76 Standard PUSH PULL OUTPUT Buffer to OPEN DRAIN OUTPUT BUFFER	Mistral Design Team		
0.02					
0.03					
0.04					

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SYSTEM BLOCK DIAGRAM



POWER SEQUENCE

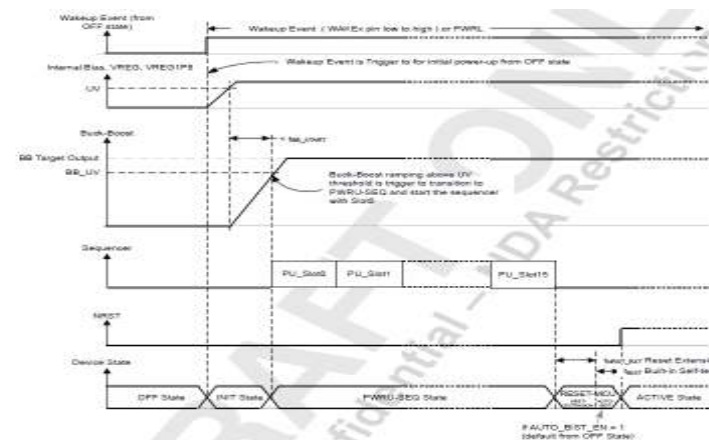
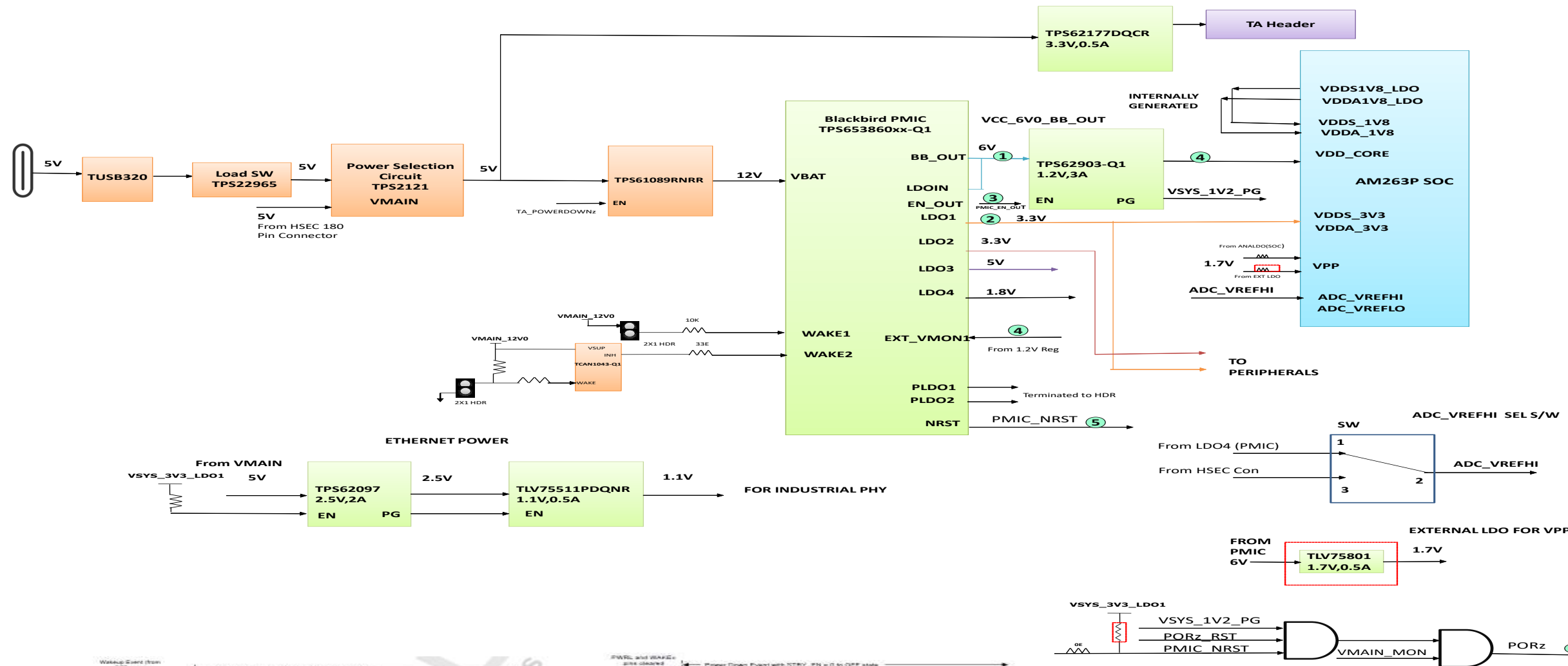


Figure 9-6. Power-Up from OFF state Example

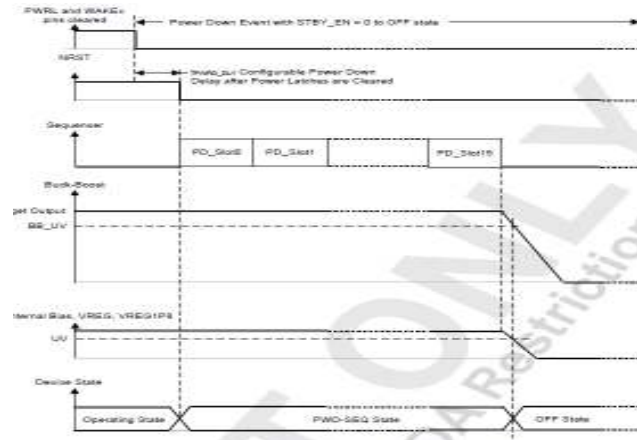
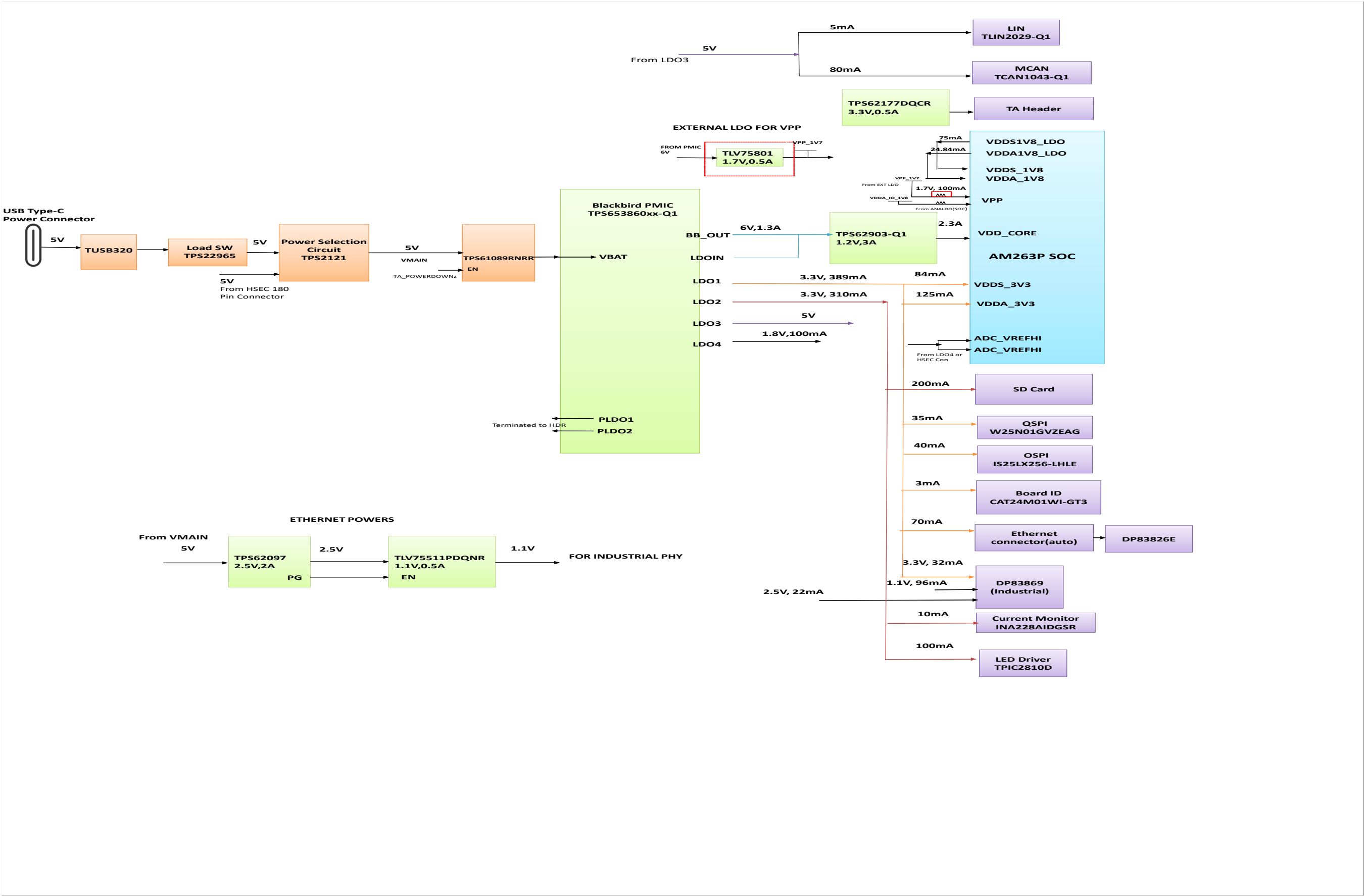


Figure 9-8. Power-Down to OFF state Example

POWER FLOW DIAGRAM



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Title POWER FLOW DIAGRAM

Size

C

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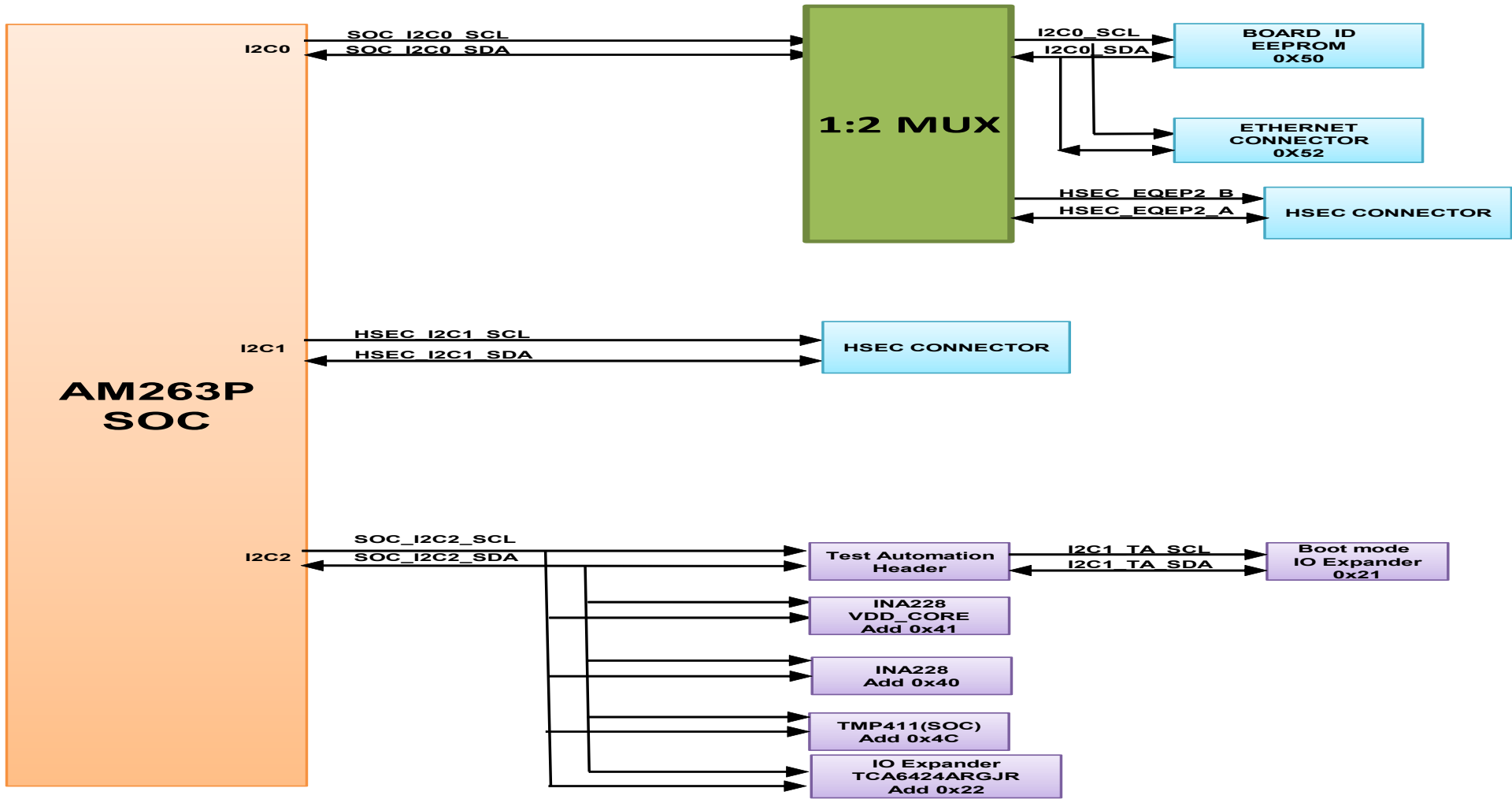
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I2C TREE DIAGRAM

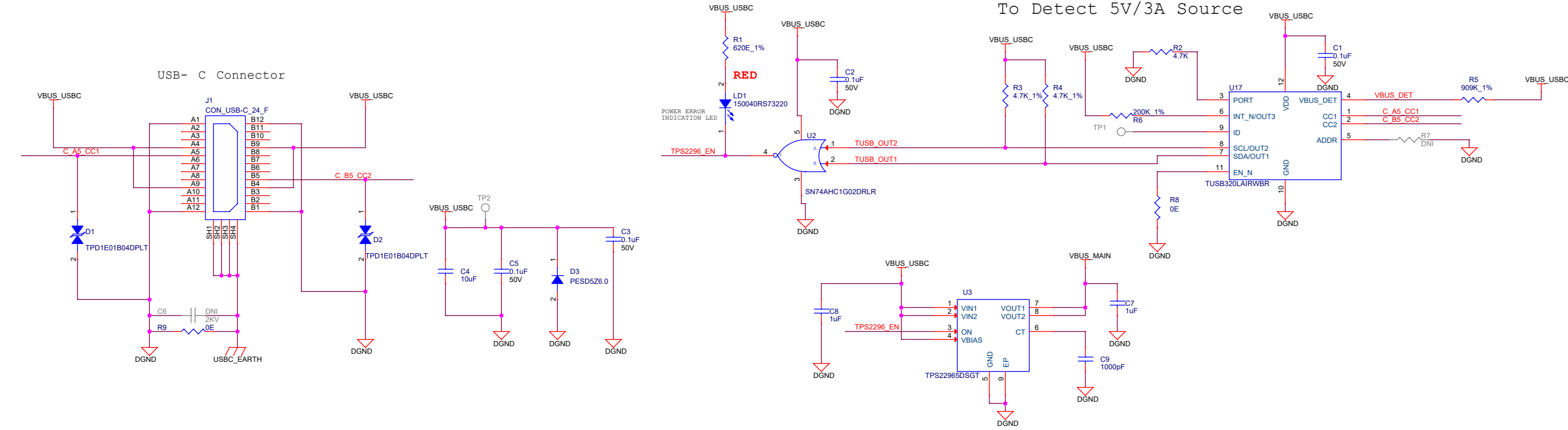


GPIO MAPPING TABLE

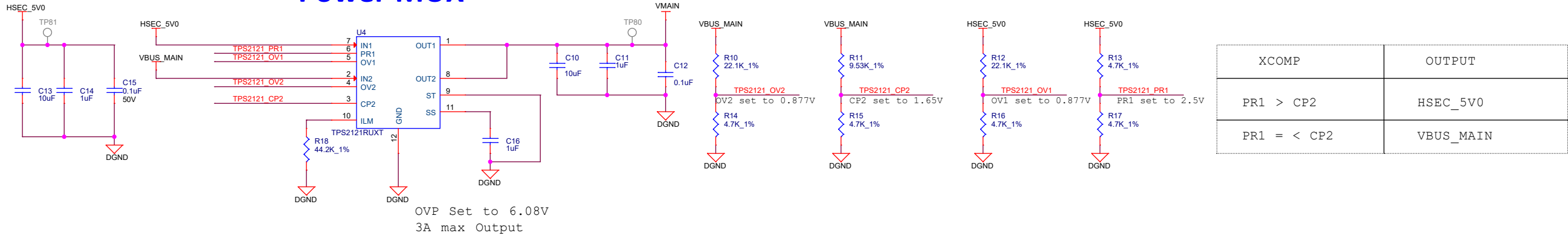
SI No.	GPIO DESCRIPTION	GPIO	Pin Name	FUNCTIONALITY	Net Name	ACTIVE STATE
1	Interrupt To SoC	GPIO21	LIN2_RXD	Interrupt	SOC_INTn	LOW
2	Interrupt To DP83826E/DP83TG720	GPIO67	EPWM12_A	Interrupt	ICSSM2_PWDN/INTn	LOW
3	User Defined LED	GPIO66	EPWM11_B	GPIO	USER_LED1	PREFERABLE
4	Interrupt To DP83869	GPIO68	EPWM12_B	Interrupt	ICSSM1_INT	LOW
5	User Defined LED	GPIO22	LIN2_TXD	GPIO	USER_LED0	PREFERABLE
6	Reset input to DP83869	GPIO35	RGMII1_TXC	Reset	GPIO_ICSSM1_RST	LOW
9	Reset input to Ethernet connector	GPIO36	RGMII1_TX_CTL	Reset	GPIO_ICSSM2_RST	LOW
10	Interrupt To SoC from PMIC	GPIO29	RGMII1_RXC	Interrupt	PMIC_INTn	LOW
11	Select line for OSPI and QSPI	GPIO37	RGMII1_TD0	Mux Selection	OSPI/QSPI_MUX_SEL	PREFERABLE
IO Expander 01						
13	Enable control to clock buffer		P01	Enable	CLK_BUF_EN	HIGH
14	Select line for ICSSM Ethernet/HSEC Mux (PRU1 signals)		P02	Mux Selection	ICSSM1_MUX_SEL	PREFERABLE
15	Select line for ICSSM ON-Board/ADD-ON PHY Mux		P03	Mux Selection	ICSSM2_MUX_SEL	PREFERABLE
16	Select line for MCAN and FSI MUX		P04	Mux Selection	FSI_MUX_SEL	PREFERABLE
17	Select line for ADC MUX 3		P05	Mux Selection	ADC3_MUX_SEL	PREFERABLE
18	Select line for ADC MUX 4		P06	Mux Selection	ADC4_MUX_SEL	PREFERABLE
19	Enable control to SD load switch		P07	Load SW Enable	GPIO_uSD_PWR_EN	HIGH
20	Select line for ADC MUX 5		P10	Mux Selection	ADC5_MUX_SEL	PREFERABLE
21	Select line for I2C0 MUX		P11	Mux Selection	I2C0_MUX_SEL	PREFERABLE
22	Select line for SPI1 MUX		P12	Mux Selection	SPI1_MUX_SEL	PREFERABLE
23	Select line for UART2 MUX		P13	MUX Selection	UART2_MUX_SEL	PREFERABLE
24	Enable control to 1.7V LDO		P14	LDO Enable	VPP_LDO_EN	PREFERABLE
25	Select line for LIN/UART MUX		P15	Mux Selection	LIN_MUX_SEL	PREFERABLE
26	Select line for ADC MUX 1		P16	Mux Selection	ADC1_MUX_SEL	PREFERABLE
27	Select line for ADC MUX 2		P17	Mux Selection	ADC2_MUX_SEL	PREFERABLE
28	GPIO to HSEC		P20	GPIO	HSEC_GPIO	PREFERABLE
29	Standby input to CAN tranciever		P21	GPIO	MCAN1_STB	HIGH
30	Select line for MDIO/MDC Mux sel 1		P22	Mux Selection	MDIO/MDC_MUX_SEL1	PREFERABLE
31	Select line for MDIO/MDC Mux sel 2		P23	Mux Selection	MDIO/MDC_MUX_SEL2	PREFERABLE
32	Select line for ICSSM Ethernet/HSEC Mux (PRU0 signals)		P24	Mux Selection	ICSSM0_MUX_SEL	PREFERABLE

USB-C Power

Configured as UFP MODE
To Detect 5V/3A Source

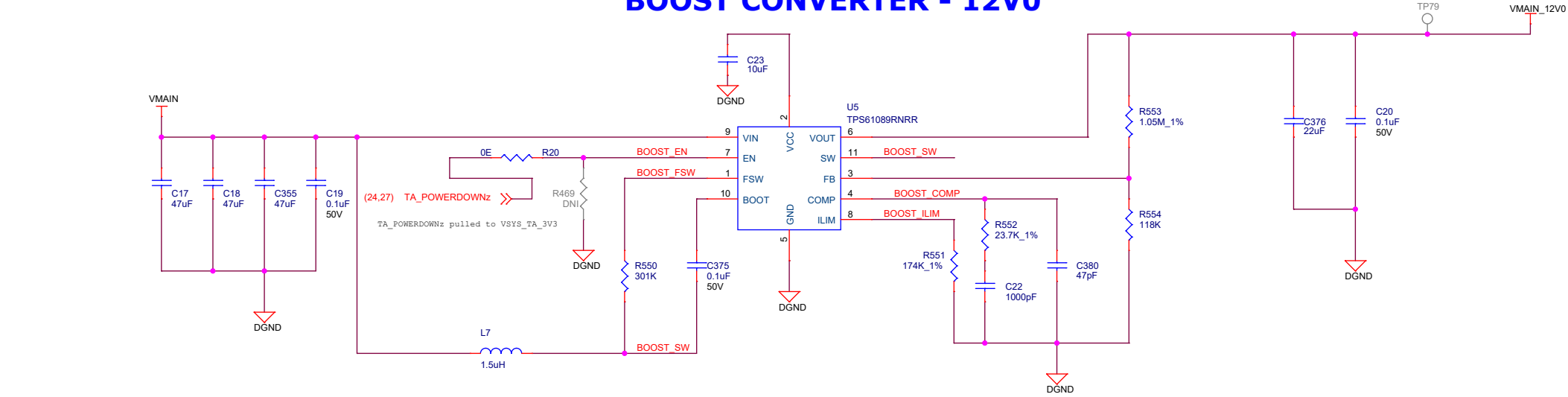


Power MUX



Designed as per reference sch

BOOST CONVERTER - 12V0



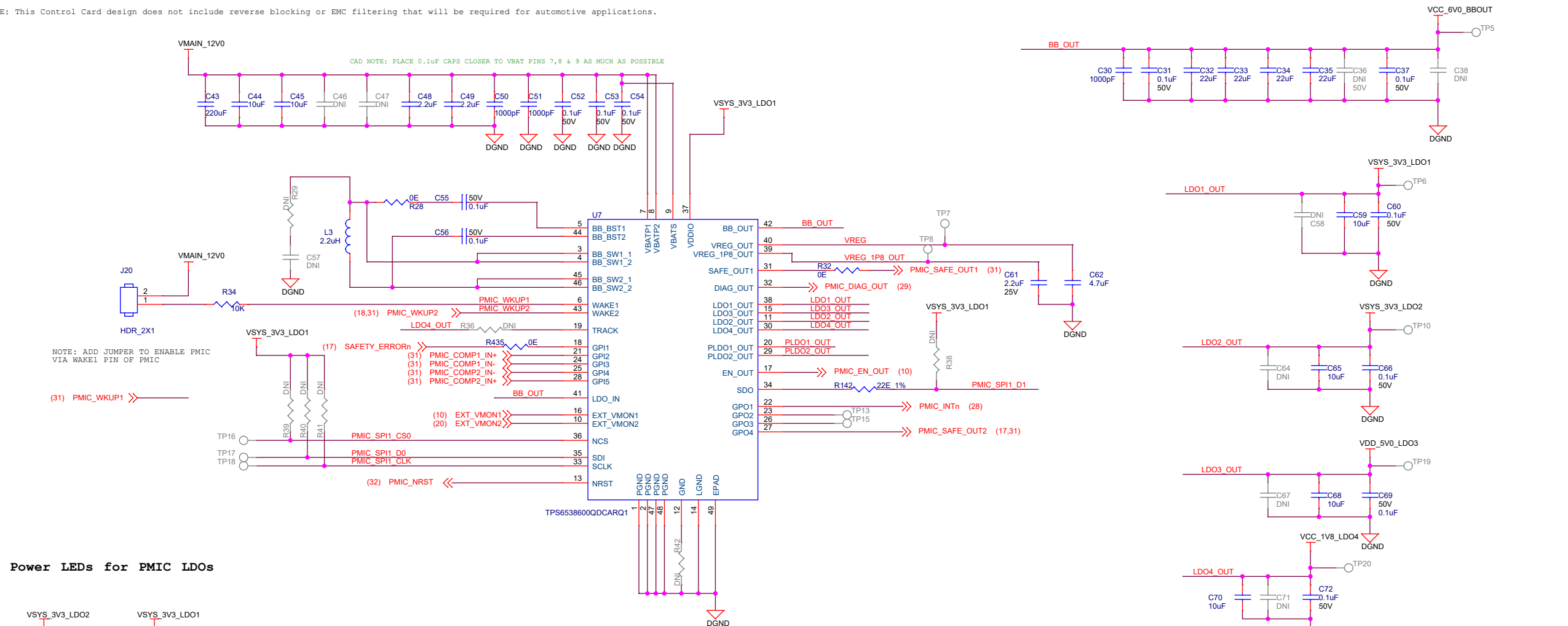
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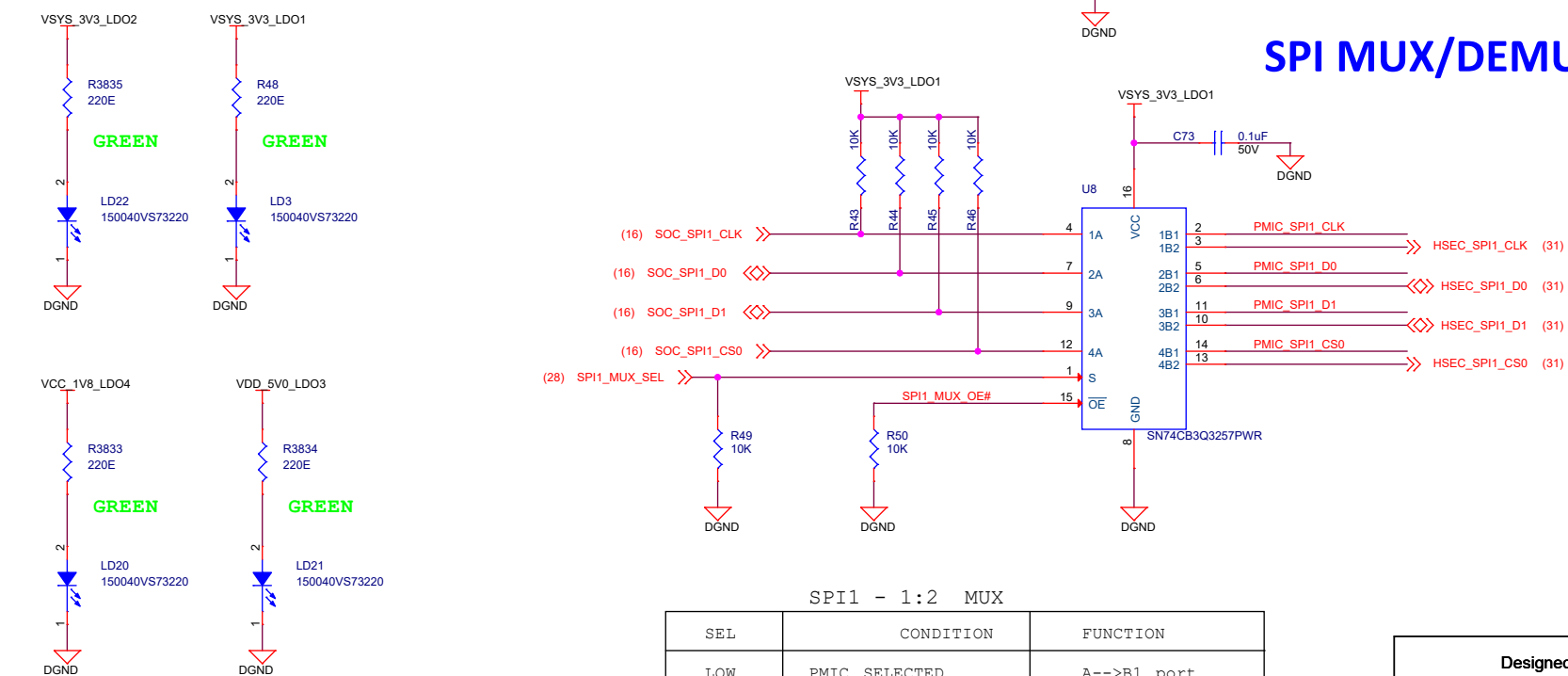
Title USB-C POWER		
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BLACKBIRD PMIC

NOTE: This Control Card design does not include reverse blocking or EMC filtering that will be required for automotive applications.



SPI MUX/DEMUX



SPI1 - 1:2 MUX		
SEL	CONDITION	FUNCTION
LOW	PMIC_SELECTED	A-->B1 port
HIGH	HSEC_SPI1_selected	A-->B2 port

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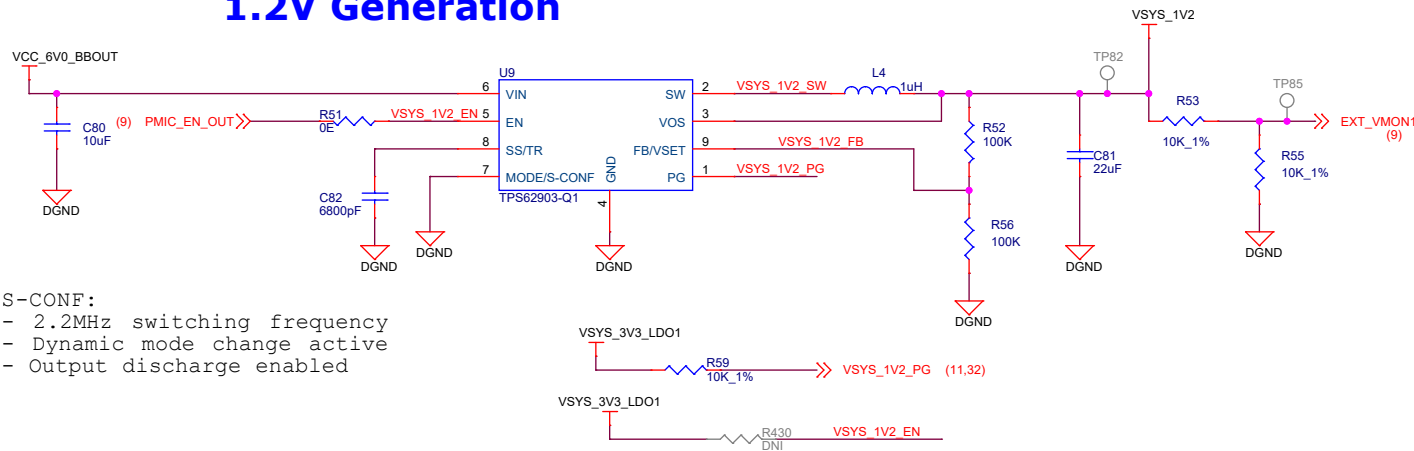


Title	BLACKBIRD PMIC
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Power Supply #1

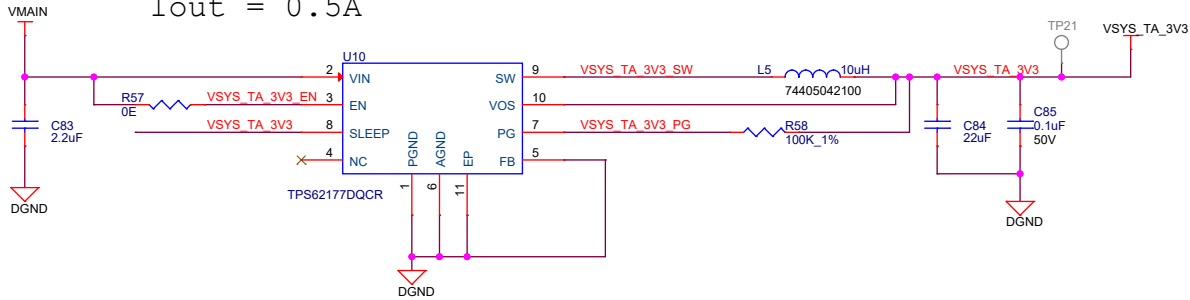
1.2V Generation



S-CONF:
- 2.2MHz switching frequency
- Dynamic mode change active
- Output discharge enabled

Test Automation Header Supply

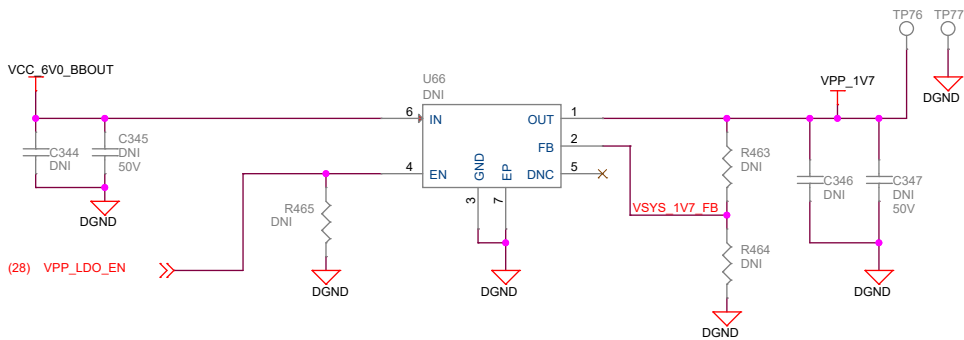
TPS62177 3.3V BUCK REGULATOR
Vout = 3.3V
Iout = 0.5A



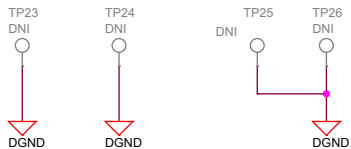
TLV75801
Vout=1.7V
Iout = .5A

1.7V VPP Generation

Place testpoints with
100mils spacing to
insert external jumper



Ground Test Points



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Title POWER SUPPLY #1

Size Variant Name = PROC159B(001)

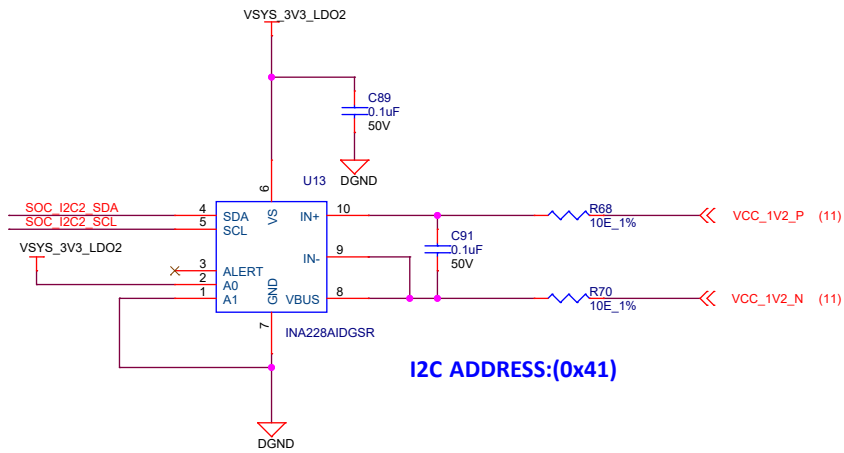
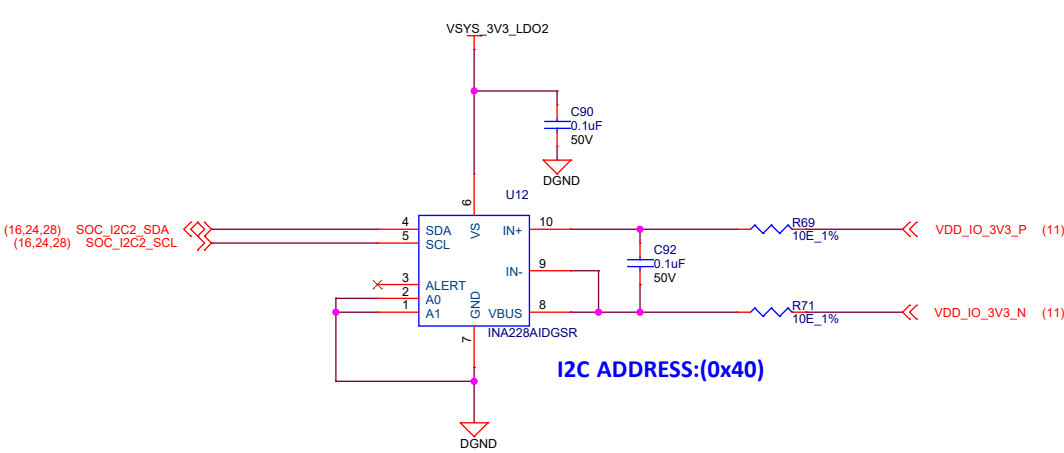
Rev

B

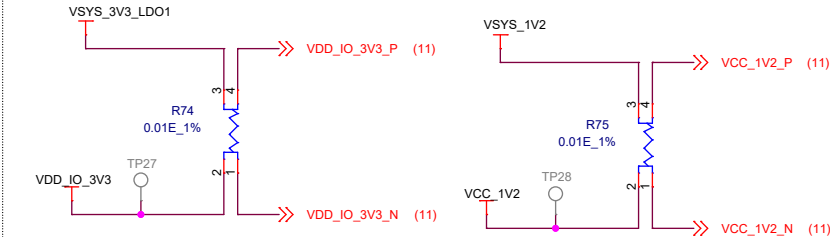
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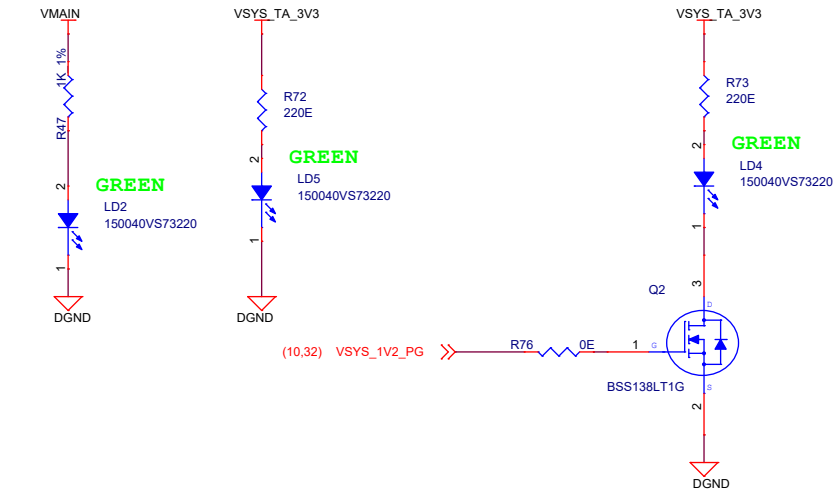
Current Monitors



Voltage In-Line Resistors



Power LEDs



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Title CURRENT MONITORING DEVICES

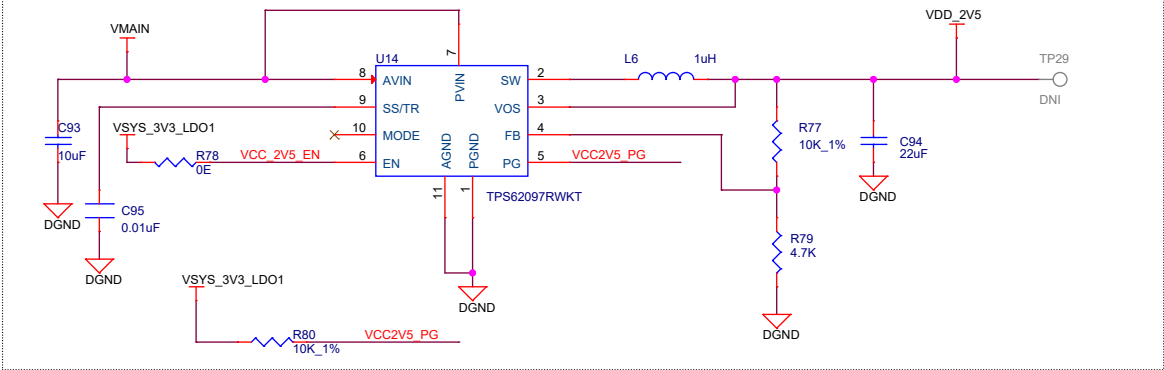
Size Variant Name = PROC159B(001)

Rev B

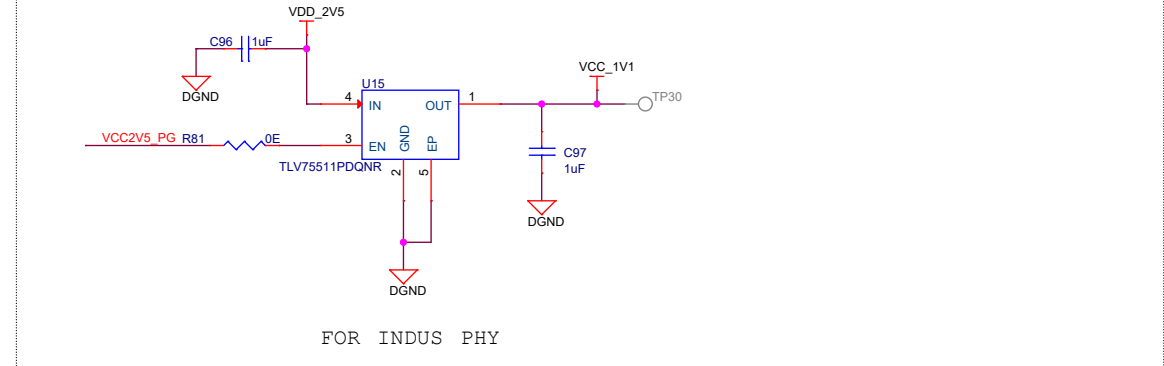
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Ethernet Powers

2.5V ETHERNET PHY POWER SUPPLY

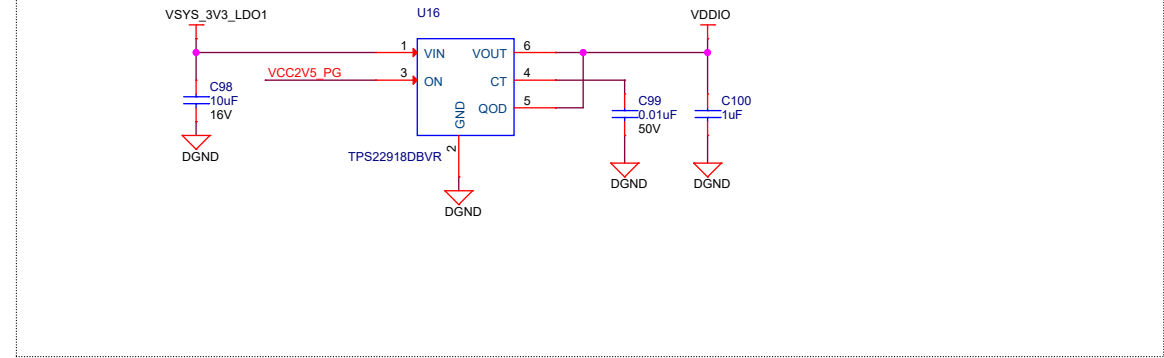


1.1V, 0.5AMPS SUPPLY



FOR INDUS PHY

Load Switch

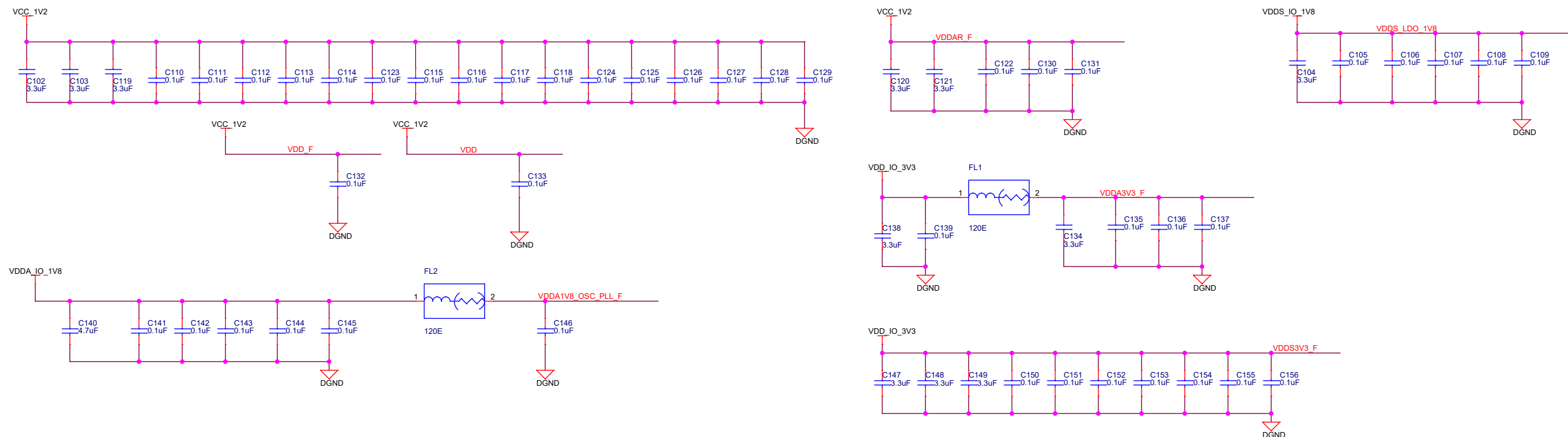
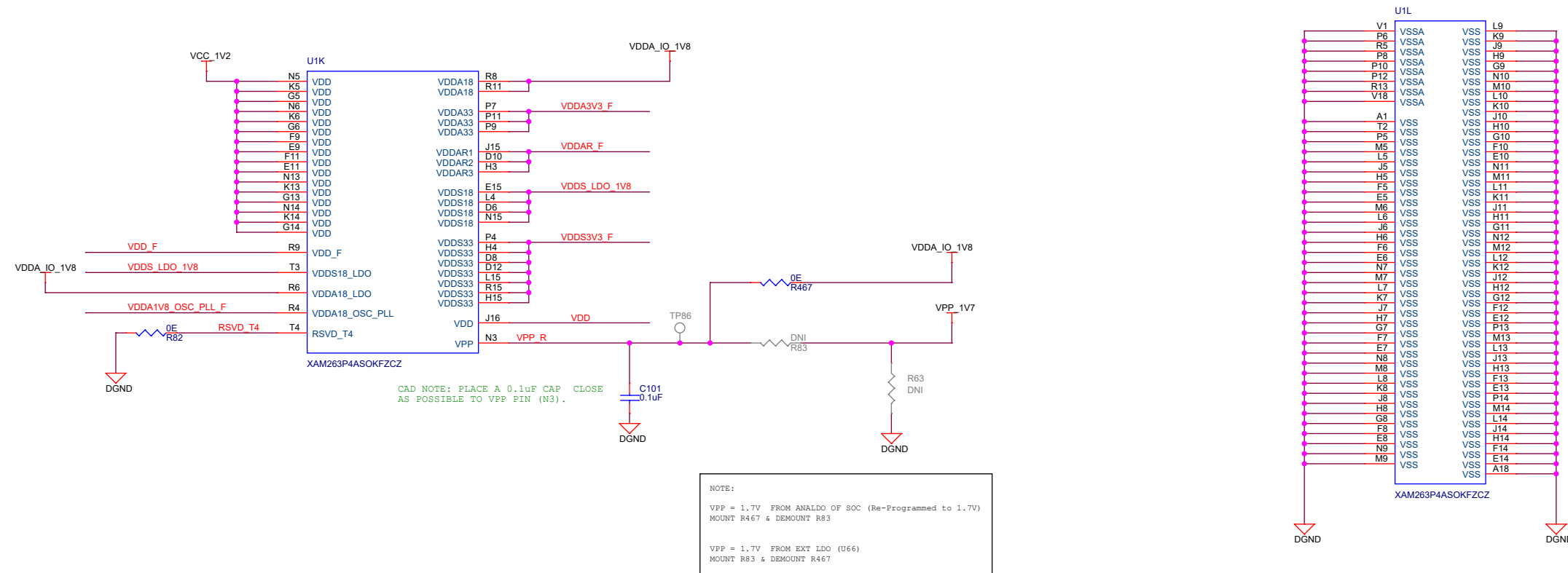


Designed for T1 by Mistral Solutions Pvt Ltd

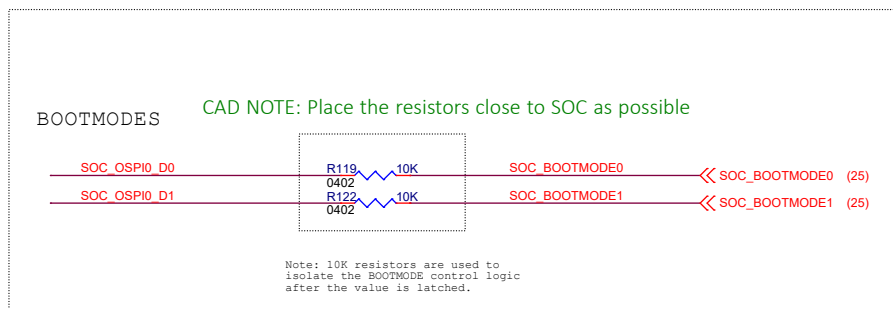
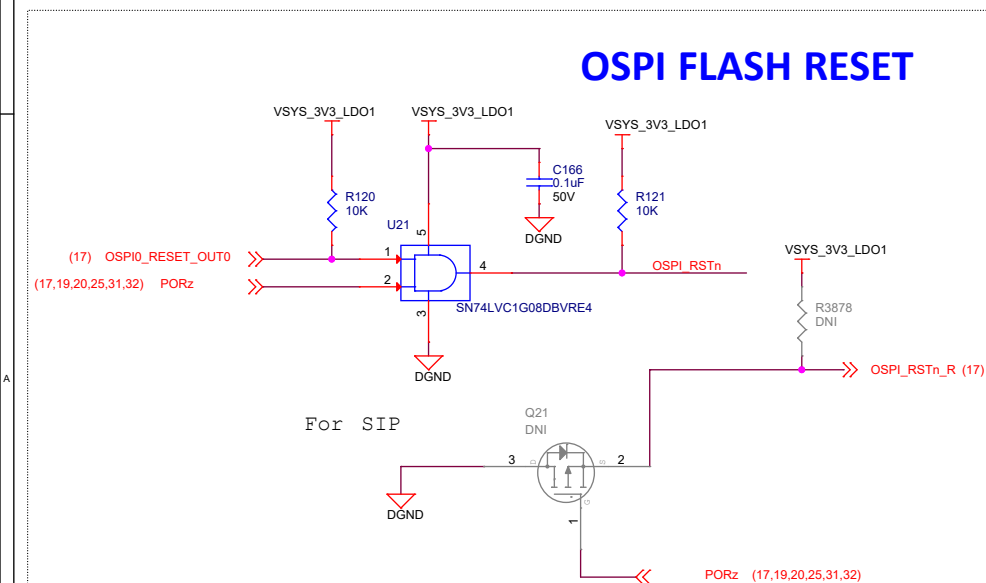
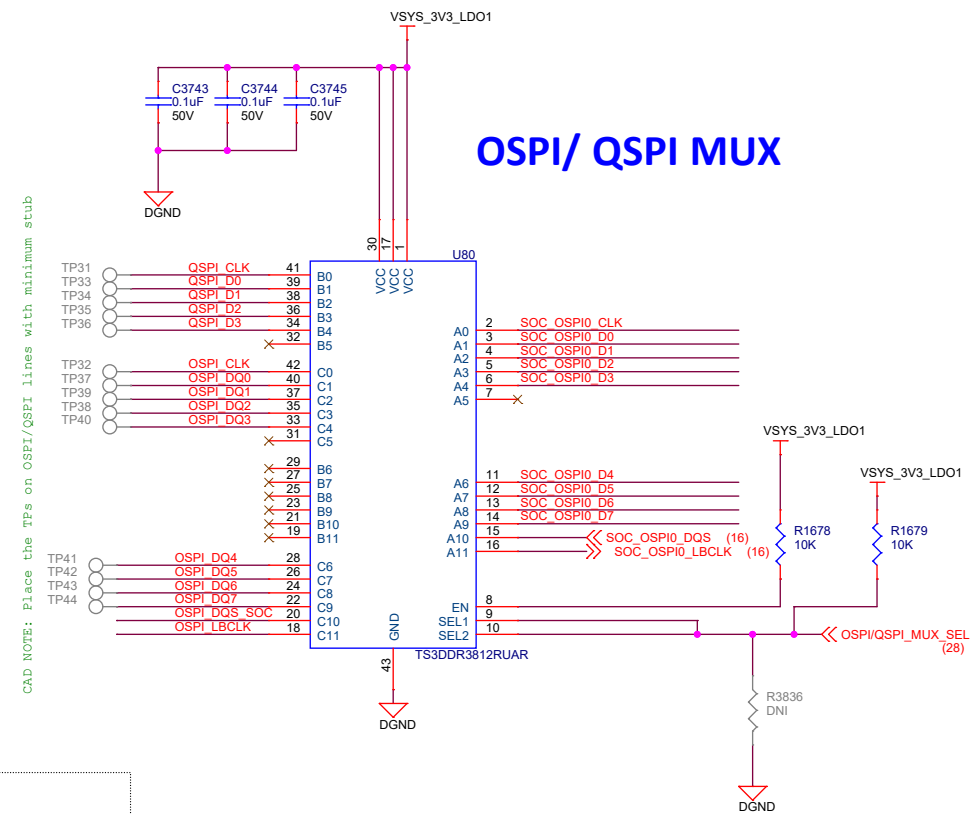
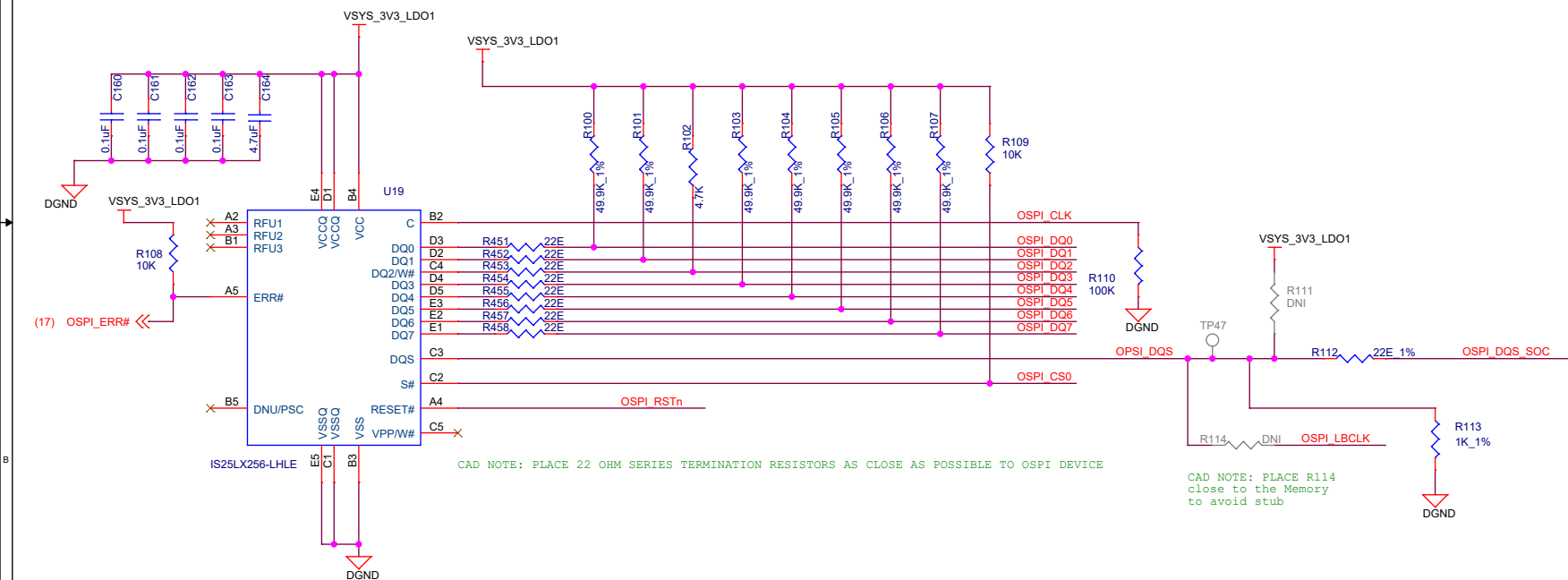
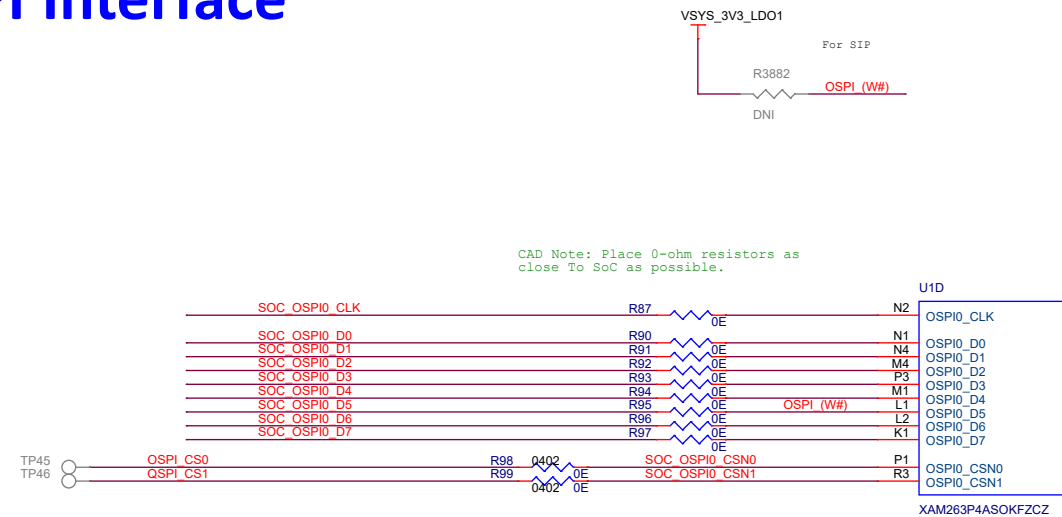
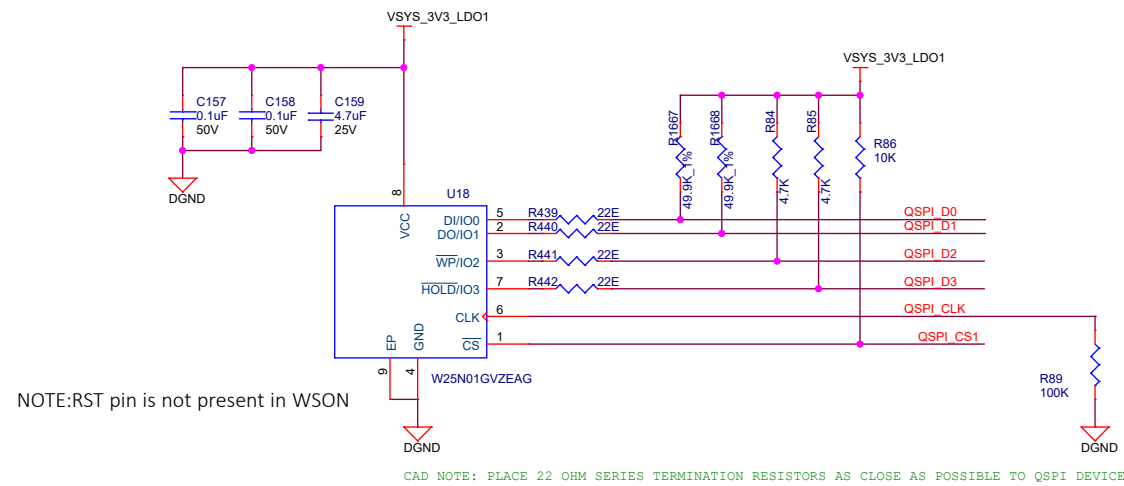


Title ETHERNET POWERS		
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SOC-POWER and GND

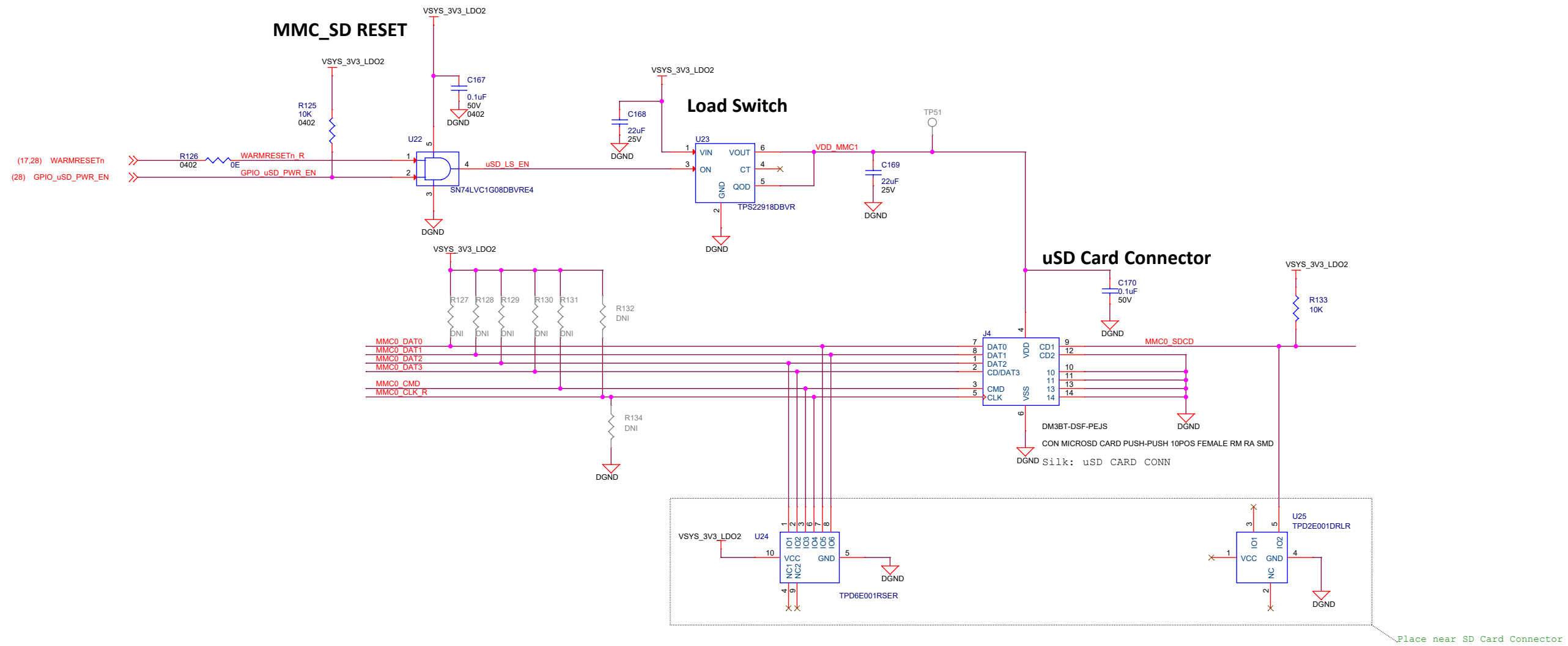
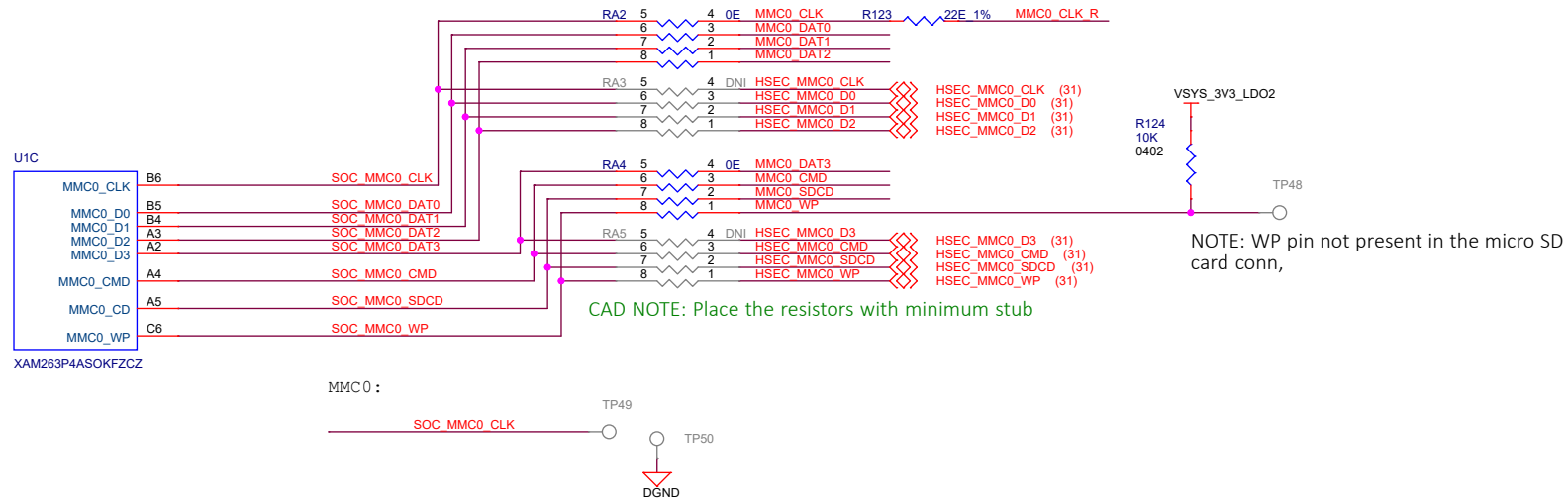


SOC - QSPI & OSPI Interface



SEL 1 & 2	CONDITION	FUNCTION
LOW	QSPI SELECTED	A-->B port
HIGH	OSPI selected	A-->C port

SOC- MMC0 Interface

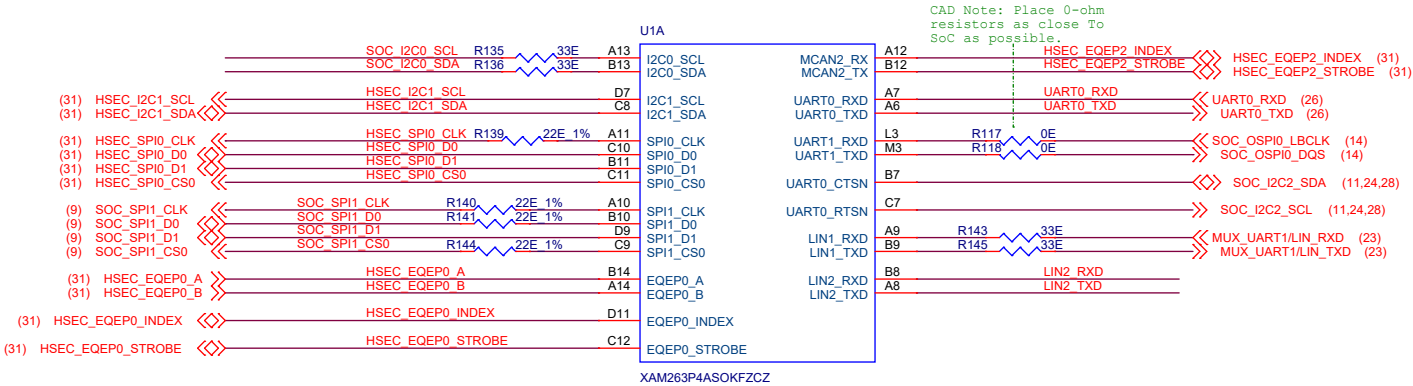


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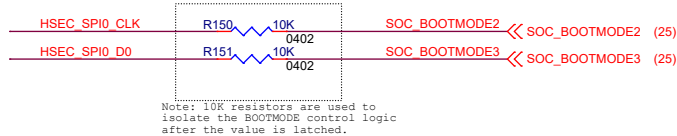


Title SOC- MMC0 Interface		
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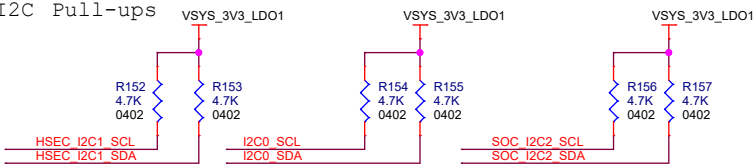
SOC-IO Interfaces



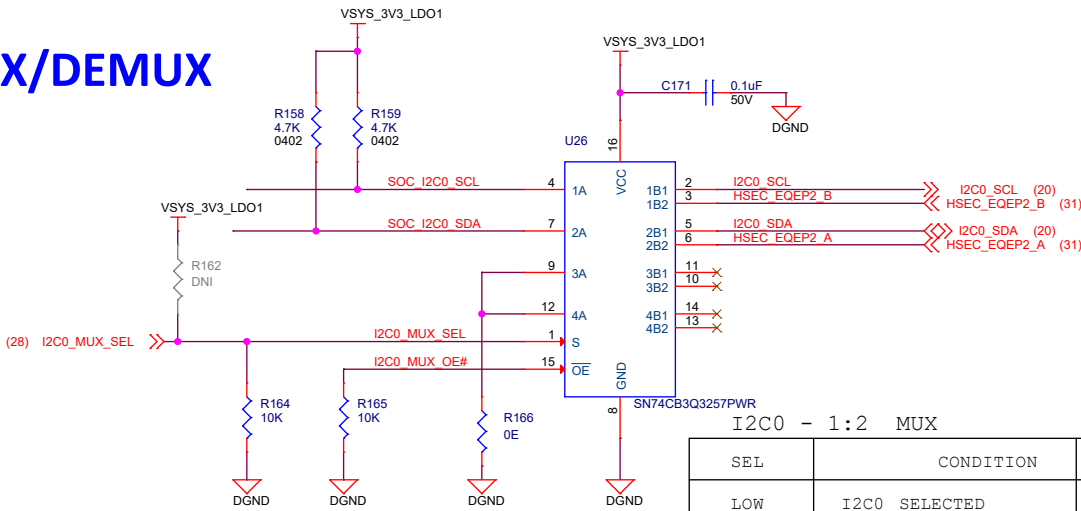
BOOTMODES



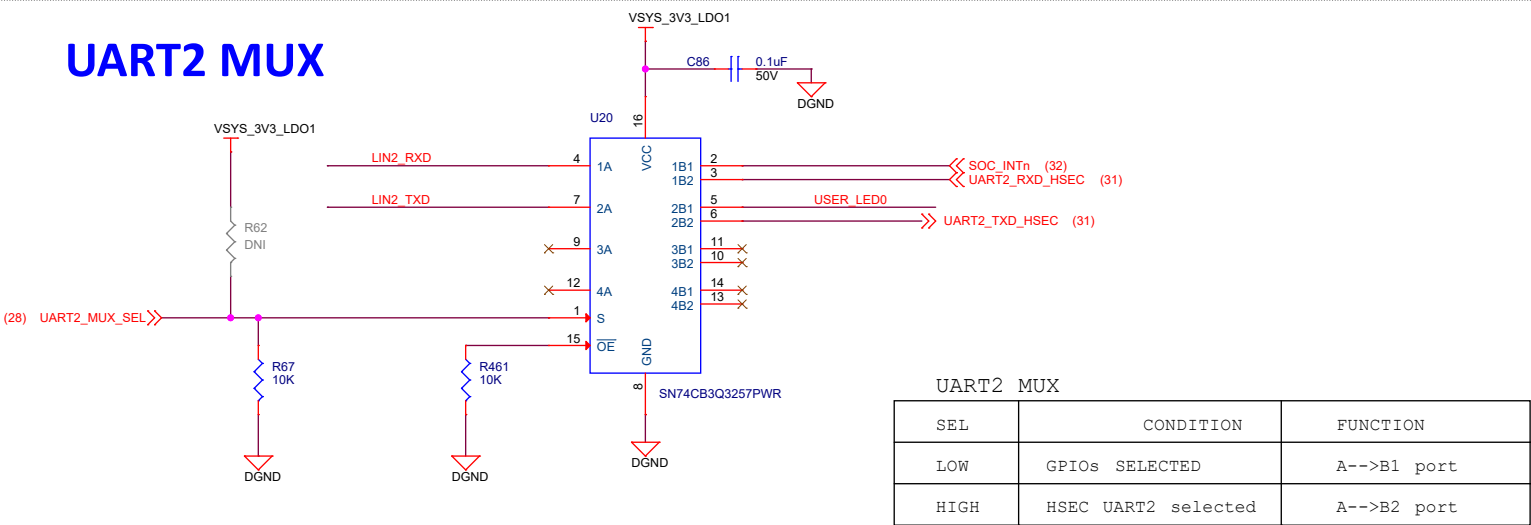
I2C Pull-ups



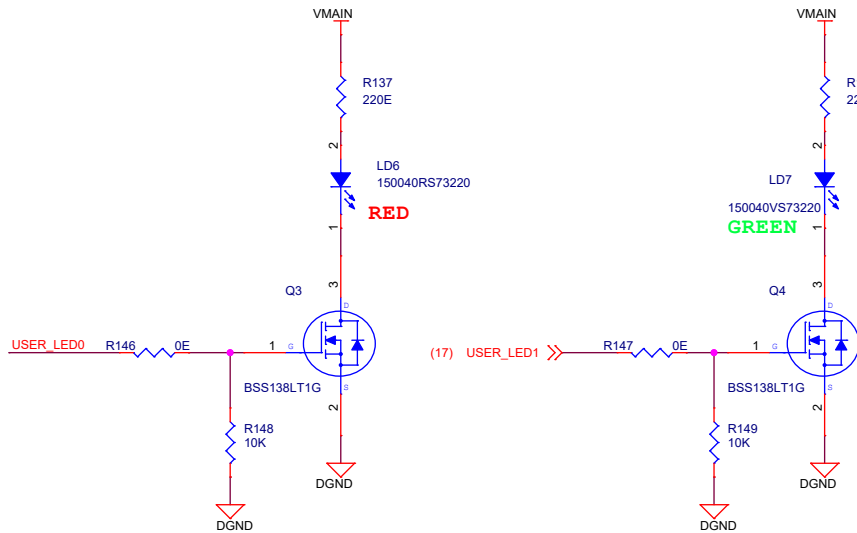
I2C0 MUX/DEMUX



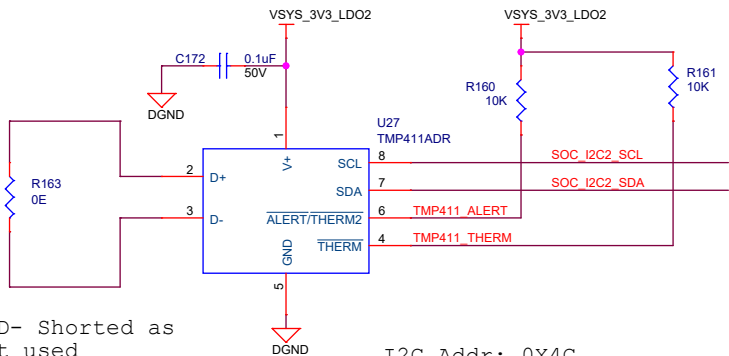
UART2 MUX



USER LEDs



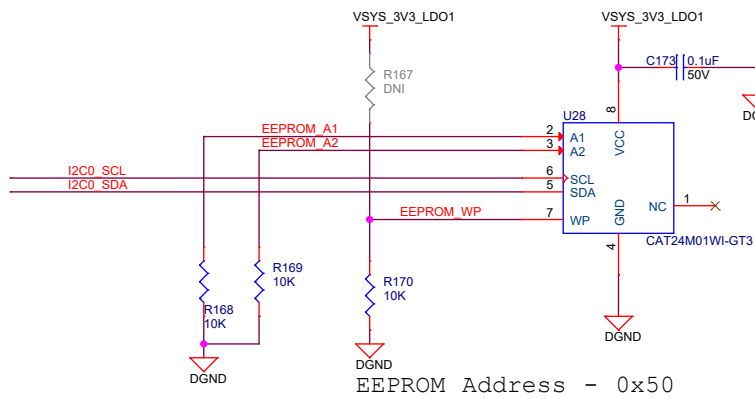
Temperature Sensor



Note: D+ and D- Shorted as TEMPCAL is not used

I2C Addr: 0X4C
PCB Note: Place Close To SOC

Board ID EEPROM



EEPROM Address - 0x50

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Title SOC-IO Interfaces

Size

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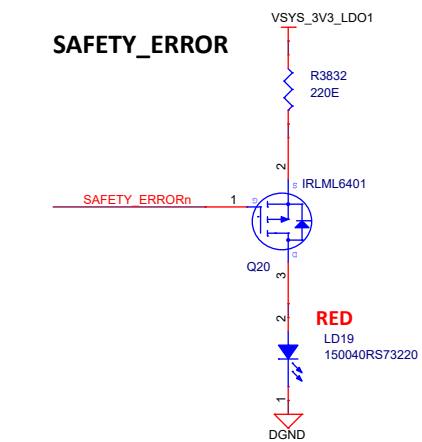
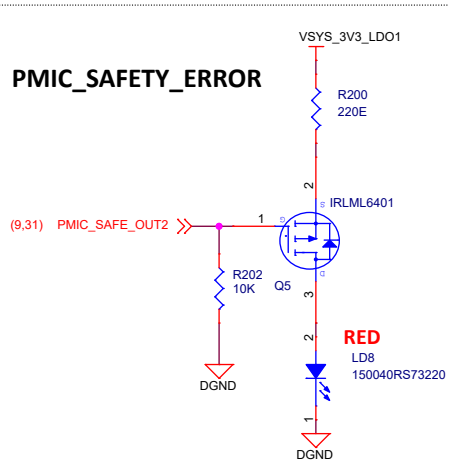
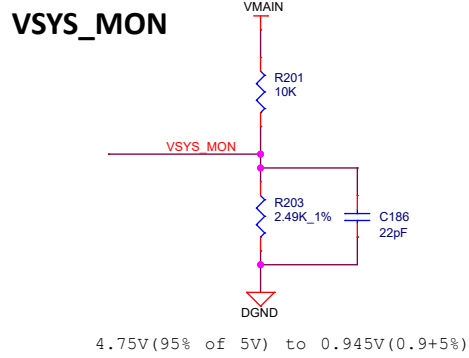
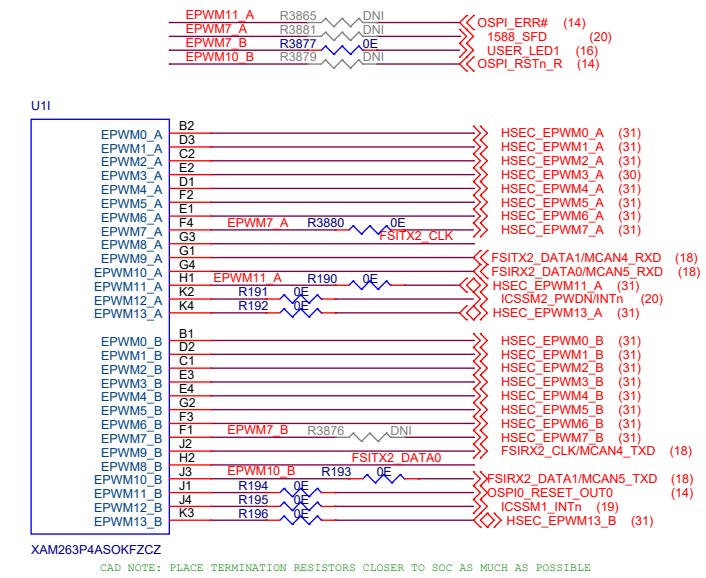
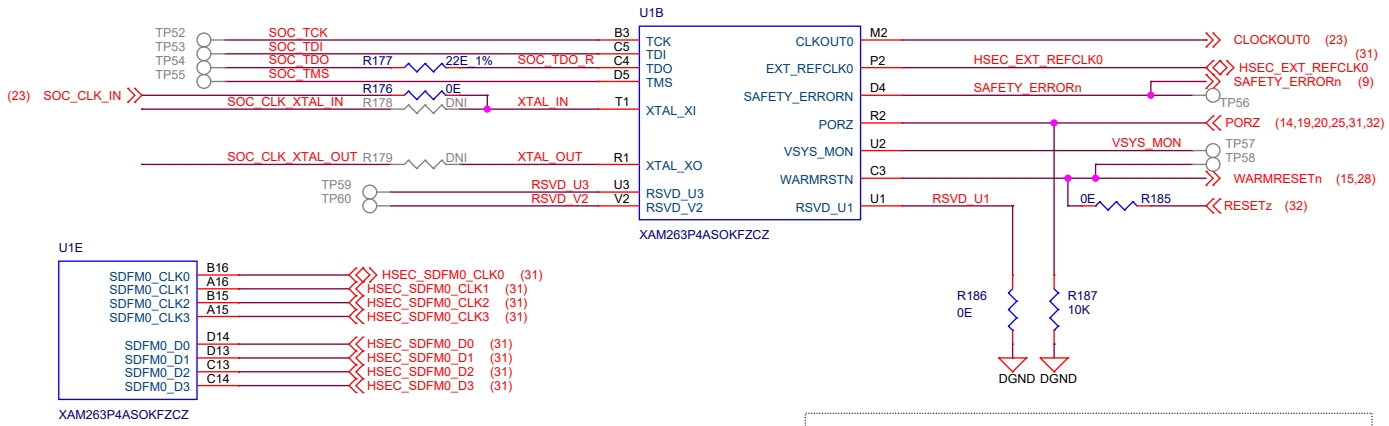
Date:

Thursday, February 13, 2025

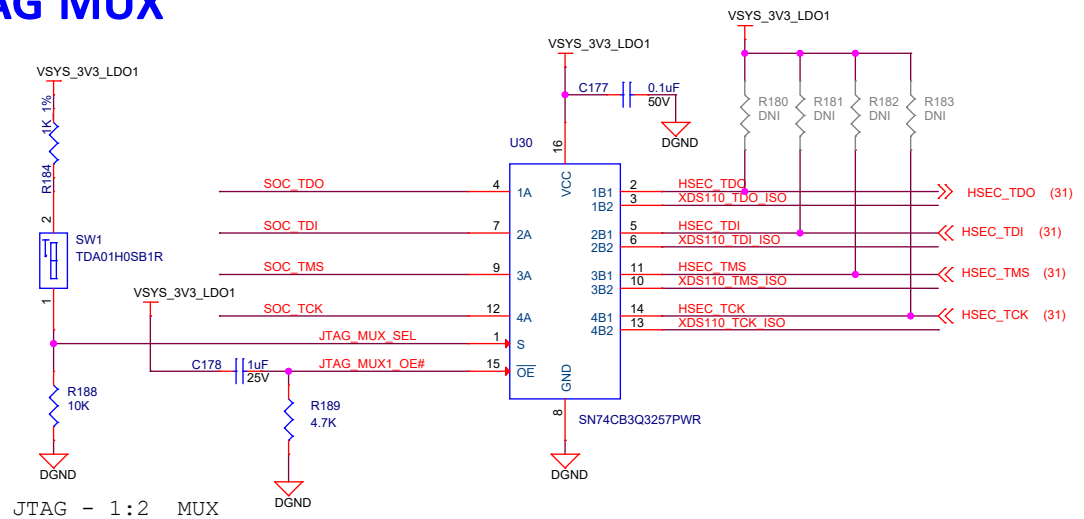
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SOC JTAG, RESET and CLKS

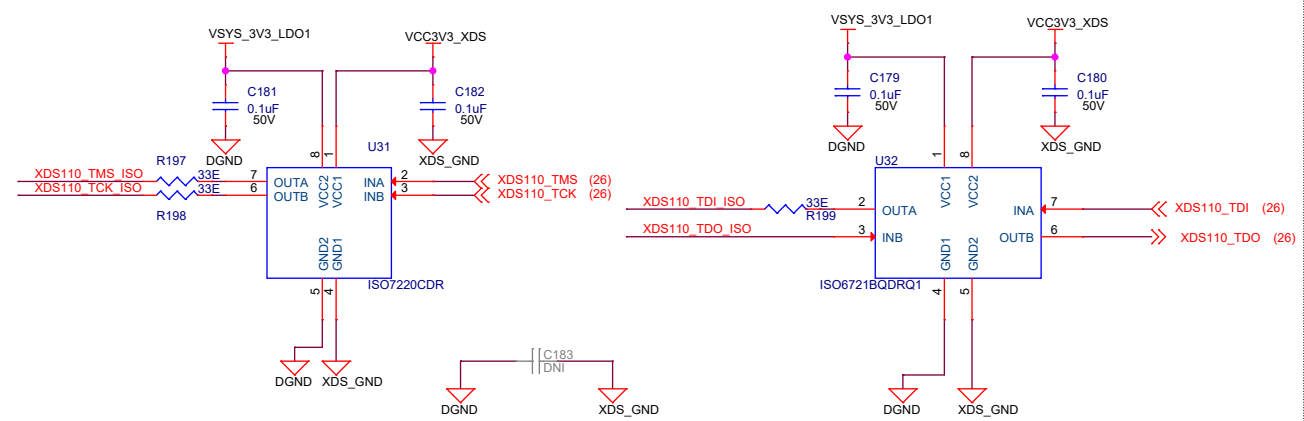


JTAG MUX

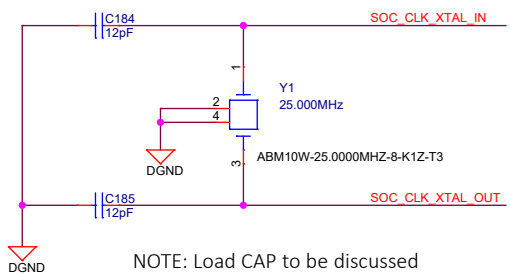


JTAG - 1:2 MUX		DGND
SW1.1	CONDITION	FUNCTION
LOW	HSEC EMU selected	A-->B1 port [EXTERNAL EMU]
HIGH	XDS110 selected	A-->B2 port [ON Board EMU]

ISOLATION FOR XDS110

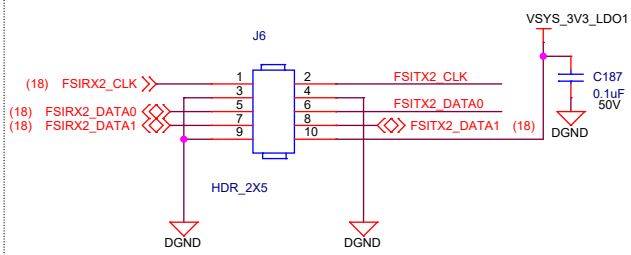


SOC Clock

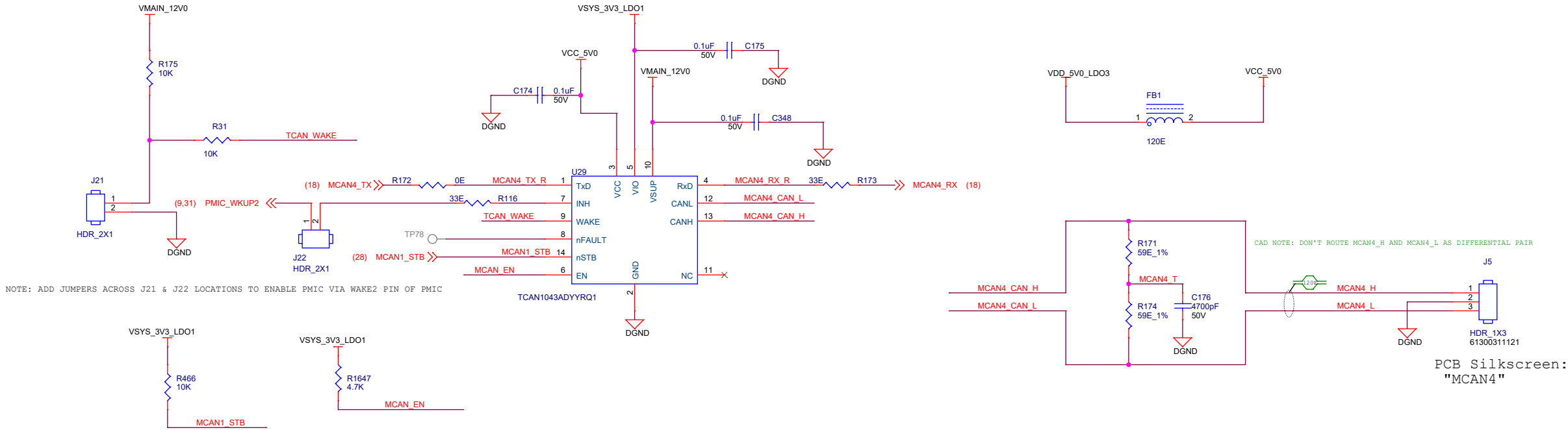


NOTE: Load CAP to be discussed

FSI Header

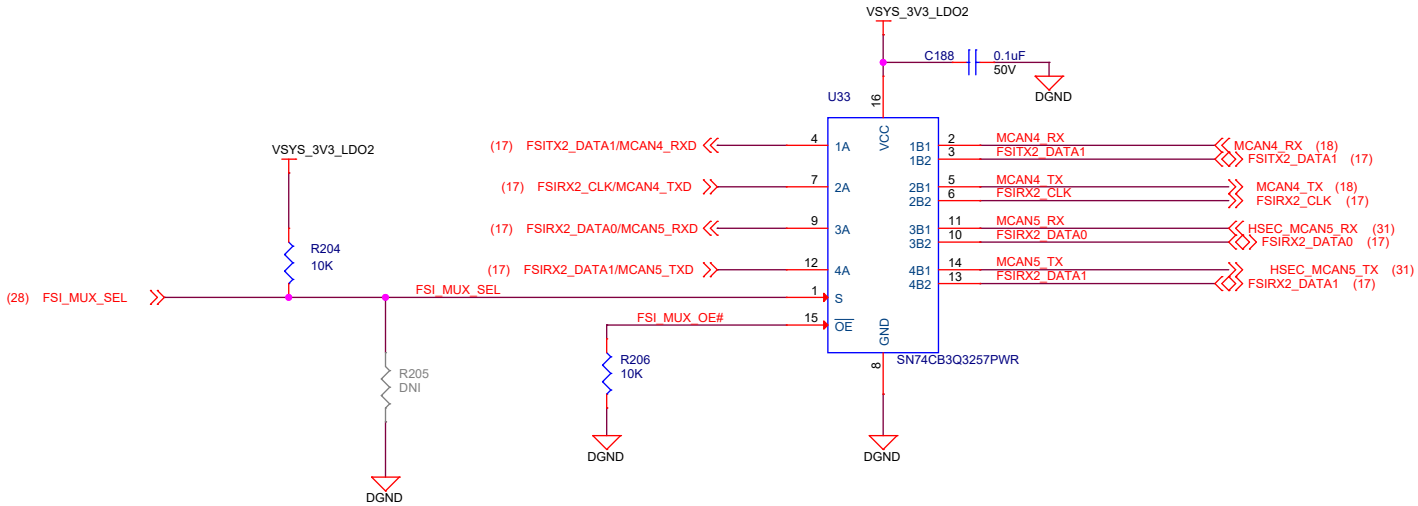


MCAN Interface



PCB Silkscreen:
"MCAN4"

MCAN AND FSI MUX



FSI MUX

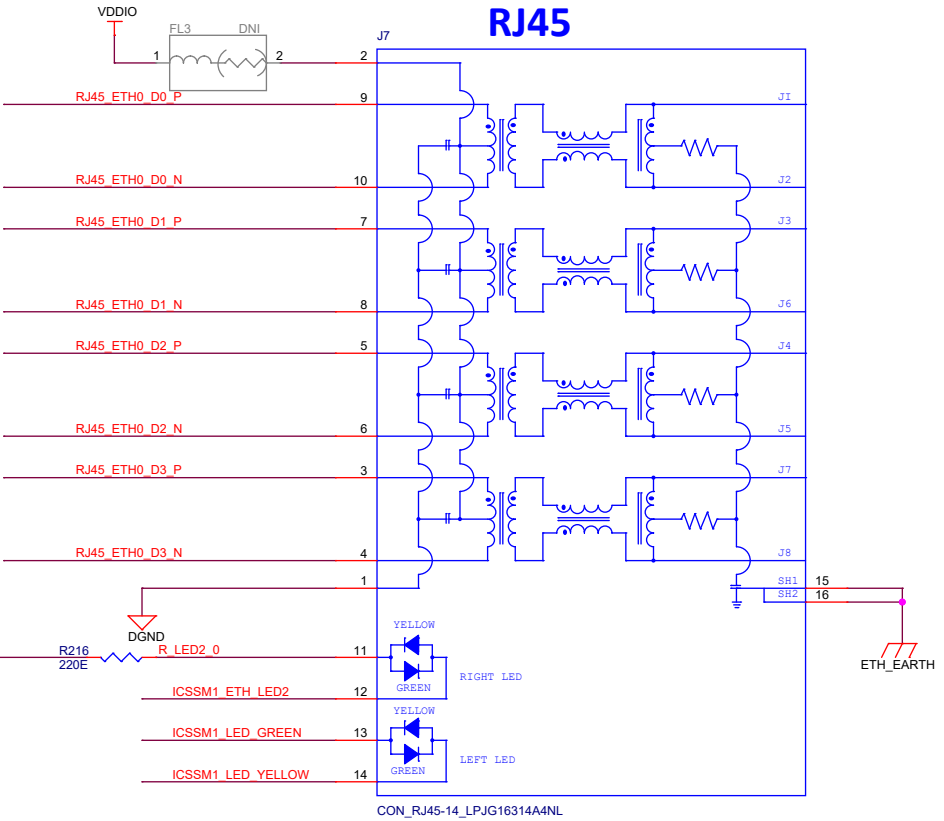
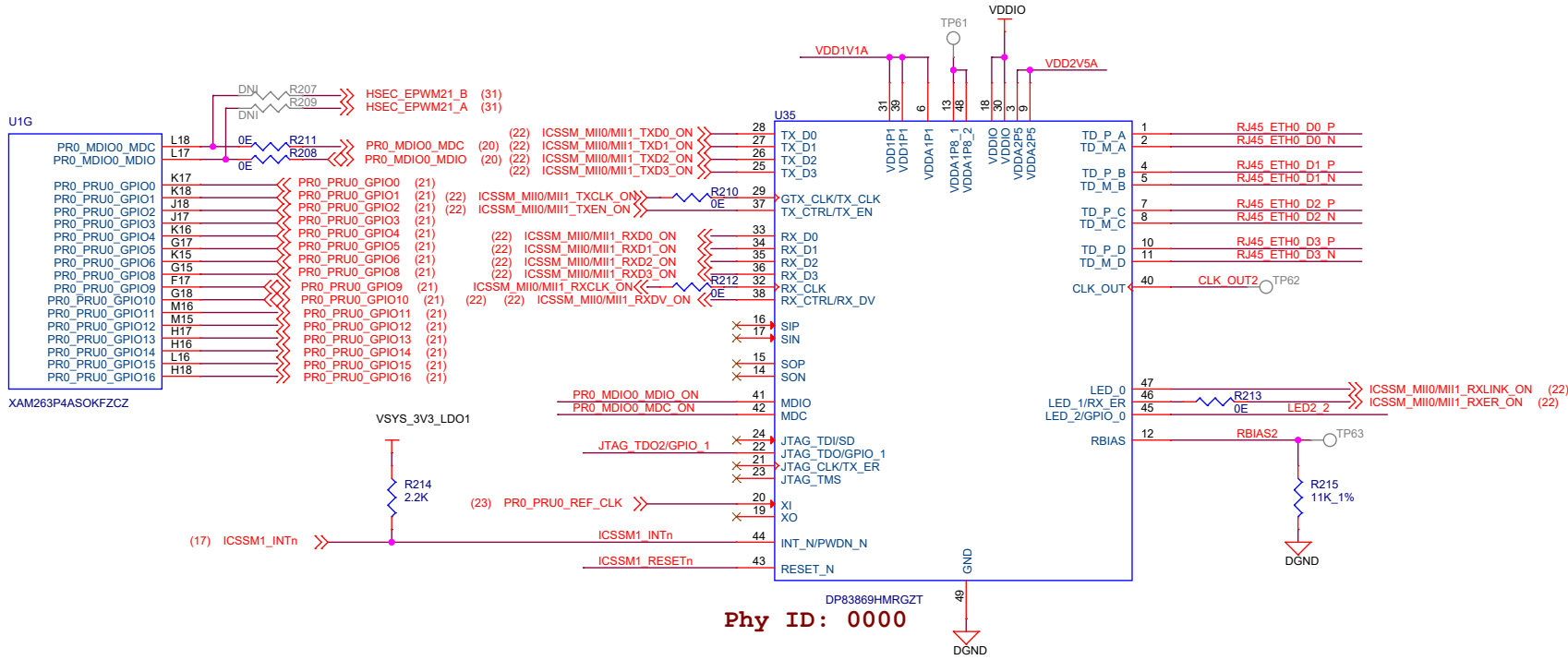
SEL	CONDITION	FUNCTION
LOW	MCAN for CAN & HSEC SELECTED	A-->B1 port
HIGH	FSI SELECTED	A-->B2 port

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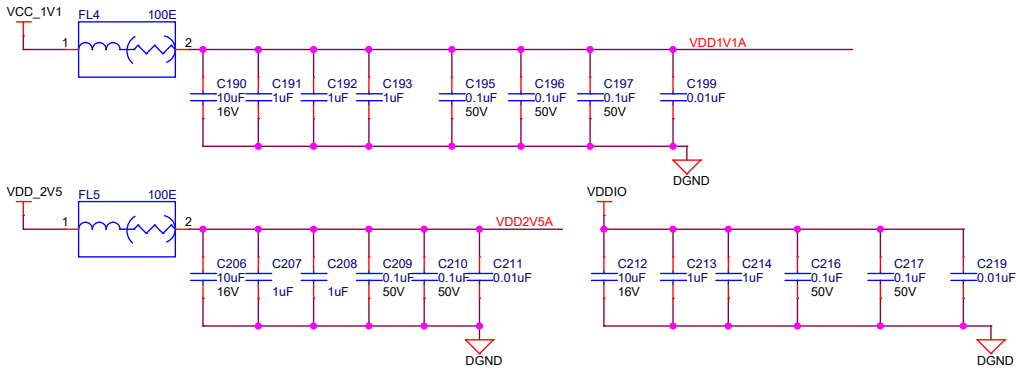


Title MCAN AND FSI MUX		
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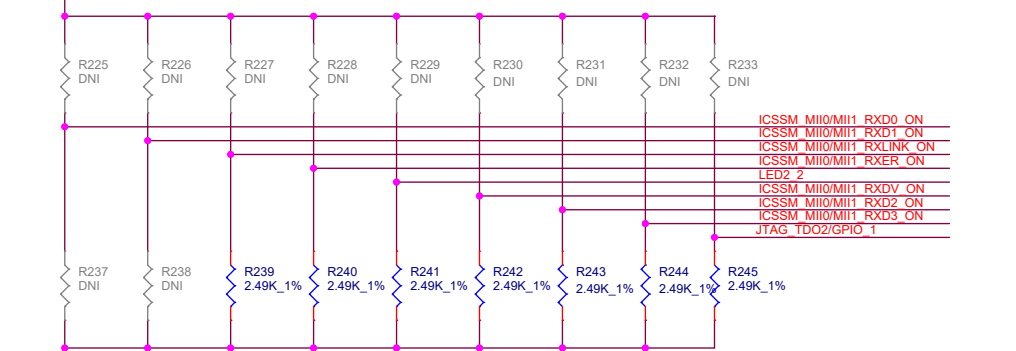
PRU0 ICSS MII0, CPSW RGMII/MII Ethernet



Place Near power pins of 10/100/1000 Ethernet PHY

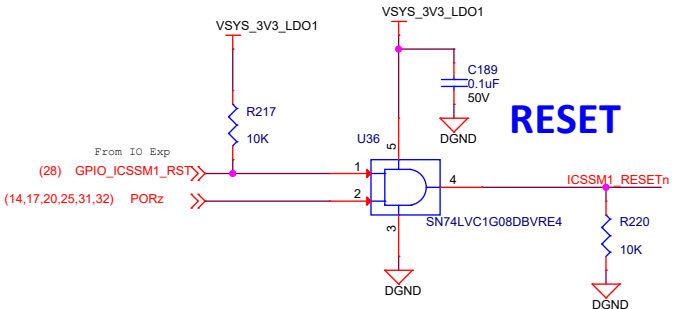


Strapping Resistors

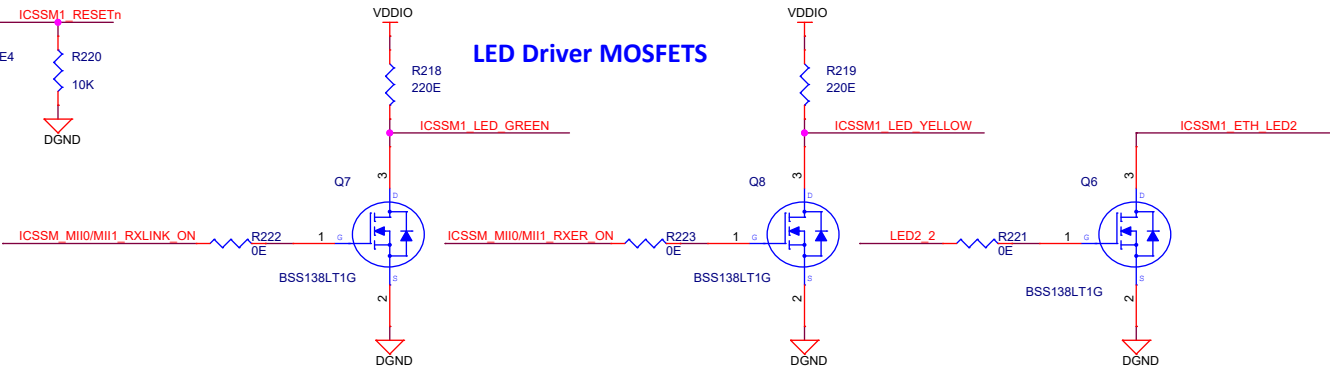


PHY ADDRESS = 00000
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X
RGMII to Copper (1000BaseT/100Base-TX/10Base-Te)

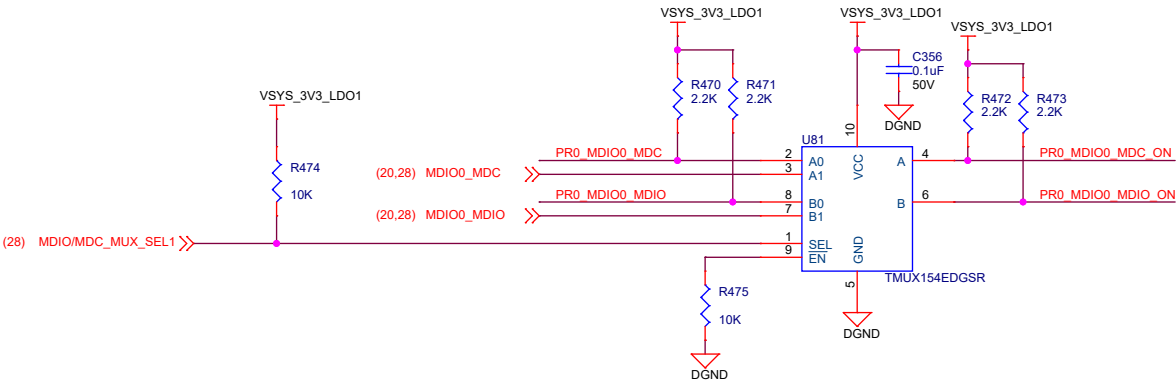
RESET



LED Driver MOSFETS



MDIO/MDC MUX FOR ON-BOARD PHY

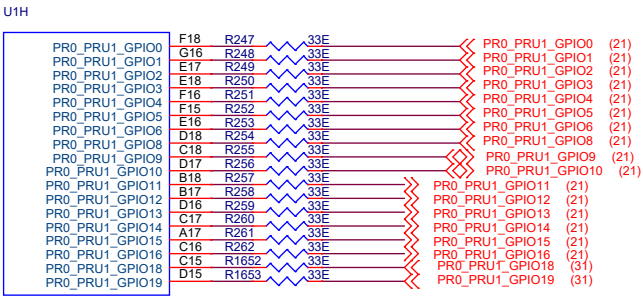


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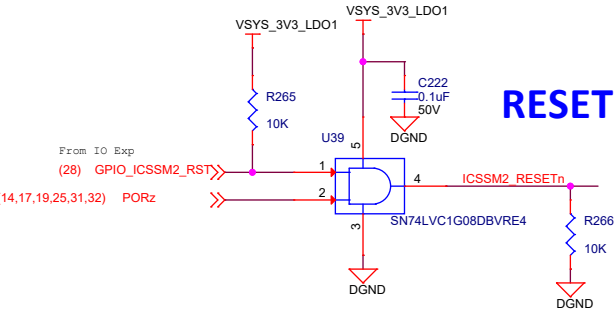
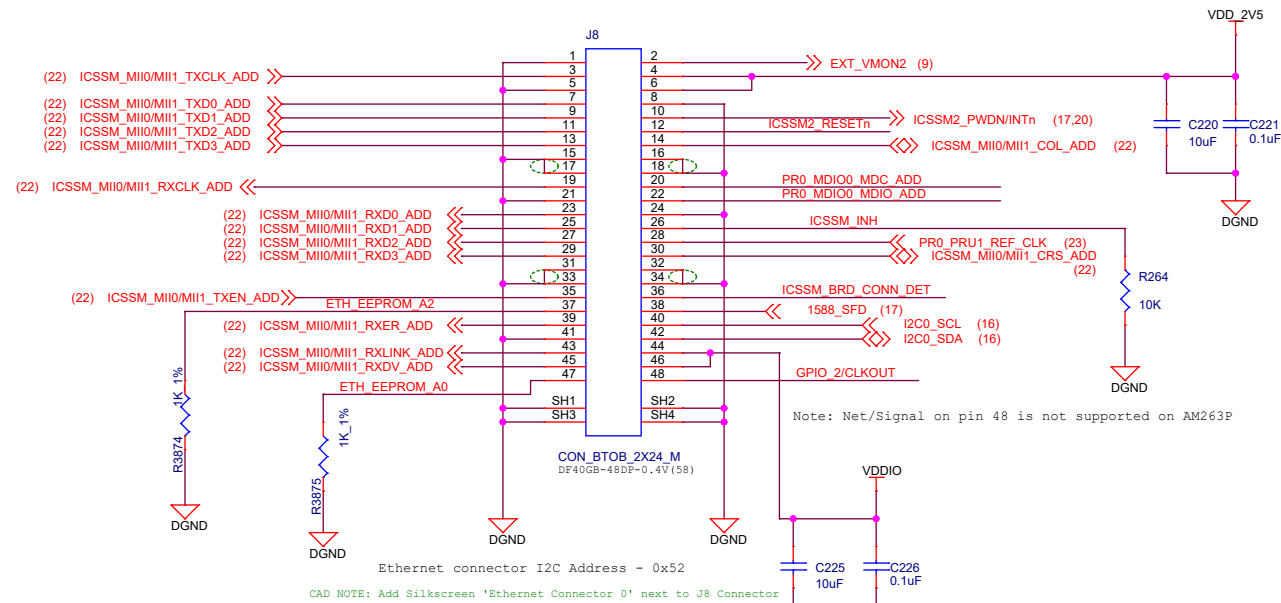
Title			SOC-ICSS DP8386(Indus)	
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PRU1 ICSS MII1 Ethernet

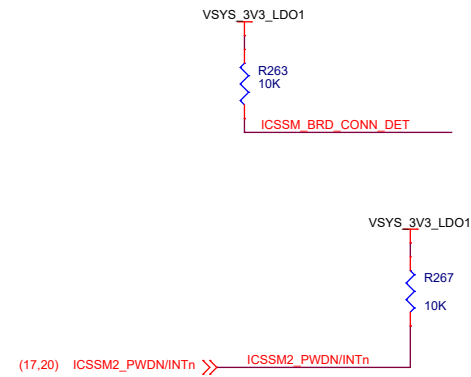
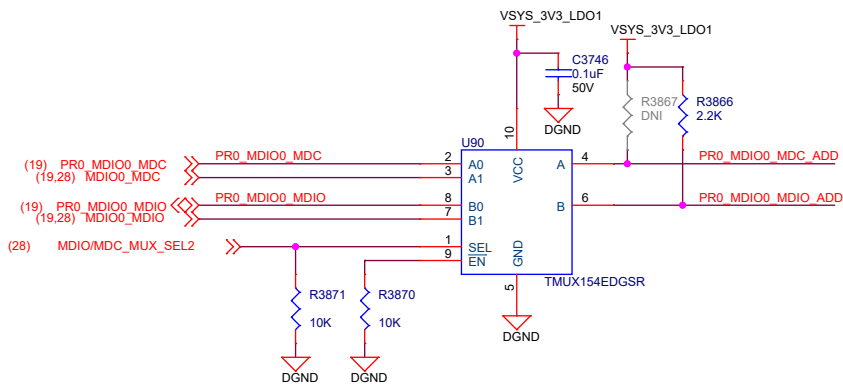


XAM263P4ASOKFZCZ

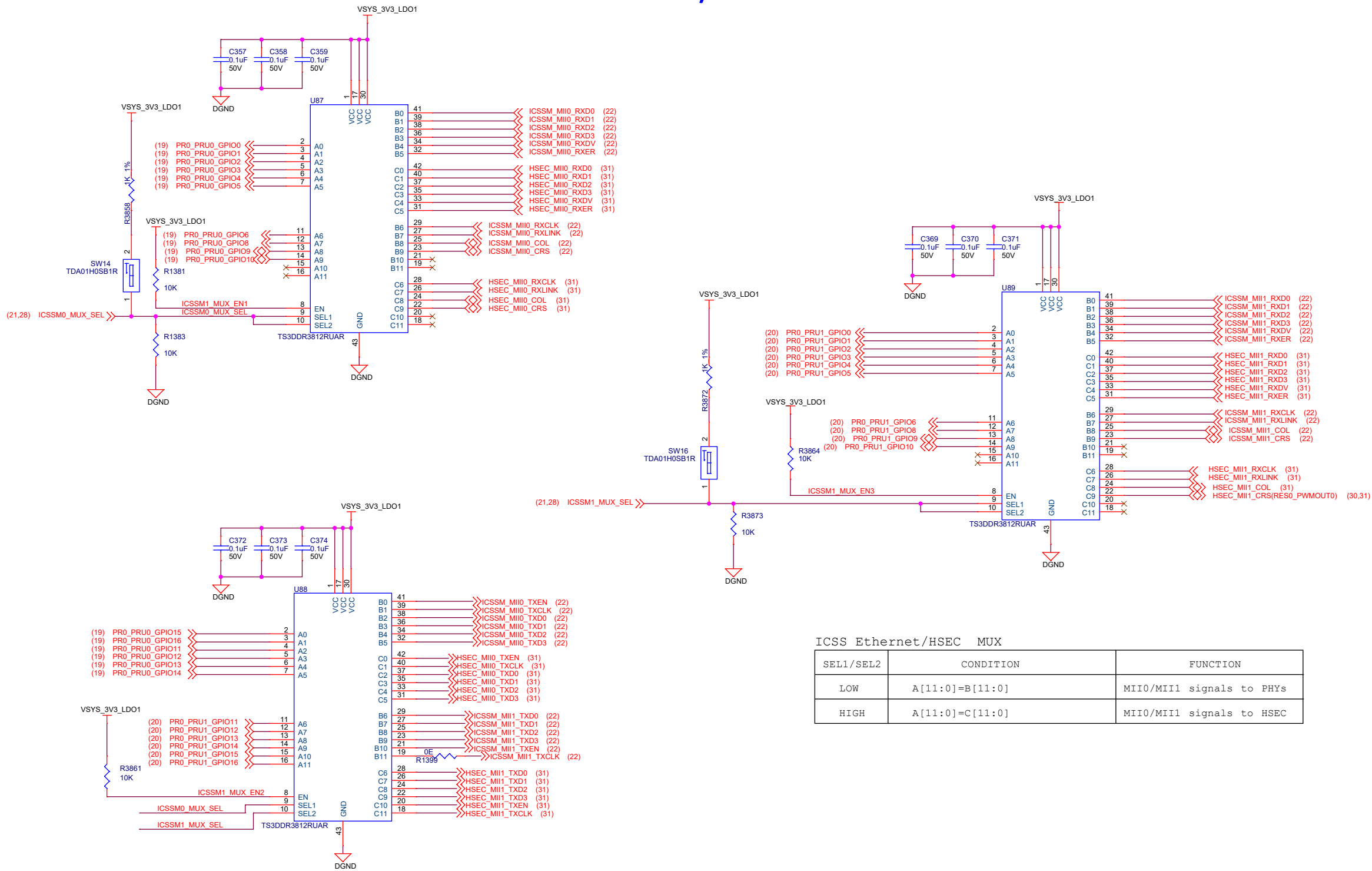
CAD NOTE: Place the resistors close to SoC with minimum stub



MDIO/MDC MUX FOR ADD-ON BOARD CONN



ICSS Ethernet/HSEC MUX



Designed for T1 by Mistral Solutions Pvt Ltd



Title ICSS ETHERNET /HSEC MUXES

Size

Variant Name = PROC159B(001)

Rev

B

Date:

Thursday, February 13, 2025

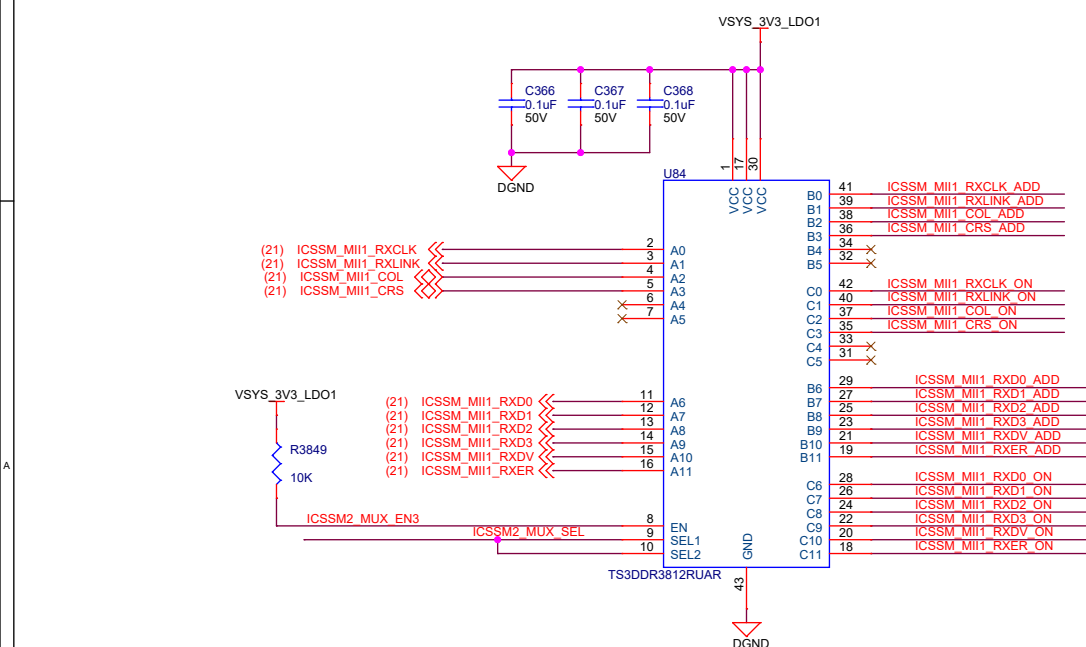
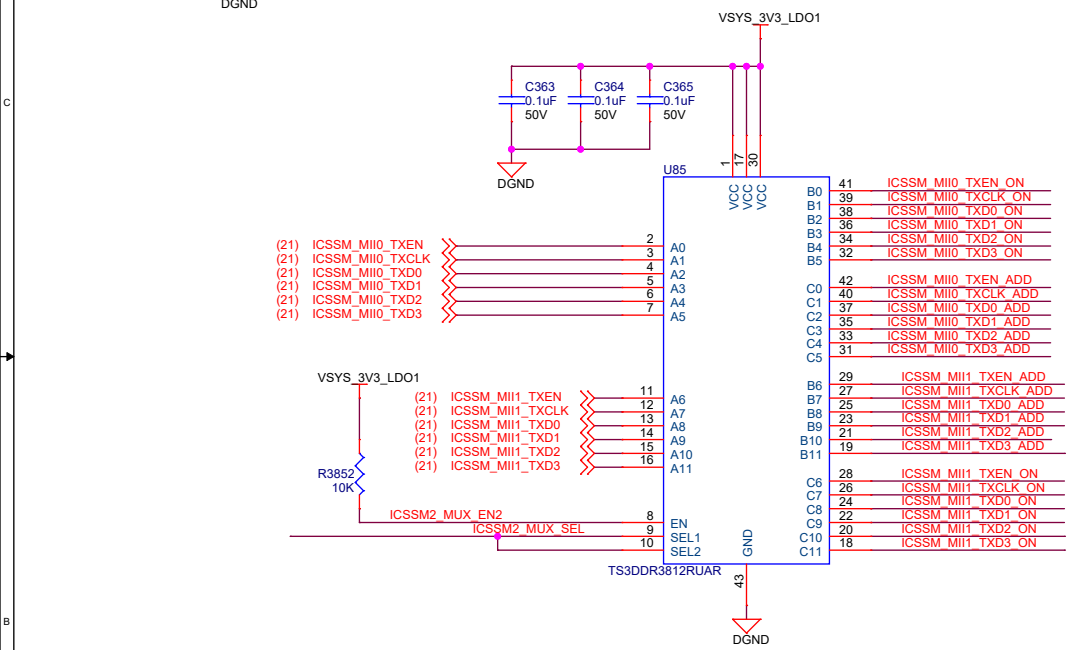
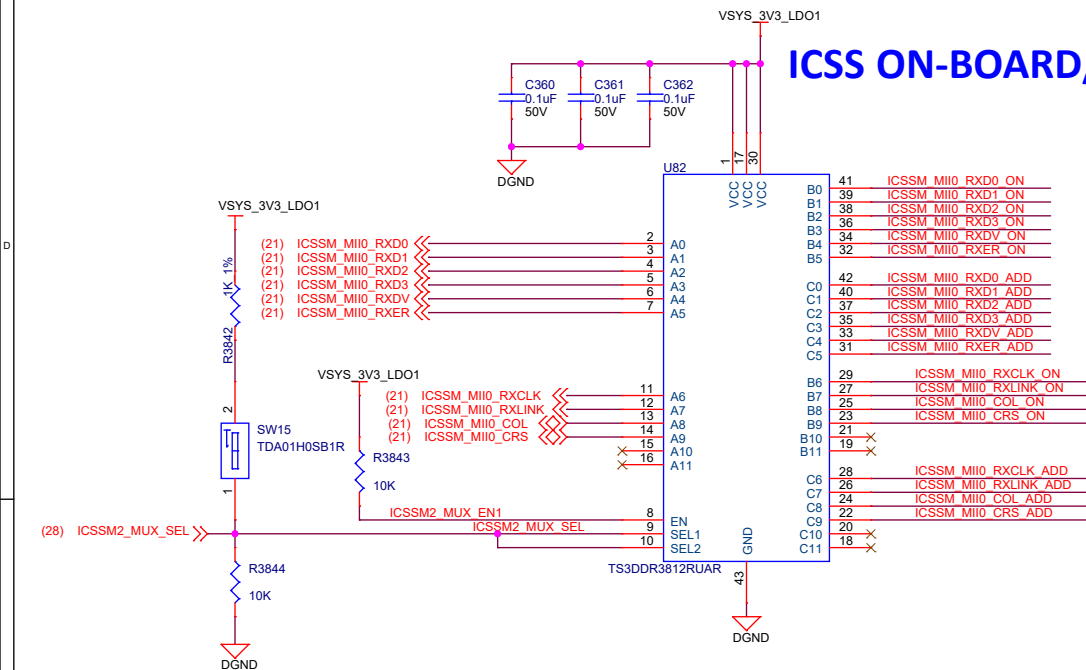
Sheet

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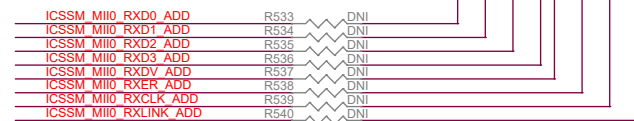
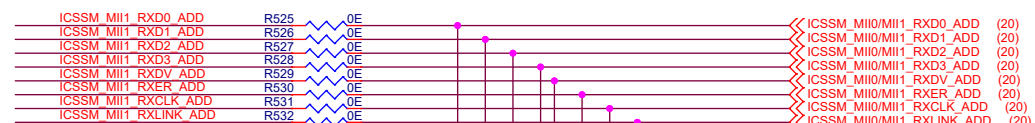
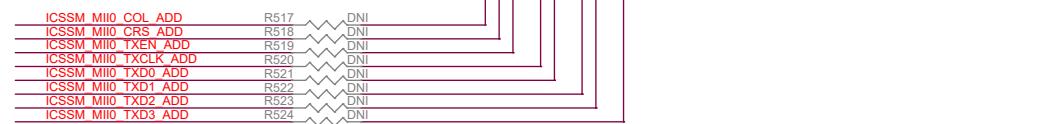
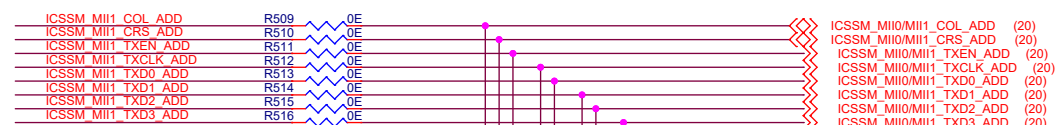
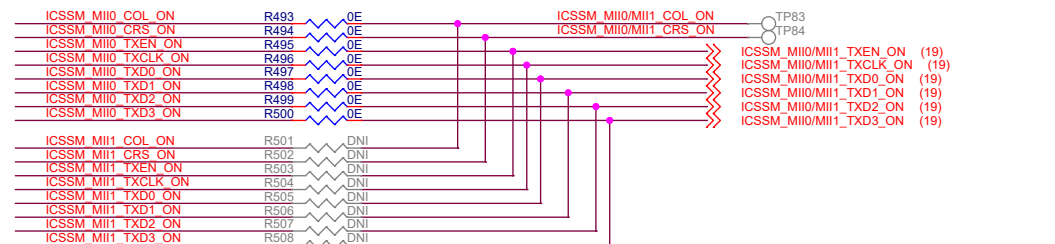
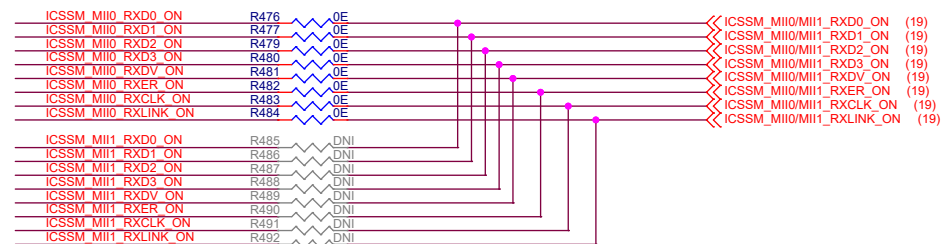
of

33

ICSS ON-BOARD/ADD-ON PHY MUX



ICSS MII0/MI1 - RESISTOR MUX



CAD NOTE: Place the resistors with minimum stub

ICSS MII0/MII1 - RESISTOR MUX

MODE	FUNCTION
Populate R476 to R484, R493 to R500, R509 to R516, R525 to R532 resistors (Default)	MII0 -> On-board PHY MII1 -> Add-on Board connector
Populate R485 to 492, R501 to R508, R517 to R524, R533 to R540 resistors	MII0 -> Add-on Board connector MII1 -> On-board PHY

ICSS ON-BOARD/ADD-ON PHY MUX

SEL1/SEL2	CONDITION	FUNCTION
LOW	A[11:0]=B[11:0]	MII0 signals to ON-BOARD PHY MII1 signals to ADD-ON BOARD
HIGH	A[11:0]=C[11:0]	MII0 signals to ADD-ON BOARD MII1 signals to ON-BOARD PHY

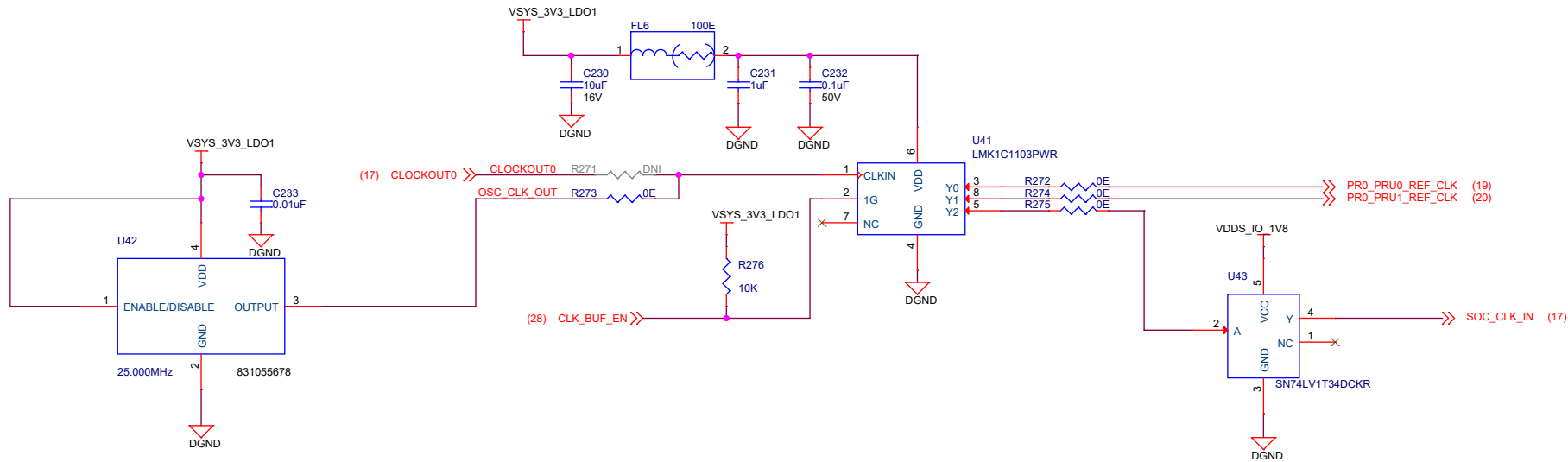
Designed for TI by Mistral Solutions Pvt Ltd



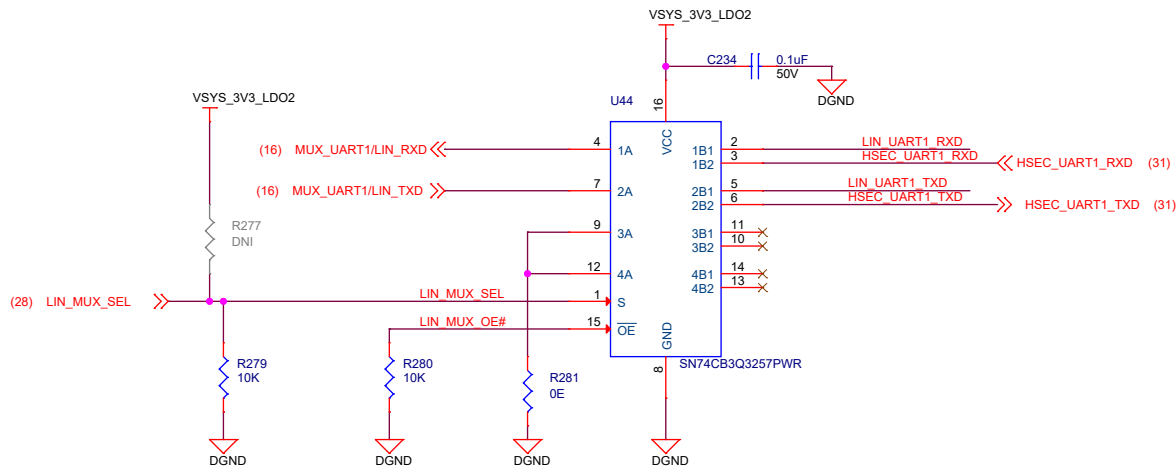
Title	ICSS ON-BOARD/ADD-ON PHY & MII0/III1 MUXES
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Size	Variant Name = PROC159B(001)	Rev
C		B
Date:	Thursday, February 13, 2025	Sheet 22 of 33

CLOCKS

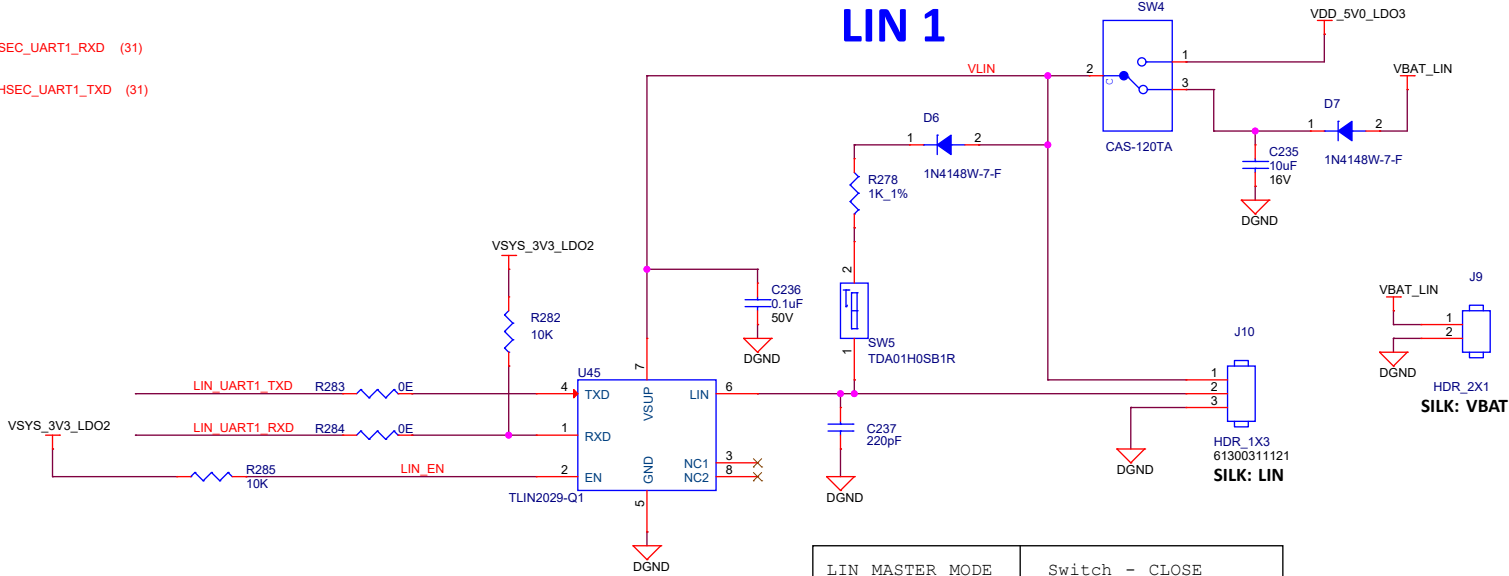


LIN MUX/DEMUX



I2C0 - 1:2 MUX		
SEL	CONDITION	FUNCTION
LOW	LIN SELECTED	A-->B1 port
HIGH	HSEC UART selected	A-->B2 port

LIN 1



LIN MASTER MODE	Switch - CLOSE
LIN SLAVE MODE	Switch - OPEN

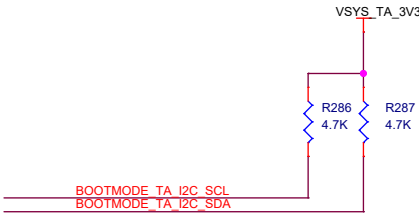
Designed for T1 by Mistral Solutions Pvt Ltd



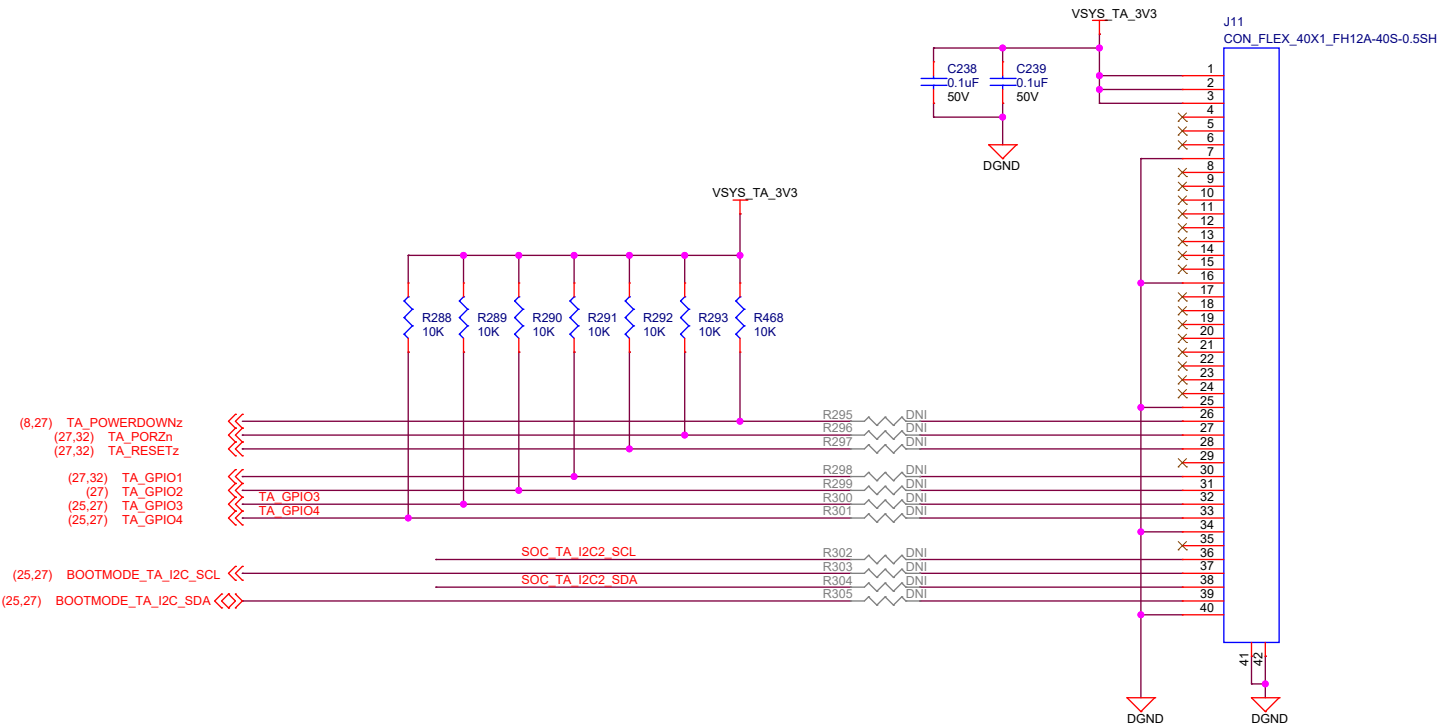
Title CLOCKS AND LIN1		
Size	Variant Name = PROC159B(001)	Rev
C		B
Date:	Thursday, February 13, 2025	Sheet 23 of 33

TEST AUTOMATION HEADER

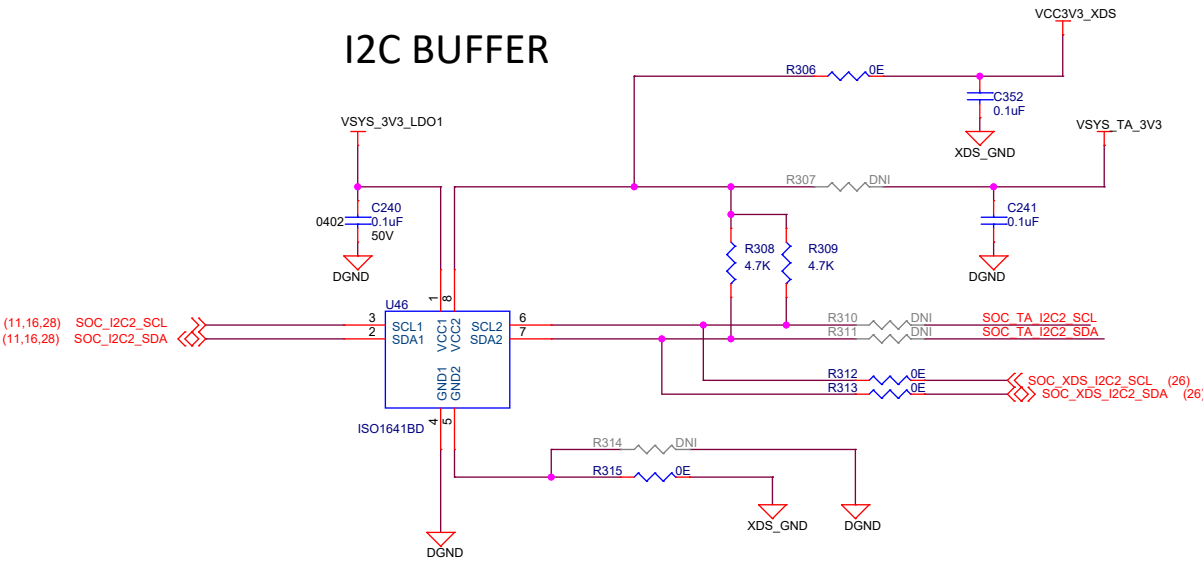
I2C Pull Ups



AUTOMATION INTERFACE
Cable : Parlex-050R40-76B, .5mm 3"



I2C BUFFER



TA Configuration
Mount : R307,R310,R311,R314
Demount : R306,R312,R313,R315

TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_GPIO1	Interrupt to SOC	OUTPUT	External Pullup
TA_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TA_GPIO4	Used Reset Bootmode IO Exp	OUTPUT	External Pullup

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Title TEST AUTOMATION HEADER

Variant Name = PROC159B(001)

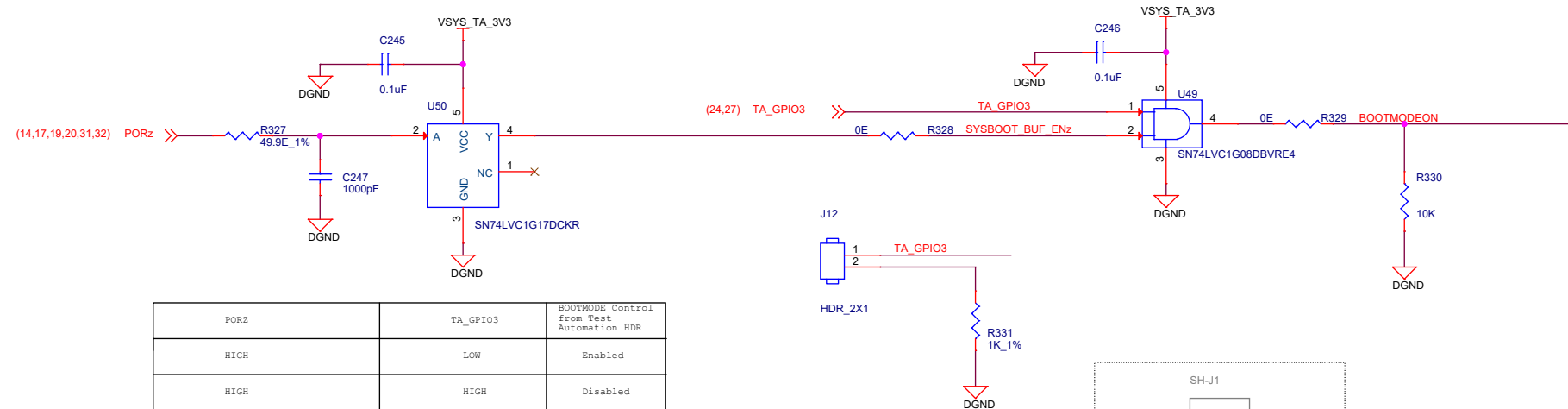
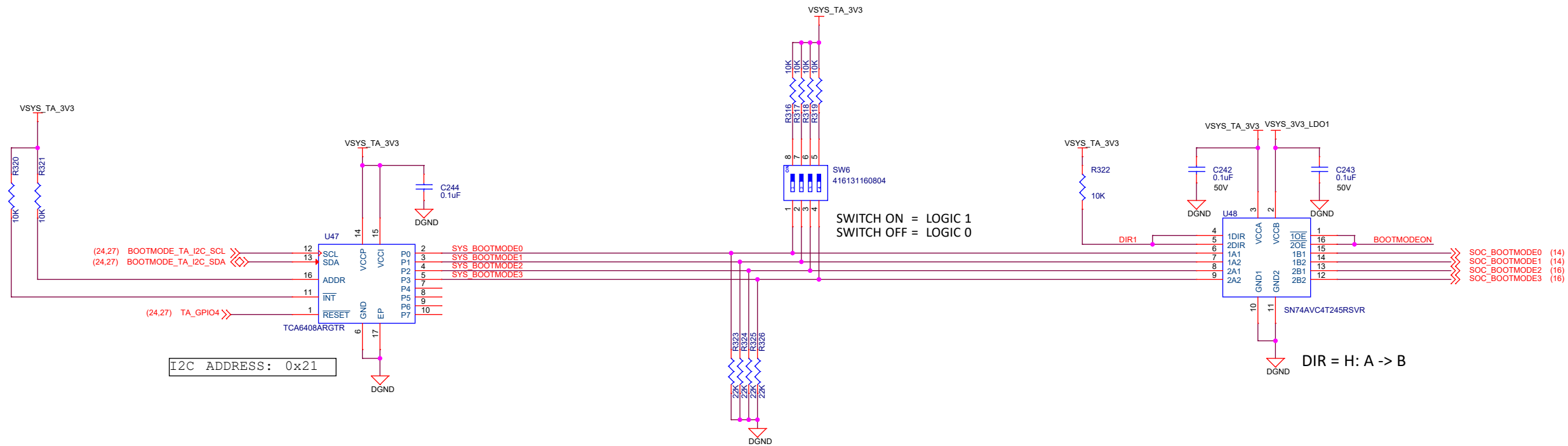
Date: Thursday, February 13, 2025

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Rev

B

BOOTMODE BUFFER AND SWITCH



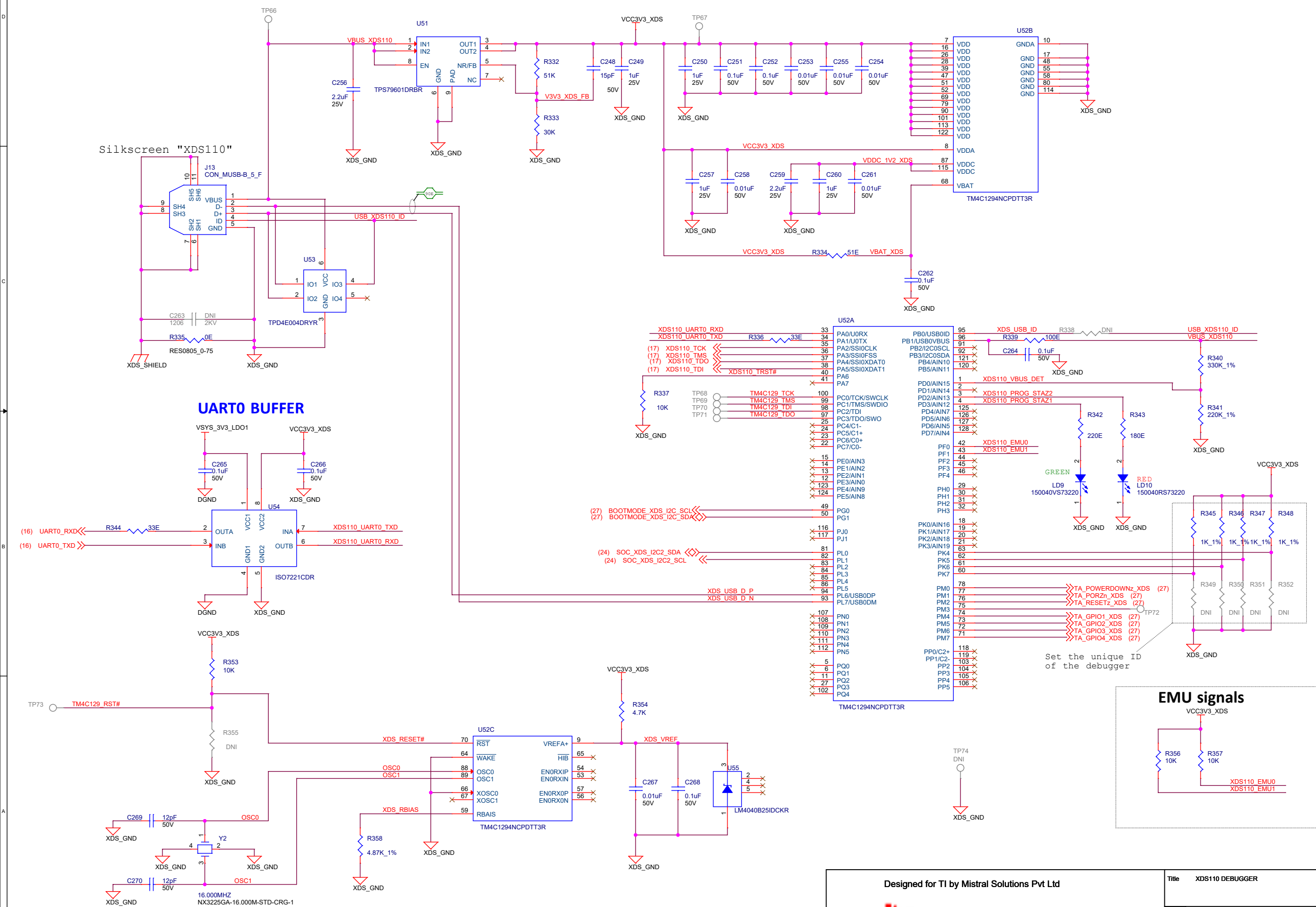
POR2	TA_GPI03	BOOTMODE Control from Test Automation HDR
HIGH	LOW	Enabled
HIGH	HIGH	Disabled

SH-J1

DNI

SH-J1 Shall be mounted to
enable the bootmode buffer

XDS110 DEBUGGER

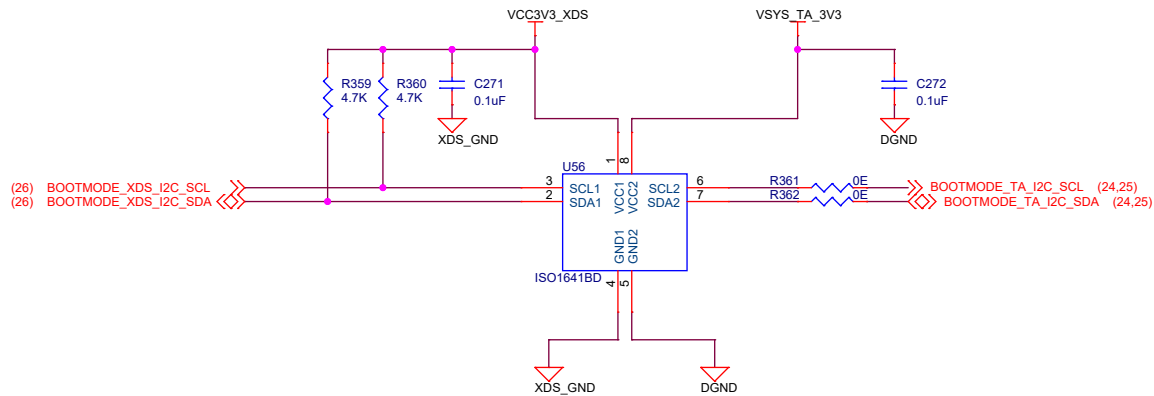


Designed for TI by Mistral Solutions Pvt Ltd

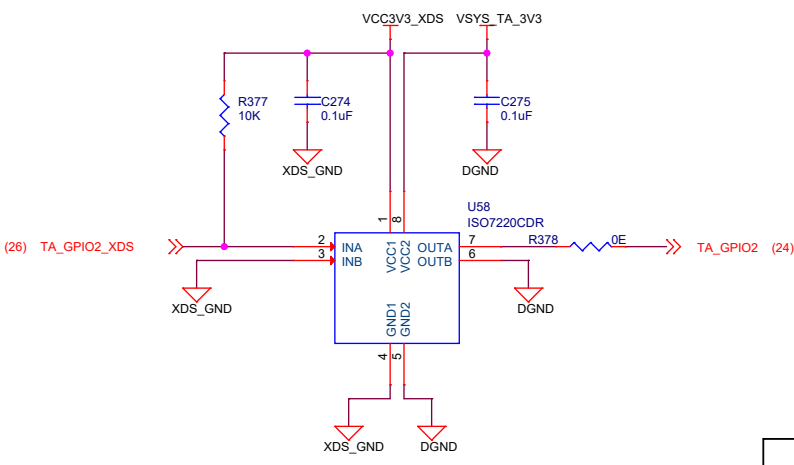
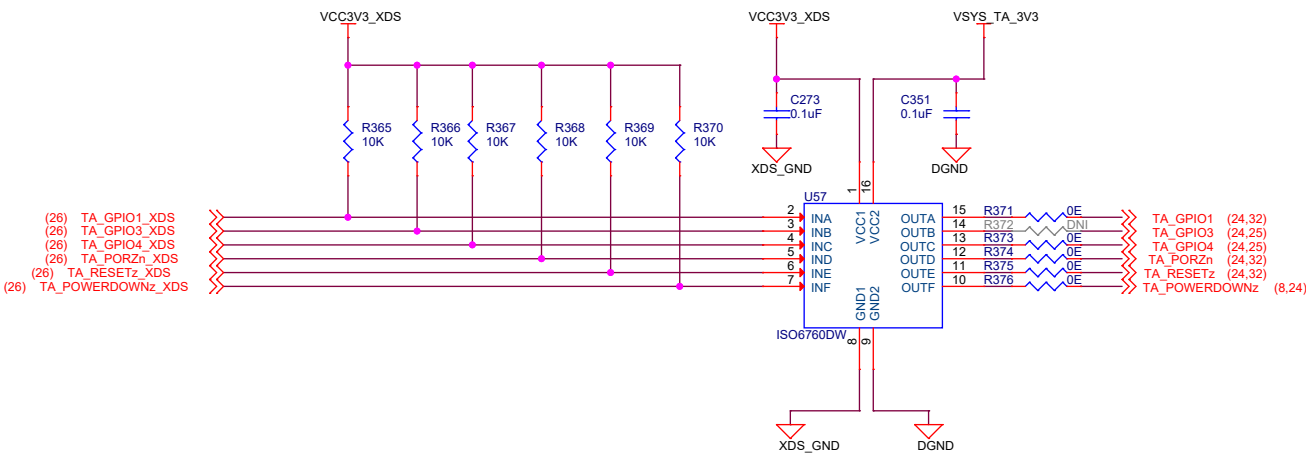


Title XDS110 DEBUGGER				
Size				Rev
C	Variant Name = PROC159B(001)			B
Date:	Thursday, February 13, 2025	Sheet	26 of	33

BOOTMODE_I2C_TA BUFFER



ISOLATION BUFFERS FOR TA SIGNALS

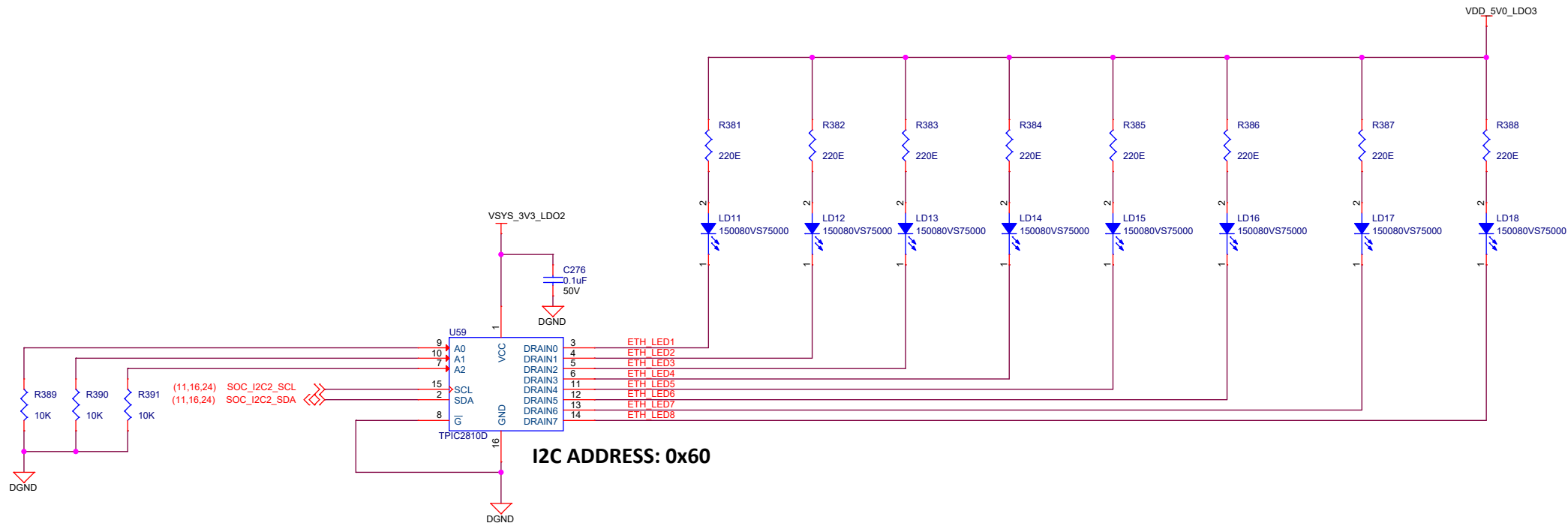


Designed for T1 by Mistral Solutions Pvt Ltd

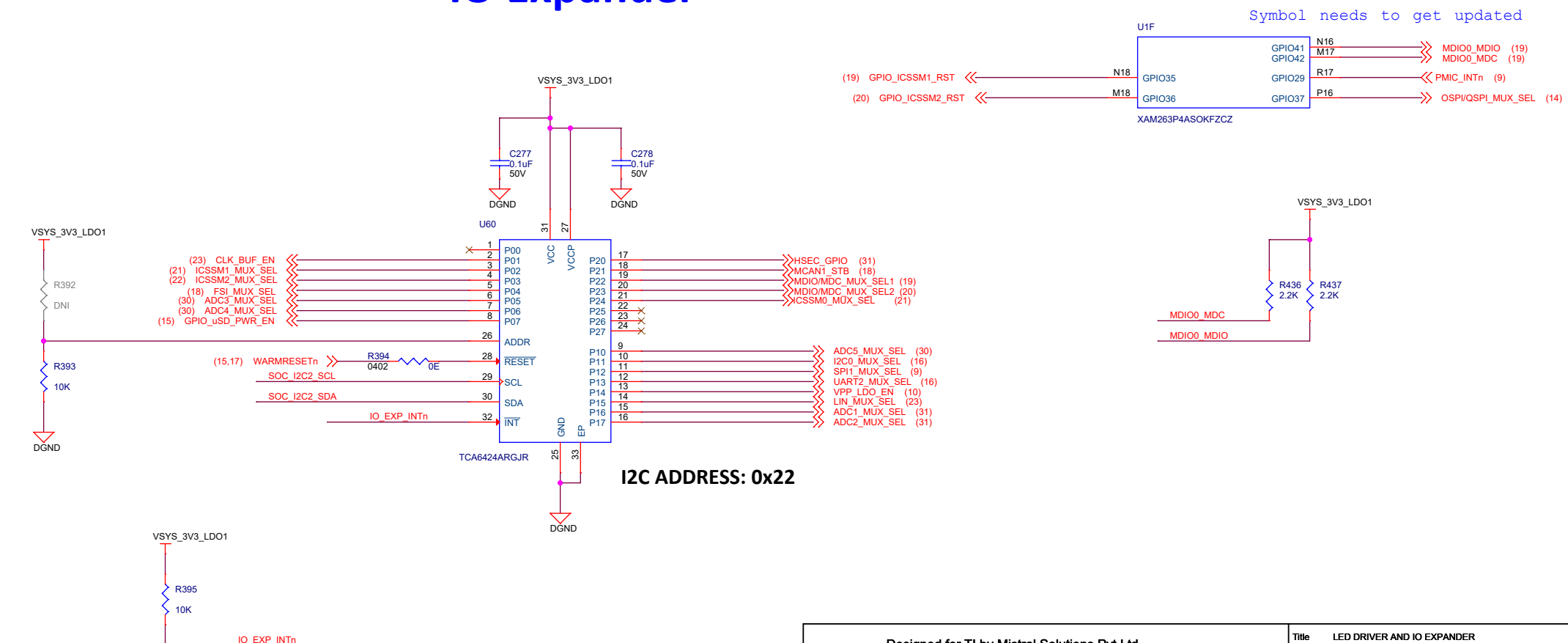


Title AUTOMATION SIGNALS BUFFER		
Size	Variant Name = PROC159B(001)	Rev
C		B
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LED Driver



IO Expander



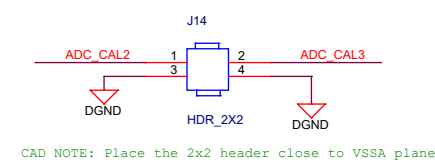
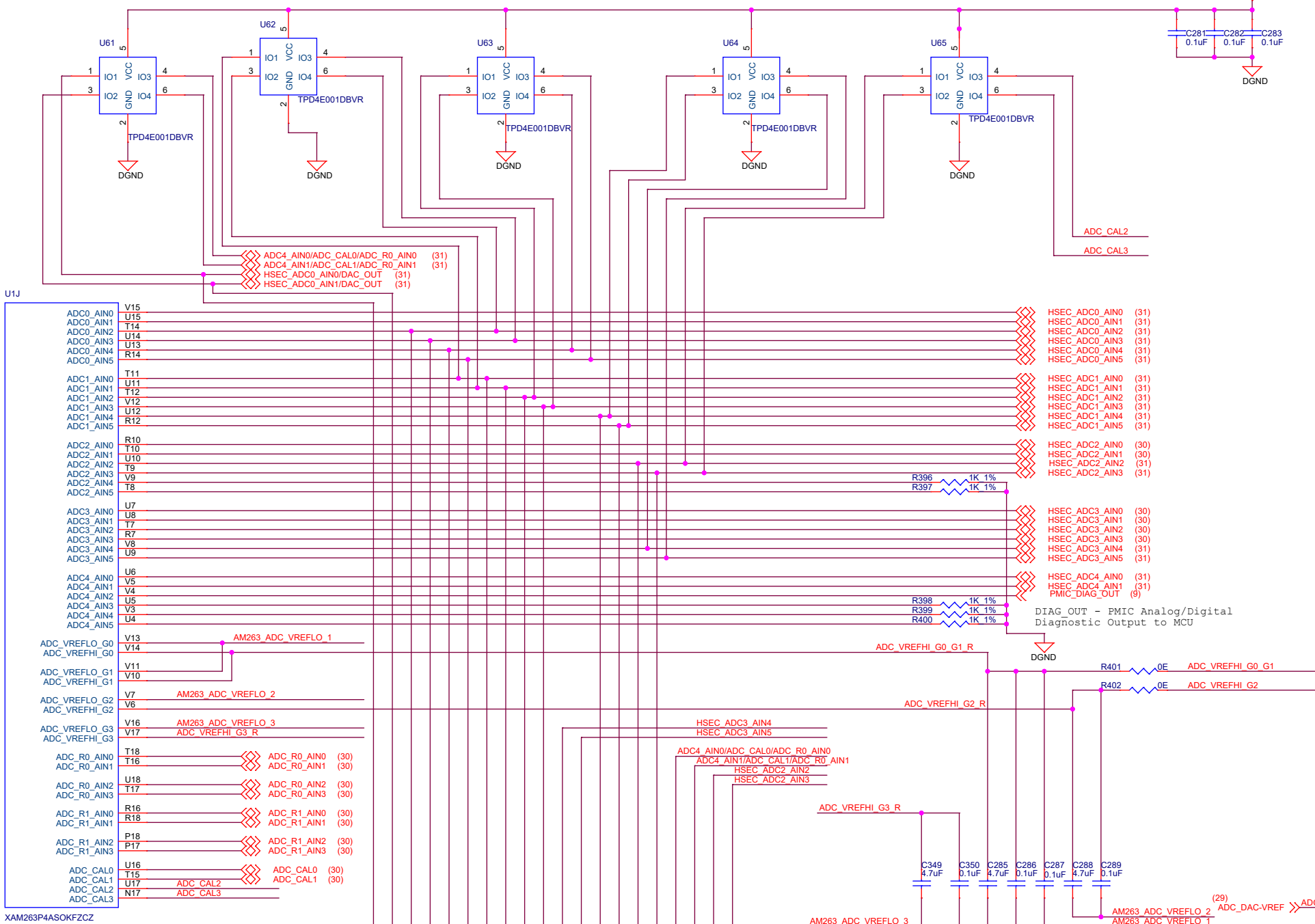
Designed for T1 by Mistral Solutions Pvt Ltd



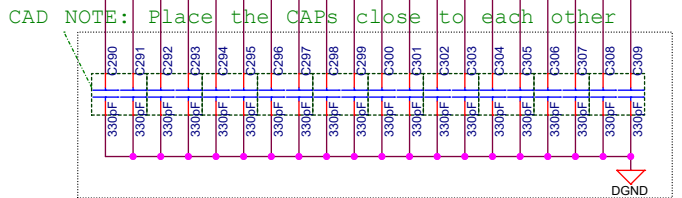
Title LED DRIVER AND IO EXPANDER		
Size	Variant Name = PROC159B(001)	Rev
C		B
Date:	Thursday, February 13, 2025	Sheet 28 of 33

SOC- ADC & DAC Interface

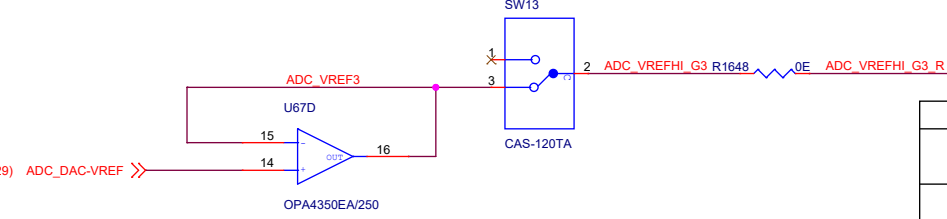
CAD NOTE: Place the ESDs close to connector



CAD NOTE: Place the 2x2 header close to VSSA plane



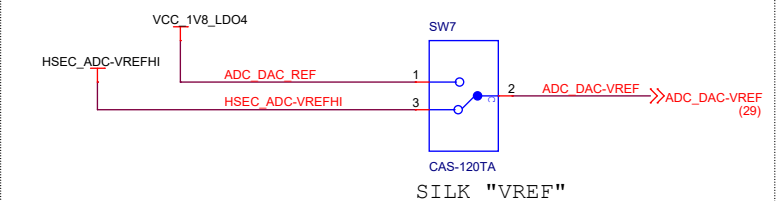
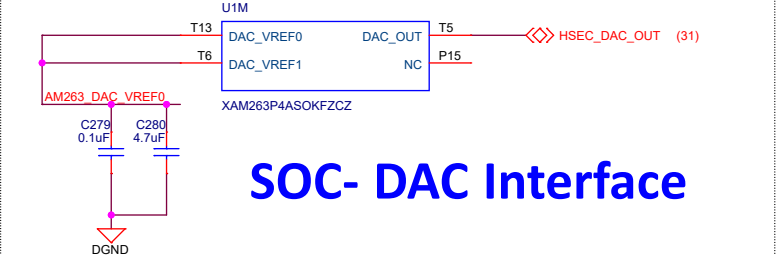
CAD NOTE: Place the CAPs close to the connector



ADC REF VOLTAGE SELECTION

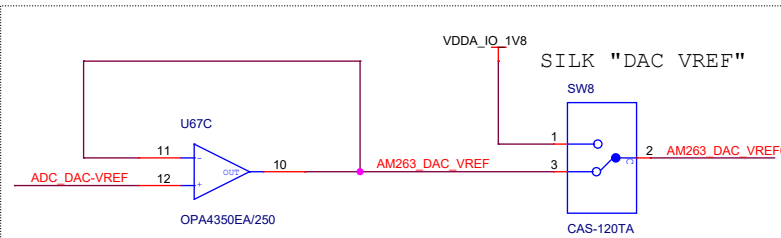
SW POSITION	SUPPLY SELECTION
PIN 1-2	OPEN - Allows AM263P on-die LDO reference (routed on-die)
PIN 2-3	selects output of VREF switch

SOC- DAC Interface



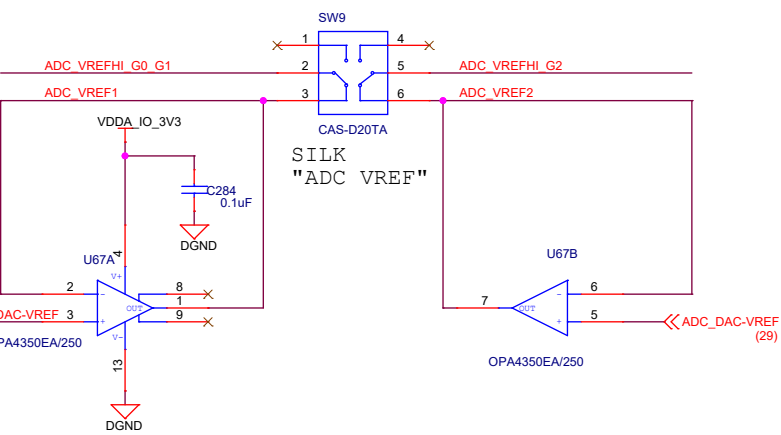
REF VOLTAGE SELECTION

SW POSITION	SUPPLY SELECTION
PIN 1-2	ON BOARD REF IS SELECTED
PIN 2-3	HSEC SUPPLY IS SELECTED



DAC REF VOLTAGE SELECTION

SW POSITION	SUPPLY SELECTION
PIN 1-2	Allows AM263P on-die LDO reference (Routed n PCB)
PIN 2-3	selects output of VREF switch



ADC REF VOLTAGE SELECTION

SW POSITION	SUPPLY SELECTION
PIN 1-2	OPEN - Allows AM263P on-die LDO reference (routed on-die)
PIN 2-3	selects output of VREF switch
PIN 4-5	OPEN - Allows AM263P on-die LDO reference (routed on-die)
PIN 5-6	selects output of VREF switch

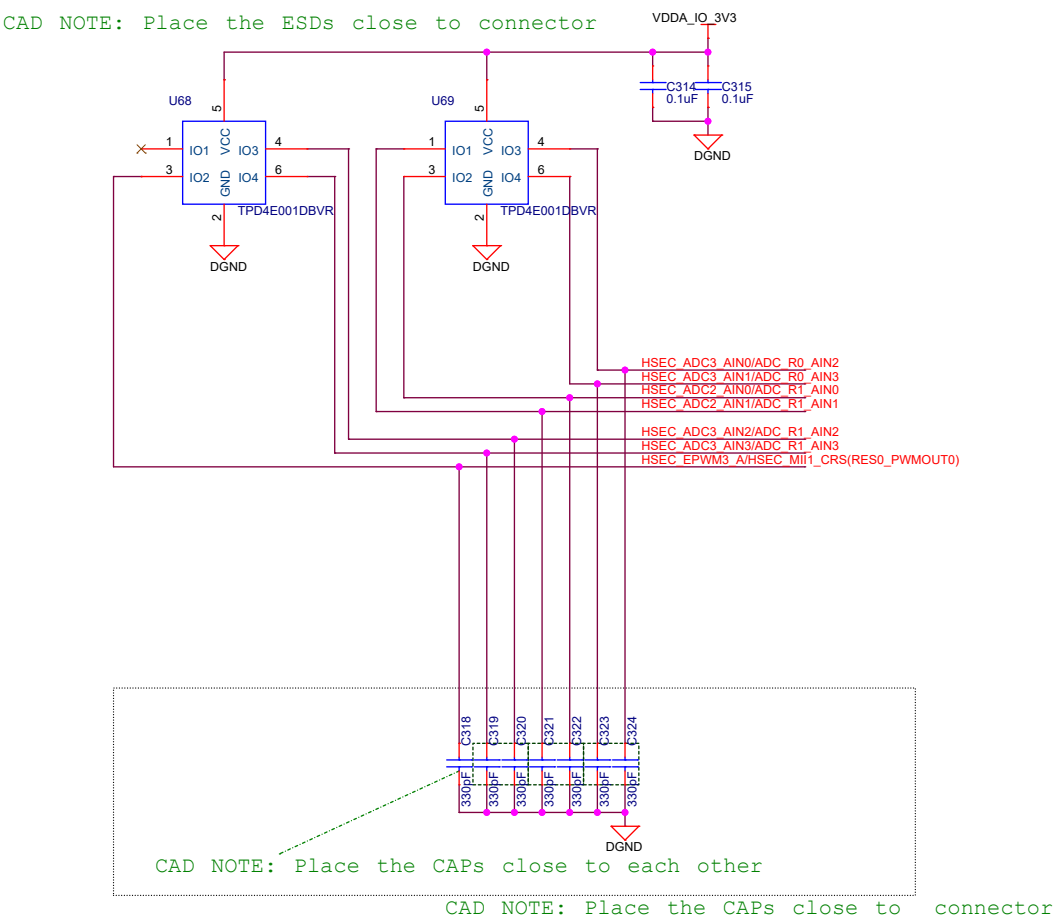
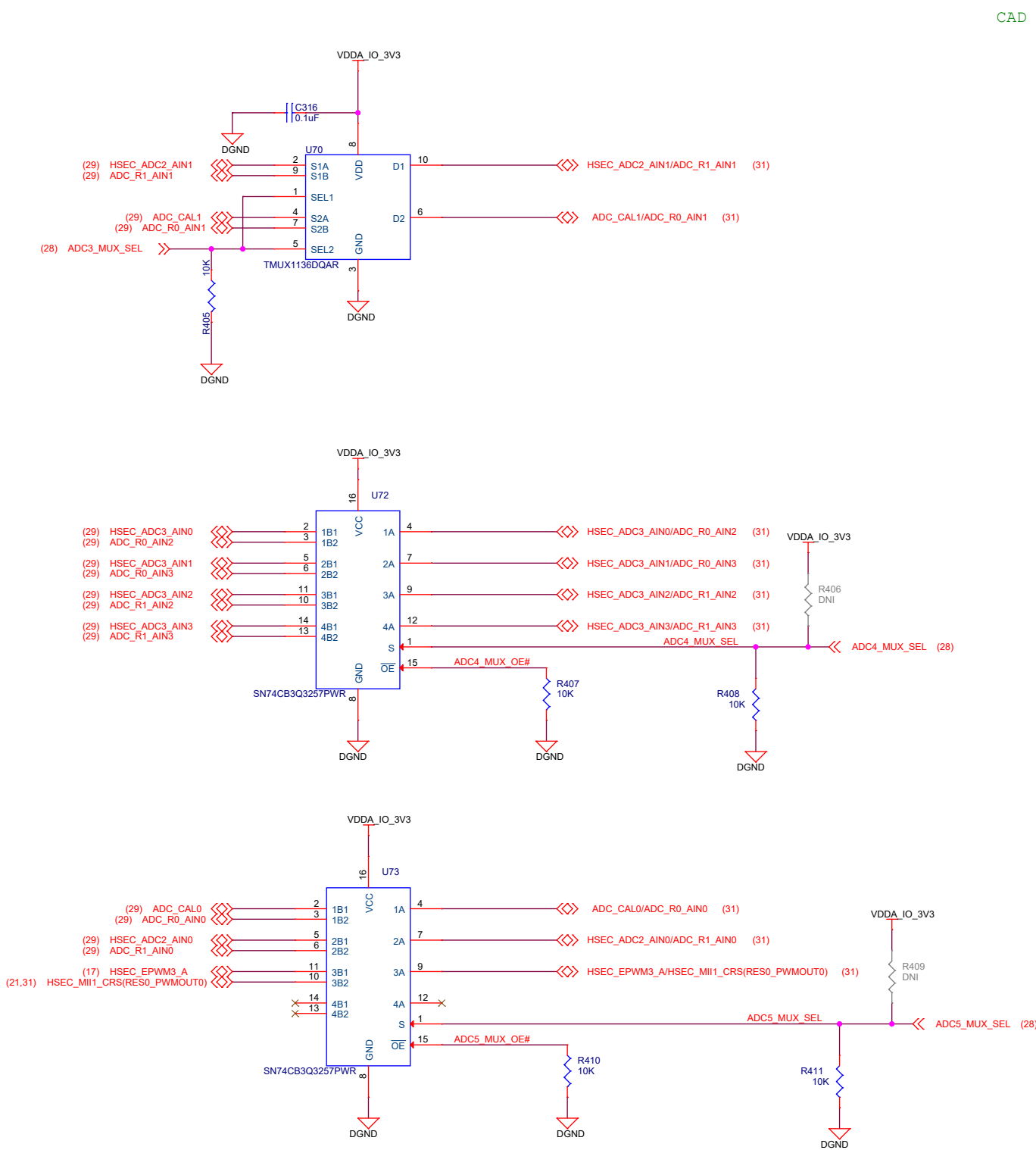
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Title SOC-ADC INTERFACE

Size	Variant Name = PROC159B(001)	Rev
C		B
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ADC MUXES

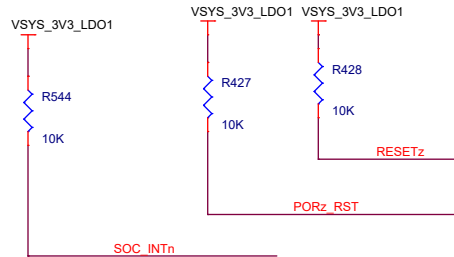
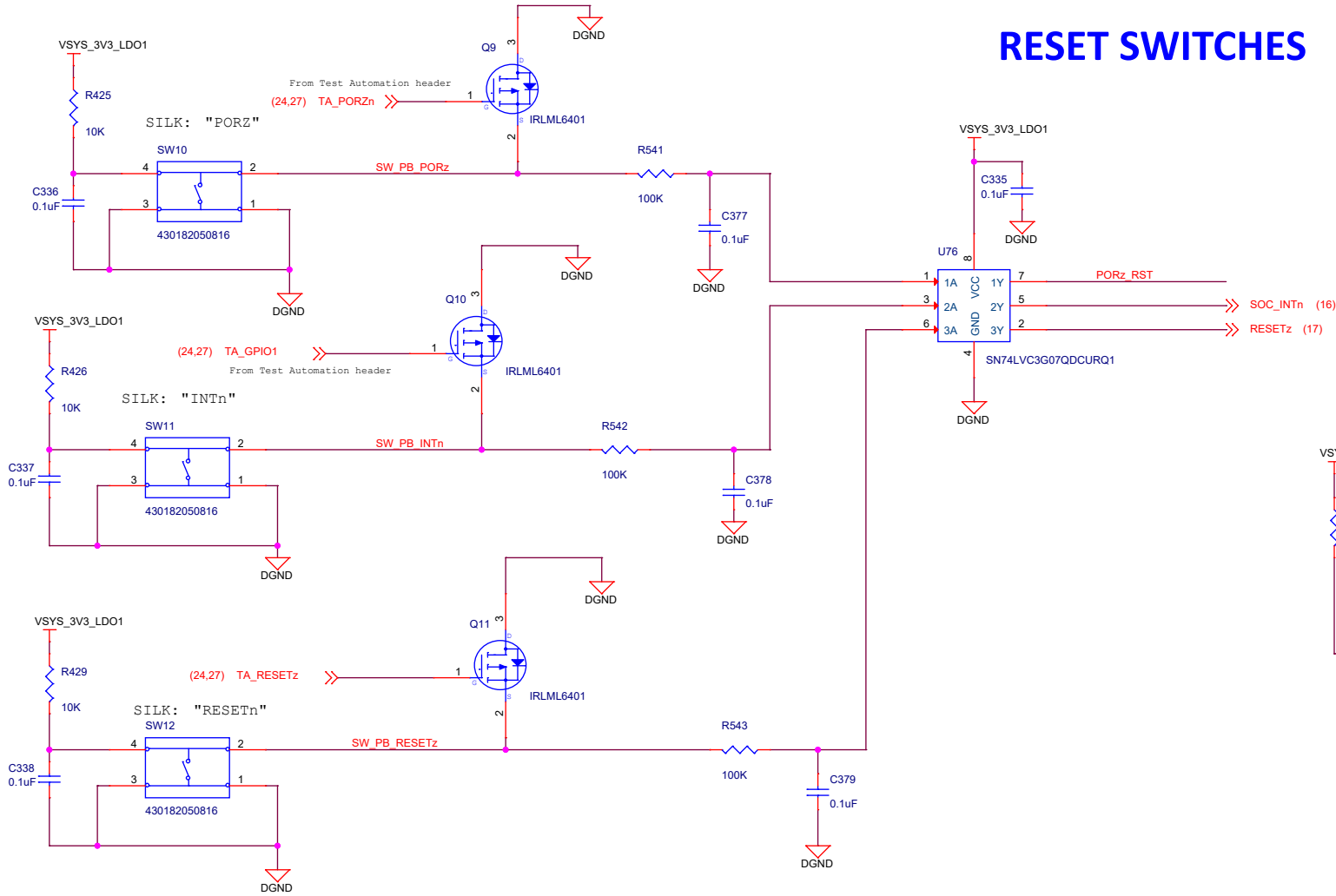


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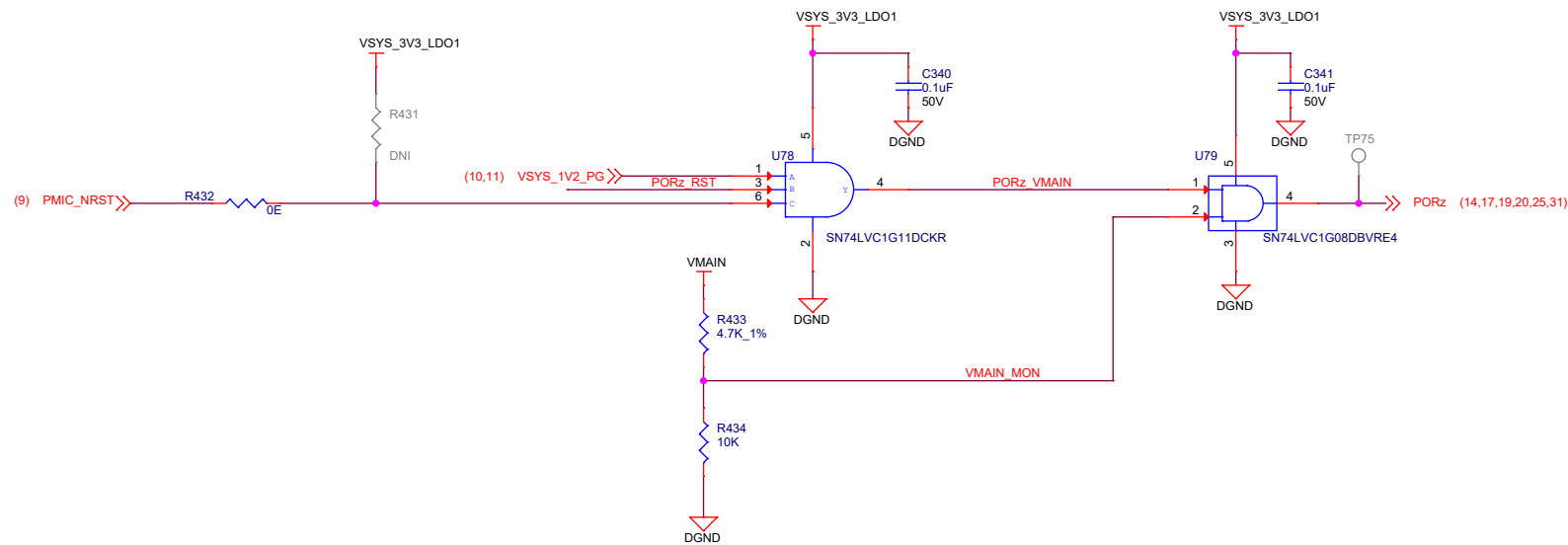


Title ADC MUXES		
Size	Variant Name = PROC159B(001)	Rev
C		B
Date:	Thursday, February 13, 2025	Sheet 30 of 33

RESET SWITCHES



PORz



Designed for T1 by Mistral Solutions Pvt Ltd



Title RESET SWITCHES		
Size	Variant Name = PROC159B(001)	Rev
C		B
Date:	Thursday, February 13, 2025	Sheet 32 of 33

EVM Development & Evaluation test circuitry

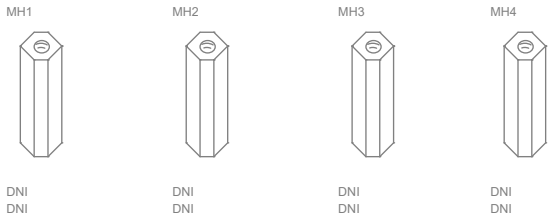
(TI EVM Only)

NOTES, HW & LABELS

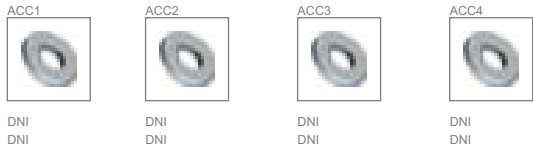
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

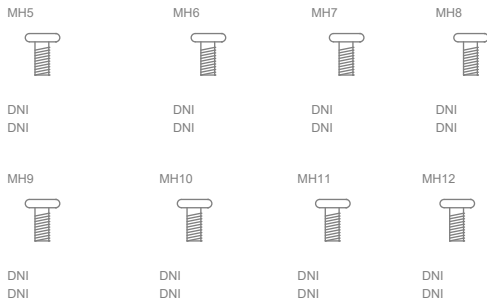
STANDOFFs



WASHER's



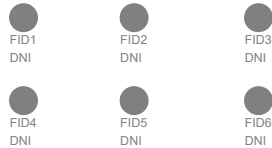
SCREWS



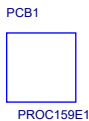
RUBBER FEET



FIDUCIALS



BARE PCB



SH-J2

SPC02SYAN

SH-J2 Shall be mounted on J20 to enable the PMIC VIA WAKE1 PIN OF PMIC

SH-J3

SPC02SYAN

SH-J3 Shall be mounted on J22 to enable the PMIC VIA WAKE2 PIN OF PMIC

SH-J4

SPC02SYAN

SH-J4 Shall be mounted on J21 to enable the TCAN WAKE

LOGOs

PCB
LOGO
DNI
Texas Instruments

PCB
LOGO
DNI
For Evaluation only; not FCC approved for resale

PCB
LOGO
DNI
WEEE Mark

PCB
LOGO
DNI
CE Mark

PCB
LOGO
DNI
High Temperature

LABELS

Board Serial No.



Assembly Revision.



EVM Orderable No.



Orderable Part Numbers

Variant	Label Text
001	TMDSCNCD263P
002	TMDSCNCD263P-SIP

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Title CC EVM NOTES,HW &LABELS

Size

C

Variant Name = PROC159B(001)

Rev

B

Date:

Thursday, February 13, 2025

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