

AM263P CC
PROC159E2

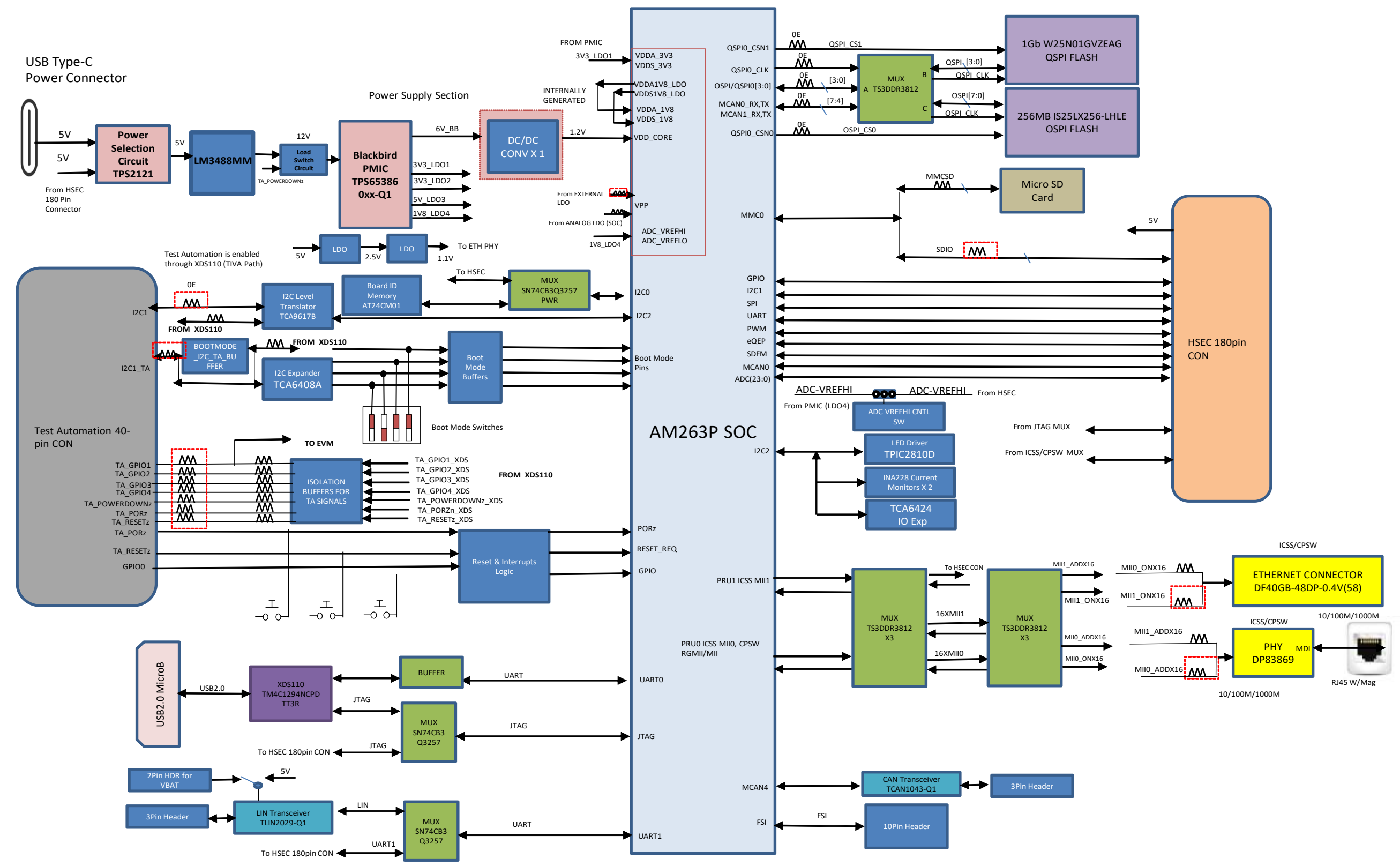
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REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	19 JUNE 2023	Drafted from REV E1 Schematics. Net names updated wrt SOC symbol (U1) pin naming conventions	Mistral Design Team		
0.02	21 JUNE 2023	Added MDIO/MDC Mux (U81) FOR MDIO0_MDIO and MDIO0_MDC signals. Changed the IO expander part (U60) from TCA6416ARTWR to TCA6424ARGJR and it's I2C slave address changed to 0x22	Mistral Design Team		
0.03	1 AUG 2023	Added Circuit for SoC Safety_error (Q20), Removed C3746 cap, C82 Cap changed to 6.8nF, DNI'd termination caps on ADC lines (C318 to C324). Added green LEDs for PMIC LDO rails	Mistral Design Team		
0.04	11 AUG 2023	Added layer of MUXing to allow MII0 OR MII1 to be inputs for either Ethernet interface - on-board PHY or Add-on board connector	Mistral Design Team		
0.05	16 AUG 2023	Added 1x2 header (J22) with jumper on INH/PMIC_WKUP2 net	Mistral Design Team		
0.06	18 AUG 2023	Added resistor mux across ICSSM Ethernet/HSEC lines	Mistral Design Team		
0.07	5 SEP 2023	Resistor muxes across ICSSM Ethernet/HSEC lines value changed from 0E to 33E	Mistral Design Team		
0.08	7 SEP 2023	SW15 - for ICSSM MII0/MII1 signals selection has been removed. SW14 will control all six ICSSM muxes	Mistral Design Team		
0.09	11 SEP 2023	Rearrangement is done wrt ICSSM signals, as resistor mux should now be at PHY end of the scheme. Rearranged signals on ADC Muxes (U70,U72,U73). DNI'd R205, Populated R204 for FSI activation. OSPI_LBCLK connection rearranged.	Mistral Design Team		
0.10	15 SEP 2023	Changed resistor arrays to individual 0201 0-ohm resistors on ICSSM lines. Added MDC/MDIO mux (U90) for Add on connector. DNI'd R3865, Populated R190 with default set to HSEC_EPWM11_A.	Mistral Design Team		
0.11	22 SEP 2023	Ethernet/HSEC muxes SEL lines changed to independently controllable SEL lines.(SW16 added for ICSSM1_MUX_SEL) Changed R474 to pull-up resistor to select CPSW for on-board PHY MDIO/MDC lines. Populated all ADC caps - 330 Pf. Populated resistors on MDC lines across U90 and U91). Changed ICSSM -> ICSS in all schematic titles	Mistral Design Team		
0.12	03 OCT 2023	Added shunt jumpers to the schematic for J20,J21,J22	Mistral Design Team		

SYSTEM BLOCK DIAGRAM



POWER SEQUENCE

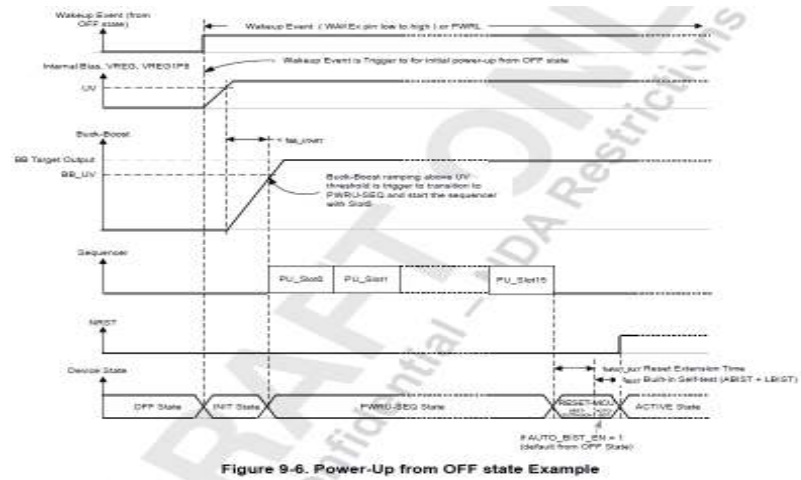
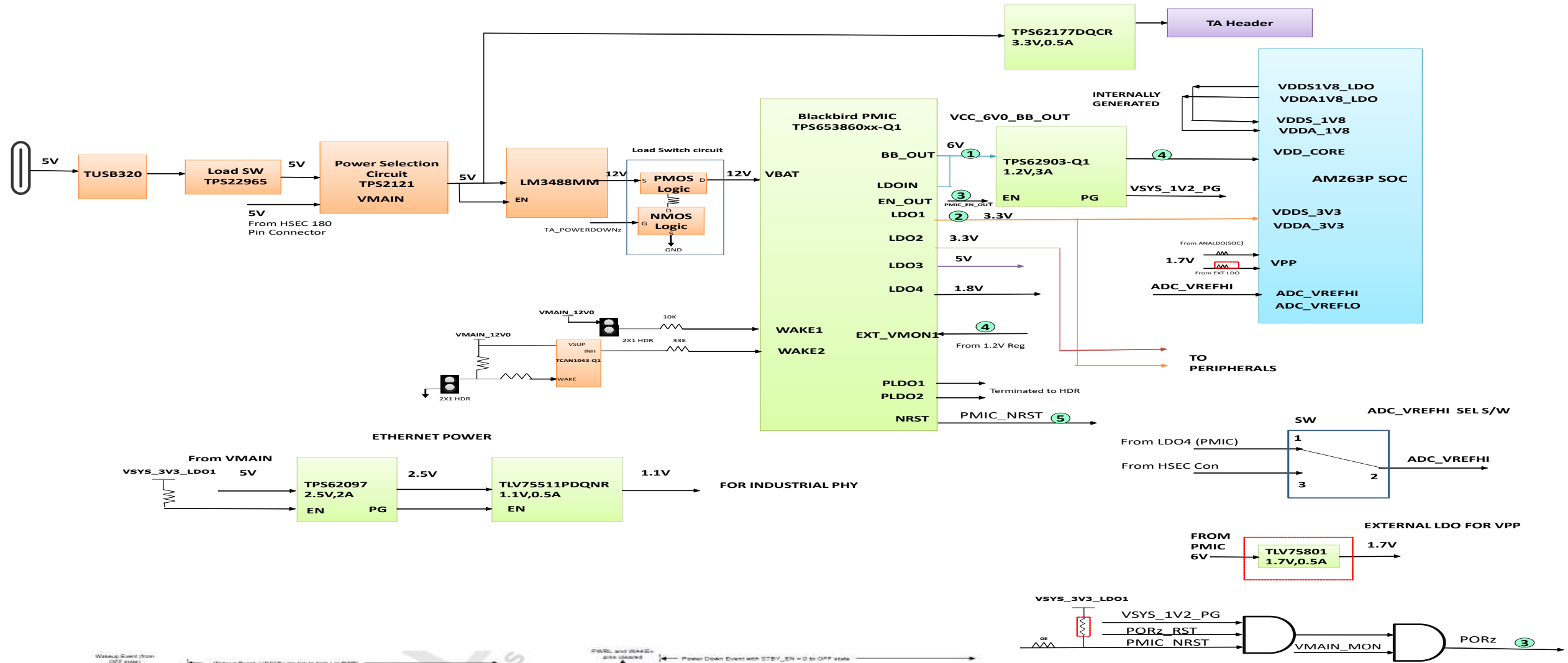


Figure 9-6. Power-Up from OFF state Example

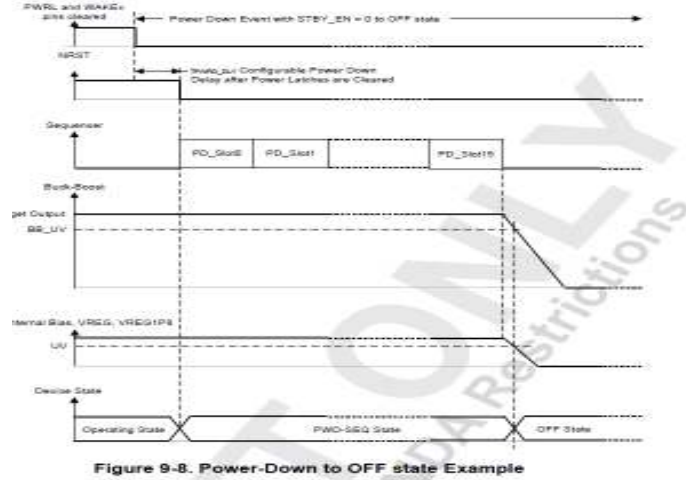
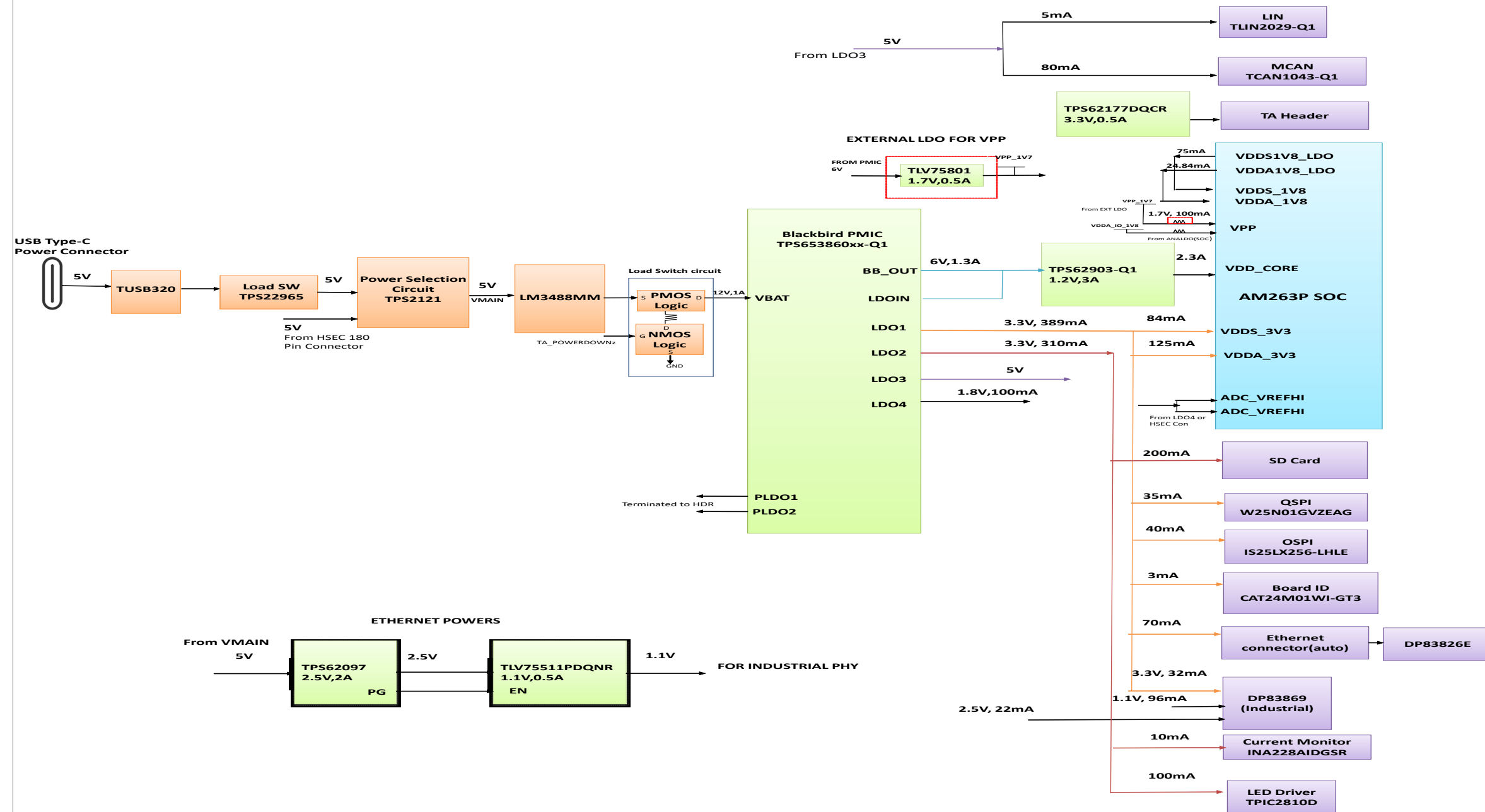
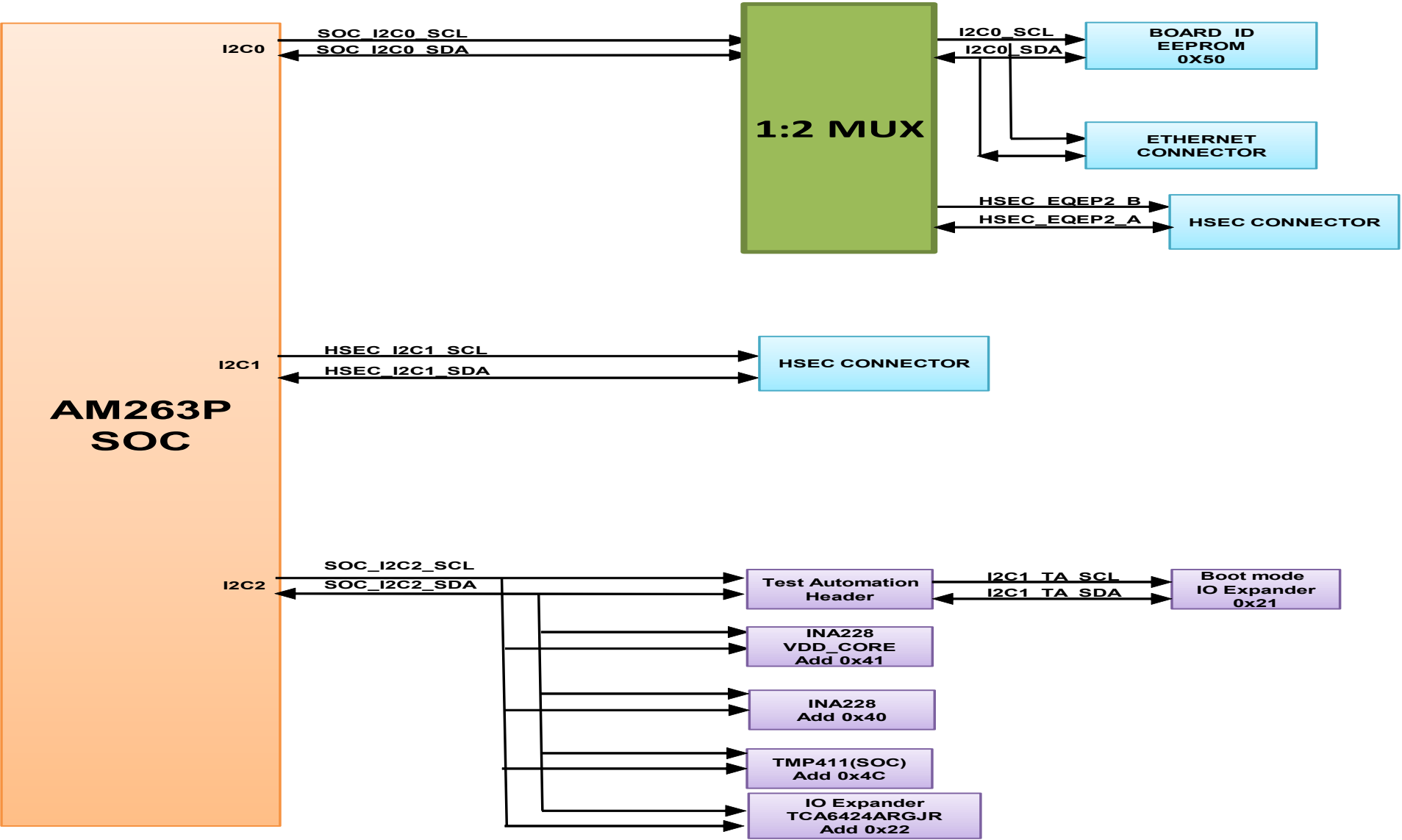


Figure 9-8. Power-Down to OFF state Example

POWER FLOW DIAGRAM



I2C TREE DIAGRAM

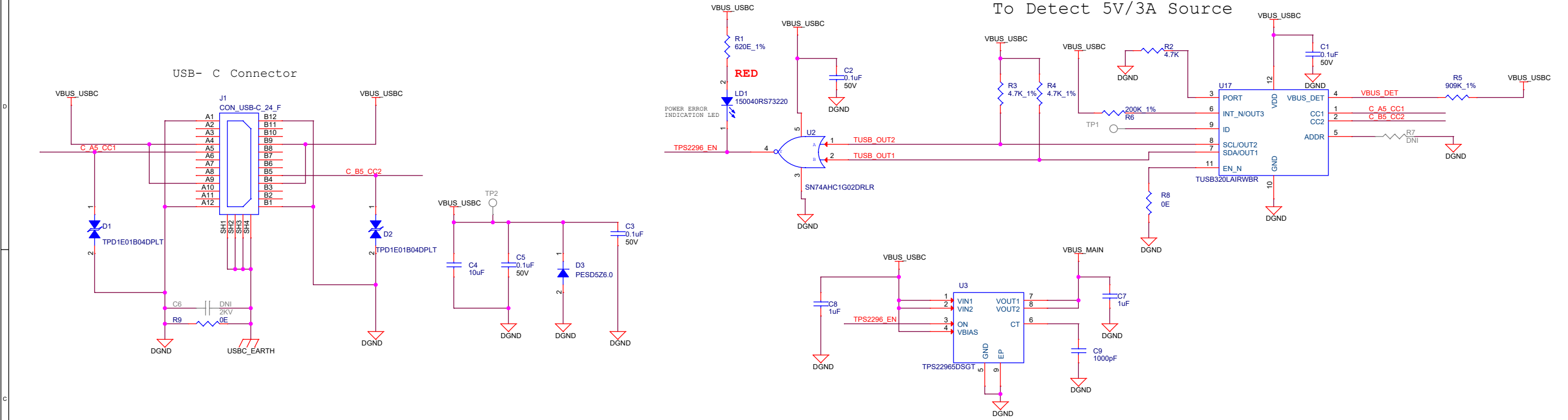


GPIO MAPPING TABLE

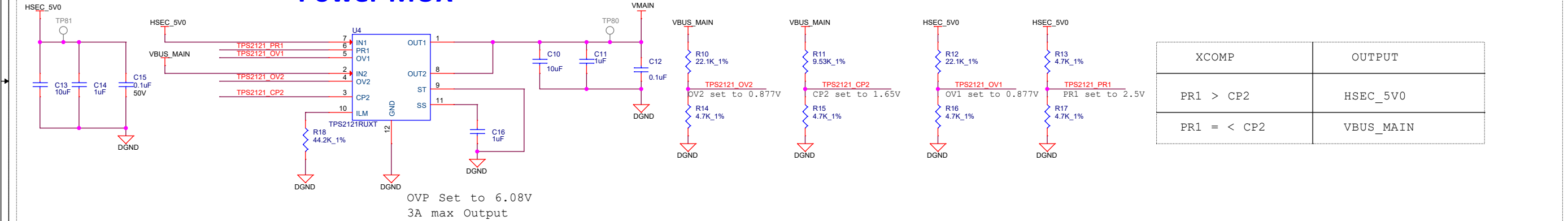
SI No.	GPIO DESCRIPTION	GPIO	Pin Name	FUNCTIONALITY	Net Name	ACTIVE STATE
1	Interrupt To SoC	GPIO21	LIN2_RXD	Interrupt	SOC_INTn	LOW
2	Interrupt To DP83826E/DP83TG720	GPIO67	EPWM12_A	Interrupt	ICSSM2_PWDN/INTn	LOW
3	User Defined LED	GPIO66	EPWM11_B	GPIO	USER_LED1	PREFERABLE
4	Interrupt To DP83869	GPIO68	EPWM12_B	Interrupt	ICSSM1_INT	LOW
5	User Defined LED	GPIO22	LIN2_TXD	GPIO	USER_LED0	PREFERABLE
6	Reset input to DP83869	GPIO35	RGMII1_TXC	Reset	GPIO_ICSSM1_RST	LOW
9	Reset input to Ethernet connector	GPIO36	RGMII1_TX_CTL	Reset	GPIO_ICSSM2_RST	LOW
10	Interrupt To SoC from PMIC	GPIO29	RGMII1_RXC	Interrupt	PMIC_INTn	LOW
11	Select line for OSPI and QSPI	GPIO37	RGMII1_TD0	Mux Selection	OSPI/QSPI_MUX_SEL	PREFERABLE
IO Expander 01						
12	Reset input to OSPI		P00	Reset	GPIO_OSPI_RSTn	LOW
13	Enable control to clock buffer		P01	Enable	CLK_BUF_EN	HIGH
14	Select line for ICSSM Ethernet/HSEC Mux (PRU1 signals)		P02	Mux Selection	ICSSM1_MUX_SEL	PREFERABLE
15	Select line for ICSSM ON-Board/ADD-ON PHY Mux		P03	Mux Selection	ICSSM2_MUX_SEL	PREFERABLE
16	Select line for MCAN and FSI MUX		P04	Mux Selection	FSI_MUX_SEL	PREFERABLE
17	Select line for ADC MUX 3		P05	Mux Selection	ADC3_MUX_SEL	PREFERABLE
18	Select line for ADC MUX 4		P06	Mux Selection	ADC4_MUX_SEL	PREFERABLE
19	Enable control to SD load switch		P07	Load SW Enable	GPIO_uSD_PWR_EN	HIGH
20	Select line for ADC MUX 5		P10	Mux Selection	ADC5_MUX_SEL	PREFERABLE
21	Select line for I2C0 MUX		P11	Mux Selection	I2C0_MUX_SEL	PREFERABLE
22	Select line for SPI1 MUX		P12	Mux Selection	SPI1_MUX_SEL	PREFERABLE
23	Select line for UART2 MUX		P13	MUX Selection	UART2_MUX_SEL	PREFERABLE
24	Enable control to 1.7V LDO		P14	LDO Enable	VPP_LDO_EN	PREFERABLE
25	Select line for LIN/UART MUX		P15	Mux Selection	LIN_MUX_SEL	PREFERABLE
26	Select line for ADC MUX 1		P16	Mux Selection	ADC1_MUX_SEL	PREFERABLE
27	Select line for ADC MUX 2		P17	Mux Selection	ADC2_MUX_SEL	PREFERABLE
28	GPIO to HSEC		P20	GPIO	HSEC_GPIO	PREFERABLE
29	Standby input to CAN transceiver		P21	GPIO	MCAN1_STB	HIGH
30	Select line for MDIO/MDC Mux sel 1		P22	Mux Selection	MDIO/MDC_MUX_SEL1	PREFERABLE
31	Select line for MDIO/MDC Mux sel 2		P23	Mux Selection	MDIO/MDC_MUX_SEL2	PREFERABLE
32	Select line for ICSSM Ethernet/HSEC Mux (PRU0 signals)		P24	Mux Selection	ICSSM0_MUX_SEL	PREFERABLE

USB-C Power

Configured as UFP MODE
To Detect 5V/3A Source

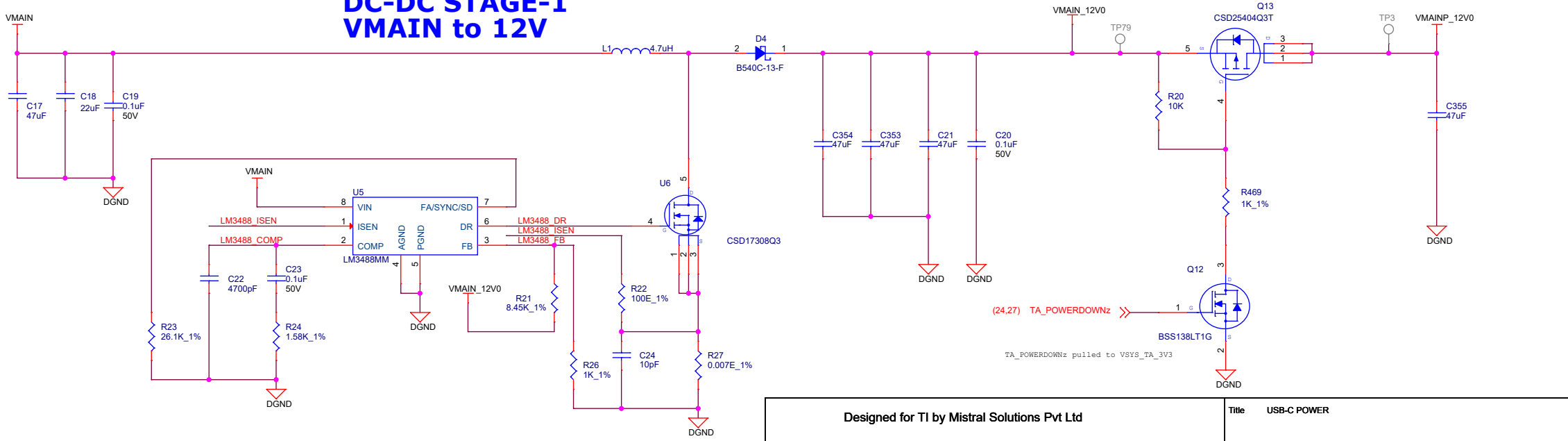


Power MUX



Designed as per reference sch

DC-DC STAGE-1
VMAIN to 12V



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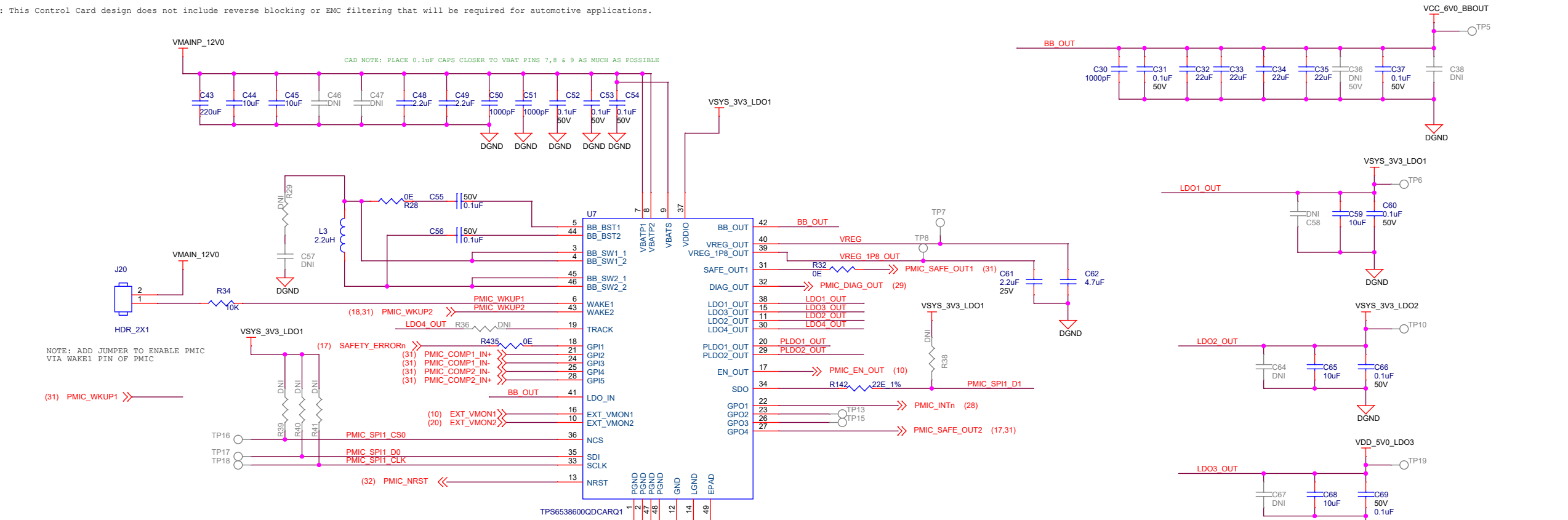


TitleUSB-C POWER

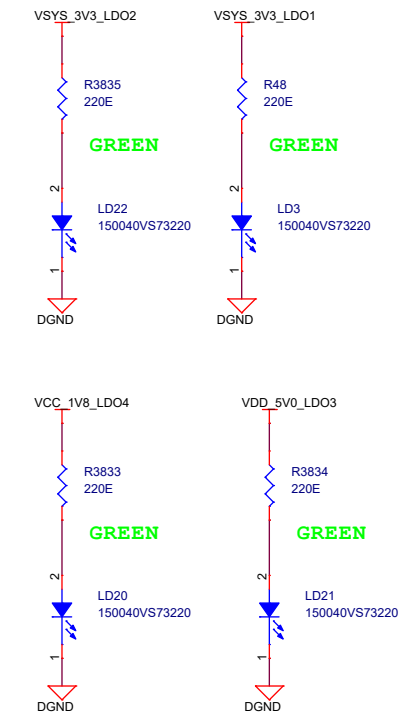
Size		Rev
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Date:	Friday, September 22, 2023	Sheet 8 of 33

BLACKBIRD PMIC

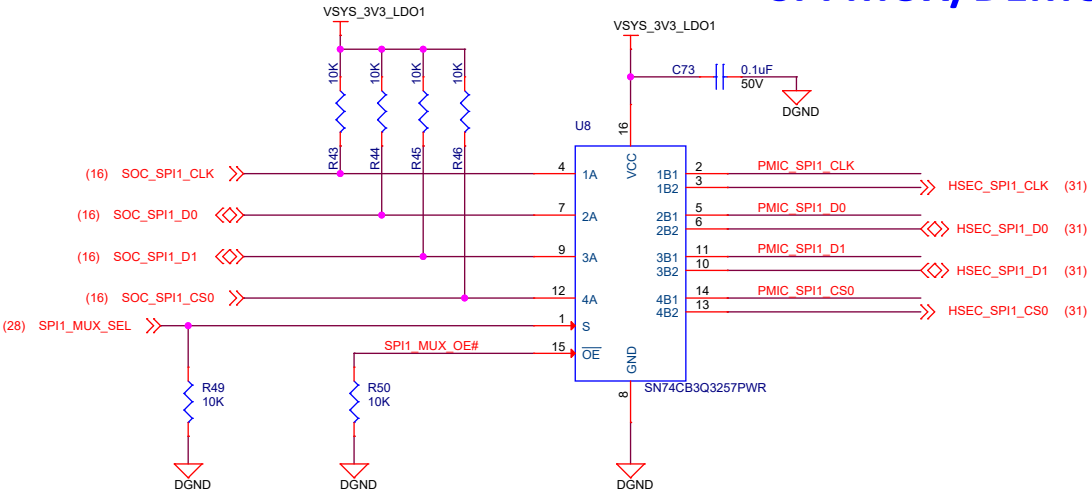
NOTE: This Control Card design does not include reverse blocking or EMC filtering that will be required for automotive applications.



Power LEDs for PMIC LDOs

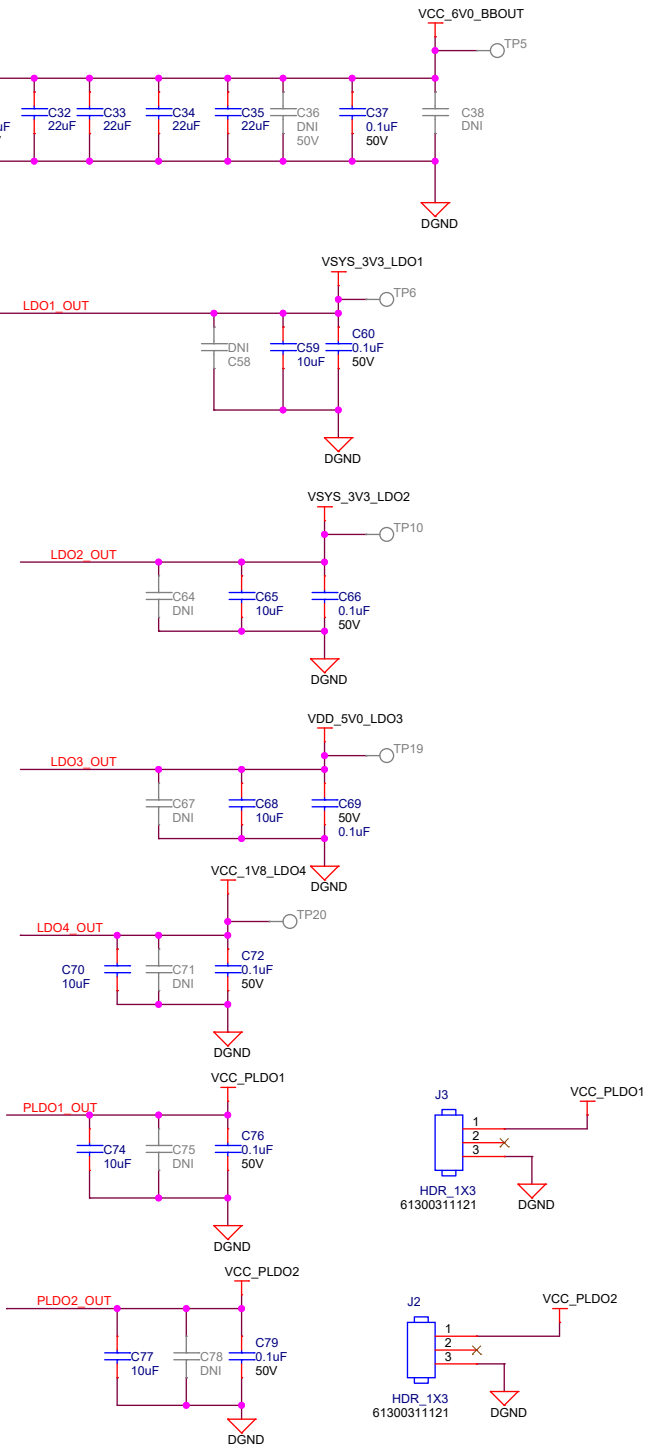


SPI MUX/DEMUX



SPI1 - 1:2 MUX

SEL	CONDITION	FUNCTION
LOW	PMIC SELECTED	A-->B1 port
HIGH	HSEC SPI1 selected	A-->B2 port



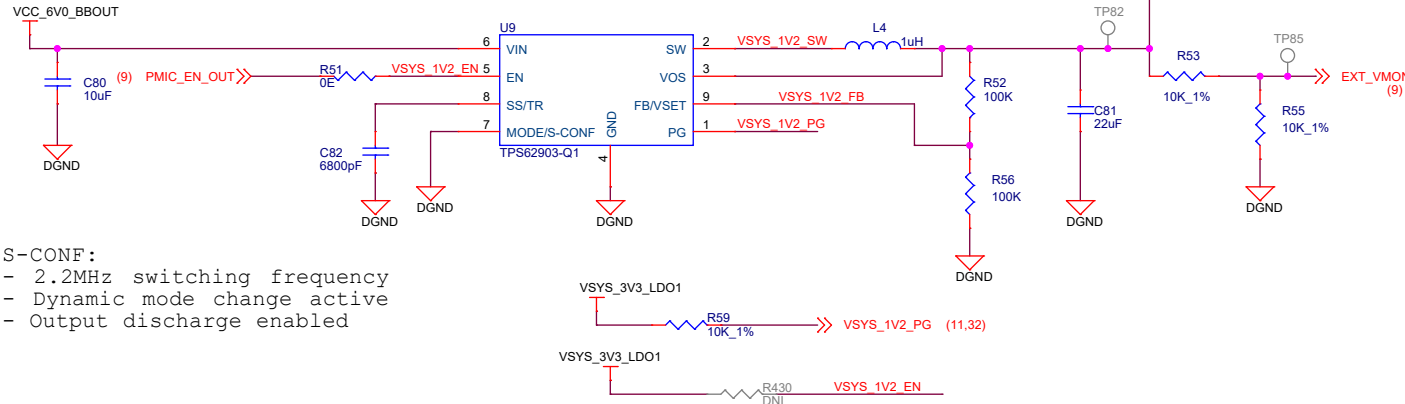
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Title BLACKBIRD PMIC		
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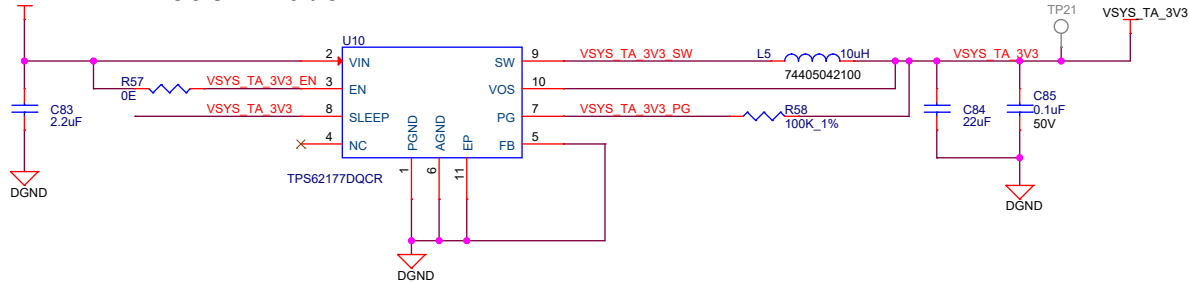
Power Supply #1

1.2V Generation



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S-CONF:
- 2.2MHz switching frequency
- Dynamic mode change active
- Output discharge enabled
```

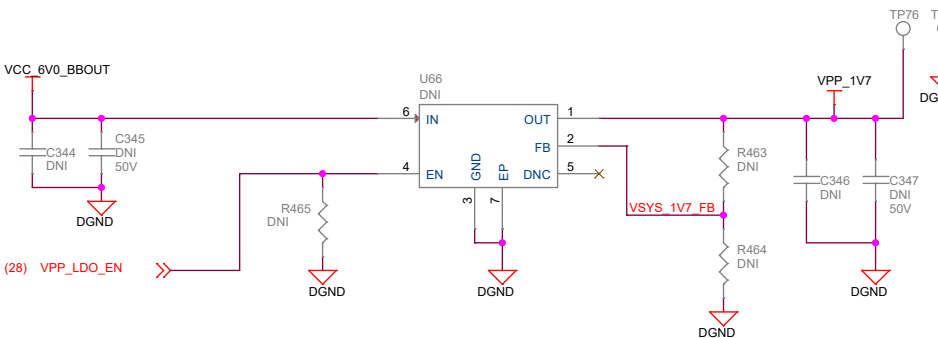
Test Automation Header Supply

TPS62177 3.3V BUCK REGULATOR
Vout = 3.3V
Iout = 0.5A

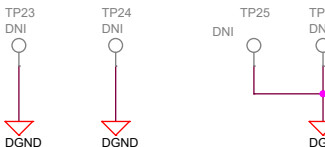
1.7V VPP Generation

TLV75801
Vout=1.7V
Iout = .5A

Place testpoints with
100mils spacing to
insert external jumper



Ground Test Points



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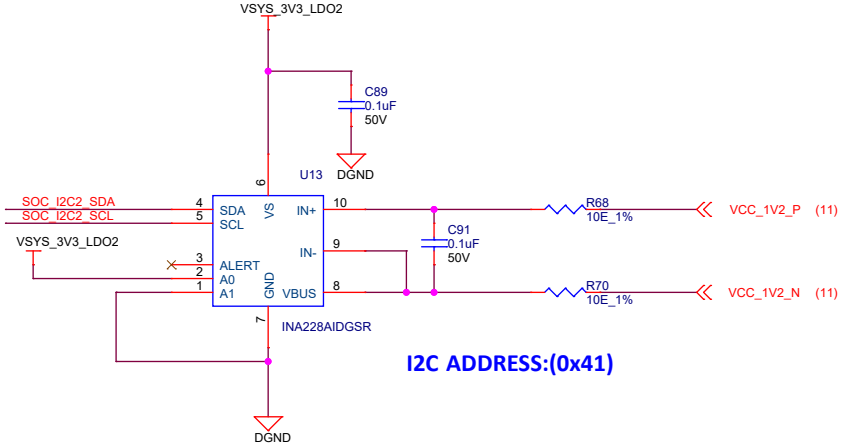
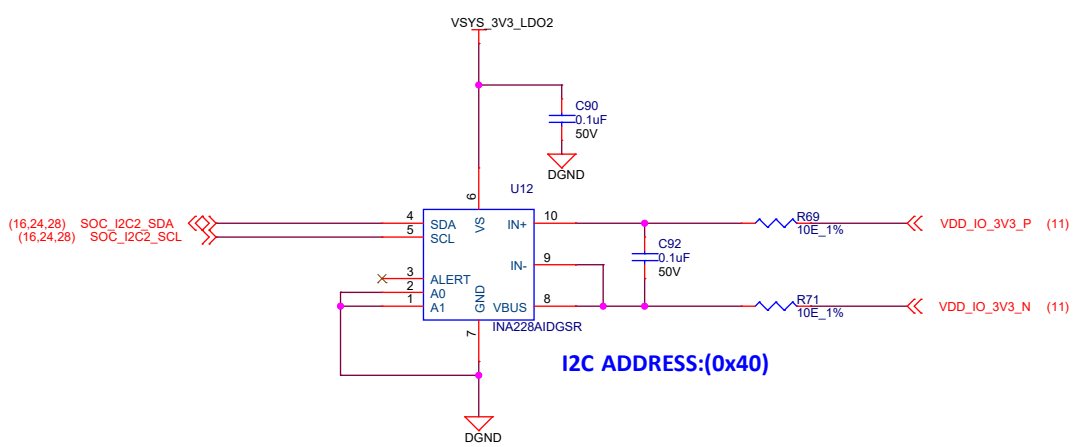
Title	POWER SUPPLY #1
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Size	
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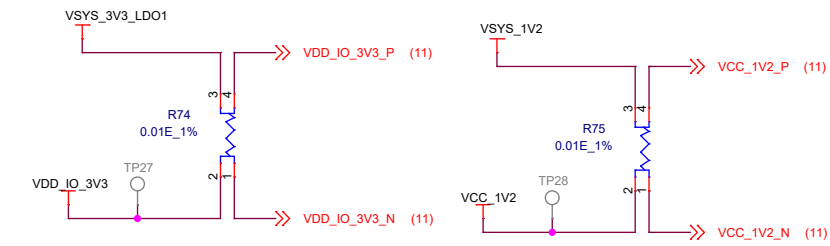
Rev
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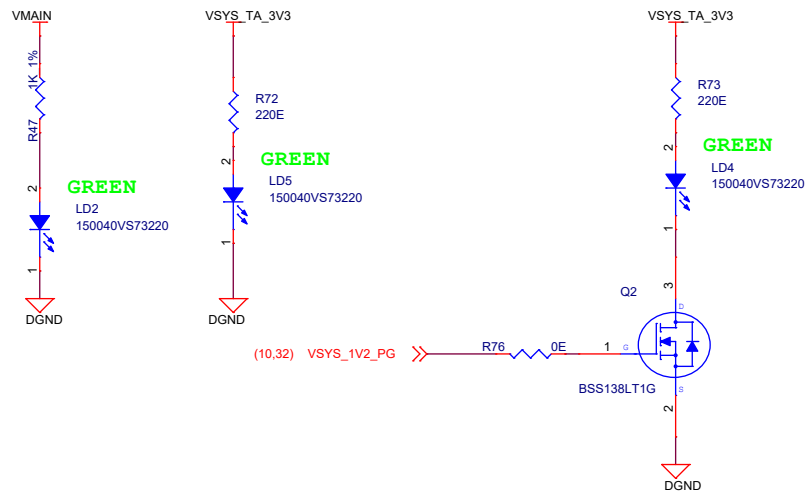
Current Monitors



Voltage In-Line Resistors



Power LEDs



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Title CURRENT MONITORING DEVICES

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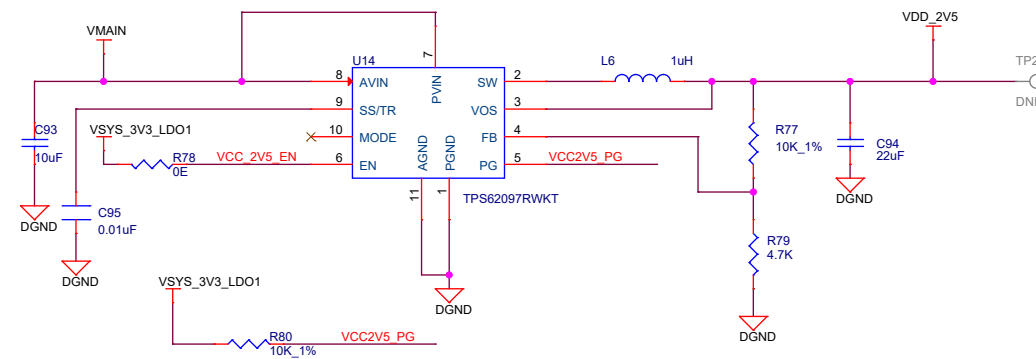
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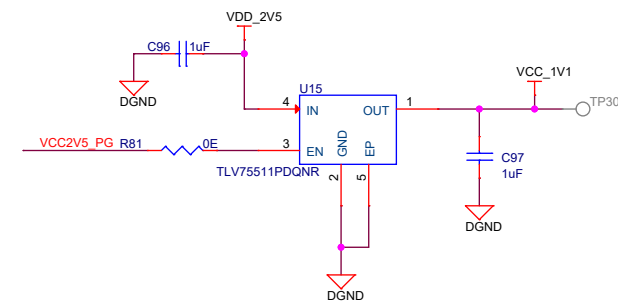
Rev E2

Ethernet Powers

2.5V ETHERNET PHY POWER SUPPLY

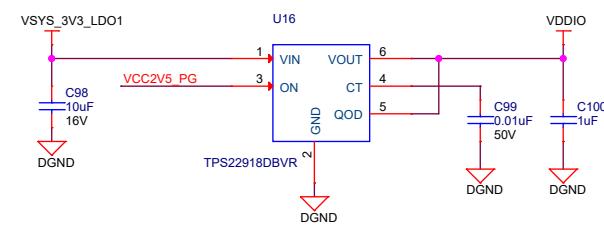


1.1V, 0.5AMPS SUPPLY



FOR INDUS PHY

Load Switch



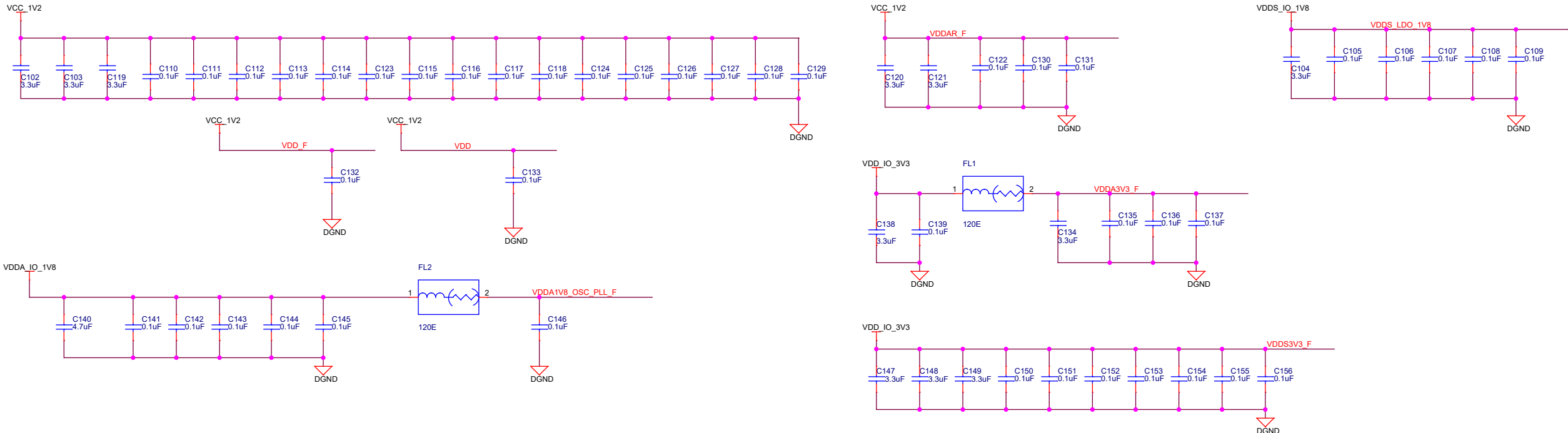
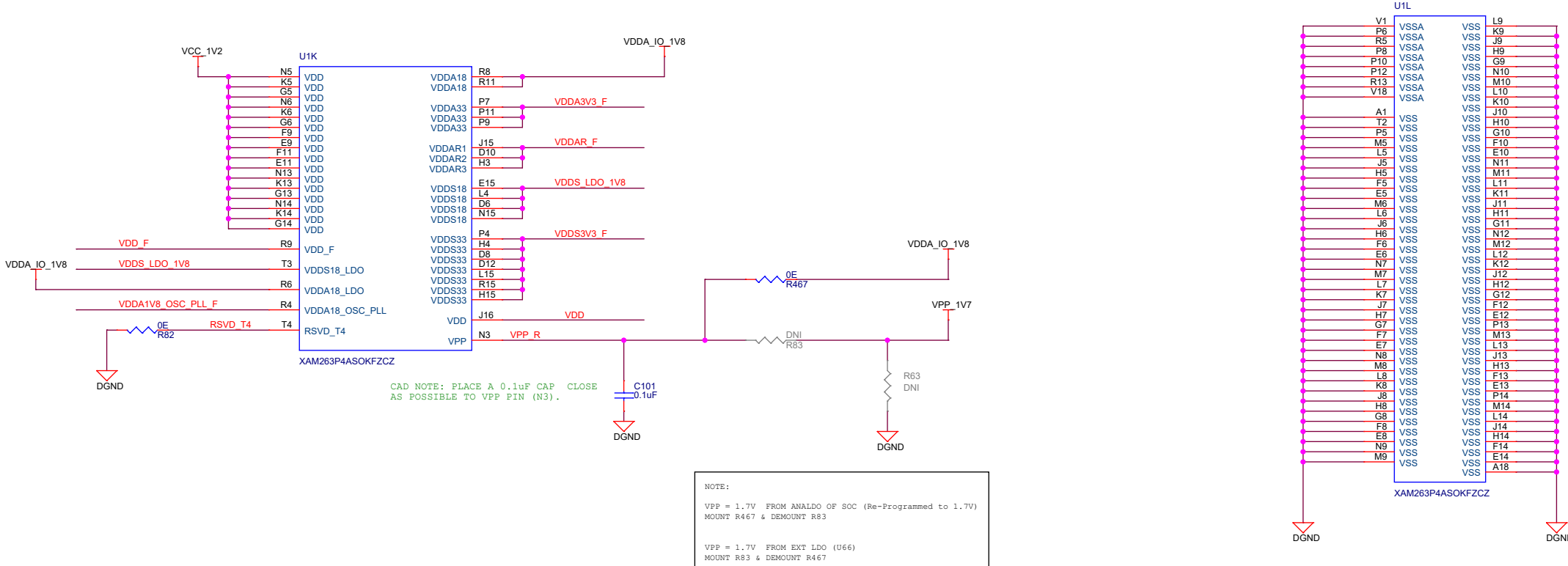
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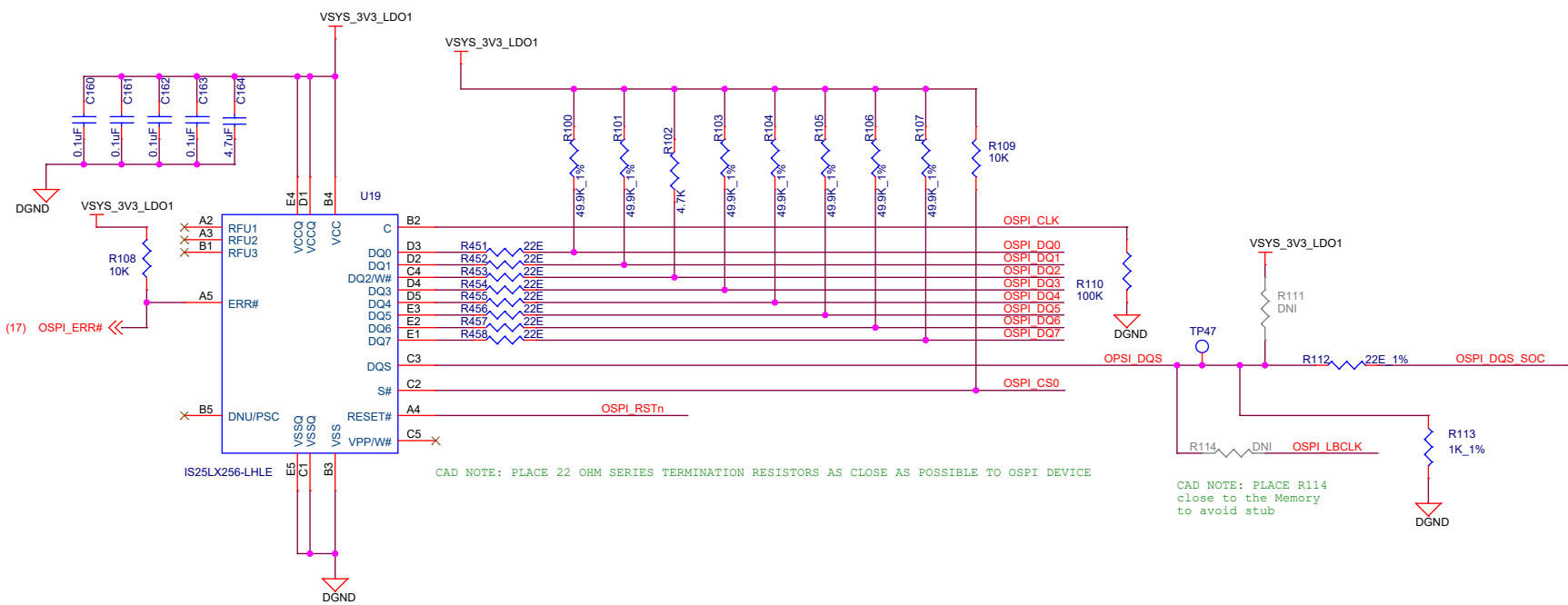
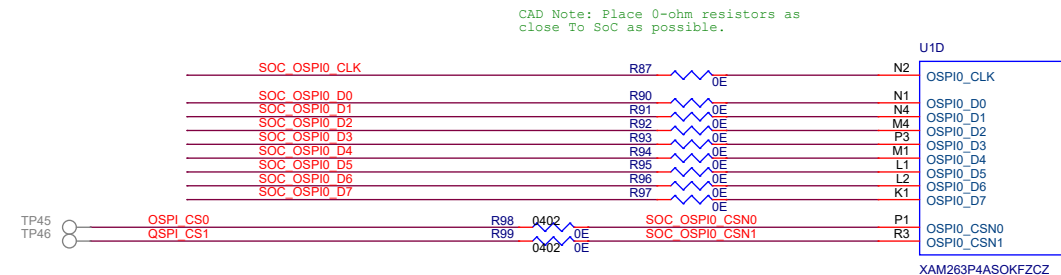
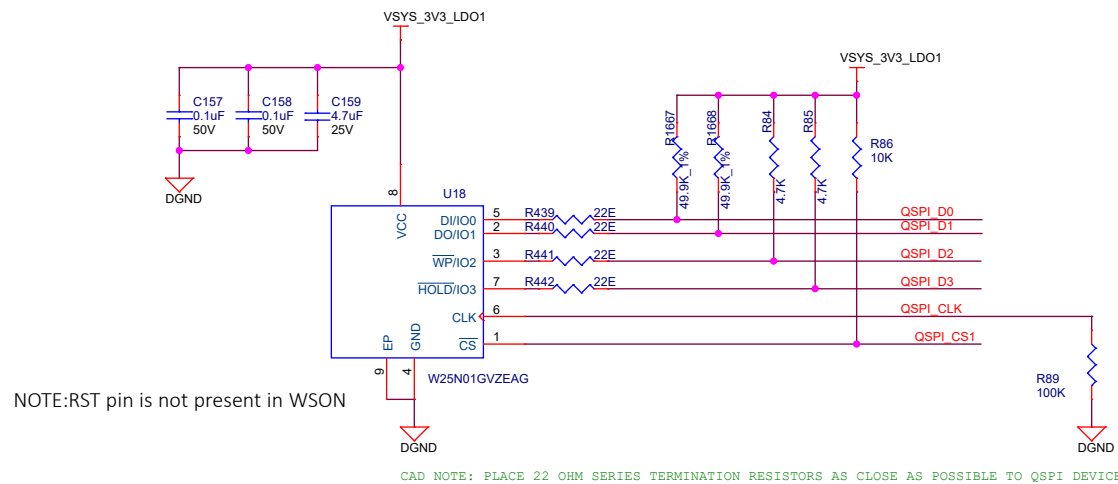
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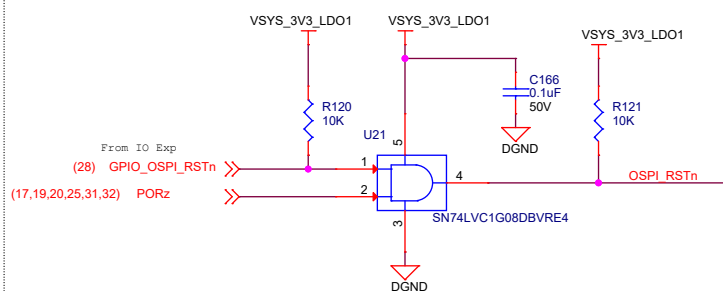
SOC-POWER and GND



SOC - QSPI & OSPI Interface

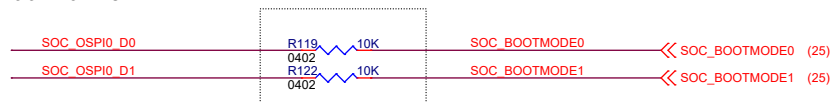


OSPI FLASH RESET



BOOTMODES

CAD NOTE: Place the resistors close to SOC as possible



SEL 1 & 2	CONDITION	FUNCTION
LOW	QSPI SELECTED	A-->B port
HIGH	OSPI selected	A-->C port

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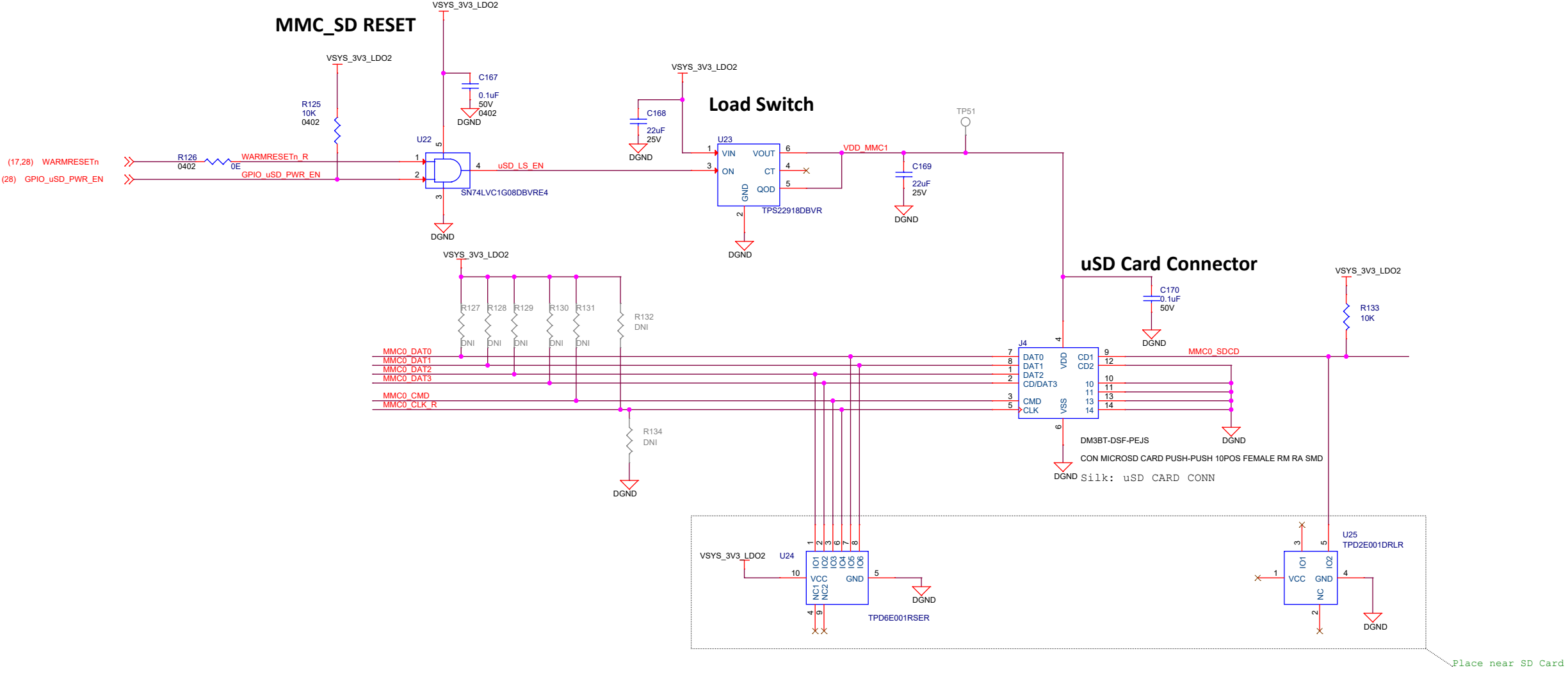
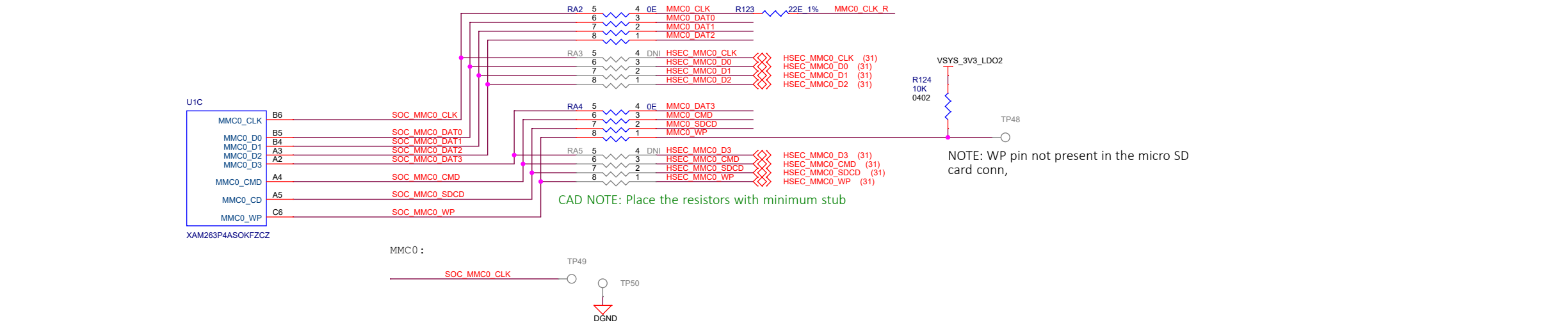
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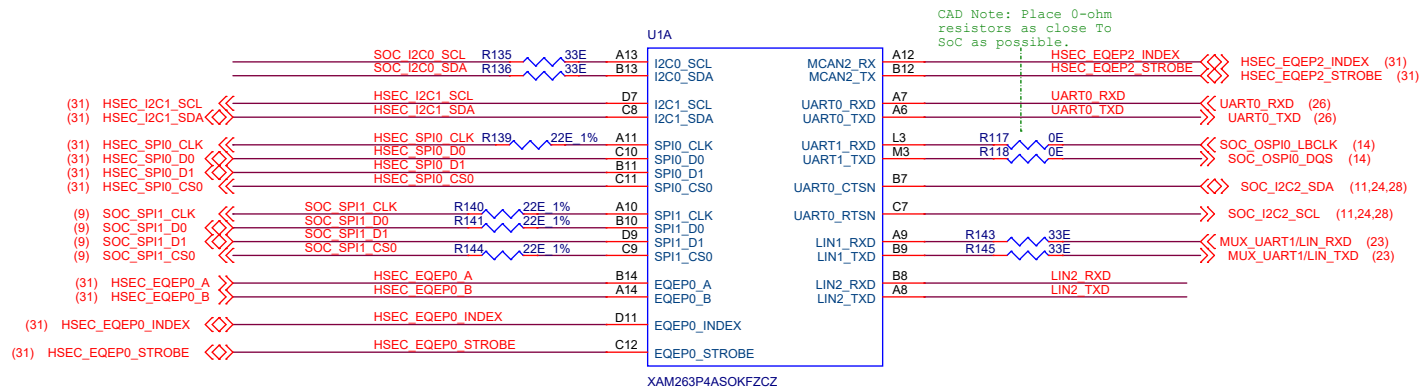
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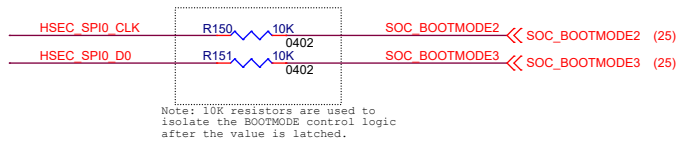
SOC- MMC0 Interface



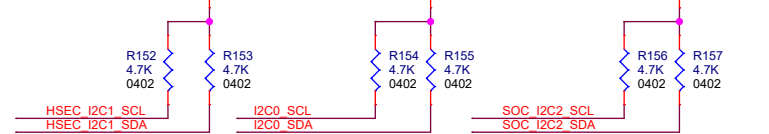
SOC-IO Interfaces



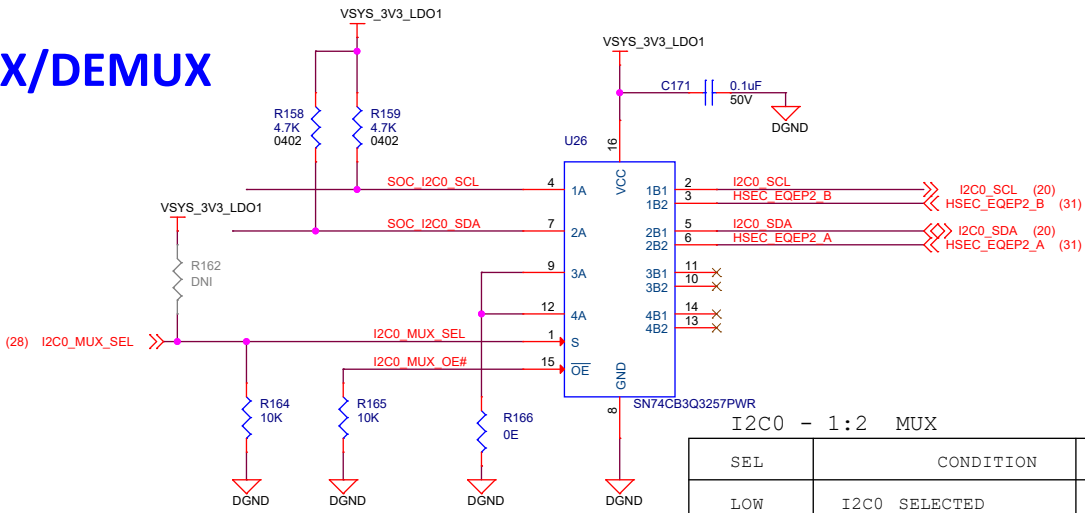
BOOTMODES



I2C Pull-ups



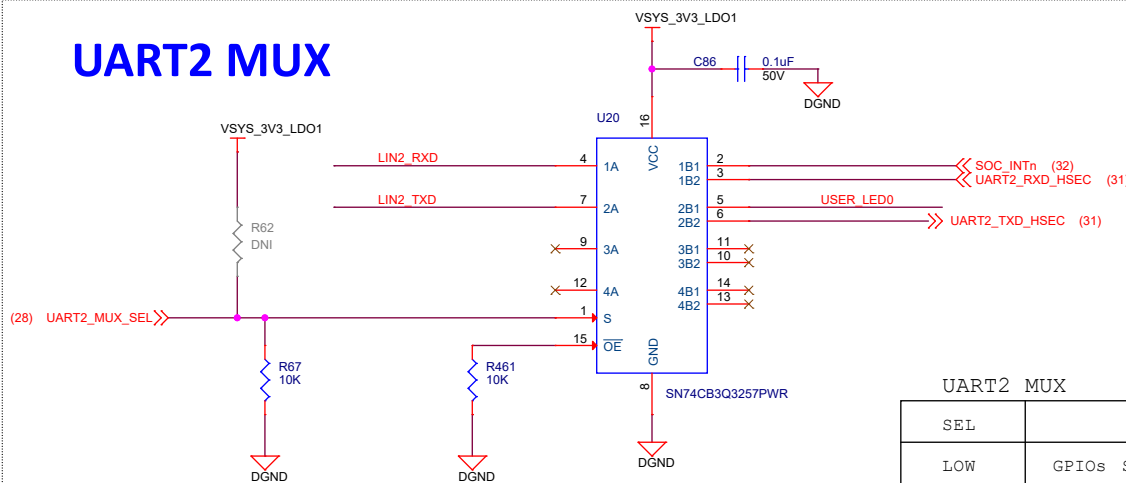
I2C0 MUX/DEMUX



I2C0 - 1:2 MUX

SEL	CONDITION	FUNCTION
LOW	I2C0 SELECTED	A-->B1 port
HIGH	HSEC EQEP selected	A-->B2 port

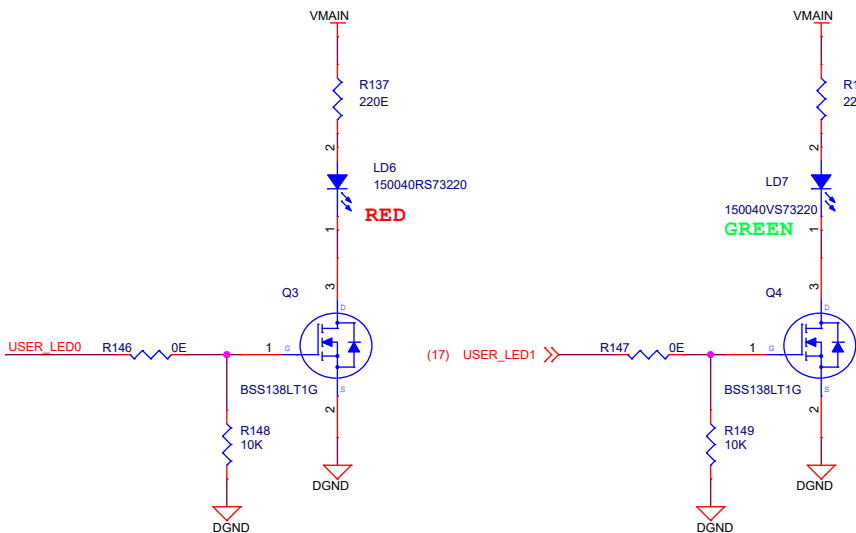
UART2 MUX



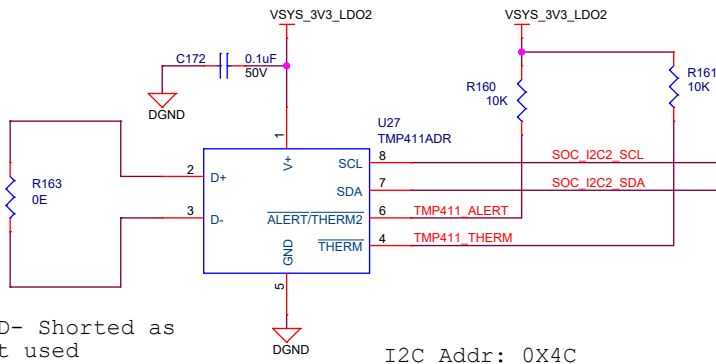
UART2 MUX

SEL	CONDITION	FUNCTION
LOW	GPIOs SELECTED	A-->B1 port
HIGH	HSEC UART2 selected	A-->B2 port

USER LEDs

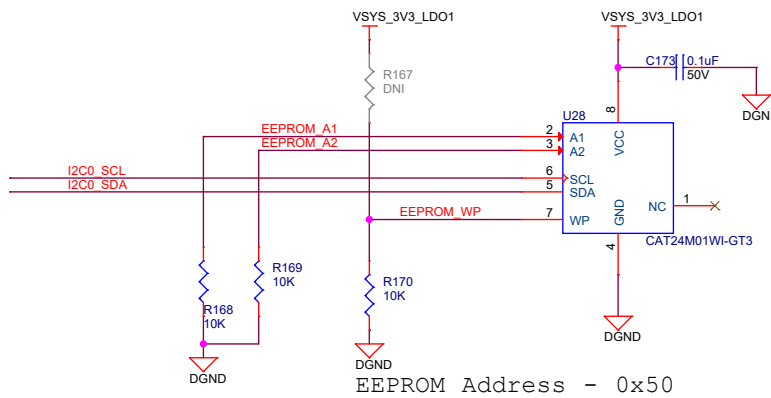


Temperature Sensor



I2C Addr: 0x4C
PCB Note: Place Close To SOC

Board ID EEPROM



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Title SOC-IO Interfaces

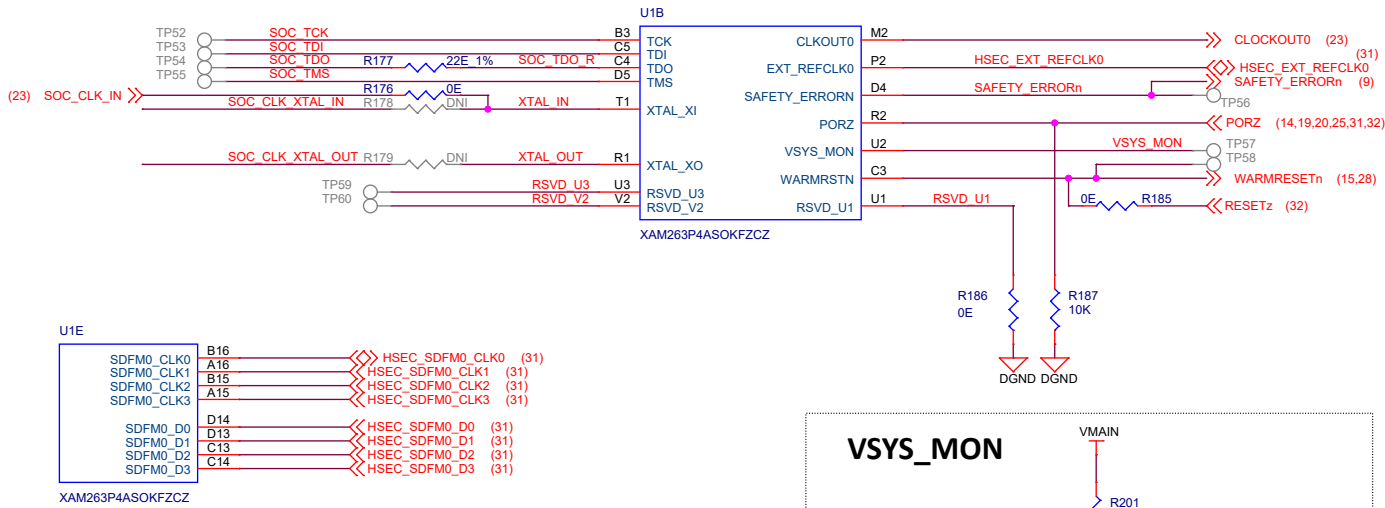
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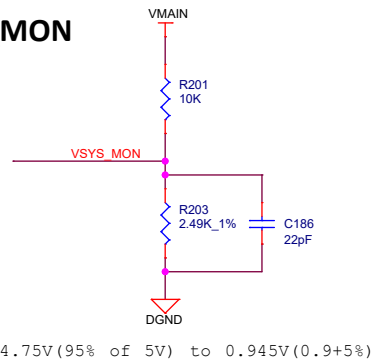
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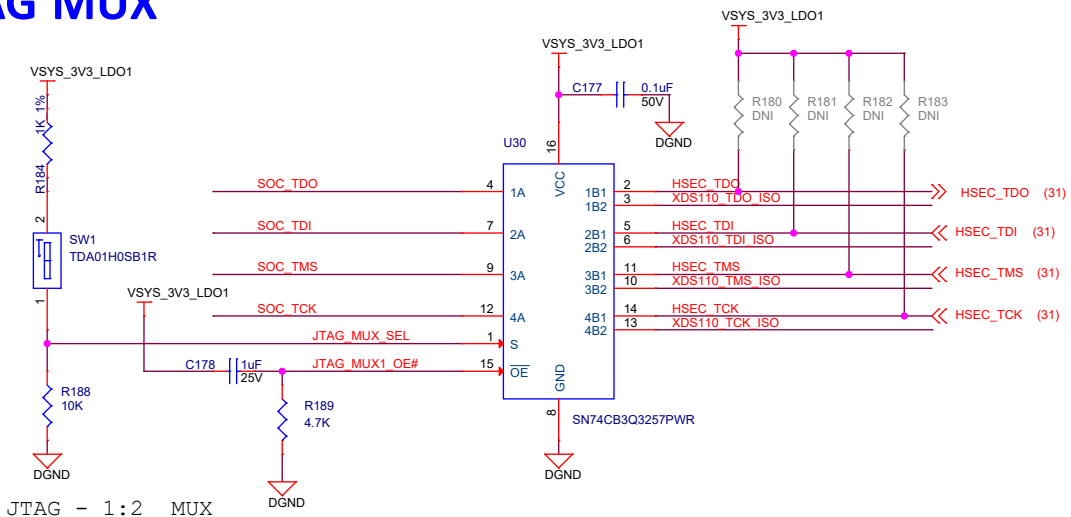
SOC JTAG, RESET and CLKS



VSYS_MON

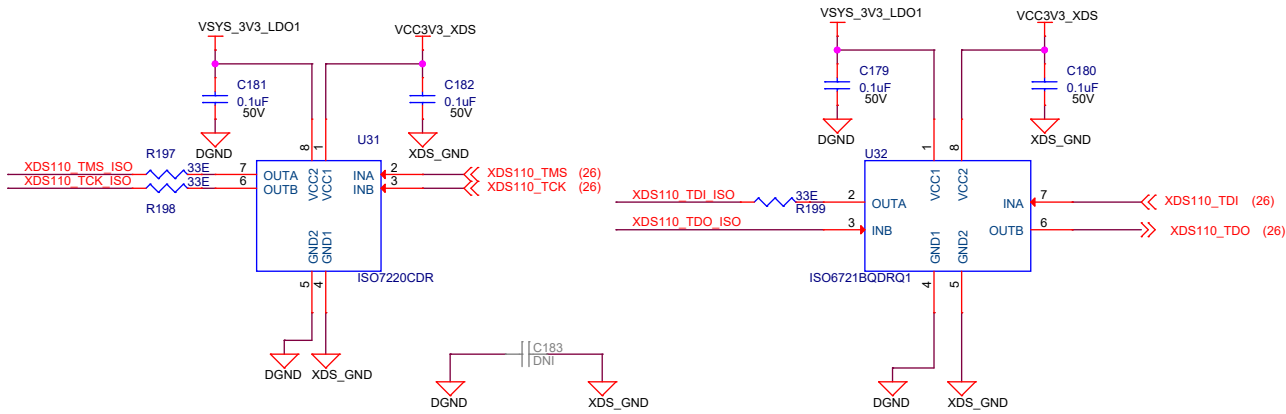


JTAG MUX

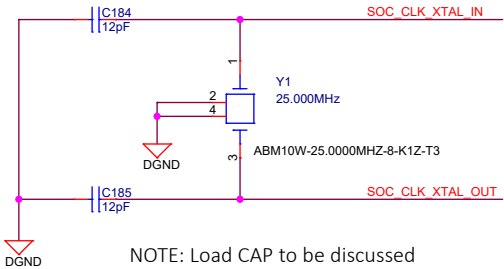


SW1.1	CONDITION	FUNCTION
LOW	HSEC EMU selected	A-->B1 port [EXTERNAL EMU]
HIGH	XDS110 selected	A-->B2 port [ON Board EMU]

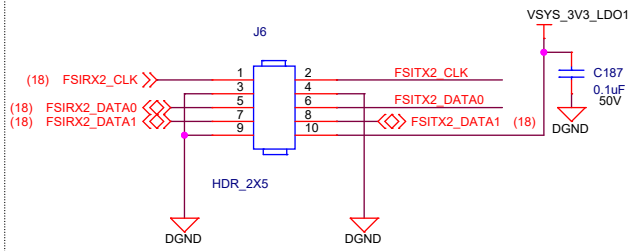
ISOLATION FOR XDS110



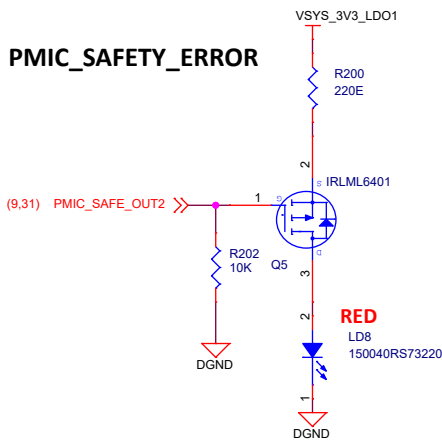
SOC Clock



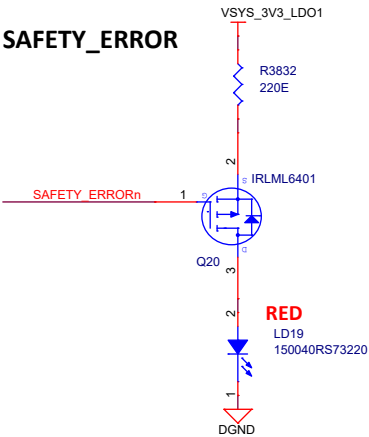
FSI Header



PMIC_SAFETY_ERROR



SAFETY_ERROR



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Title SOC JTAG, RESET and CLKS

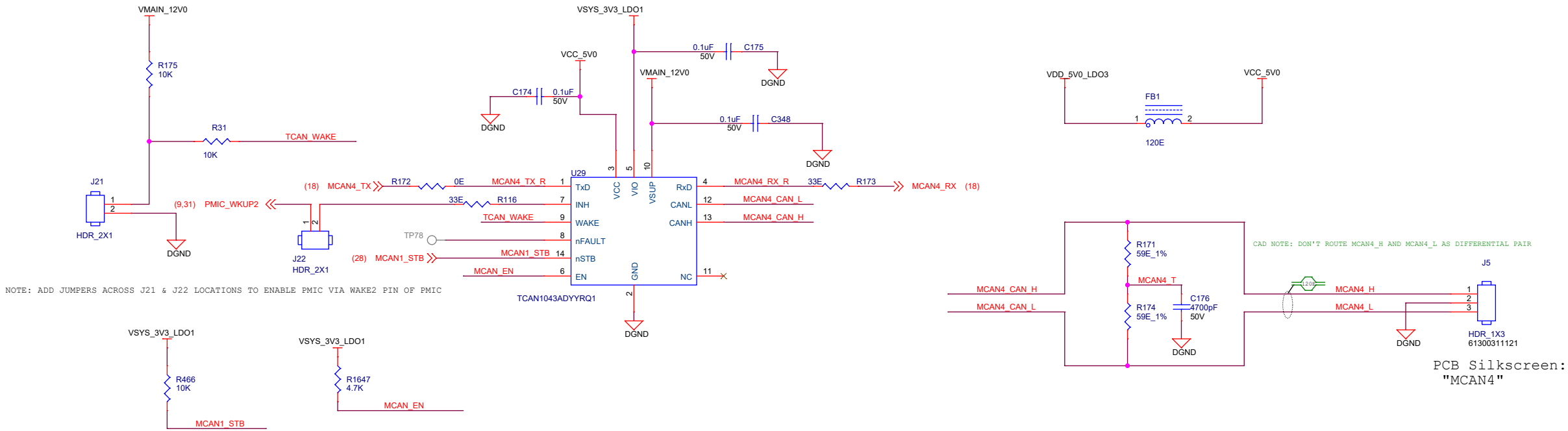
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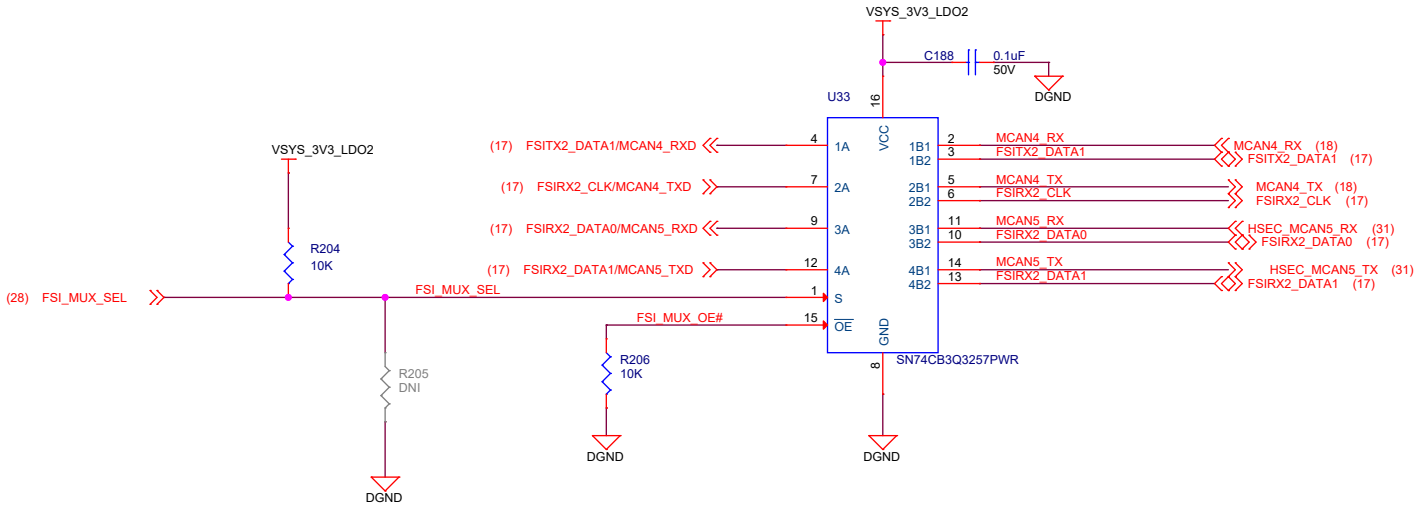
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MCAN Interface



MCAN AND FSI MUX



FSI MUX

SEL	CONDITION	FUNCTION
LOW	MCAN for CAN & HSEC SELECTED	A-->B1 port
HIGH	FSI SELECTED	A-->B2 port

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Title MCAN AND FSI MUX

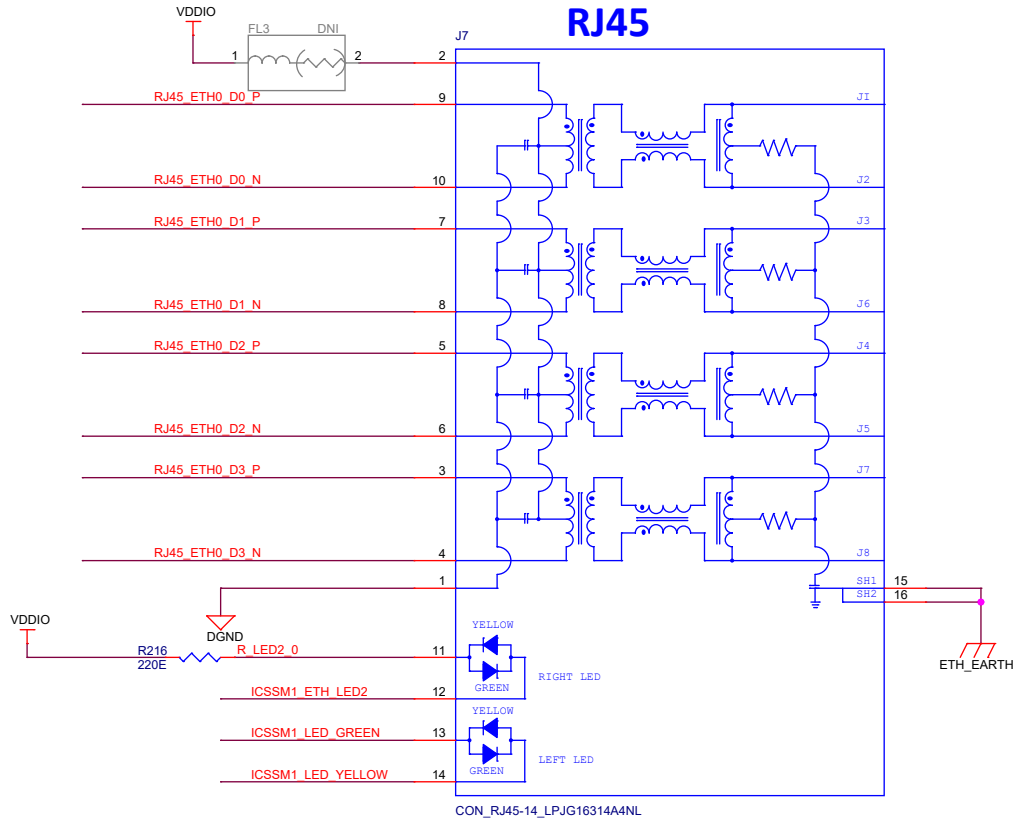
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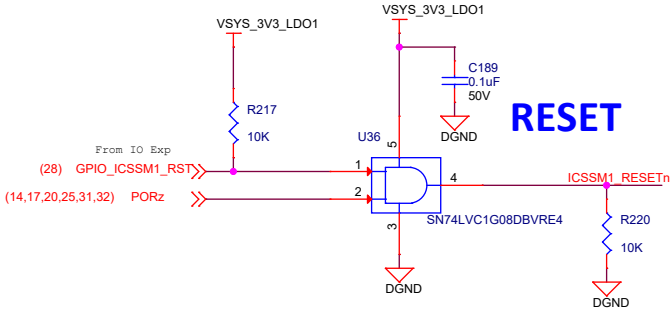
PRU0 ICSS MII0, CPSW RGMII/MII Ethernet

RJ45

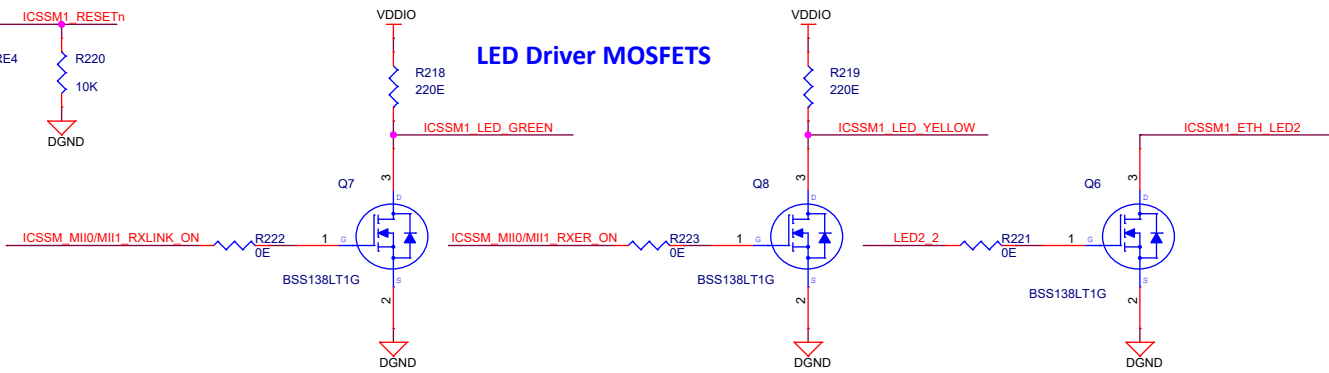


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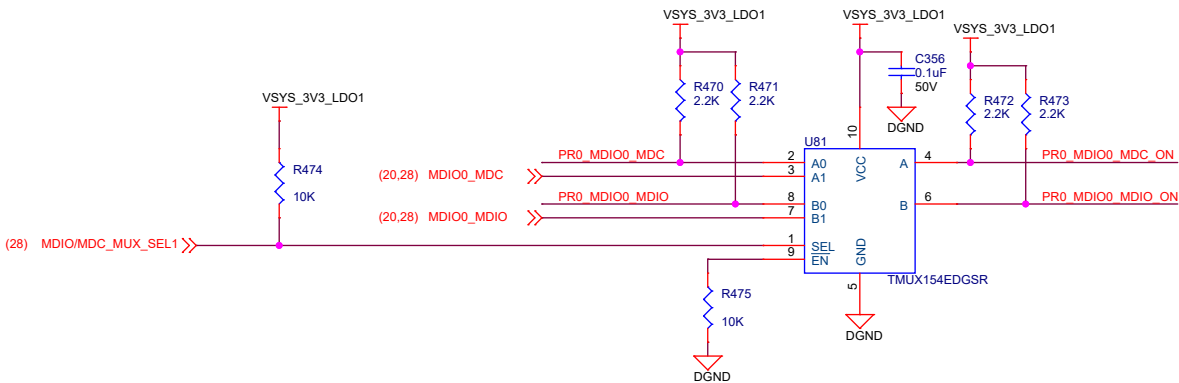
RESET



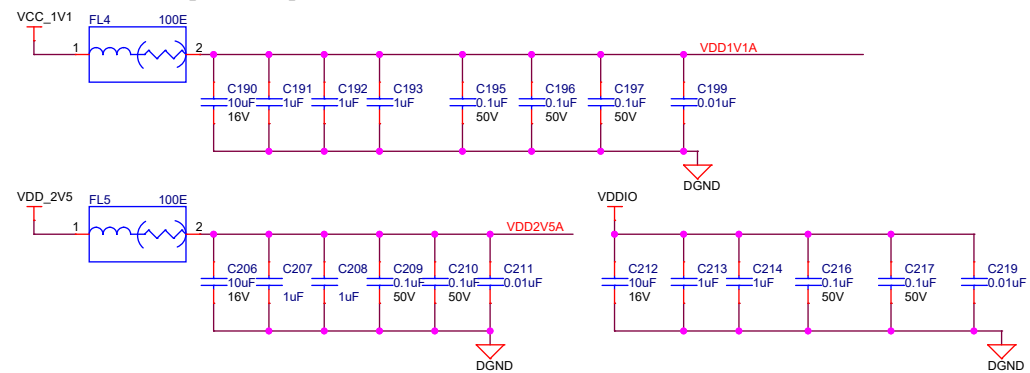
LED Driver MOSFETS



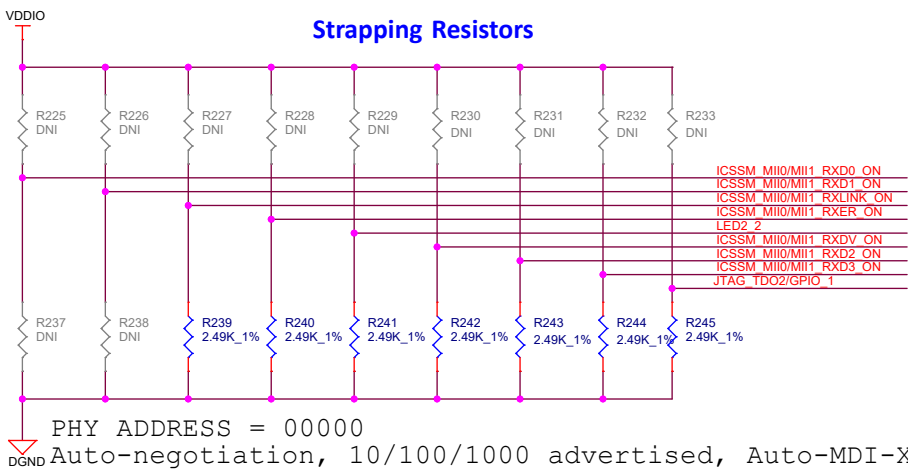
MDIO/MDC MUX FOR ON-BOARD PHY



Place Near power pins of 10/100/1000 Ethernet PHY



Strapping Resistors



PHY ADDRESS = 00000

Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X
RGMII to Copper (1000BaseT/100Base-TX/10Base-Te)

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Title SOC-ICSS DP8386(Indus)

Size
C Variant Name = PROC159E2(001)

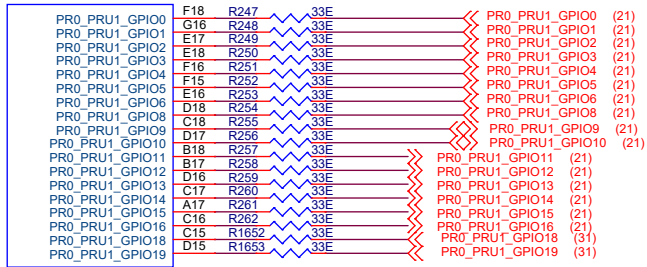
Date: Friday, September 22, 2023

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E2

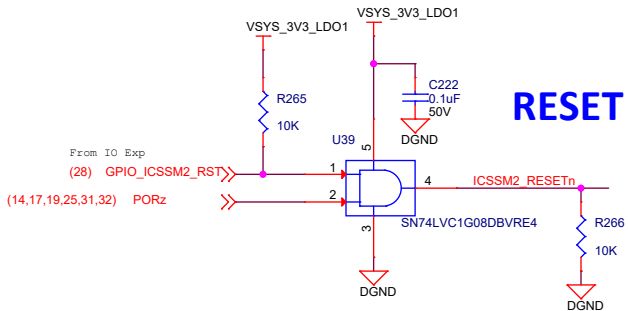
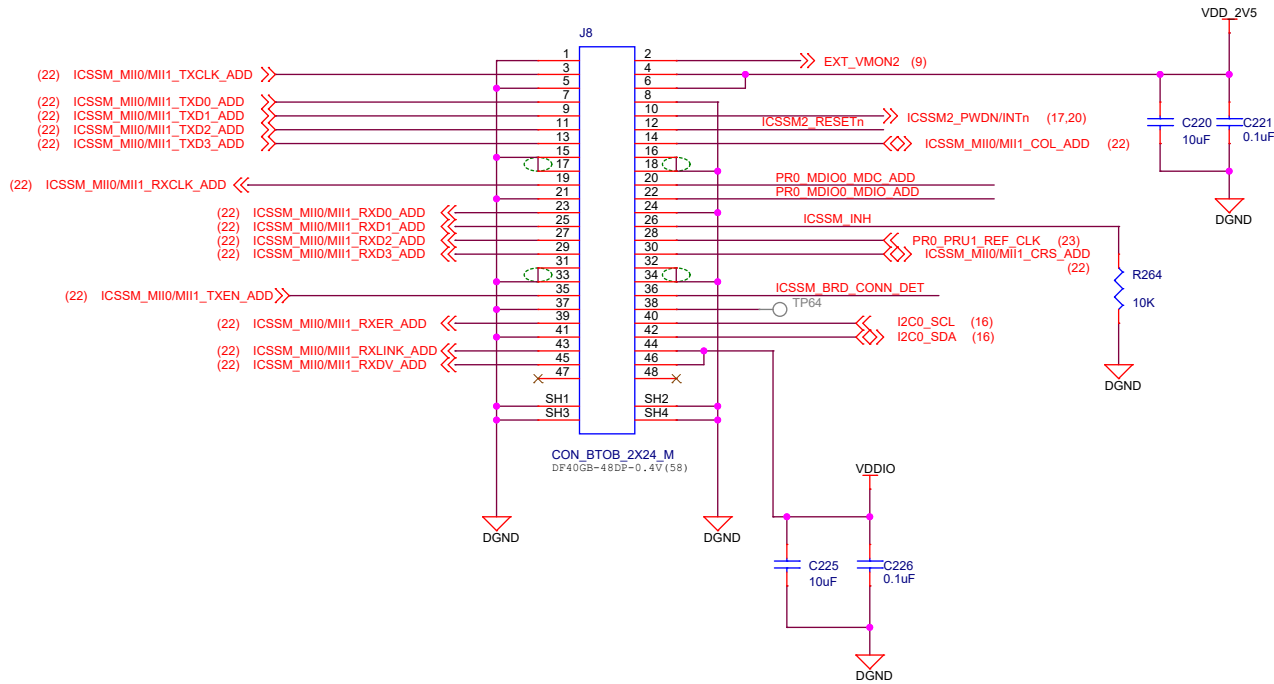
PRU1 ICSS MII1 Ethernet

U1H

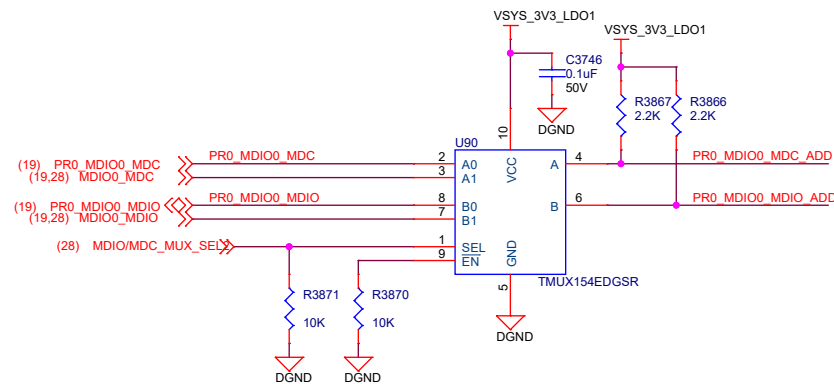


XAM263P4ASOKFZCZ

CAD NOTE: Place the resistors close to SoC with minimum stub



MDIO/MDC MUX FOR ADD-ON BOARD CONN



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Title SOC-ICSS ETHERNET CONN

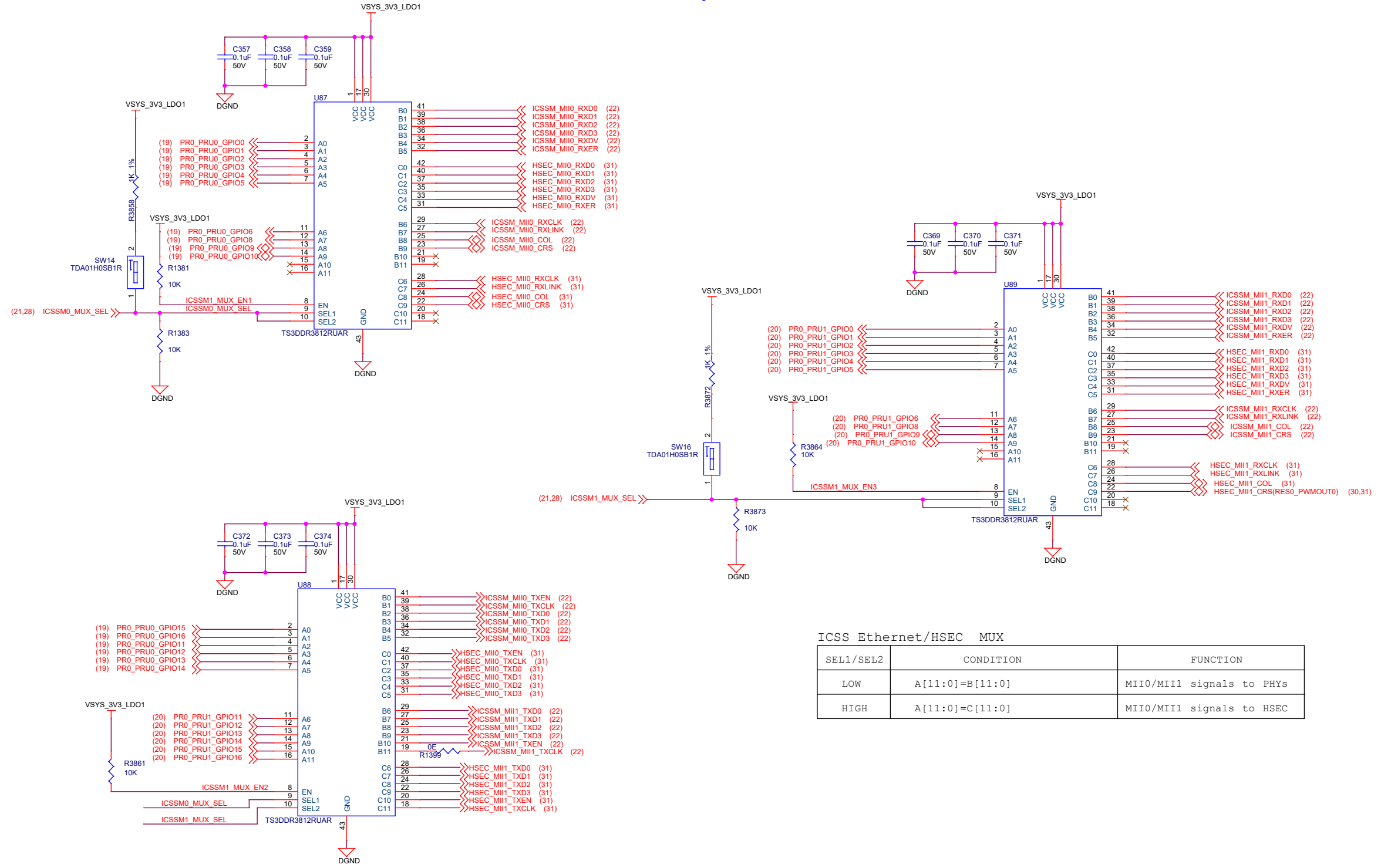
Size Variant Name = PROC159E2(001)

Date: Friday, September 22, 2023

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Rev E2

ICSS Ethernet/HSEC MUX



ICSS Ethernet/HSEC MUX

SEL1/SEL2	CONDITION	FUNCTION
LOW	A[11:0]=B[11:0]	MII0/MII1 signals to PHYs
HIGH	A[11:0]=C[11:0]	MII0/MII1 signals to HSEC

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Title ICSS ETHERNET /HSEC MUXES

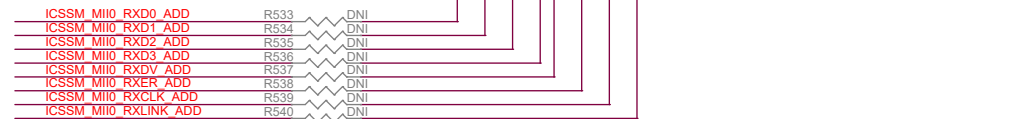
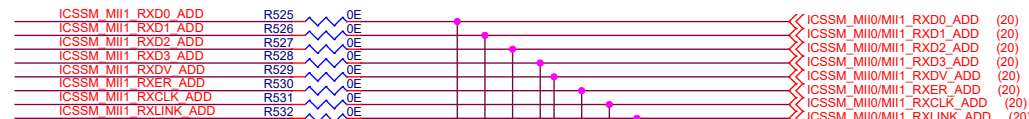
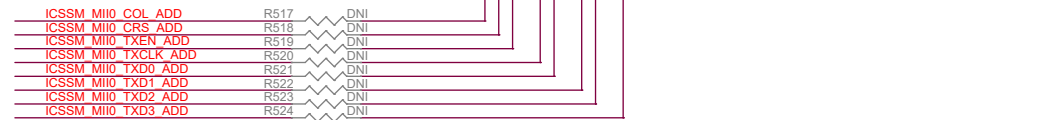
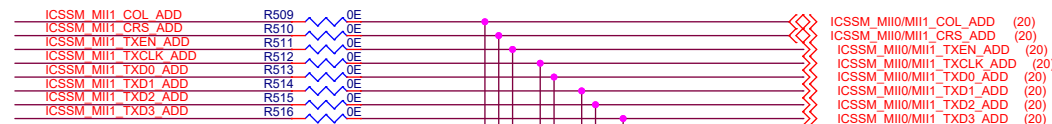
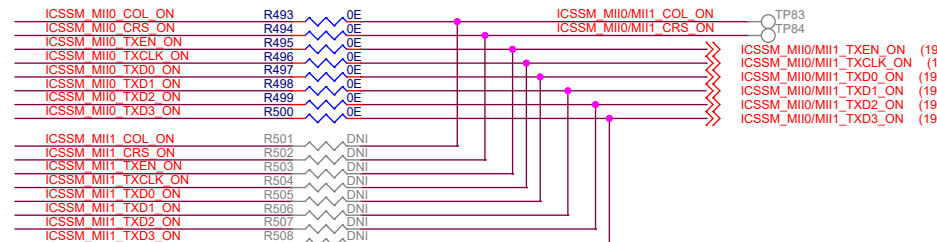
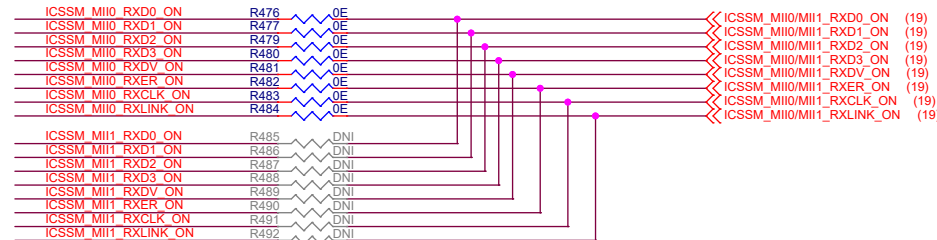
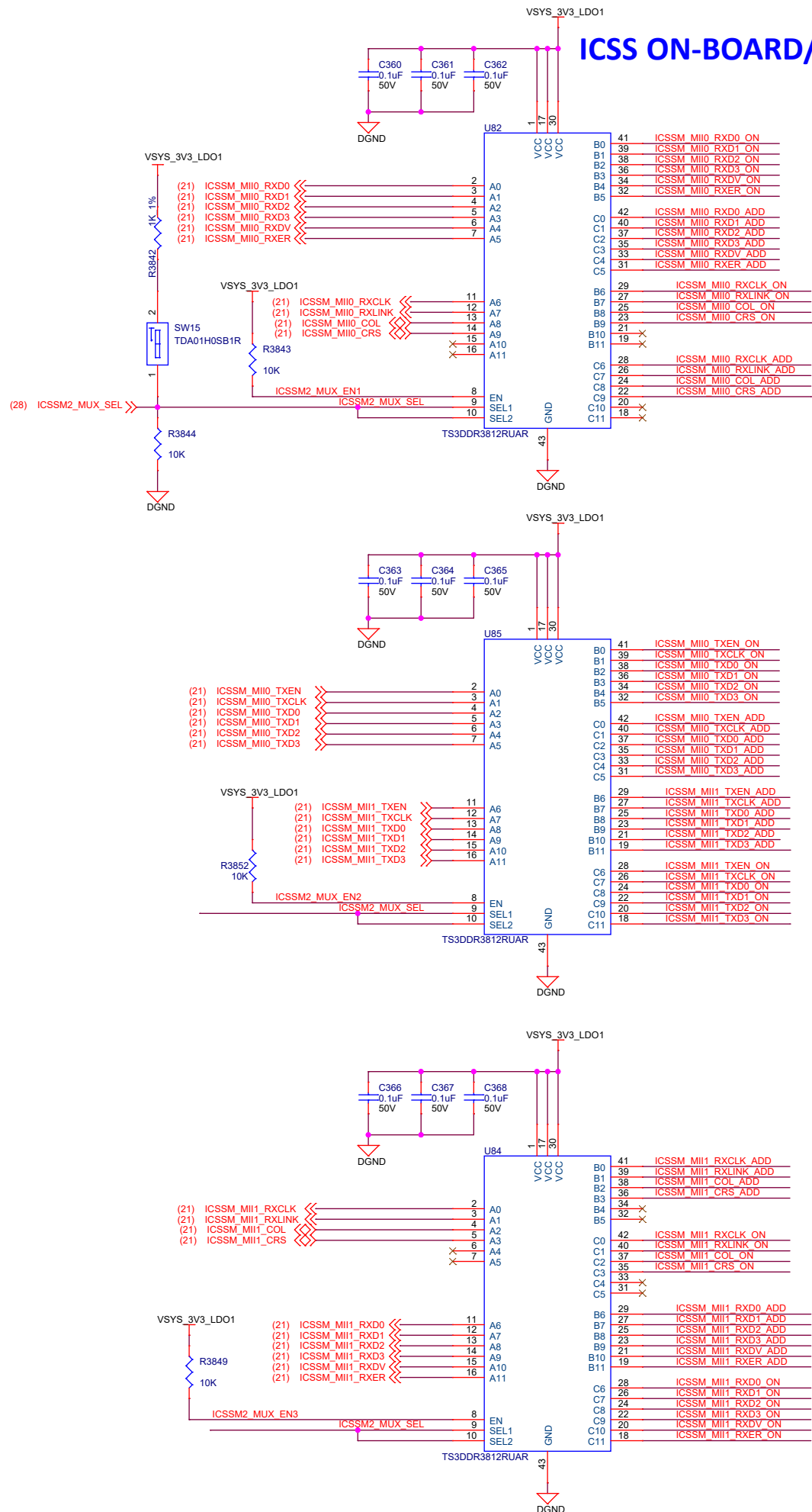
Size
C Variant Name = PROC159E2(001)

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ICSS ON-BOARD/ADD-ON PHY MUX

ICSS MII0/MII1 - RESISTOR MUX



CAD NOTE: Place the resistors with minimum stub

ICSS MII0/MII1 - RESISTOR MUX

MODE	FUNCTION
Populate R476 to R484, R493 to R500, R509 to R516, R525 to R532 resistors (Default)	MII0 -> On-board PHY MII1 -> Add-on Board connector
Populate R485 to R492, R501 to R508, R517 to R524, R533 to R540 resistors	MII0 -> Add-on Board connector MII1 -> On-board PHY

ICSS ON-BOARD/ADD-ON PHY MUX

SEL1/SEL2	CONDITION	FUNCTION
LOW	A[11:0]=B[11:0]	MII0 signals to ON-BOARD PHY MII1 signals to ADD-ON BOARD
HIGH	A[11:0]=C[11:0]	MII0 signals to ADD-ON BOARD MII1 signals to ON-BOARD PHY

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Title ICSS ON-BOARD/ADD-ON PHY & MII0/MII1 MUXES

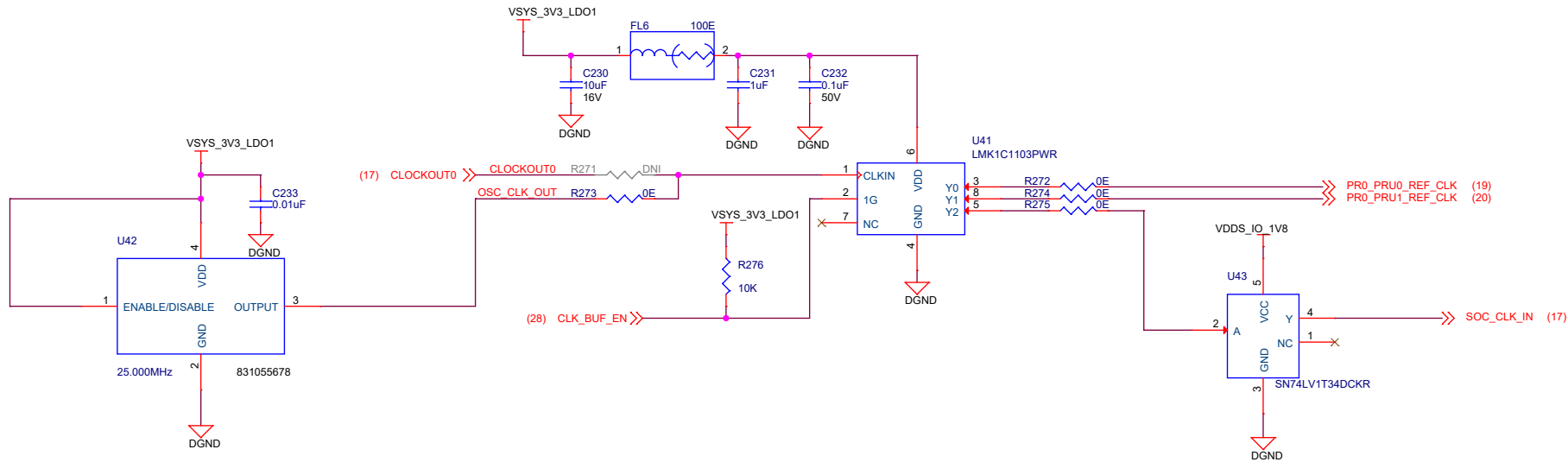
Size
C Variant Name = PROC159E2(001)

Rev
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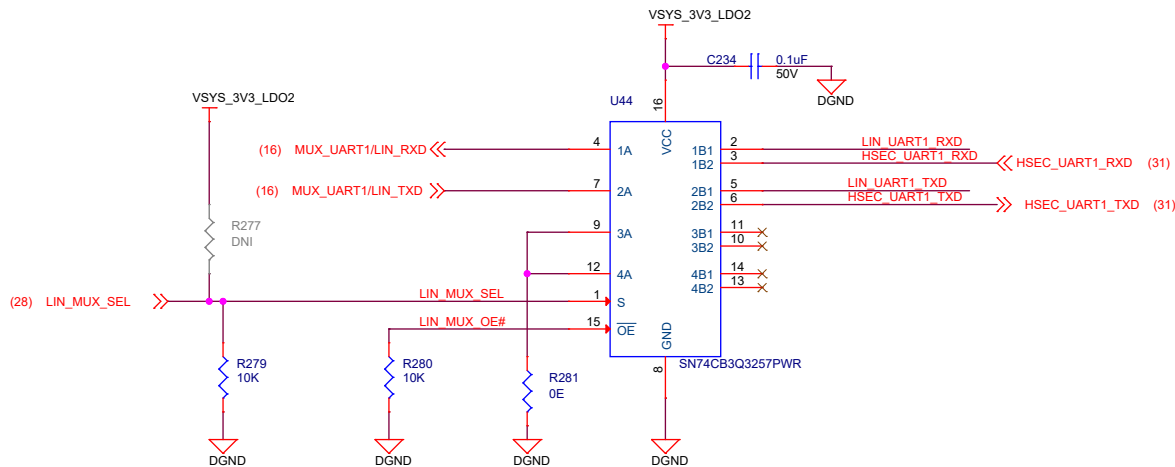
Date: Friday, September 22, 2023

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CLOCKS



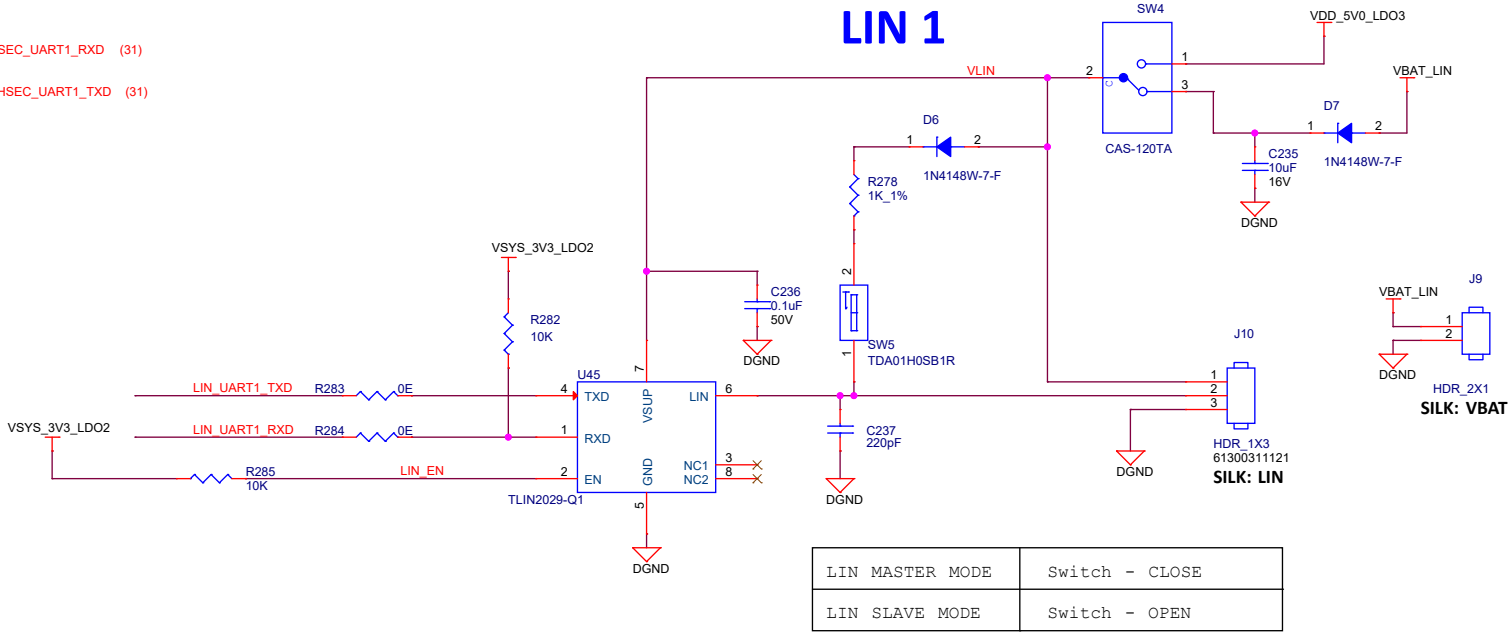
LIN MUX/DEMUX



I2C0 - 1:2 MUX

SEL	CONDITION	FUNCTION
LOW	LIN SELECTED	A-->B1 port
HIGH	HSEC UART selected	A-->B2 port

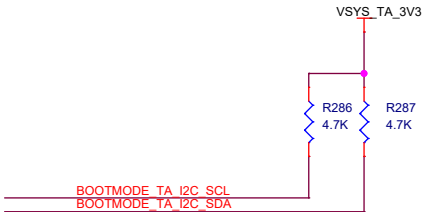
LIN 1



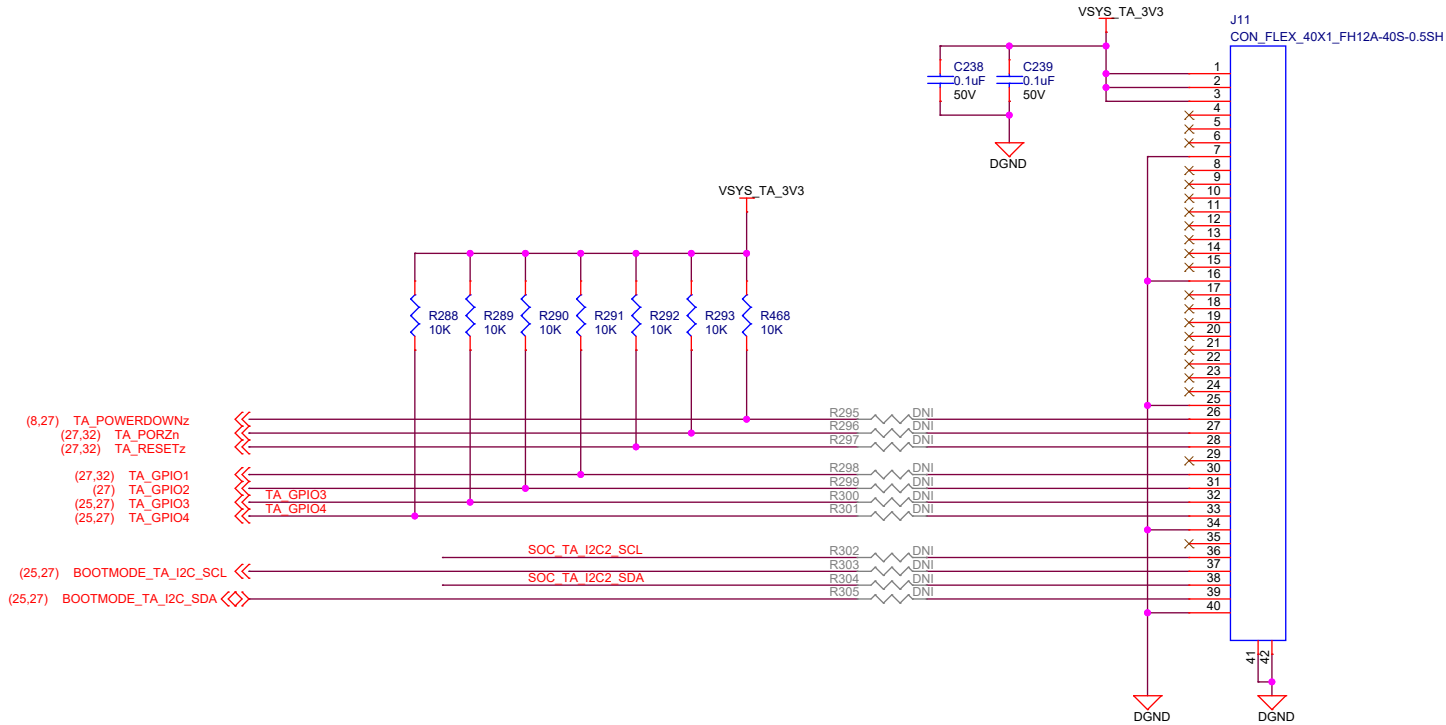
LIN MASTER MODE	Switch - CLOSE
LIN SLAVE MODE	Switch - OPEN

TEST AUTOMATION HEADER

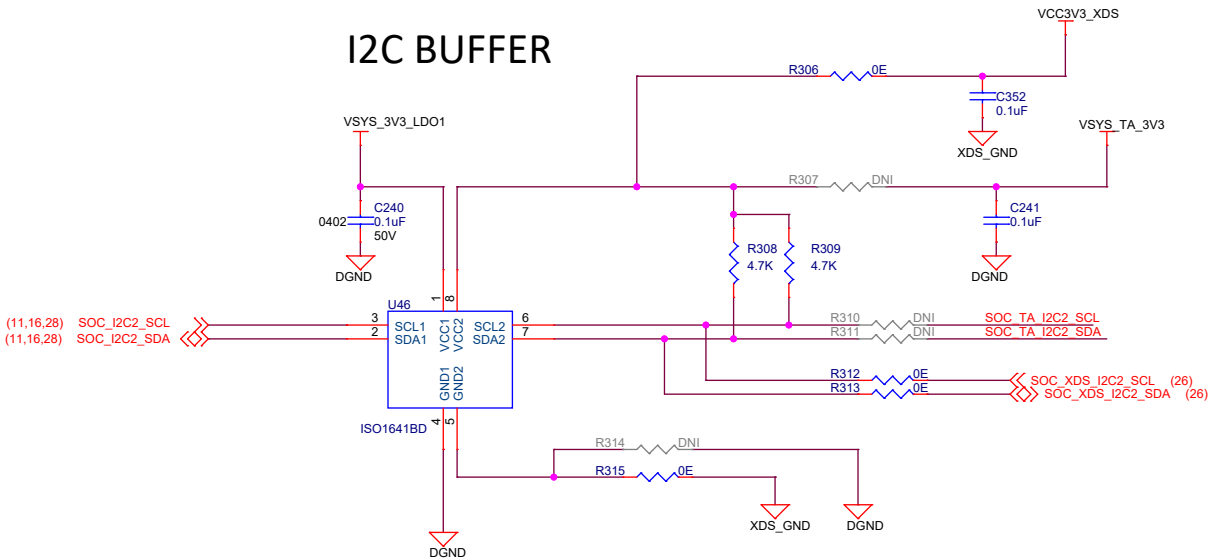
I2C Pull Ups



AUTOMATION INTERFACE
Cable : Parlex-050R40-76B, .5mm 3"



I2C BUFFER



TA Configuration
Mount : R307,R310,R311,R314
Demount : R306,R312,R313,R315

TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TA_RESEtZ	SoC Warmreset	OUTPUT	External Pullup
TA_GPIO1	Interrupt to SOC	OUTPUT	External Pullup
TA_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TA_GPIO4	Used Reset Bootmode IO Exp	OUTPUT	External Pullup

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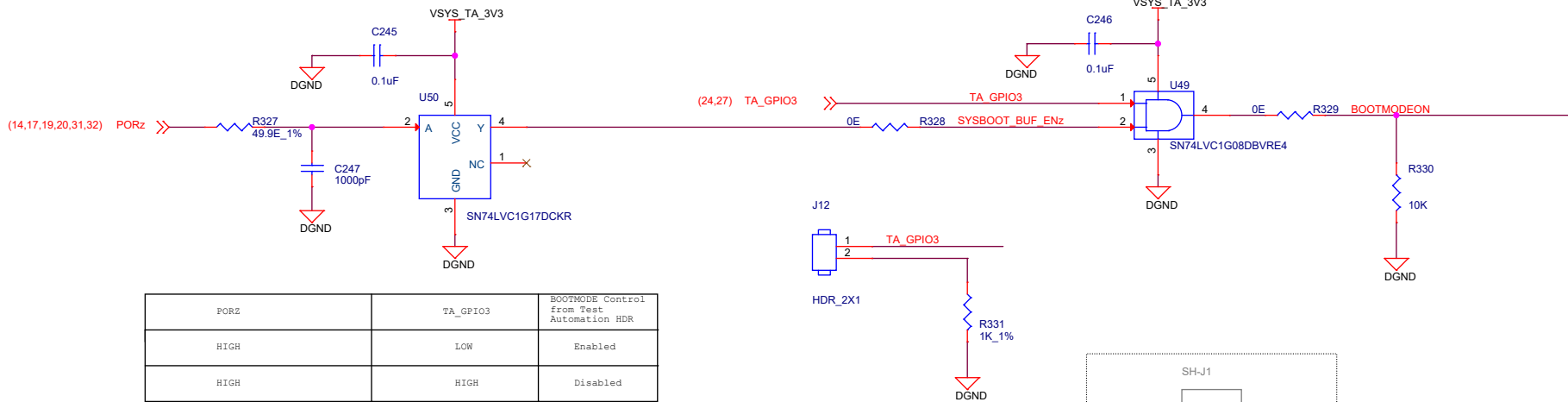
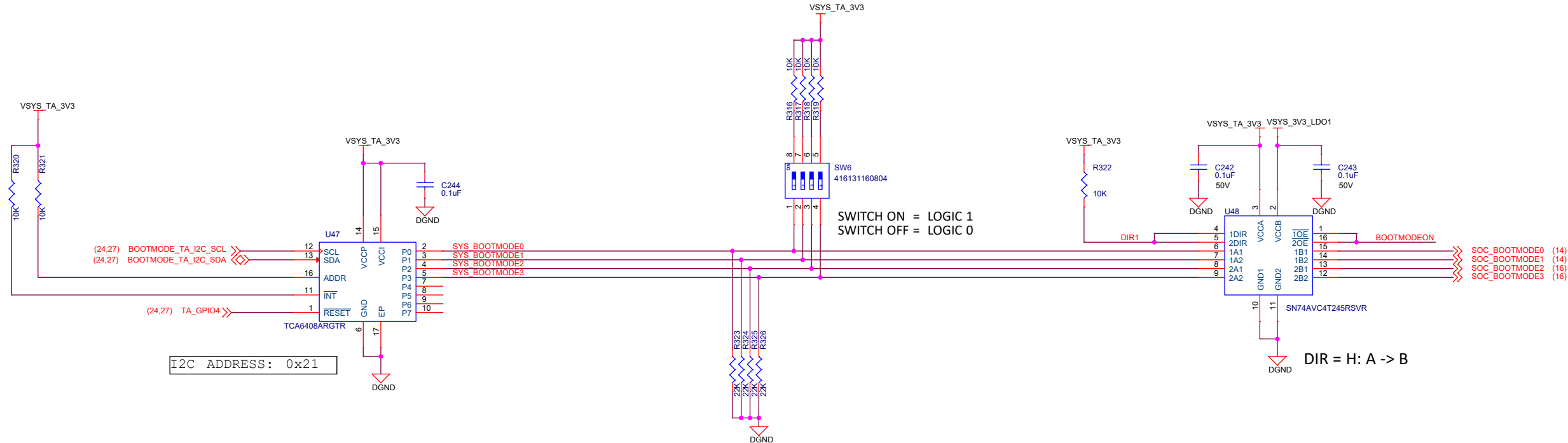
Title TEST AUTOMATION HEADER

Size
C Variant Name = PROC159E2(001)

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BOOTMODE BUFFER AND SWITCH



PORz	TA_GPIO3	BOOTMODE Control from Test Automation HDR
HIGH	LOW	Enabled
HIGH	HIGH	Disabled

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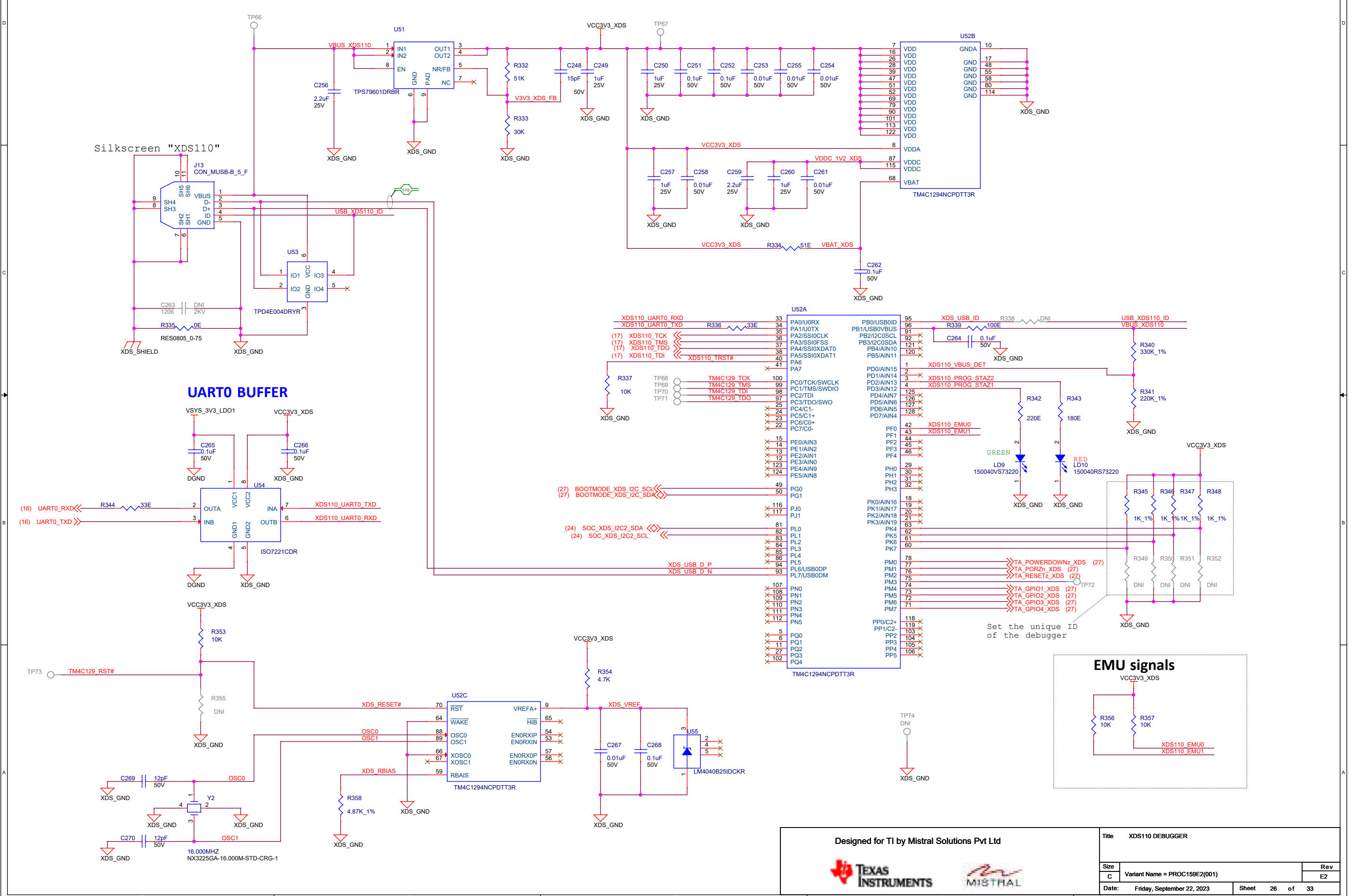
Title BOOTMODE BUFFER AND SWITCH

Size C Variant Name = PROC159E2(001)

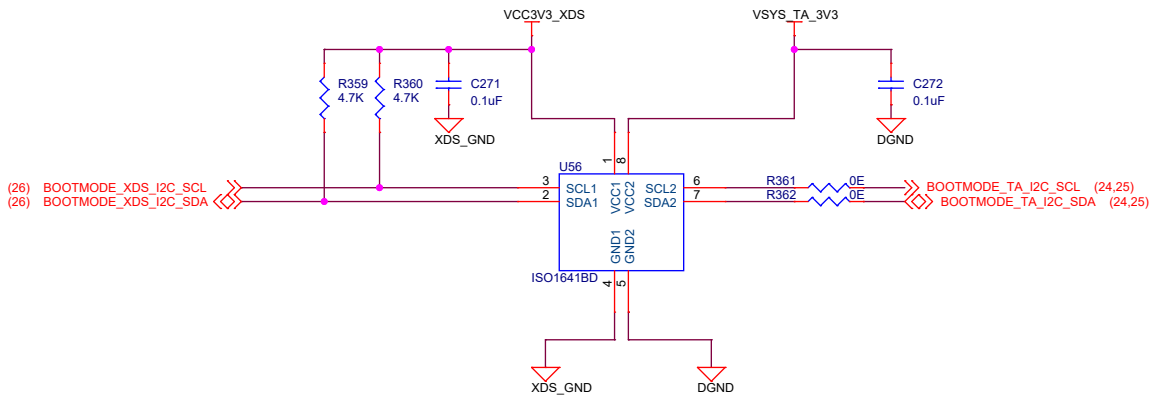
Rev E2

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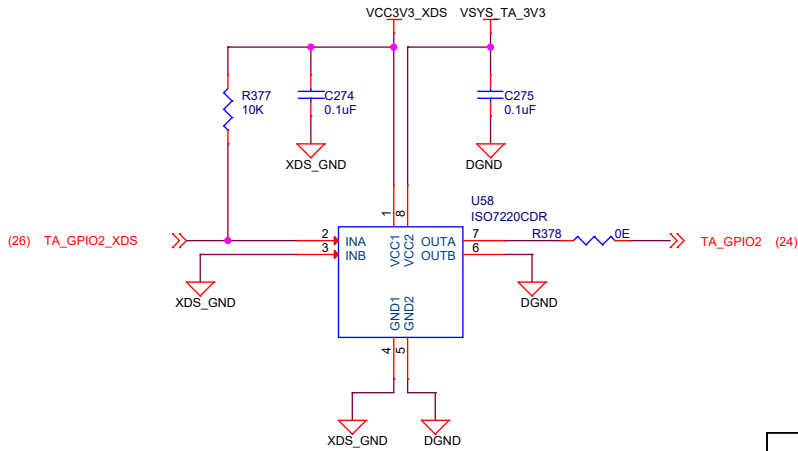
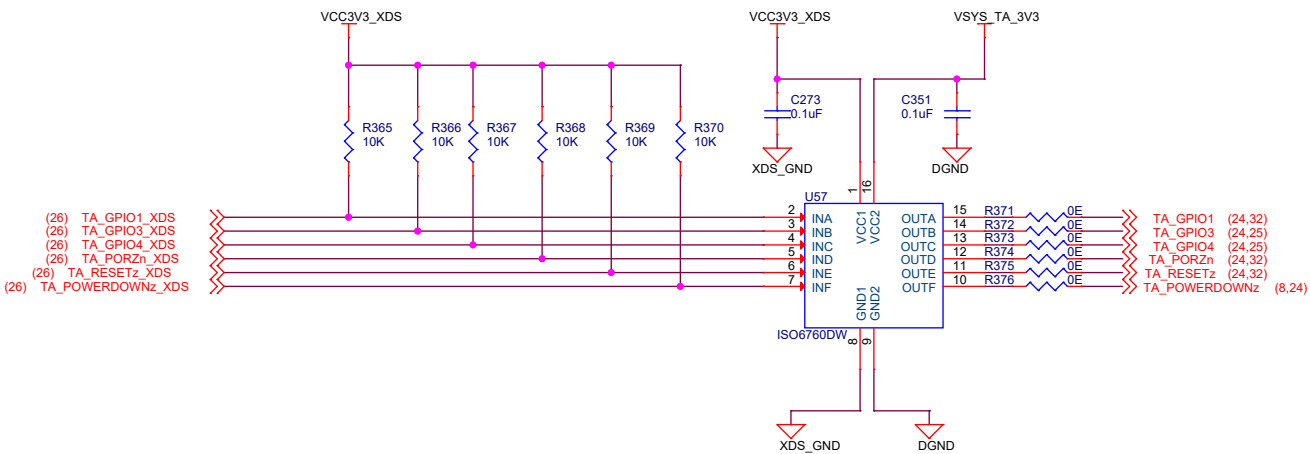
XDS110 DEBUGGER



BOOTMODE_I2C_TA BUFFER



ISOLATION BUFFERS FOR TA SIGNALS



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Title AUTOMATION SIGNALS BUFFER

Size Variant Name = PROC159E2(001)

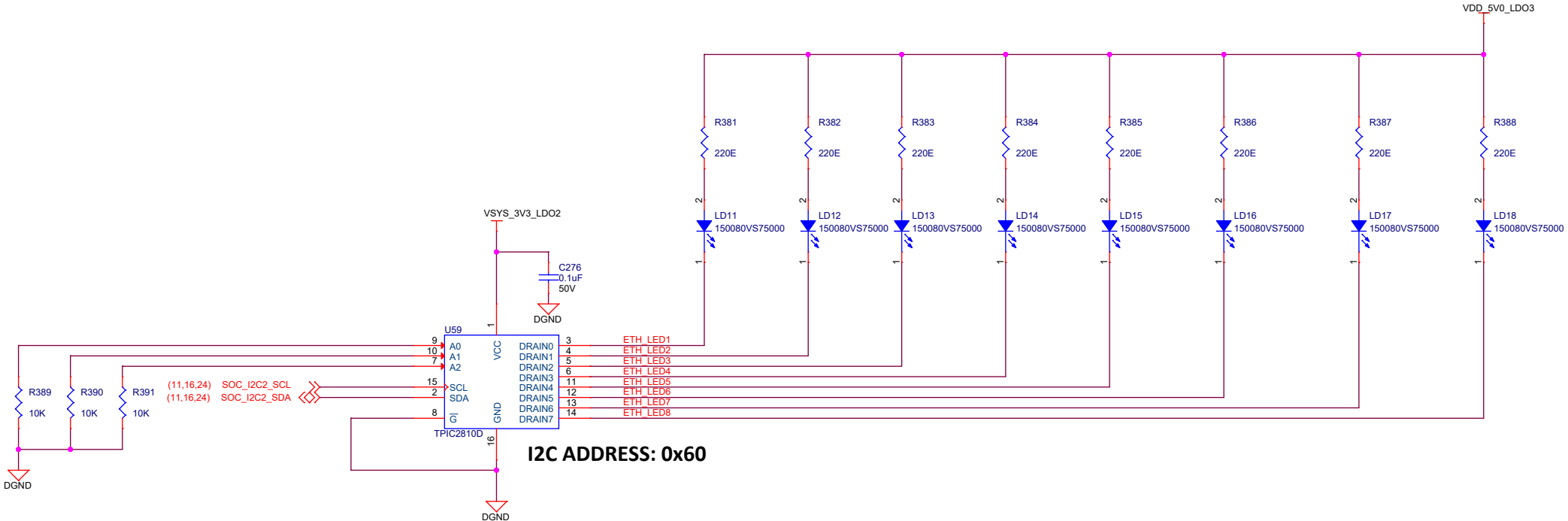
Rev

E2

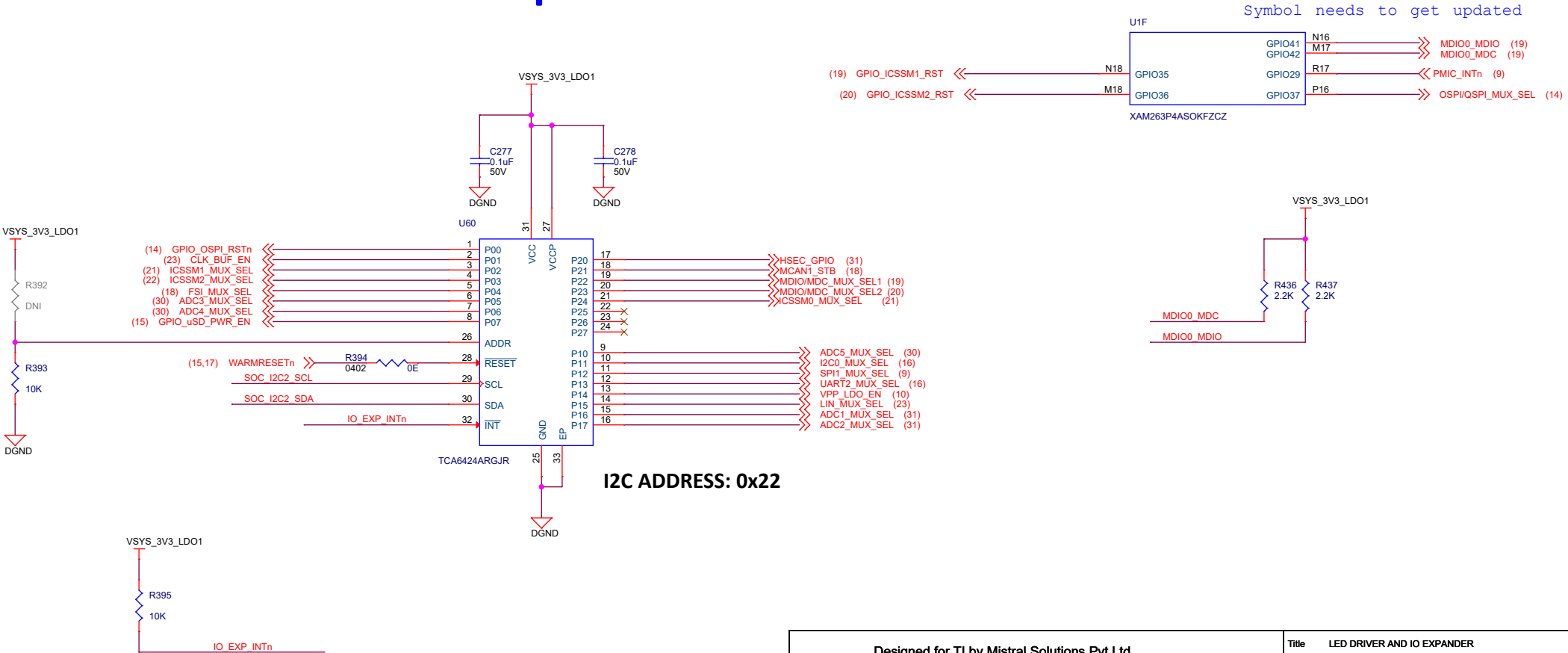
Date: Friday, September 22, 2023

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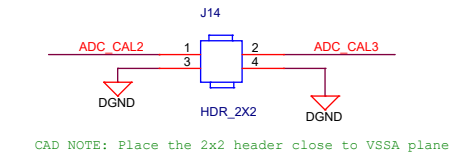
LED Driver



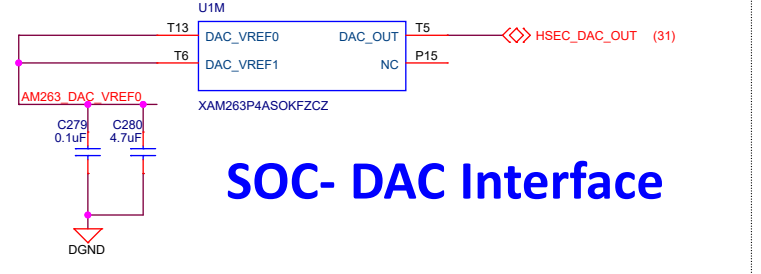
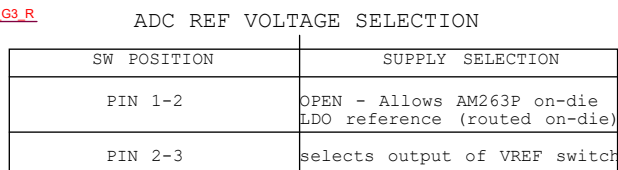
IO Expander



CAD NOTE: Place the ESDs close to connector



CAD NOTE: Place the CAPs close to the connector



VCC_1V8_LDO4

HSEC_ADC-VREFHI

ADC_DAC_REF

SW7

1

3

2

ADC_DAC-VREF

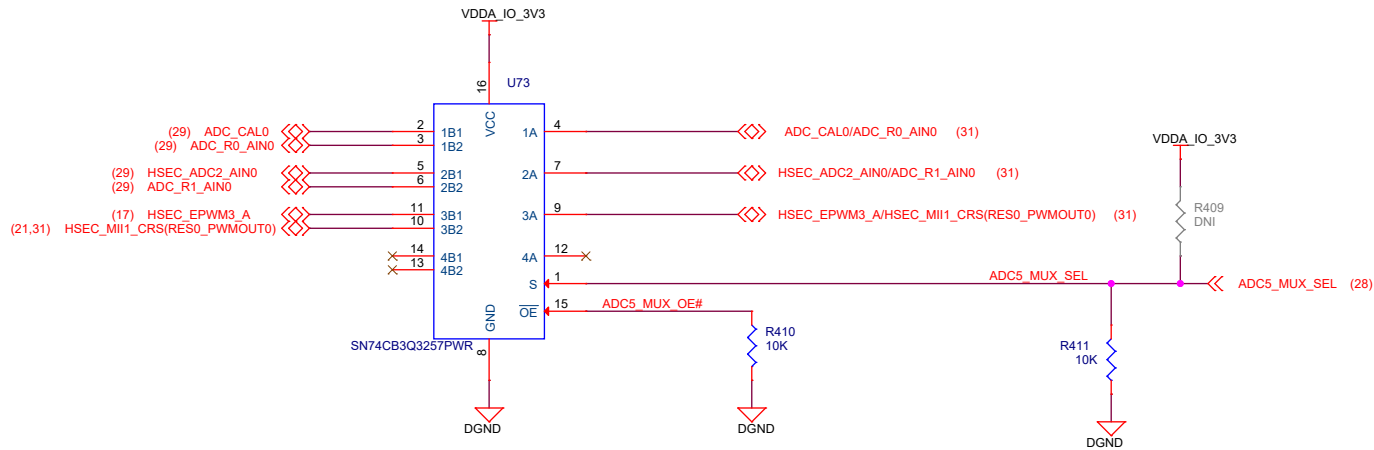
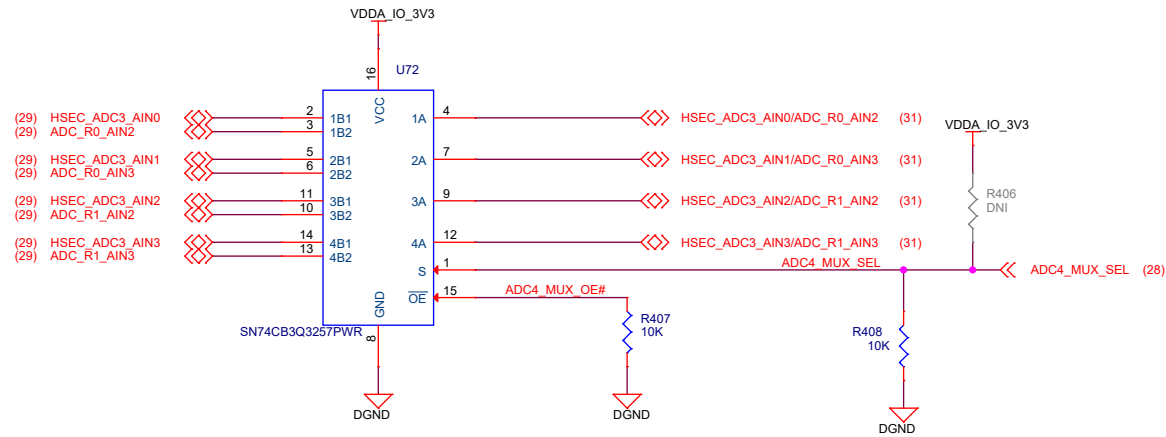
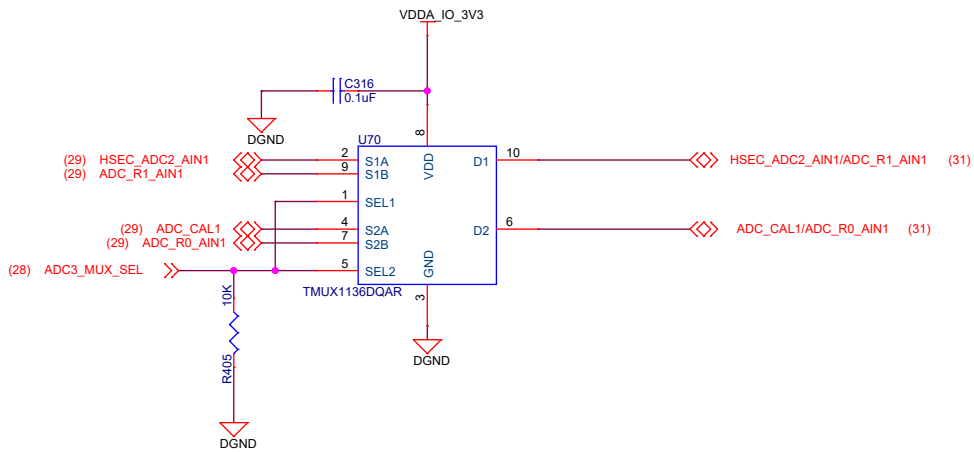
ADC_DAC-VREF (29)

CAS-120TA

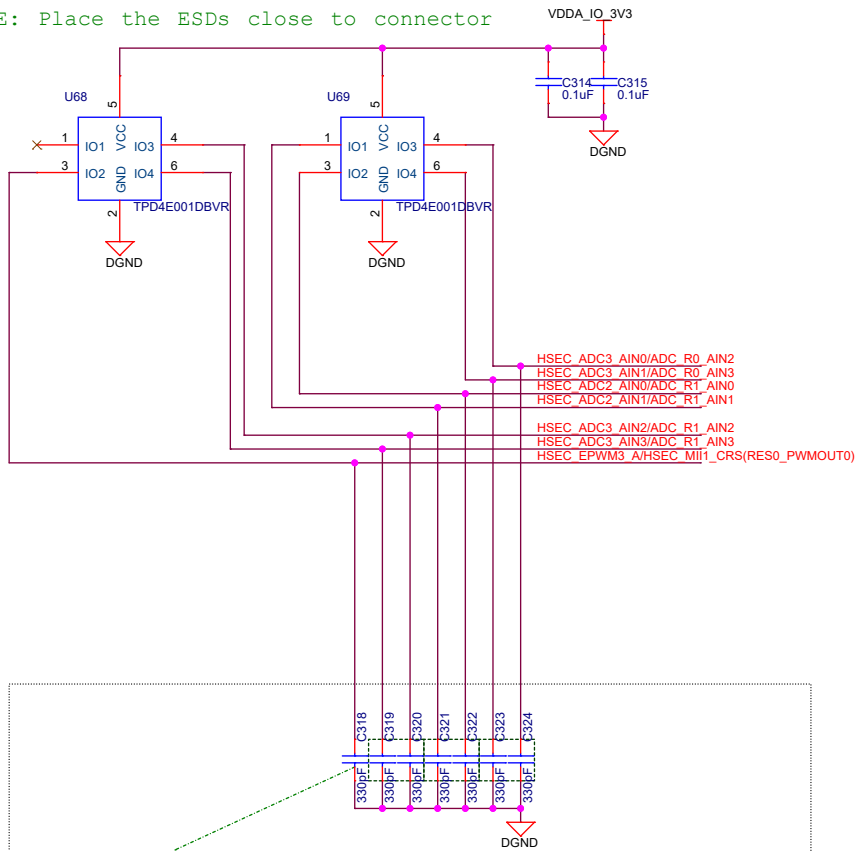
SILK "VREF"

SW POSITION	SUPPLY SELECTION
PIN 1-2	OPEN - Allows AM263P on-die LDO reference (routed on-die)
PIN 2-3	selects output of VREF switch
PIN 4-5	OPEN - Allows AM263P on-die LDO reference (routed on-die)
PIN 5-6	selects output of VREF switch

ADC MUXES



CAD NOTE: Place the ESDs close to connector



CAD NOTE: Place the CAPs close to each other

CAD NOTE: Place the CAPs close to connector

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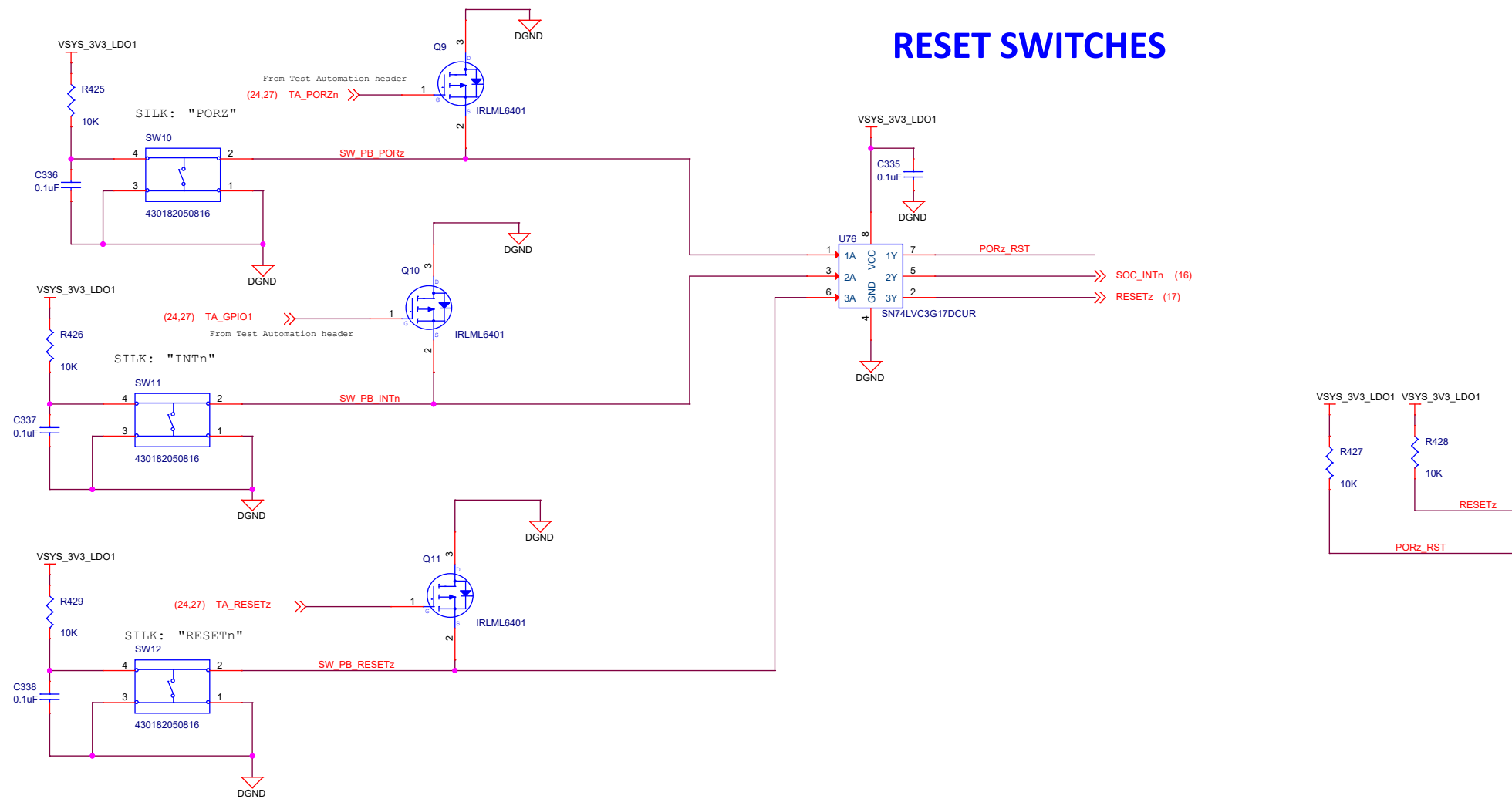
Title ADC MUXES

Size Variant Name = PROC159E2(001)

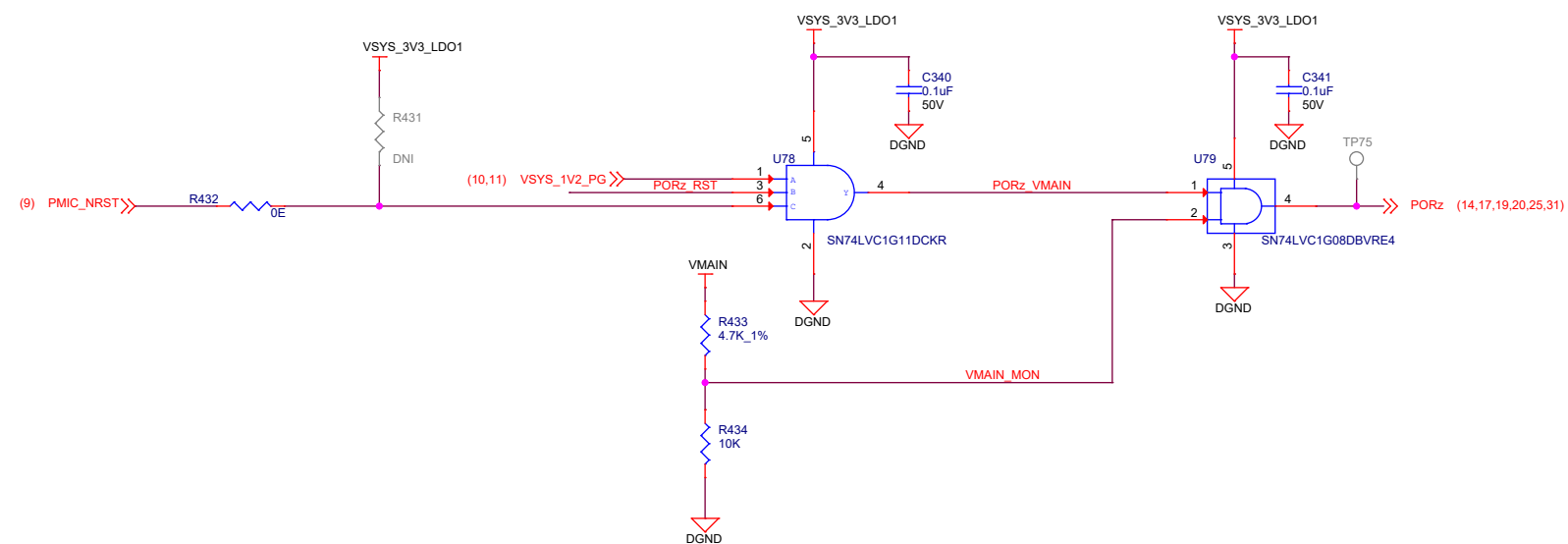
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Rev E2

RESET SWITCHES



PORz



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Title	RESET SWITCHES
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Size	Variant Name = PROC159E2(001)	Rev
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EVM Development & Evaluation test circuitry

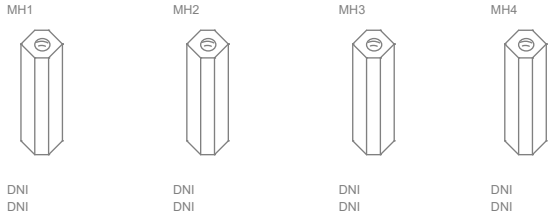
(TI EVM Only)

NOTES, HW & LABELS

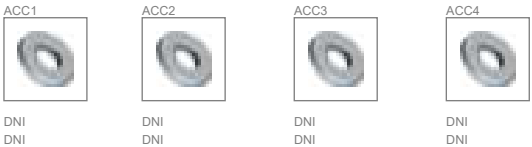
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

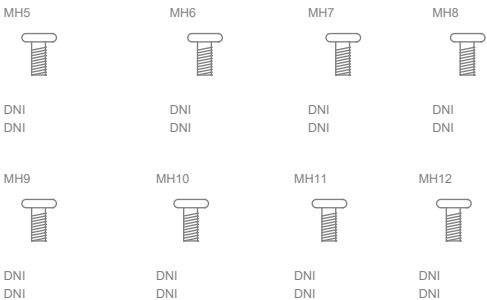
STANDOFFS



WASHER's



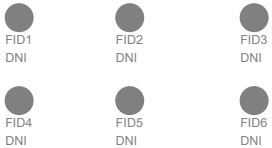
SCREWS



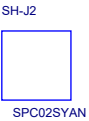
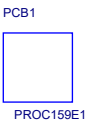
RUBBER FEET



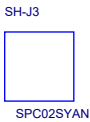
FIDUCIALS



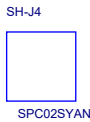
BARE PCB



SH-J2 Shall be mounted on J20 to enable the PMIC VIA WAKE1 PIN OF PMIC



SH-J3 Shall be mounted on J22 to enable the PMIC VIA WAKE2 PIN OF PMIC



SH-J4 Shall be mounted on J21 to enable the TCAN WAKE

LABELS

Board Serial No.



Assembly Revision.



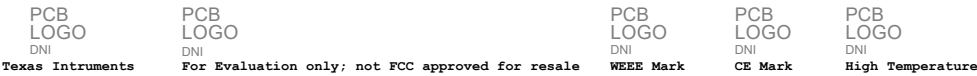
EVM Orderable No.



Orderable Part Numbers

Variant	Label Text
001	TMDSCNCD263P

LOGOs



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Title CC EVM NOTES,HW &LABELS

Size Variant Name = PROC159E2(001)

Date: Tuesday, October 03, 2023

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Rev E2