

J722S/AM67x/TDA4VEN/TDA4AEN Evaluation Module

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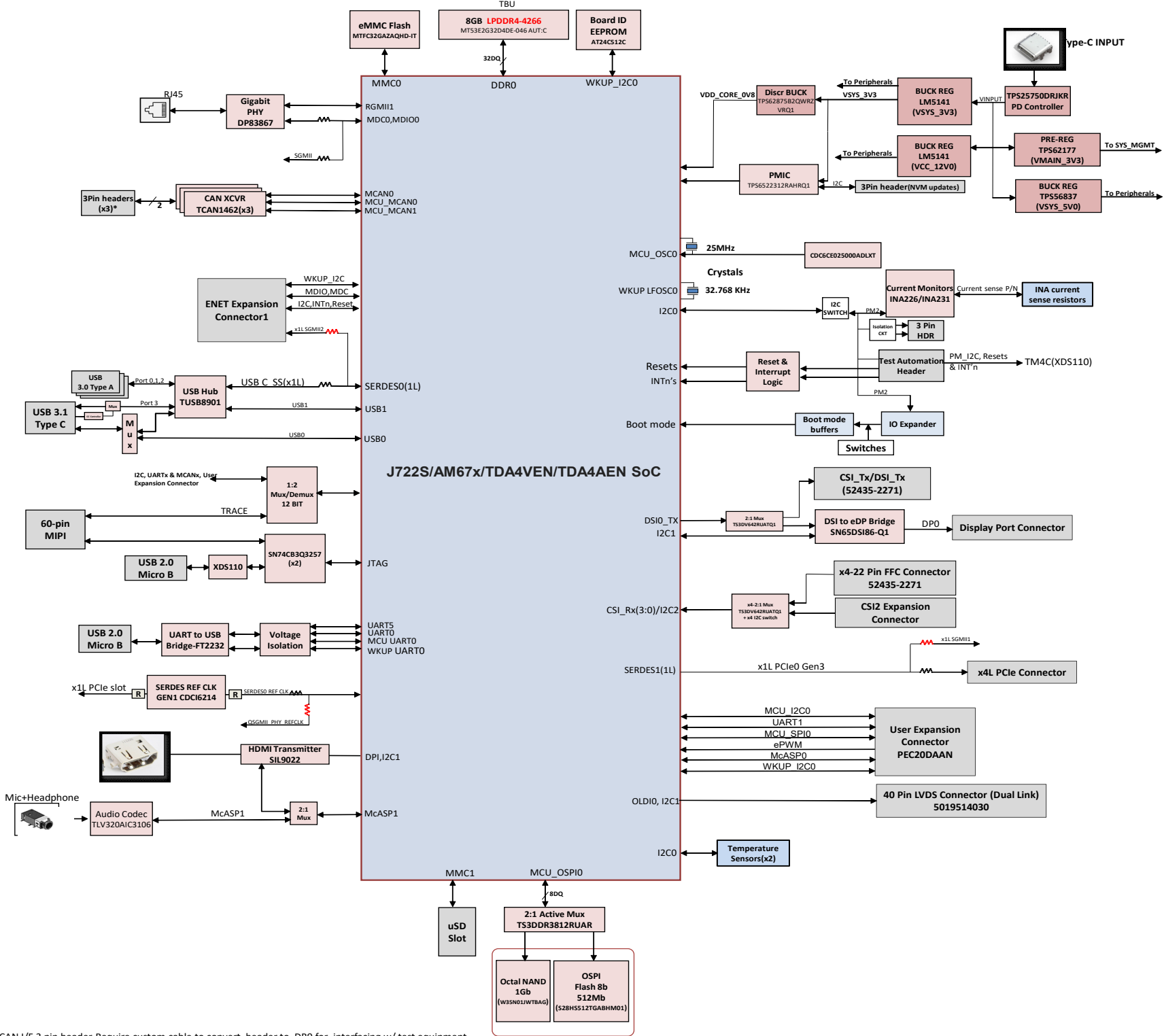
REVISION HISTORY #1

	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	0.1	14 JUN 2023	Draft schematic	Mistral Design Team		
	0.2	26 JUN 2023	V0.11 Breakout schematic imported to core evm schematic			
	0.3	06 JULY 2023	Review comments updated			
	0.4	19 JULY 2023	Updated schematic to breakout V0.14			
	0.5	04 AUG 2023	Updated schematic to PDN 7G v0.16			
	0.6	05 SEPT 2023	Review comments updated			
	0.7	11 SEPT 2023	Board released to Fab	Mistral Design Team	TI	TI
	0.8	06 OCT 2023	Since LM61480Q5RPHRQ1 IC gives a default 5V0 output and does not need a resistor divider feedback. So,R443 is DNI'd and R448 is replaced with 0E. Feedback to VDD_RAM_0V85 supply is after the ferrite bead. There seems to be more noise in feedback. FL17 is replaced with 0E. Seeing 1.8V @ EN_TPS62177_ON signal which will enable the device even with jumper on J30. Replaced R775 with 0E in order to avoid voltage divide. Change in the compensation network values of 12V0 circuit. R438 is replaced with 10Kohm. To get default 100MHz clk from U10 LMK device, the enable should be either floating or pulled down. R58 is DNI'd to get default output. In order to source the 19.2MHz clock to DSI to eDP bridge external oscillator path is enabled by populating R410 and R412 DNI'd. Change in compensation values of 3V3 generation circuit to avoid initial power up issue. C241: 390pf, R385:7.5k, C240:3300pf I2C address text updated for U88 IO expander	Mistral Design Team	TI	TI
E2	0.9	15 Nov 2023	Replaced Compensation network for 12V0 and 3V3 values with new values suggested by TI Feedback VDDR supply is given before the FB Fix for TRACE DATA 13 U190 and U12 mux replaced with the mux which do not have internal pull down.			
	1.0	13 Dec 2023	LMK3H0102 devices are replaced with x2 NVM programmed parts. Resistor mount option changed for PCIe clock default to internal clock. Added support for RADAR(R-option or Mux for SPI on Expansion header) Added R-Option to connect MCU_OBSCLK and OBSCLK to test point.	Mistral Design Team	TI	TI
E3	1.1	11 JAN 2024	Added a open drain buffer to RGMII_INT# Signal Added 49.9E pull down resistors to SERDES REFCLK outputs. Pin VDD_MMC0 (W10) is connected to VDD_RAM_0v85 (non-filtered)			
	1.2	24 JAN 2024	Added 4x PMIC Resource Selection (RS[3:0]) bits to use diff PMIC power & GPIO resources and 5x 0E Rs to use diff interface signals on PMIC GPIO1,2 & 4 for supporting diff J722S/TDA4AEN/VEN PDN Schemes Updated RS[3:0] notes & fixed GPIO R-Muxes inadvertent REF DES changes back to existing R85 & R82 to enable net list generation. Changed power nets connected to VDD_MMC0 (BGA-W10) and input to PHY analog filters (FL23, 24 & 26) from VDD_RAM_0V85 to VDD_0V85 (new name) that is the output of 2:1 R-Mux which selects either VDD_RAM_0V85 or VDD_CORE as source for fixed 0.85V inputs per SoC operation & PDN diagrams. Changed following power net names to align with desired operation & PDN diagrams: From: VDD_IORET_0V75_xxx To: VDD_IORET_CORE_xxx TPS65224_EN PMIC_EN Added new 2:1 R-Mux (R6115 & R6114) to use VSYS_CAN_5V0 as input voltage to SD Card LDO (U191). This will remove the delayed ramp of VDD_SD_DV' (LDO's Vo)) due to slow turn-on & ramp of VSYS_5V0.	Mistral Design Team	TI	TI
	1.3	02 FEB 2024	U57.4 Net name changed from USBC_PWR_EN to USBC_PWR_OUT_EN	Mistral Design Team	TI	TI
E3A	1.4	05 APR 2024	DNI'd R603 - Pull down resistor for DDR0_ODT_CA_A signal DNI'd R604 - Pull down resistor for DDR0_ODT_CA_B signal DNI'd R332 in 001 variant - Pull up resistor for MCU_ONAND_D7 signal	Mistral Design Team	TI	TI
E3B	1.5	30 AUG 2024	PMIC Part no changed from TPS6522311-Q1 to TPS6522312-Q1 DNI'd R82 - TRIG_WDOG Signal	Mistral Design Team	TI	TI
	1.6	11 SEP 2024	Fix for the VCC voltage issue in the U190 and U12 IC's Replaced the SoC(U48) in 001 variant with the GP SoC part#XJ722SGAAMW	Mistral Design Team	TI	TI
	1.6	07 APR 2025 14 APR 2025	DNI'd - R207 Resistor Added "SCH Note" to SOC HCPS buck loop compensation components (SCH pg27).	Mistral Design Team	TI	TI

REVISION HISTORY #2

BLOCK DIAGRAM

J722S/AM67x/TDA4VEN/TDA4AEN Evaluation Module

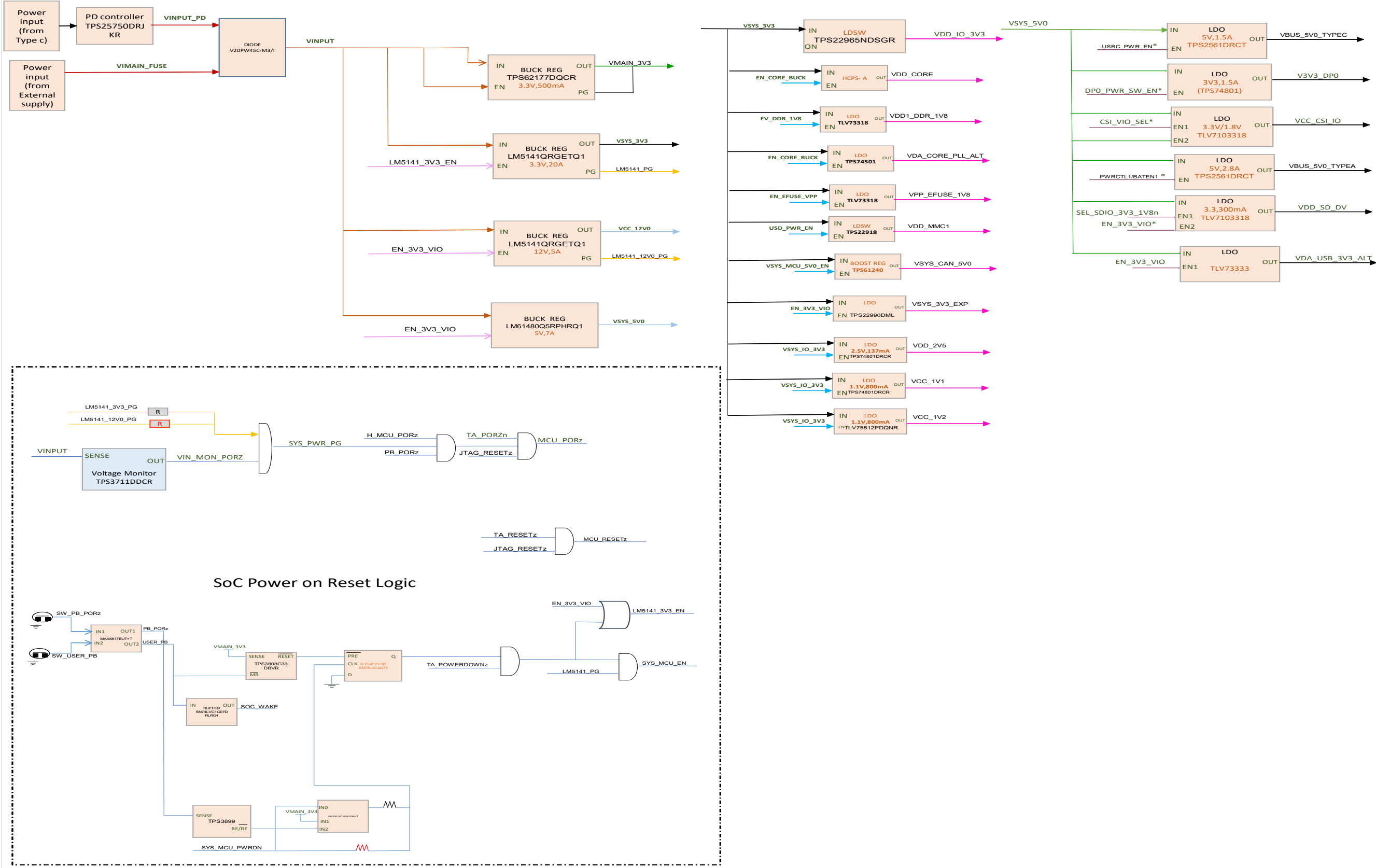


*CAN I/F 3 pin header-Require custom cable to convert header to DB9 for interfacing w/ test equipment.




POWER SEQUENCE

J722S TDA4VEN TDA4AEN AM67 Board Power Sequencing

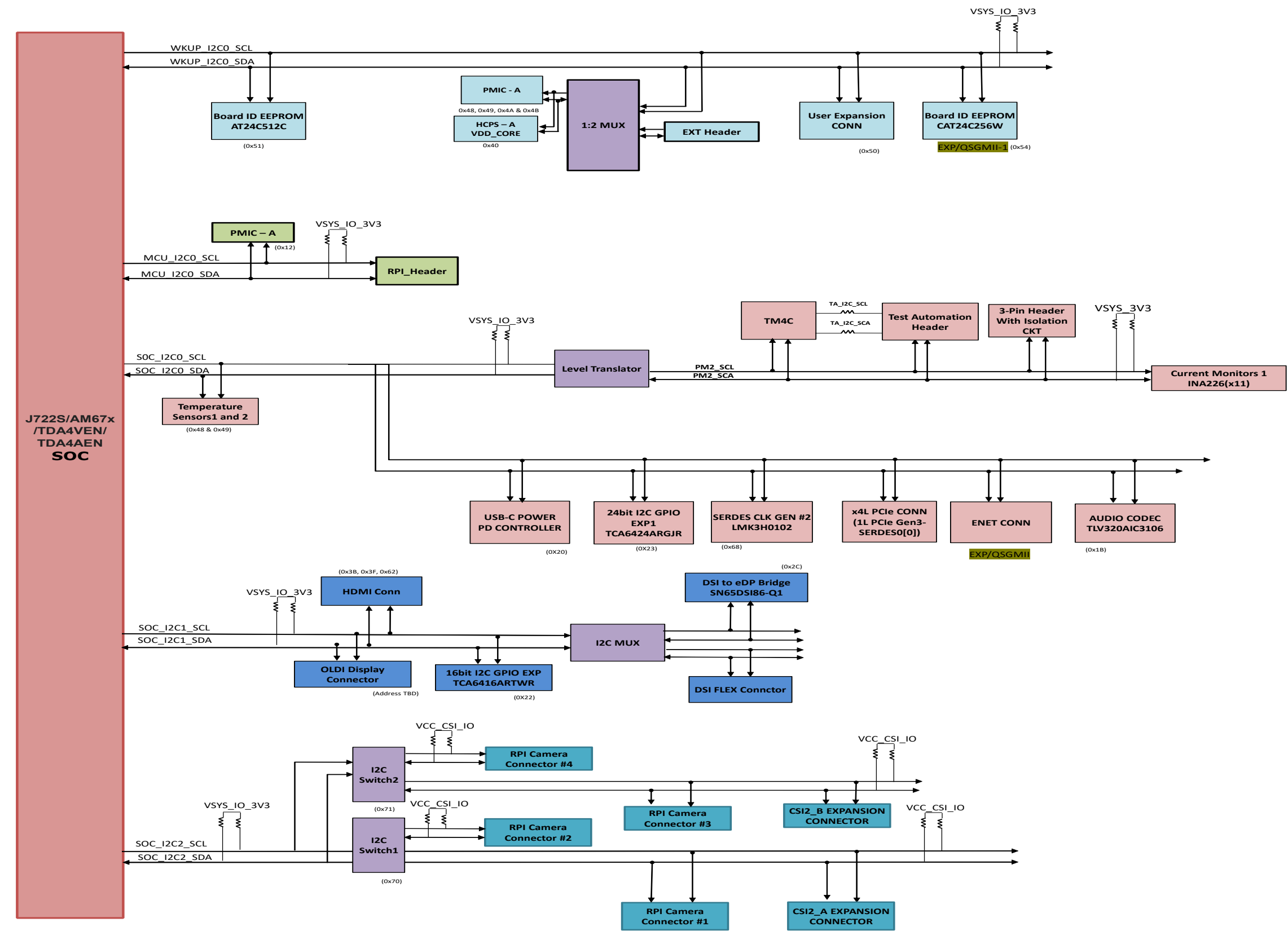


PDN

Please see the PDN file "J722S EVM Single PMIC and HCPS PDN-7D.DES v0.29 pdf" which is included in the released design file

Project : J7 EVM				Title PDN	
				Size C	Rev E3B
				Date: Friday, August 30, 2024	Sheet 7 of 68

I2C TREE



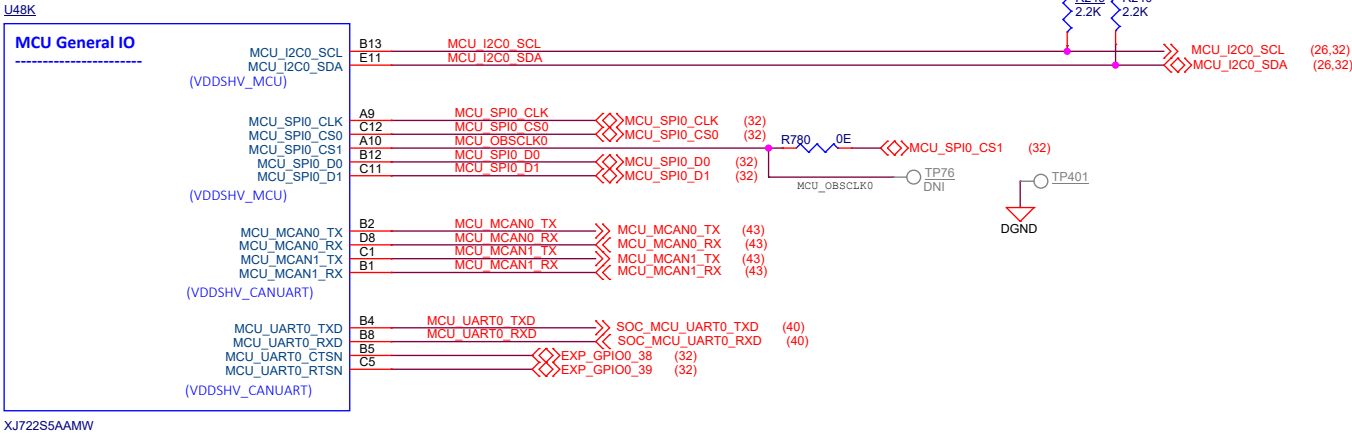
I2C TABLE

BOARD	DEVICE DESCRIPTION	PART#	ADDRESS	J722S TDA4VEN TDA4AEN AM67 PORT MAPPING
EVM	Board ID EEPROM	AT24C512C-MAHM-T	0X51	WKUP_I2C0
EXP/QSGMII -1	Board ID EEPROM	CAT24C256WI-GT3	0X54	
EXPANSION	User Expansion Connector	<connector interface>	0X50	
EVM	VDD_CORE REGULATOR	TPS62875	0X44	
EVM	PMIC	TPS65221-Q1	0x48,0x49, 0x4A, 0x4B	
EXPANSION	User Expansion Connector	<connector interface>		MCU_I2C0
EVM	PMIC	TPS65221-Q1	NA	
EXP/QSGMII -1	ENET	<connector interface>		SOC_I2C0
EVM	IO Expander 1	TCA6424ARGJR	0X23	
EVM	Temperature Sensors	TMP100NA/3K	0X48,0X49	
EVM	AUDIO CODEC	TLV320AIC3106IRGZT	0X1B	
EVM	Test automation	FH12A-40S		
EVM	x1LANE PCIe0	<connector interface>		
EVM	USB C PD Controller	TPS25750D	0X20	
EVM	INA226 device for VDD_CORE	INA226AIDGSR	0X40	
EVM	INA226 device for VDD_RAM_0V85	INA226AIDGSR	0X41	
EVM	INA226 device for VDA_PHY_1V8	INA226AIDGSR	0X42	
EVM	INA226 device for VDD_IOPRET_CORE	INA226AIDGSR	0X43	
EVM	INA226 device for VDD_SD_DV	INA226AIDGSR	0X44	
EVM	INA226 device for VDD_IO_1V8	INA226AIDGSR	0X45	
EVM	INA226 device for VSYS_3V3	INA226AIDGSR	0X46	
EVM	INA226 device for VDD_DDR_1V1	INA226AIDGSR	0X47	
EVM	INA226 device for VDD_IO_3V3	INA226AIDGSR	0X4C	
EVM	INA226 device for VDA_PLL_1V8	INA226AIDGSR	0X4D	
	INA226 device for VDD1_DDR_1V8	INA226AIDGSR	0X4E	
EVM	CLKGEN 2	LMK3H0102	0x68	
EVM	Bootmode Buffer	TCA6424ARGJR	0x22	TA_I2C_SCL
EVM	IO Expander	TCA6416ARTWR	0X20	SOC_I2C1
EVM	HDMI	SiI9022ACNU	0x3B, 0x3F, 0x62	
EVM	DSI Flex Connector	<connector interface>(Via Mux)		
EVM	DSI to eDP Bridge	SN65DSI86IPAPQ1(Via Mux)	0X2C	
EVM	OLDI	<connector interface>		
EVM	I2C switch	TCA9543APWR	0X70,0X71	SOC_I2C2(Via Mux)
EVM	CSI2_A Expansion Connector	QSH-020-01-L-D-DP-A-K(J1002)	From 0x70 Switch	CSIO_I2C2_SDA
EVM	FPC Camera Connector 1	CON_FLEX_22X1_52435(J1004)		CSI1_I2C2_SDA
EVM	FPC Camera Connector 2	CON_FLEX_22X1_52435(J1005)		
EVM	CSI2_B Expansion Connector	QSH-020-01-L-D-DP-A-K(J1003)	From 0x71 Switch	CSI2_I2C2_SDA
EVM	FPC Camera Connector 3	CON_FLEX_22X1_52435(J1006)		CSI3_I2C2_SDA
EVM	FPC Camera Connector 4	CON_FLEX_22X1_52435(J1007)		

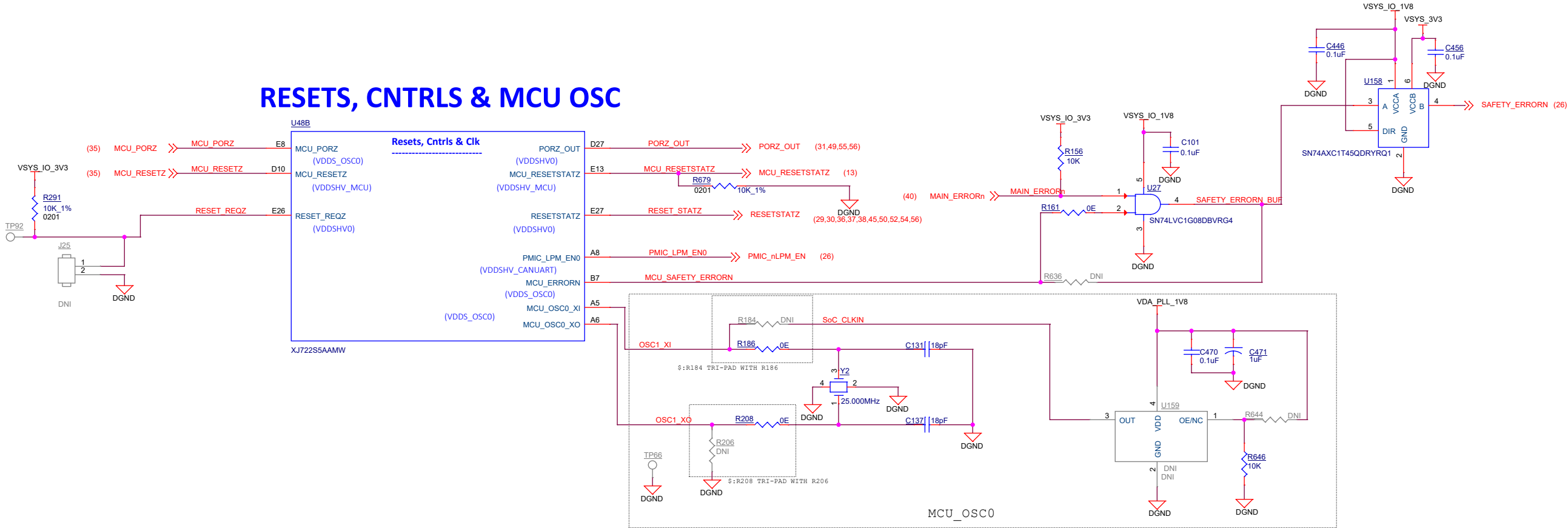
GPIO EXPANDER MAP/TABLE

	GPIO net name	Package Signal name	GPIO No	Input/Output	Default	State	Usage
SOC GPIO	SOC GPIO						
	MCU_INTn_1V8	OSPIO_CSN1	GPIO0_12	Input	PU	Active Low	PMIC Interrupt
	RGMII1_INT#	OSPIO_CSN2	GPIO0_13	Input	PU	Active low	MCU Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
	OSPIO_INT#/ECC_FAIL	OSPIO_CSN3	GPIO0_14	Input	PU	Active Low	Interrupt from OSPI to SoC
	CSI2_EXP_A_GPIO0	GPMC0_CLK	GPIO0_31	IO	NA	NA	CSI2 Expansion Board Specific. 1:2 Mux on the path
	CSI2_EXP_A_GPIO1	GPMC0_AD0	GPIO0_15	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_A_GPIO2	GPMC0_AD1	GPIO0_16	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_A_GPIO3	GPMC0_AD2	GPIO0_17	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_A_GPIO4	GPMC0_AD3	GPIO0_18	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_B_GPIO0	MMC2_CLK	GPIO0_69	IO	NA	NA	CSI2 Expansion Board Specific.
	CSI2_EXP_B_GPIO1	GPMC0_AD4	GPIO0_19	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_B_GPIO2	GPMC0_AD5	GPIO0_20	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_B_GPIO3	GPMC0_AD6	GPIO0_21	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_B_GPIO4	GPMC0_AD7	GPIO0_22	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	EXP_GPIO0_33	GPMC0_OEn_REn	GPIO0_33	IO	NA	NA	User Expansion Specific.1:2 Mux on the path
	EXP_GPIO0_36	GPMC0_BE1n	GPIO0_36	IO	NA	NA	User Expansion Specific.1:2 Mux on the path
	EXP_GPIO0_38	MCU_UART0_CTSn	MCU_GPIO0_7	IO	NA	NA	User Expansion Specific.
	EXP_GPIO0_39	MCU_UART0_RTSn	MCU_GPIO0_8	IO	NA	NA	User Expansion Specific.1:2 Mux on the path
	EXP_GPIO0_41	GPMC0_CSn0	GPIO0_41	IO	NA	NA	User Expansion Specific.1:2 Mux on the path
	EXP_GPIO0_42	GPMC0_CSn1	GPIO0_42	IO	NA	NA	User Expansion Specific.1:2 Mux on the path
	IOEXP1_INT#	MMC2_DAT1	GPIO0_67	Input	PU	Active low	Interrupt for IO Expander 1 ('0' - Interrupt, '1' - No interrupt)
	CSI2_EXP_RSTz	MMC2_DAT0	GPIO0_68	Output	PD	Active low	CSI2 Expansion Interface Reset ('0' - device reset, '1' - normal operation)
	SEL_SDIO_3V3_1V8n	MMC2_CMD	GPIO0_70	Output	PU	Active low	SW controls & transition Sd card to high speed 1.8V signaling if card type supports
	ENET1_EXP_INTB	MMC2_SDWP	GPIO0_72	Input	PU	Active low	ENET expansion 1 Interrupt signal
	EN_EFUSE_VPP	SPI0_D1	GPIO1_19	Output	PD	Active High	VPP_EFUSE LDO enable
	SYS_MCU_PWRDN	EXT_REFCLK1	GPIO1_30	Output	NA	Active low	SYS_MCU_PWRDN('1' - PWR ON, '0' - PWR OFF)
	TA_SOC_INT1z	EXTINTn	GPIO1_31	Input	PU	Active low	Test automation Interrupt to SOC
	SOC_GPIO1_49	MMC1_SDWP	GPIO1_49	Output	NA	Active High	User LED1 ('1' - LED ON, '0' - LED OFF)
	TA_SOC_INT2z/SOC_WAKE	WKUP_UART0_CTSn	MCU_GPIO0_11	Input	PU	Active low	Test automation Interrupt to SOC
	MCU_CAN_STB	WKUP_UART0_RTSn	MCU_GPIO0_12	Output	PU	Active High	Wake from IO retention mode
	TRIG_WDOG	WKUP_CLKOUT	MCU_GPIO0_23	Input	NA	Active Low	MCU CAN0 Standby
		MMC2_SDCD	GPIO0_71				Trigger WDOG to PMIC
							Open
I2C0/0X23	GPIO Expander - 1 Part # TCA6424ARGJR						
	TRC_MUX_SEL		P00	Output	PU	NA	Mux Select Line('0'- MCASP&User Expansion,'1'-TRC data)(Default to TRACE)
	OSPI/ONAND_MUX_SEL		P01	Output	DIP_SEL	NA	Flash Memory Selection ('0' - OSPIO, '1' - OCTAL NAND)
	MCASP1_FET_SEL		P02	Output	PD	Active low	McASP1 FET SWITCH Select Line ('1' - Audio, '0' - HDMI)
	CTRL_PM_I2C_OE#		P03	Output	PU	Active High	I2c Switch Enable ('1' - Enable, '0' - Disable)
	CSI_VIO_SEL		P04	Output	DIP_SEL	Active High	LVC MOS IO Voltage Selection Enable Pin('0'- xxV, '1'- xxV)
	USB2_0_MUX_SEL		P05	Output	PD	Active low	Mux Select Line ('1'- D to 2D, '0'- D to 1D)
	CSI01_MUX_SEL_2		P06	Output	PD	Active low	CSI MUX select ('0'- D to A,'1'-D to B)
	CSI23_MUX_SEL_2		P07	Output	PD	Active low	CSI MUX select ('0'- D to A,'1'-D to B)
	LMK1_OE1		P10	Output	PU	Active low	Clock generator 1 Output 1 Enable
	LMK1_OE0		P11	Output	PU	Active low	Clock generator 1 Output 0 Enable
	LMK2_OE0		P12	Output	PU	Active low	Clock generator 2 Output 0 Enable
	LMK2_OE1		P13	Output	PU	Active low	Clock generator 2 Output 1 Enable
	GPIO_RGMII1_RST#		P14	Output	PU	Active low	Reset for RGMII ('1' - Enable, '0' - Disable)
	GPIO_AUD_RSTn		P15	Output	PU	Active low	Reset for Audio ('1' - Enable, '0' - Disable)
	GPIO_eMMC_RSTn		P16	Output	PU	Active low	Reset for Emmc ('1' - Enable, '0' - Disable)
	GPIO_uSD_PWR_EN		P17	Output	PU	Active High	Load switch ('1' - ON, '0' - OFF)
	USER_LED2		P20	Output	PD	Active low	User LED2 Enable ('1' - LED Off, '0' - LED On)
	MCAN0_STB		P21	Output	PU	Active High	MCAN0 Standby
	PCIe0_1L_RC_RSTz		P22	Output	PD	Active low	PCIe1 1-Lane RC Reset Control ('0' - device reset, '1' - normal operation)
	PCIe0_1L_PRSENT#		P23	Input	PU	Active High	PCIe0 1-Lane Hot Plug / Card Detect ('0' - PCIe Card Detected, '1' - no card detected)
	ENET1_EXP_SPARE2		P24	Input	NA	NA	Ethernet Expansion1 Spare2 ('0' - not defined, '1' - not defined)
	ENET1_EXP_PWRDN		P25	Output	PU	Active High	Ethernet Expansion1 PHY Powerdown ('0' - normal operation, '1' - device power down)
	ENET1_I2CMUX_SEL		P26	Output	PD	NA	Signal Mux Control ('0' - No Connect, '1' - I2C0)
	ENET1_EXP_RESETZ		P27	Output	PD	Active low	Ethernet Expansion1 Reset ('0' - device reset, '1' - normal operation)
I2C1/0X22	GPIO Expander - 2 Part # TCA6416ARTWR						
	DSI_Mux_SEL_2		P00	Output	PD	Active High	DSI Mux Select ('1'- DSI FPC Connector,'0'- DSI to EDP)
	GPIO_eDP_ENABLE		P01	Output	PD	Active High	eDP Bridge Enable
	DPO_PWR_SW_EN		P02	Output	PD	Active High	Enalbe for Display port LDO
	GPIO_OLDI_RSTn		P03	Output	PD	Active low	Reset for OLDI ('1' - Enable, '0' - Disable)
	GPIO_HDMI_RSTn		P04	Output	PD	Active low	HDMI Transmitter Reset Control GPIO
	HDMI_LS_OE		P05	Output	PD	NA	HDMI ESD Device
	PCIe0_1L_PERSTz		P06	Input	NA	NA	PCIe0 1-Lane Bus Reset ('0' - device reset, '1' - normal operation)
	DSI_GPIO0		P10	IO	NA	NA	DSI flex Connector
	DSI_GPIO1		P11	IO	NA	NA	DSI flex Connector
	DSI_EDID		P12	Input	NA	Active low	Interrupt
	IO_eDP_IRQ		P13	Input	PU	NA	Interrupt signal from DSI to eDP bridge
	OLDI_INT#		P14	Input	PU	Active low	Interrupt from OLDI display
	HDMI_INTn		P15	Input	PU	Active low	Interrupt from HDMI display

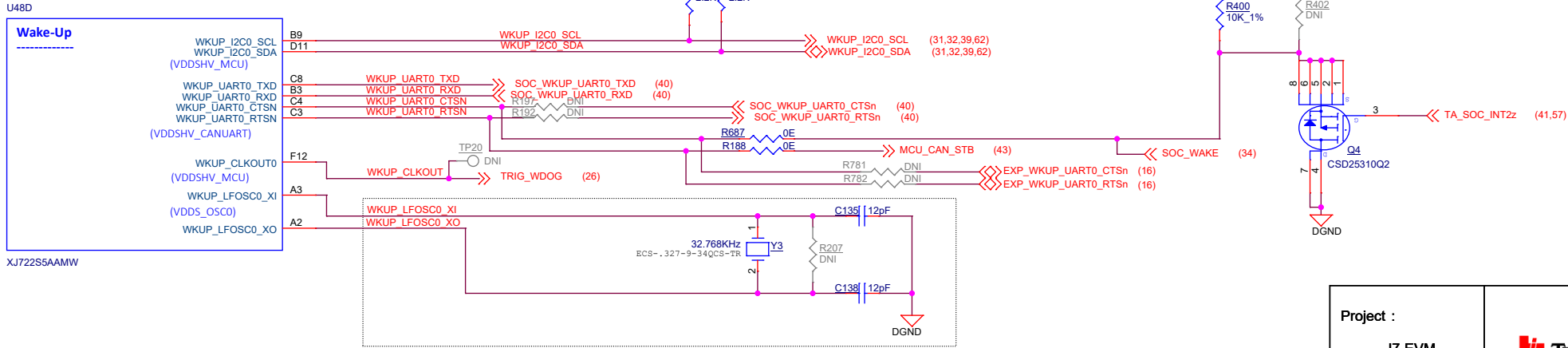
MCU GENERAL IO




RESETS, CNTRLS & MCU OSC

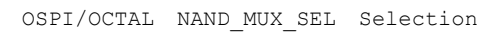


WKUP RESETS, CNTRLS & OSC



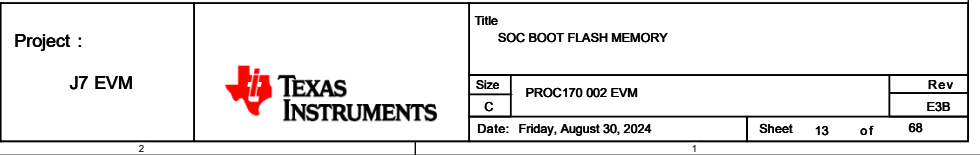
Project : J7 EVM		Title SOC MCU IO CNTRLOSC & WKUP	
		Size C	Rev E3B
		Date: Tuesday, September 17, 2024	
		Sheet 11 of 68	

2:1 Mux for OSPI/OCTAL NAND

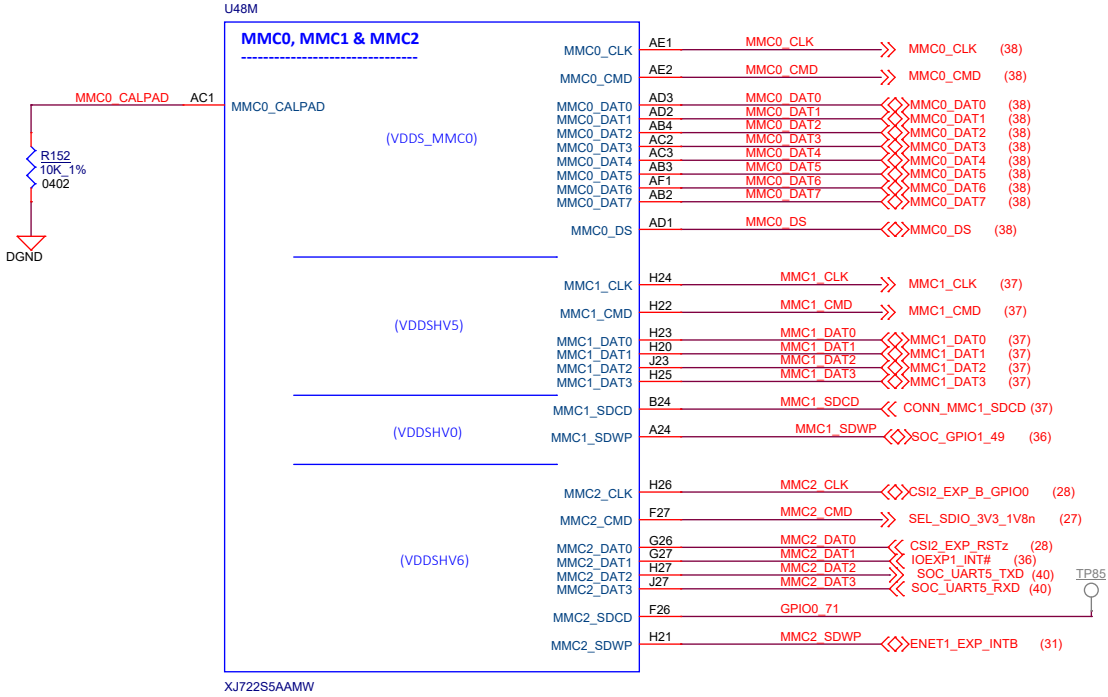


'0' - (A --> B) OSPI Flash
'1' - (A --> C) OCTAL NAND
Note: Default set by dip switch

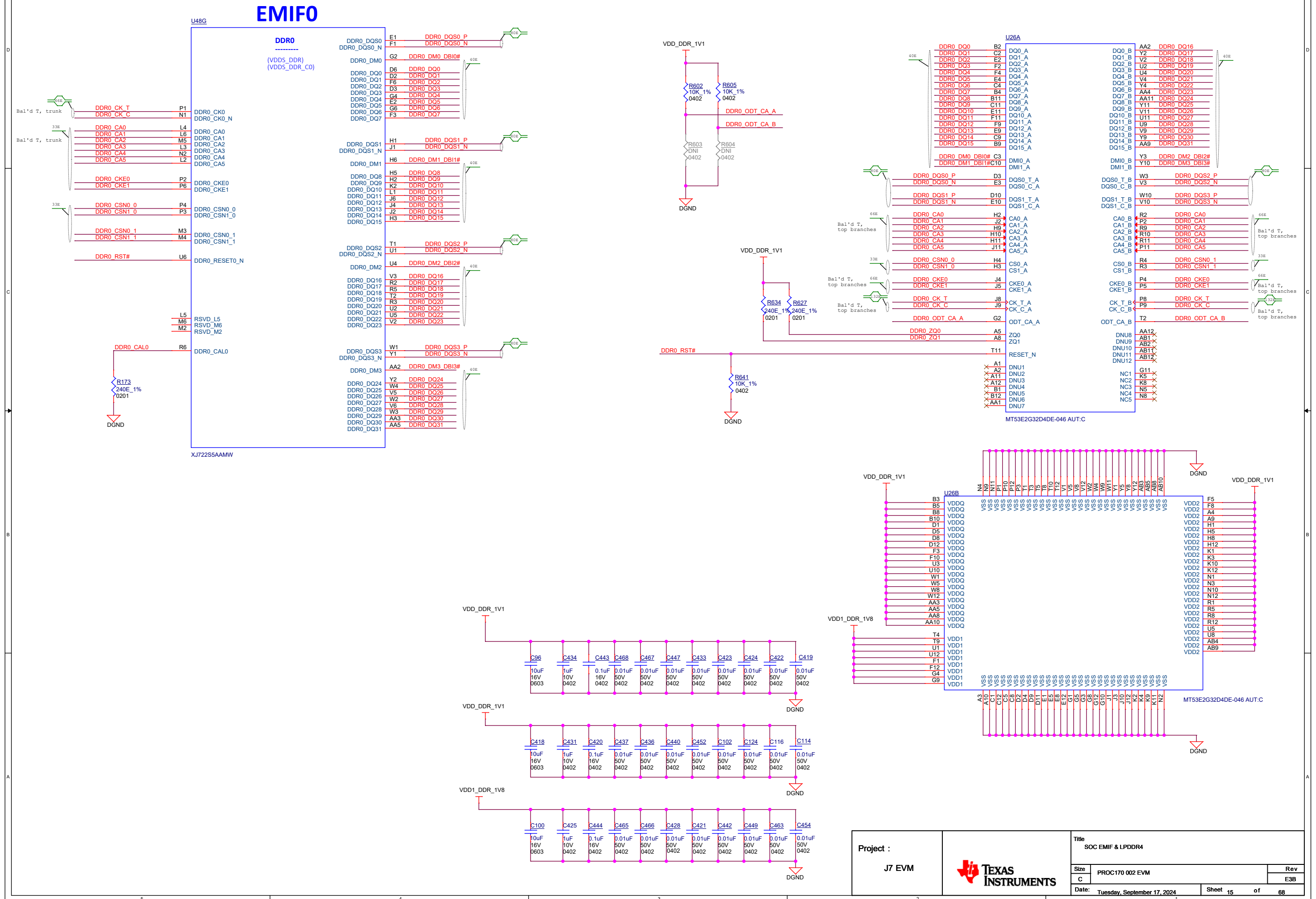
OSPI/ONAND_MUX_SEL (36)



MMC 0, 1, 2



LPDDR4 MEMORY I/F



U48A

General IO

(VDDSHV0)

D23 I2C0_SCL
B22 I2C0_SDA
C24 I2C1_SCL
A22 I2C1_SDA
D20 SPI0_CLK
B20 SPI0_CS0
C20 SPI0_CS1
E19 SPI0_D0
E20 SPI0_D1
F20 UART0_TXD
F19 UART0_RXD
E22 UART0_CTSN
B21 UART0_RTSN
B23 EXTINTN
A23 EXT_REFCLK1
D22 MCAN0_TX
C22 MCAN0_RX
F24 MCASP0_ACLKR
C27 MCASP0_AFSR
F23 MCASP0_AXR0
B25 MCASP0_AXR1
A26 MCASP0_AXR2
A25 MCASP0_AXR3
D25 MCASP0_ACLKX
C26 MCASP0_AFSX

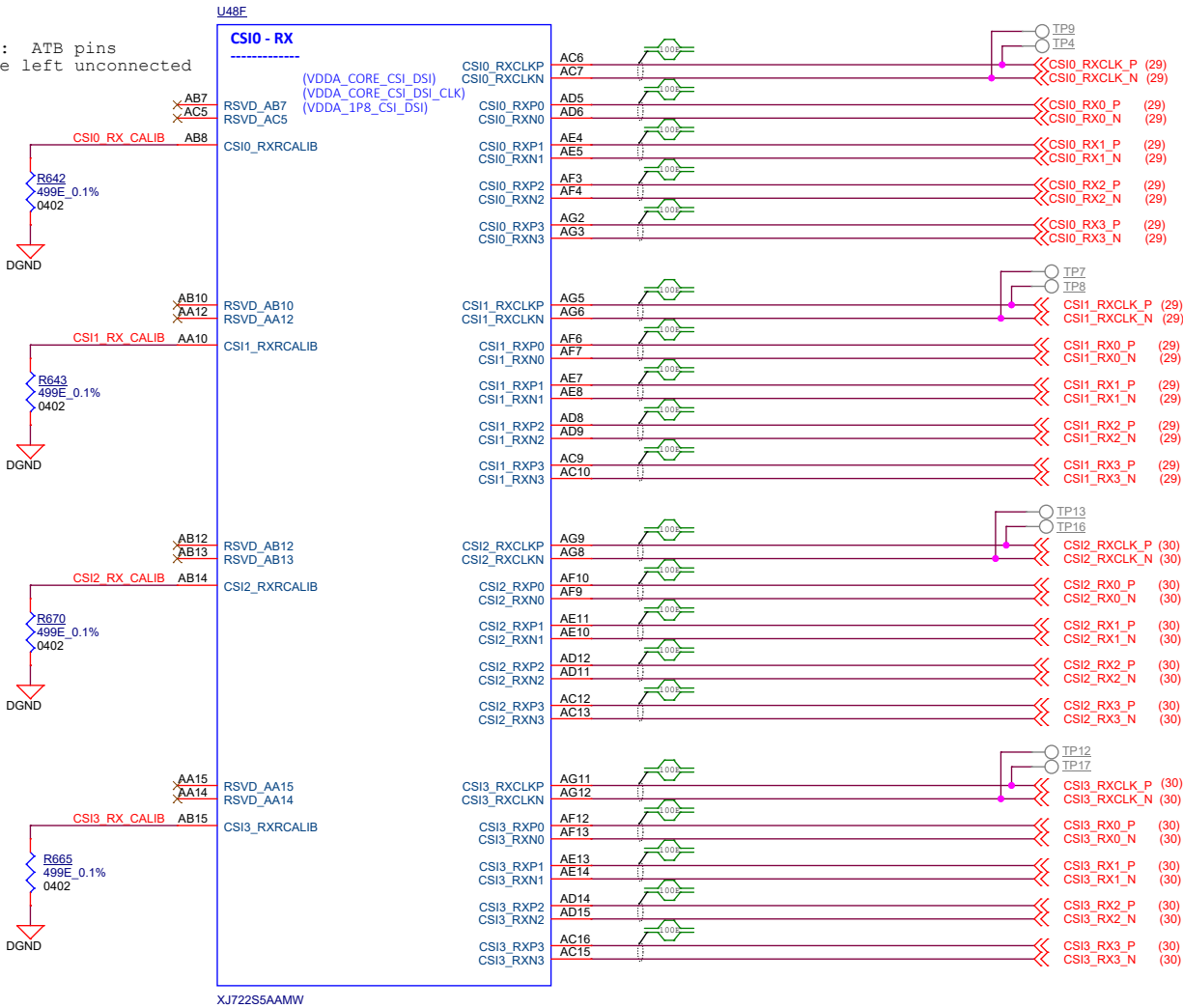
SOC_I2C0_SCL (31,33,36,39,50,55,57,58)
SOC_I2C0_SDA (31,33,36,39,50,55,57,58)
SOC_I2C1_SCL (36,52,54)
SOC_I2C1_SDA (36,52,54)
EHRPWM1_A (32)
EHRPWM0_A (32)
ECAP0_IN_APWM_OUT (32)
EHRPWM1_B (32)
EN_EFUSE_VPP (27)
EXP_GPIO1_19 (16)
SOC_UART0_TXD (40)
SOC_UART0_RXD (40)
UART0_CTSN (40)
UART0_RTSN (40)
EXTINTN
SYS_MCU_PWRDN (34)
MCAN0_TX (44)
MCAN0_RX (44)
UART1_TXD (32)
UART1_RXD (32)
MCASP0_AXR0 (32)
MCASP0_AXR1 (32)
MCASP0_AXR2 (32)
MCASP0_AXR3 (32)
MCASP0_ACLKX (32)
MCASP0_AFSX (32)

R270 2.2K
R271 2.2K
R277 2.2K
R690 10K
Q5 CSD25310Q2
VSYS_IO_3V3
DGND

The diagram shows two test points, TP403 and TP402, connected to a common ground. TP403 is connected to a signal line labeled OBCLK0. TP402 is connected to a ground symbol labeled DGND.

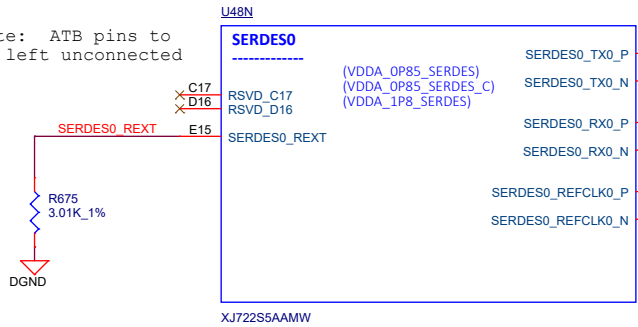
CSI 0, 1, 2, 3

Note: ATB pins
to be left unconnected



SERDES0

Note: ATB pins to be left unconnected



B18 SERDES0_TX0_P
B19 SERDES0_TX0_N
A19 SERDES0_RX0_P
A20 SERDES0_RX0_N
A16 SERDES0_REFCLK_P
A17 SERDES0_REFCLK_N



R63 DNI
R60 DNI

R796 DNI

R797 DNI

DGND

For External 156.25MHz Clk support:
DNI: R676, R678
Assemble: R64,R59,R63,R60

For SoC 156.25MHz Clk support:
DNI: R64,R59
Assemble: R676,R678,R63, R60

C153 DNI

C157 DNI

R269 DNI

R278 DNI

C154

0.22uF

C155

0.22uF

R272

0E

R276

0E

ENET EXPANSION

QSGMII1_PHY_REFCLK_P (31)
QSGMII1_PHY_REFCLK_N (31)

SGMII2_TX0_P (31)
SGMII2_TX0_N (31)

SGMII2_RX0_P (31)
SGMII2_RX0_N (31)

USB 3.0 HUB

USBC_SS_TX0_P (45)

USBC_SS_TX0_N (45)

USBC_SS_RX0_P (45)

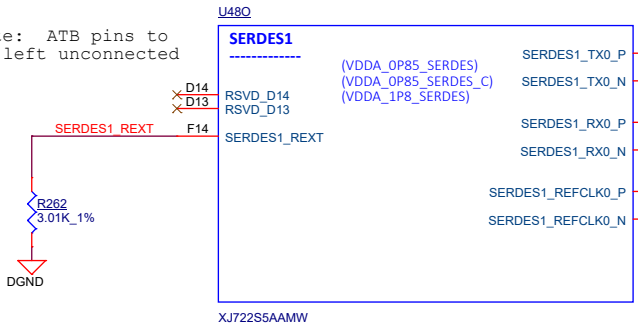
USBC_SS_RX0_N (45)

CLKGEN_SERDES0_REFCLK_P (33)

CLKGEN_SERDES0_REFCLK_N (33)

SERDES1

Note: ATB pins to be left unconnected



A14 SERDES1_TX0_P
A13 SERDES1_TX0_N
C15 SERDES1_RX0_P
C14 SERDES1_RX0_N
B16 SERDES1_REFCLK_P
B15 SERDES1_REFCLK_N



R798

49.9E_1%

R799

49.9E_1%

DGND

C152 DNI

C148 DNI

R255 DNI

R247 DNI

C151

0.22uF

C149

0.22uF

R253

0E

R248

0E

PCIe x4L Connector

PCIE0_TX0_P (55)

PCIE0_TX0_N (55)

PCIE0_RX0_P (55)

PCIE0_RX0_N (55)

SOC_SERDES1_REFCLK_P (55)

SOC_SERDES1_REFCLK_N (55)

ENET EXPANSION

SGMII1_TX0_P (31)
SGMII1_TX0_N (31)

SGMII1_RX0_P (31)
SGMII1_RX0_N (31)

Project :

J7 EVM



Title
SOC SERDES 0 & 1

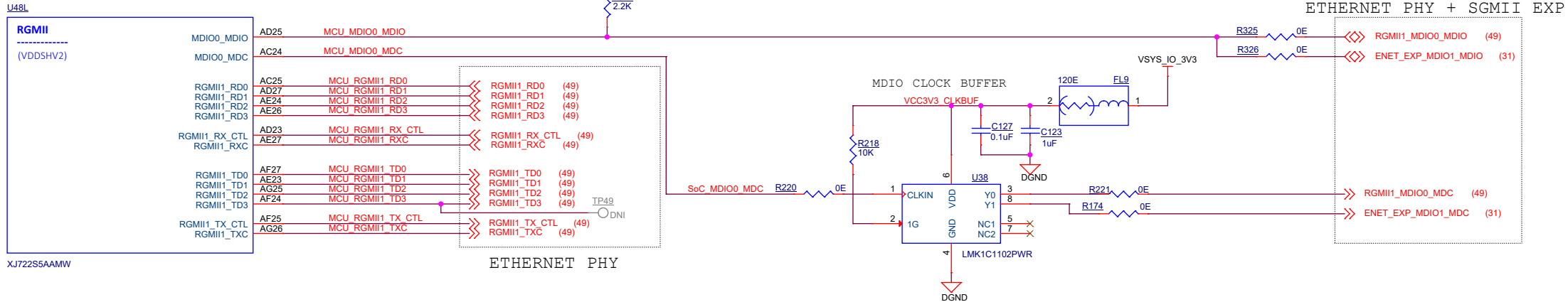
Size
C PROC170 002 EVM

Date: Tuesday, September 17, 2024

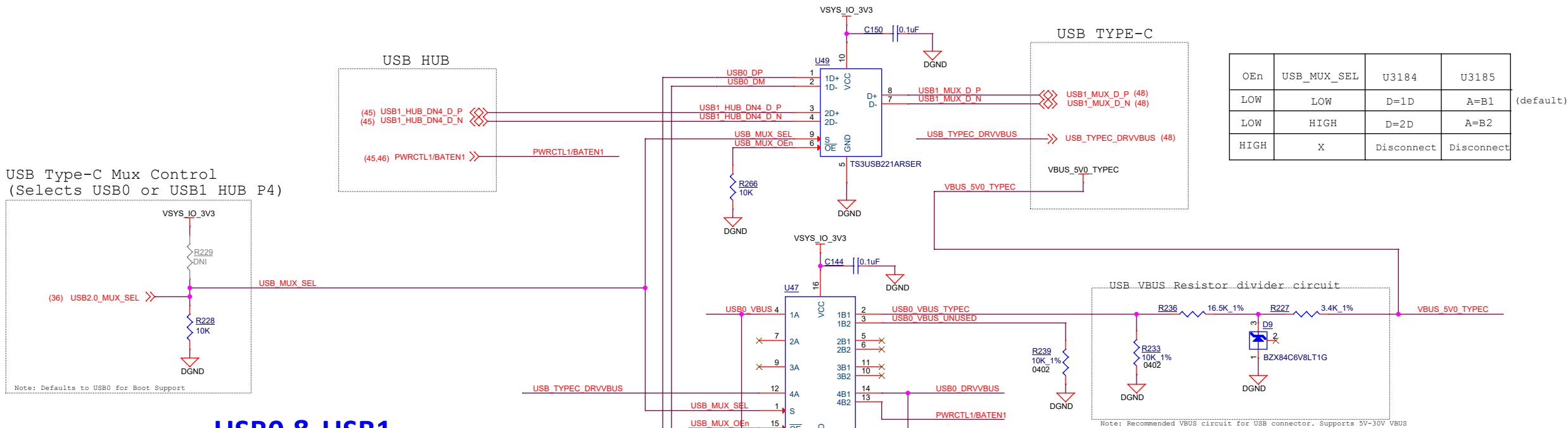
Rev
E3B

Sheet 18 of 68

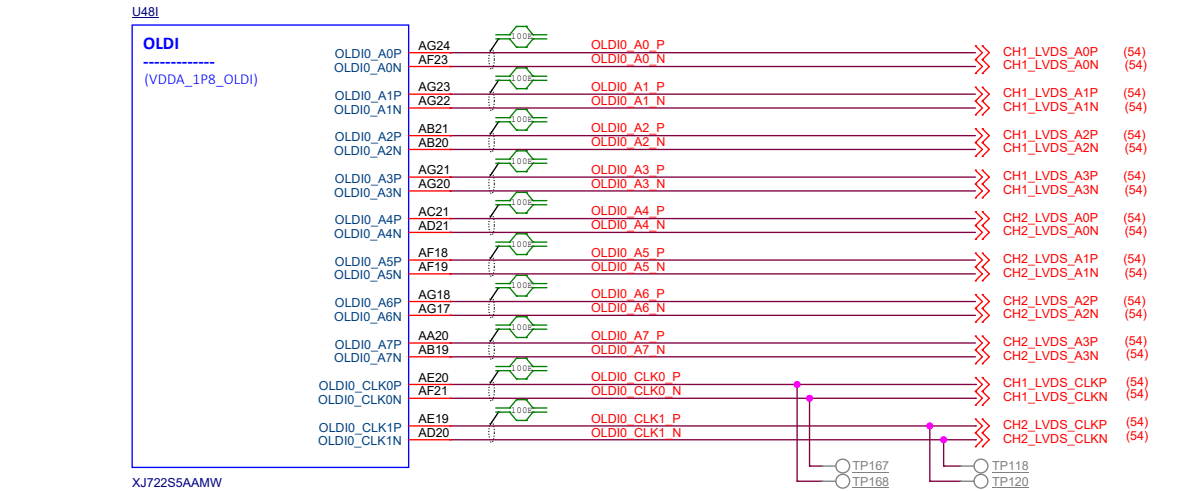
RGMII



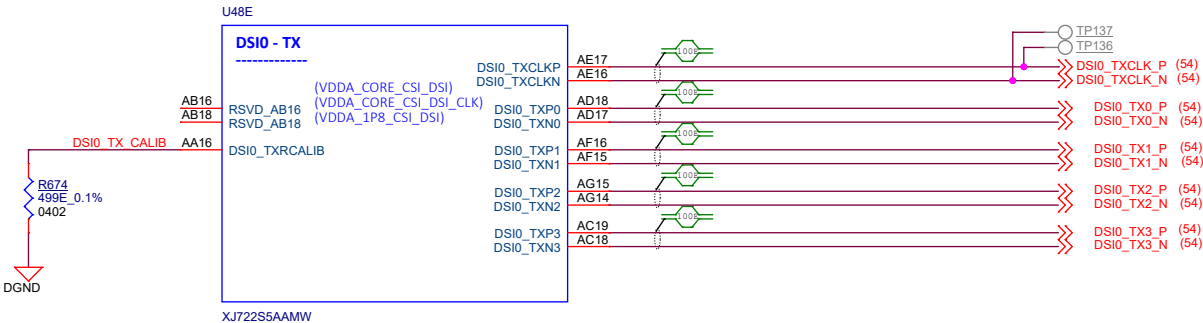
USB Type-C Mux
(Selects USB0 or USB1 HUB P4)



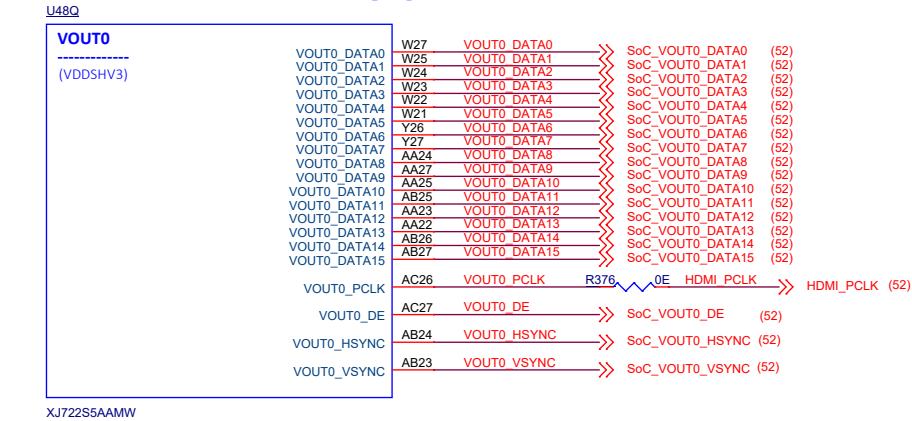
OLDI



DSI



VOUT



monitoring VSYS_3V3, to protect SoC from 1st stage power fault.

Project :

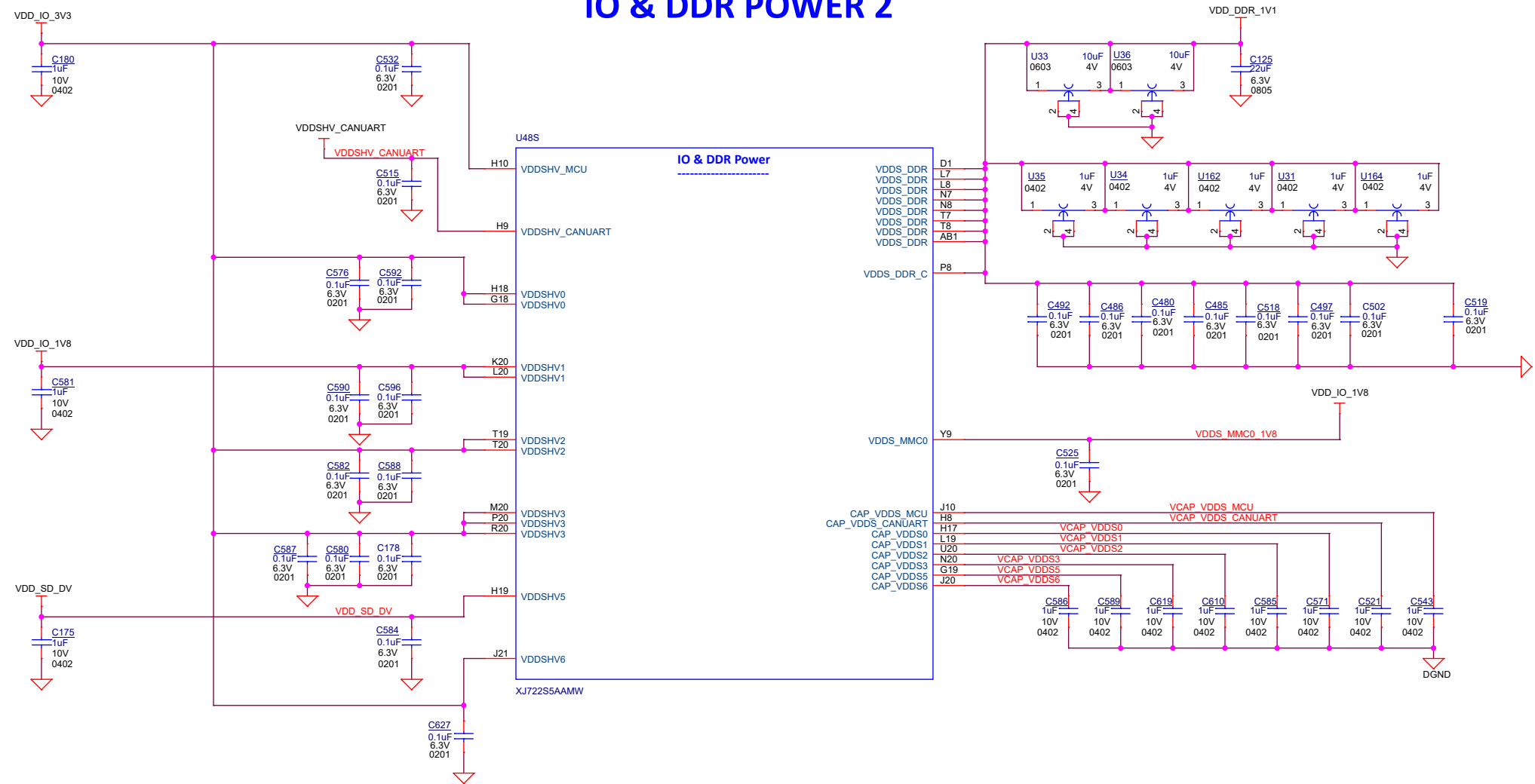
J7 EVM



Title	SOC VMON, JTAG
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Size	PROC170 002 EVM	Rev
C		E3B
Date:	Tuesday, September 17, 2024	Sheet 21 of 68

IO & DDR POWER 2

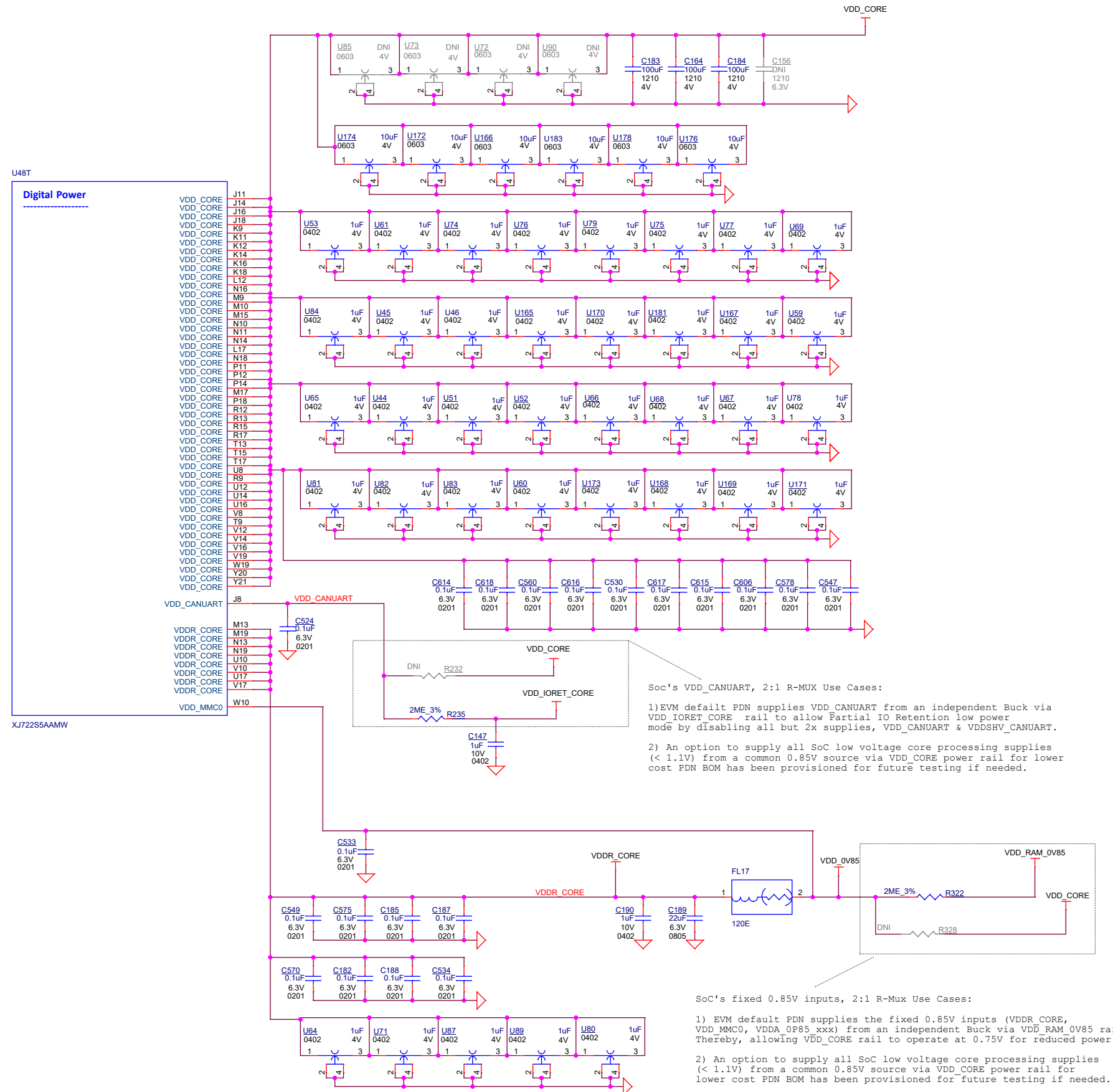


Note:

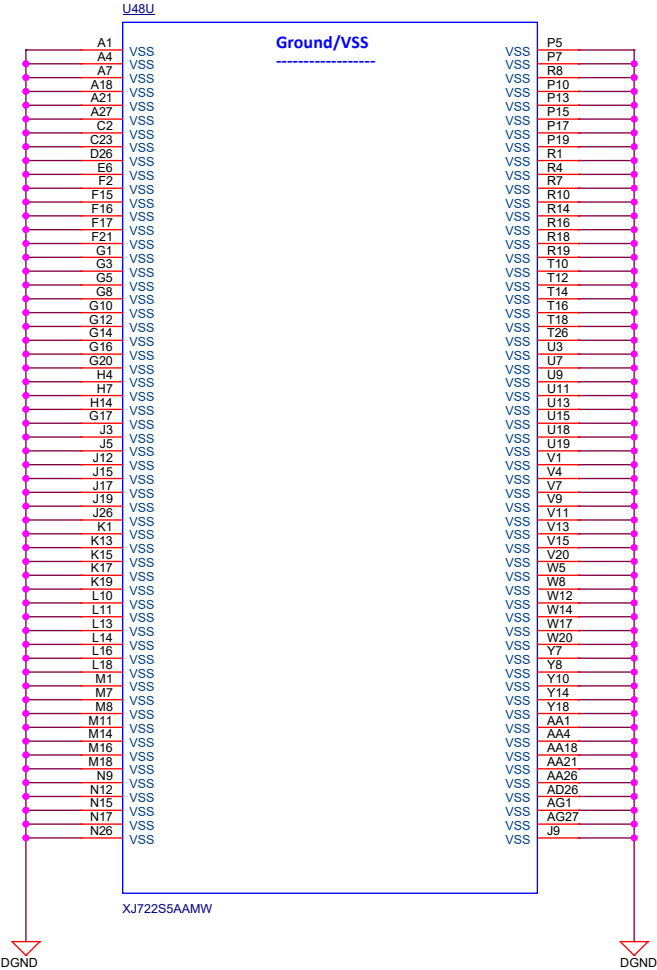
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

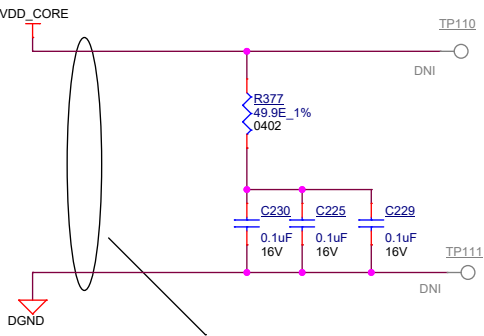
DIGITAL POWER 3



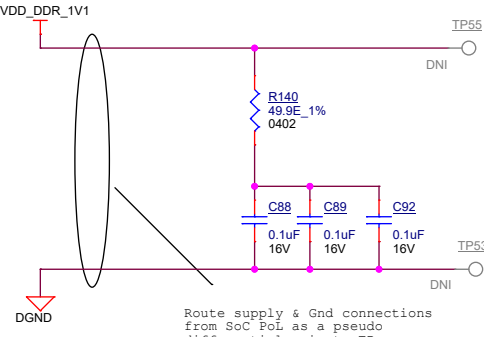
SOC GROUND



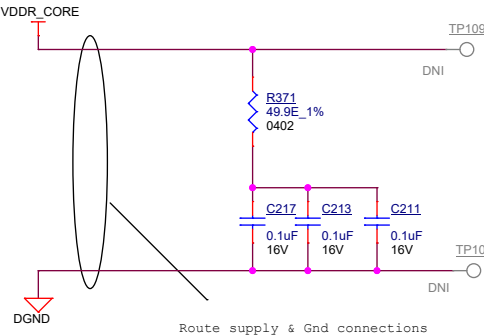
SoC Supply Noise Kelvin Sensing



Route supply & Gnd connections from SoC Pol as a pseudo differential pair to TPs near R & C termination for easy access



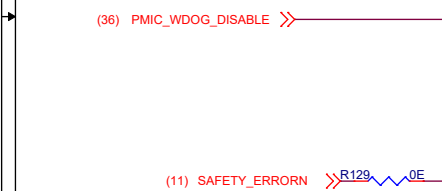
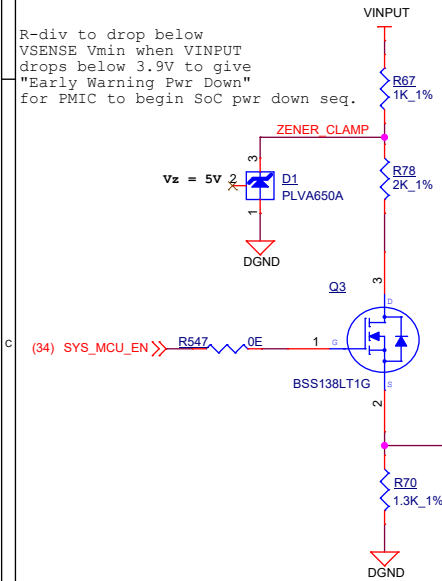
Route supply & Gnd connections from SoC Pol as a pseudo differential pair to TPs near R & C termination for easy access



Route supply & Gnd connections from SoC Pol as a pseudo differential pair to TPs near R & C termination for easy access

SOC PMIC POWER

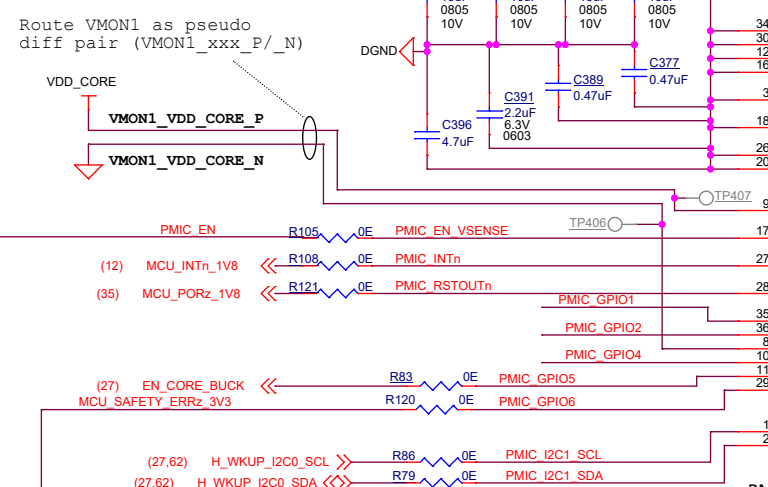
R-div to drop below VSENSE Vmin when VINPUT drops below 3.9V to give "Early Warning Pwr Down" for PMIC to begin SoC pwr down seq.



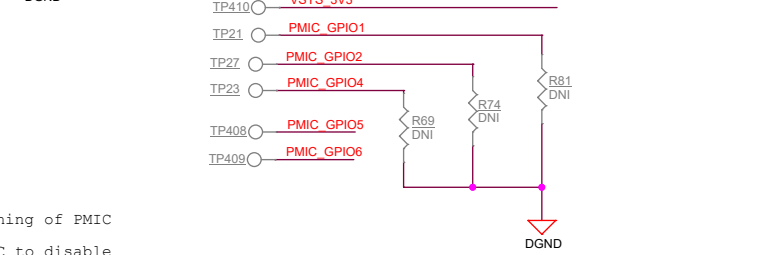
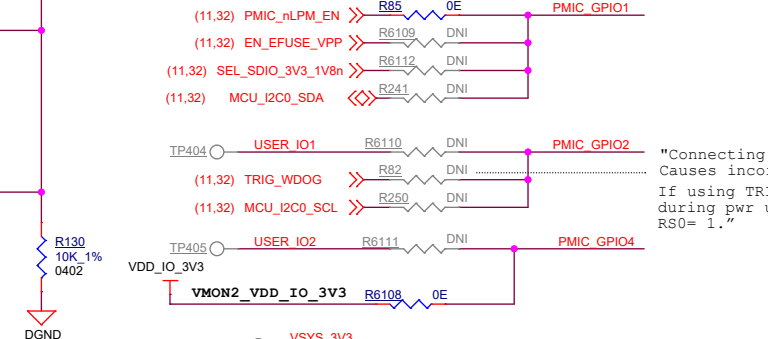
PMIC's GPIO6 supports 2x PDN functions:
A) DISABLE WDOG: PMIC reads logic level at GPIO6 pin at beginning of PMIC start-up sequence before NVM initialization.
a) High level at GPIO6 pin (SW-1/Jmpr-1 = closed) directs PMIC to disable Watch-Dog Timer (by setting WD_PWRHOLD bit to disable timer's long-window time-out).
b) Low level at GPIO6 pin (SW-1/Jmpr-1 = open due to PMIC default internal pull-down R) enables Watch-Dog Timer (default setting enables timer's long-window time-out).
B) MCU SAFETY ERROR: After PMIC NVM initialization, GPIO6 function is set to Error Signal Monitor (ESM) function.

SWITCH (SW2 - 5)	Description
CLOSED	Disables WDog, high latched at Pwr-Up
OPEN (Default)	Enables WDog, low latched at Pwr-Up

Route VMON1 as pseudo diff pair (VMON1_xxx_P/_N)



R-Muxes On GPIO inputs allow selecting diff interface signals as needed for diff PDN Schemes



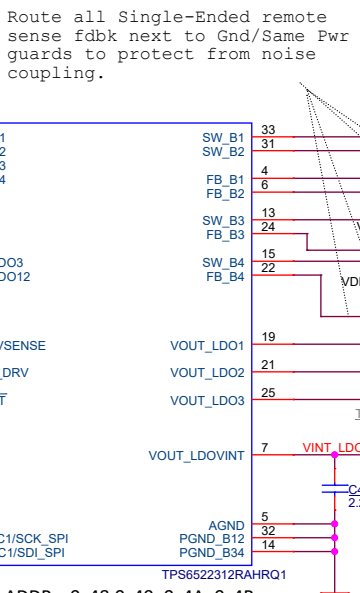
PMIC GPIO_1 & GPIO_2, 2:1 R-Mux Use Cases:

- 1) Install R85 to support SoC's Partial IO Ret low power mode that needs PMIC_nLPM_EN connected to GPIO1.
- 2) Install R82 to support alternative Trigger WDog timer mode of operation.

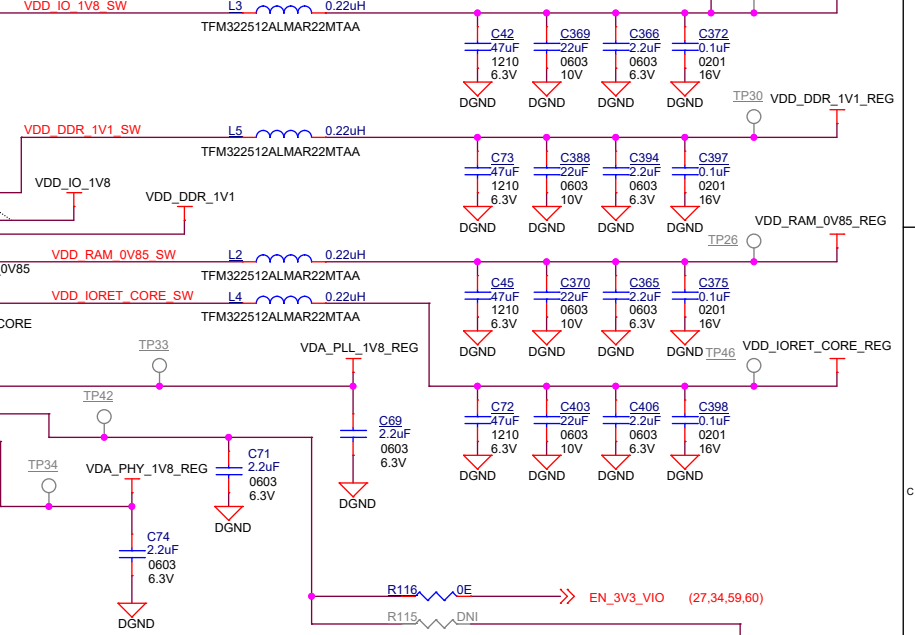
TI EVM default board & BOM supports Use Case #1

Note:
Previous J7xxx PDNs used a 2nd, indep I2C Ch (MCU_I2C0_SCL/SDA) for WDOG operations. Burton PMIC has limited GPIOs, so 1x I2C Ch will be timed multiplexed (PMIC control/settings & WDOG ops) in order to support low pwr modes.

Route all Single-Ended remote sense fdbk next to Gnd/Same Pwr guards to protect from noise coupling.



PMIC I2C1 ADDRs: 0x48,0x49, 0x4A, 0x4B "Watch Dog Timer" I2C1 ADDR: 0x12

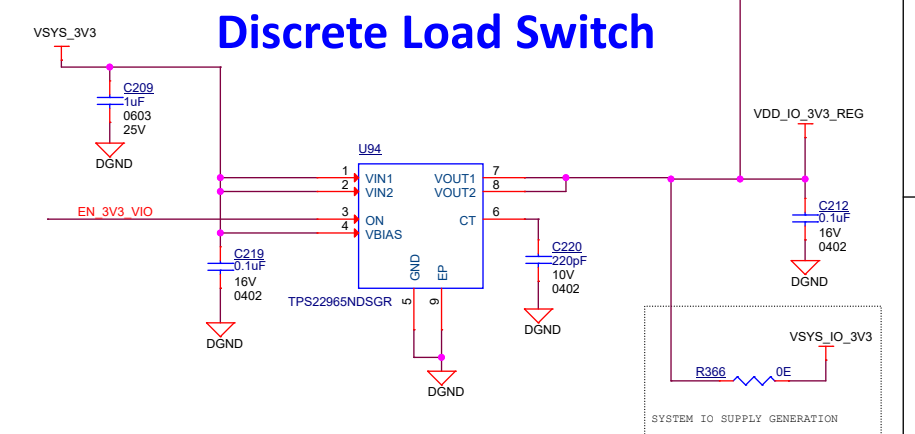


PMIC LDO2, 2:1 R-Mux Use Cases:

- 1) Install R116 to use LDO2 Vout as "EN_3V3_VIO" control signal on a discrete load switch to supply VDD_IO_3V3 loads > 165mA, SoC & all board peripheral components.
- 2) Install R115 to use LDO2 in FET Bypass/Load Switch mode to supply VDD_IO_3V3 loads < 165mA, SoC & all board peripheral components.

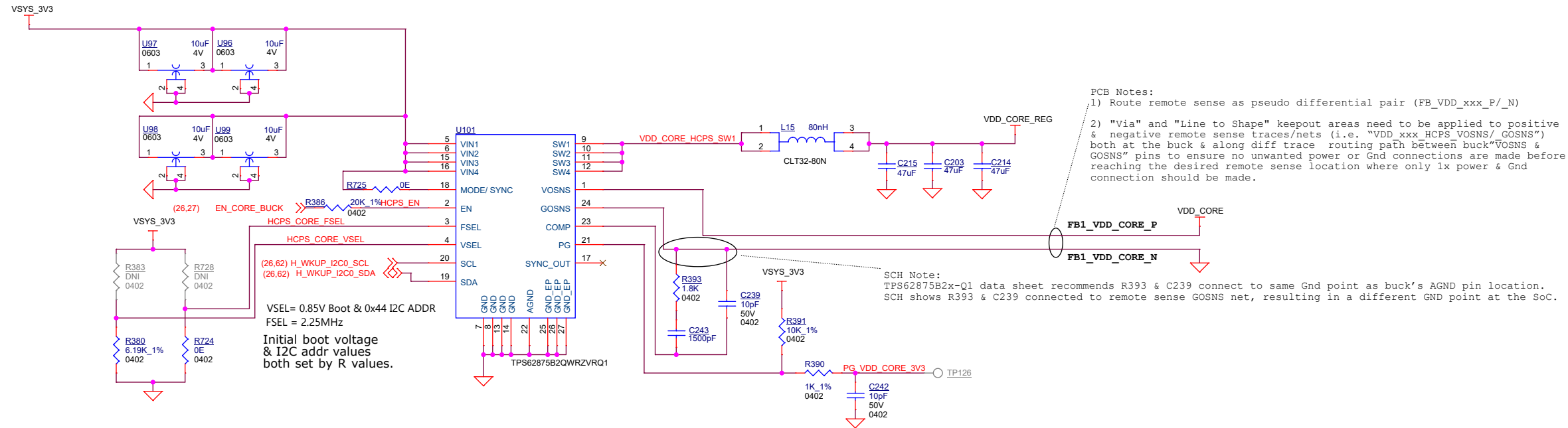
TI EVM default board & BOM is use case #1.

Discrete Load Switch

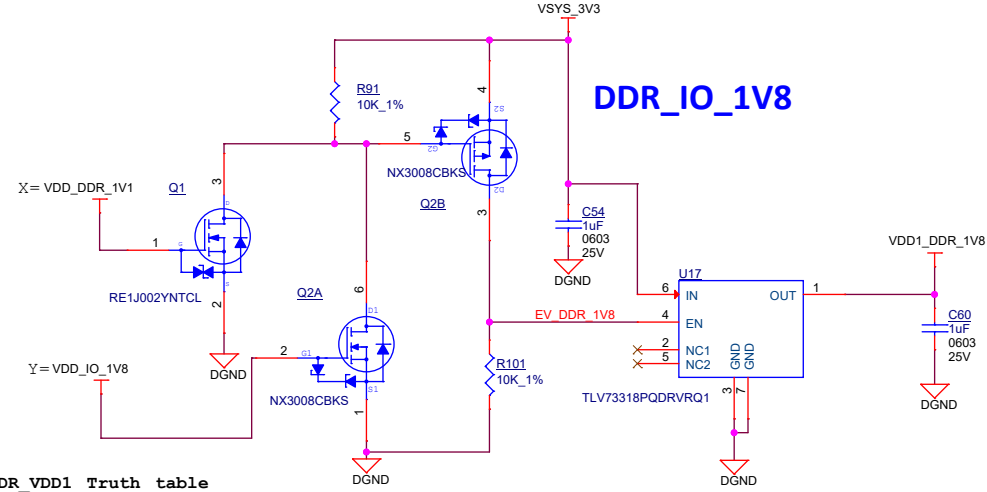
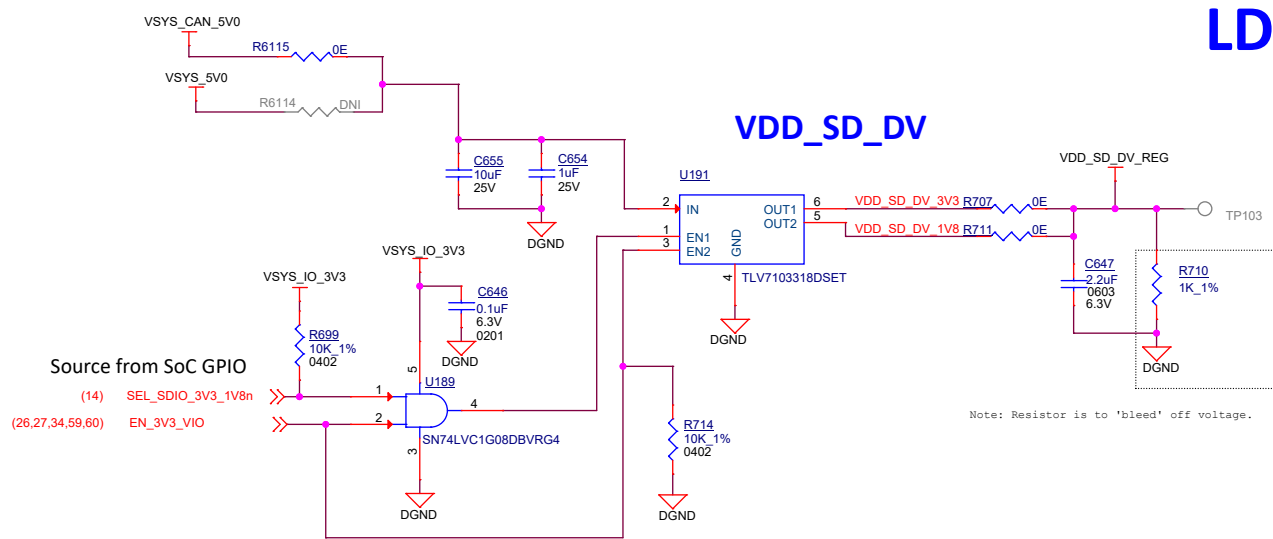


Project : J7 EVM		Title SOC PMIC & LDSW POWER	
		Size C	Rev E3B
		Date: Thursday, September 12, 2024	
		Sheet 26 of 68	

VDD_CORE High-Current Power Stage (HCPS)

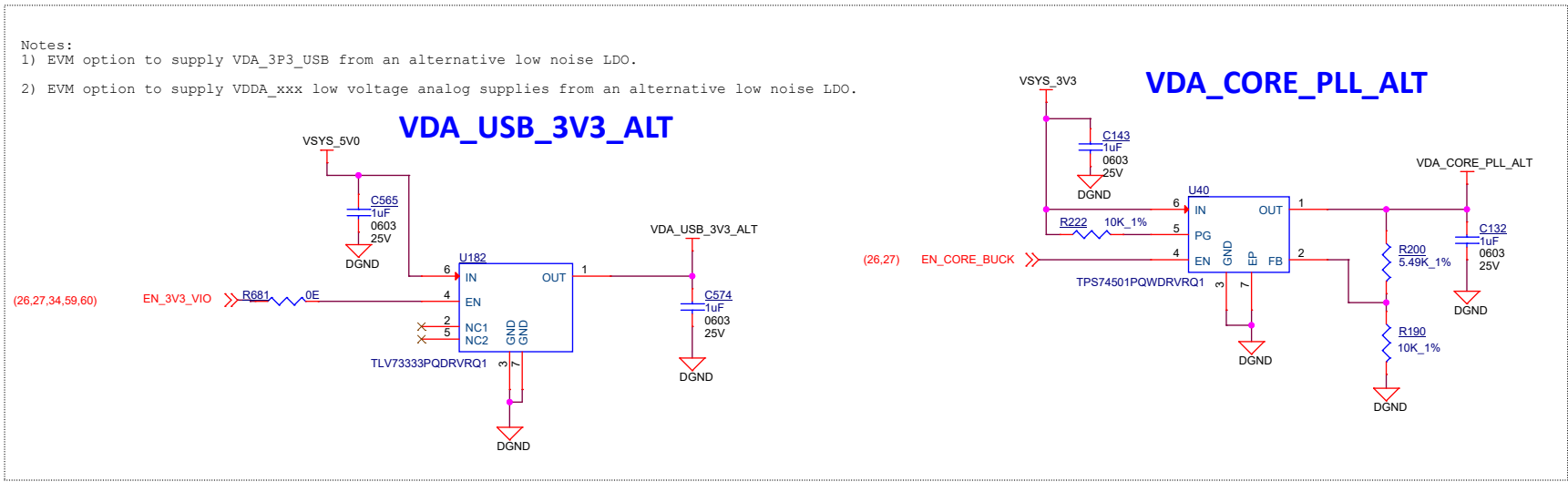


LDOs

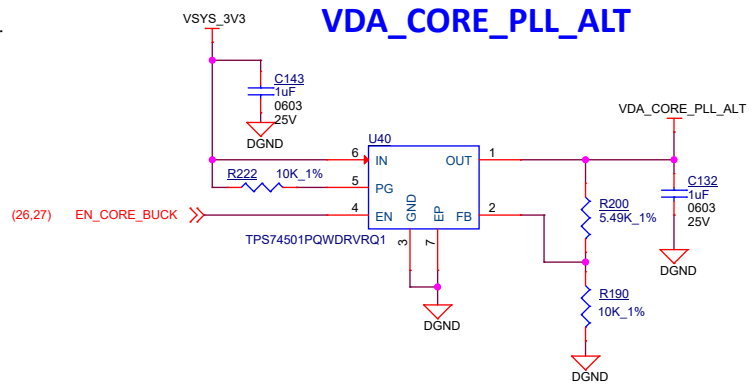


EN_DDR_VDD1 Truth table

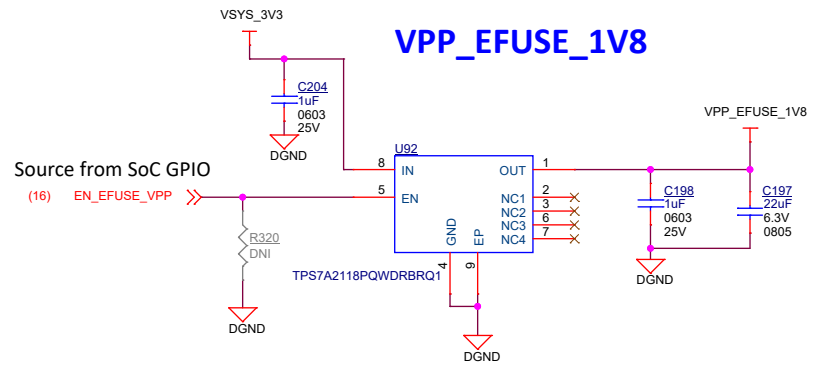
Descrt	"OR" Gate Logic	EN_DDR_1V8
X	Y	OUTPUT
0	0	0
0	1	1
1	0	1
1	1	1



VDA_CORE_PLL_ALT

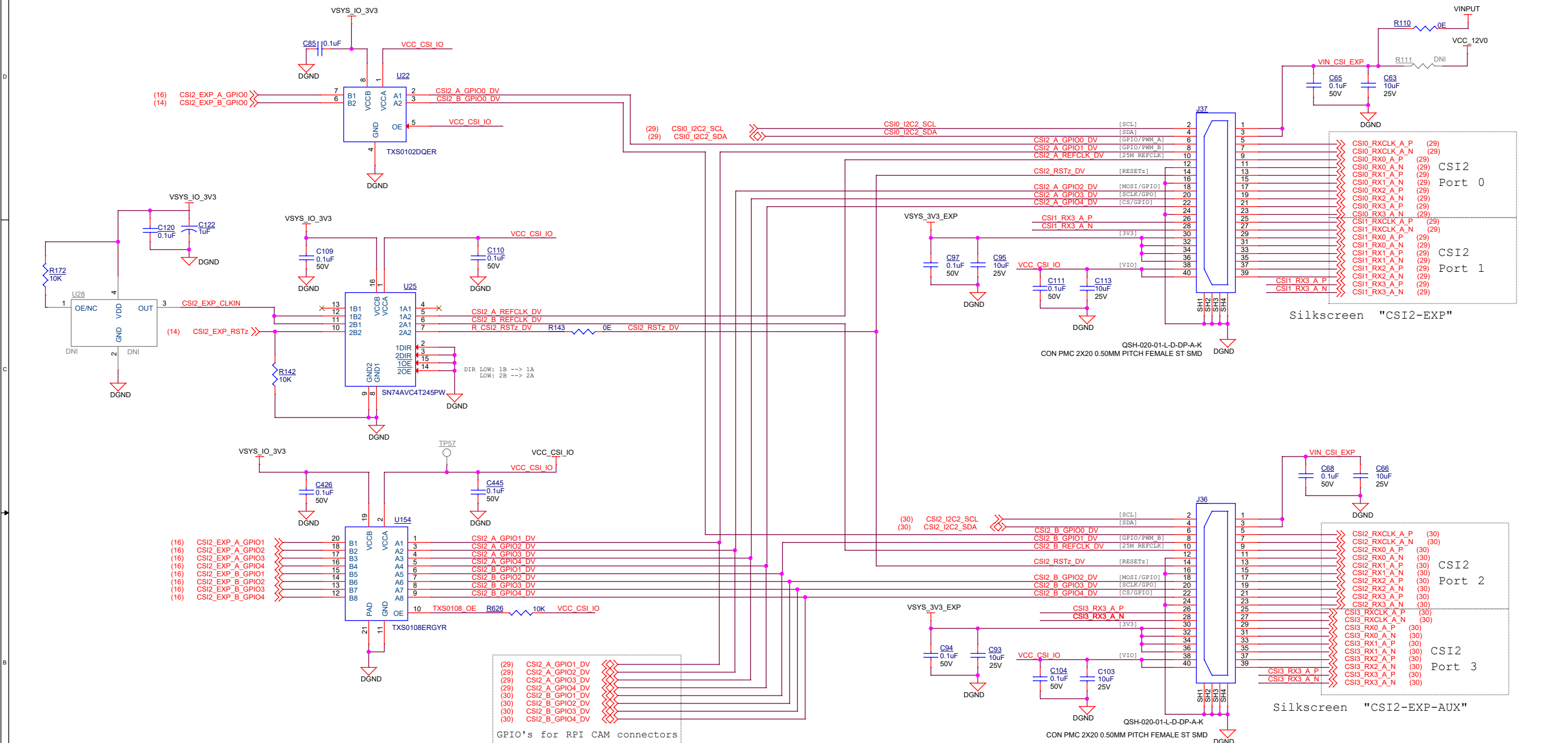


VPP_EFUSE_1V8

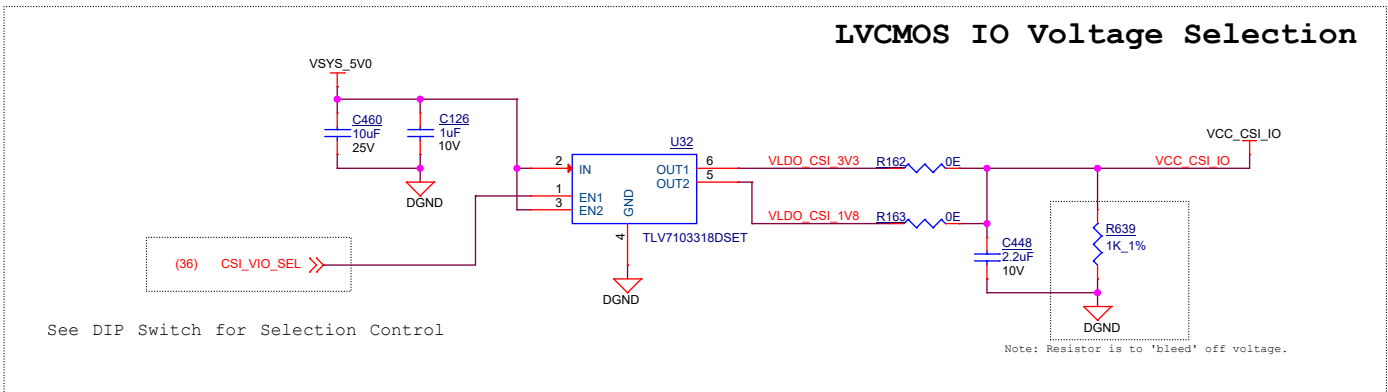


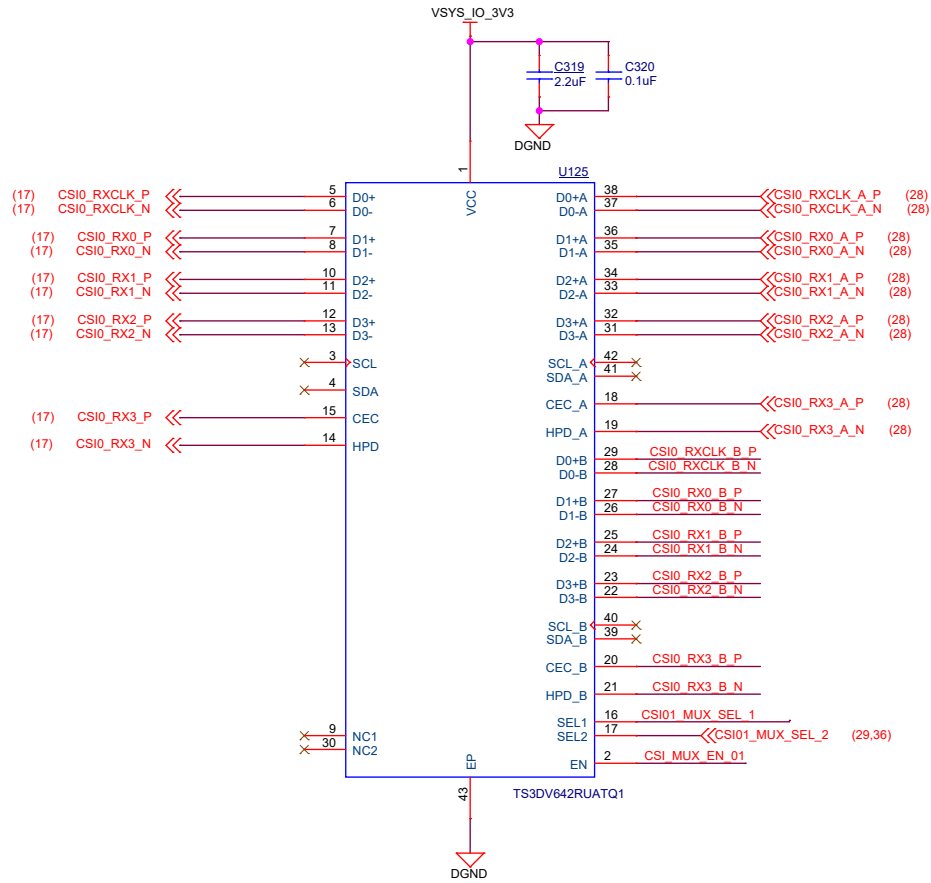
Level Translation for LVCMOS

CSI2 EXPANSION CONNECTORS



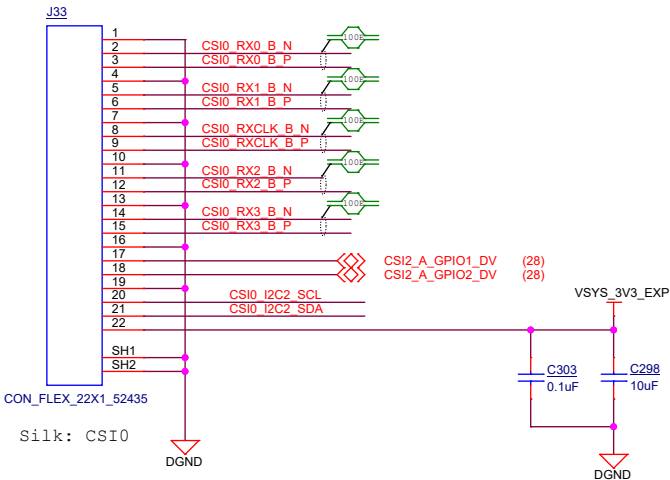
CSI2_EXP_A GPIO2, 4 are connected to SOC GPIO and others are from IO expander



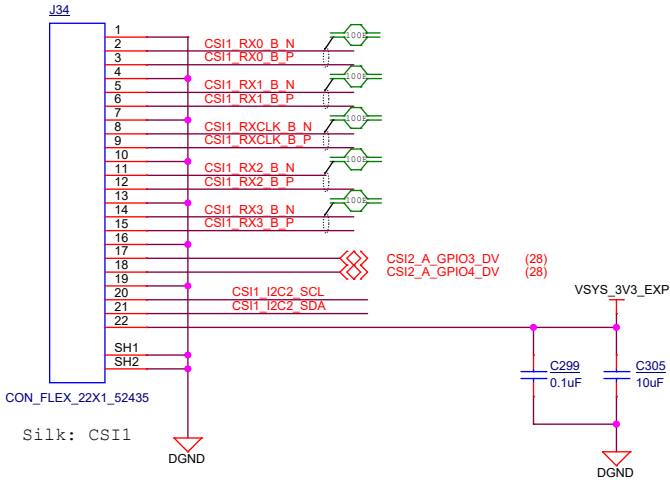


From CSI EXP Conn

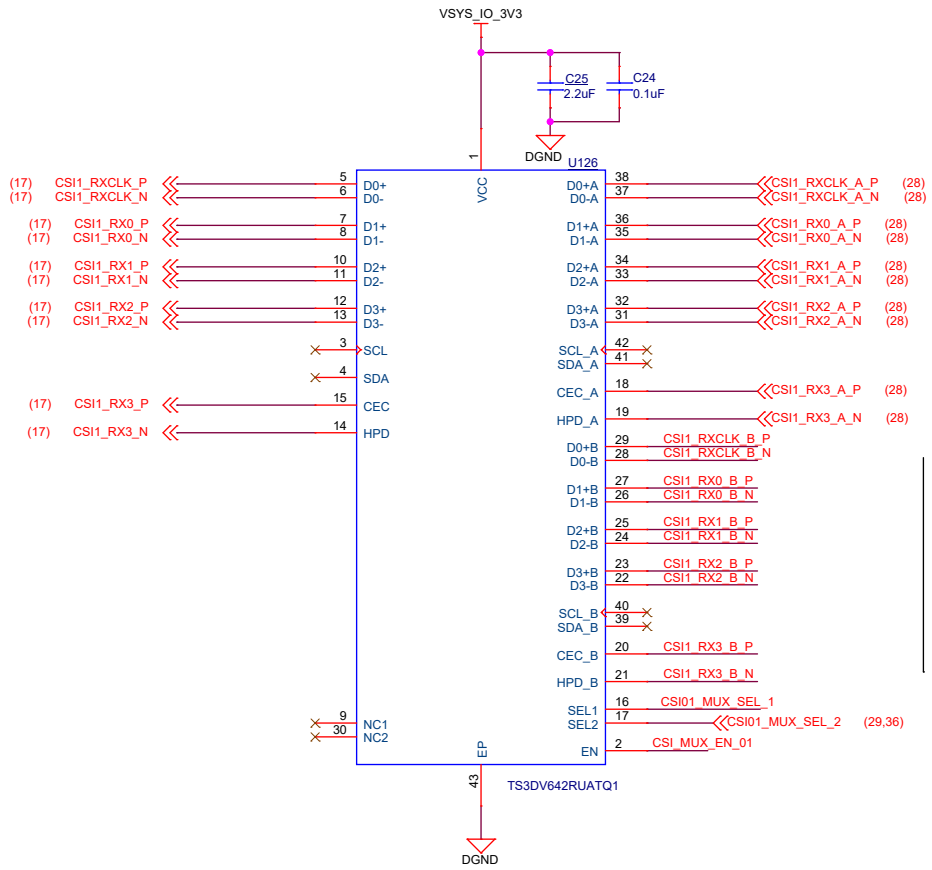
From FPC Camera Conn



Silk: CSI0



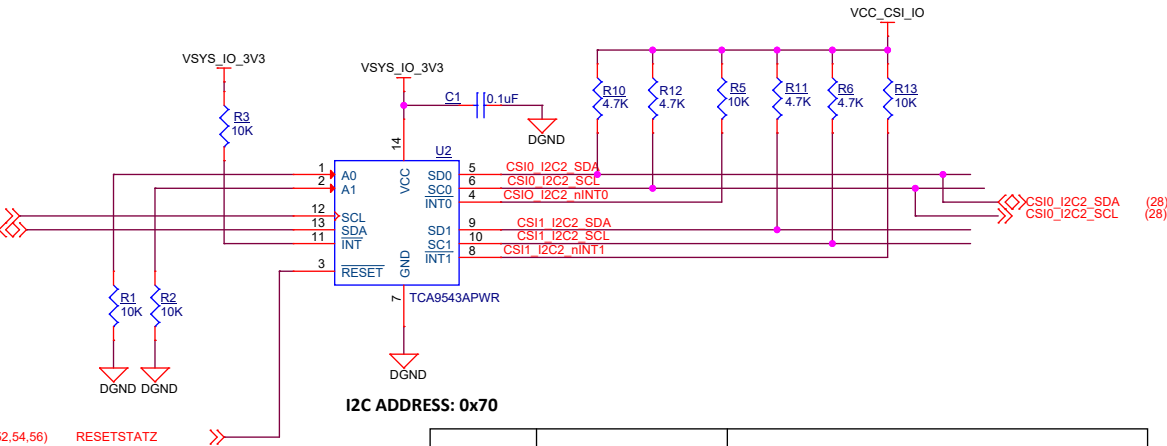
Silk: CSI1



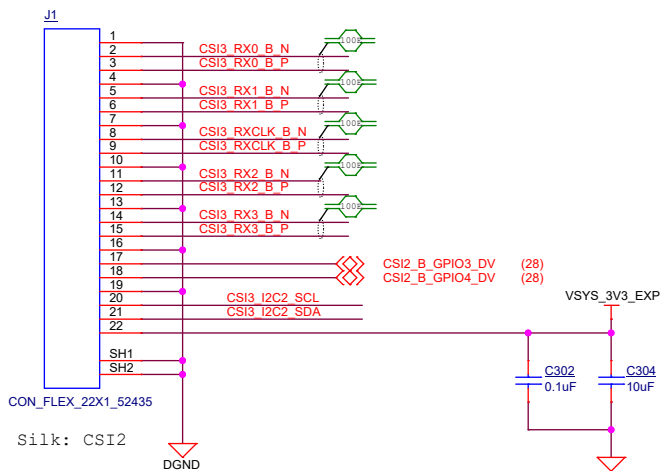
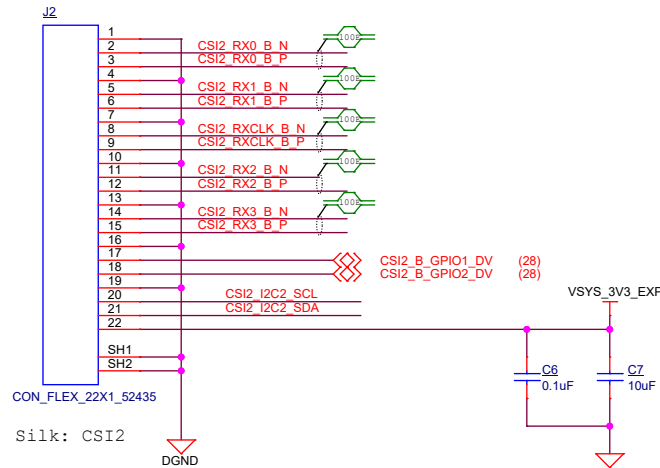
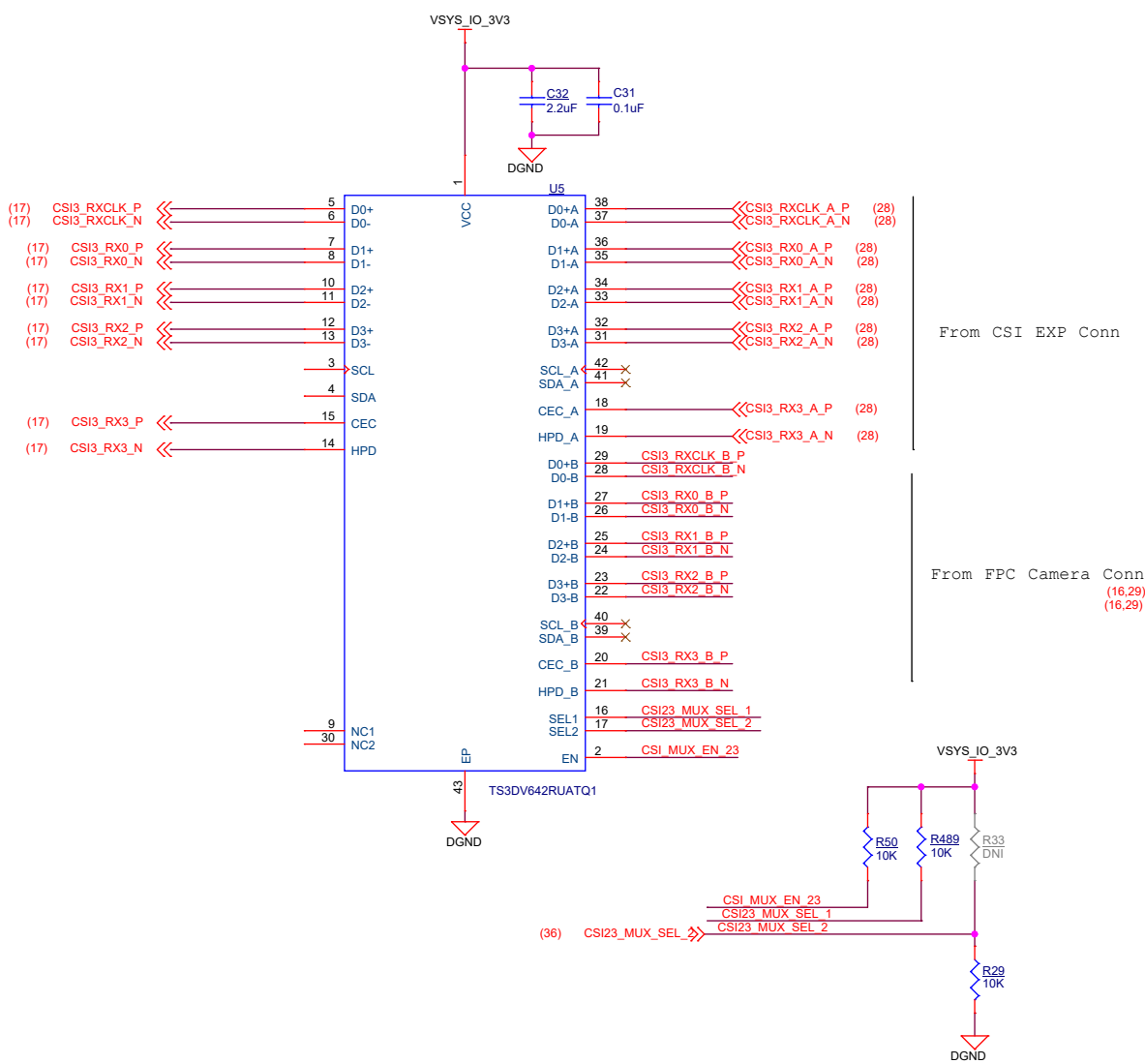
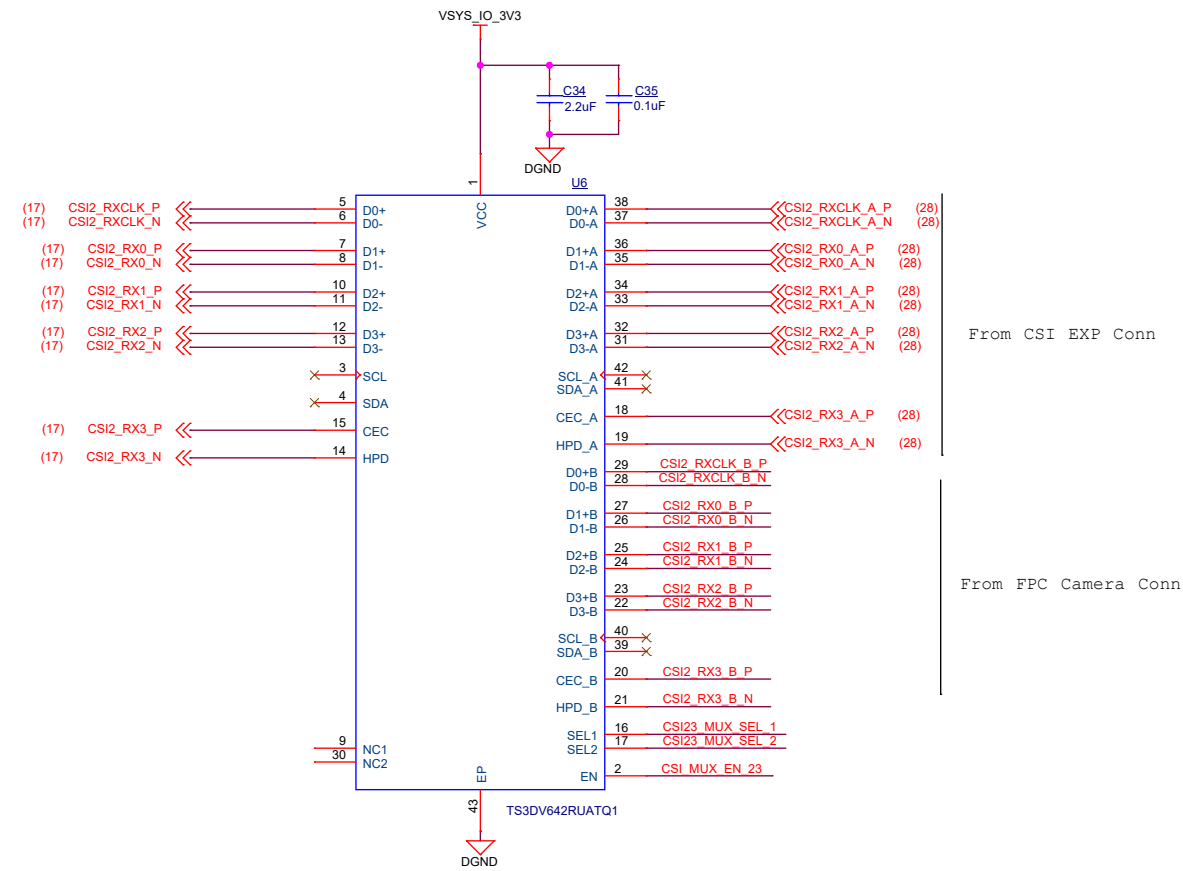
From CSI EXP Conn

From FPC Camera Conn

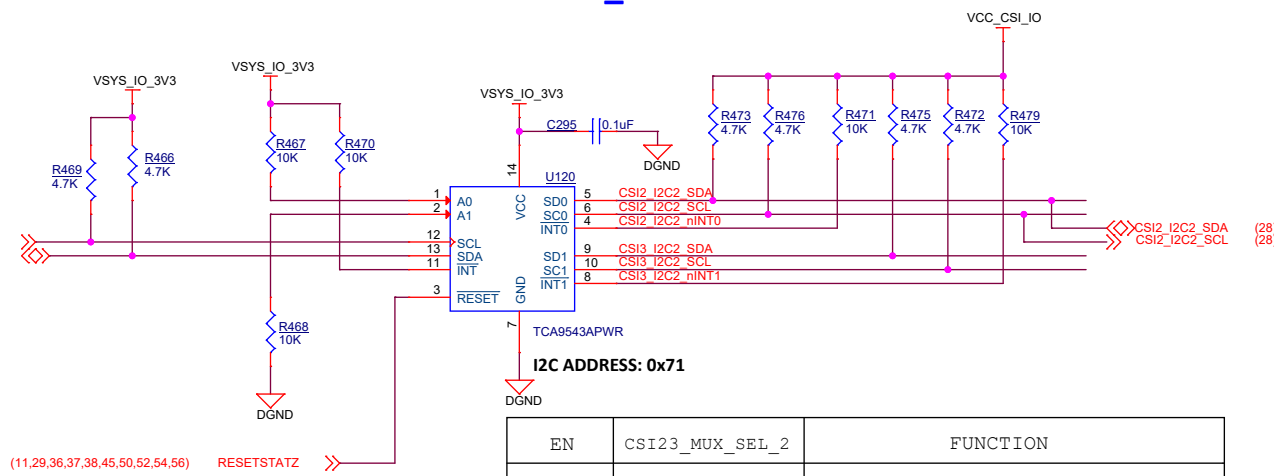
I2C SWITCH FOR SoC_I2C2



EN	CSI01_MUX_SEL_2	FUNCTION
HIGH	LOW	INPUT<-- A Port [CSI2 Connector] (default)
HIGH	HIGH	INPUT<--B port [FPC Camera Connector]
LOW	X	Disconnect

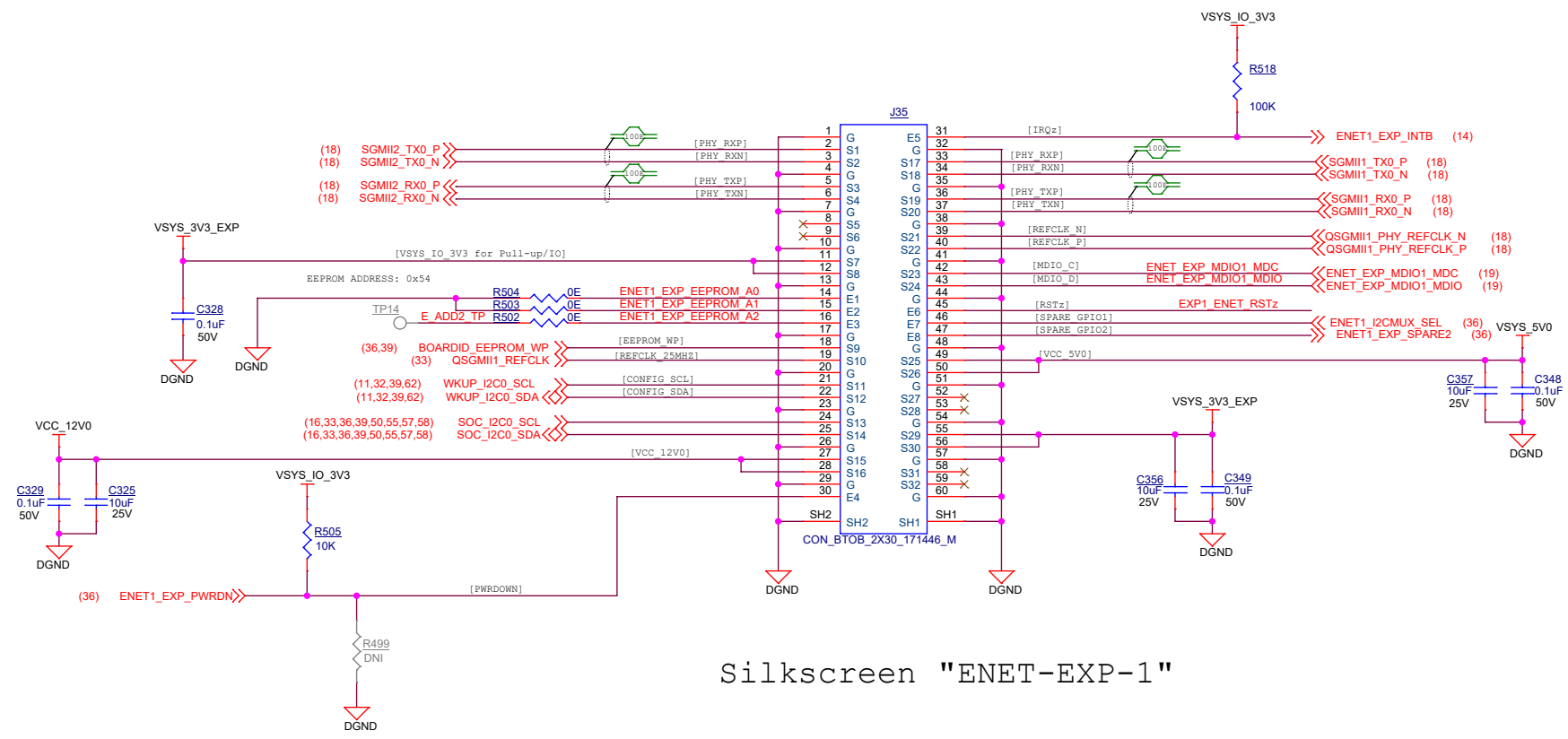


I2C SWITCH FOR SoC_I2C2

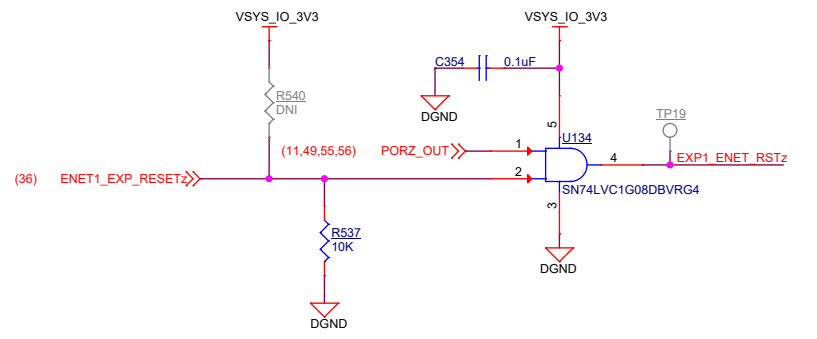


EN	CSI23_MUX_SEL_2	FUNCTION	
HIGH	LOW	INPUT<-- A Port [CSI2 Connector]	(default)
HIGH	HIGH	INPUT<--B port [FPC Camera Connector]	
LOW	X	Disconnect	

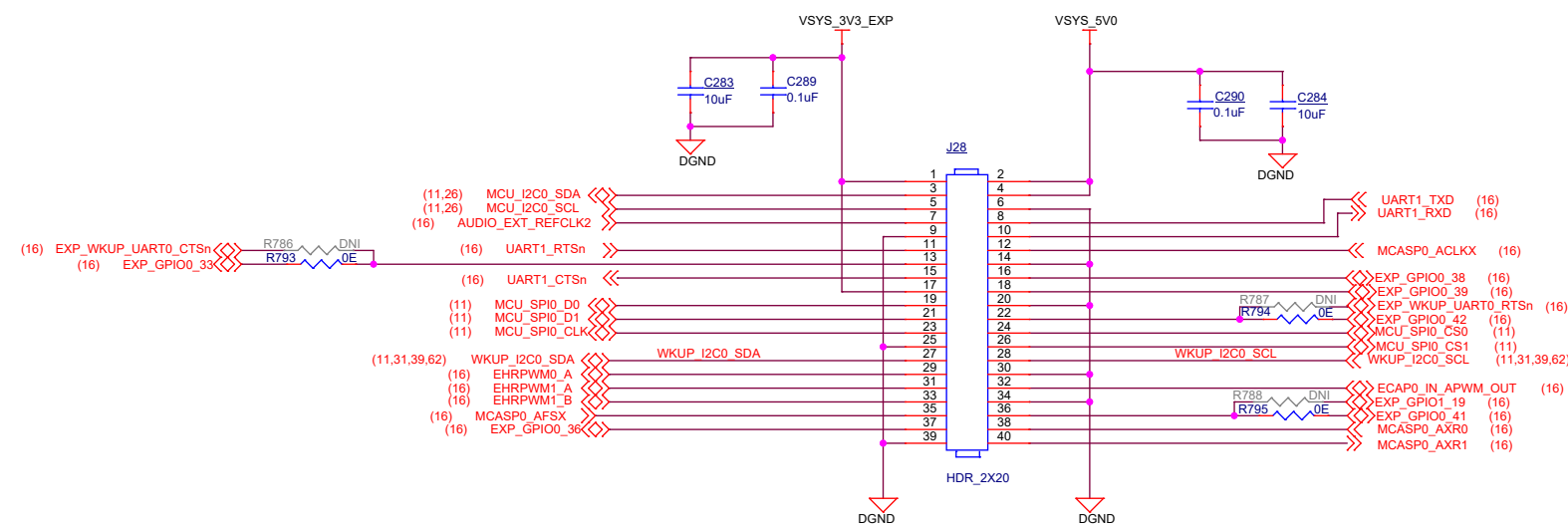
ENET EXPANSION CONNECTOR



Silkscreen "ENET-EXP-1"

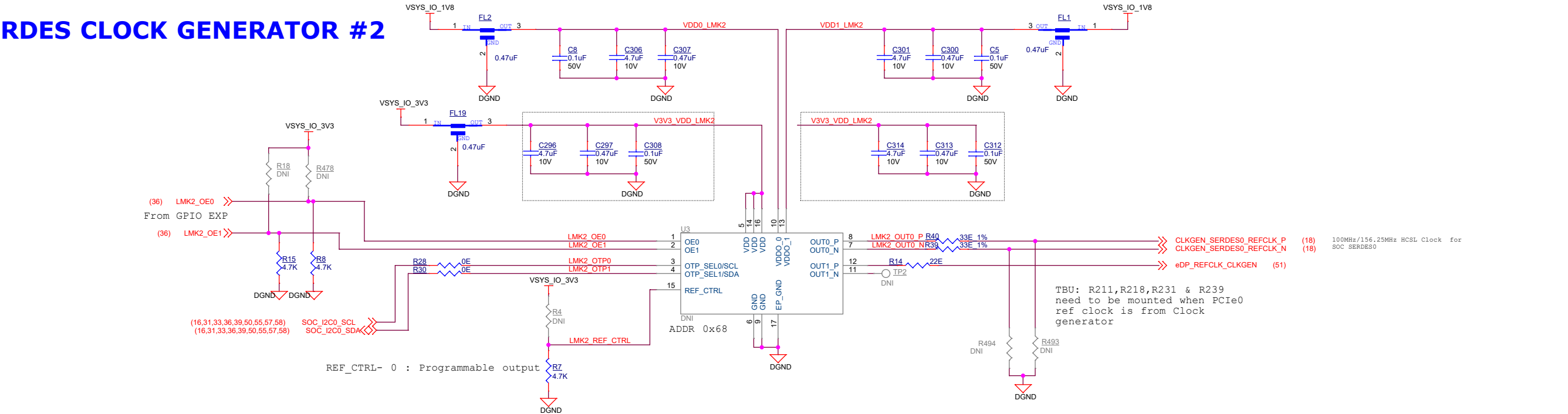


USER EXPANSION CONNECTOR



Silk Screen "40p EXP HDR"

SERDES CLOCK GENERATOR #2

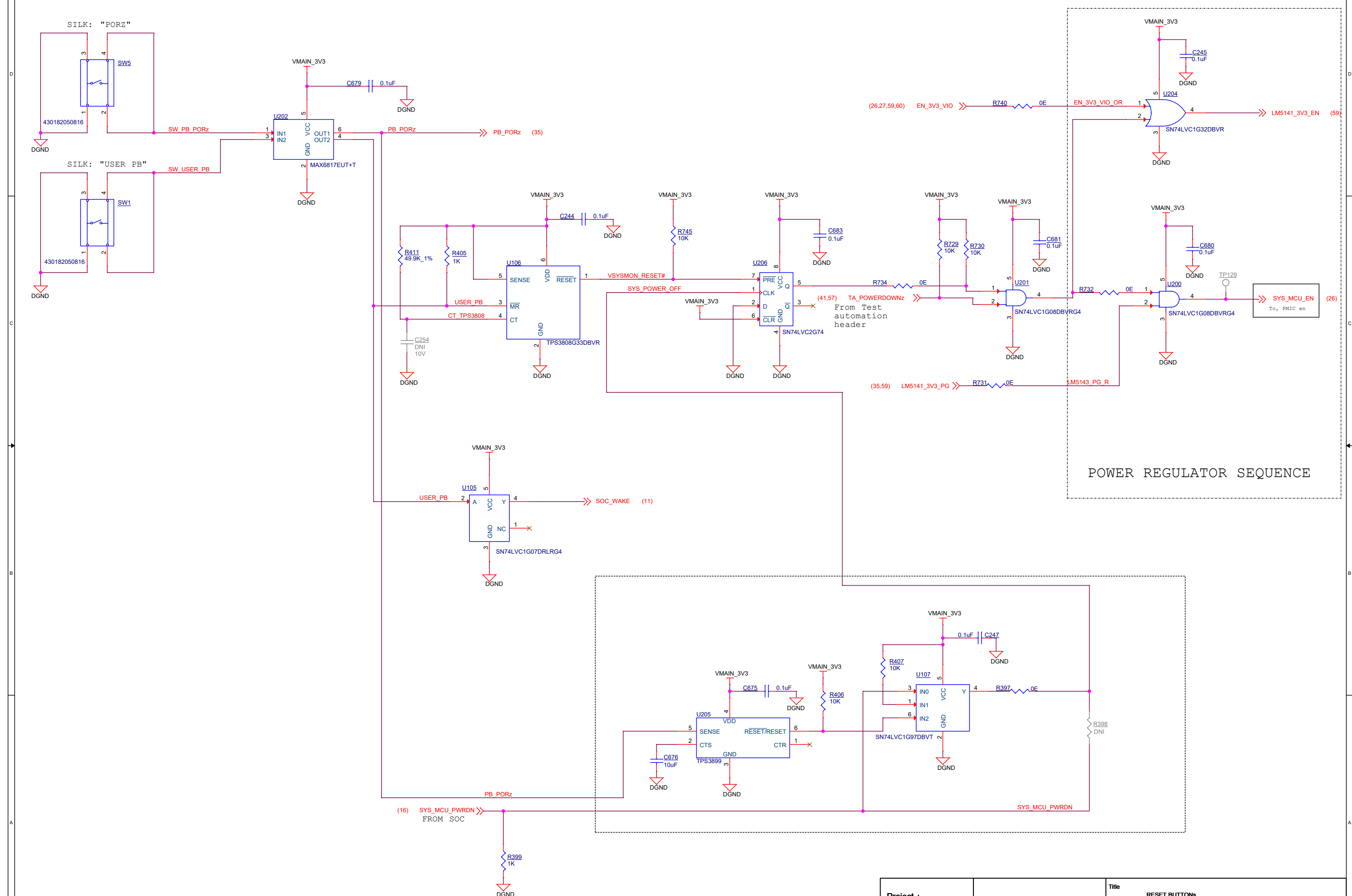


Project : J7 EVM

TEXAS INSTRUMENTS

Title		
SERDES CLOCK GENERATOR #1		
Size	Rev	
C	PROC170 002 EVM	E3B
Date:	Friday, August 30, 2024	Sheet 33 of 68

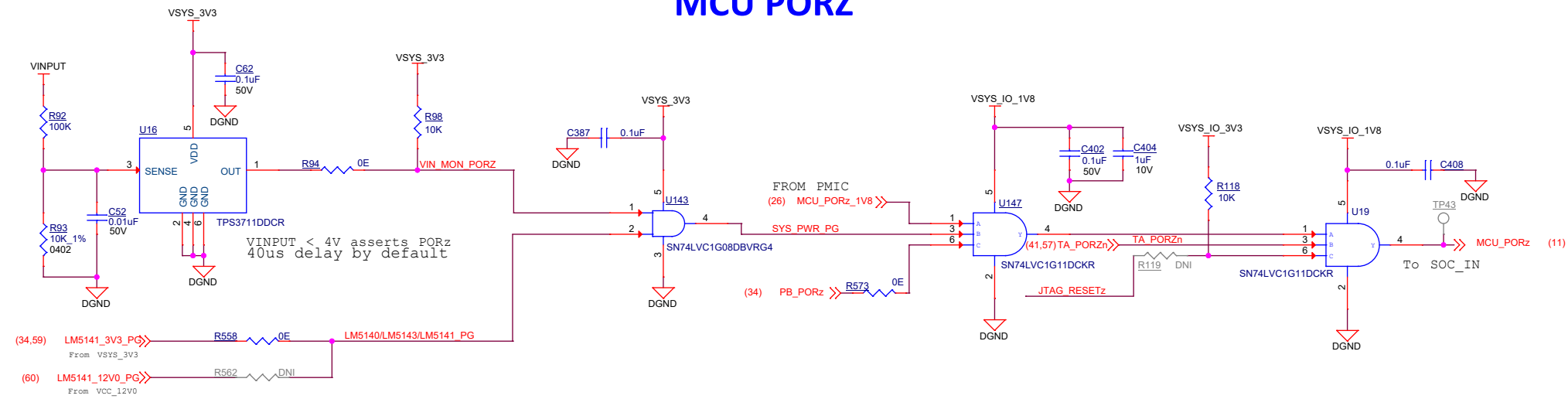
RESET BUTTONs



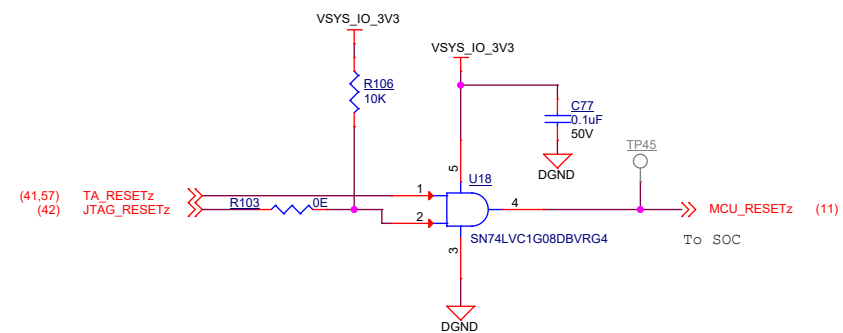
RESET INPUTS

Under Voltage Monitor (VINPUT)

MCU PORZ



MCU_RESET



Project : J7 EVM

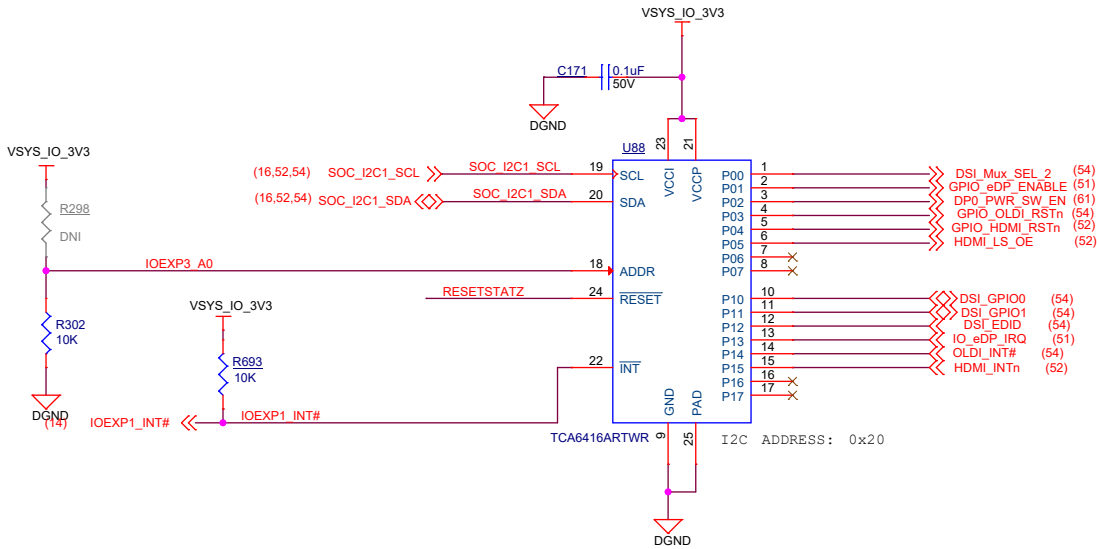
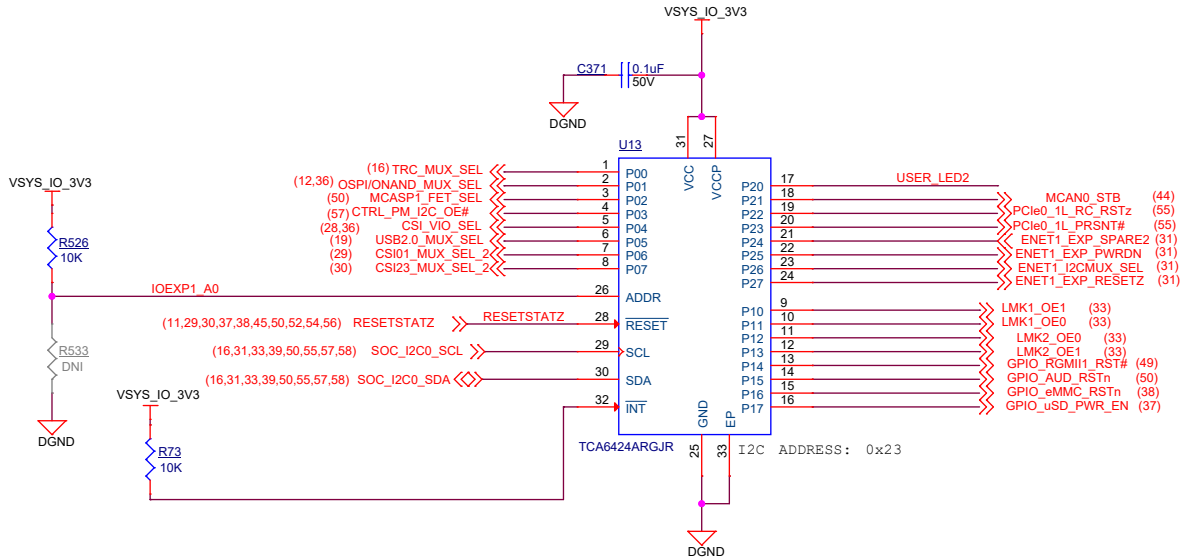


Title	RESET INPUTS
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Size	PROC170 002 EVM	Rev
C		E3B
Date:	Friday, August 30, 2024	Sheet 35 of 68

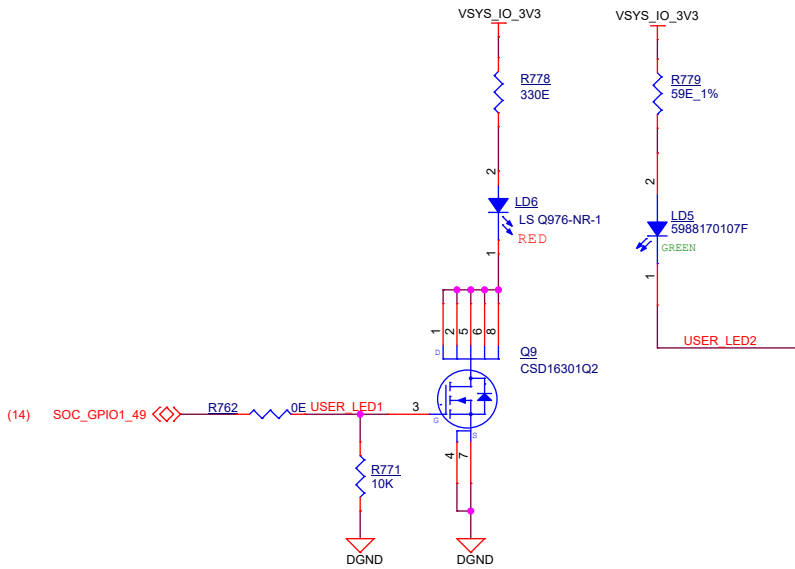
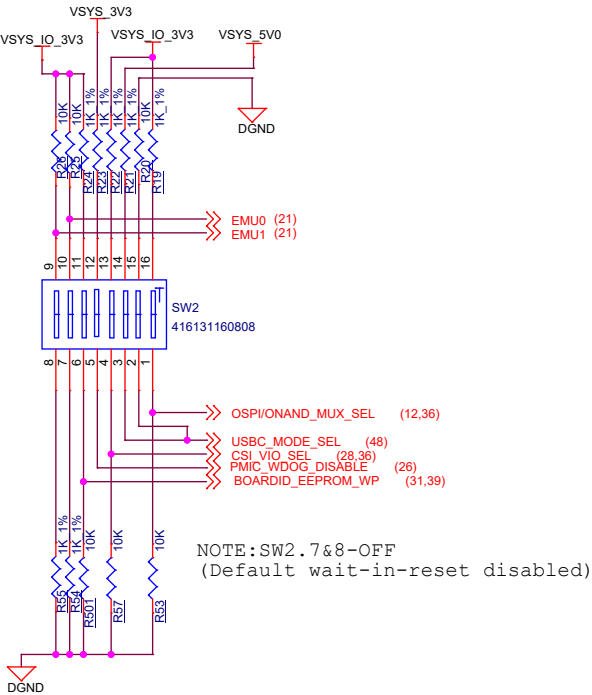
GPIO EXPANDERS

I2C GPIO EXPANDER1

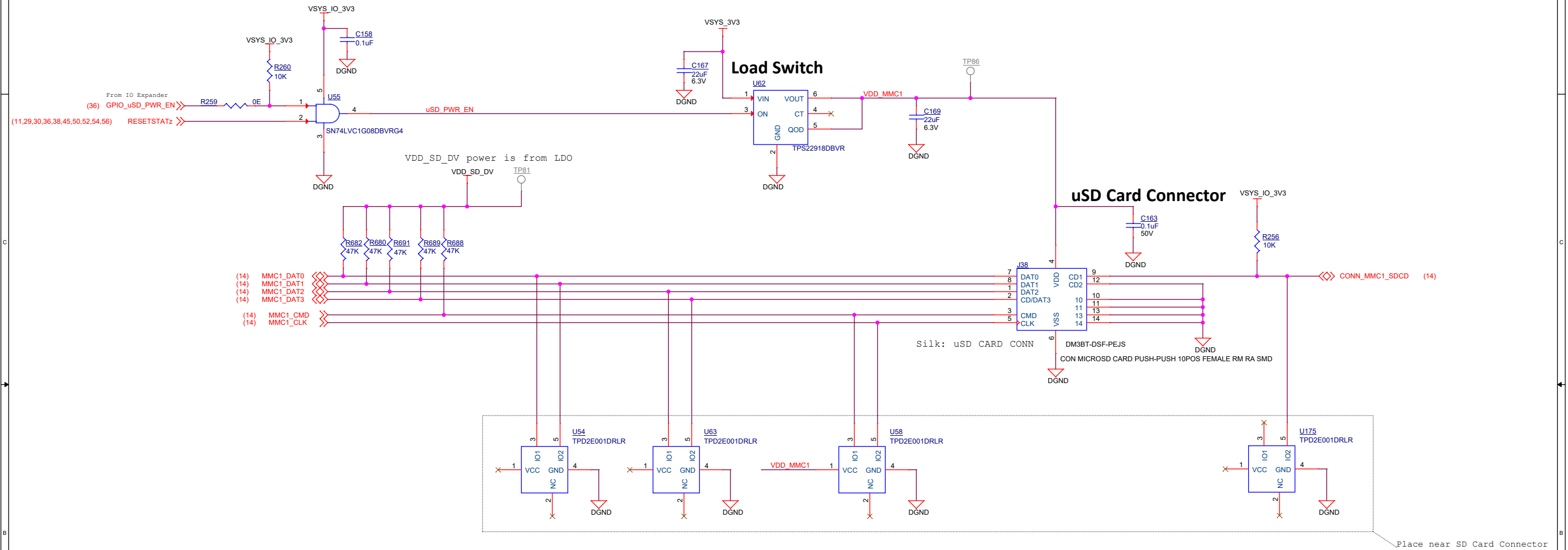


SWITCH (SW2.4)	Description
CLOSED	Disables WDog, high latched at Pwr-Up
OPEN (Default)	Enables WDog, low latched at Pwr-Up

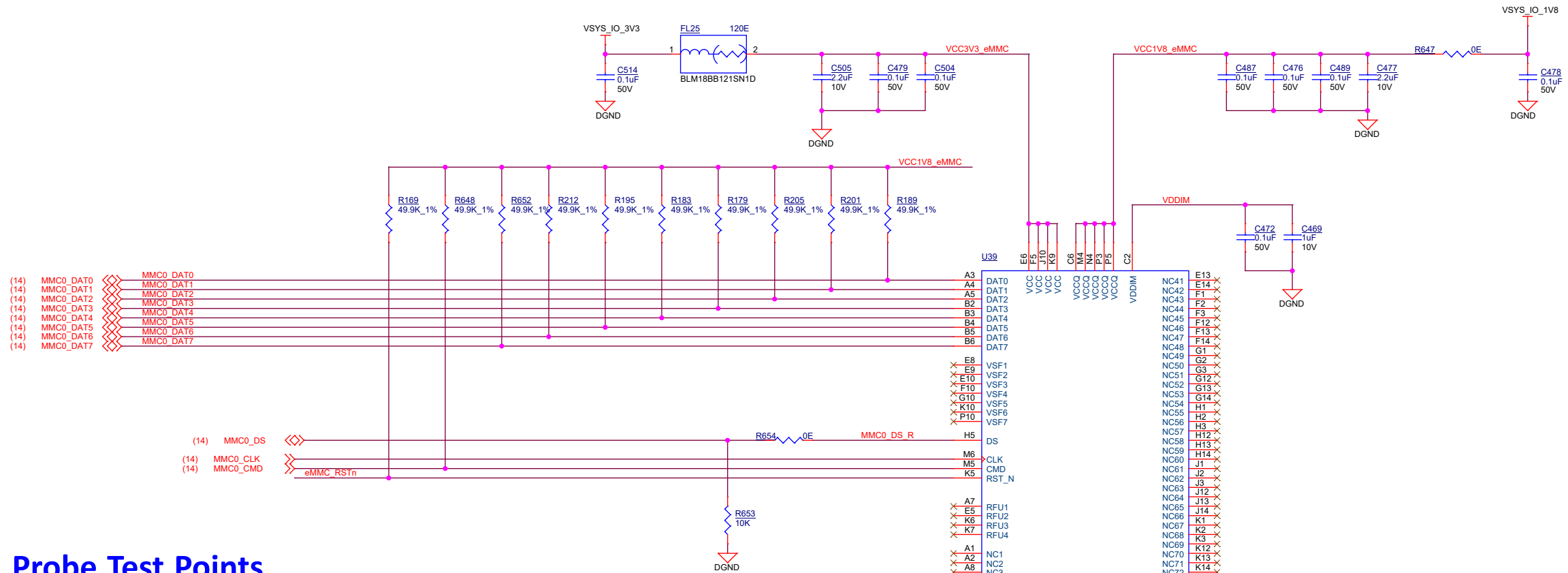
CONFIG DIP SWITCH



Micro SD CARD INTERFACE



eMMC FLASH

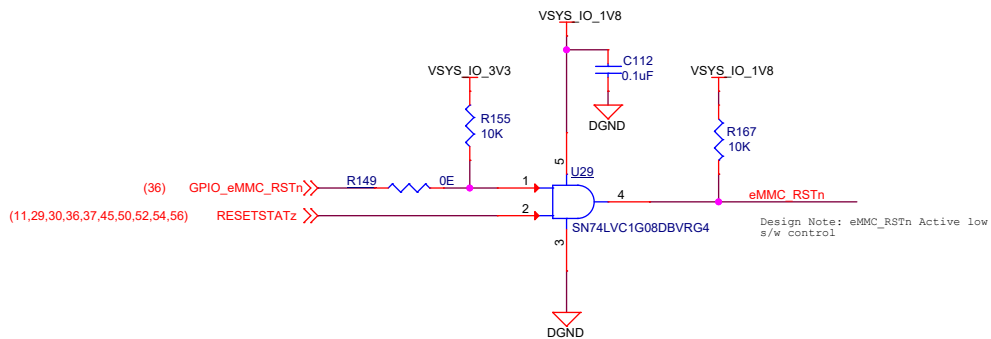


Via Probe Test Points

Place Near eMMC side

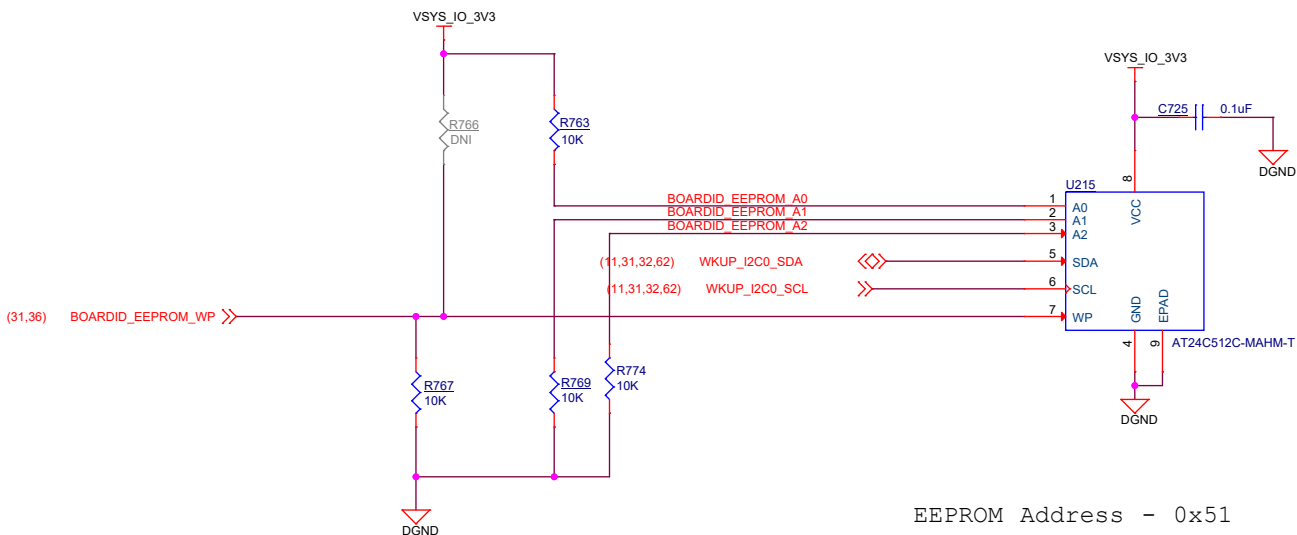
TP63	DNI	MMC0_DAT0
TP67	DNI	MMC0_DAT1
TP69	DNI	MMC0_DAT2
TP59	DNI	MMC0_DAT3
TP61	DNI	MMC0_DAT4
TP65	DNI	MMC0_DAT5
TP70	DNI	MMC0_DAT6
TP161	DNI	MMC0_DAT7
TP159	DNI	MMC0_DS_R
TP56	DNI	MMC0_CLK
TP160	DNI	MMC0_CMD

eMMC FLASH RESET



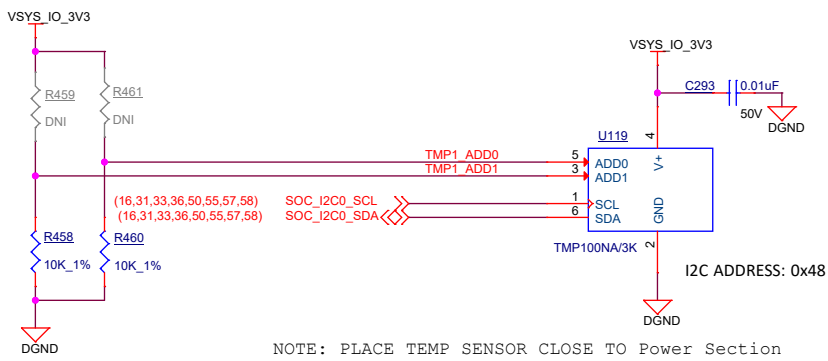
I2C for BOARD ID EEPROMs

BOARD ID EEPROM

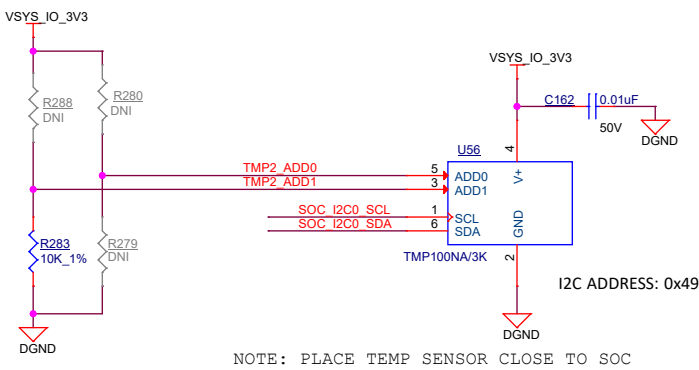


EEPROM Address - 0x51

TEMPERATURE SENSORS
(TI EVM Only)

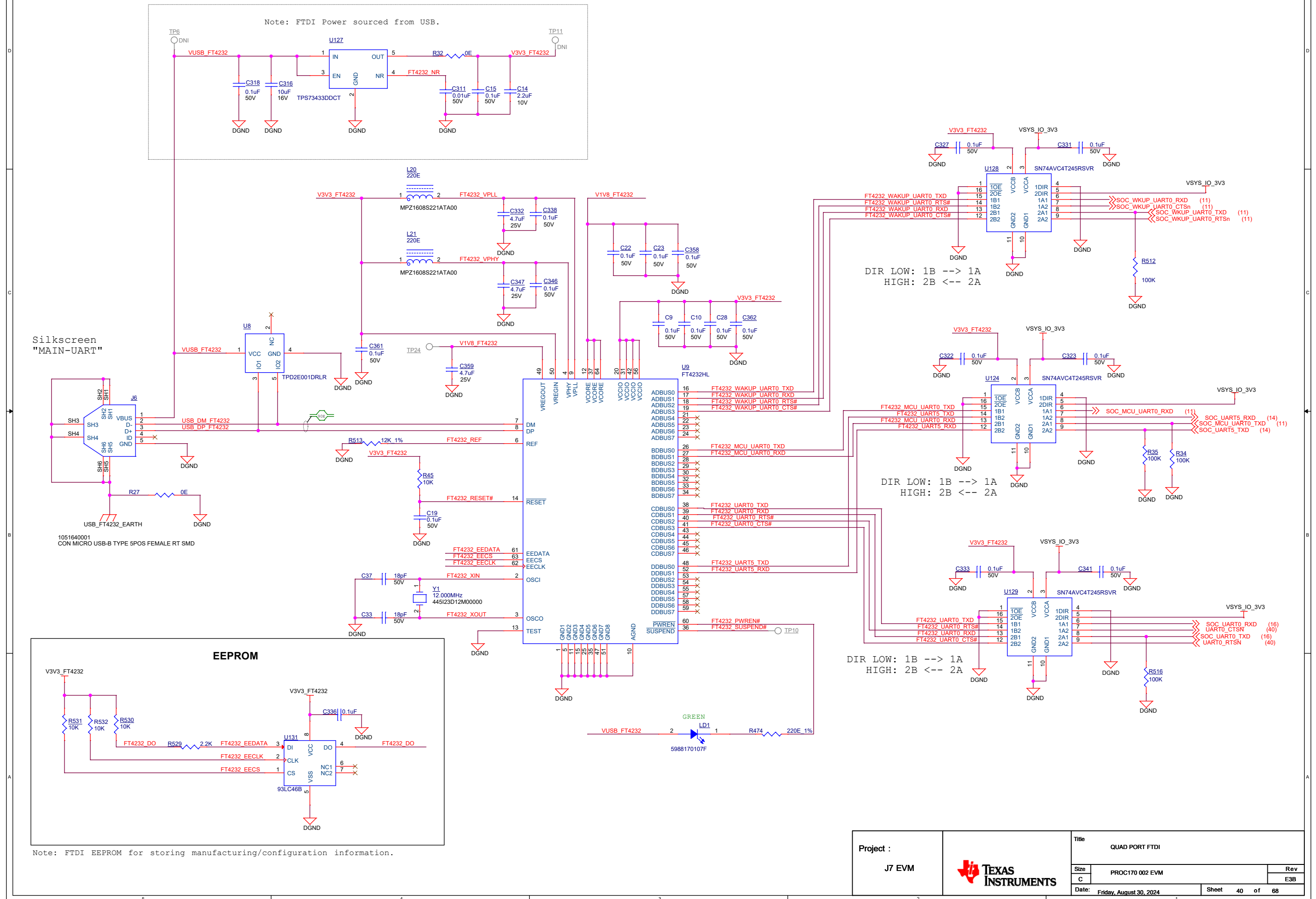


NOTE: PLACE TEMP SENSOR CLOSE TO Power Section



NOTE: PLACE TEMP SENSOR CLOSE TO SOC

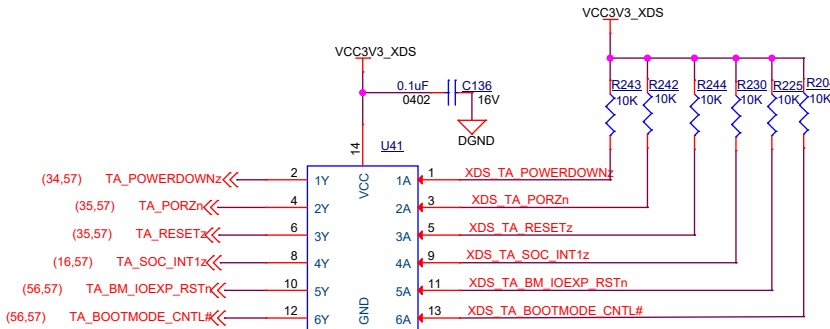
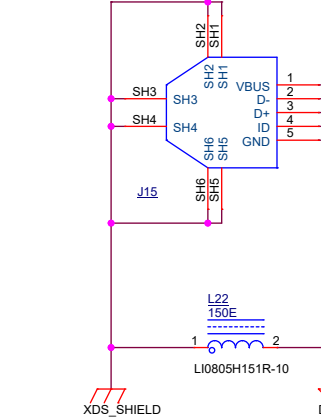
QUAD PORT FTDI



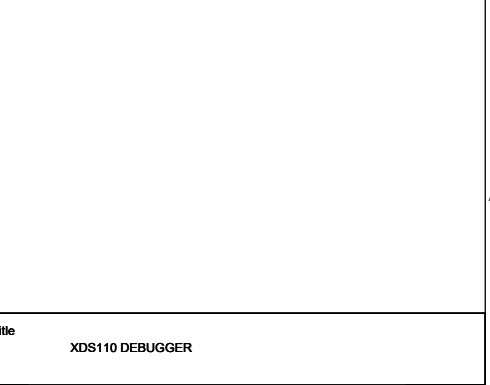
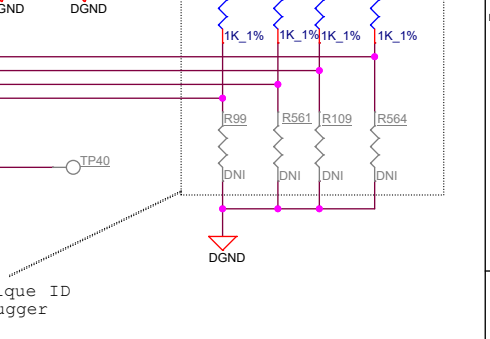
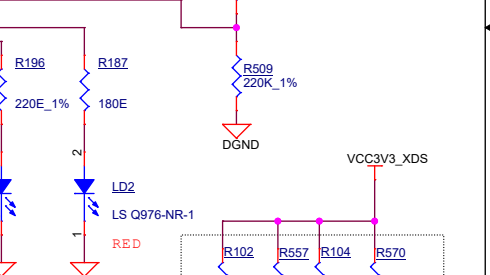
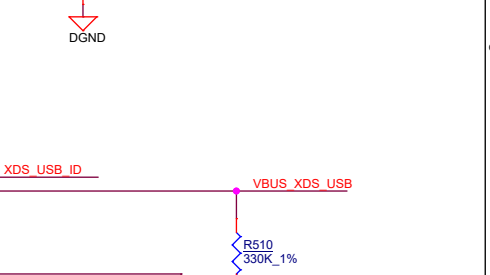
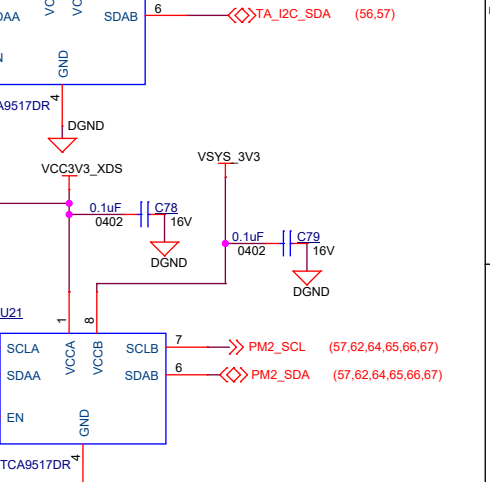
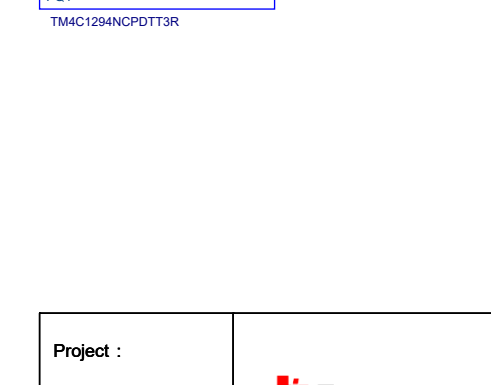
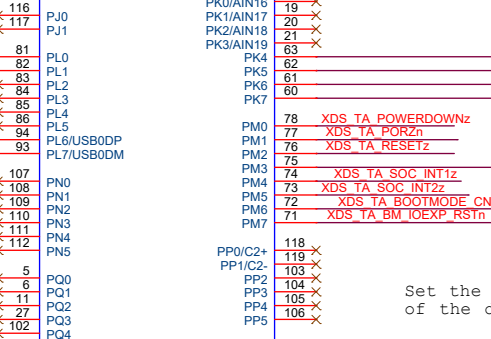
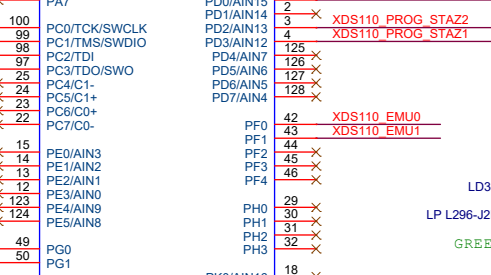
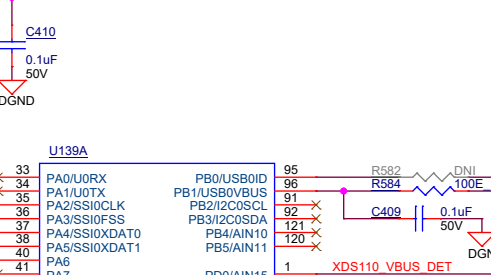
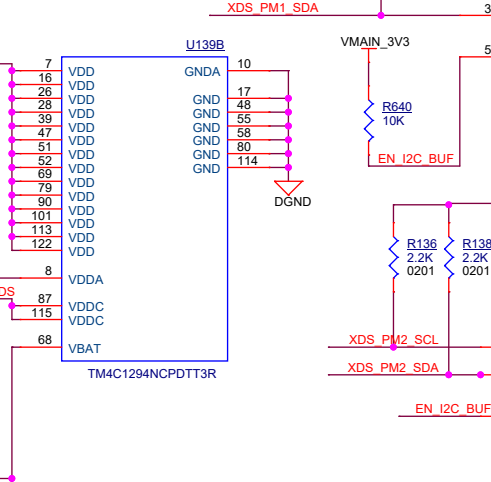
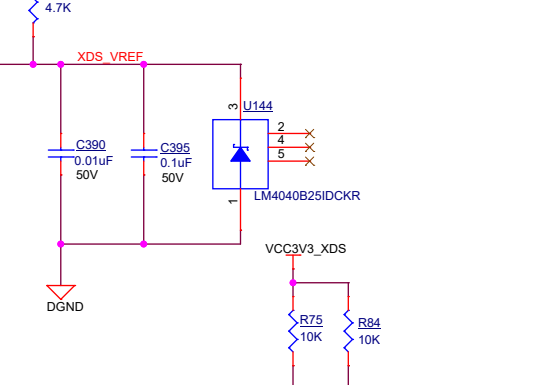
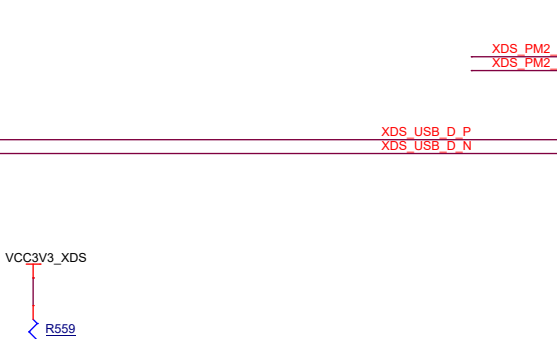
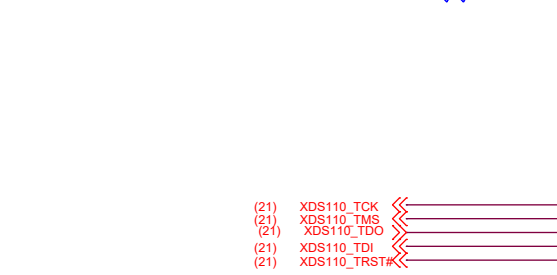
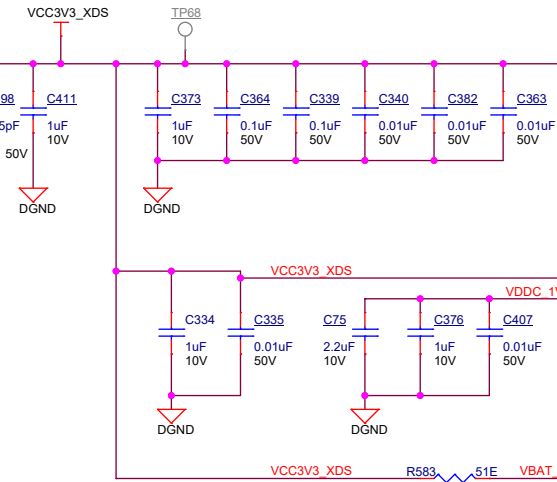
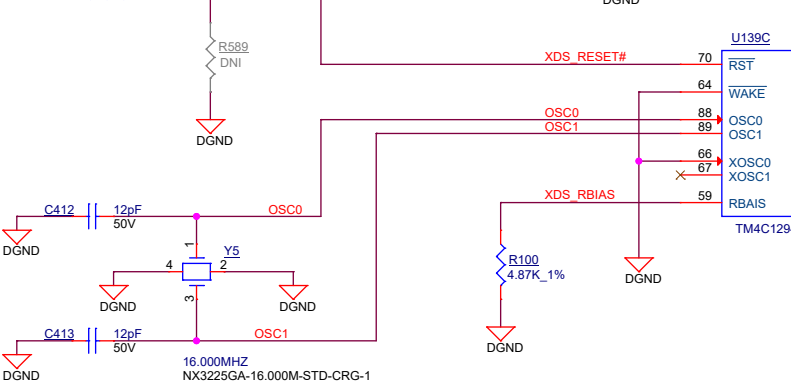
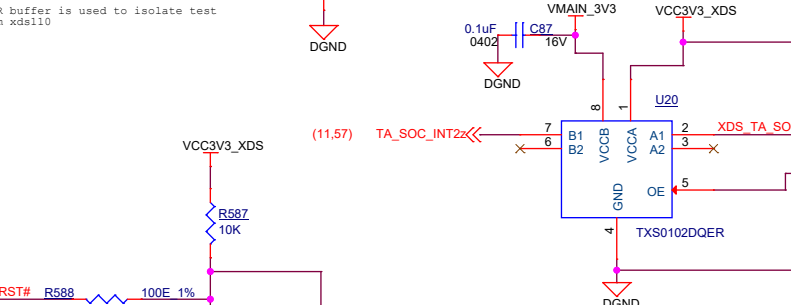
XDS110 DEBUGGER

Silkscreen "XDS110"

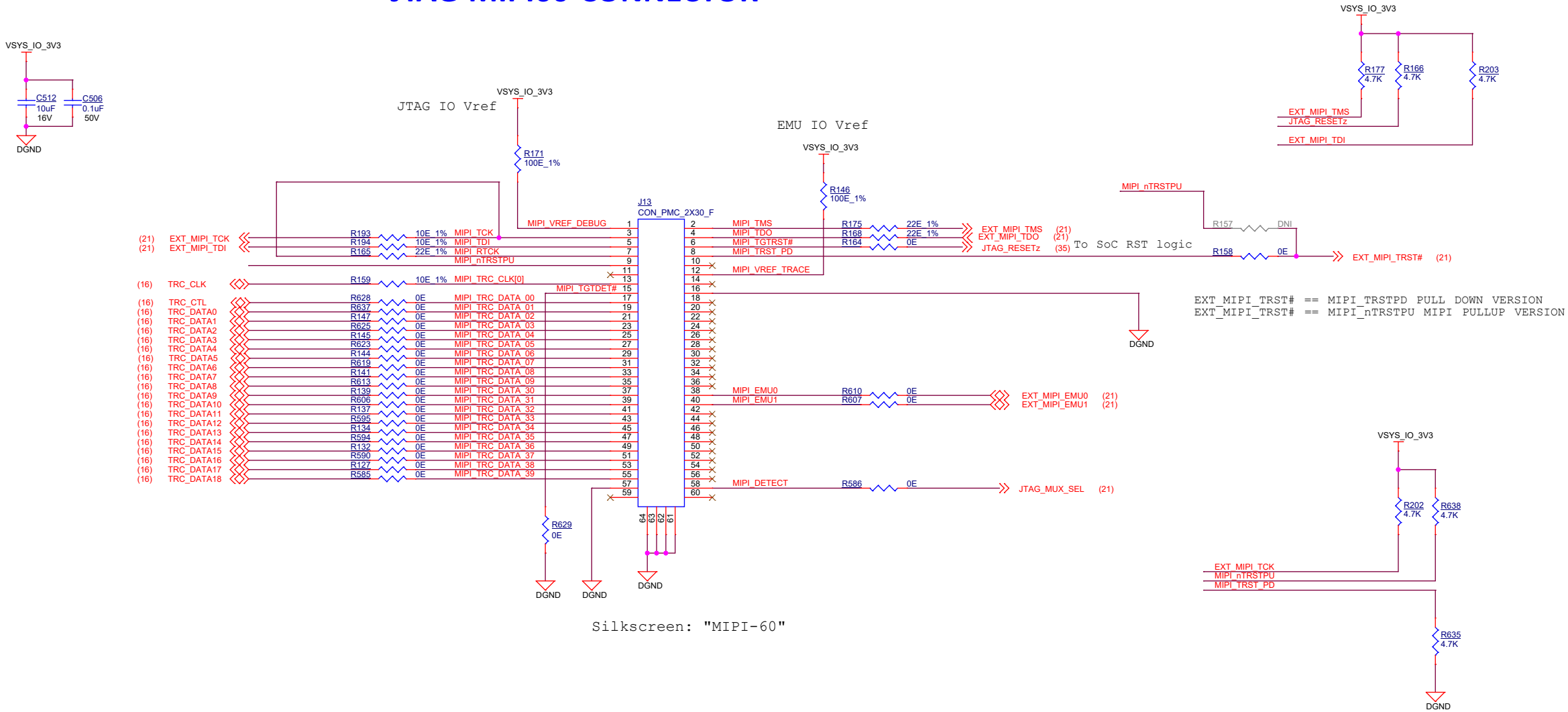
1051640001
CON MICRO USB-B TYPE 5POS FEMALE RT SMD



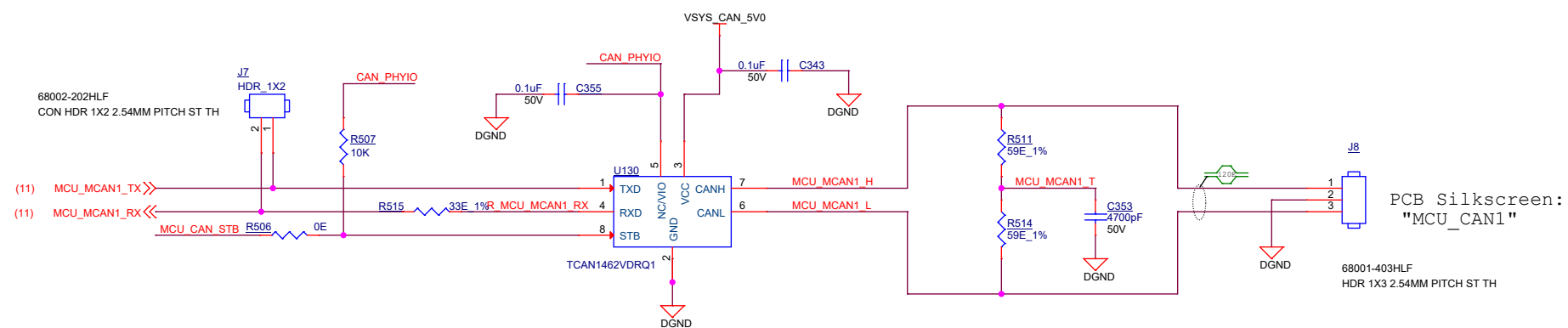
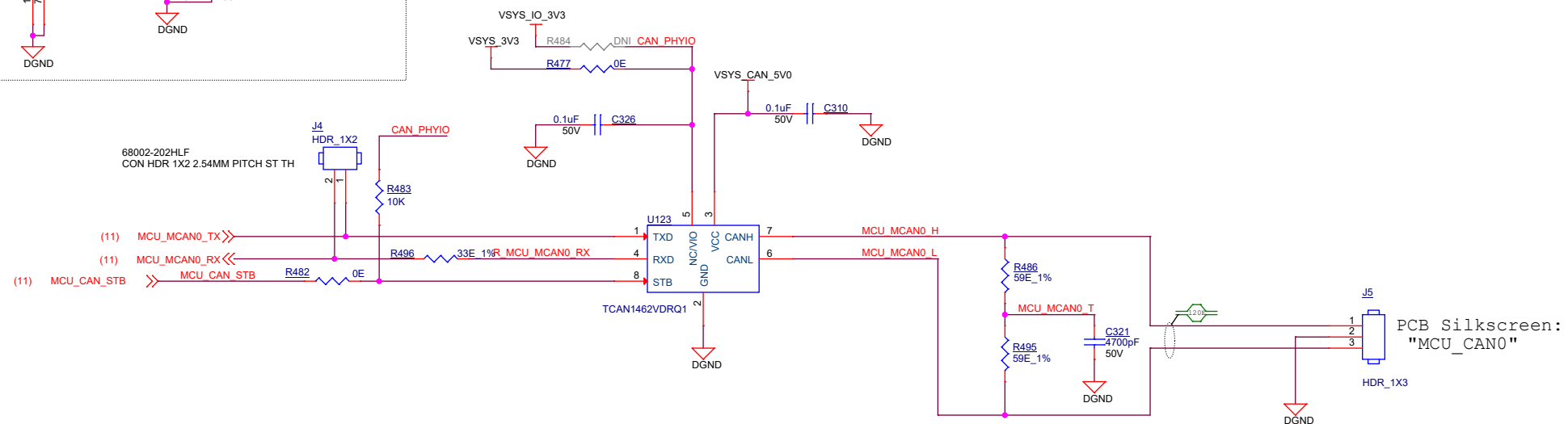
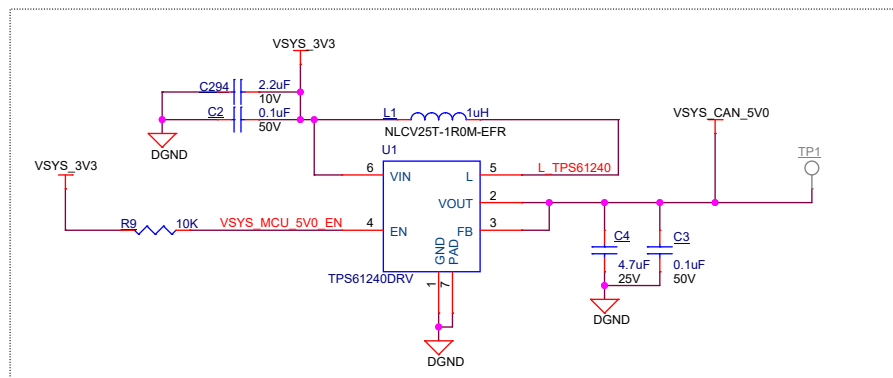
SN74AVC87245PWR buffer is used to isolate test automation from xds110



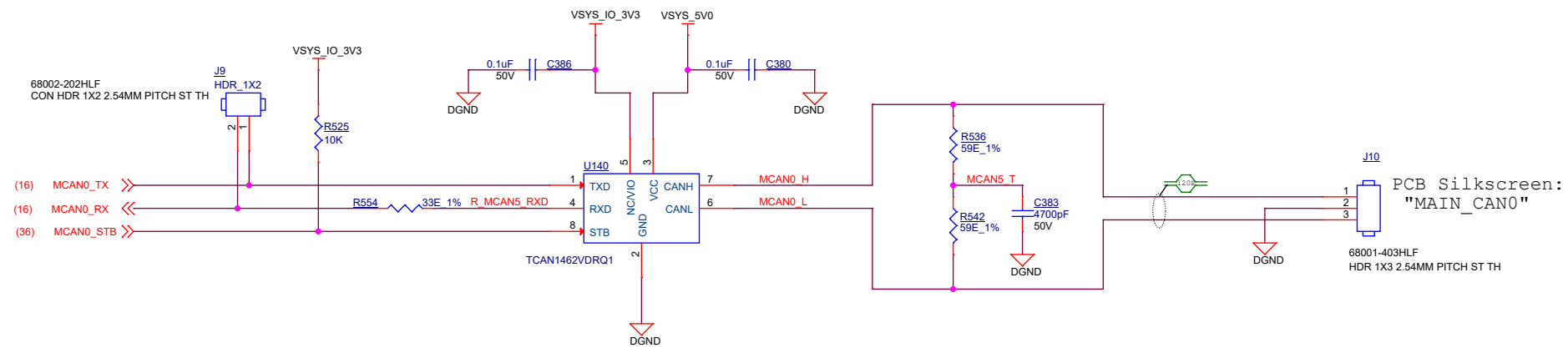
JTAG MIPI60 CONNECTOR



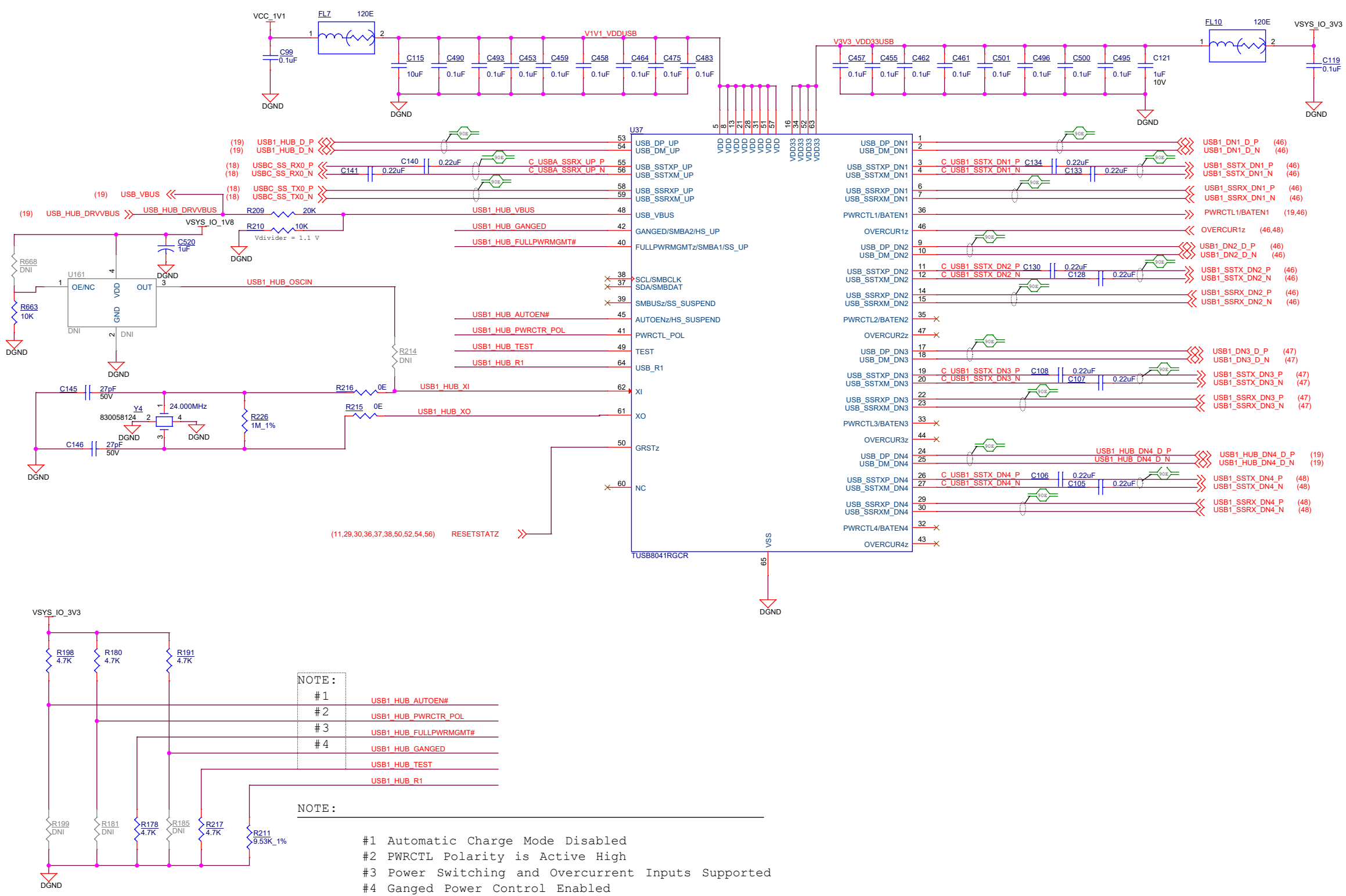
CAN TRANSCEIVERS #1-MCU DOMAIN



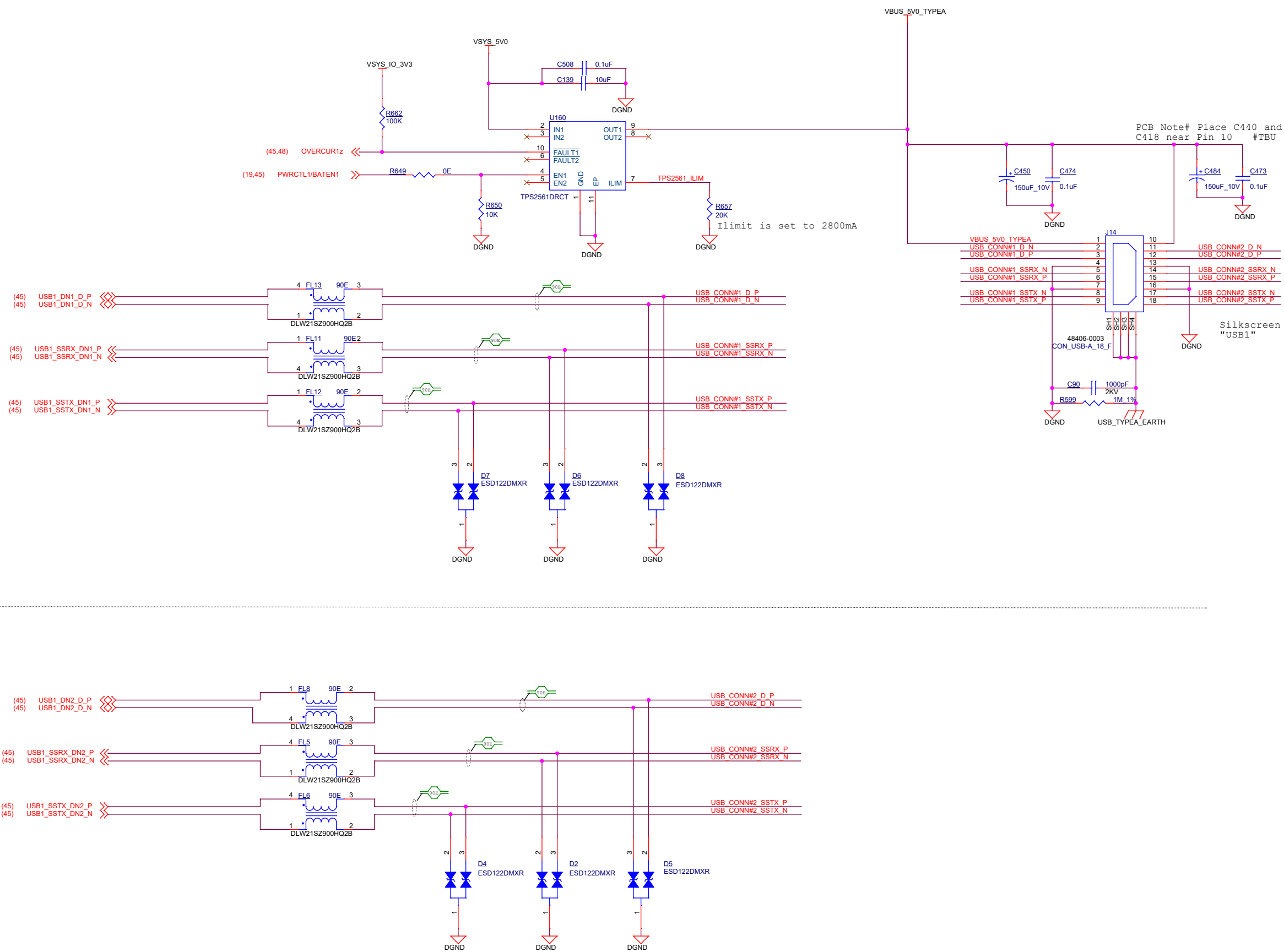
CAN TRANSCEIVERS #2-MAIN DOMAIN



USB3.0 HUB



USB 3.0 TYPE-A CONNECTORS - 1



Project :

J7 EVM



Title
USB 2.0 TYPE-A CONNECTORS

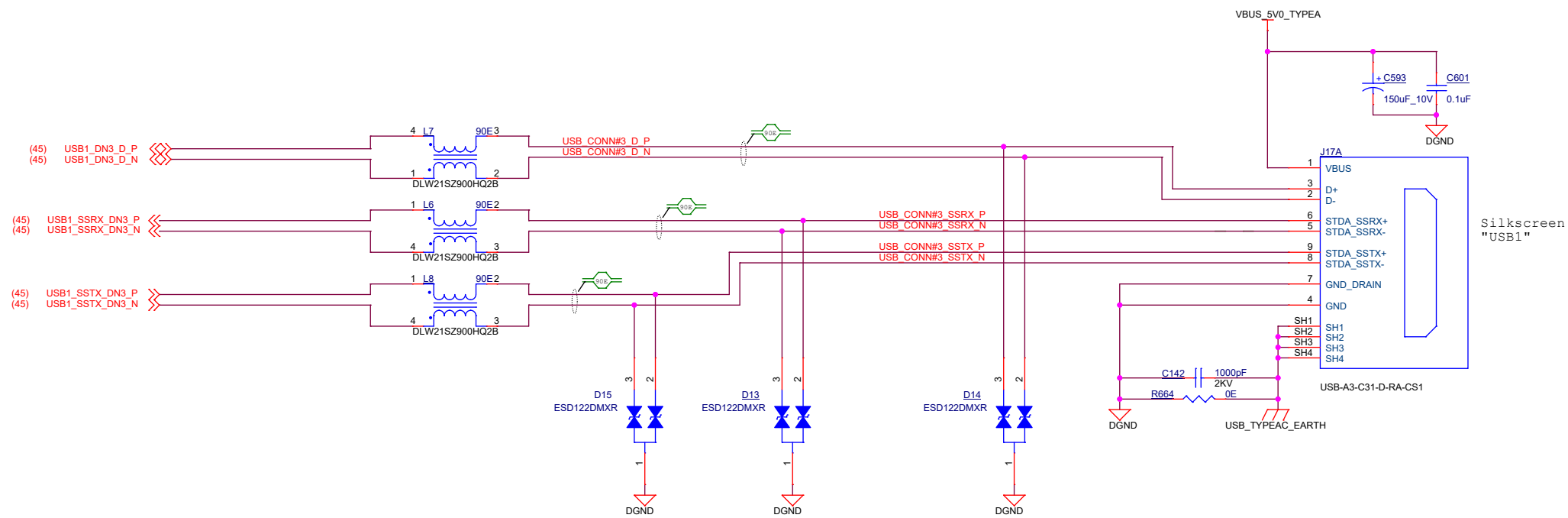
Size
C
PROC170 002 EVM

Date: Friday, August 30, 2024

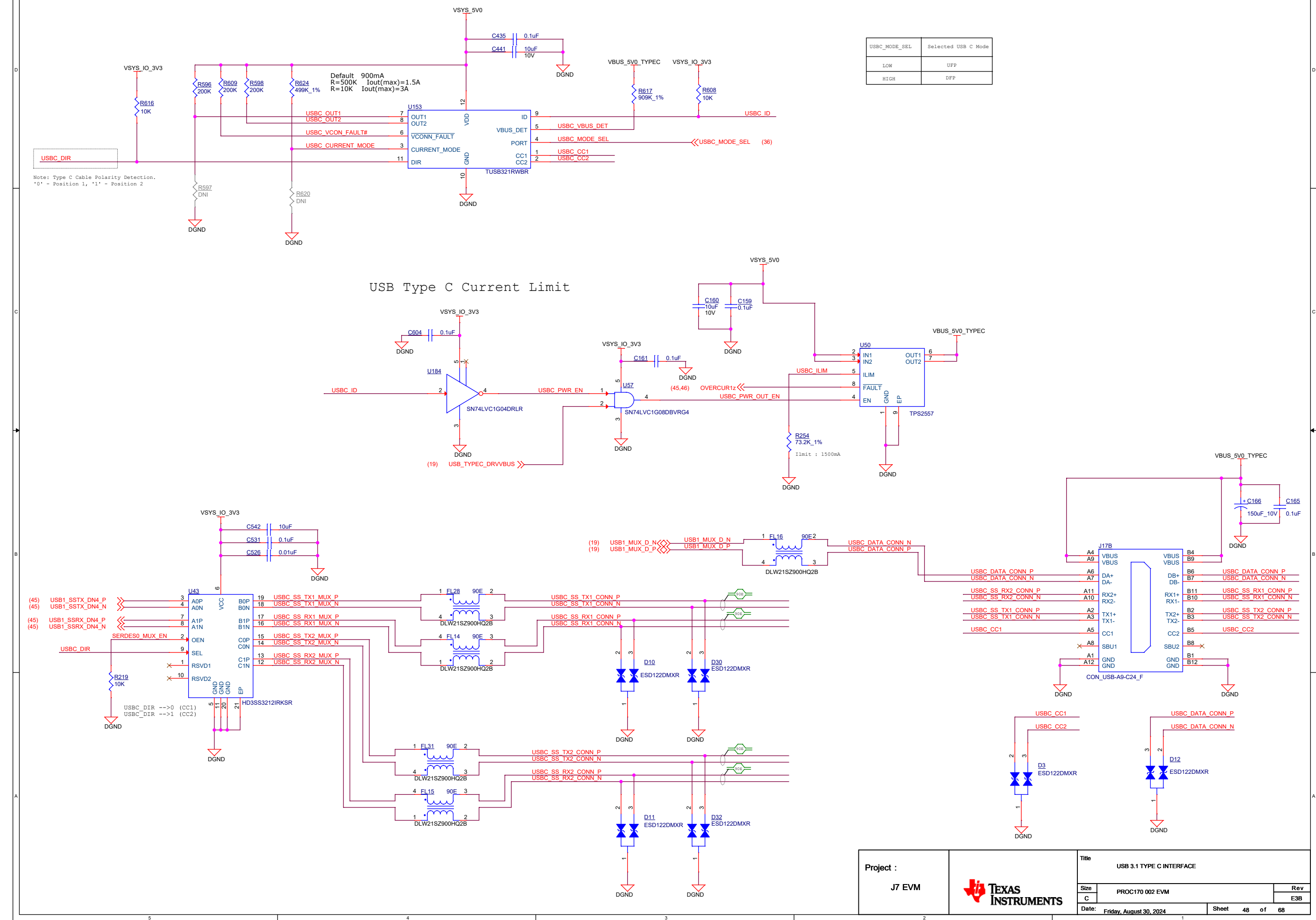
Sheet 46 of 68

Rev
E3B

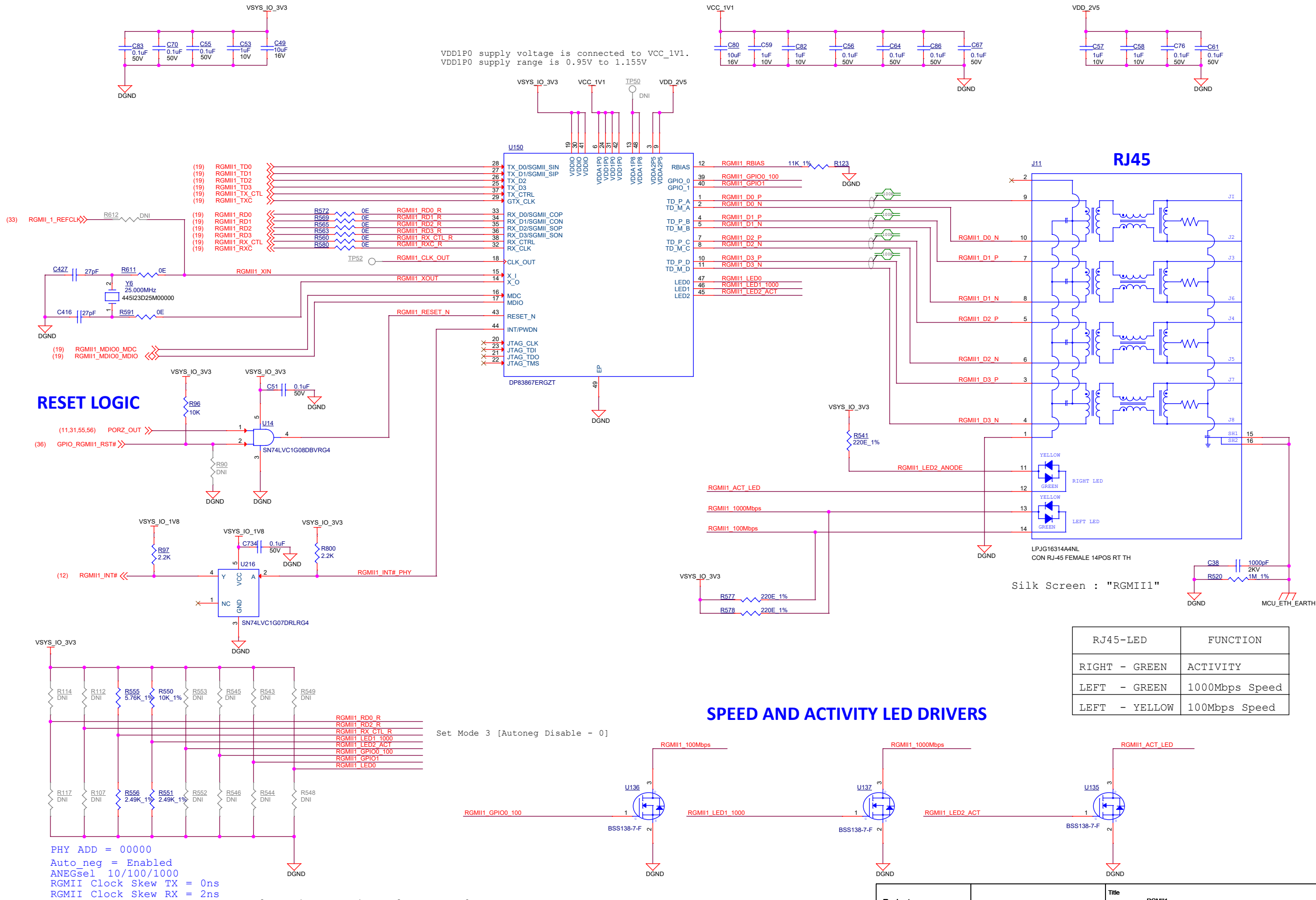
USB 3.0 TYPE-A CONNECTORS - 2



USB 3.0 TYPE C INTERFACE



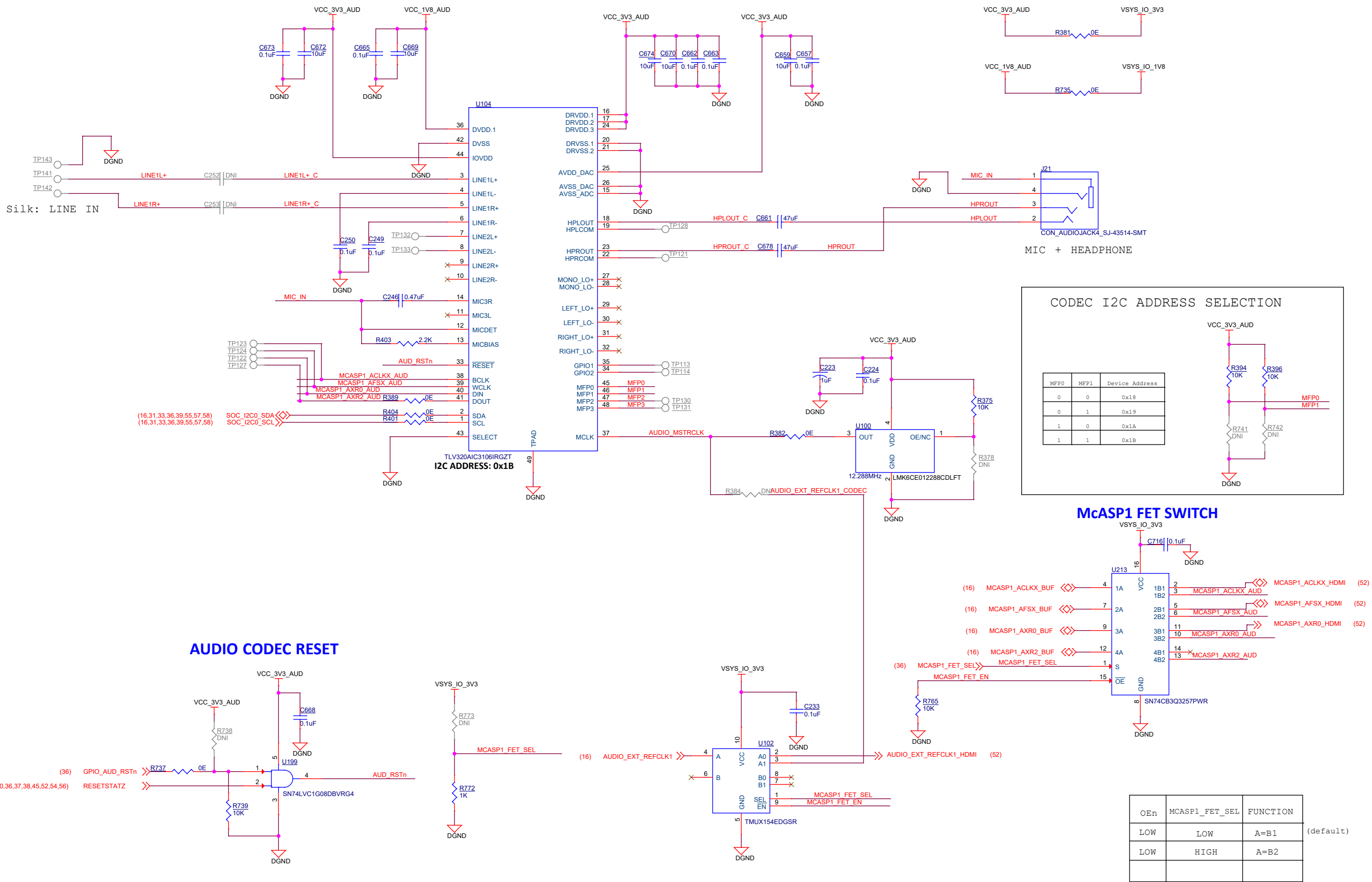
RGMII1



RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

SPEED AND ACTIVITY LED DRIVERS

AUDIO CODEC



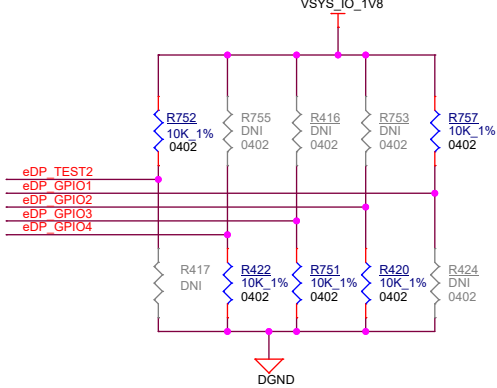
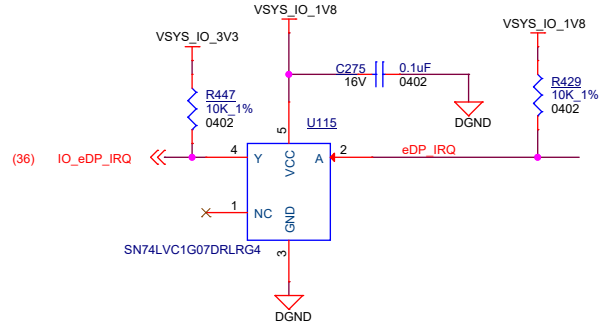
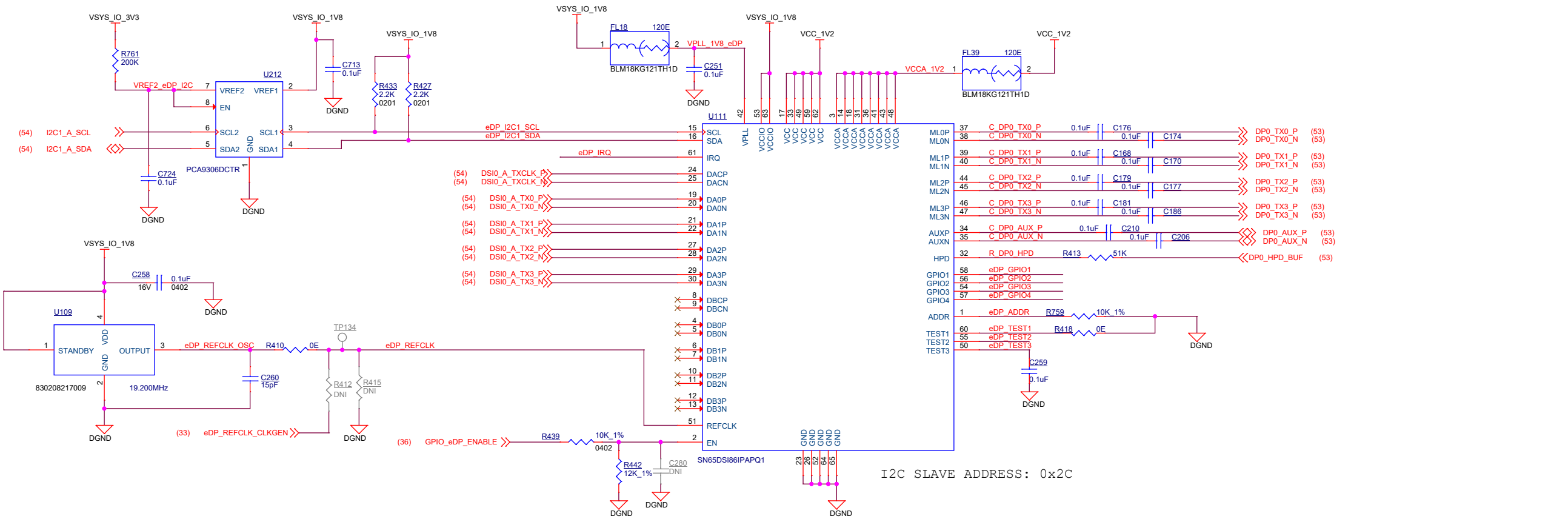
CODEC I2C ADDRESS SELECTION

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B

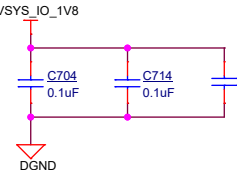
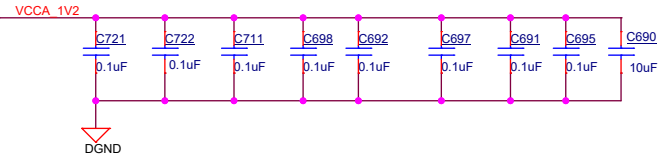
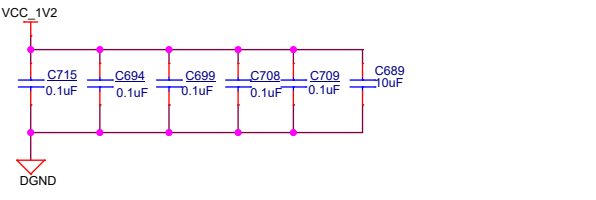
McASP1 FET SWITCH

OEn	McASP1_FET_SEL	FUNCTION
LOW	LOW	A=B1 (default)
LOW	HIGH	A=B2

DSI to eDP Bridge

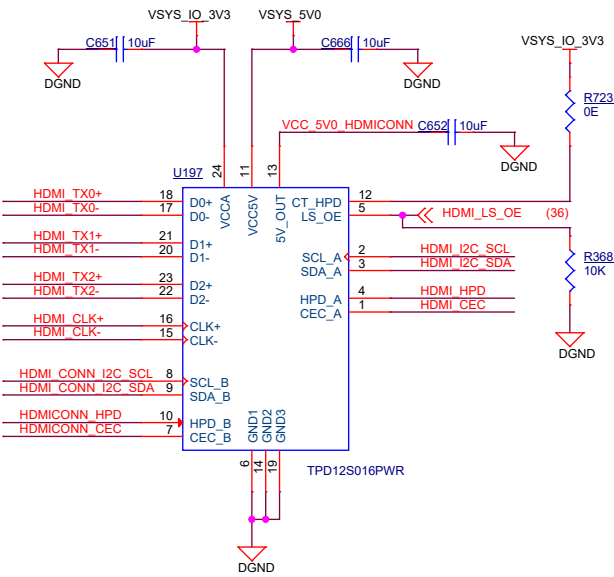


GPIO[3:1] is set as 3'b001 for 19.2MHz External Refclk

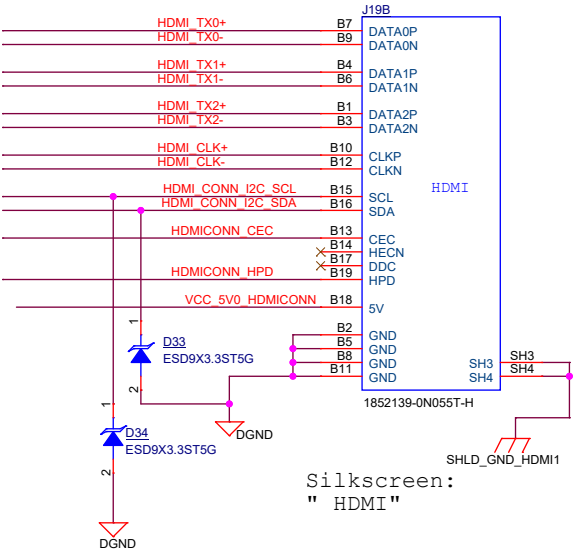


HDMI INTERFACE

HDMI ESD DEVICE

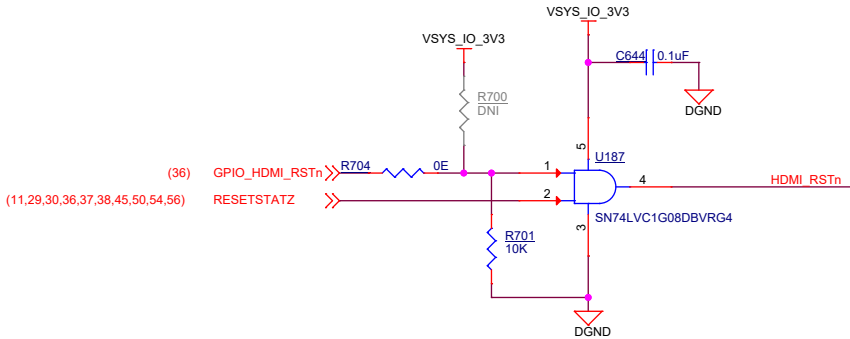


NOTE:
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.



Silkscreen:
" HDMI "

HDMI RESET



Project :

J7 EVM



Title
SOC DIGITAL IO & SUPPORT POWER 2

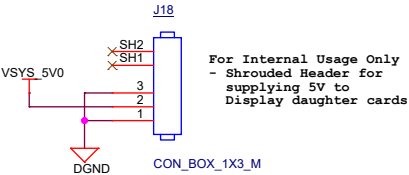
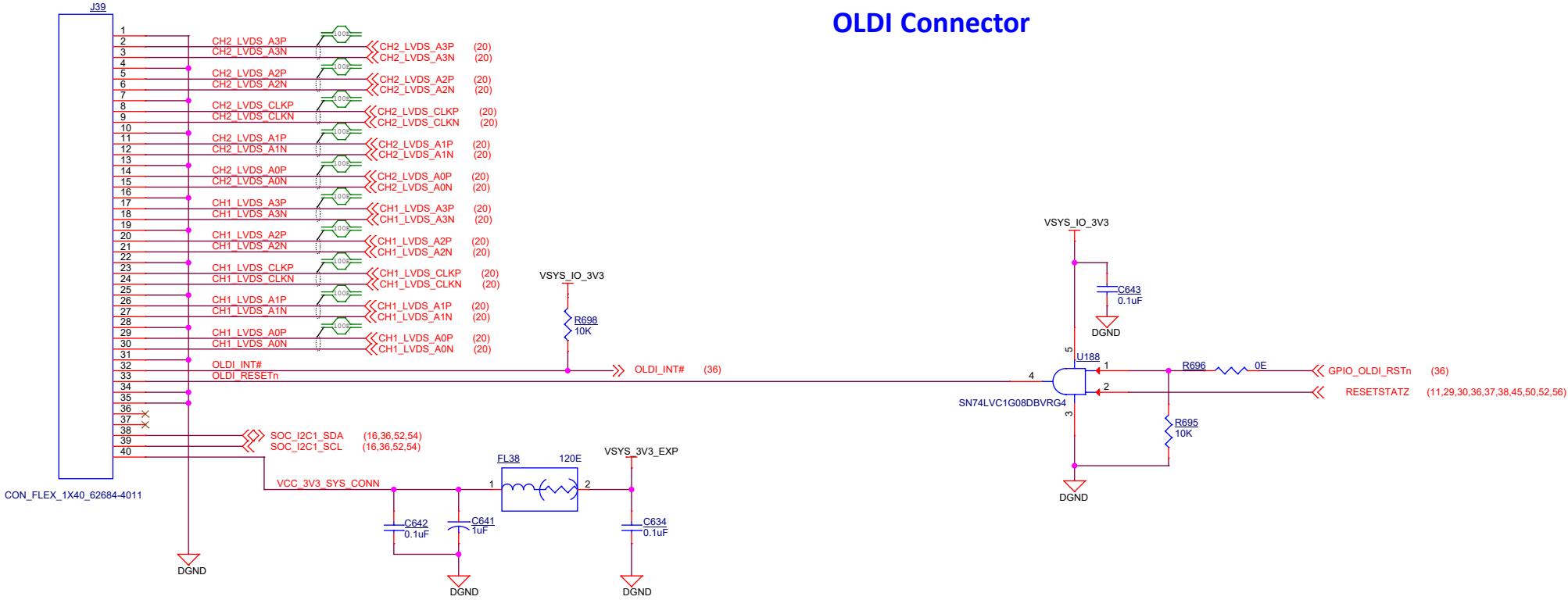
Size
PROC170 002 EVM

C
Date: Friday, August 30, 2024

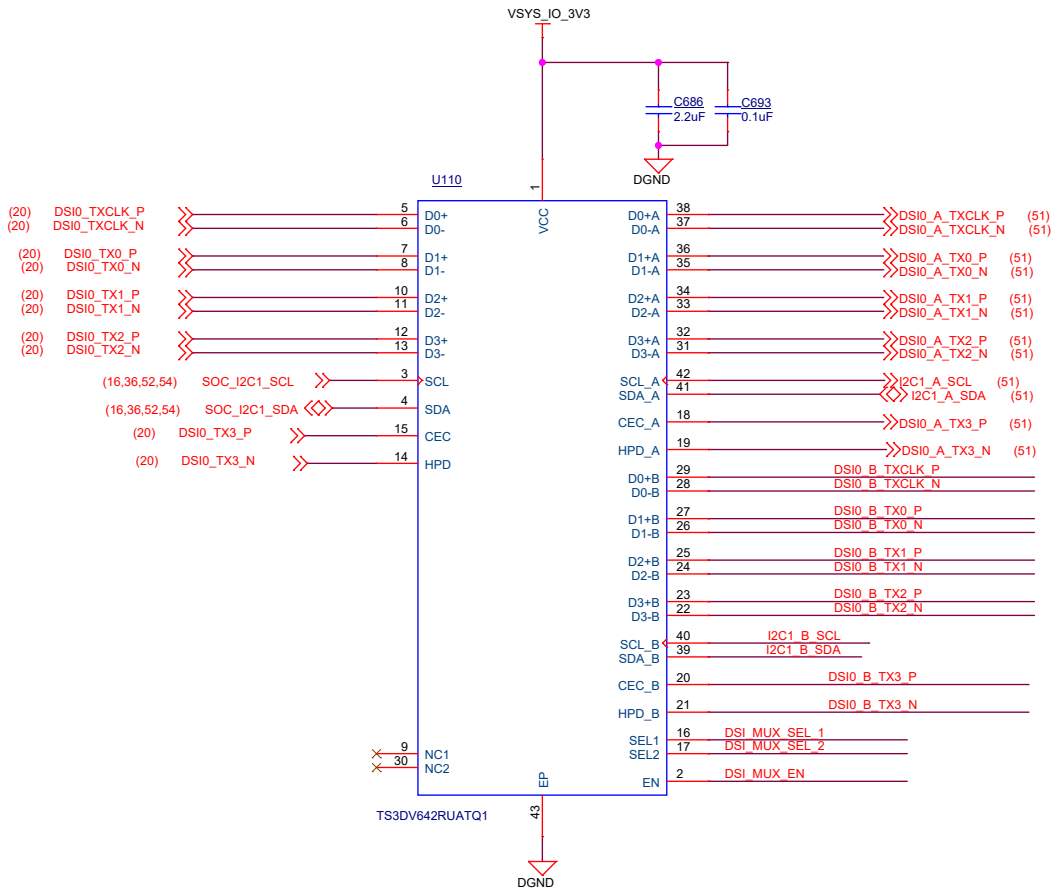
Rev
E3B

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OLDI Connector

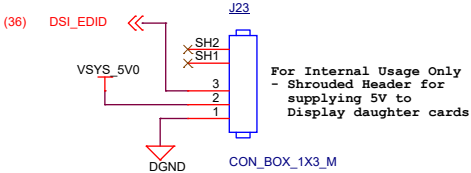
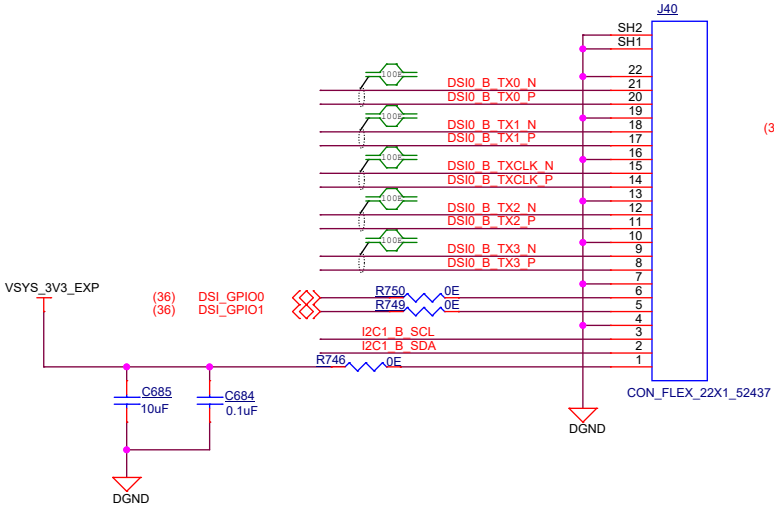


DSI Flex Connector

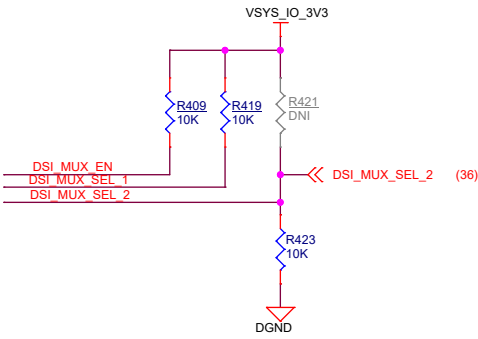


To DSI to eDP Bridge

To DSI FPC Connector



EN	DSI_MUX_SEL_2	FUNCTION
HIGH	LOW	INPUT --> A Port [DSI to eDP Bridge]
HIGH	HIGH	INPUT -->B port [DSI FPC Connector] (default)
LOW	X	Disconnect

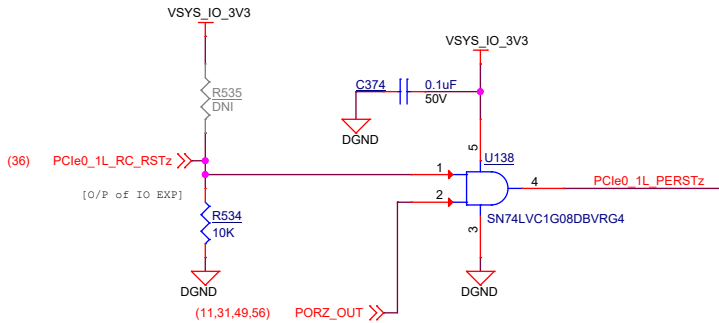
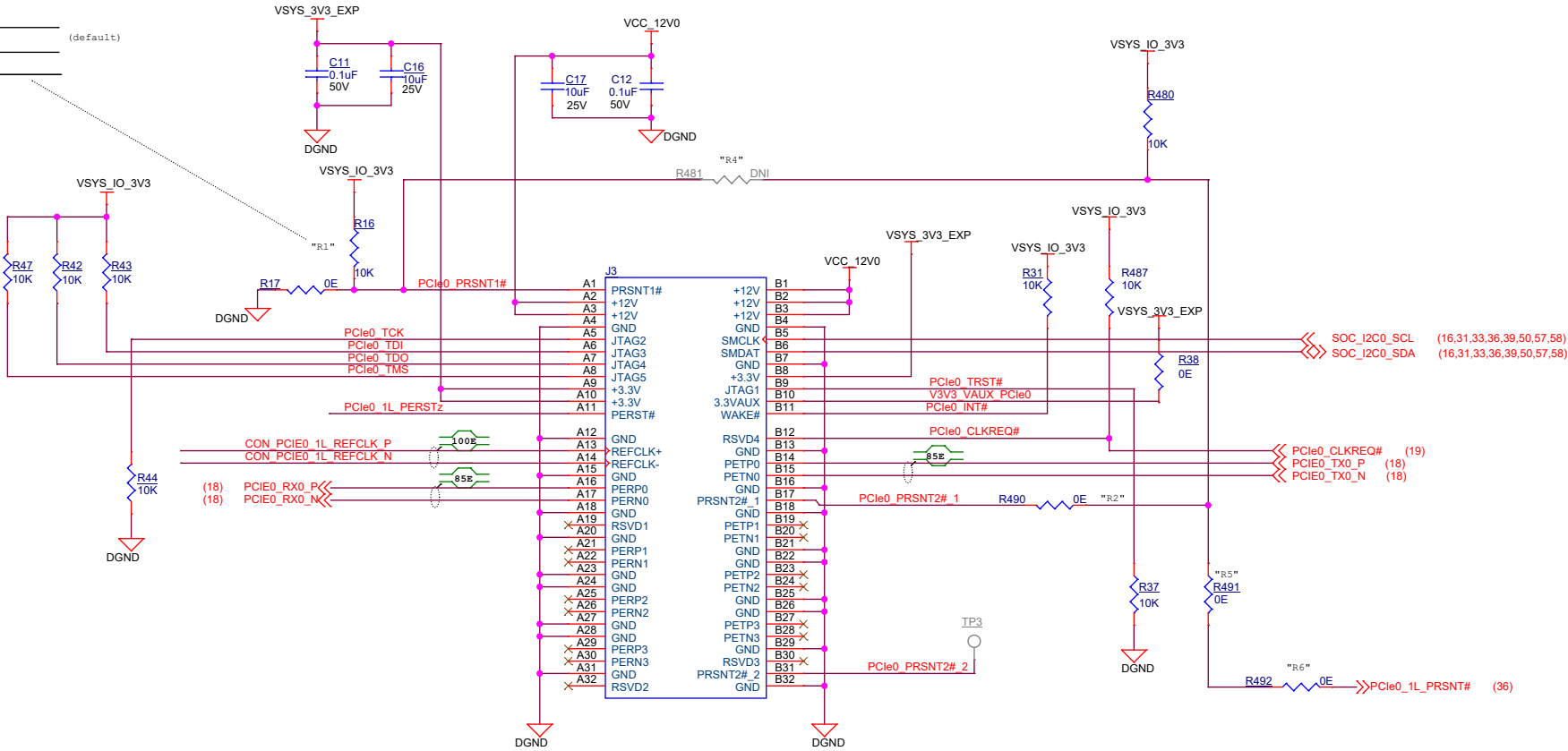


ONLY RC MODE is supported

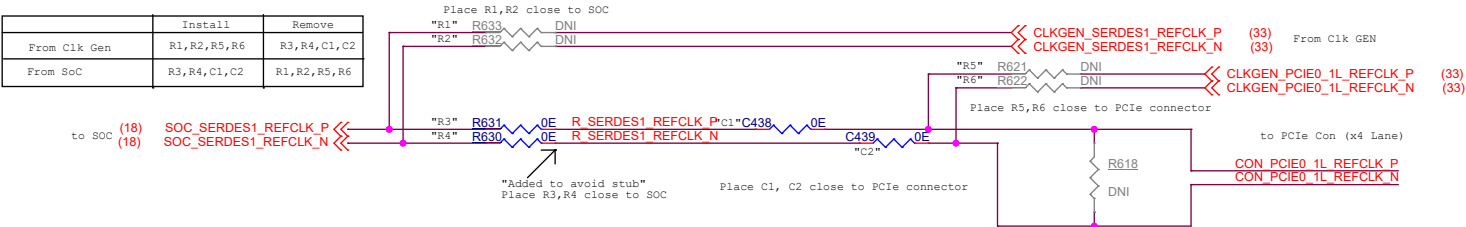
x1LANE PCIe0 Interface

x4 Lane PCIe Connector

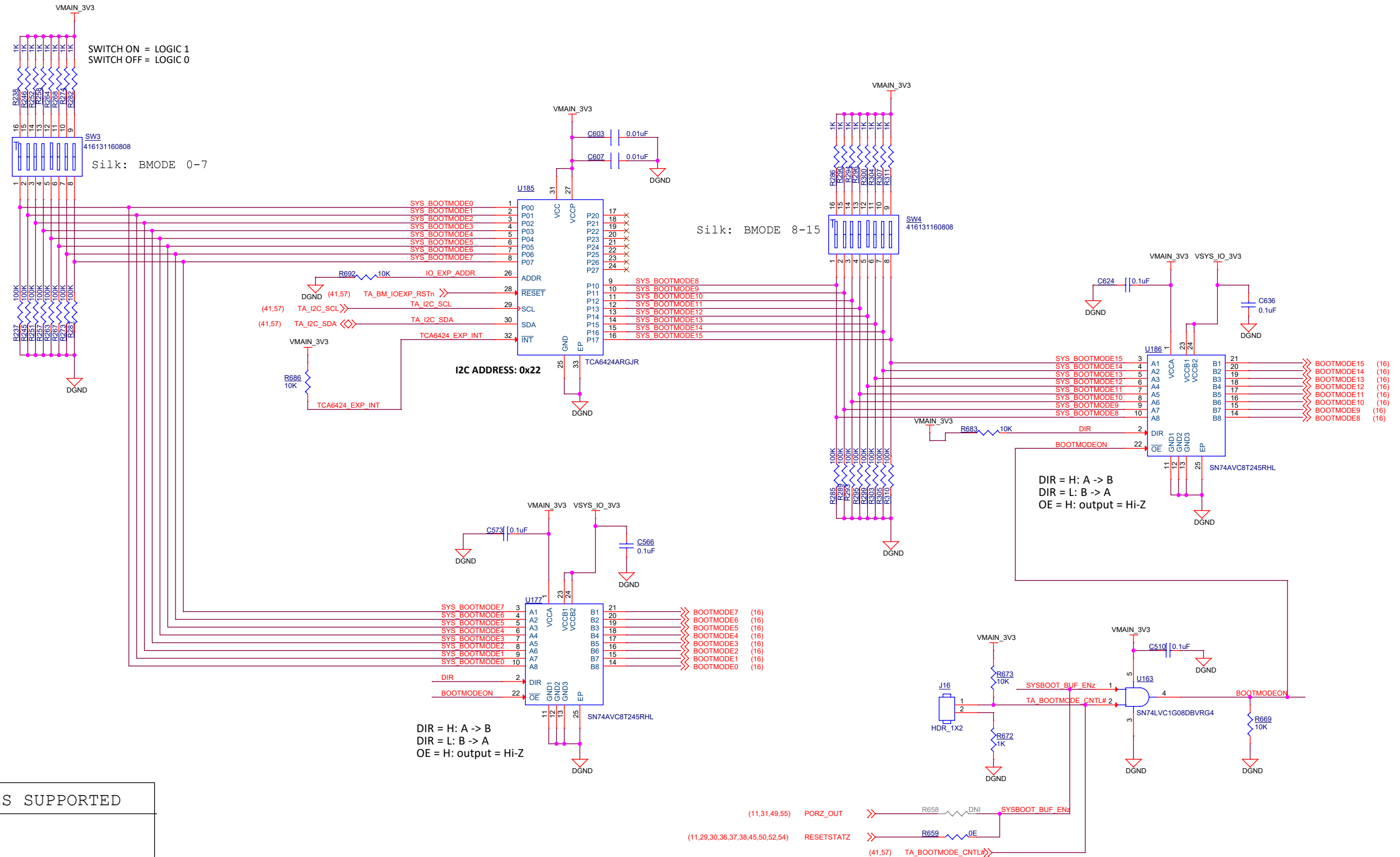
MODE	INSTALL	DNI	PCie Lanes	(default)
RC	R1, R6	R3,R4,R2,R5	Set for 4L	
RC	R1, R2,R5,R6	R3,R4	Set for 2L	



CLOCK ROOT SELECTION



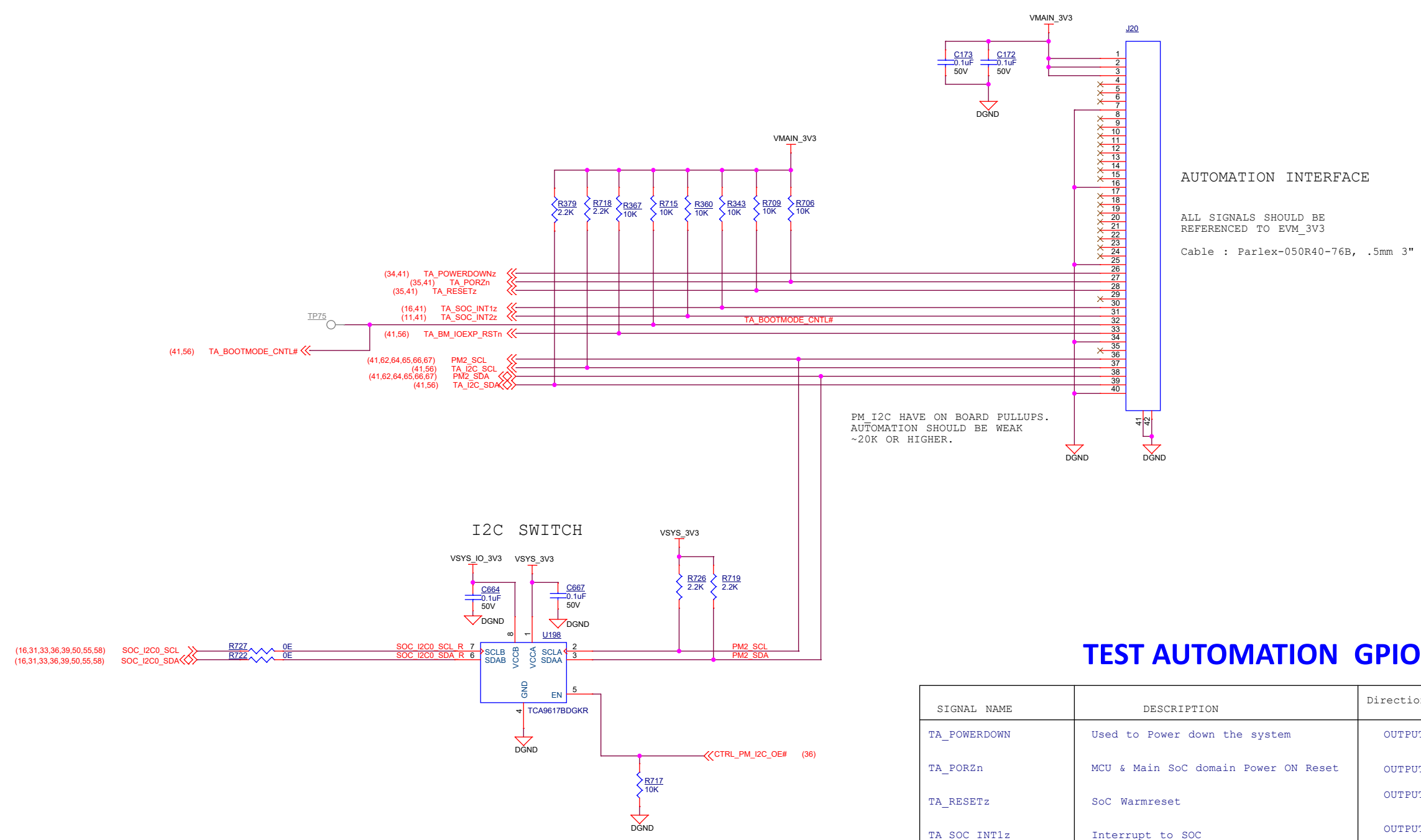
BOOT MODE BUFFERS



BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD (default)
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. No Boot

TEST AUTOMATION HEADER

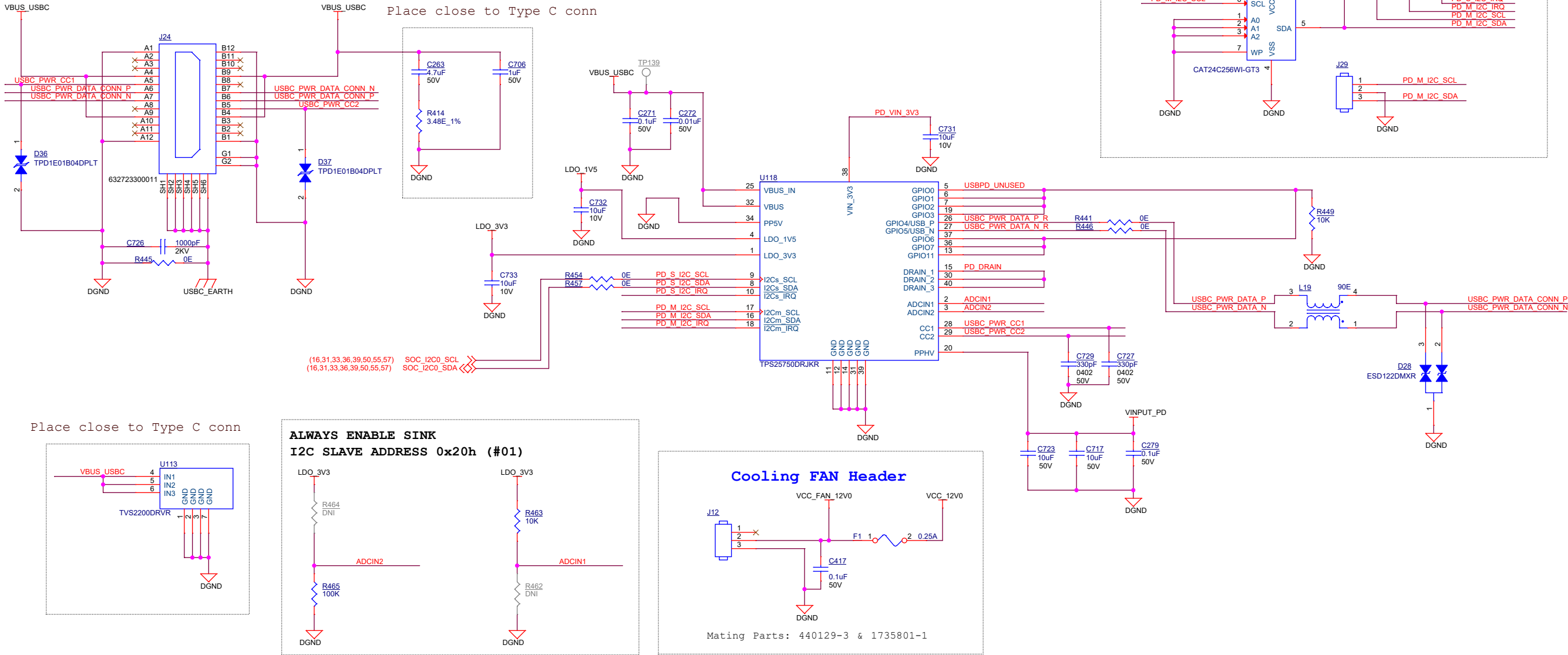
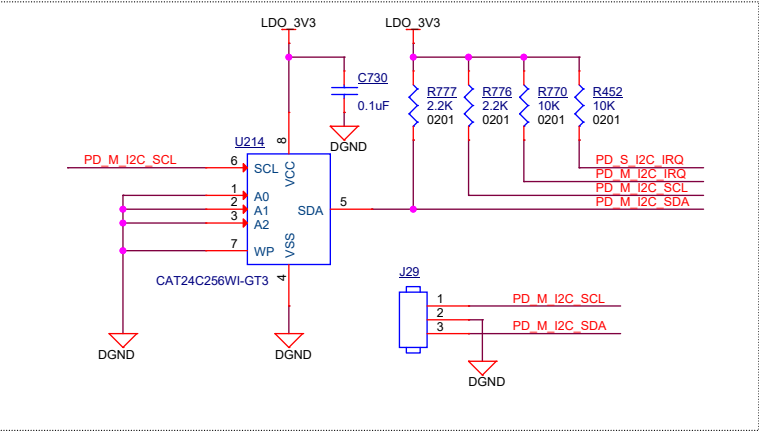


TEST AUTOMATION GPIO MAPPING

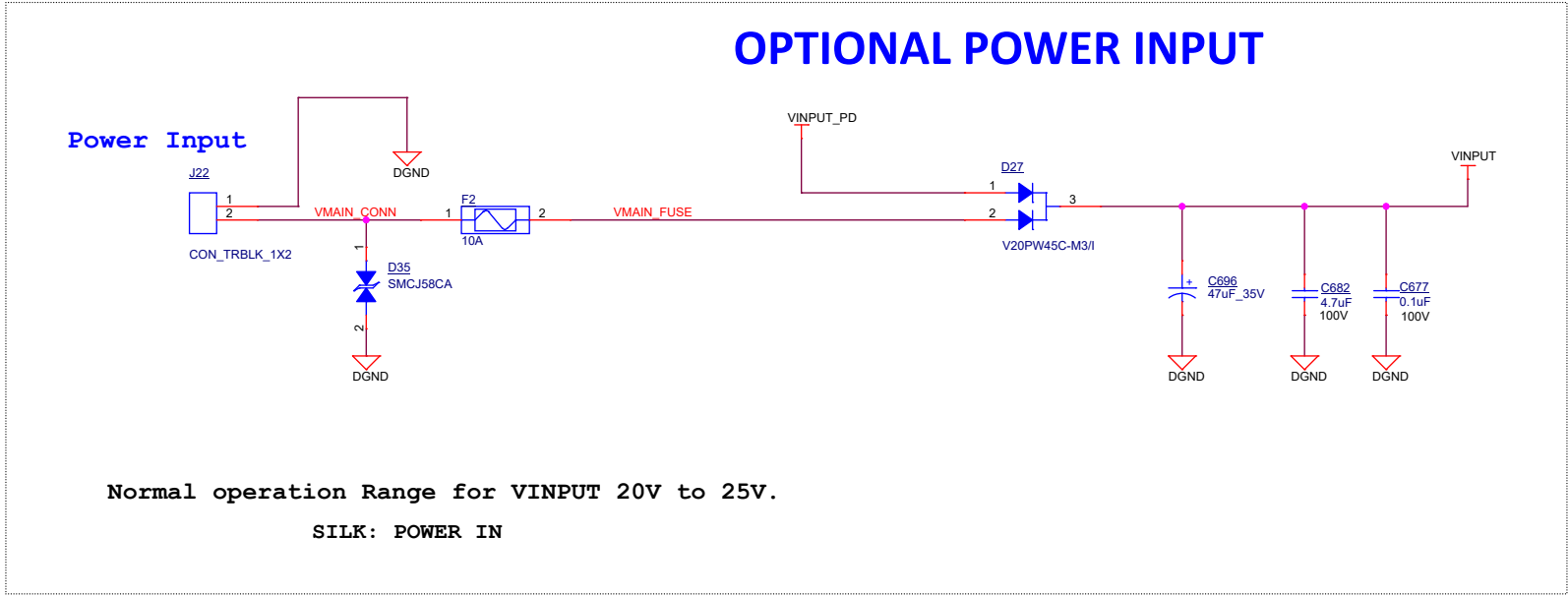
SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

USB-C Power

EEPROM & PROGRAMMING HEADER

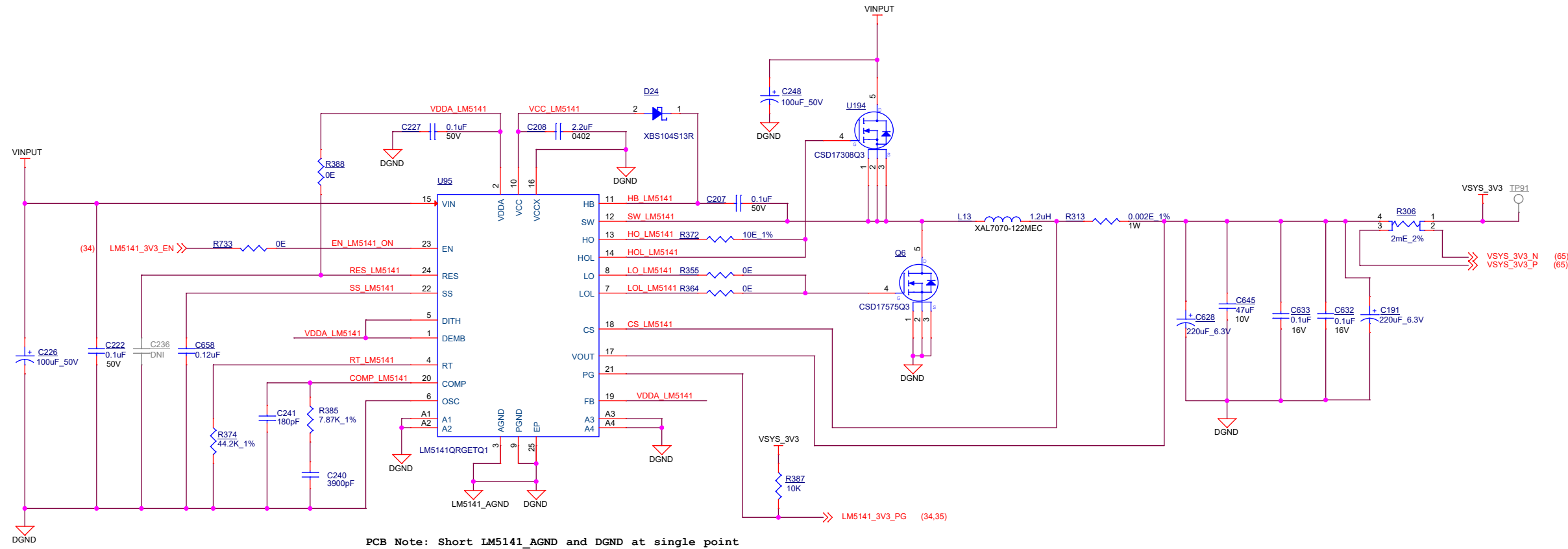


OPTIONAL POWER INPUT

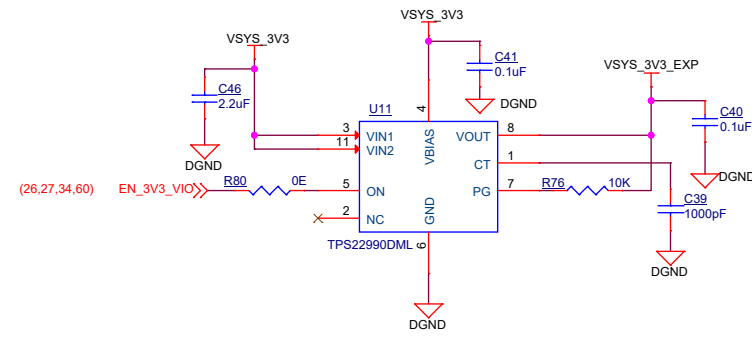


POWER SUPPLY #1
3.3V GENERATION

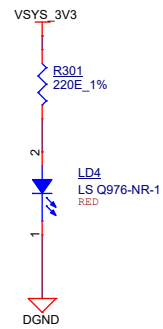
TI WEBENCH Simulation Inputs:
Vin (min) = 4.5V Vin (max) = 24V
Vout1 = 3.3V@20A
Ta = 25 deg



EXP3.3V GENERATION

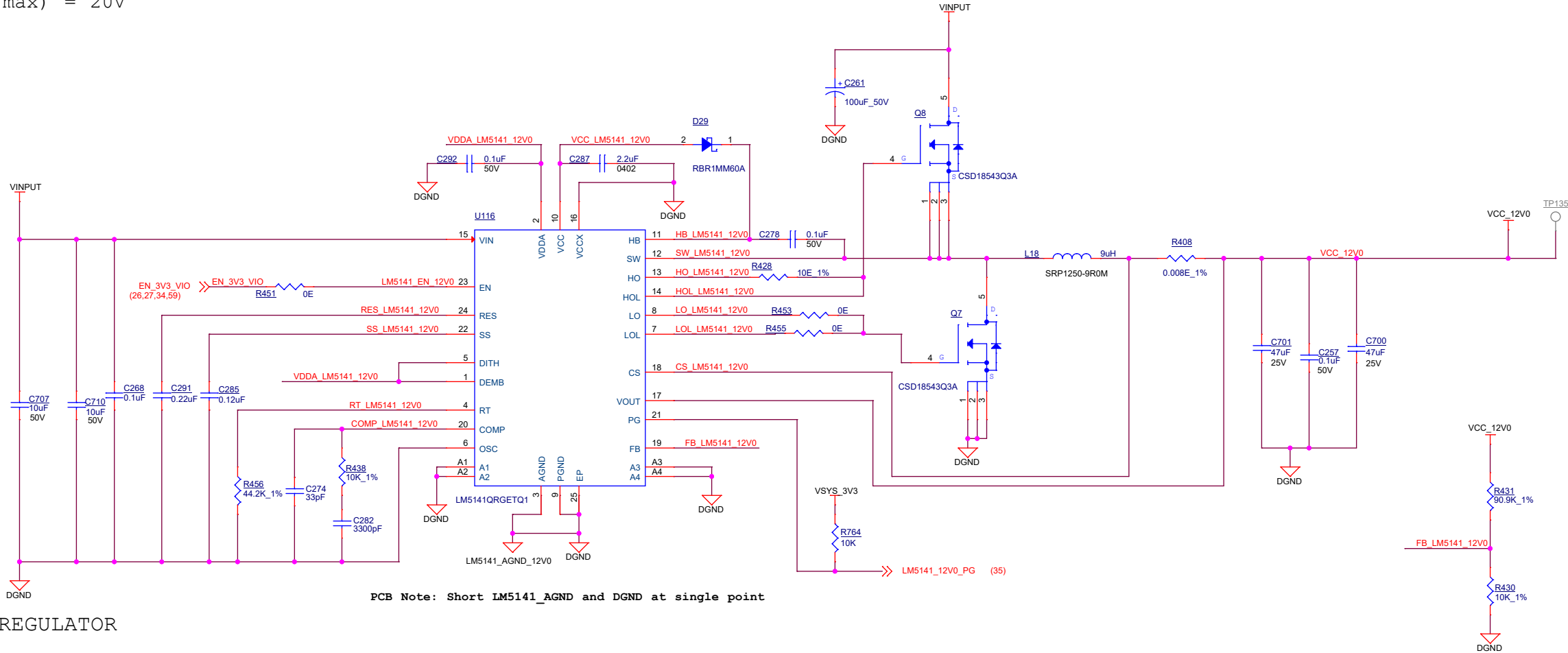


POWER INDICATION LED'S



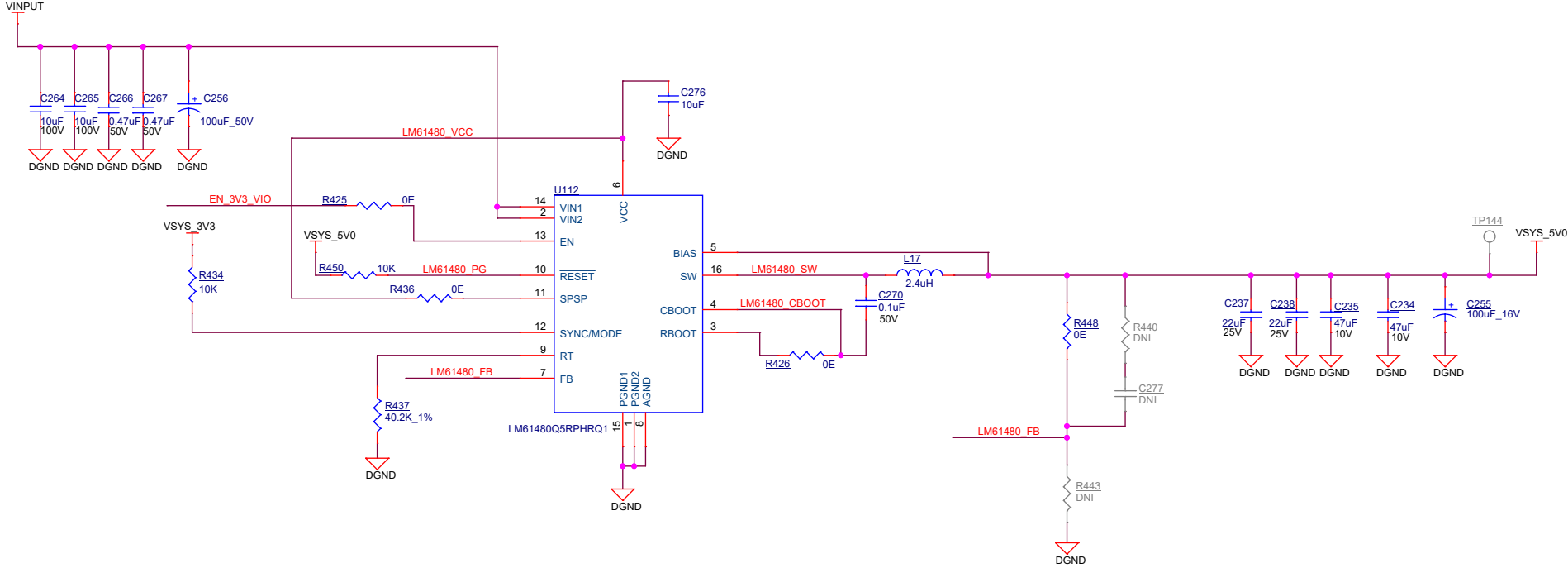
TI WEBENCH Simulation Inputs:
Vin (min) = 15V Vin (max) = 20V
Vout = 12V@5A
Ta = 25 deg

POWER SUPPLY #2

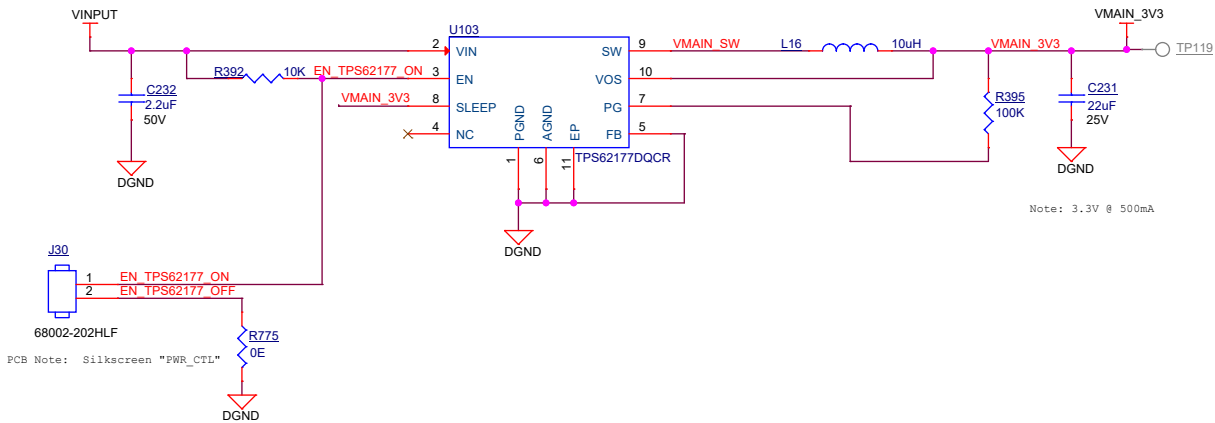


LM61460 5V BUCK REGULATOR
VinMin = 12V
VinMax = 24V
Vout = 5.0V
Iout = 7A

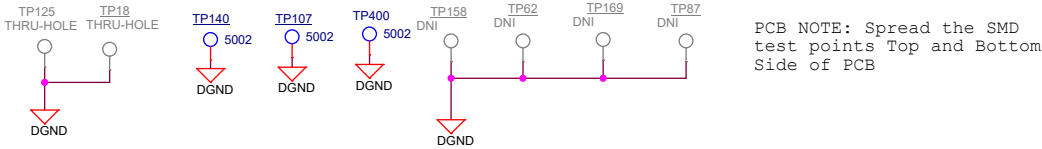
5V GENERATION



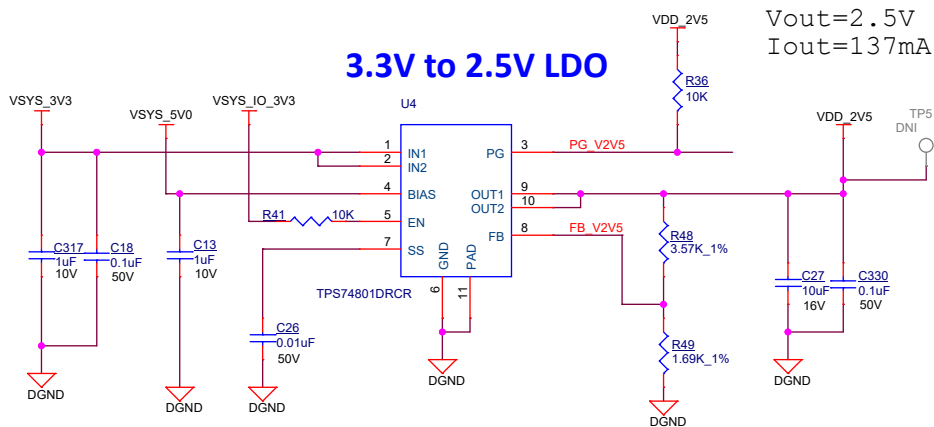
SYSTEM MANAGEMENT 3.3V REGULATOR



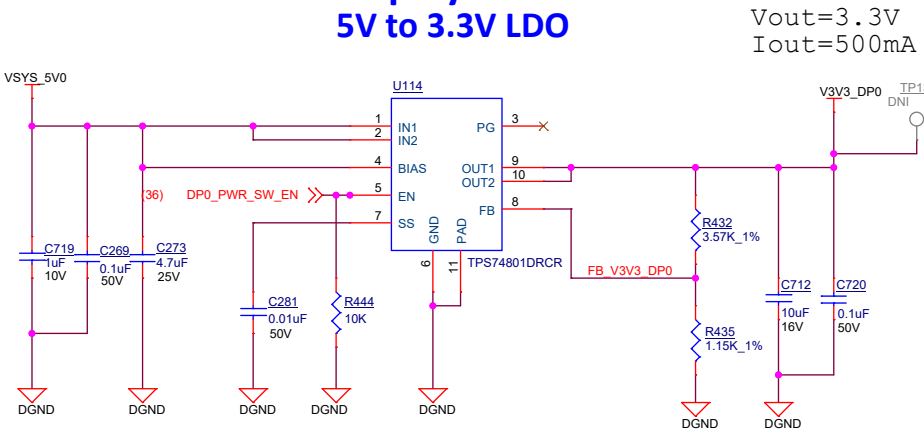
GROUND TEST POINTS



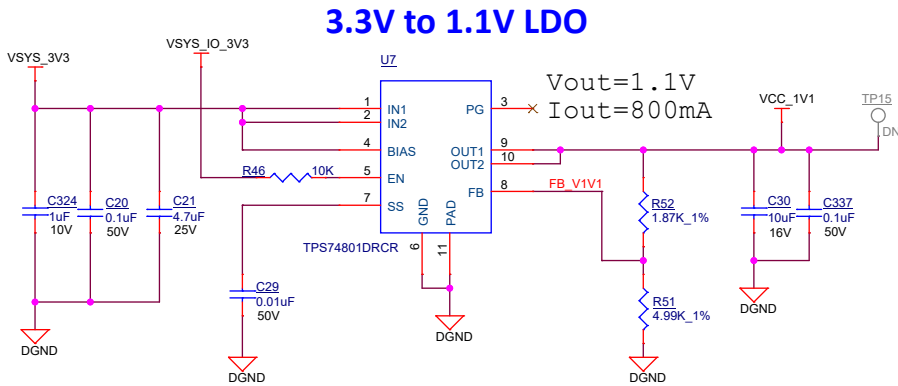
ETHERNET POWER- RGMII1



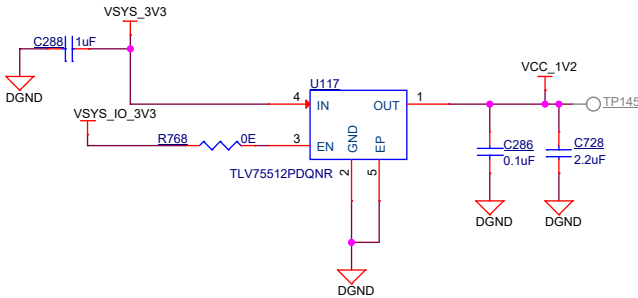
Display Port1
5V to 3.3V LDO



USB HUB POWER & ETHERNET POWER - RGMII1



eDP bridge and HDMI Power
1.2V, 0.5AMPS SUPPLY

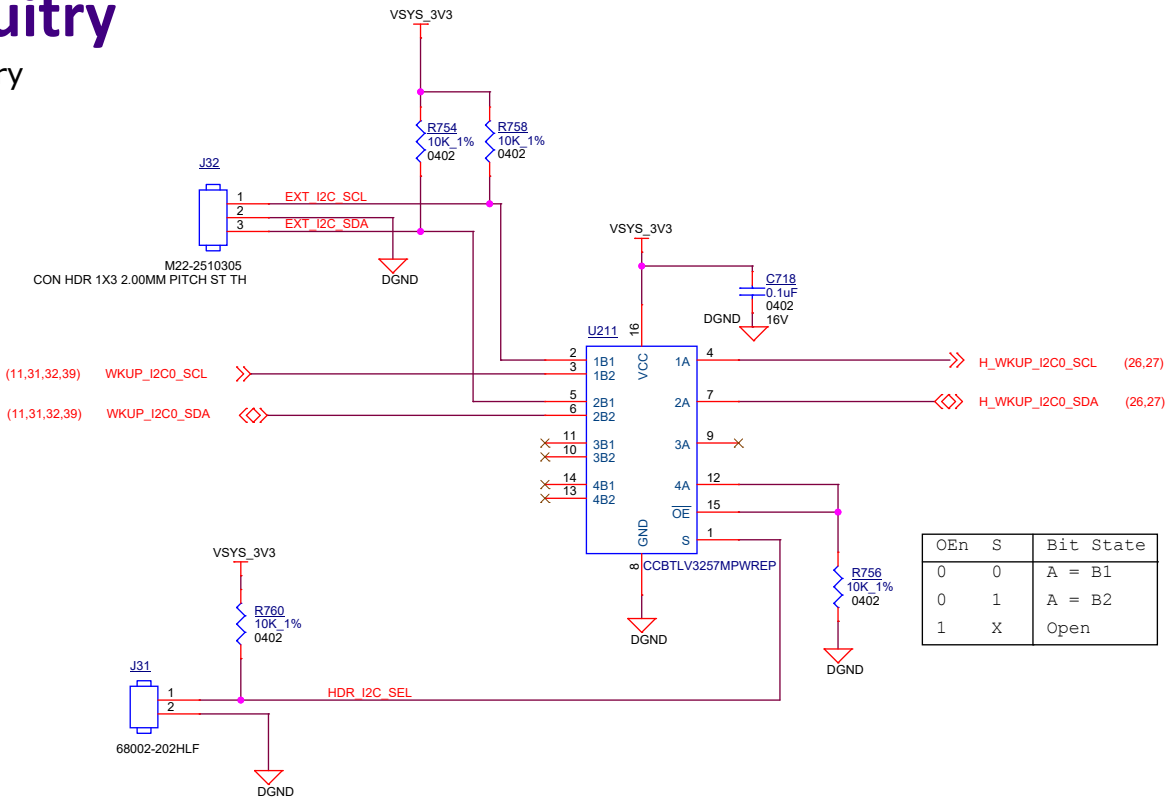


PCB NOTE:Keep 4.7uF capacitor close BIAS pin

Project : J7 EVM		Title POWER SUPPLY #1	
		Size C	Rev E3B
		Date: Friday, August 30, 2024	Sheet 61 of 68

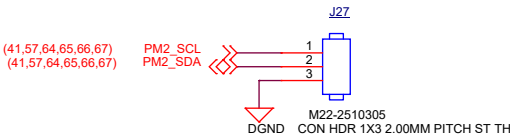
EVM PMIC Support Circuitry

EVM development & evaluation Test circuitry
(TI EVM Only)

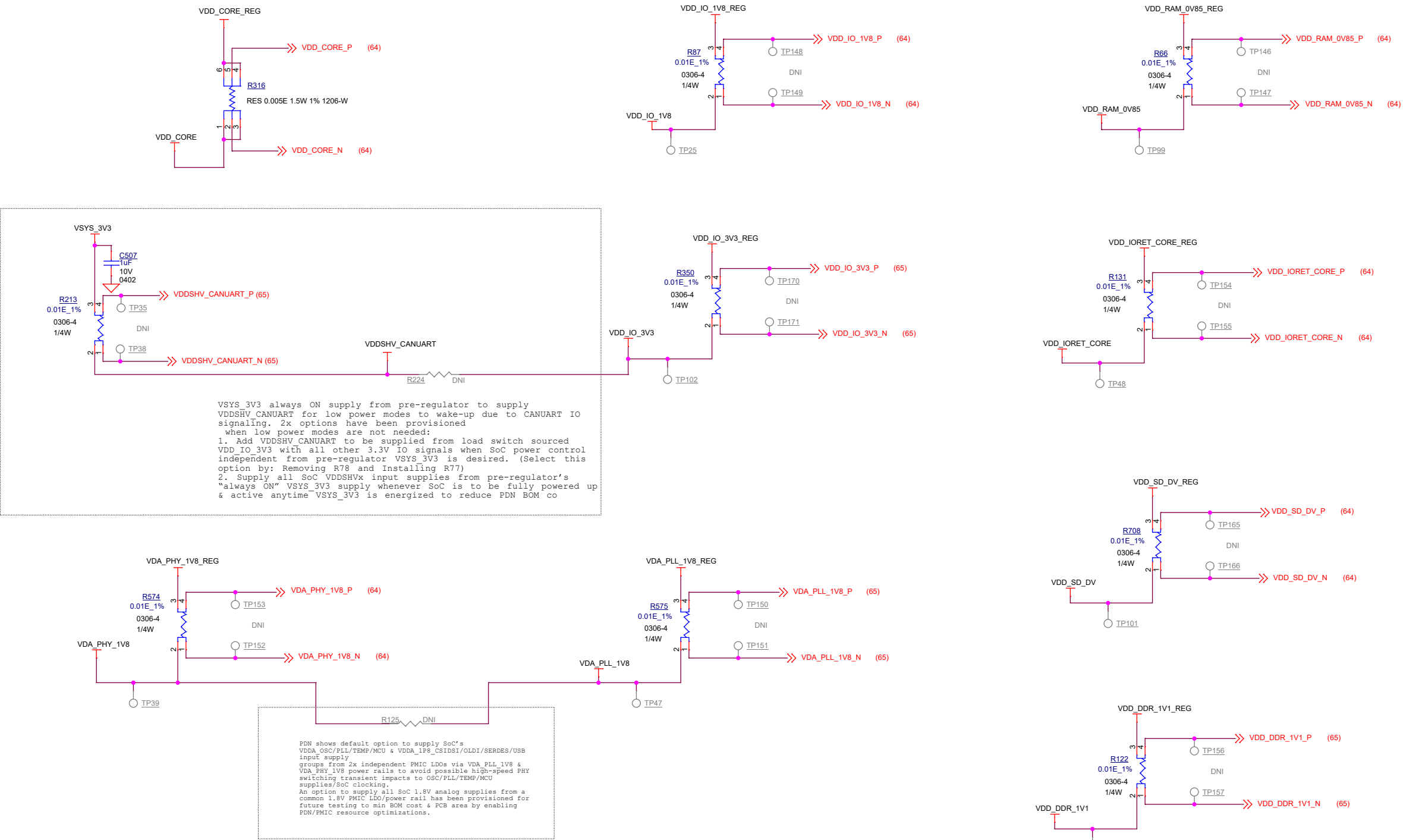


EVM POWER MEASUREMENT I2C BUS ISOLATION

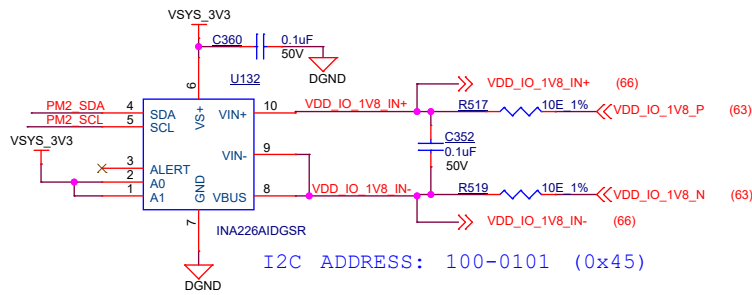
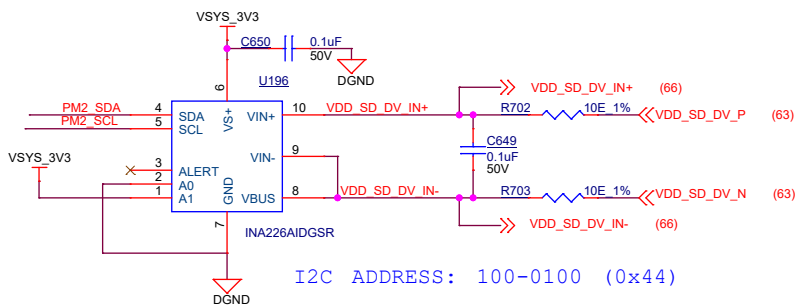
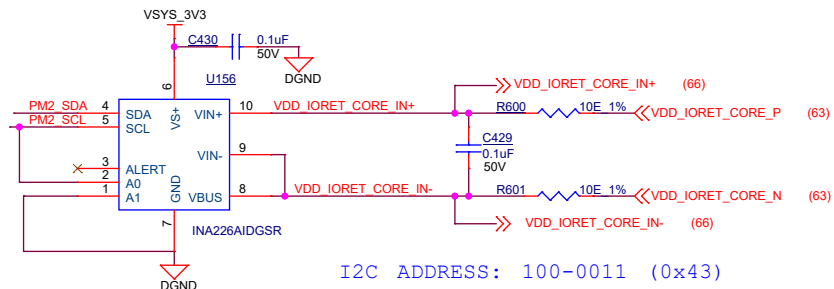
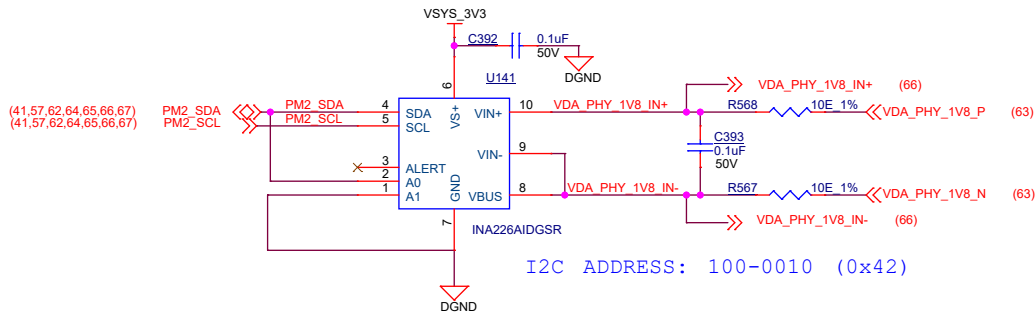
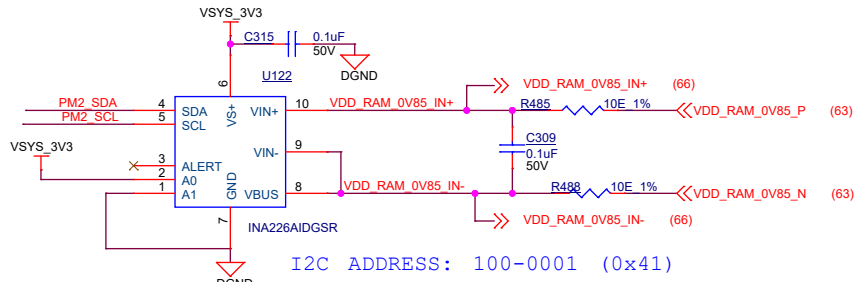
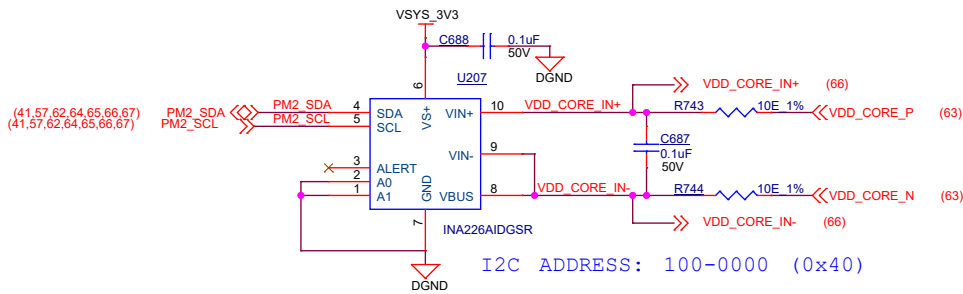
EVM development & evaluation Test circuitry
(TI EVM Only)



SOC Current Sense Resistors



CURRENT MONITORS #1



Project :

J7 EVM



Title
CURRENT MONITORS #1

Size
C

PROC170 002 EVM

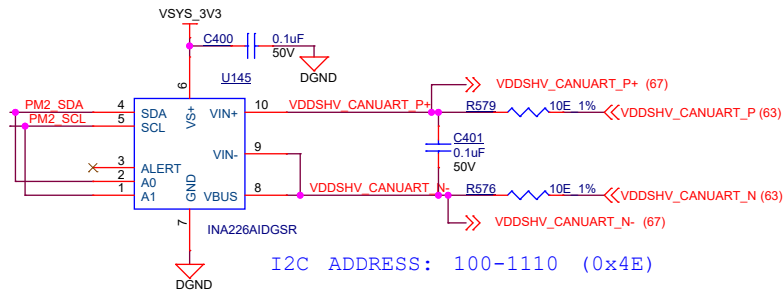
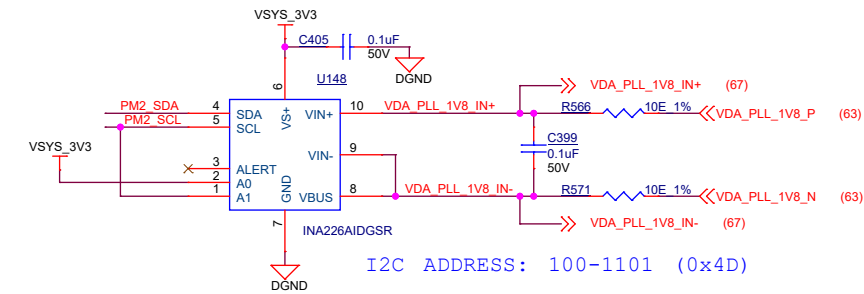
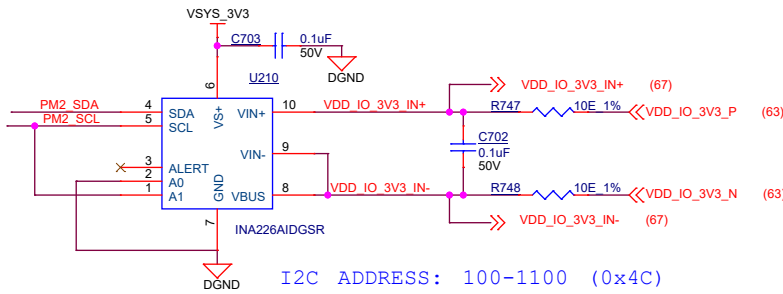
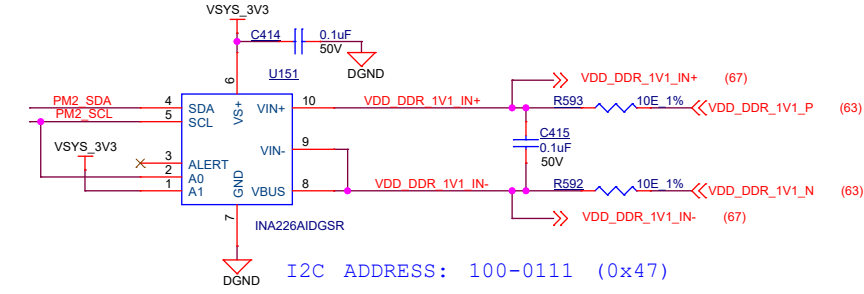
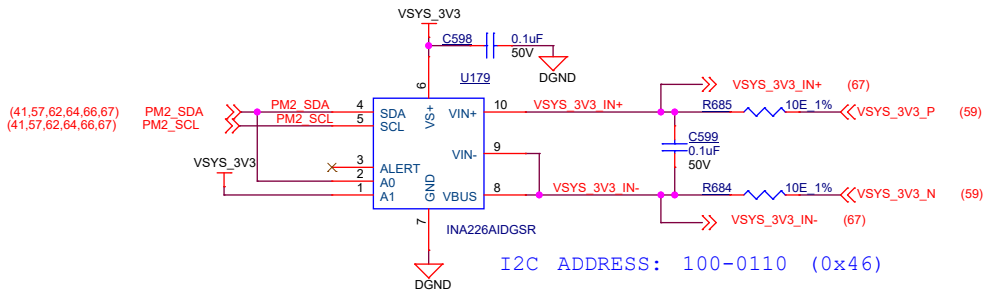
Rev

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Date: Friday, August 30, 2024

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CURRENT MONITORS #2



Project :

J7 EVM



Title
CURRENT MONITORS #2

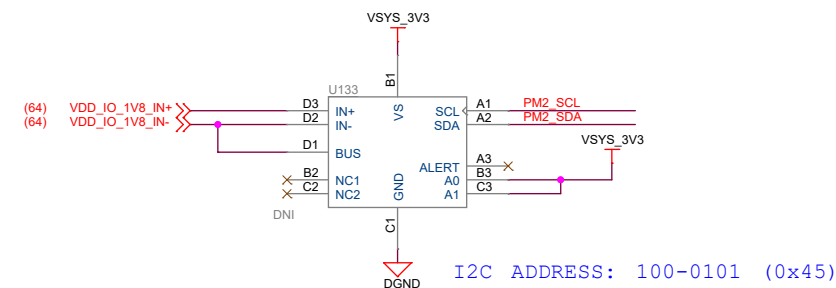
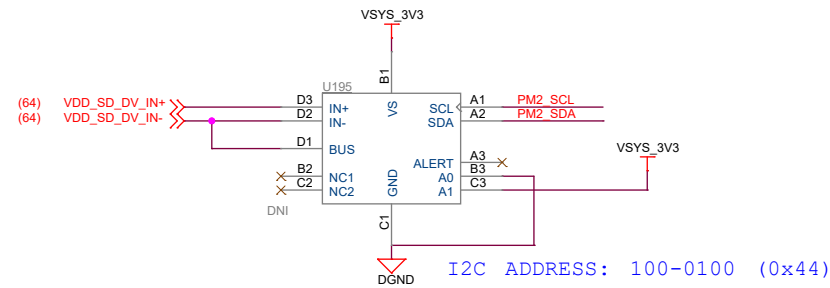
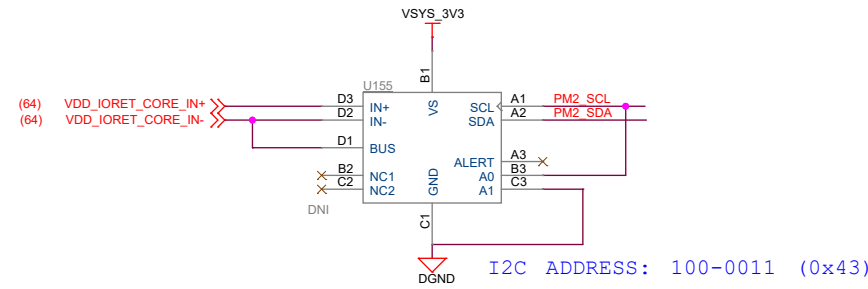
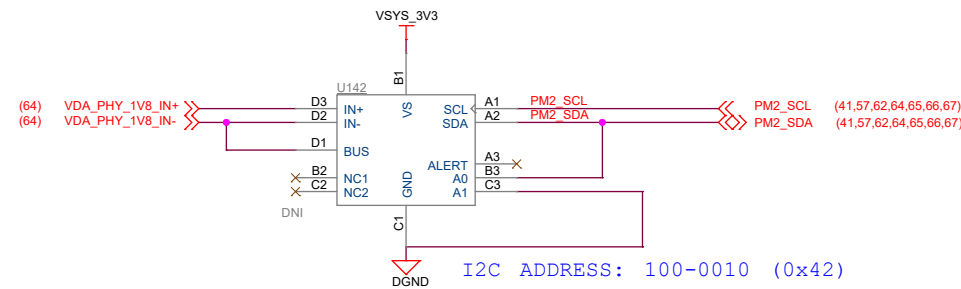
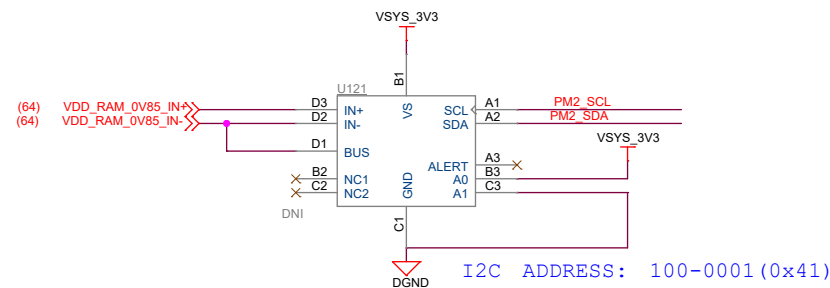
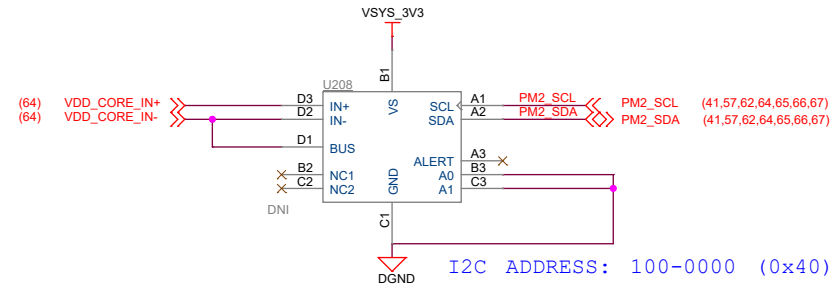
Size
C
PROC170 002 EVM

Date: Friday, August 30, 2024

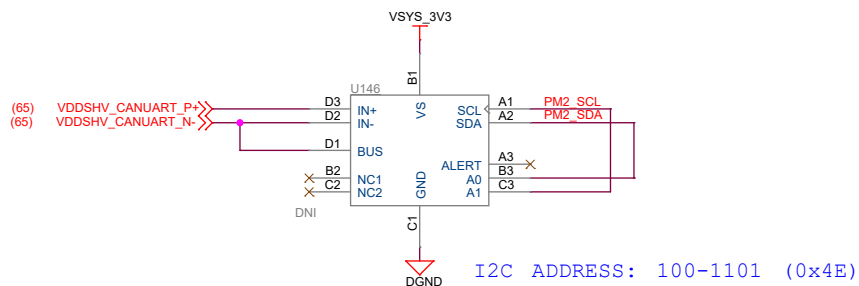
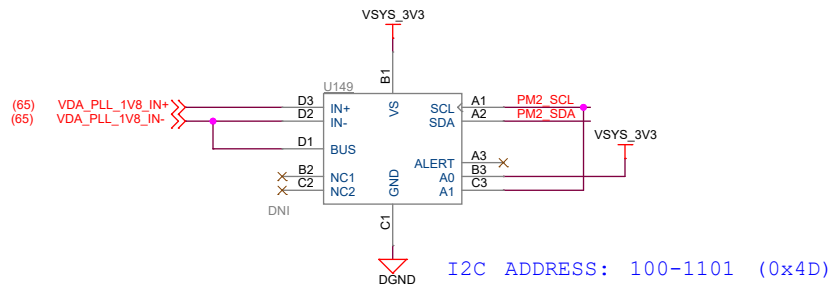
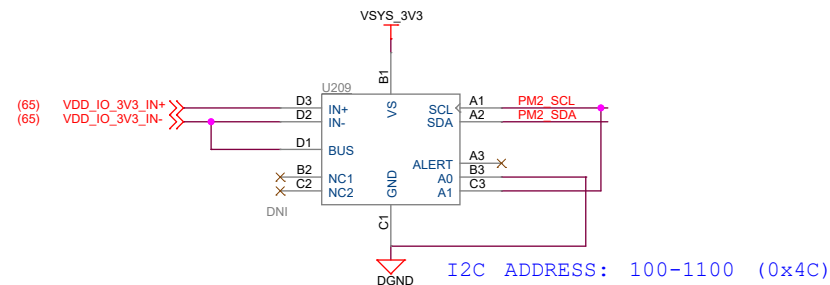
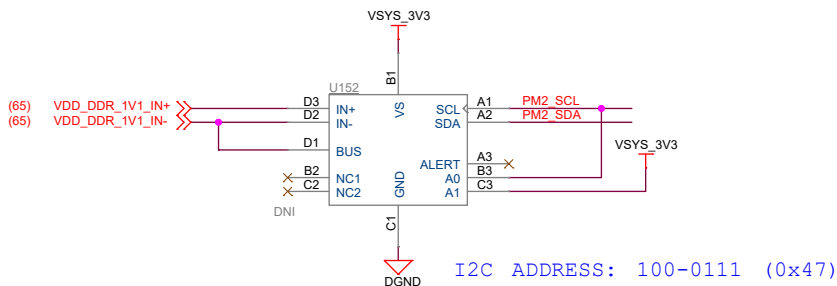
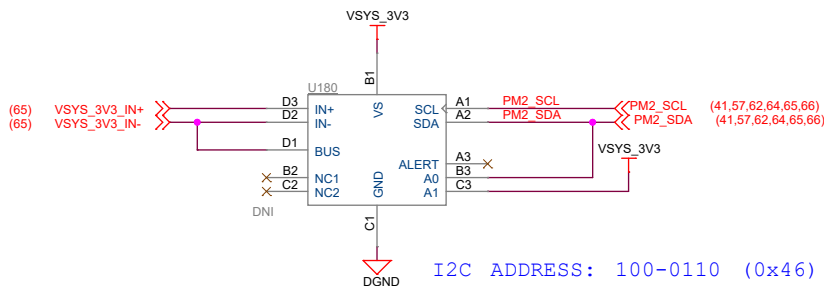
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Rev
E3B

CURRENT MONITORS - INA231



CURRENT MONITORS - INA231



NOTES, HW & LABELS

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

LABELS

Board Serial No.



AM6-COMPROCEVM

Assembly Revision.



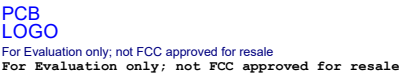
AM6-COMPROCEVM

EVM Orderable Part No.

Orderable Part Numbers

Variant	Label Text
001:Soldered GP SoC	J722SXG01EVM
002:Soldered HS SoC	J722SXH01EVM
003:Socketed SoC	J722SXS01EVM

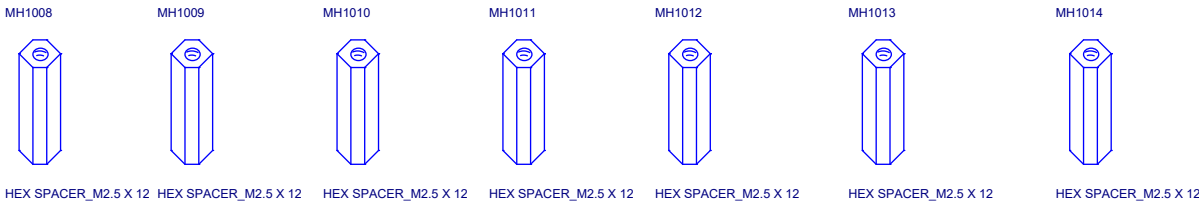
LOGOs



SCREWS



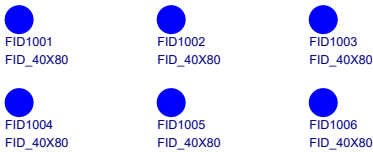
STANDOFFs



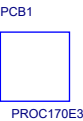
WASHER



FIDUCIALS



BARE PCB



J722S TDA4VEN TDA4AEN AM67 SOC



SOCKET



Project :

J7 EVM



Title
HARDWARE SCHEMATICS

Size
C
PROC170 002 EVM

Date: Friday, August 30, 2024

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Rev
E3B