

TDA4VEN/AEN and AM67 Evaluation Module


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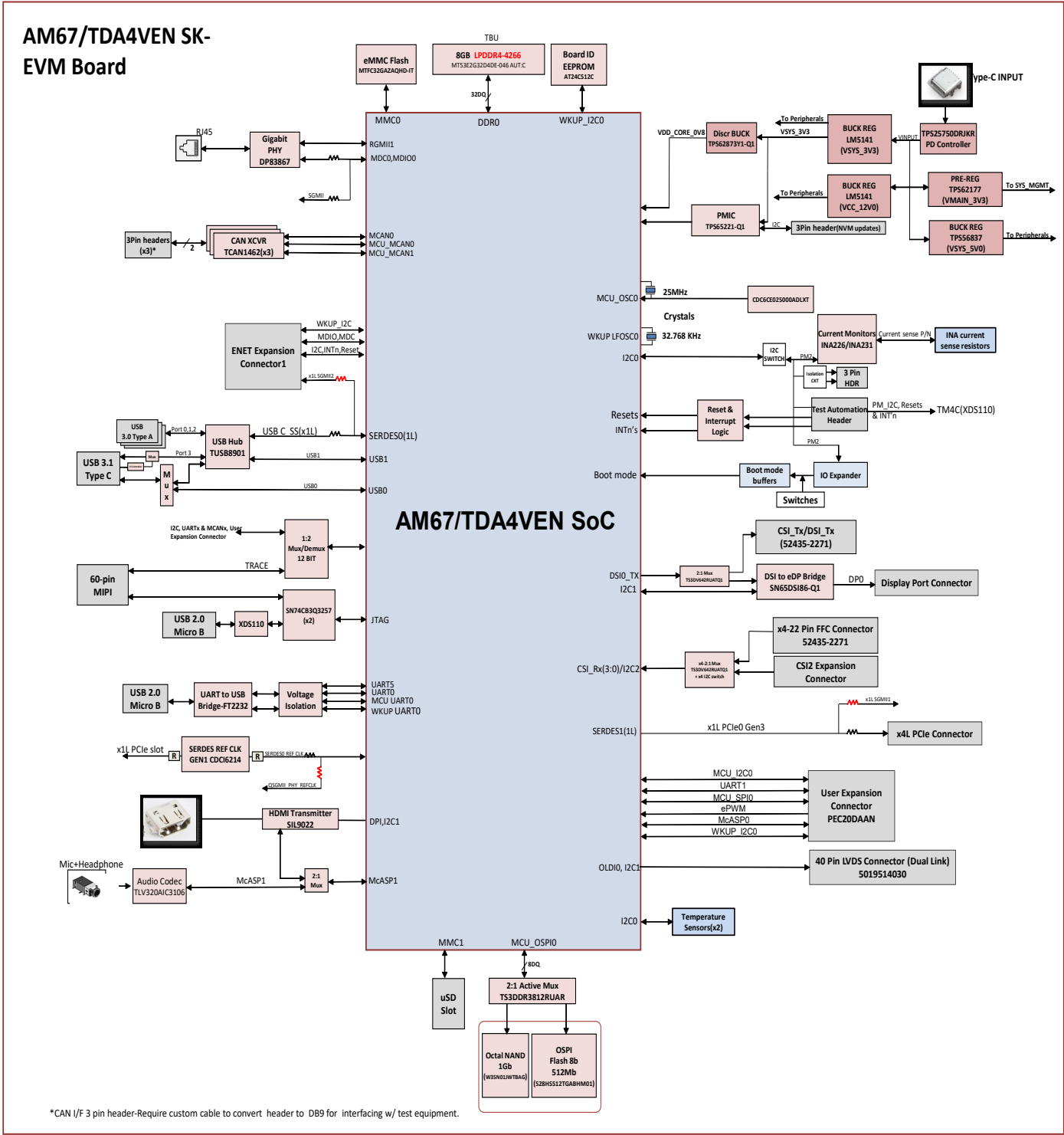
REVISION HISTORY #1

E1	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
	0.1	14 JUN 2023	Draft schematic	Mistral Design Team		
	0.2	26 JUN 2023	V0.11 Breakout schematic imported to core evm schematic			
	0.3	06 JULY 2023	Review comments updated			
	0.4	19 JULY 2023	Updated schematic to breakout V0.14			
	0.5	04 AUG 2023	Updated schematic to PDN 7G v0.16			
	0.6	05 SEPT 2023	Review comments updated			
	0.7	11 SEPT 2023	Board released to Fab	Mistral Design Team	TI	TI
	0.8	06 OCT 2023	Since LM61480Q5RPHRQ1 IC gives a default 5V0 output and does not need a resistor divider feedback. So,R443 is DNI'd and R448 is replaced with 0E. Feedback to VDD_RAM_0V85 supply is after the ferrite bead. There seems to be more noise in feedback. FL17 is replaced with 0E. Seeing 1.8V @ EN_TPS62177_ON signal which will enable the device even with jumper on J30. Replaced R775 with 0E in order to avoid voltage divide. Change in the compensation network values of 12V0 circuit. R438 is replaced with 10Kohm. To get default 100MHz clk from U10 LMK device, the enable should be either floating or pulled down. R58 is DNI'd to get default output. In order to source the 19.2MHz clock to DSI to eDP bridge external oscillator path is enabled by populating R410 and R412 DNI'd. Change in compensation values of 3V3 generation circuit to avoid initial power up issue. C241: 390pf, R385:7.5k, C240:3300pf I2C address text updated for U88 IO expander	Mistral Design Team	TI	TI
	0.9	15 Nov 2023	Replaced Compensation network for 12V0 and 3V3 values with new values suggested by TI Feedback VDDR supply is given before the FB Fix for TRACE DATA 13 U190 and U12 mux replaced with the mux which do not have internal pull down.			
E2	1.0	13 Dec 2023	LMK3H0102 devices are replaced with x2 NVM programmed parts. Resistor mount option changed for PCIe clock default to internal clock. Added support for RADAR(R-option or Mux for SPI on Expansion header) Added R-Option to connect MCU_OBSCLK and OBSCLK to test point.	Mistral Design Team	TI	TI

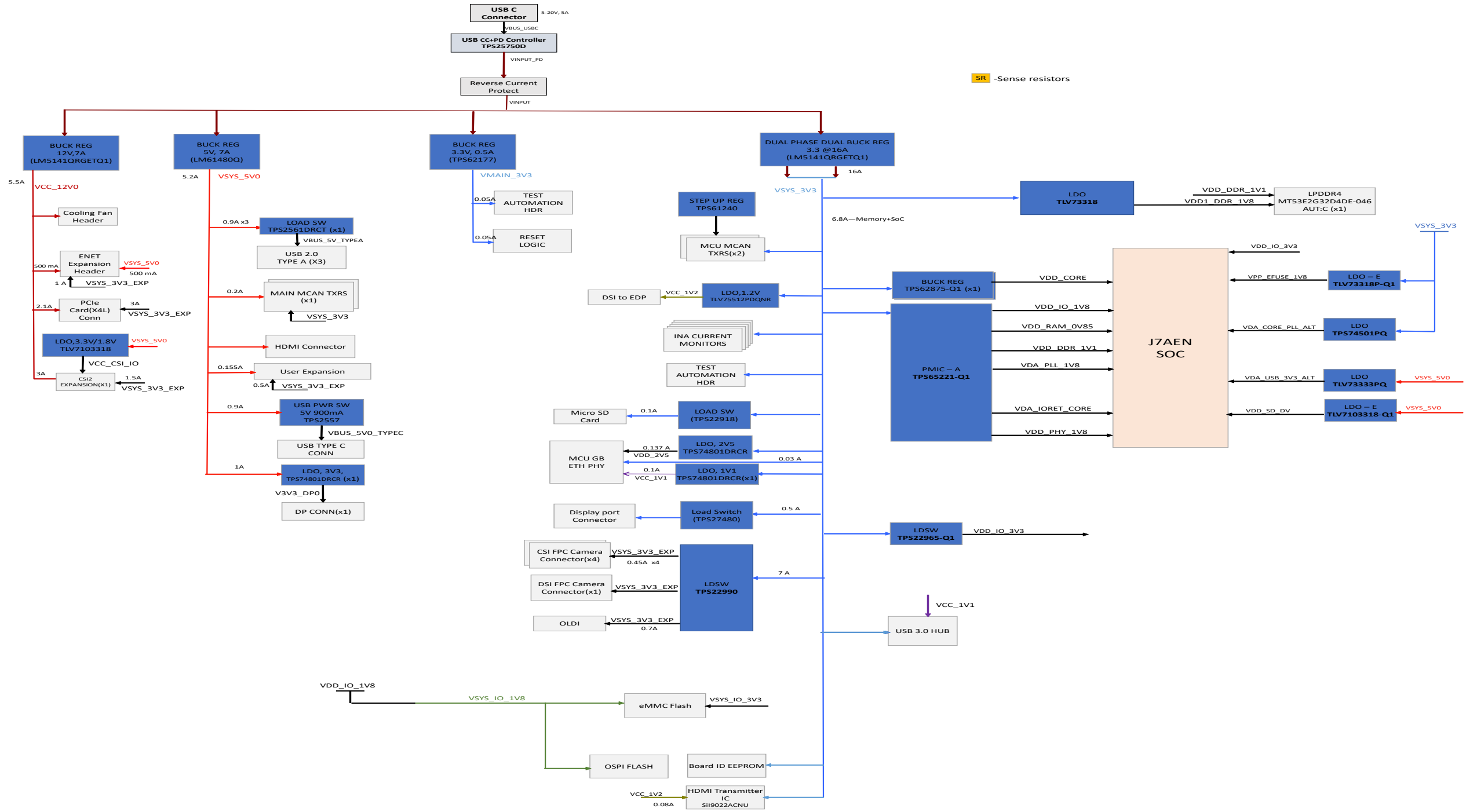
REVISION HISTORY #2

Project : J7 EVM				Title REVISION HISTORY#2	
				Size C	Rev E1
				Date: Thursday, December 14, 2023	Sheet 3 of 68

BLOCK DIAGRAM

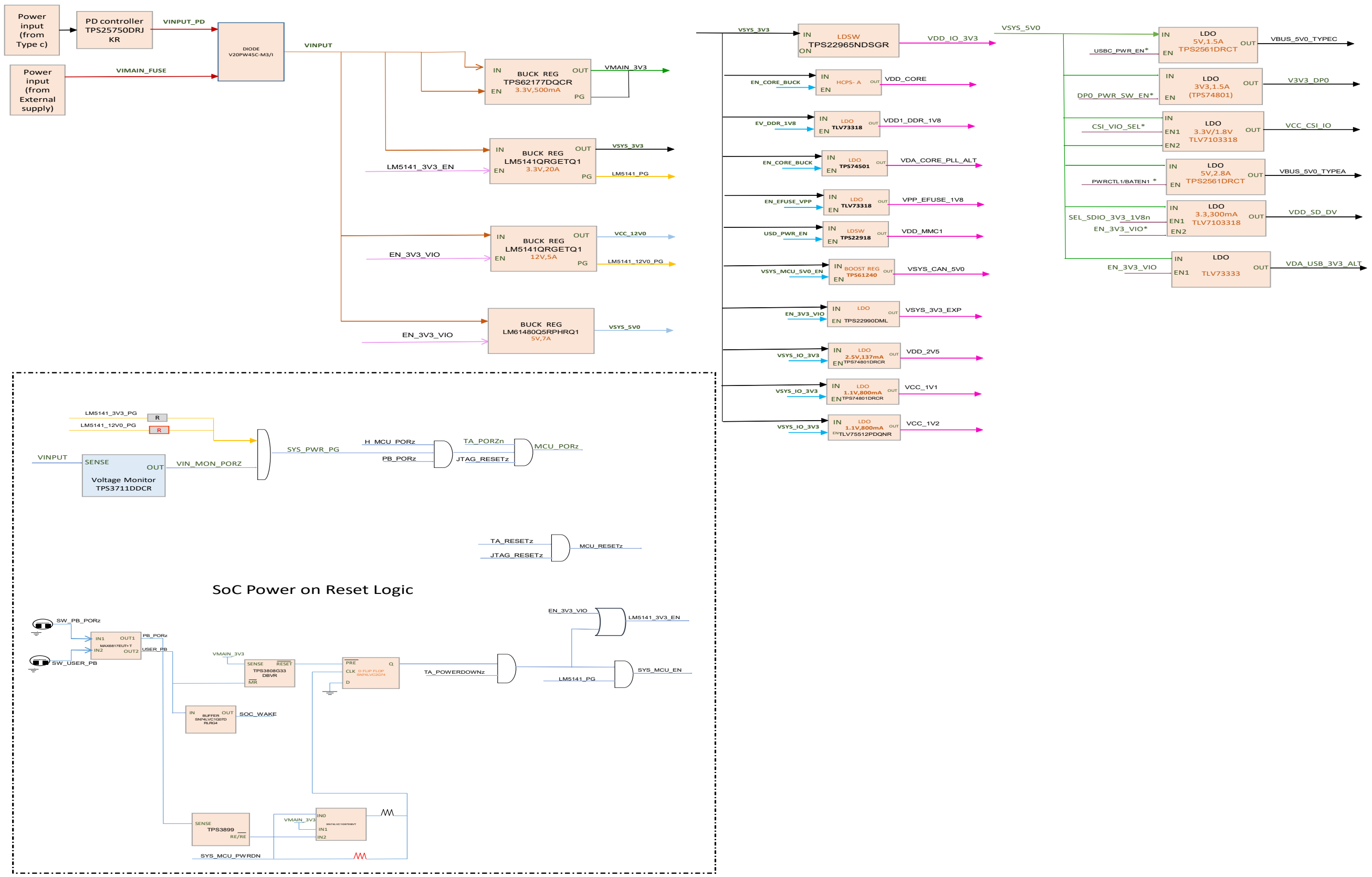


POWER FLOW DIAGRAM



POWER SEQUENCE

J7AEN SK EVM Board Power Sequencing



PDN

I722S EVM Burton PMIC + Orchid HCPS PDN-7G
(All SoC PN variants: TDA4AEN/VEN)
(Power Rail & GPIO Mapping Overview)



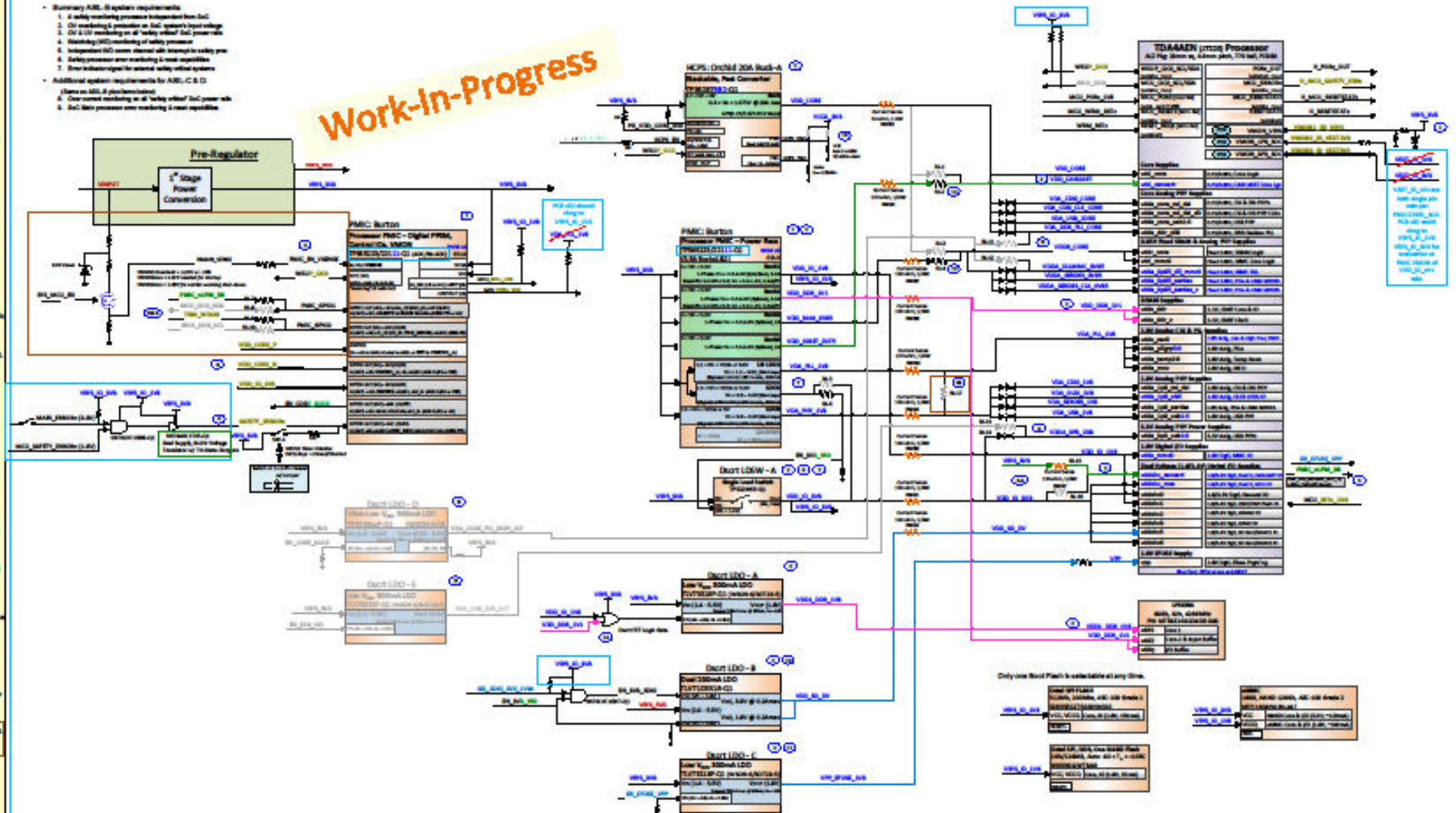
Features Supported (EVM Max Features):

- 1. SoC's 4x A53s clock at 1.4GHz with **SERDES operational per "EVM" use case** (EVM UC combines FCD + CMS use cases)
- 2. Functional Safety: **ASIL-B** capable system
- 3. SDRAM: 1x EMIF with LPDDR4 (32GB, 4x Die, 32B, 4000MT/s, VIO = 1.1V)
- 4. Flash: Octal SPI or NOR-Flash for boot & eMMC for mass storage
- 5. Dual Voltage Signaling: Dual VIO (3.3/1.8V)
- 6. Low power modes:
 - a. **Partial IO Retention**
 - b. **Partial IO + DOR Retention**

7. End Product Options:
- a. Compliant high-speed UHS-I SD Card
 - b. Best Effort USB 2.0 data eye (analog filter VDD_3D_0V is to reduce noise for better eye)
 - c. HS SoC fuses programming on-board (needs 1 indep per rail & 1 ctrl signal)

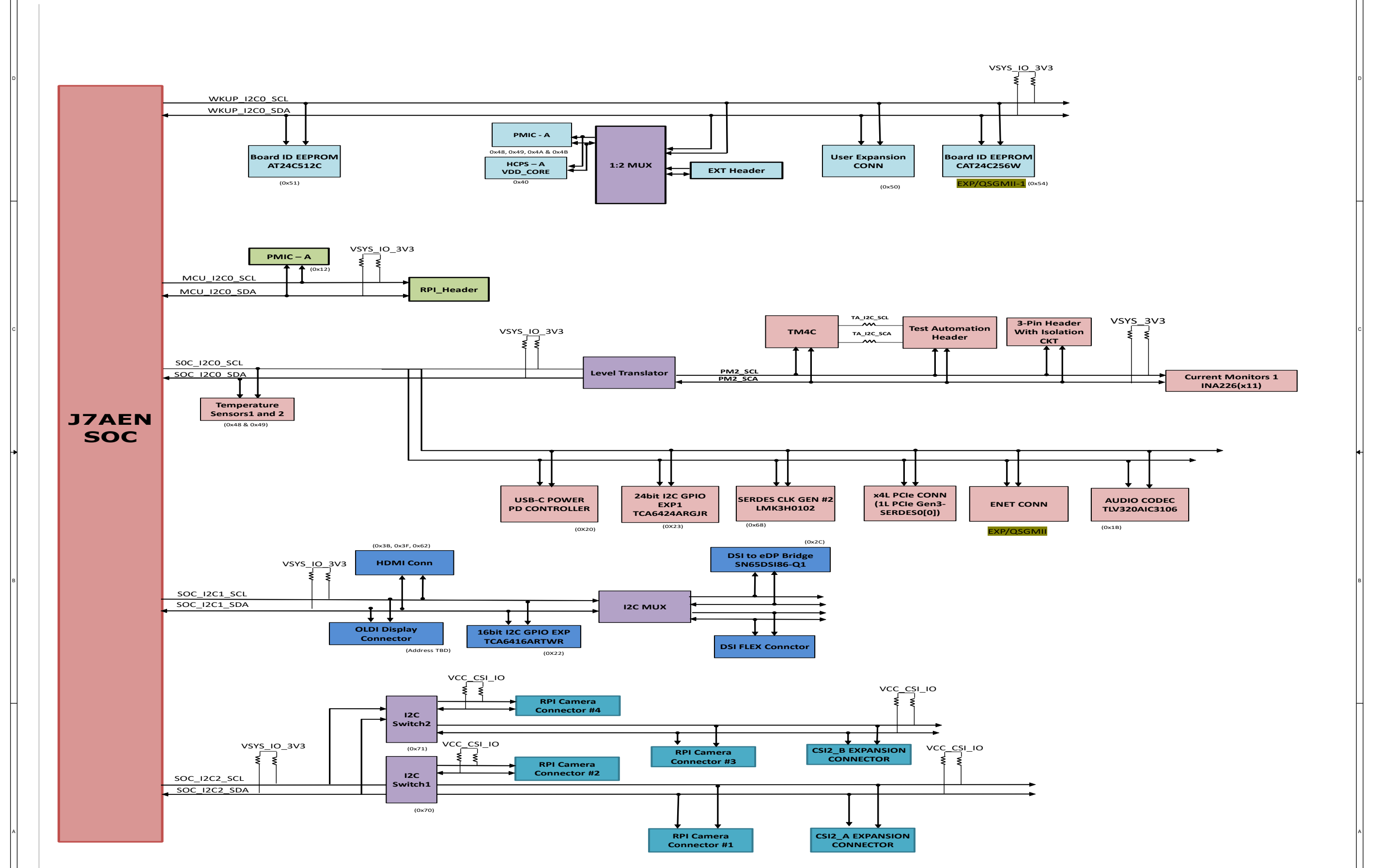
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Work-In-Progress



MSL comparison	Default output voltage	DC device address	Group comparison	Transfer output mode
MSL 125 to 1200	2.25V	0x00	enabled	enabled
MSL 1200 to 1250	2.75V	0x01		
MSL 1250 to 1300	3.25V	0x02		

I2C TREE



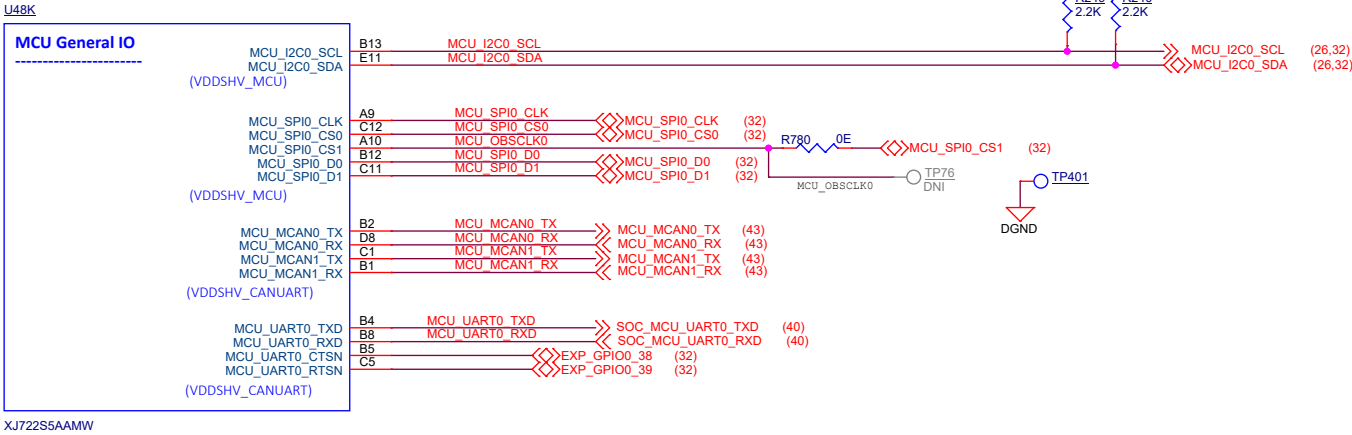
I2C TABLE

BOARD	DEVICE DESCRIPTION	PART#	ADDRESS	J7AEN PORT MAPPING
EVM	Board ID EEPROM	AT24C512C-MAHM-T	0X51	WKUP_I2C0
EXP/QSGMII -1	Board ID EEPROM	CAT24C256WI-GT3	0X54	
EXPANSION	User Expansion Connector	<connector interface>	0X50	
EVM	VDD_CORE REGULATOR	TPS62875	0X44	
EVM	PMIC	TPS65221-Q1	0x48,0x49, 0x4A, 0x4B	
EXPANSION	User Expansion Connector	<connector interface>		MCU_I2C0
EVM	PMIC	TPS65221-Q1	NA	
EXP/QSGMII -1	ENET	<connector interface>		SOC_I2C0
EVM	IO Expander 1	TCA6424ARGJR	0X23	
EVM	Temperature Sensors	TMP100NA/3K	0X48,0X49	
EVM	AUDIO CODEC	TLV320AIC3106IRGZT	0X1B	
EVM	Test automation	FH12A-40S		
EVM	x1LANE PCIe0	<connector interface>		
EVM	USB C PD Controller	TPS25750D	0X20	
EVM	INA226 device for VDD_CORE	INA226AIDGSR	0X40	
EVM	INA226 device for VDD_RAM_0V85	INA226AIDGSR	0X41	
EVM	INA226 device for VDA_PHY_1V8	INA226AIDGSR	0X42	
EVM	INA226 device for VDD_IORET_CORE	INA226AIDGSR	0X43	
EVM	INA226 device for VDD_SD_DV	INA226AIDGSR	0X44	
EVM	INA226 device for VDD_IO_1V8	INA226AIDGSR	0X45	
EVM	INA226 device for VSYS_3V3	INA226AIDGSR	0X46	
EVM	INA226 device for VDD_DDR_1V1	INA226AIDGSR	0X47	
EVM	INA226 device for VDD_IO_3V3	INA226AIDGSR	0X4C	
EVM	INA226 device for VDA_PLL_1V8	INA226AIDGSR	0X4D	
	INA226 device for VDD1_DDR_1V8	INA226AIDGSR	0X4E	
EVM	CLKGEN 2	LMK3H0102	0x68	
EVM	Bootmode Buffer	TCA6424ARGJR	0x22	TA_I2C_SCL
EVM	IO Expander	TCA6416ARTWR	0X20	SOC_I2C1
EVM	HDMI	Sii9022ACNU	0x3B, 0x3F, 0x62	
EVM	DSI Flex Connector	<connector interface>(Via Mux)		
EVM	DSI to eDP Bridge	SN65DSI86IPAPQ1(Via Mux)	0X2C	
EVM	OLDI	<connector interface>		
EVM	I2C switch	TCA9543APWR	0X70,0X71	SOC_I2C2(Via Mux)
EVM	CSI2_A Expansion Connector	QSH-020-01-L-D-DP-A-K(J1002)	From 0x70 Switch	CSI0_I2C2_SDA
EVM	FPC Camera Connector 1	CON_FLEX_22X1_52435(J1004)		
EVM	FPC Camera Connector 2	CON_FLEX_22X1_52435(J1005)		CSI1_I2C2_SDA
EVM	CSI2_B Expansion Connector	QSH-020-01-L-D-DP-A-K(J1003)	From 0x71 Switch	CSI2_I2C2_SDA
EVM	FPC Camera Connector 3	CON_FLEX_22X1_52435(J1006)		
EVM	FPC Camera Connector 4	CON_FLEX_22X1_52435(J1007)		CSI3_I2C2_SDA

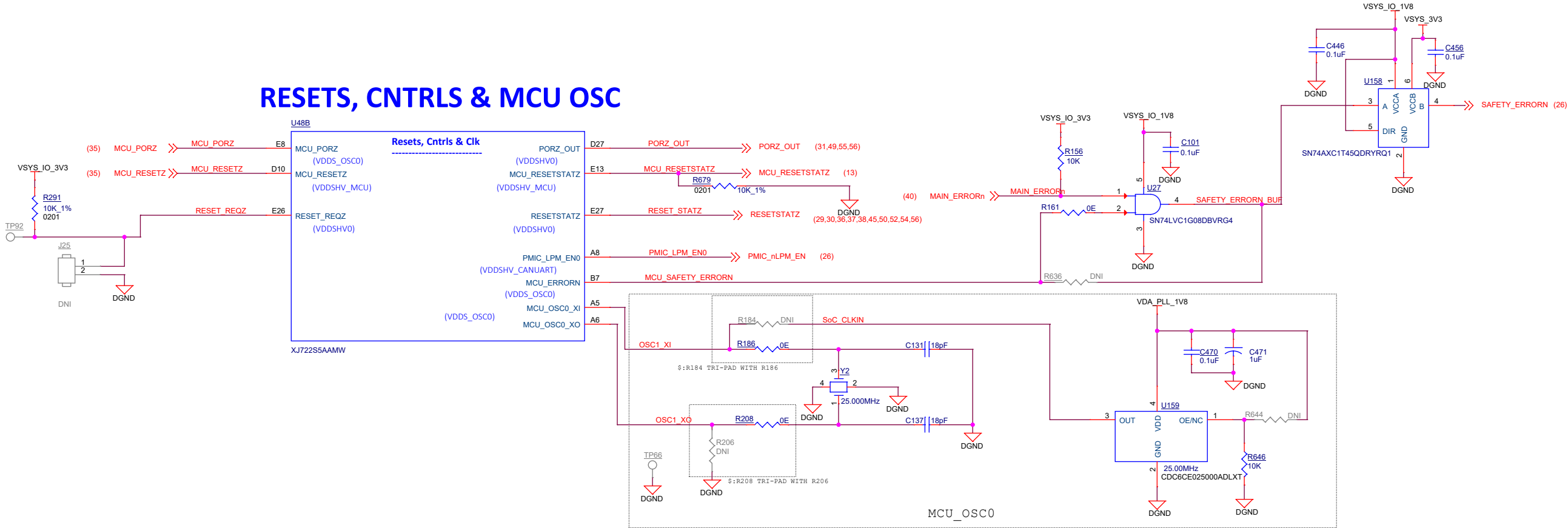
GPIO EXPANDER MAP/TABLE

	GPIO net name	Package Signal name	GPIO No	Input/Output	Default	State	Usage
SOC GPIO	SOC GPIO						
	MCU_INTn_1V8	OSPIO_CSN1	GPIO0_12	Input	PU	Active Low	PMIC Interrupt
	RGMII1_INT#	OSPIO_CSN2	GPIO0_13	Input	PU	Active low	MCU Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
	OSPIO_INT#/ECC_FAIL	OSPIO_CSN3	GPIO0_14	Input	PU	Active Low	Interrupt from OSPI to SoC
	CSI2_EXP_A_GPIO0	GPMC0_CLK	GPIO0_31	IO	NA	NA	CSI2 Expansion Board Specific. 1:2 Mux on the path
	CSI2_EXP_A_GPIO1	GPMC0_AD0	GPIO0_15	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_A_GPIO2	GPMC0_AD1	GPIO0_16	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_A_GPIO3	GPMC0_AD2	GPIO0_17	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_A_GPIO4	GPMC0_AD3	GPIO0_18	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_B_GPIO0	MMC2_CLK	GPIO0_69	IO	NA	NA	CSI2 Expansion Board Specific.
	CSI2_EXP_B_GPIO1	GPMC0_AD4	GPIO0_19	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_B_GPIO2	GPMC0_AD5	GPIO0_20	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_B_GPIO3	GPMC0_AD6	GPIO0_21	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	CSI2_EXP_B_GPIO4	GPMC0_AD7	GPIO0_22	IO	NA	NA	CSI2 Expansion/RPI Camera Board Specific. 1:2 Mux on the path
	EXP_GPIO0_33	GPMC0_OEn_REn	GPIO0_33	IO	NA	NA	User Expansion Specific.1:2 Mux on the path
	EXP_GPIO0_36	GPMC0_BE1n	GPIO0_36	IO	NA	NA	User Expansion Specific.1:2 Mux on the path
	EXP_GPIO0_38	MCU_UART0_CTSn	MCU_GPIO0_7	IO	NA	NA	User Expansion Specific.
	EXP_GPIO0_39	MCU_UART0_RTSn	MCU_GPIO0_8	IO	NA	NA	User Expansion Specific.1:2 Mux on the path
	EXP_GPIO0_41	GPMC0_CSn0	GPIO0_41	IO	NA	NA	User Expansion Specific.1:2 Mux on the path
	EXP_GPIO0_42	GPMC0_CSn1	GPIO0_42	IO	NA	NA	User Expansion Specific.1:2 Mux on the path
	IOEXP1_INT#	MMC2_DAT1	GPIO0_67	Input	PU	Active low	Interrupt for IO Expander 1 ('0' - Interrupt, '1' - No interrupt)
	CSI2_EXP_RSTz	MMC2_DAT0	GPIO0_68	Output	PD	Active low	CSI2 Expansion Interface Reset ('0' - device reset, '1' - normal operation)
	SEL_SDIO_3V3_1V8n	MMC2_CMD	GPIO0_70	Output	PU	Active low	SW controls & transition Sd card to high speed 1.8V signaling if card type supports
	ENET1_EXP_INTB	MMC2_SDWP	GPIO0_72	Input	PU	Active low	ENET expansion 1 Interrupt signal
	EN_EFUSE_VPP	SPI0_D1	GPIO1_19	Output	PD	Active High	VPP_EFUSE LDO enable
	SYS_MCU_PWRDN	EXT_REFCLK1	GPIO1_30	Output	NA	Active low	SYS_MCU_PWRDN('1' - PWR ON, '0' - PWR OFF)
	TA_SOC_INT1z	EXTINTn	GPIO1_31	Input	PU	Active low	Test automation Interrupt to SOC
	SOC_GPIO1_49	MMC1_SDWP	GPIO1_49	Output	NA	Active High	User LED1 ('1' - LED ON, '0' - LED OFF)
	TA_SOC_INT2z/SOC_WAKE	WKUP_UART0_CTSn	MCU_GPIO0_11	Input	PU	Active low	Test automation Interrupt to SOC
	MCU_CAN_STB	WKUP_UART0_RTSn	MCU_GPIO0_12	Output	PU	Active High	Wake from IO retention mode
	TRIG_WDOG	WKUP_CLKOUT	MCU_GPIO0_23	Input	NA	Active Low	MCU CAN0 Standby
		MMC2_SDCD	GPIO0_71				Trigger WDOG to PMIC
							Open
I2C0/0X23	GPIO Expander - 1 Part # TCA6424ARGJR						
	TRC_MUX_SEL		P00	Output	PU	NA	Mux Select Line('0'- MCASP&User Expansion,'1'-TRC data)(Default to TRACE)
	OSPI/ONAND_MUX_SEL		P01	Output	DIP_SEL	NA	Flash Memory Selection ('0' - OSPIO, '1' - OCTAL NAND)
	MCASP1_FET_SEL		P02	Output	PD	Active low	McASP1 FET SWITCH Select Line ('1' - Audio, '0' - HDMI)
	CTRL_PM_I2C_OE#		P03	Output	PU	Active High	I2c Switch Enable ('1' - Enable, '0' - Disable)
	CSI_VIO_SEL		P04	Output	DIP_SEL	Active High	LVC MOS IO Voltage Selection Enable Pin('0'- xxV, '1'- xxV)
	USB2_0_MUX_SEL		P05	Output	PD	Active low	Mux Select Line ('1'- D to 2D, '0'- D to 1D)
	CSI01_MUX_SEL_2		P06	Output	PD	Active low	CSI MUX select ('0'- D to A,'1'-D to B)
	CSI23_MUX_SEL_2		P07	Output	PD	Active low	CSI MUX select ('0'- D to A,'1'-D to B)
	LMK1_OE1		P10	Output	PU	Active low	Clock generator 1 Output 1 Enable
	LMK1_OE0		P11	Output	PU	Active low	Clock generator 1 Output 0 Enable
	LMK2_OE0		P12	Output	PU	Active low	Clock generator 2 Output 0 Enable
	LMK2_OE1		P13	Output	PU	Active low	Clock generator 2 Output 1 Enable
	GPIO_RGMII1_RST#		P14	Output	PU	Active low	Reset for RGMII ('1' - Enable, '0' - Disable)
	GPIO_AUD_RSTn		P15	Output	PU	Active low	Reset for Audio ('1' - Enable, '0' - Disable)
	GPIO_eMMC_RSTn		P16	Output	PU	Active low	Reset for Emmc ('1' - Enable, '0' - Disable)
	GPIO_uSD_PWR_EN		P17	Output	PU	Active High	Load switch ('1' - ON, '0' - OFF)
	USER_LED2		P20	Output	PD	Active low	User LED2 Enable ('1' - LED Off, '0' - LED On)
	MCAN0_STB		P21	Output	PU	Active High	MCAN0 Standby
	PCIE0_1L_RC_RSTz		P22	Output	PD	Active low	PCIE1 1-Lane RC Reset Control ('0' - device reset, '1' - normal operation)
	PCIE0_1L_PRSENT#		P23	Input	PU	Active High	PCIE0 1-Lane Hot Plug / Card Detect ('0' - PCIE Card Detected, '1' - no card detected)
	ENET1_EXP_SPARE2		P24	Input	NA	NA	Ethernet Expansion1 Spare2 ('0' - not defined, '1' - not defined)
	ENET1_EXP_PWRDN		P25	Output	PU	Active High	Ethernet Expansion1 PHY Powerdown ('0' - normal operation, '1' - device power down)
	ENET1_I2CMUX_SEL		P26	Output	PD	NA	Signal Mux Control ('0' - No Connect, '1' - I2C0)
	ENET1_EXP_RESETZ		P27	Output	PD	Active low	Ethernet Expansion1 Reset ('0' - device reset, '1' - normal operation)
I2C1/0X22	GPIO Expander - 2 Part # TCA6416ARTWR						
	DSI_Mux_SEL_2		P00	Output	PD	Active High	DSI Mux Select ('1'- DSI FPC Connector,'0'- DSI to EDP)
	GPIO_eDP_ENABLE		P01	Output	PD	Active High	eDP Bridge Enable
	DPO_PWR_SW_EN		P02	Output	PD	Active High	Enalbe for Display port LDO
	GPIO_OLDI_RSTn		P03	Output	PD	Active low	Reset for OLDI ('1' - Enable, '0' - Disable)
	GPIO_HDMI_RSTn		P04	Output	PD	Active low	HDMI Transmitter Reset Control GPIO
	HDMI_LS_OE		P05	Output	PD	NA	HDMI ESD Device
	PCIE0_1L_PERSTz		P06	Input	NA	NA	PCIE0 1-Lane Bus Reset ('0' - device reset, '1' - normal operation)
	DSI_GPIO0		P10	IO	NA	NA	DSI flex Connector
	DSI_GPIO1		P11	IO	NA	NA	DSI flex Connector
	DSI_EDID		P12	Input	NA	Active low	Interrupt
	IO_eDP_IRQ		P13	Input	PU	NA	Interrupt signal from DSI to eDP bridge
	OLDI_INT#		P14	Input	PU	Active low	Interrupt from OLDI display
	HDMI_INTn		P15	Input	PU	Active low	Interrupt from HDMI display

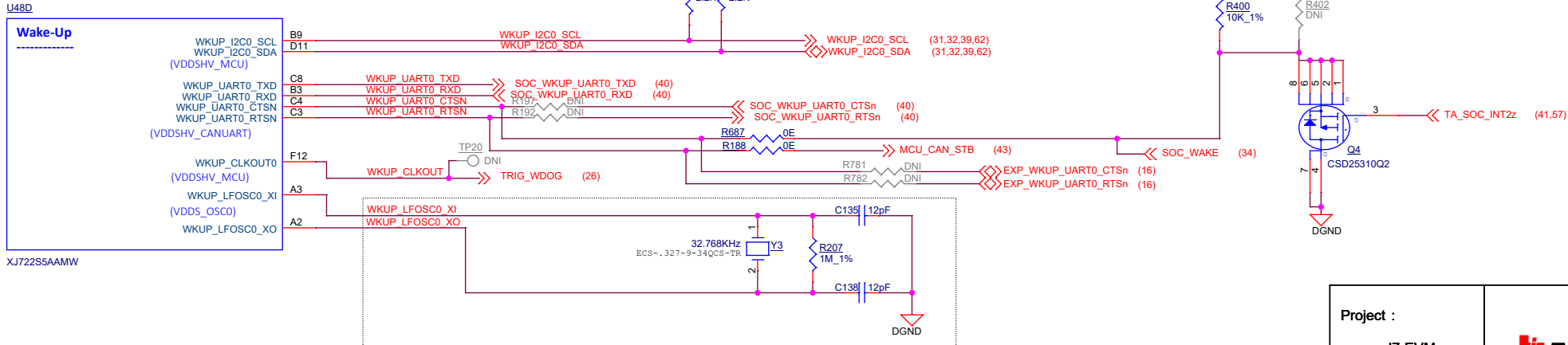
MCU GENERAL IO



RESETS, CNTRLS & MCU OSC



WKUP RESETS, CNTRLS & OSC



Project :

J7 EVM



Title
SOC MCU IO CNTRLOSC & WKUP

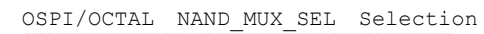
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E1

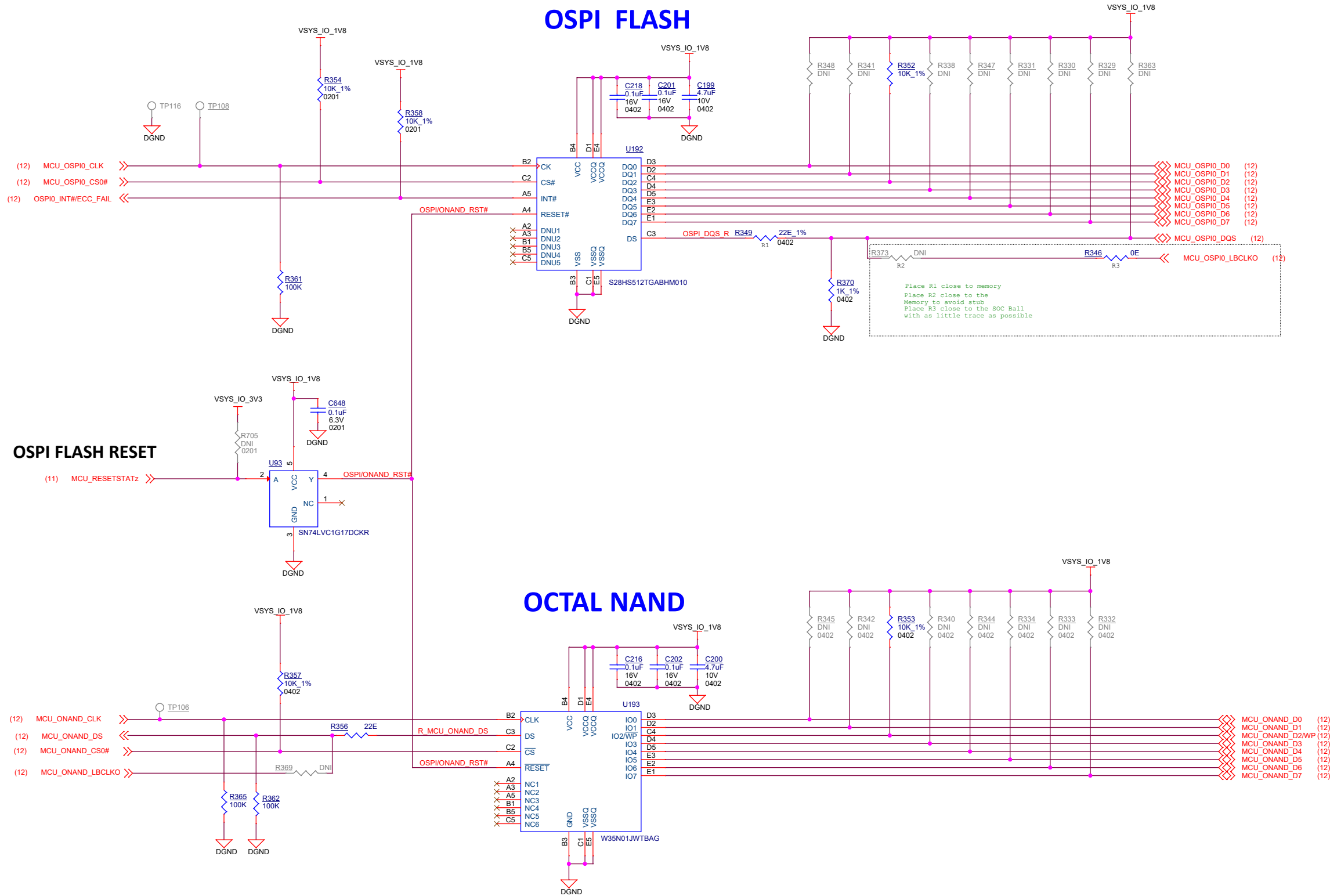
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2:1 Mux for OSPI/OCTAL NAND

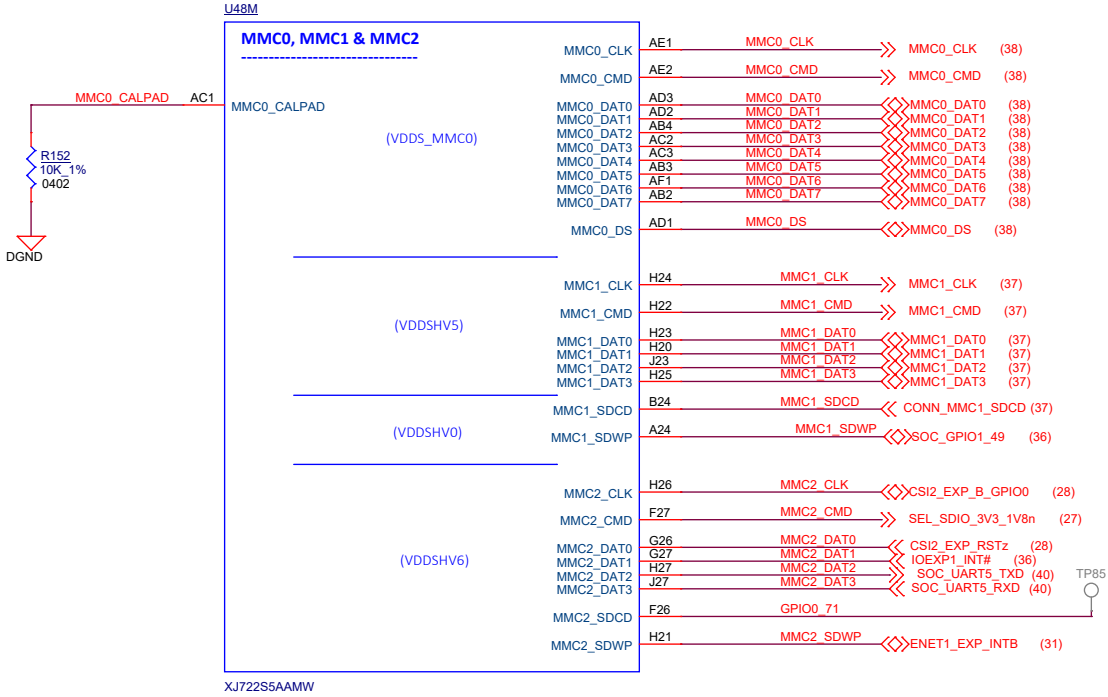


'0' - (A --> B) OSPI Flash
'1' - (A --> C) OCTAL NAND
Note: Default set by dip switch

OSPI/ONAND_MUX_SEL (36)

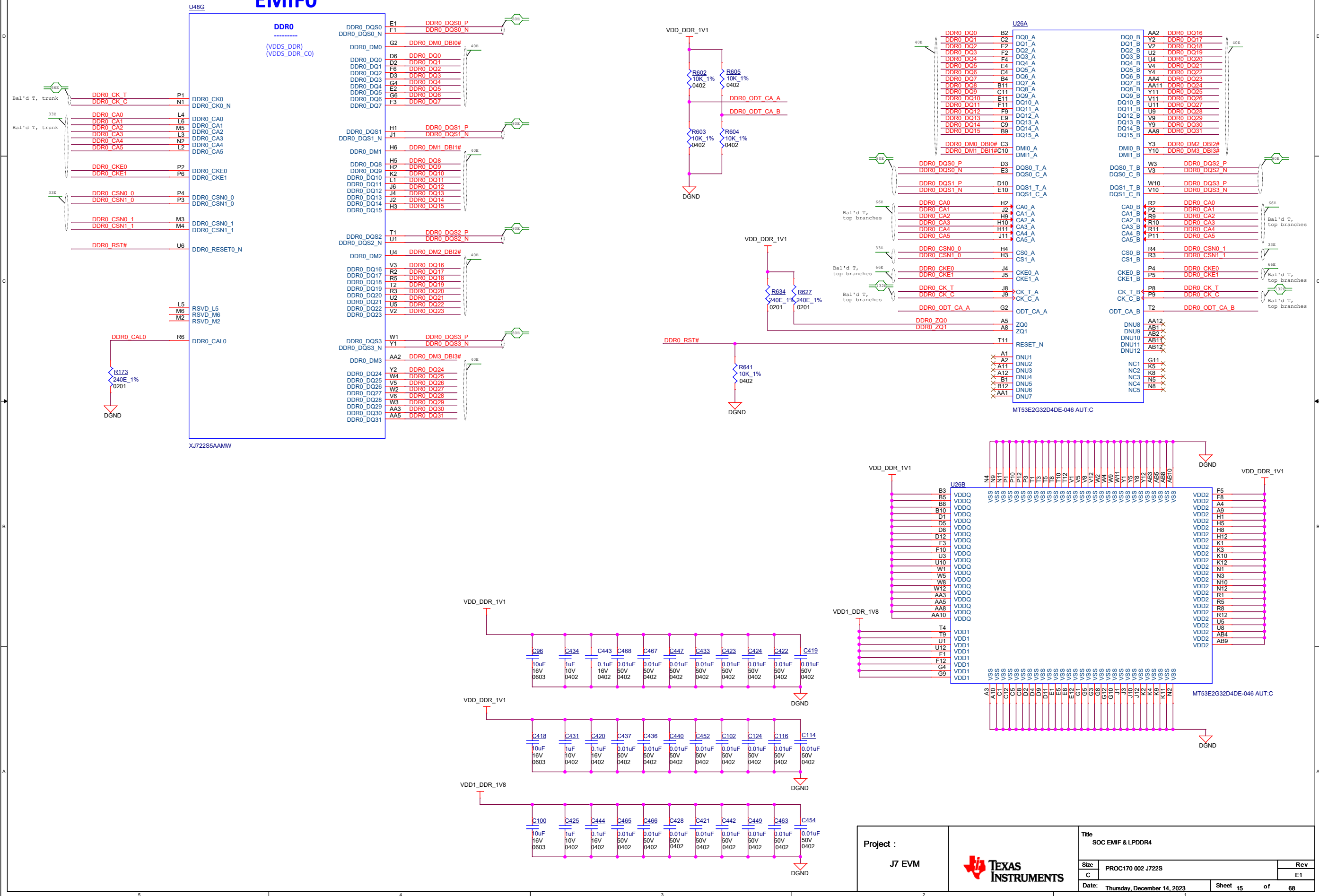


MMC 0, 1, 2



LPDDR4 MEMORY I/F

EMIF0



U48A

General IO

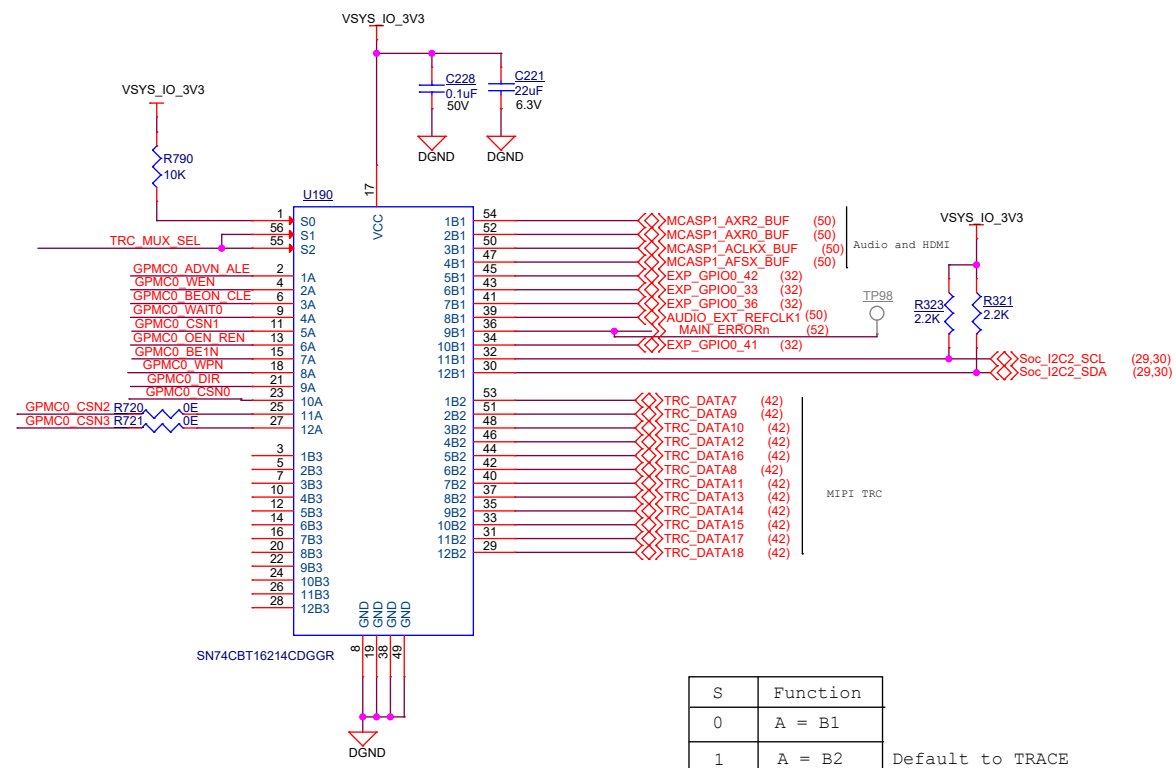
(VDDSHV0)

The diagram shows the General IO block (U48A) connected to several peripheral modules:

- I2C0:** I2C0_SCL (D23) and I2C0_SDA (B22) connect to SOC_I2C0_SCL and SOC_I2C0_SDA (pins 31,33,36,39,50,55,57,58).
- I2C1:** I2C1_SCL (C24) and I2C1_SDA (A22) connect to SOC_I2C1_SCL and SOC_I2C1_SDA (pins 36,52,54).
- SPI0:** SPI0_CLK (D20), SPI0_CS0 (B20), SPI0_CS1 (C20), SPI0_D0 (E19), and SPI0_D1 (E20) connect to EHRPWM1_A, EHRPWM0_A, ECAP0_IN_APWM_OUT, EHRPWM1_B, and EN_EFUSE_VPP (pins 32, 27, 16).
- UART0:** UART0_TXD (F20), UART0_RXD (F19), UART0_CTSN (B21), and UART0_RTSN (B21) connect to SOC_UART0_TXD, SOC_UART0_RXD, UART0_CTSN, and UART0_RTSN (pins 40, 40, 40).
- EXTINTN:** EXTINTN (B23) connects to EXT_REFCLK1 (A23), which then connects to SYS_MCU_PWRDN (pin 34).
- MCAN0:** MCAN0_TX (D22) and MCAN0_RX (C22) connect to MCAN0_TX (pin 44) and MCAN0_RX (pin 44).
- MCASP0:** MCASP0_ACLKR (F24), MCASP0_AFSR (C27), MCASP0_AXR0 (F23), MCASP0_AXR1 (B25), MCASP0_AXR2 (A26), MCASP0_AXR3 (A25), MCASP0_ACLKX (D25), and MCASP0_AFSX (C26) connect to UART1_TXD, UART1_RXD, MCASP0_AXR0, MCASP0_AXR1, UART1_RTSn, UART1_CTSn, MCASP0_ACLKX, and MCASP0_AFSX (pins 32, 32, 32, 32, 32, 32).

A level shifter circuit is shown on the right, consisting of a 3V3 supply, a 10K resistor (R690), and a CSD25310Q2 MOSFET (Q5) connected to TA_SOC_INT1z (pin 41,57).

XJ722S5AAMW



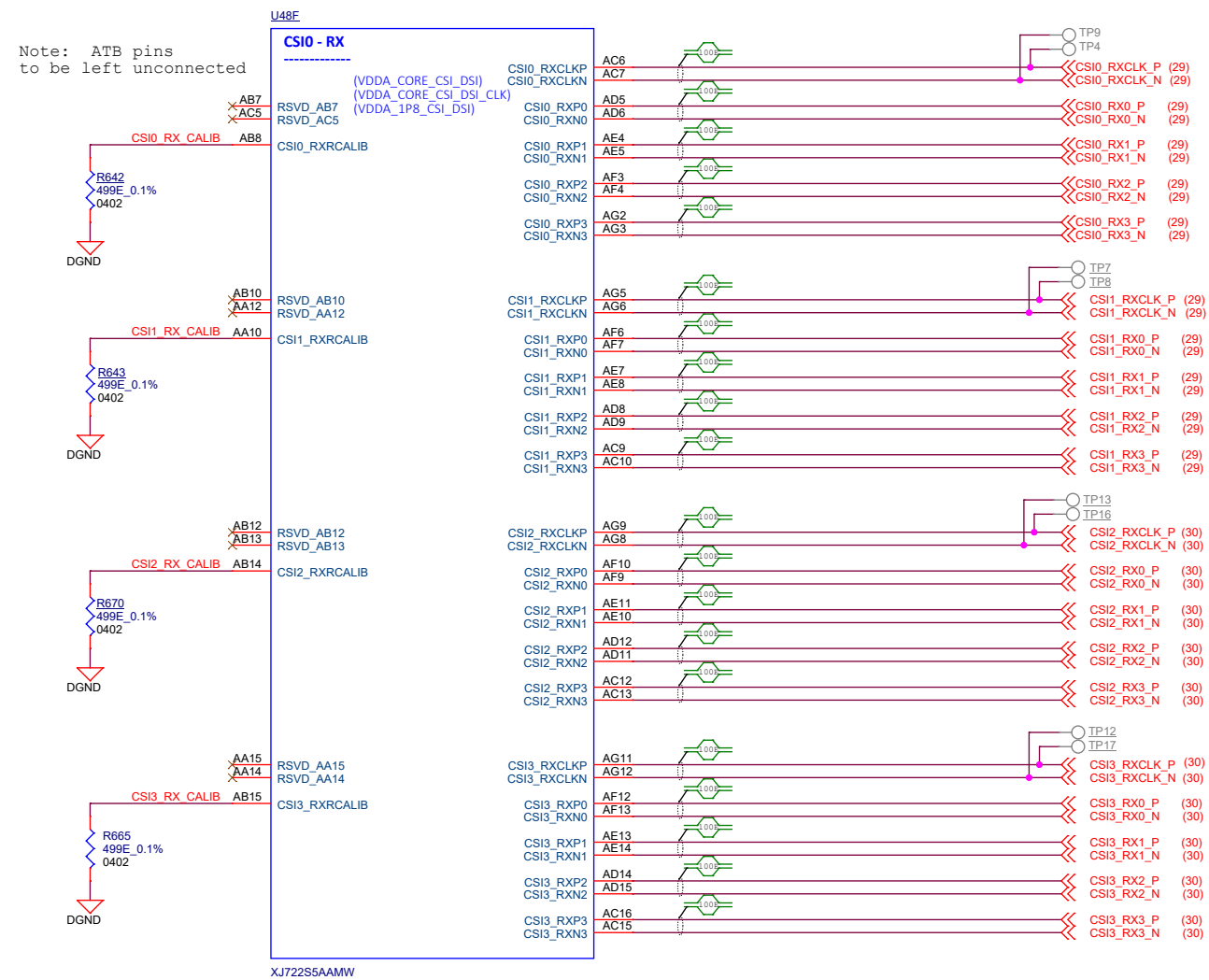
S	Function
0	A = B1
1	A = B2

Default to TRACE

The diagram shows the connection of the GPMC0 module to the SN74CBT16214CDGGR. The GPMC0 module is connected to the SN74CBT16214CDGGR via a 0.1uF capacitor. The GPMC0 module is connected to the SN74CBT16214CDGGR via a 0.1uF capacitor. The GPMC0 module is connected to the SN74CBT16214CDGGR via a 0.1uF capacitor.

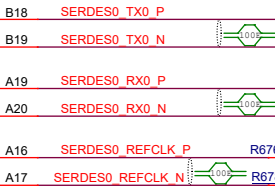
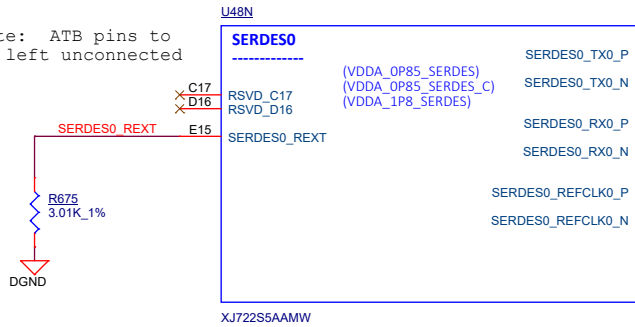
NOTE: 1K Resistors are used to isolate the BOOTMODE control logic after the value is latched

CSI 0, 1, 2, 3



SERDES0

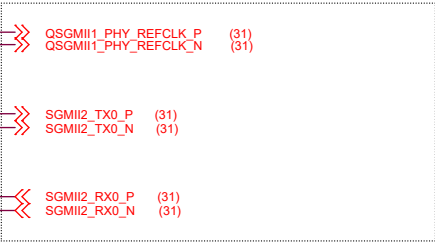
Note: ATB pins to be left unconnected



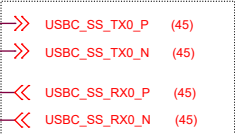
For External 156.25MHz Clk support:
DNI: R676, R678
Assemble: R64,R59,R63,R60

For SoC 156.25MHz Clk support:
DNI: R64,R59
Assemble: R676,R678,R63, R60

ENET EXPANSION

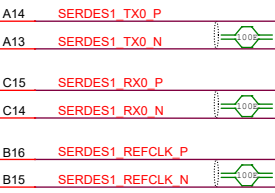
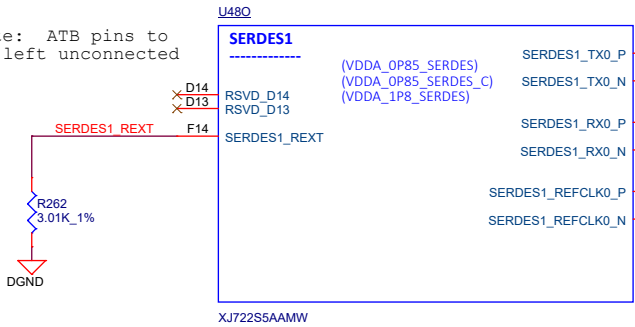


USB 3.0 HUB

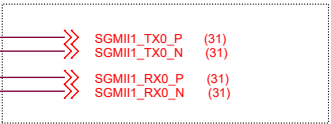


SERDES1

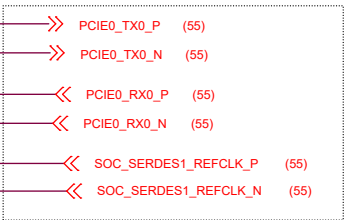
Note: ATB pins to be left unconnected



ENET EXPANSION



PCIe x4L Connector



Project :

J7 EVM



Title
SOC SERDES 0 & 1

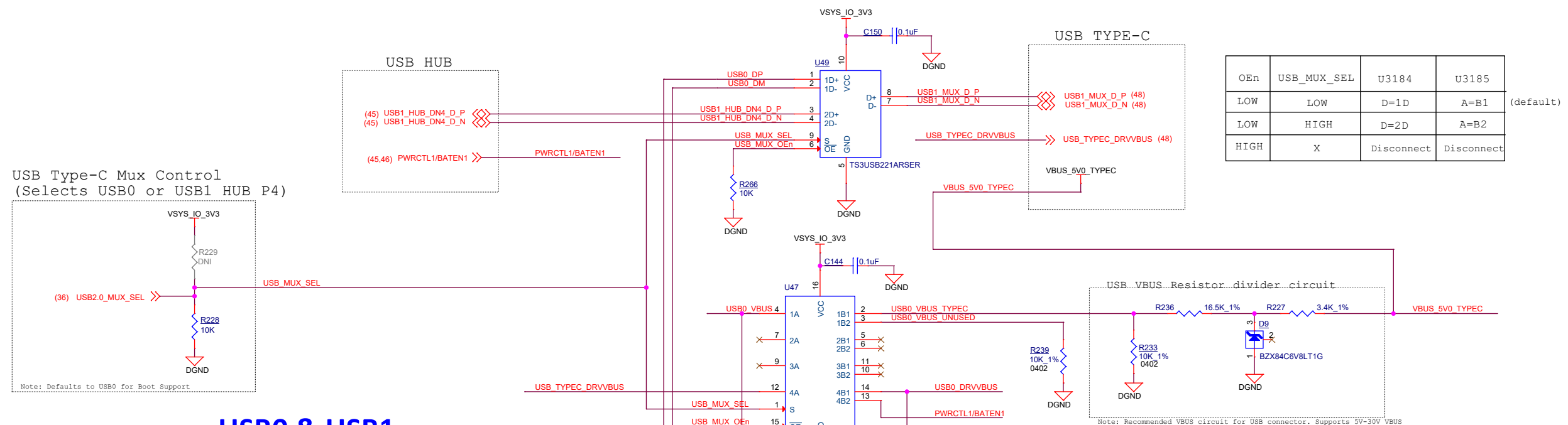
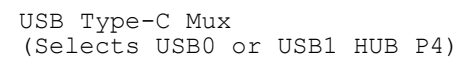
Size
C PROC170 002 J722S

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Rev
E1

U48L							
RGMII	MDIO0_MDIO	AD25	MCU MDIO0 MDIO				
	MDIO0_MDC	AC24	MCU MDIO0 MDC				
	RGMII1_RD0	AC25	MCU RGMII1 RD0				
	RGMII1_RD1	AD27	MCU RGMII1 RD1				
	RGMII1_RD2	AE24	MCU RGMII1 RD2				
	RGMII1_RD3	AE26	MCU RGMII1 RD3				
	RGMII1_RX_CTL	AD23	MCU RGMII1 RX_CTL				
	RGMII1_RXC	AE27	MCU RGMII1 RXC				
	RGMII1_TD0	AF27	MCU RGMII1 TD0				
	RGMII1_TD1	AE23	MCU RGMII1 TD1				
	RGMII1_TD2	AG25	MCU RGMII1 TD2				
	RGMII1_TD3	AF24	MCU RGMII1 TD3				
	RGMII1_TX_CTL	AF25	MCU RGMII1 TX_CTL				
	RGMII1_TXC	AG26	MCU RGMII1 TXC				



The schematic diagram illustrates the USB HUB interface circuit. The U48P (XJ722S5AAMW) is connected to the USB HUB. The U48P has pins for USB0 and USB1, including DP, DM, VBUS, DRVVBUS, and CLKREQN. The USB HUB has pins for USB1_HUB_D_P, USB1_HUB_D_N, USB_VBUS, and USB_HUB_DRVVBUS. The circuit includes resistors R182, R275, R265, and R261, and a voltage divider circuit for USB VBUS. The USB HUB is connected to a 5V supply and GND.

U48P (XJ722S5AAMW) Pins:

- AA6: USB0_DP
- AB5: USB0_DM
- W7: USB0_VBUS
- E25: USB0_DRVVBUS
- D17: USB1_DP
- E17: USB1_DM
- F18: USB1_VBUS
- B27: USB1_DRVVBUS
- F25: PCIE0_CLKREQN

USB HUB Pins:

- USB1_HUB_D_P (45)
- USB1_HUB_D_N (45)
- USB_VBUS (45)
- USB_HUB_DRVVBUS (45)

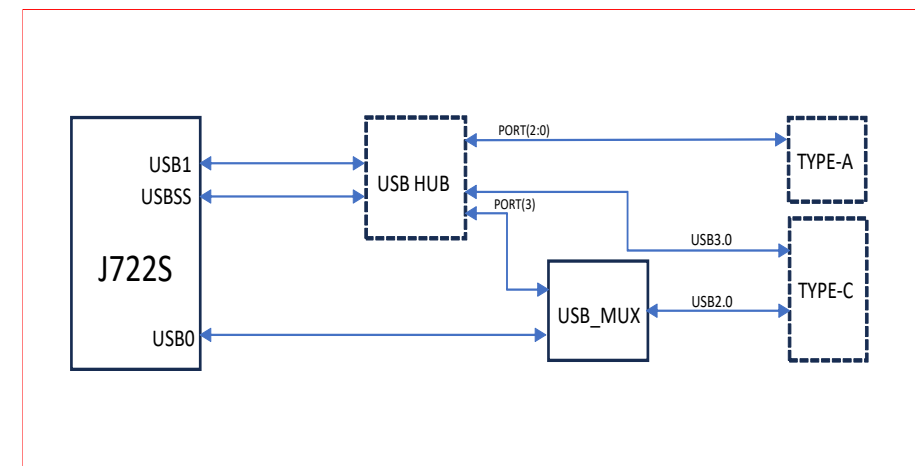
Resistors and Components:

- R182: 499E 0.1% (connected to AA8)
- R275: 499E 0.1% (connected to E18)
- R265: 9.09K 1% (connected to F18)
- R261: 10K 1% (connected to B27)

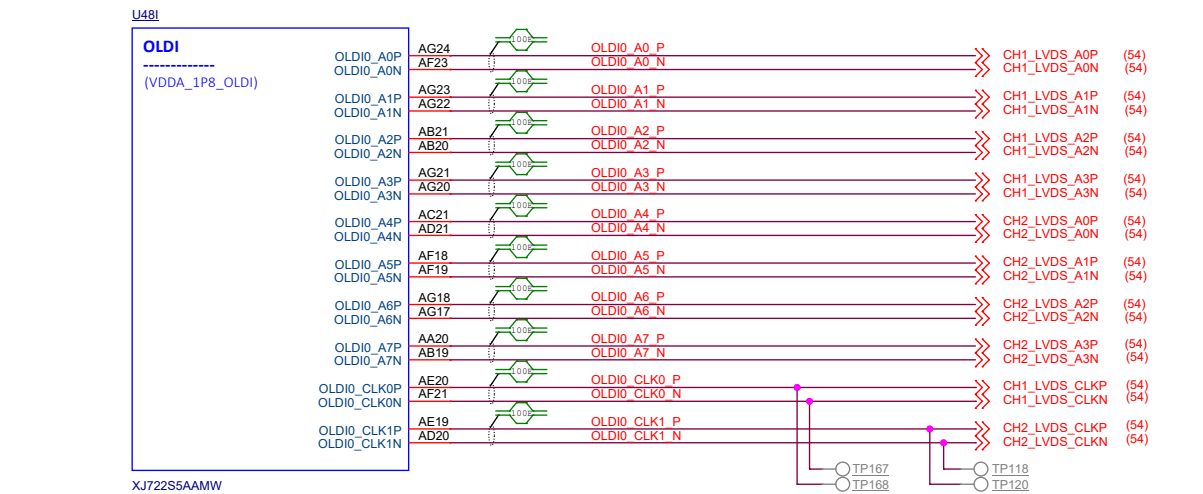
Connections:

- AA8: USB0_RCALIB
- E18: USB1_RCALIB
- AA6: USB0_DP
- AB5: USB0_DM
- W7: USB0_VBUS
- E25: USB0_DRVVBUS
- D17: USB1_DP
- E17: USB1_DM
- F18: USB1_VBUS
- B27: USB1_DRVVBUS
- F25: PCIE0_CLKREQN

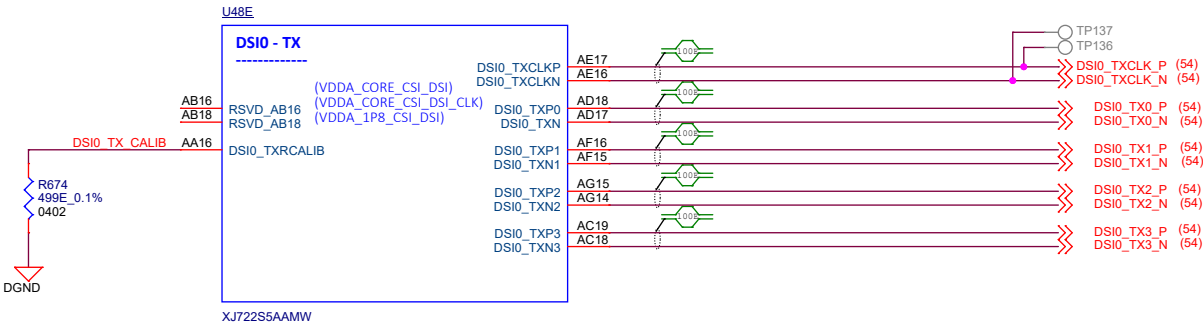
Note: USB VBUS Resistor divider circuit.



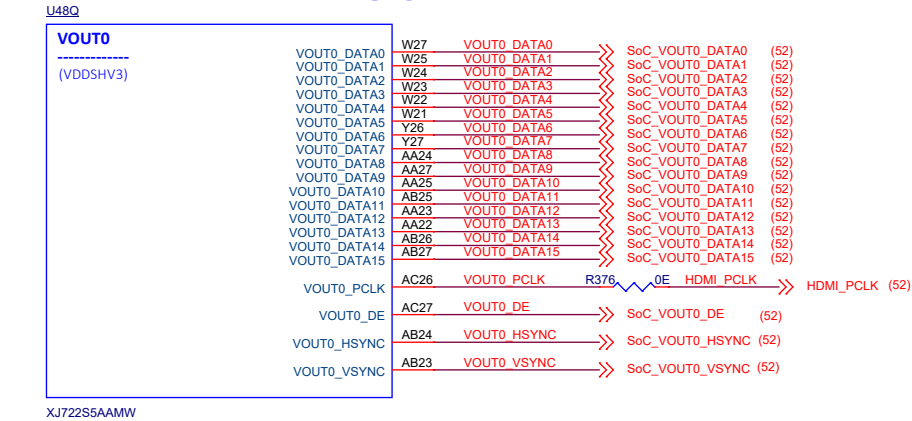
OLDI



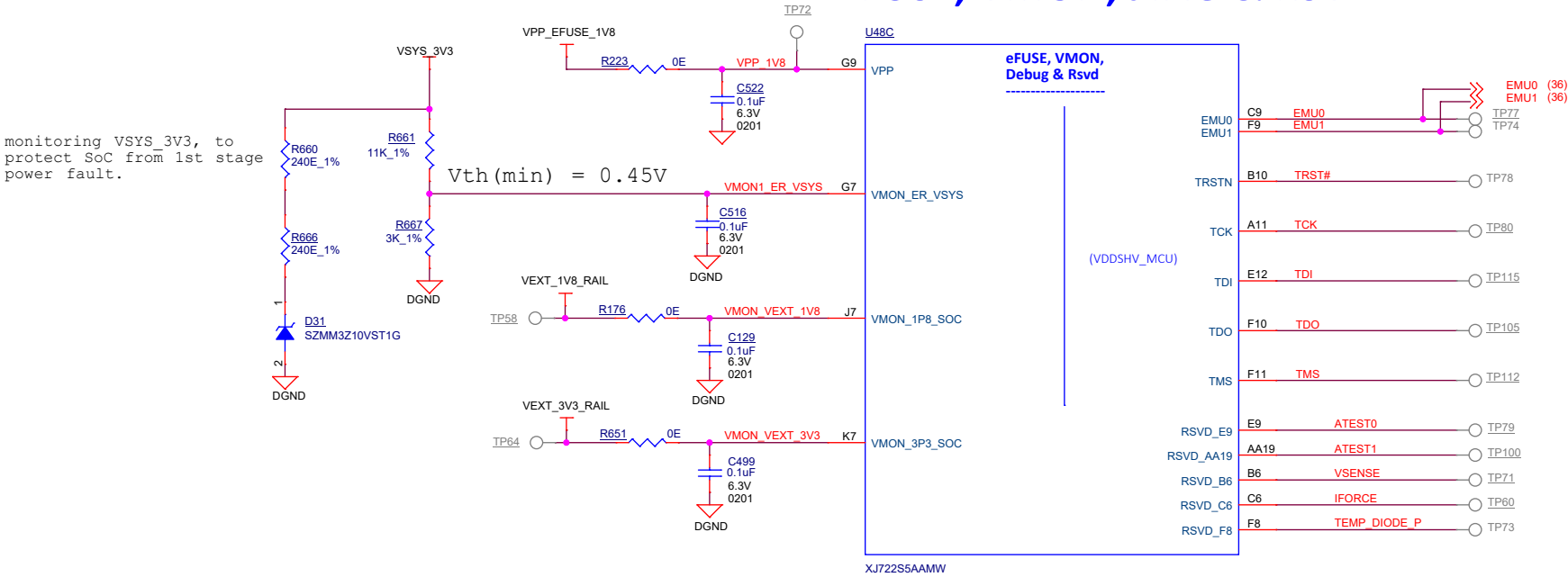
DSI



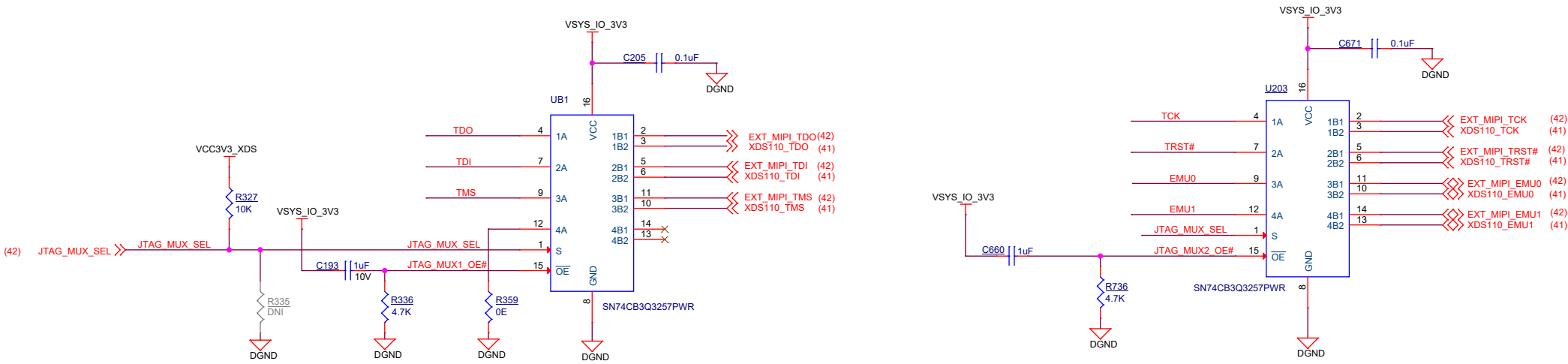
VOUT



EFUSE, VMON, JTAG & RSVD

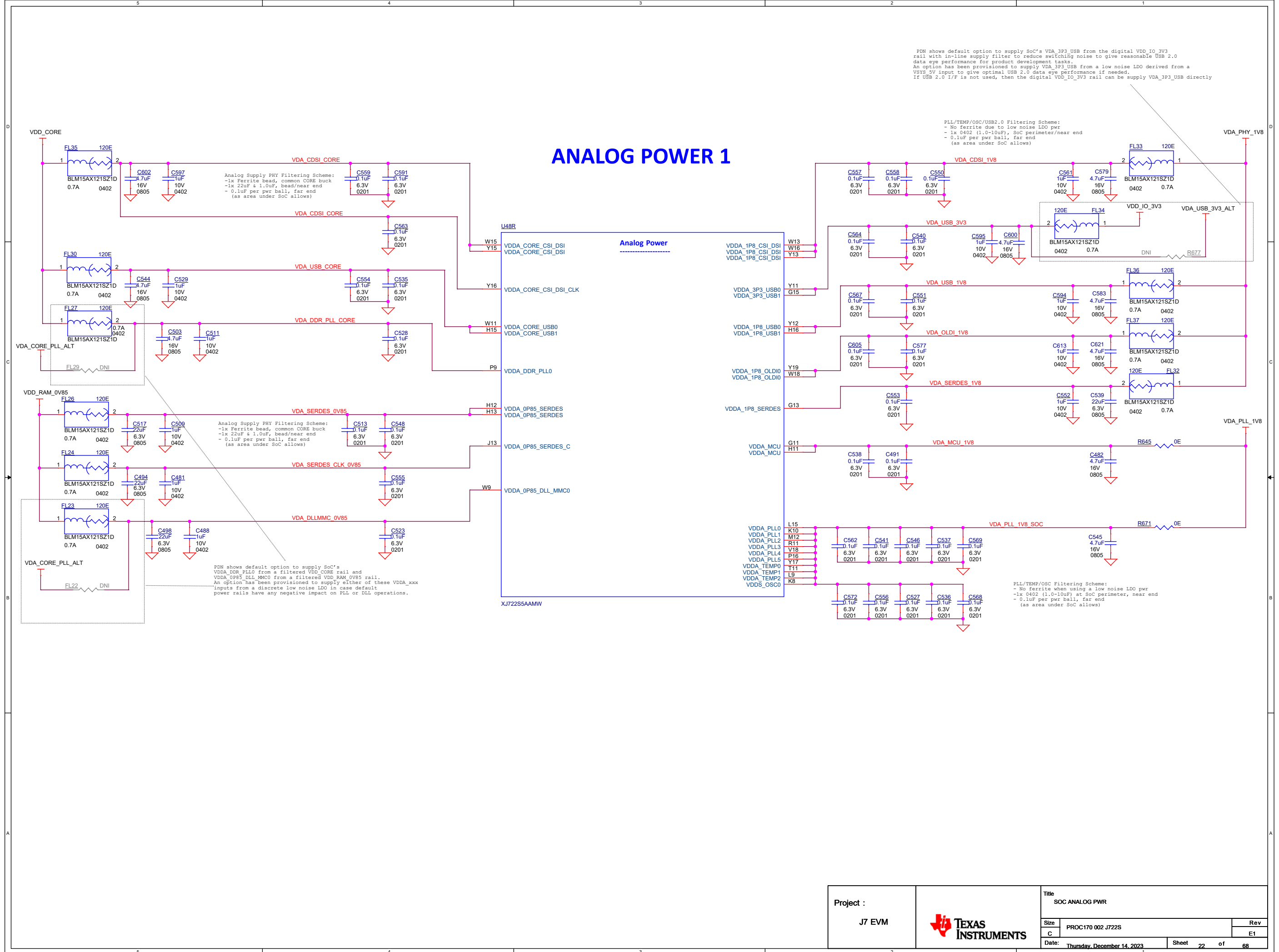


JTAG AND TRACE MUX

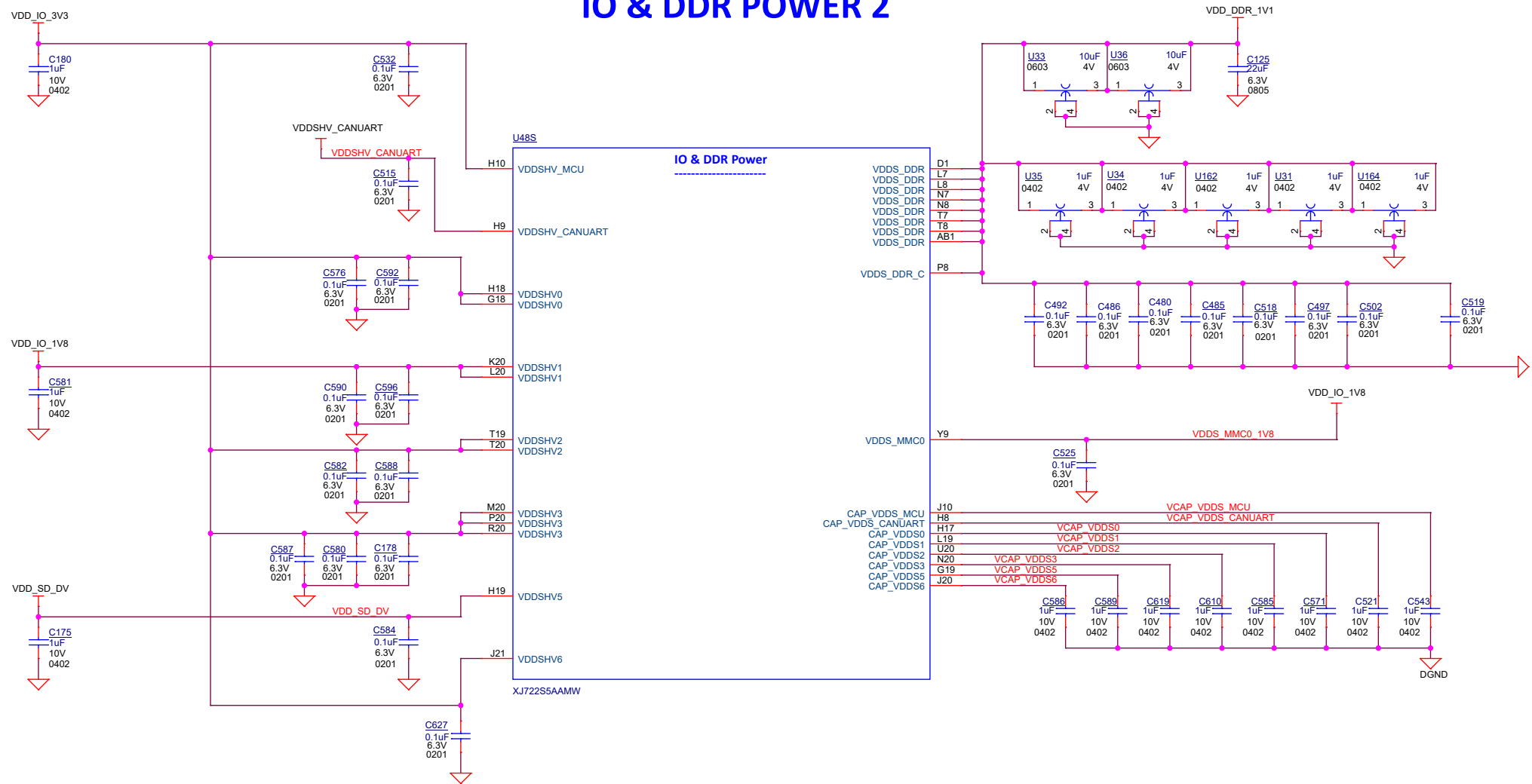


JTAG - 1:2 MUX : Truth Table

MUX_SEL	CONDITION	FUNCTION
LOW	External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU] (default)
HIGH	No External Emulator attached & XDS110 Powered via USB	A-->B2 port [ON Board EMU]
LOW	External Emulator attached & XDS110 Powered via USB	A-->B1 port [EXTERNAL EMU]
LOW	No External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]



IO & DDR POWER 2

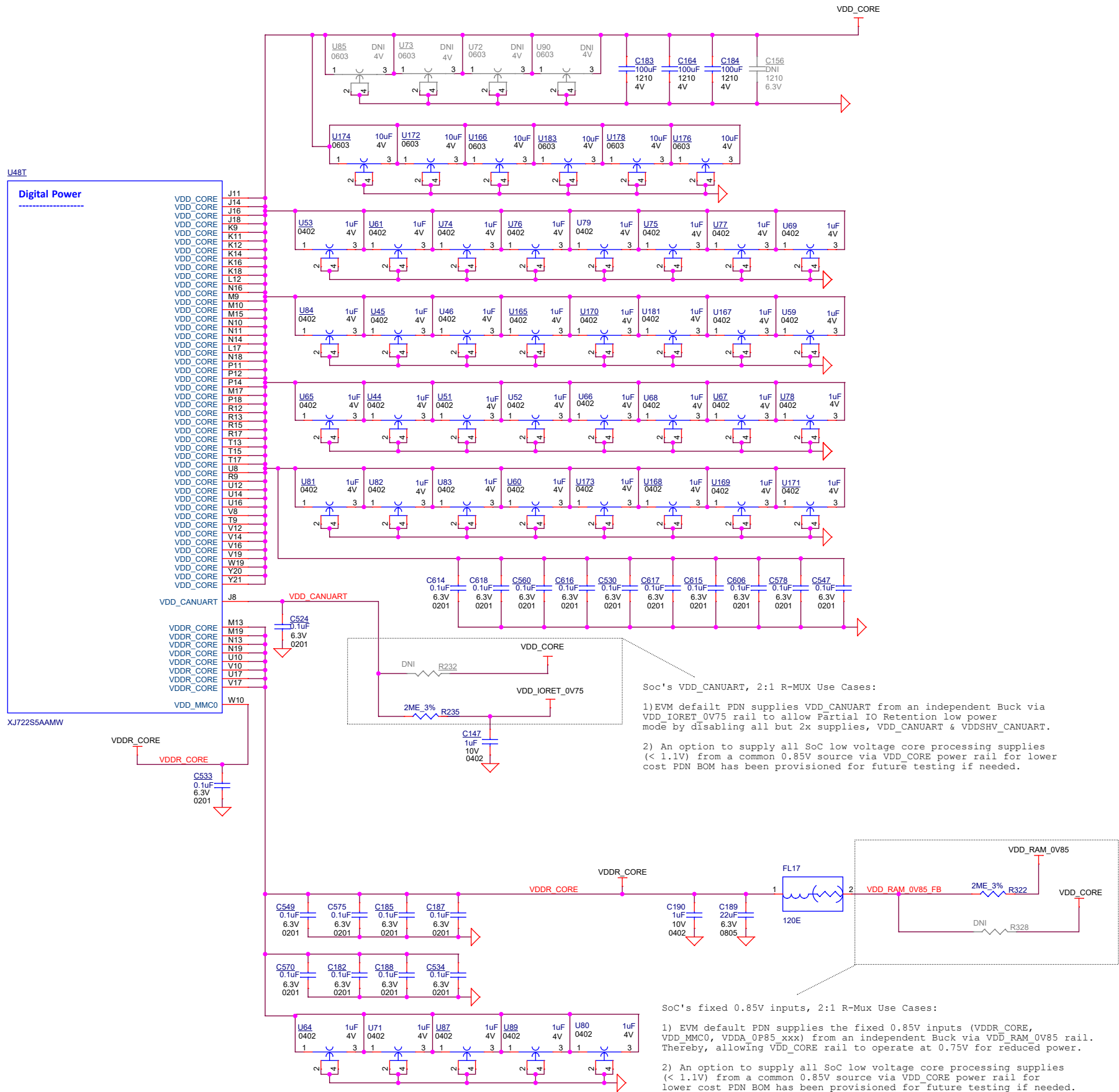


Note:

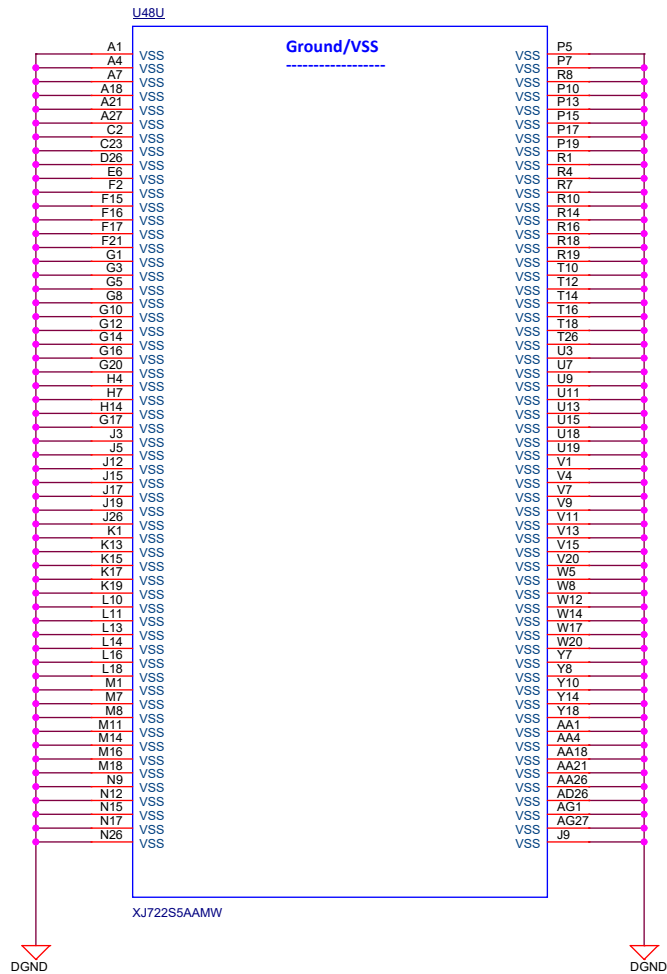
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

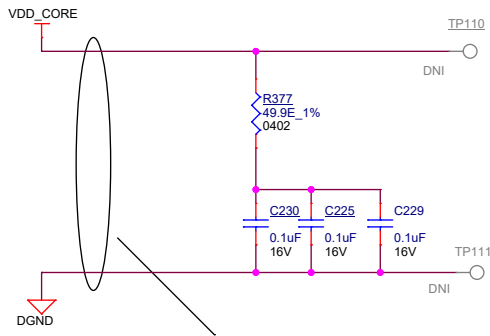
DIGITAL POWER 3



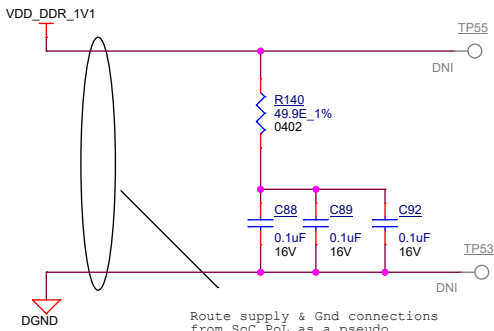
SOC GROUND



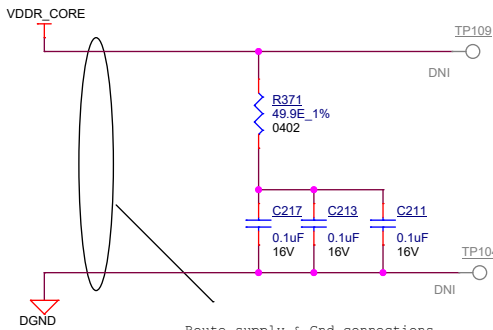
SoC Supply Noise Kelvin Sensing



Route supply & Gnd connections from SoC Pol as a pseudo differential pair to TPs near R & C termination for easy access

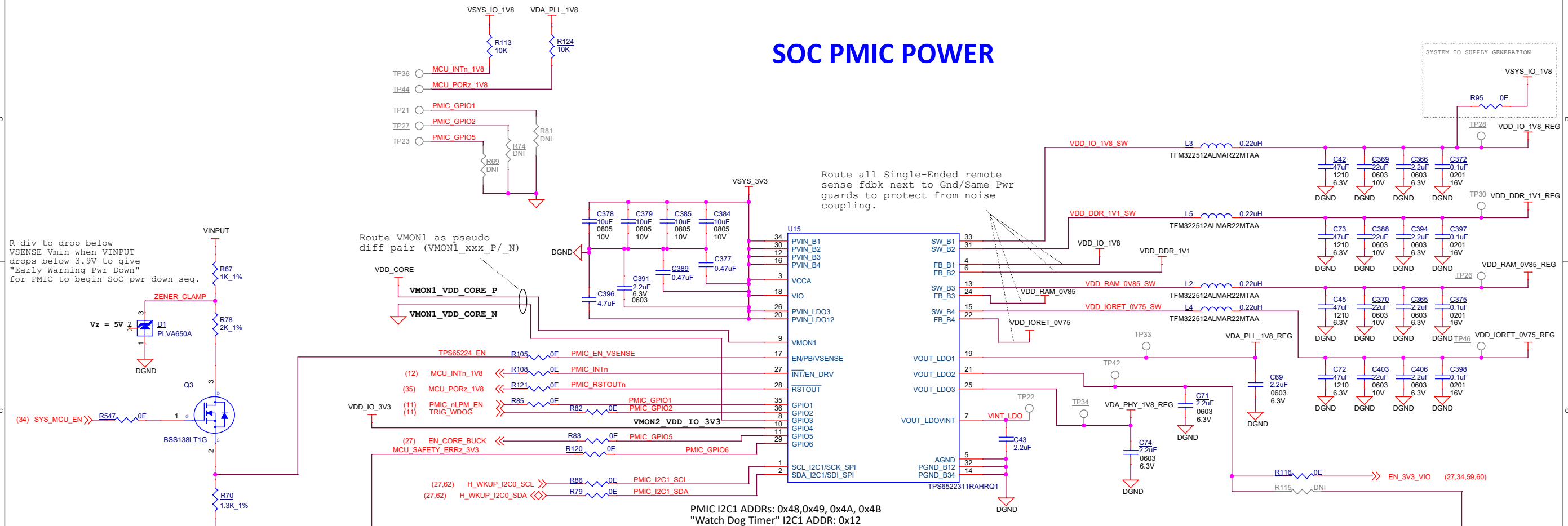


Route supply & Gnd connections from SoC Pol as a pseudo differential pair to TPs near R & C termination for easy access



Route supply & Gnd connections from SoC Pol as a pseudo differential pair to TPs near R & C termination for easy access

Route all Single-Ended remote sense fdbk next to Gnd/Same Pwr guards to protect from noise coupling.



```
R-div to drop below
VSENSE Vmin when VINPUT
drops below 3.9V to give
"Early Warning Pwr Down"
for PMIC to begin SoC pwr down seq.
```

```
Route VMON1 as pseudo
diff pair (VMON1_xxx_P/_N)
```

Route all Single-Ended remote sense fdbk next to Gnd/Same Pwr guards to protect from noise coupling.

PMIC I2C1 ADDRs: 0x48,0x49, 0x4A, 0x4B
"Watch Dog Timer" I2C1 ADDR: 0x12

PMIC GPIO_1 & GPIO_2, 2:1 R-Mux Use Cases:

- 1) Install R85 to support SoC's Partial IO Ret low power mode that needs PMIC_nLPM_EN connected to GPIO1.

Install R82 to support alternative Trigger WDog timer mode of operation.

- 2) Install both R241 & 250 to use 2x independent I2C channels for PMIC settings & status and WDog timer in long window mode.

TI EVM default board & BOM supports Use Case #1

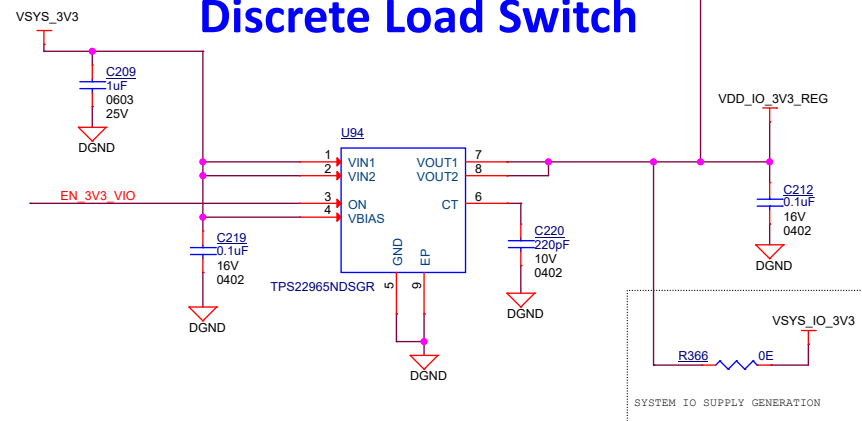
Note:
Previous J7xxx PDNs used a 2nd, indep I2C Ch (MCU I2C0_SCL/SDA) for WDOG operations.
Burton PMiC has limited GPIOs, so 1x I2C Ch will be timed multiplexed (PMiC control/settings & WDOG ops) in order to support low pwr modes.

PMIC LDO2, 2:1 R-Mux Use Cases:

- 1) Install R116 to use LDO2 Vout as "EN_3V3_VIO" control signal on a discrete load switch to supply VDD_IO_3V3 loads > 165mA, SoC & all board peripheral components.

2) Install R115 to use LDO2 in FET Bypass/Load Switch mode to supply VDD_IO_3V3 loads < 165mA, SoC & all board peripheral components.

TI EVM default board & BOM is use case i#1.

[illegible]

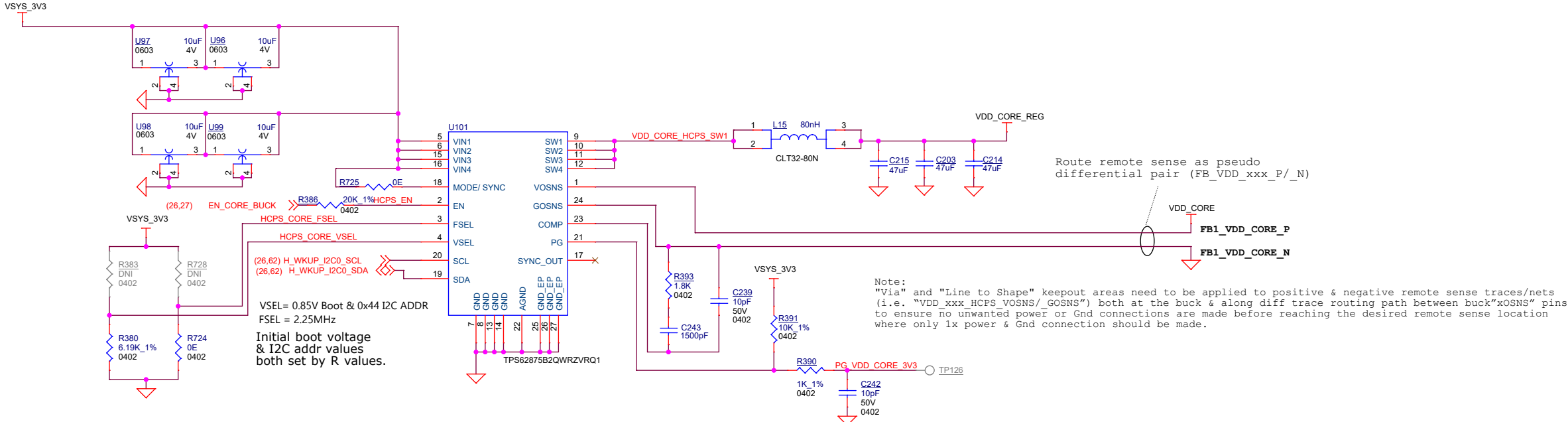
PMIC's GPIO6 supports 2x PDN functions:

- A) DISABLE WDOG: PMIC reads logic level at GPIO6 pin at beginning of PMIC start-up sequence before NVM initialization.
 - a) High level at GPIO6 pin (SW-1/Jmpr-1 = closed) directs PMIC to disable Watch-Dog Timer (by setting WD_PWRHOLD bit to disable timer's long-window time-out).
 - b) Low level at GPIO6 pin (SW-1/Jmpr-1 = open due to PMIC default internal pull-down R) enables Watch-Dog Timer (default setting enables timer's long-window time-out).

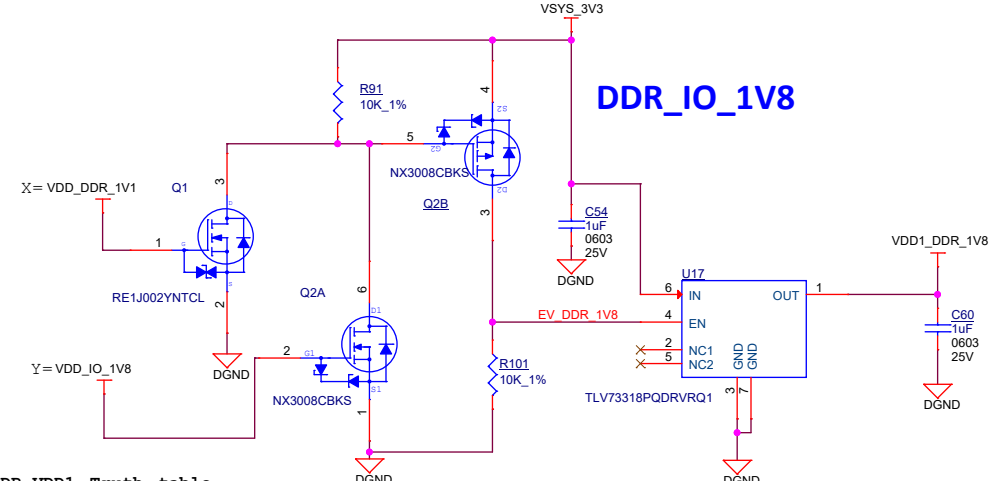
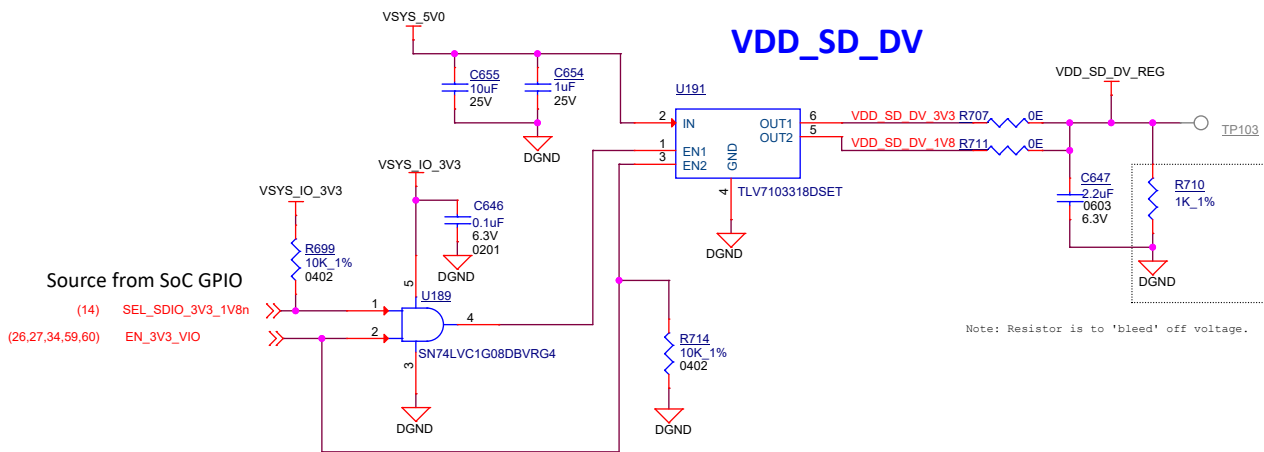
B) MCU_SAFETY_ERROR: After PMIC NVM initialization, GPIO6 function is set to Error Signal Monitor (ESM) function.

SWITCH (SW2 - 5)	Description
CLOSED	Disables WDog, high latched at Pwr-Up
OPEN (Default)	Enables WDog, low latched at Pwr-Up

VDD_CORE High-Current Power Stage (HCPS)



LDOs

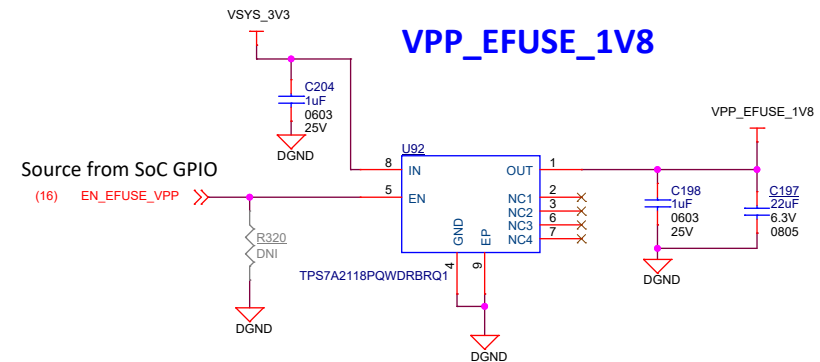
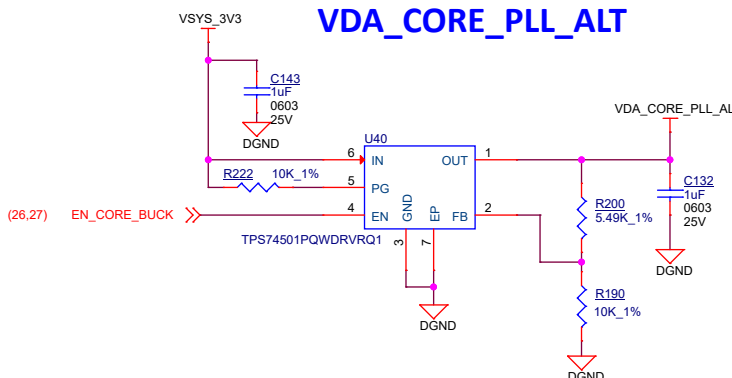
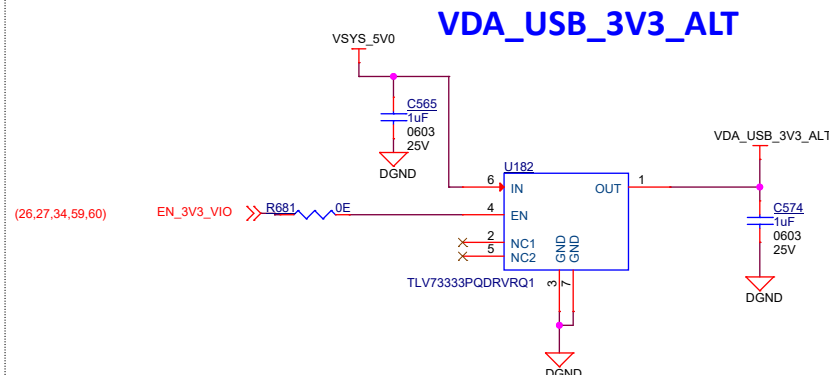


EN_DDR_VDD1 Truth table

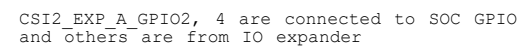
Dscrt "OR" Gate Logic		EN_DDR_iv8
X	Y	OUTPUT
0	0	0
0	1	1
1	0	1
1	1	1

Notes:

- 1) EVM option to supply VDA_3P3_USB from an alternative low noise LDO.
- 2) EVM option to supply VDDA xxx low voltage analog supplies from an alternative low noise LDO.



CSI2 EXPANSION CONNECTORS

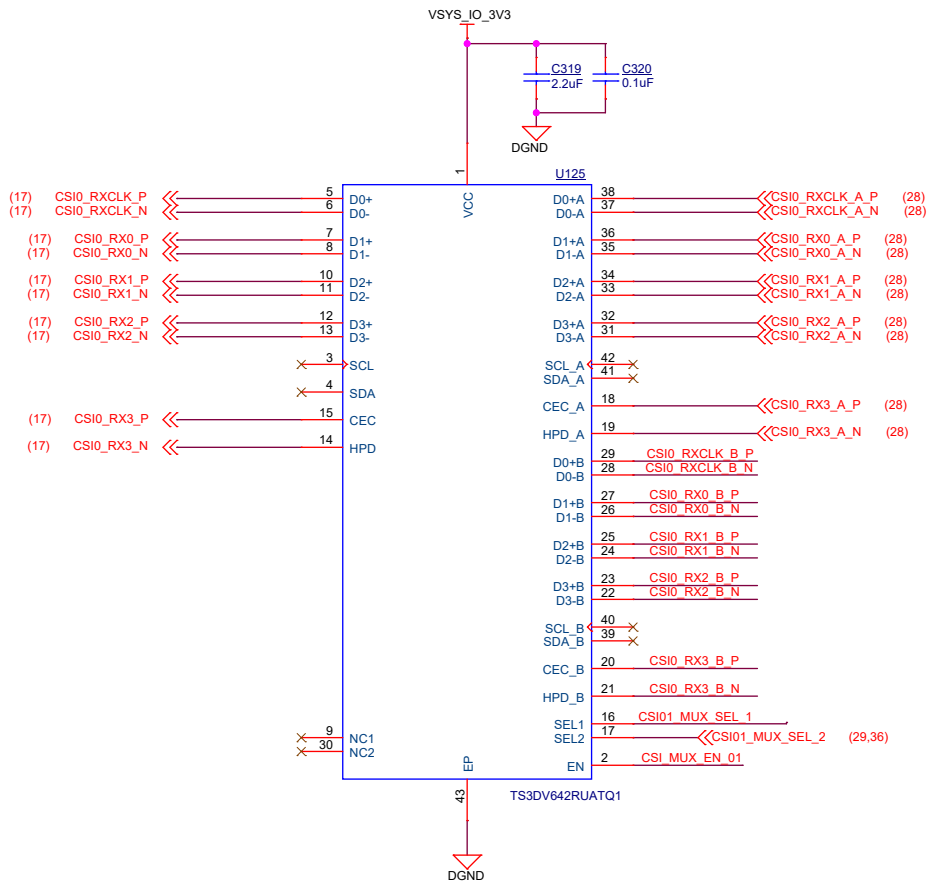


J7 EVM



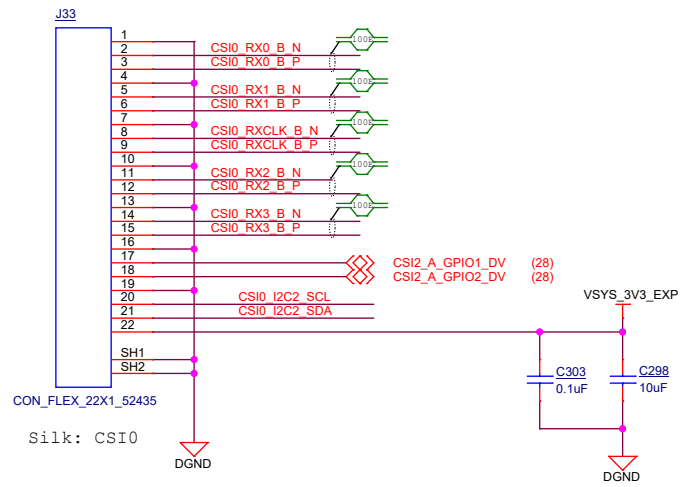
Title	CSI2 EXPANSION CONNECTORS
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Size	PROC170 002 J722S	R
C		E
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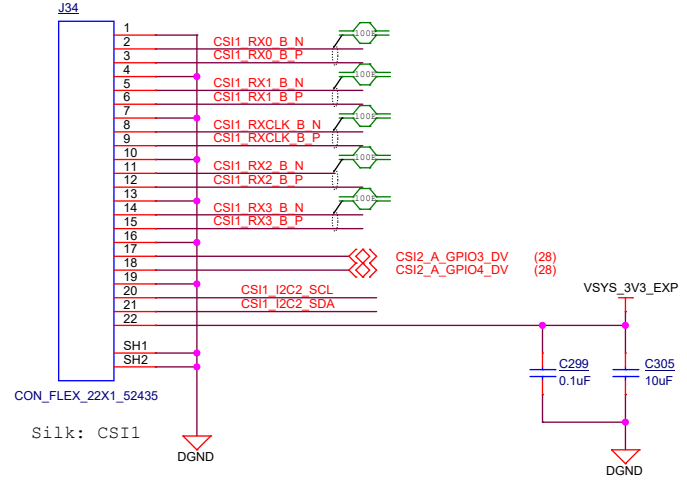


From CSI EXP Conn

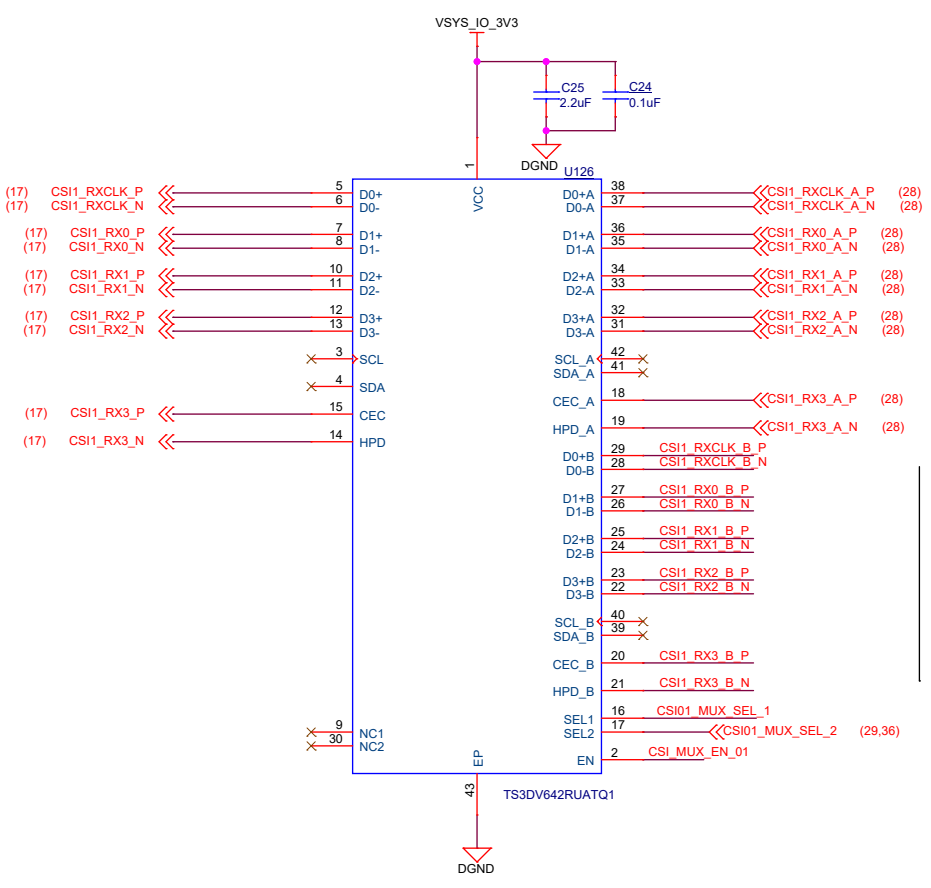
From FPC Camera Conn



Silk: CSI0



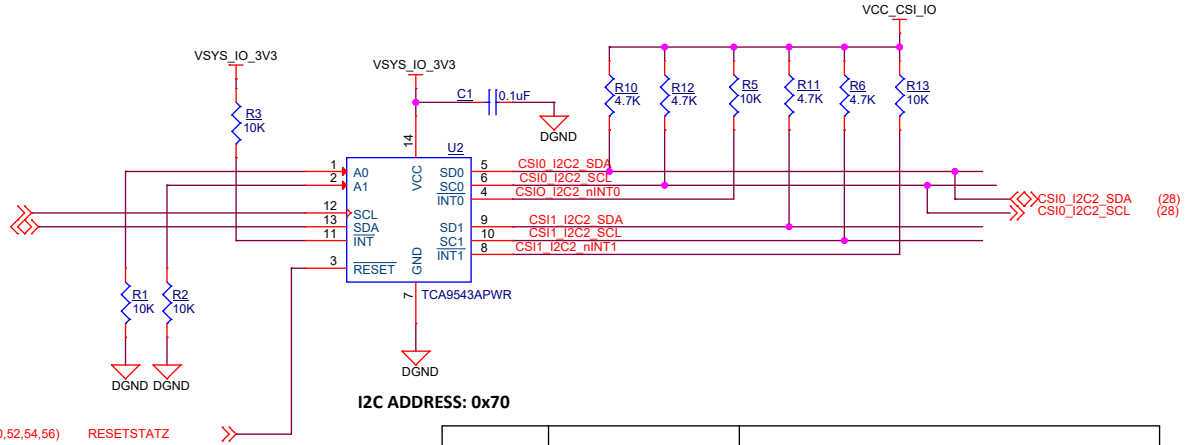
Silk: CSI1



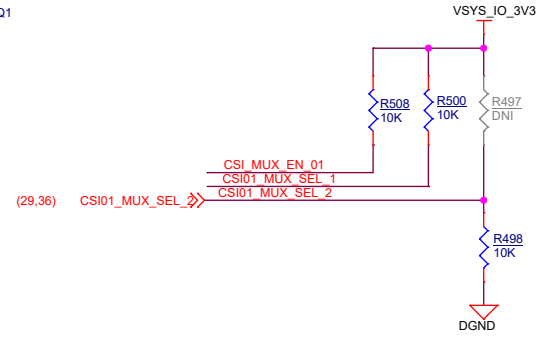
From CSI EXP Conn

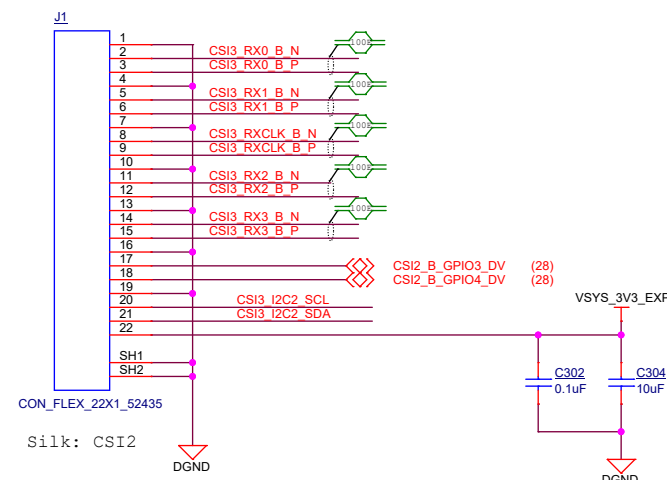
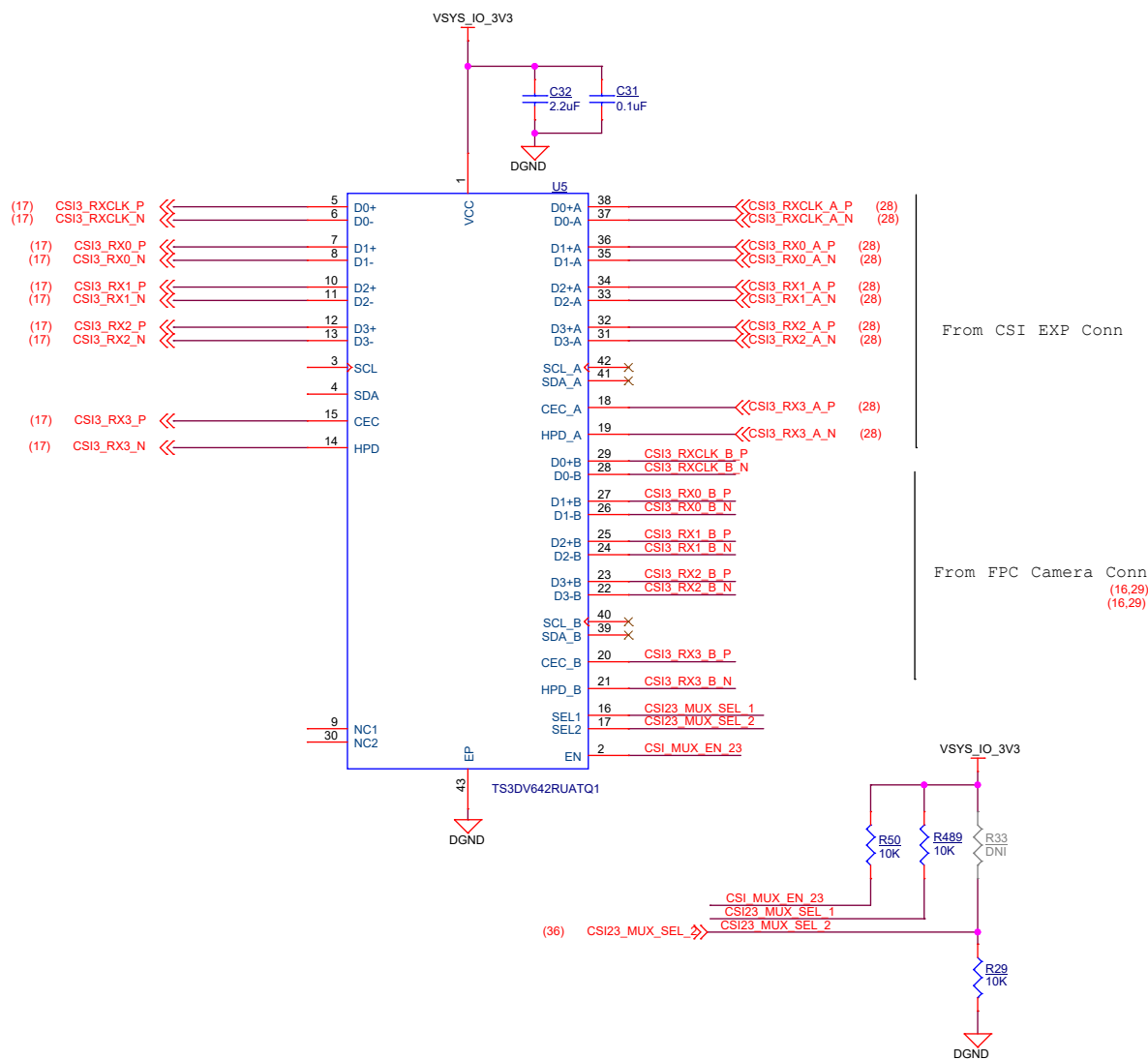
From FPC Camera Conn

I2C SWITCH FOR SoC_I2C2



EN	CSI01_MUX_SEL_2	FUNCTION	
HIGH	LOW	INPUT<-- A Port [CSI2 Connector]	(default)
HIGH	HIGH	INPUT<--B port [FPC Camera Connector]	
LOW	X	Disconnect	



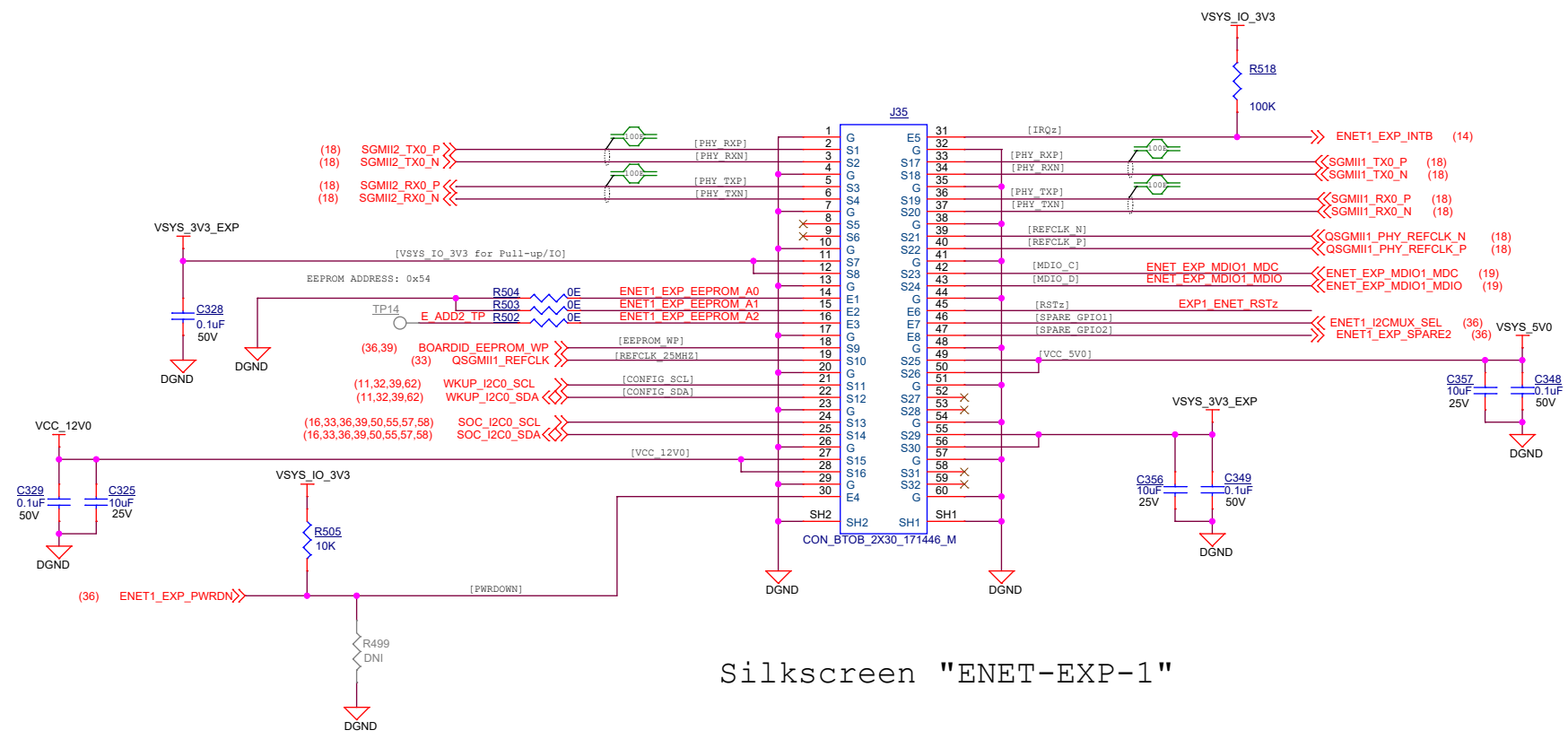


I2C ADDRESS: 0x71

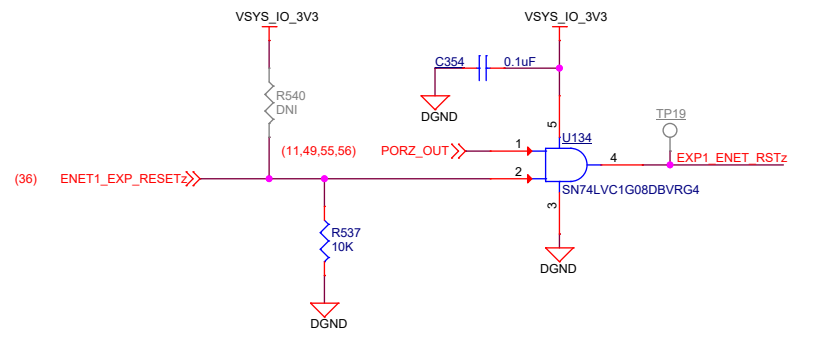
EN	CSI23_MUX_SEL_2	FUNCTION

EN	CSI23_MUX_SEL_2	FUNCTION	
HIGH	LOW	INPUT<-- A Port [CSI2 Connector]	(default)
HIGH	HIGH	INPUT<--B port [FPC Camera Connector]	
LOW	X	Disconnect	

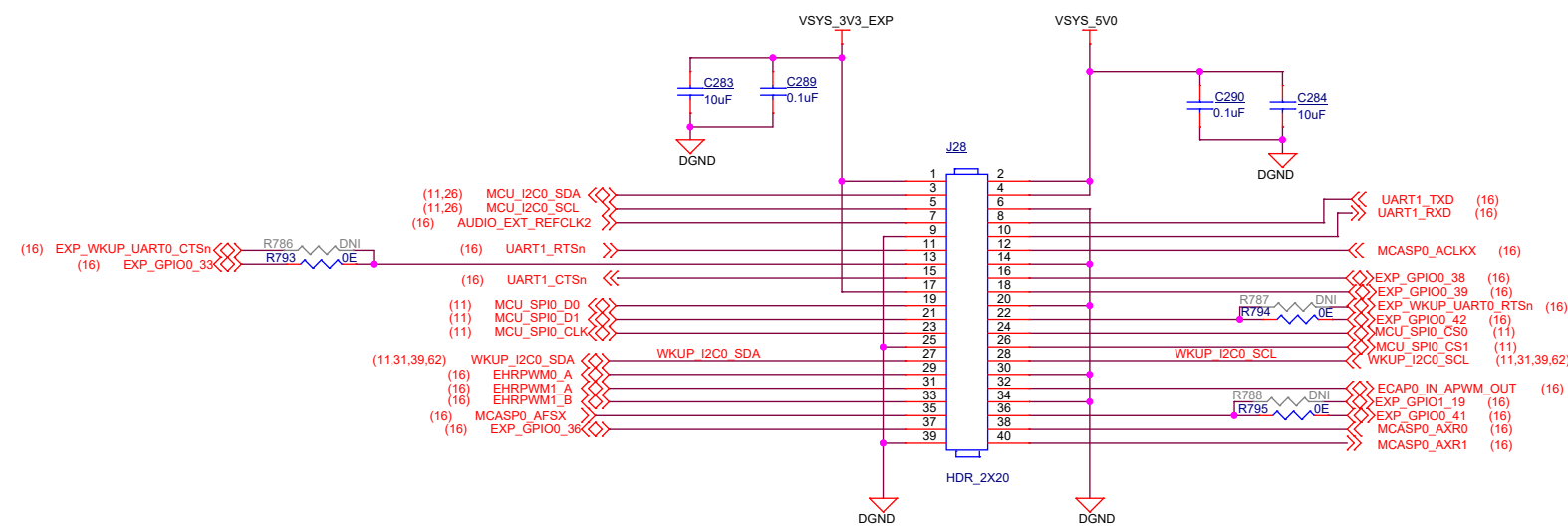
ENET EXPANSION CONNECTOR



Silkscreen "ENET-EXP-1"

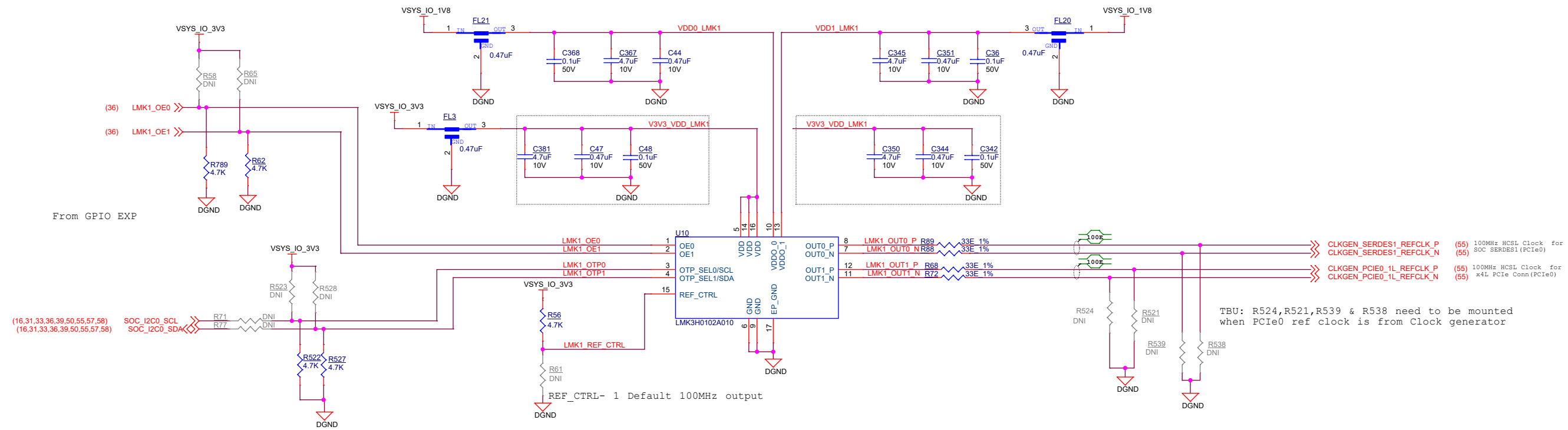


USER EXPANSION CONNECTOR

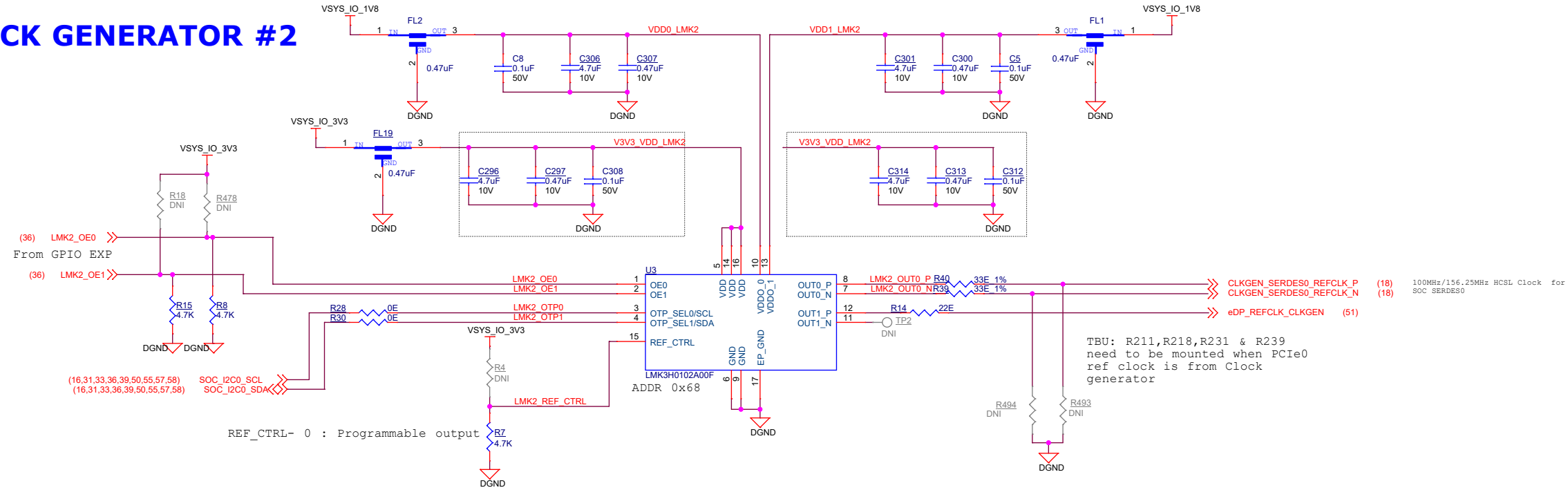


Silk Screen "40p EXP HDR"

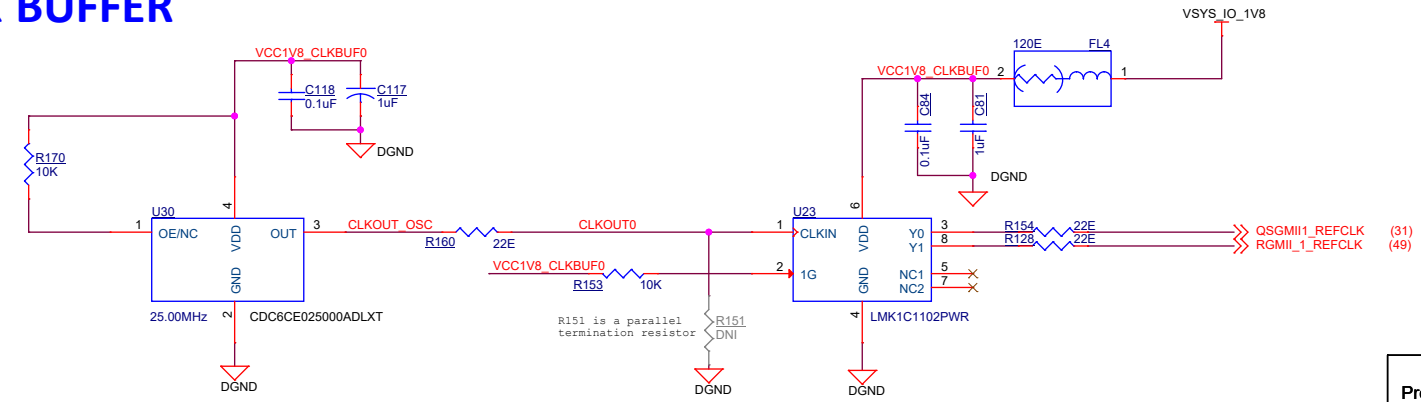
SERDES CLOCK GENERATOR #1



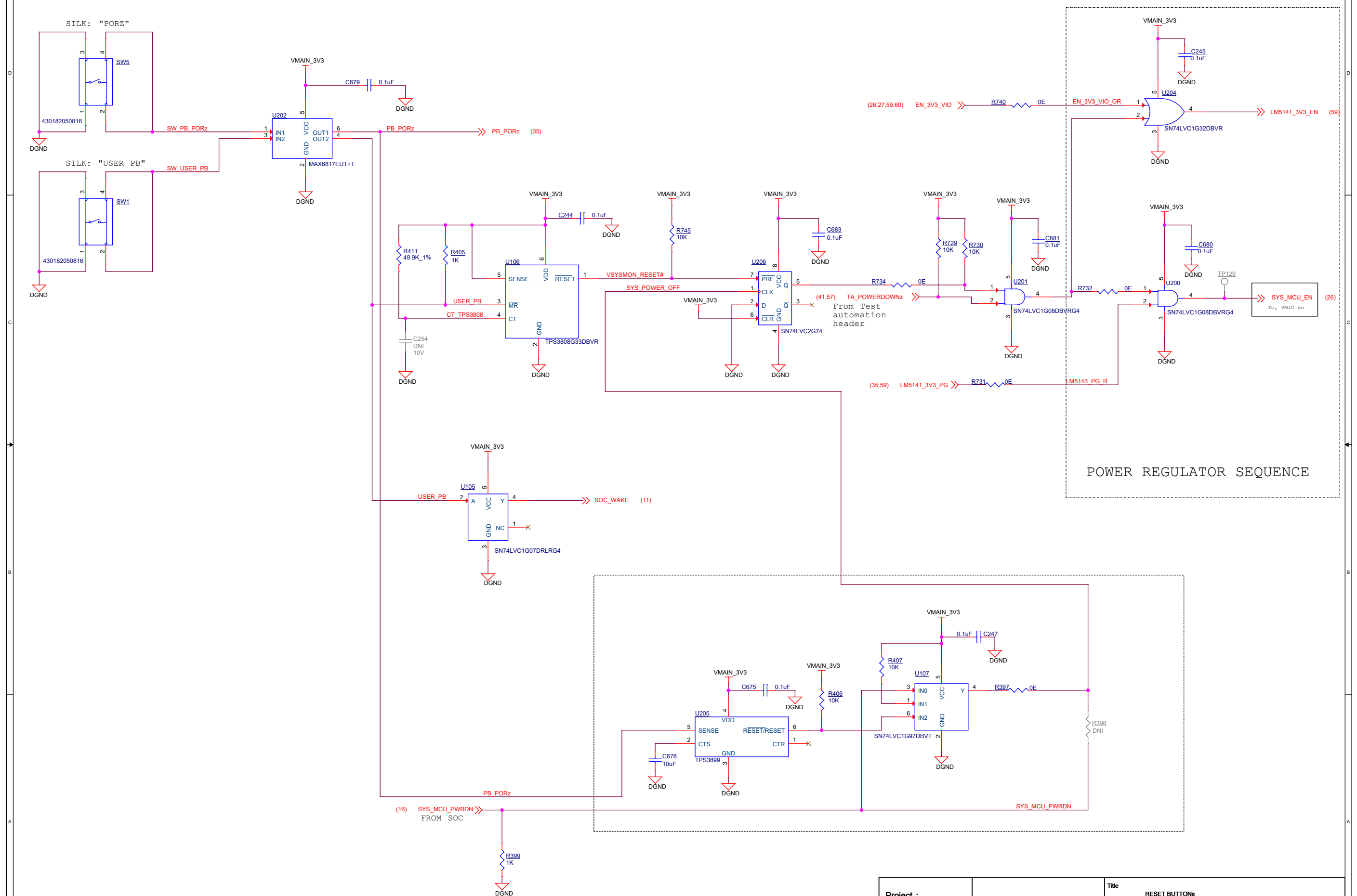
SERDES CLOCK GENERATOR #2



PERIPHERAL CLOCK BUFFER



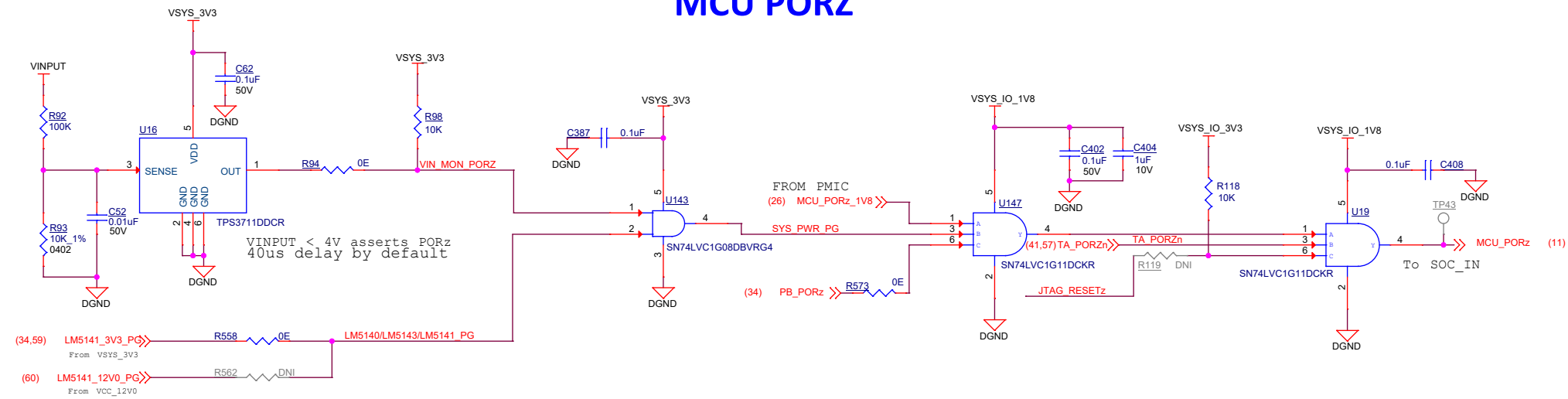
RESET BUTTONs



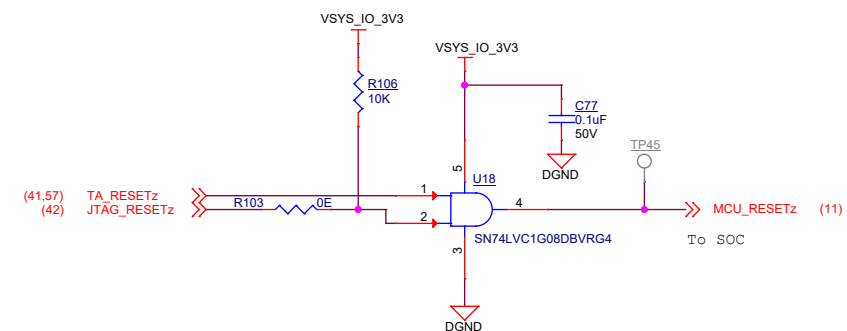
RESET INPUTS

Under Voltage Monitor (VINPUT)

MCU PORZ



MCU_RESET



Project : J7 EVM

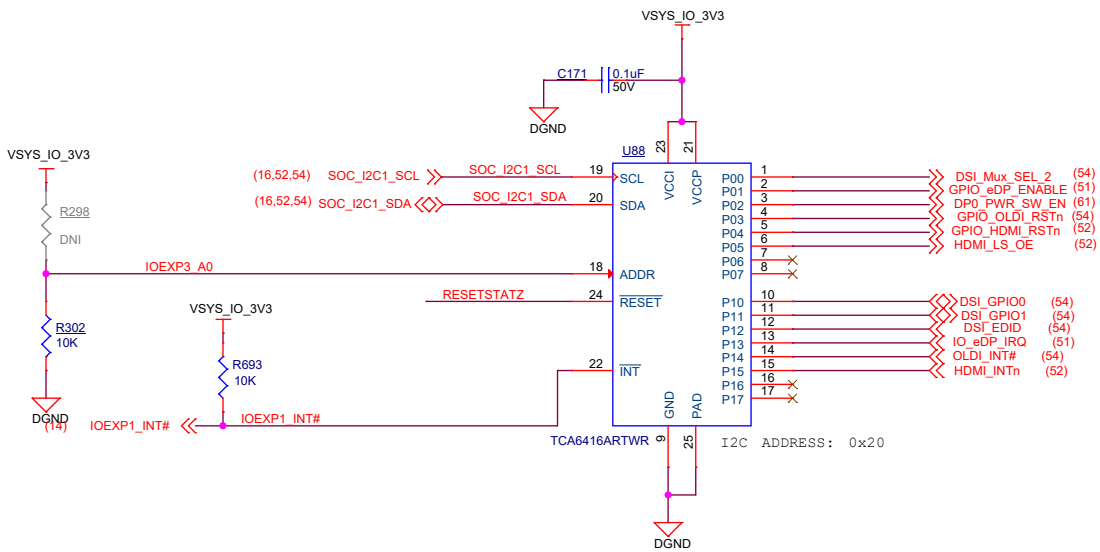
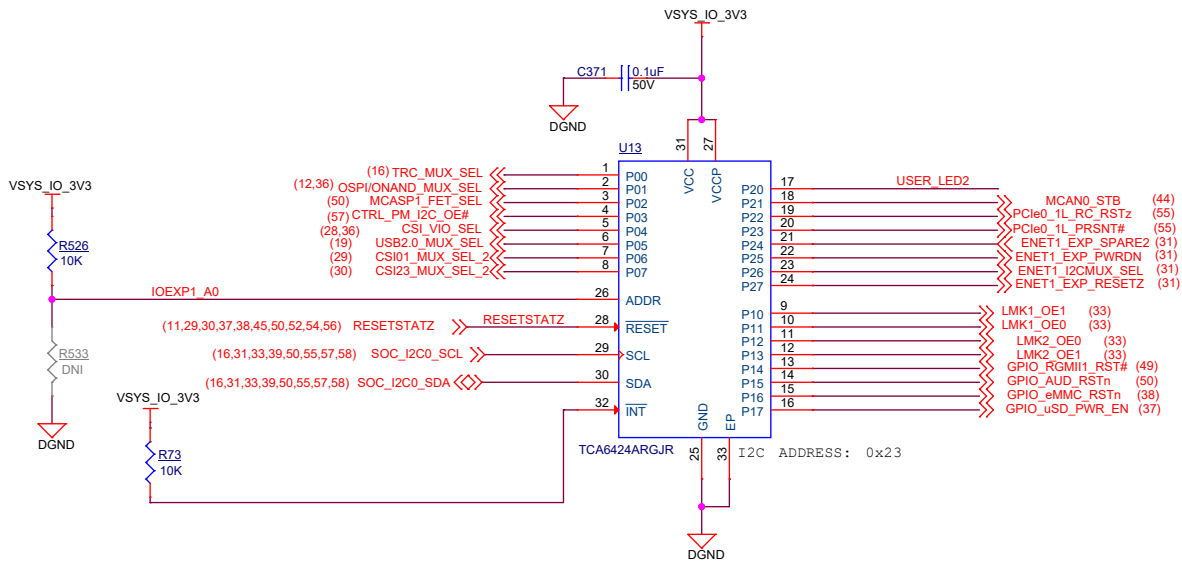


Title	RESET INPUTS
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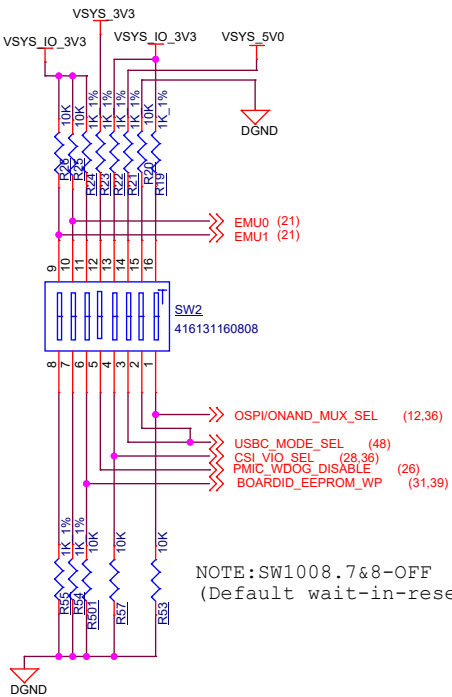
GPIO EXPANDERS

I2C GPIO EXPANDER1

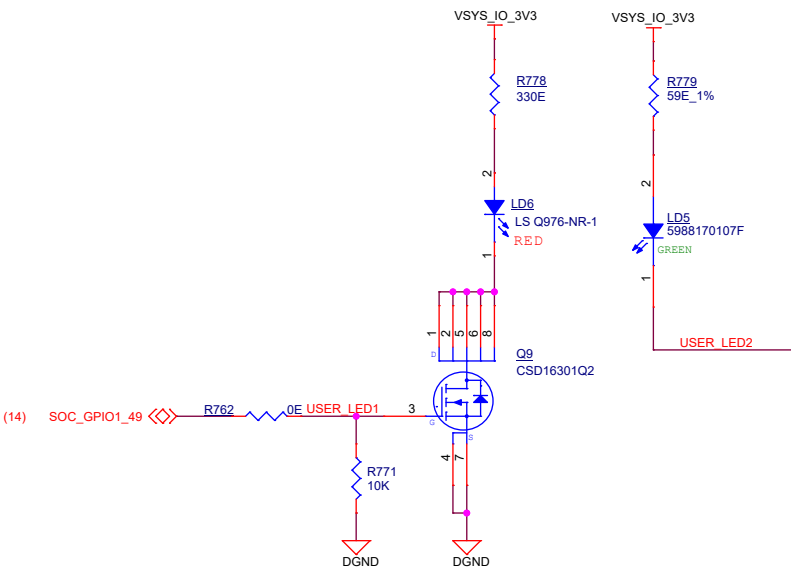


SWITCH (SW1008.4)	Description
CLOSED	Disables WDog, high latched at Pwr-Up
OPEN (Default)	Enables WDog, low latched at Pwr-Up

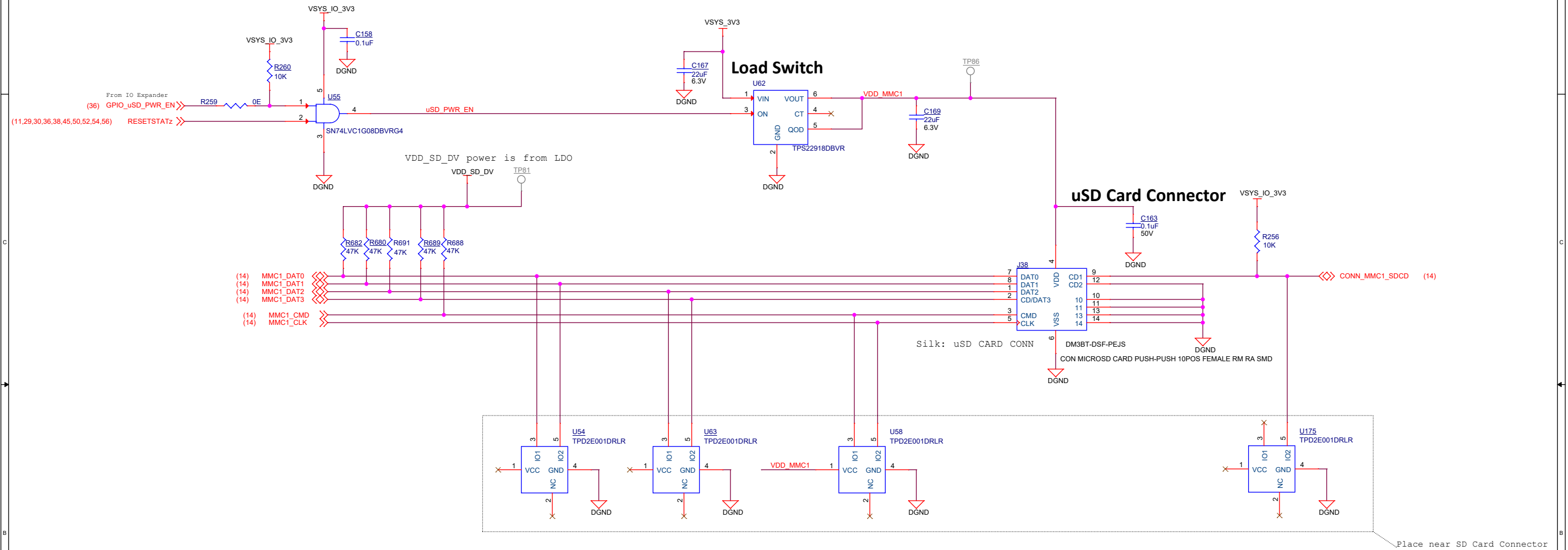
CONFIG DIP SWITCH



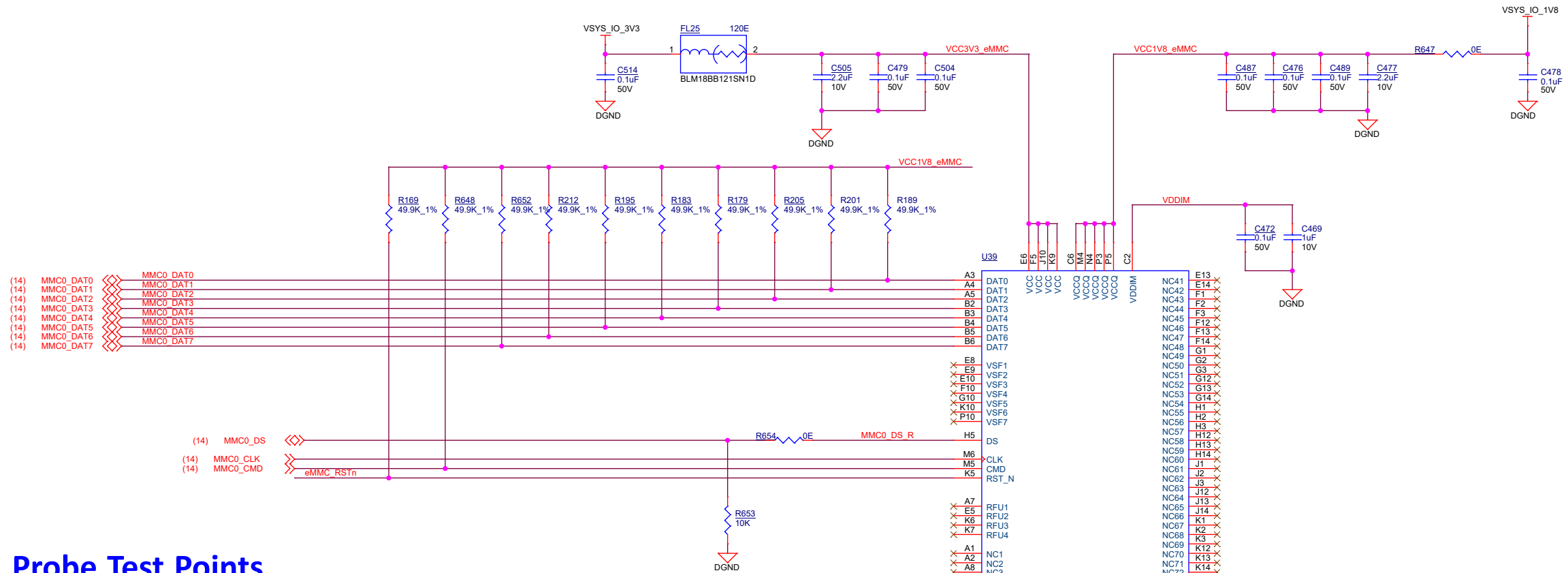
NOTE: SW1008.7&8-OFF
(Default wait-in-reset disabled)



Micro SD CARD INTERFACE



eMMC FLASH

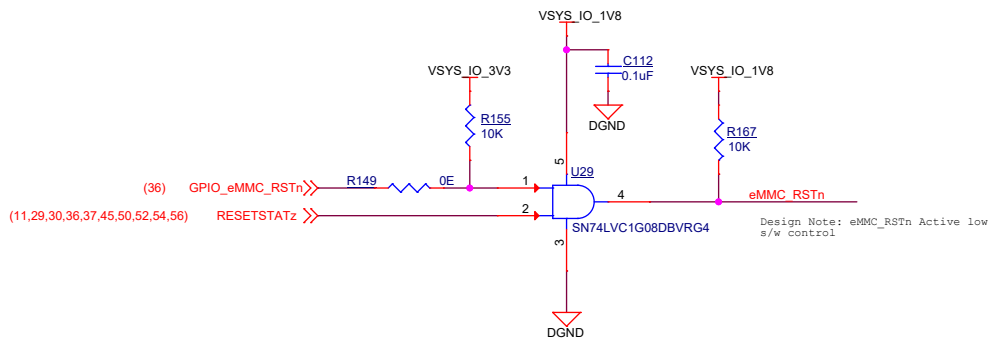


Via Probe Test Points

Place Near eMMC side

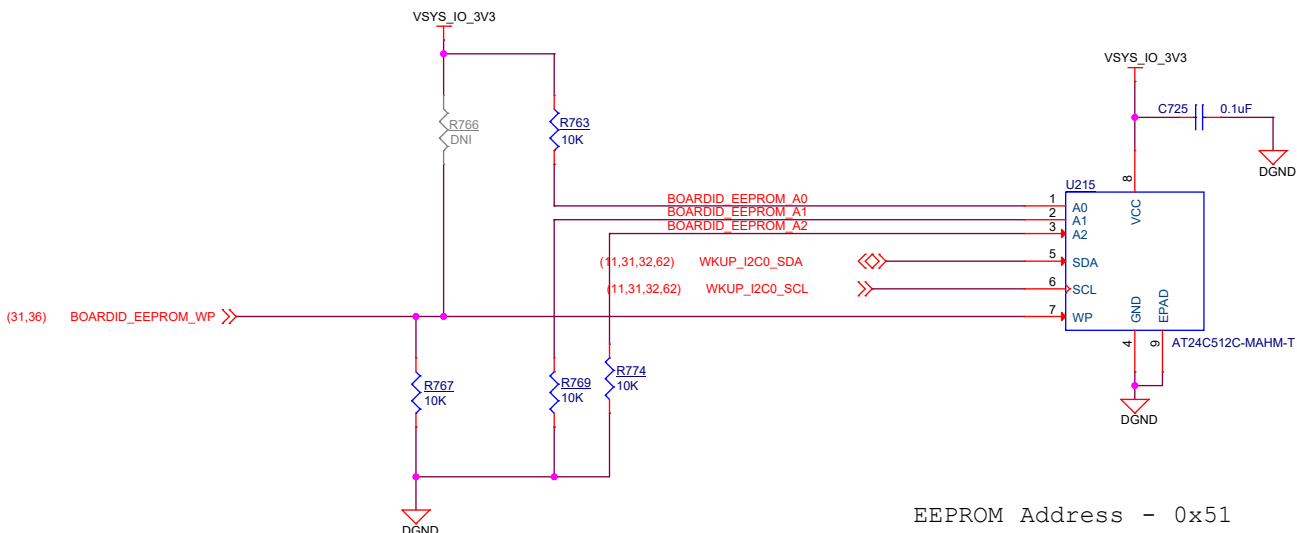
TP63	DNI	MMC0_DAT0
TP67	DNI	MMC0_DAT1
TP69	DNI	MMC0_DAT2
TP59	DNI	MMC0_DAT3
TP61	DNI	MMC0_DAT4
TP65	DNI	MMC0_DAT5
TP70	DNI	MMC0_DAT6
TP161	DNI	MMC0_DAT7
TP159	DNI	MMC0_DS_R
TP56	DNI	MMC0_CLK
TP160	DNI	MMC0_CMD

eMMC FLASH RESET

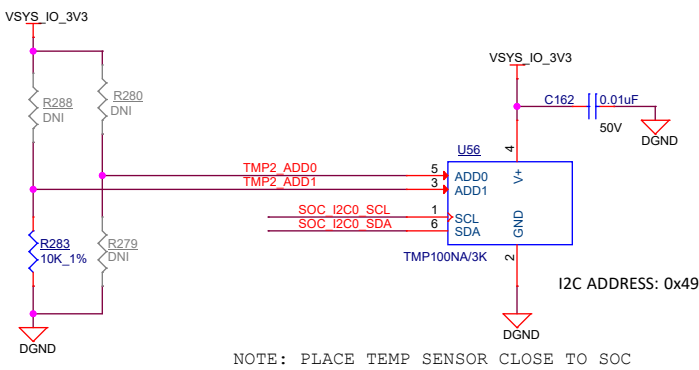
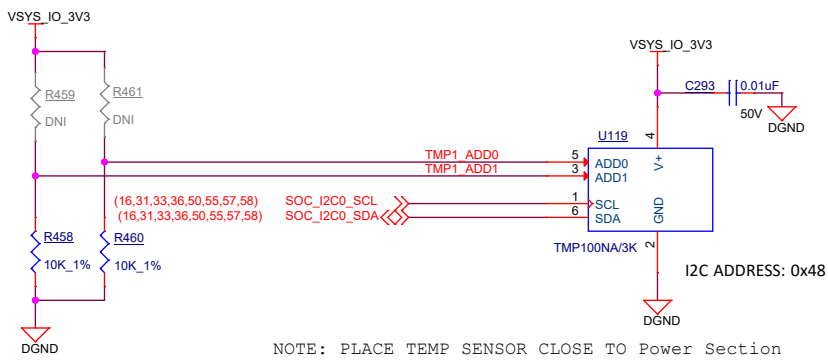


I2C for BOARD ID EEPROMs

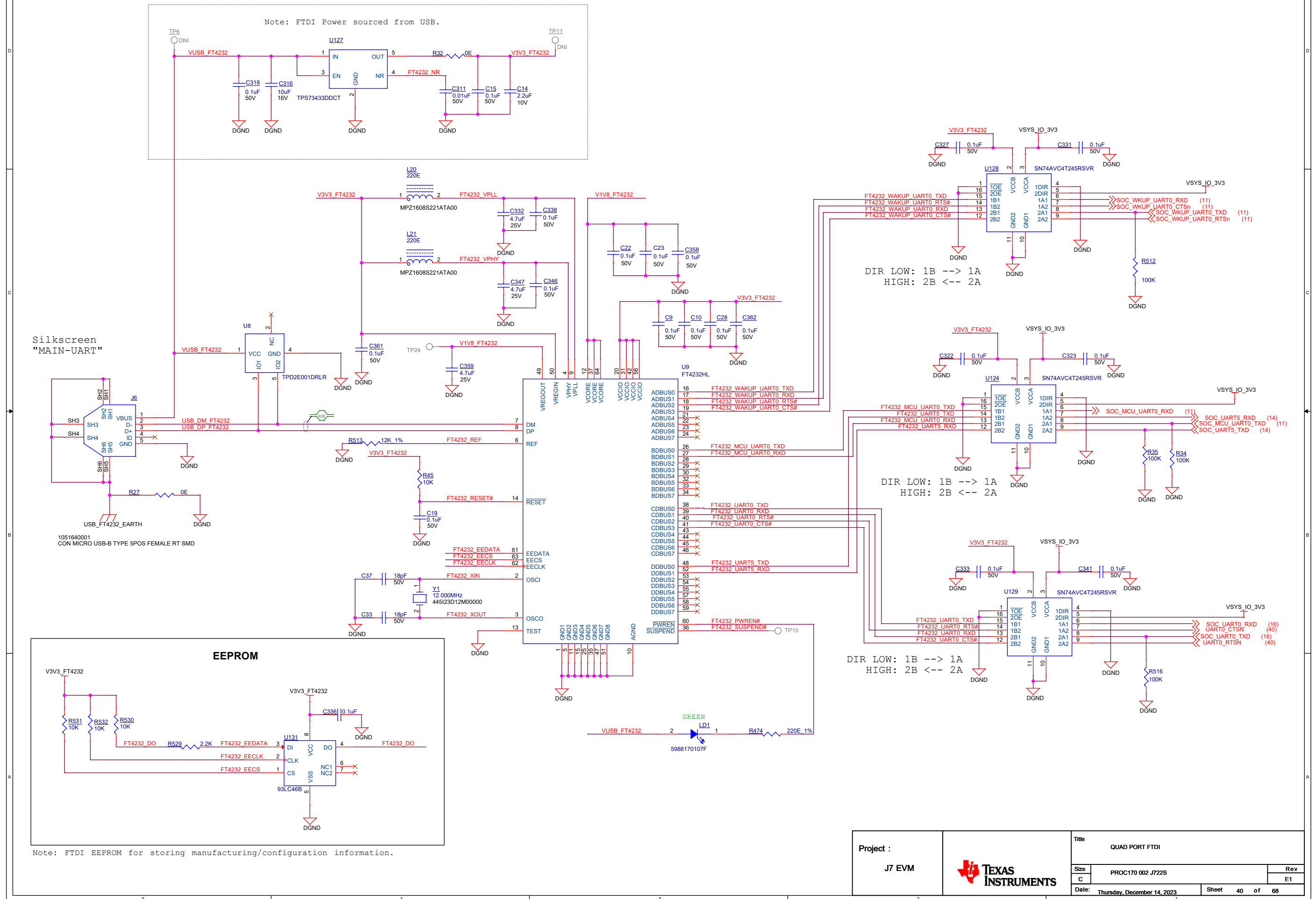
BOARD ID EEPROM



TEMPERATURE SENSORS
(TI EVM Only)



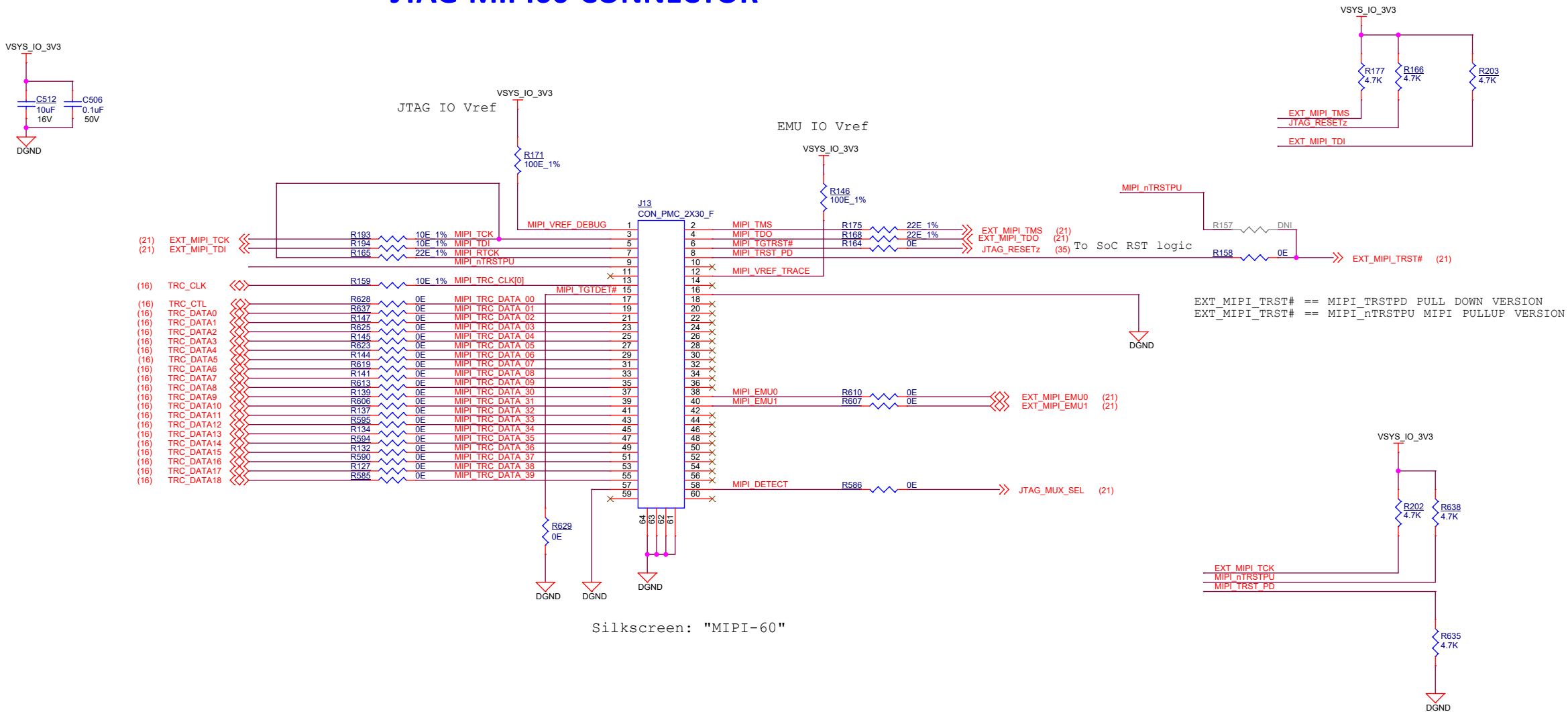
QUAD PORT FTDI



XDS110 DEBUGGER

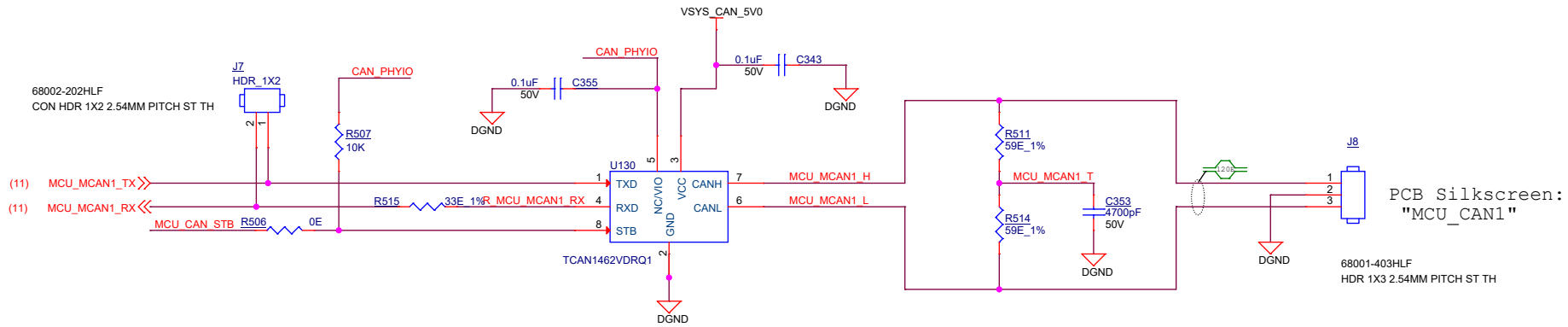
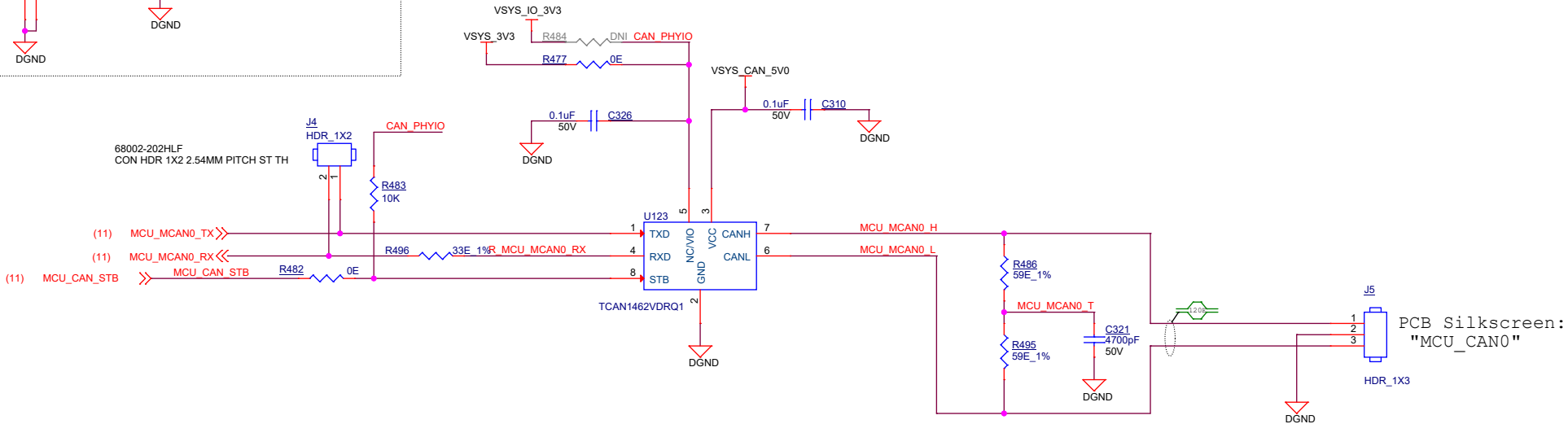
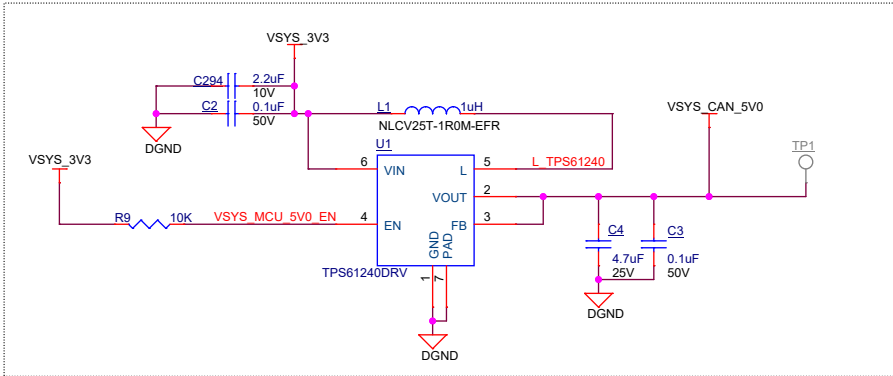


JTAG MIPI60 CONNECTOR

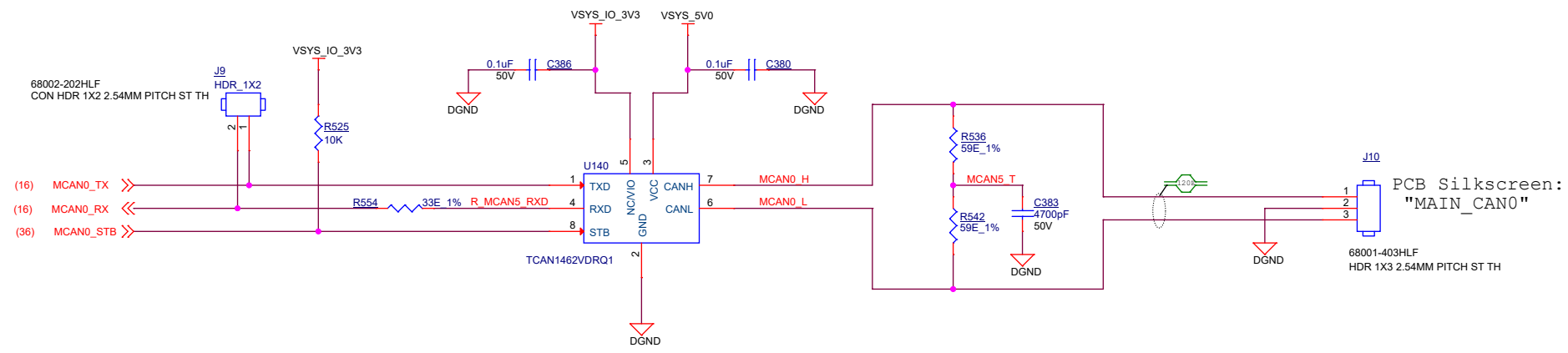


Silkscreen: "MIPI-60"

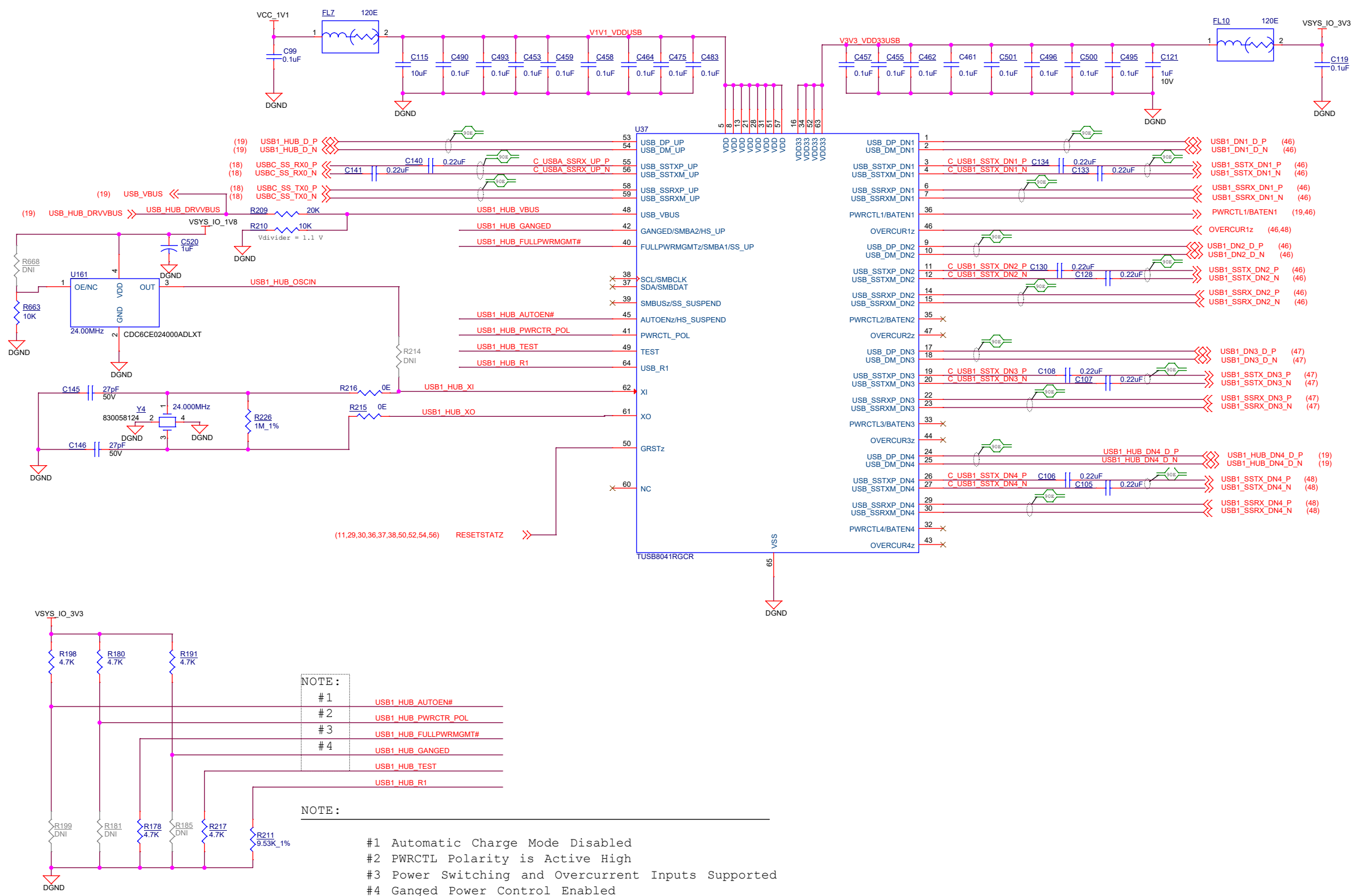
CAN TRANSCEIVERS #1-MCU DOMAIN



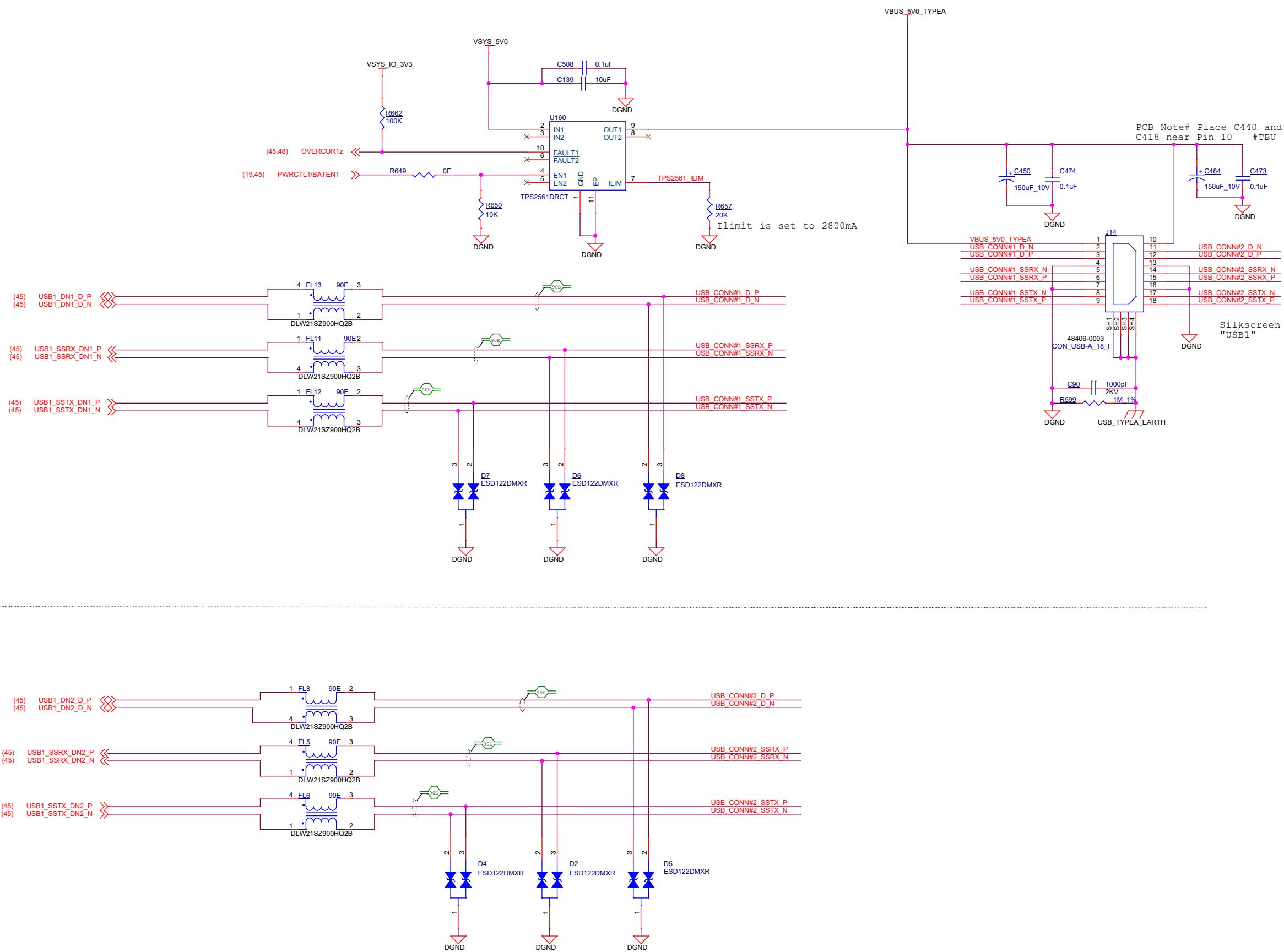
CAN TRANSCEIVERS #2-MAIN DOMAIN



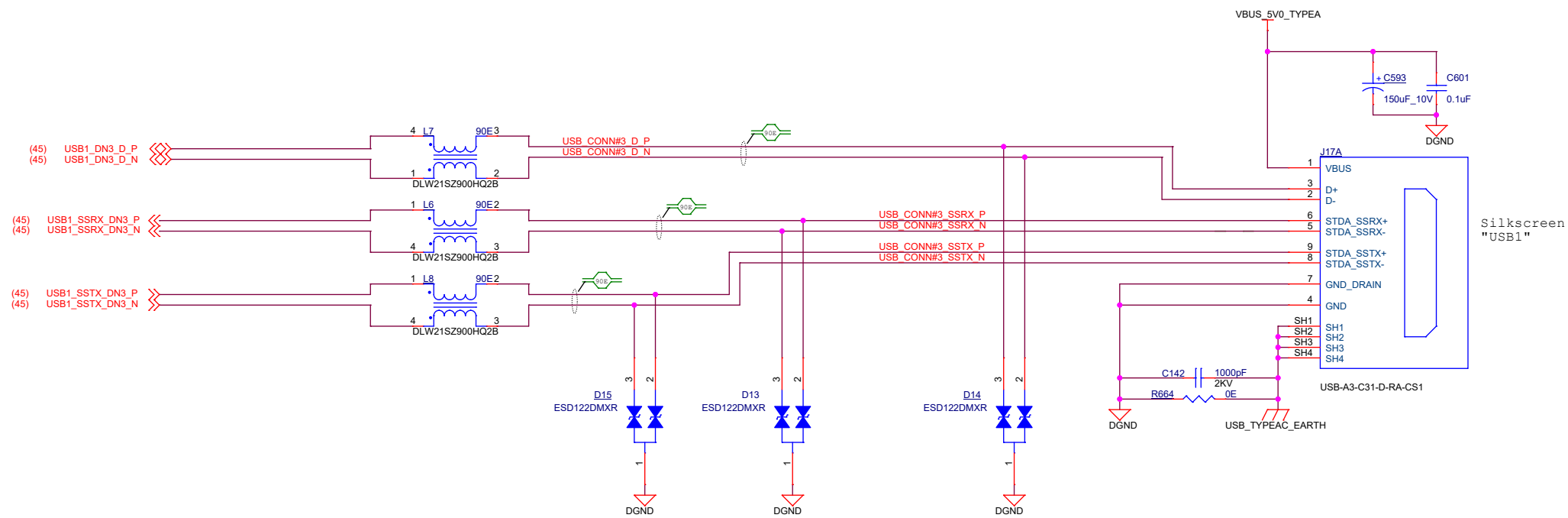
USB3.0 HUB



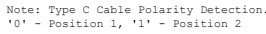
USB 3.0 TYPE-A CONNECTORS - 1



USB 3.0 TYPE-A CONNECTORS - 2

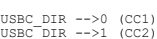


USB 3.0 TYPE C INTERFACE

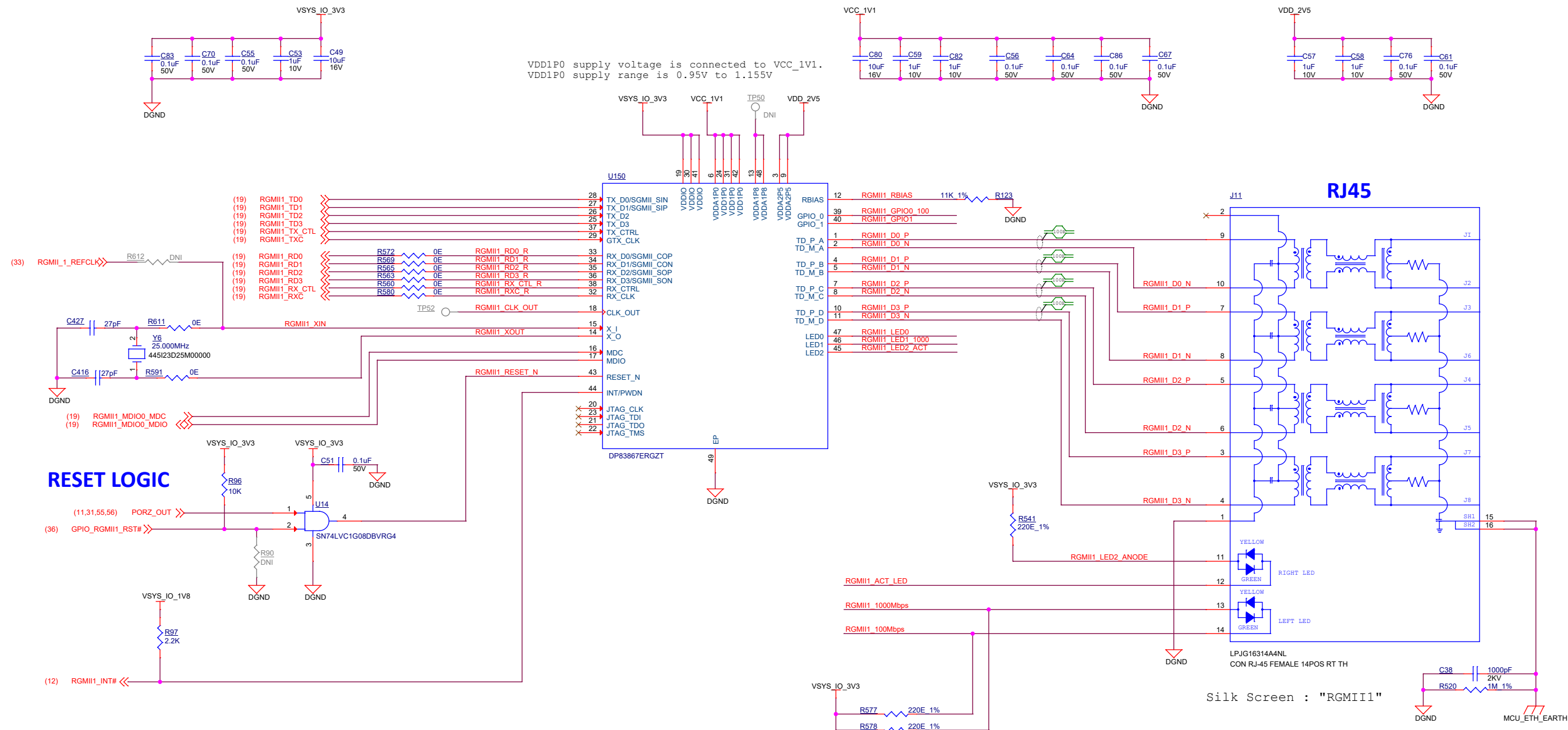


USBC_PORT_SEL1	USBC_PORT_SEL0	Selected USB C Mode
LOW	LOW	DFF
X	HIGH	UFP

USB Type C Current Limit

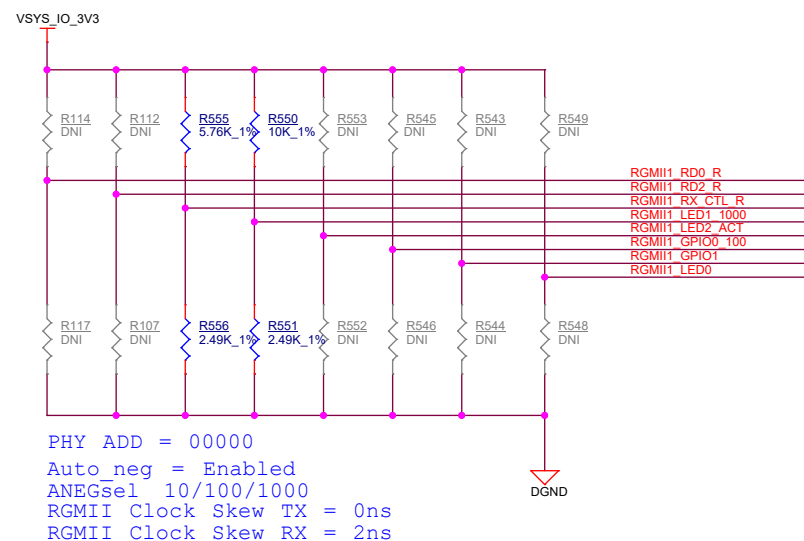


RGMII1

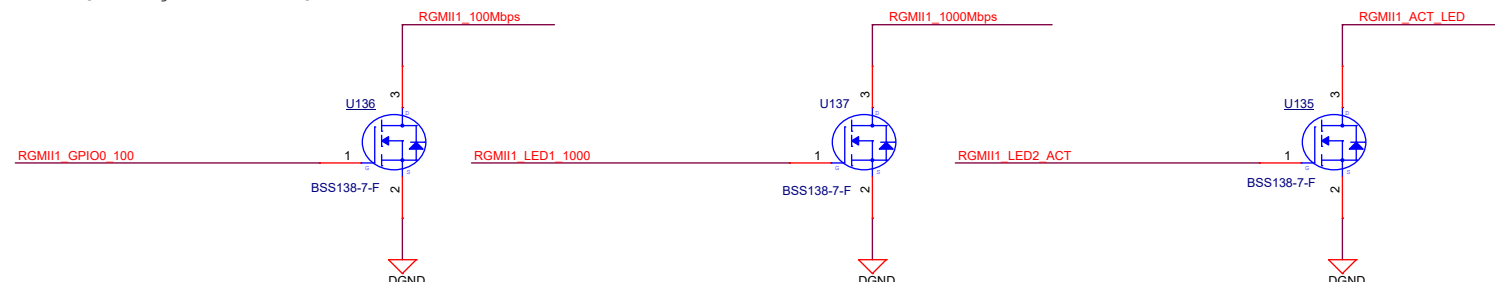


RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

SPEED AND ACTIVITY LED DRIVERS



```
Set Mode 3 [Autoneg Disable - 0]
```



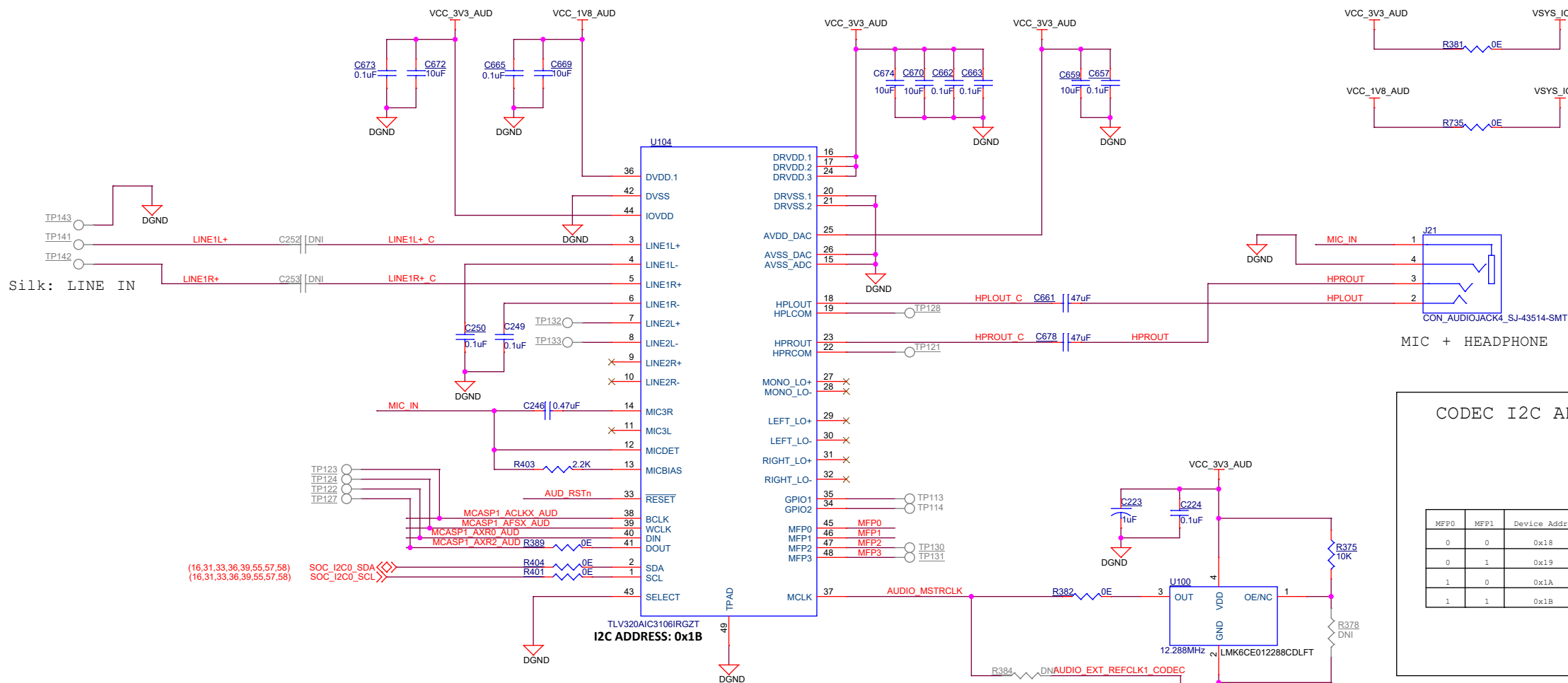
```
LED_2-MODE1    & LED_1-MODE2-TX  SKEW=0nS
GPIO0-MODE1    & GPIO1-MODE1-RX  SKEW=2nS
```

Project : J7 EVM



Title			
RGMII1			
Size	PROC170 002 J722S		Rev
C			E1
Date:	Thursday, December 14, 2023	Sheet	49 of 68

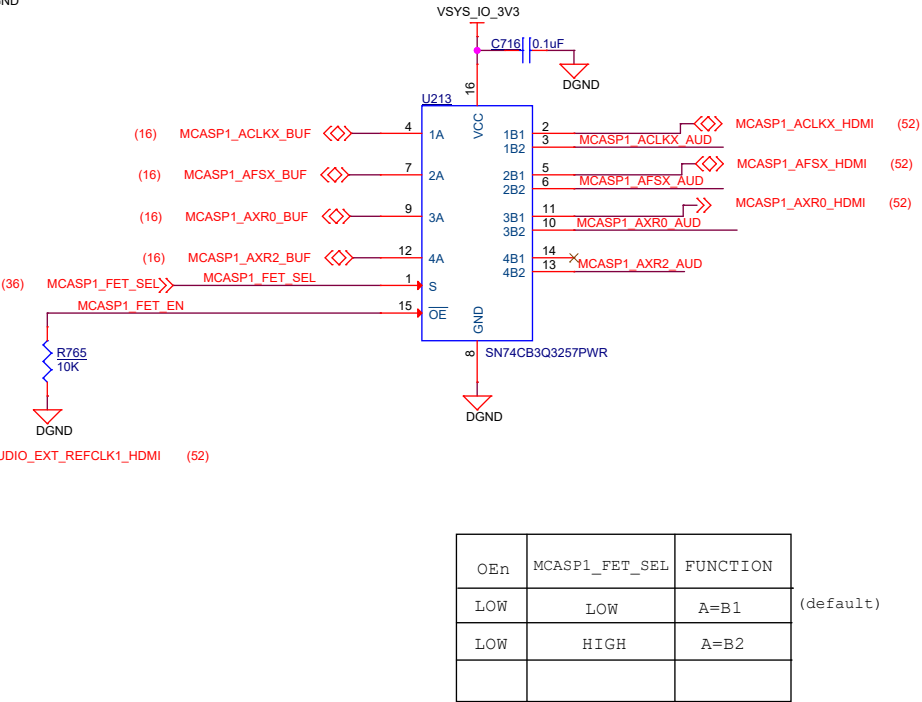
AUDIO CODEC



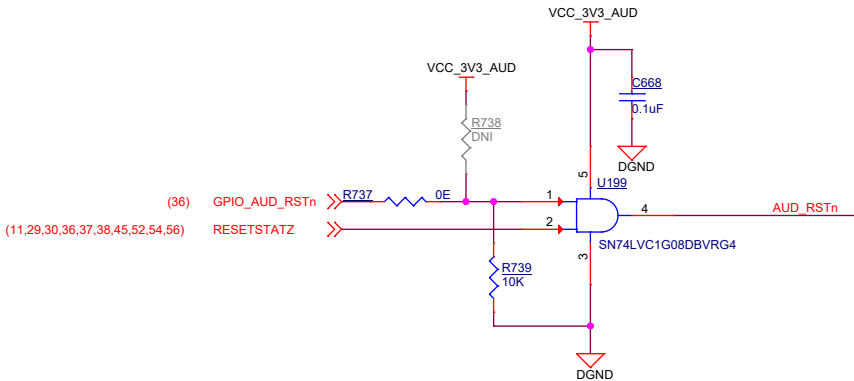
CODEC I2C ADDRESS SELECTION

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B

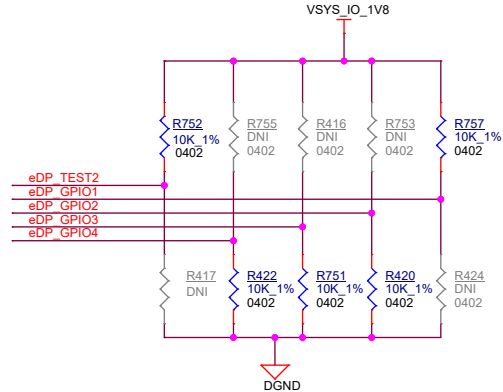
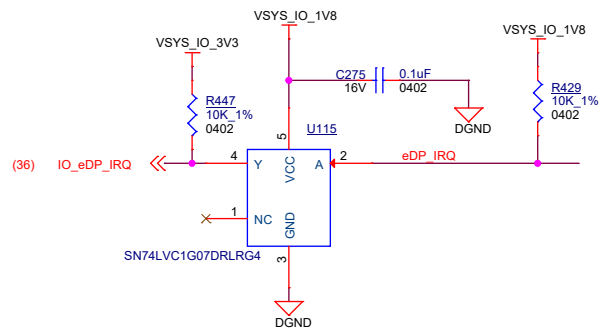
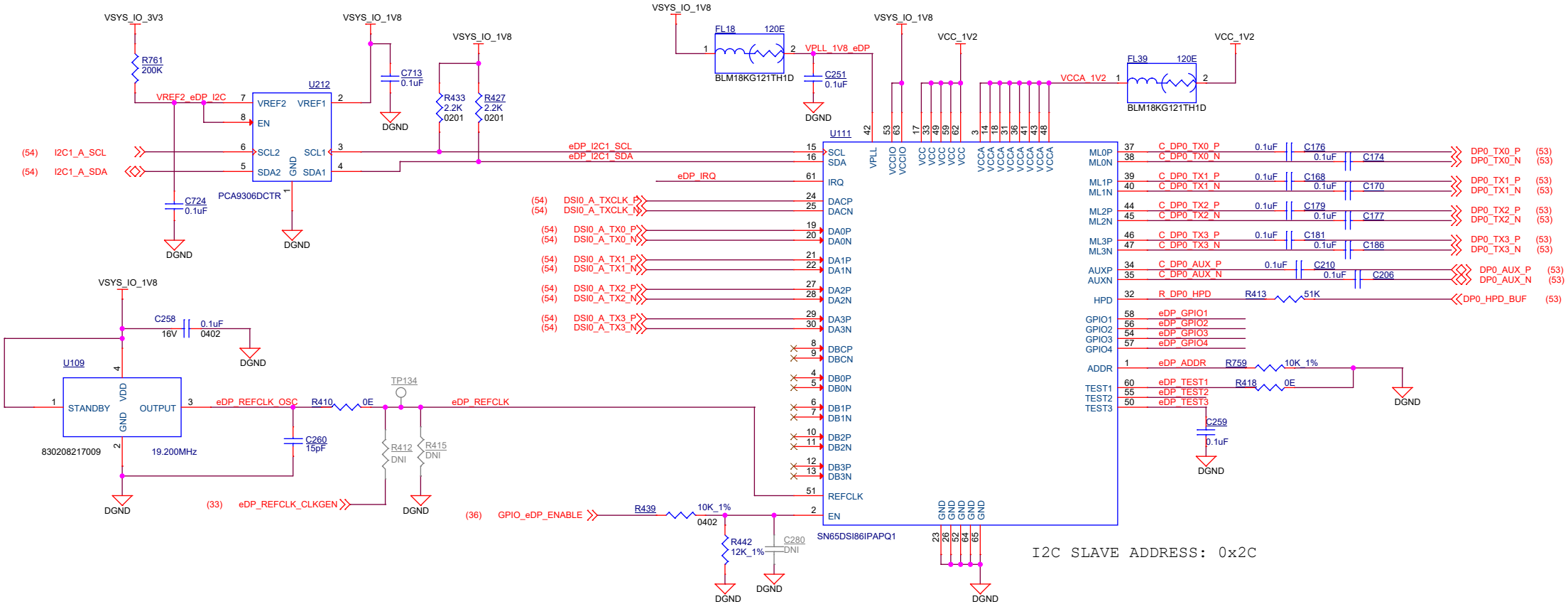
McASP1 FET SWITCH



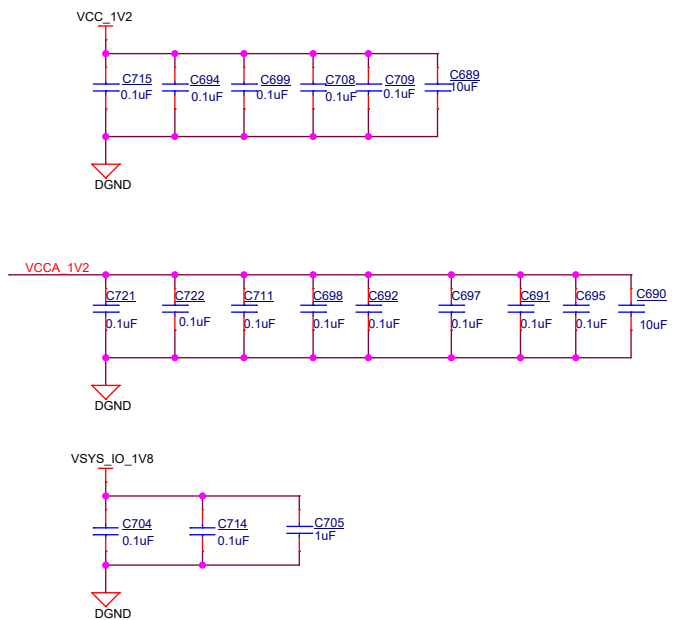
AUDIO CODEC RESET



DSI to eDP Bridge

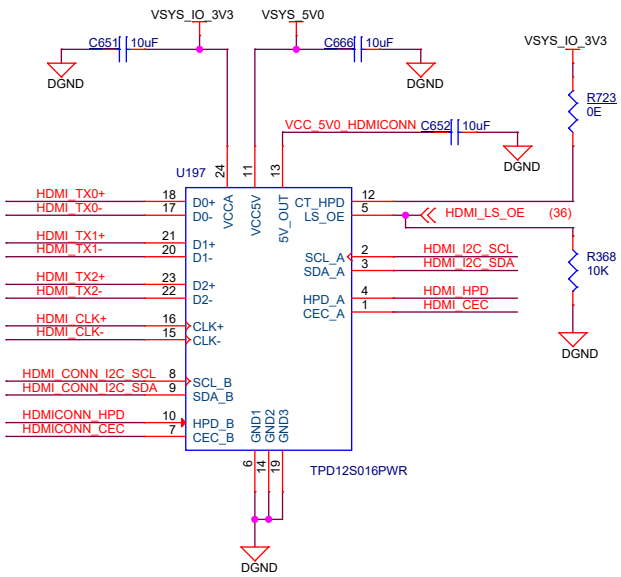


GPIO[3:1] is set as 3'b001 for 19.2MHz External Refclk

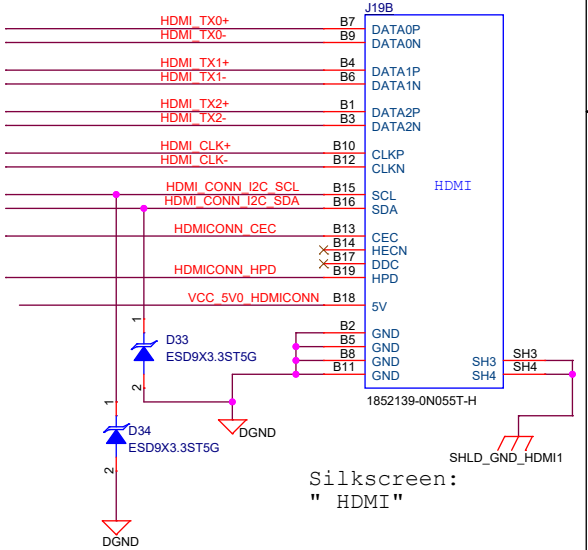


HDMI INTERFACE

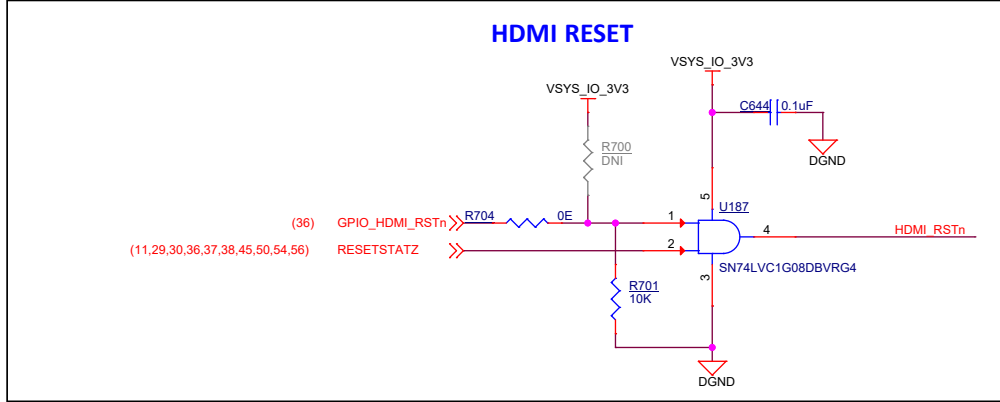
HDMI ESD DEVICE



NOTE:
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.



Silkscreen:
" HDMI "



HDMI RESET

I2C ADDRESS: 0x3B, 0x3F, 0x62

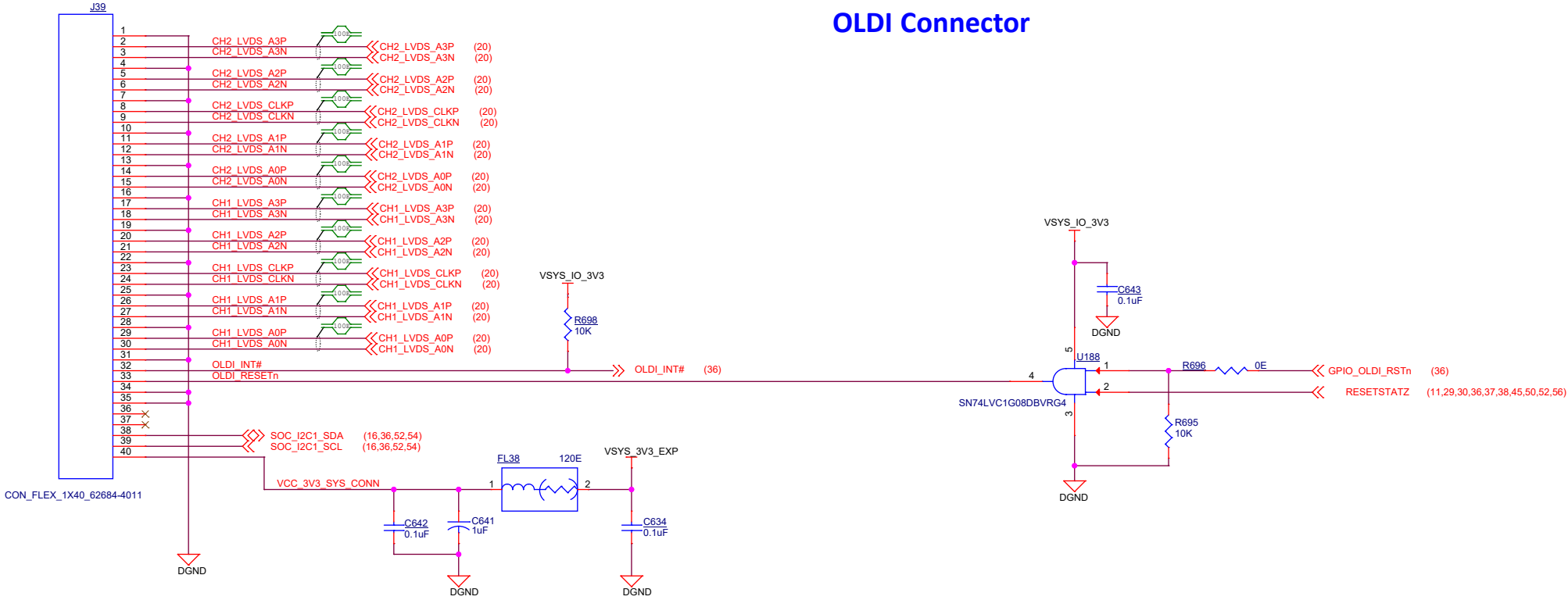
Project :

J7 EVM

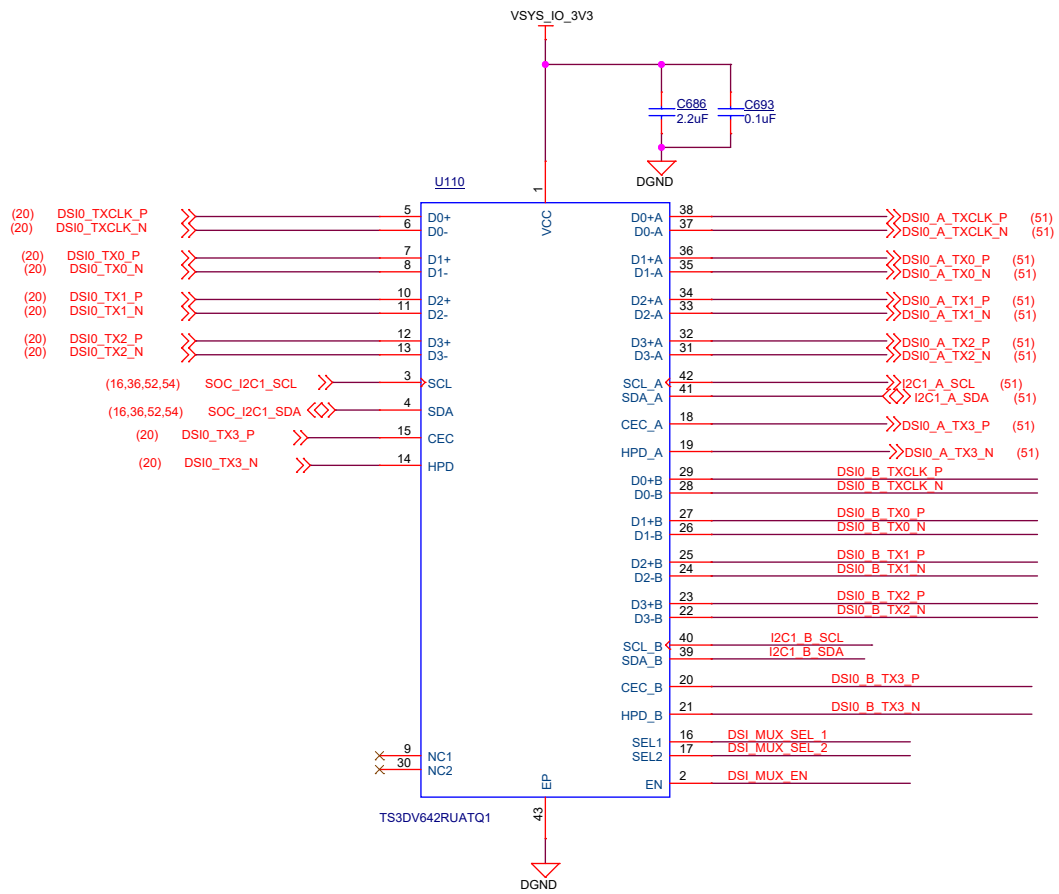


Title SOC DIGITAL IO & SUPPORT POWER 2		
Size	PROC170 002 J722S	Rev
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OLDI Connector

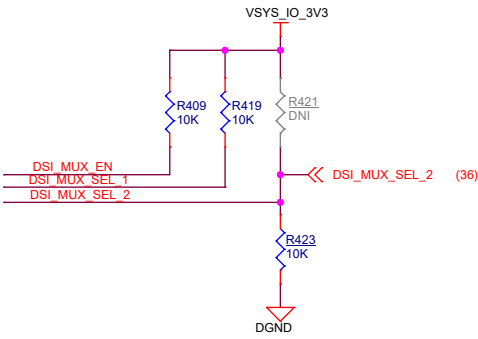


DSI Flex Connector



To DSI to eDP Bridge

To DSI FPC Connector



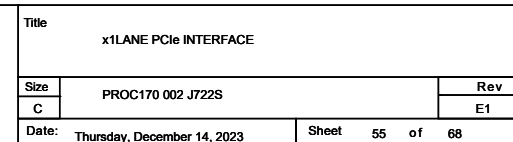
EN	DSI_MUX_SEL_2	FUNCTION
HIGH	LOW	INPUT --> A Port [DSI to eDP Bridge]
HIGH	HIGH	INPUT -->B port [DSI FPC Connector] (default)
LOW	X	Disconnect

x4 Lane PCIe Connector

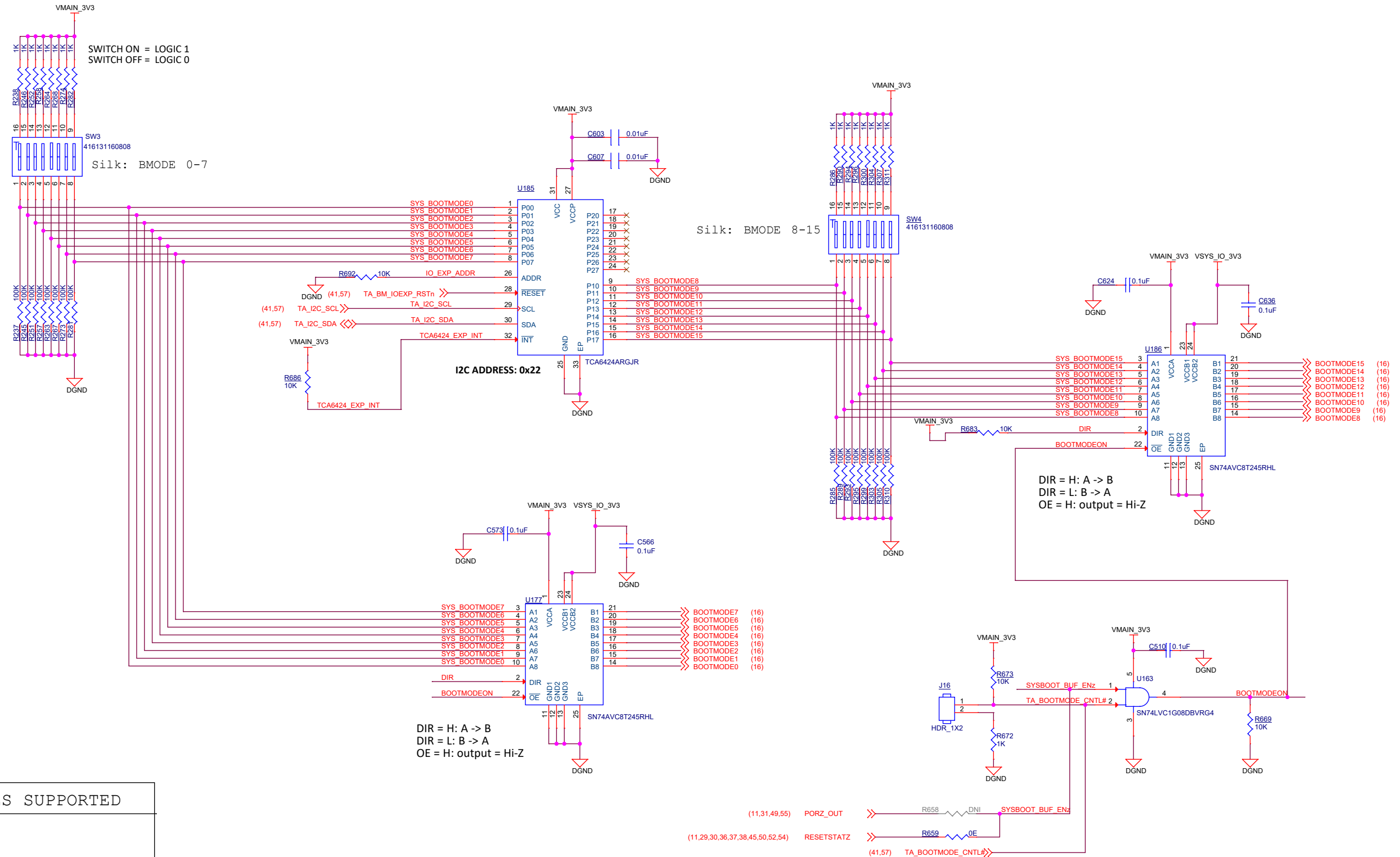
C

2

Project :
J7 EVM



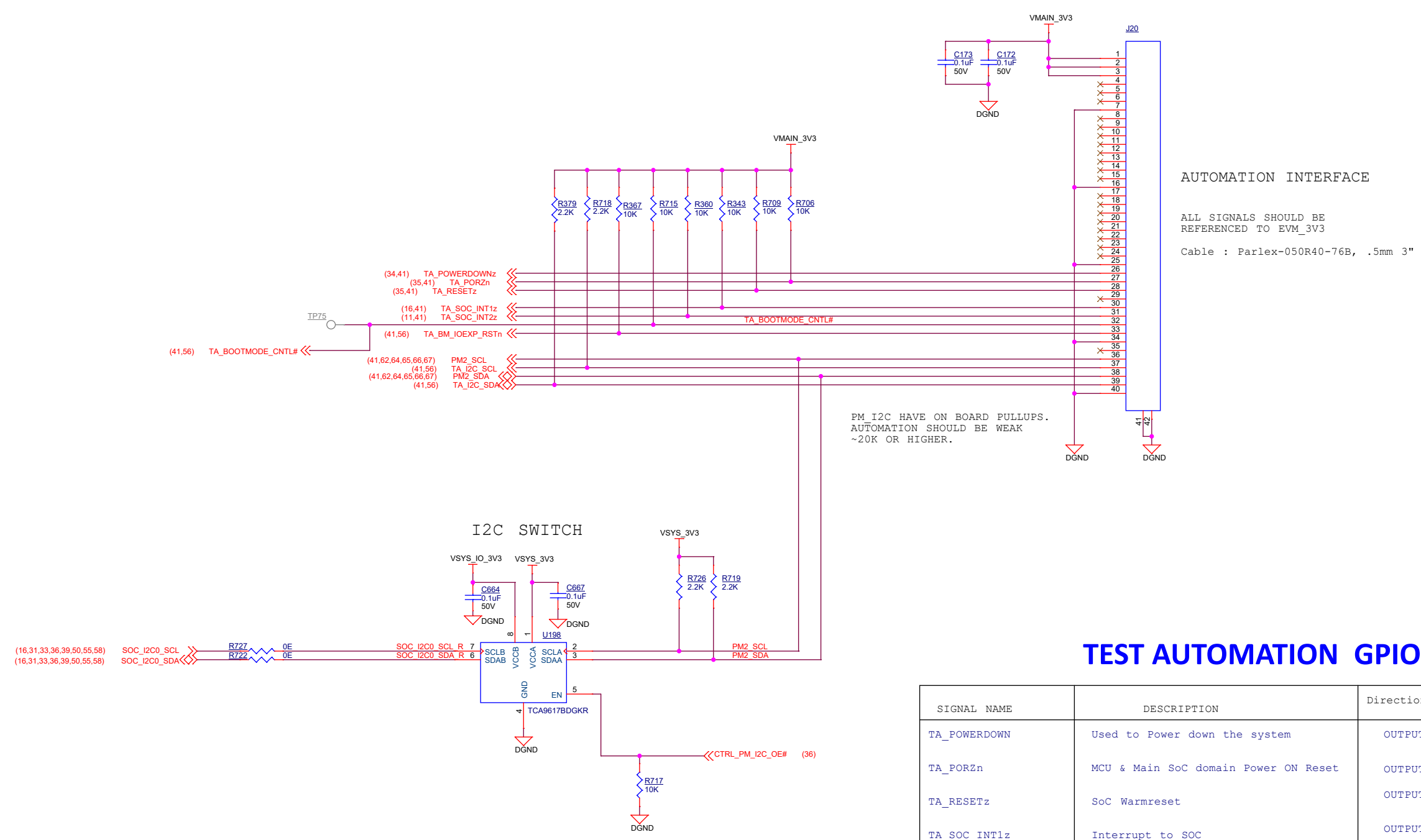
BOOT MODE BUFFERS



BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD (default)
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. No Boot

TEST AUTOMATION HEADER

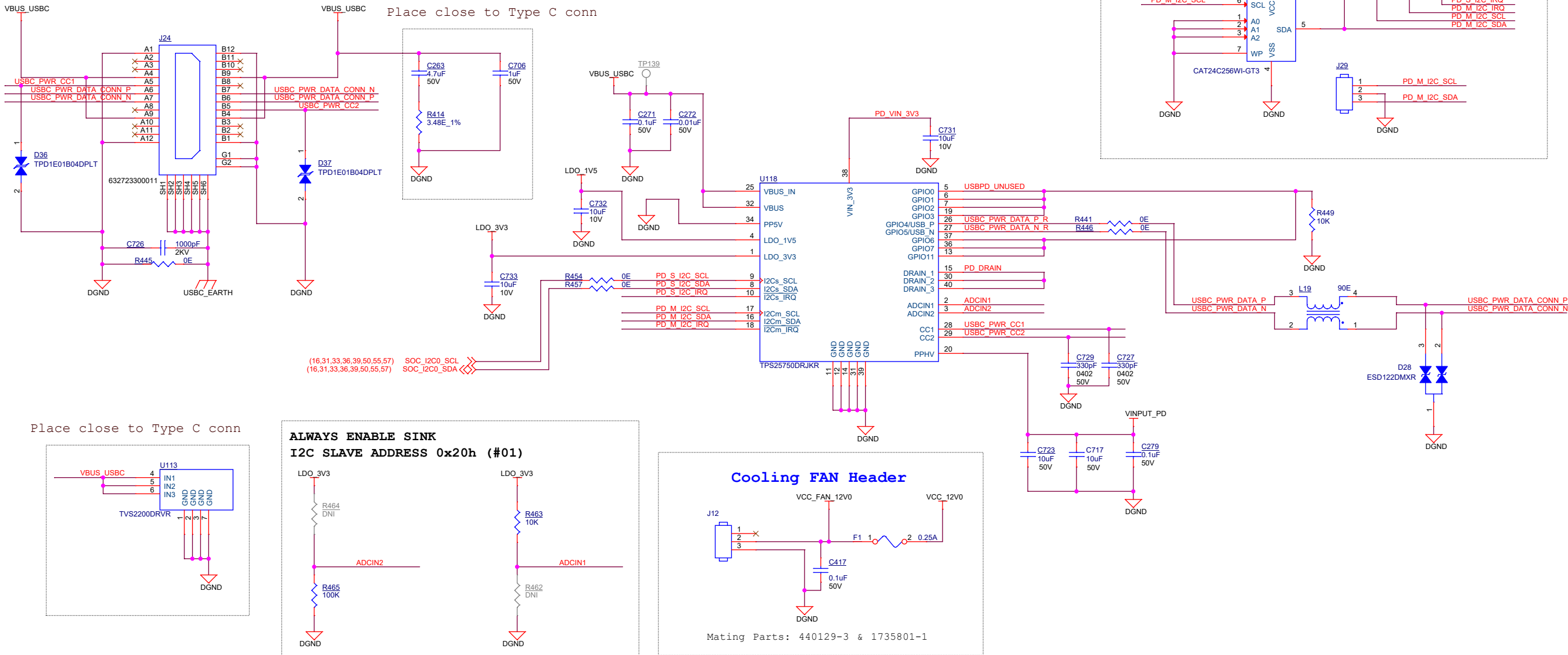
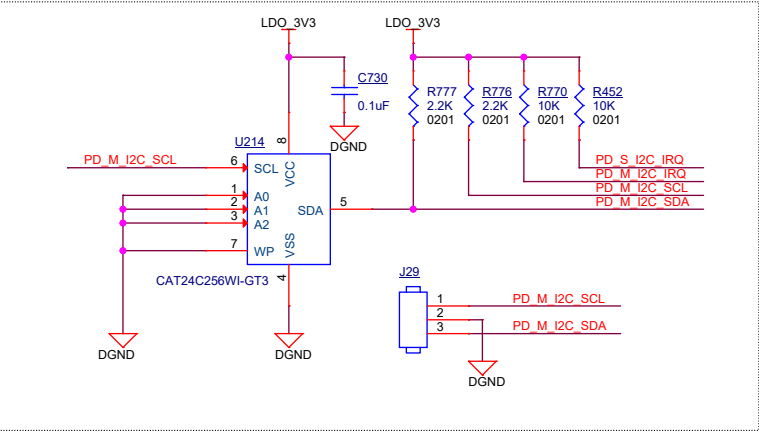


TEST AUTOMATION GPIO MAPPING

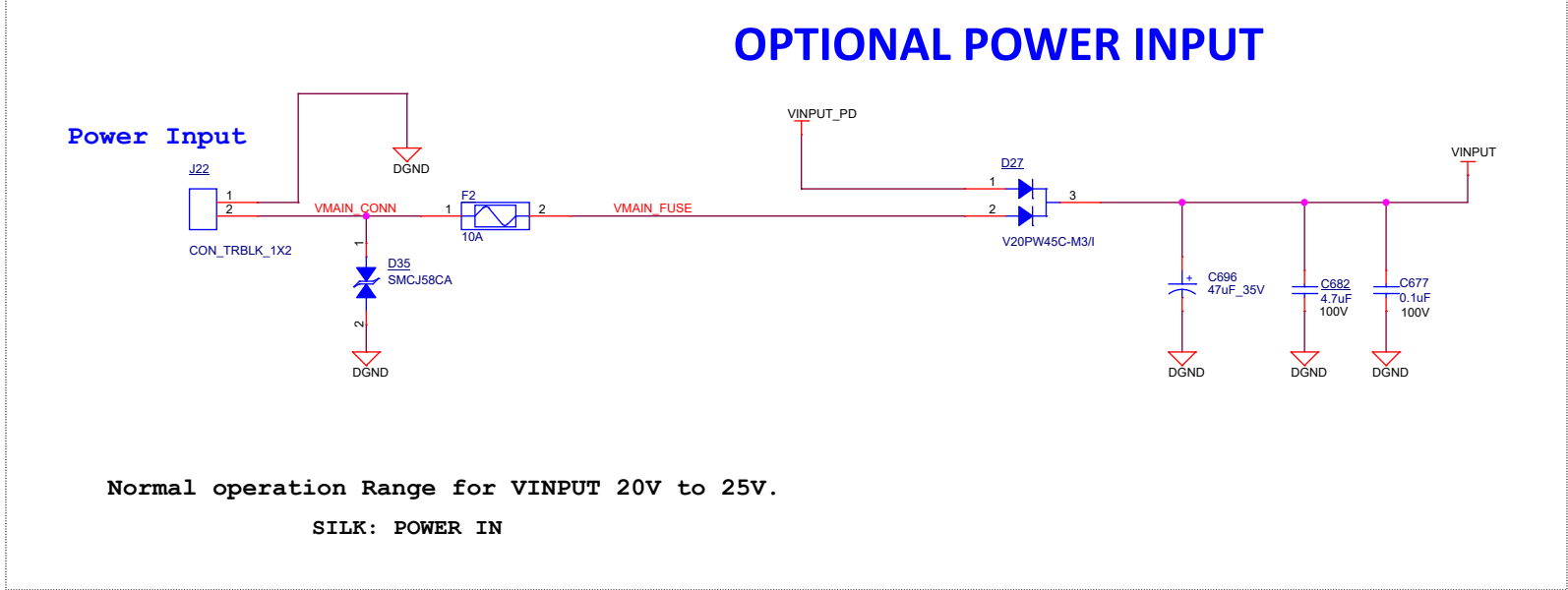
SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

USB-C Power

EEPROM & PROGRAMMING HEADER

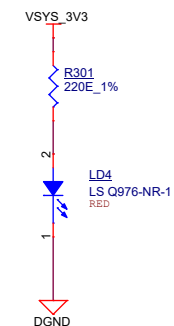


OPTIONAL POWER INPUT

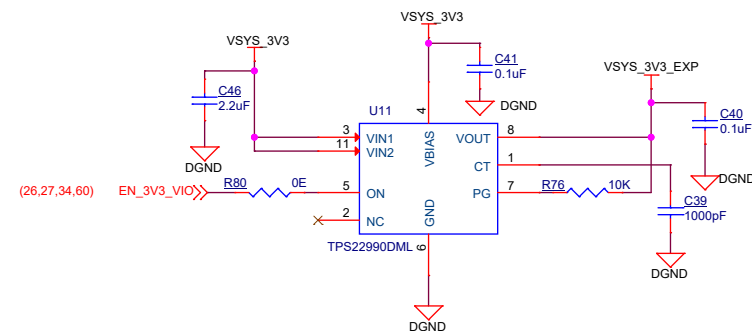


Normal operation Range for VININPUT 20V to 25V.
SILK: POWER IN

TI WEBENCH Simulation Inputs:
Vin (min) = 4.5V Vin (max) = 24V
Vout1 = 3.3V@20A
Ta = 25 deg

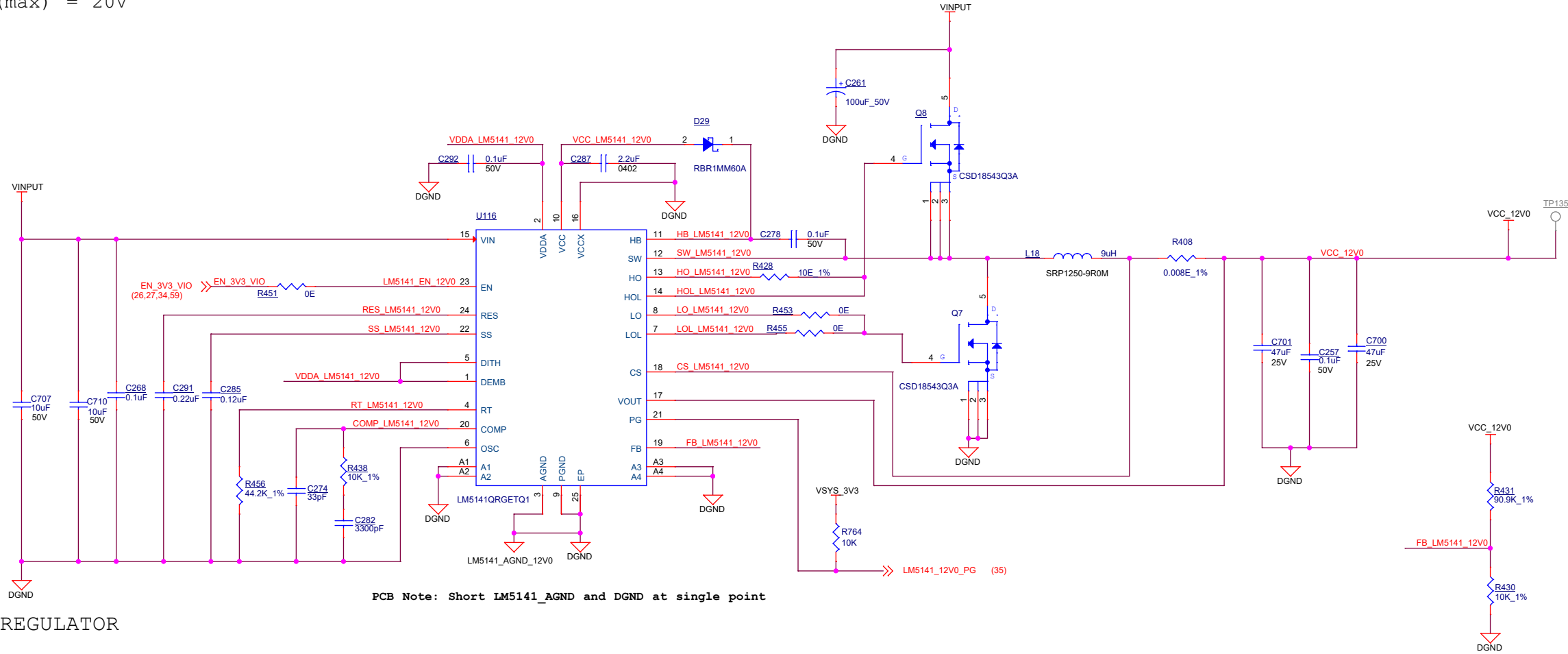


EXP3.3V GENERATION



TI WEBENCH Simulation Inputs:
Vin (min) = 15V Vin (max) = 20V
Vout = 12V@5A
Ta = 25 deg

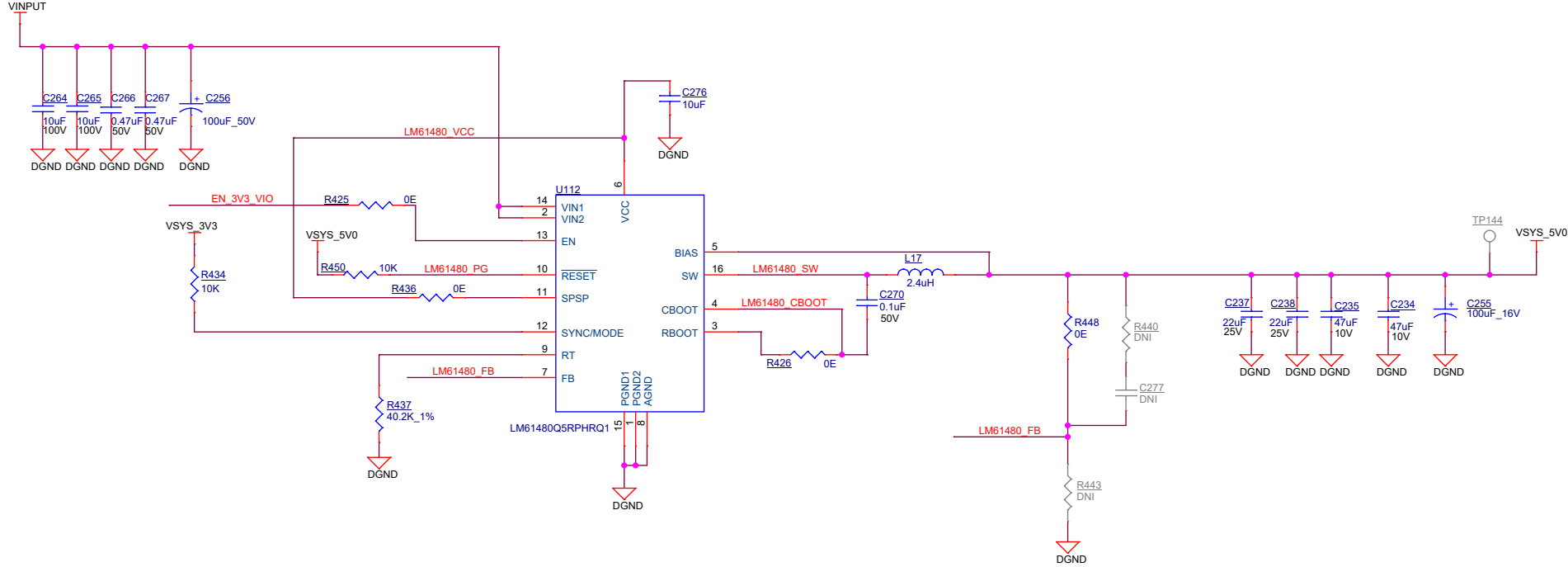
POWER SUPPLY #2



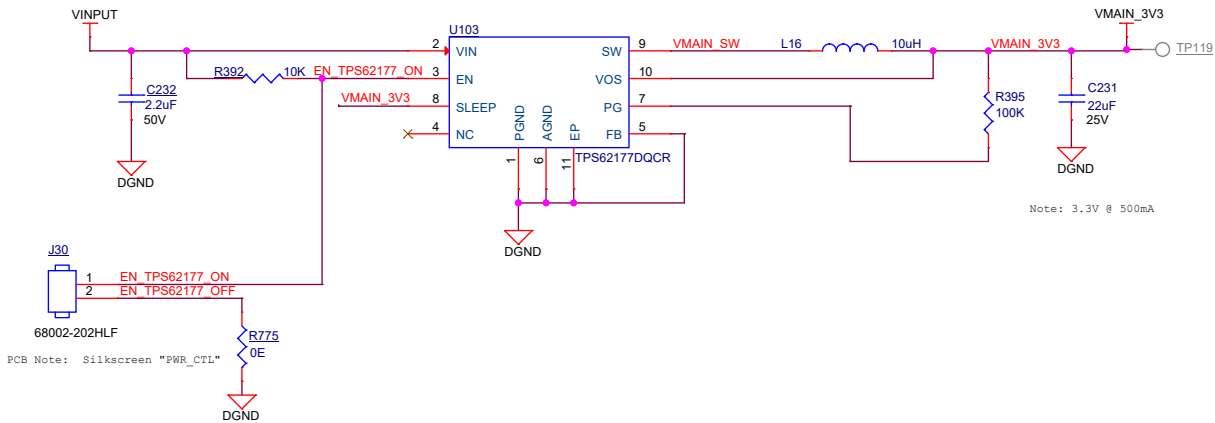
PCB Note: Short LM5141_AGND and DGND at single point

LM61460 5V BUCK REGULATOR
VinMin = 12V
VinMax = 24V
Vout = 5.0V
Iout = 7A

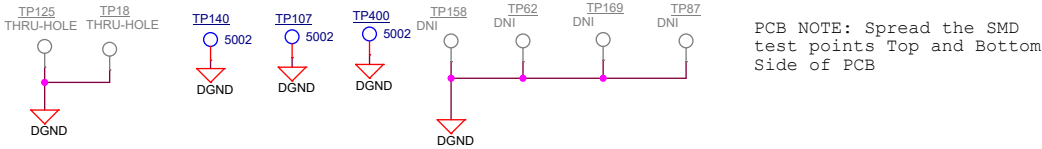
5V GENERATION



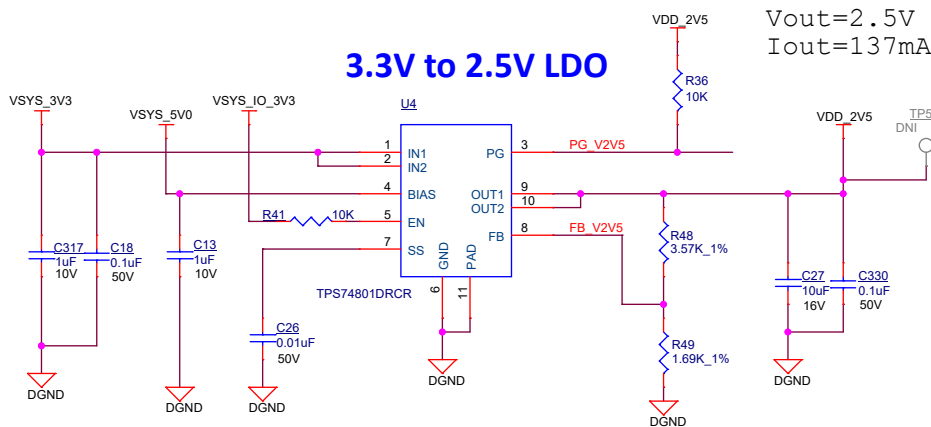
SYSTEM MANAGEMENT 3.3V REGULATOR



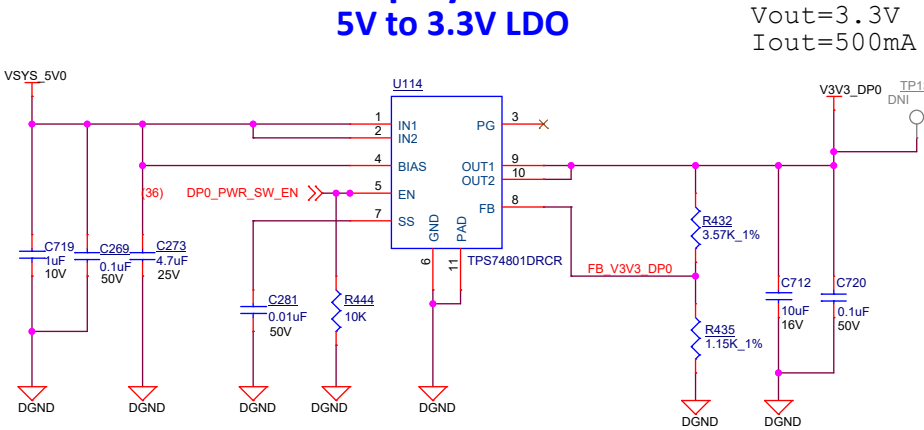
GROUND TEST POINTS



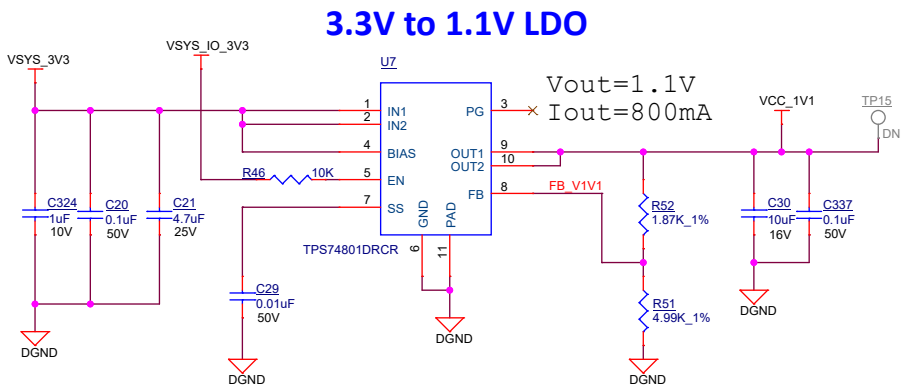
ETHERNET POWER- RGMII1



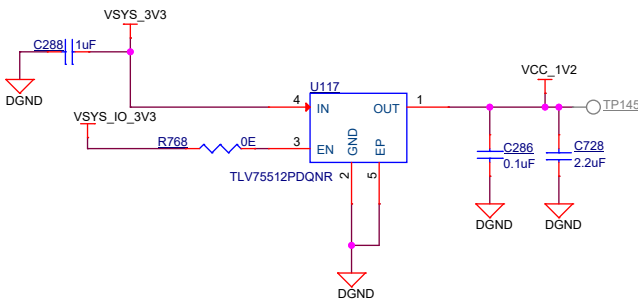
Display Port1
5V to 3.3V LDO



USB HUB POWER & ETHERNET POWER - RGMII1



eDP bridge and HDMI Power
1.2V, 0.5AMPS SUPPLY

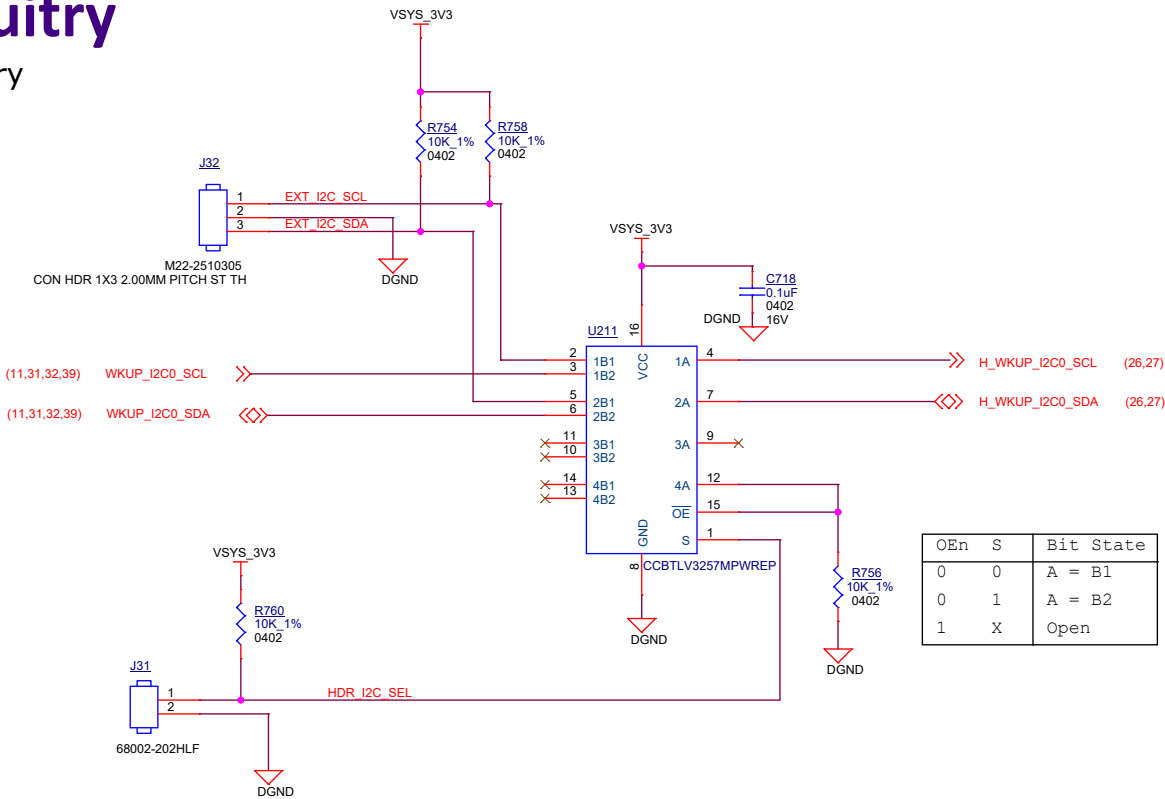


PCB NOTE:Keep 4.7uF capacitor close BIAS pin

Project : J7 EVM		Title POWER SUPPLY #1	
Size C		PROC170 002 J722S	Rev E1
Date: Thursday, December 14, 2023		Sheet 61 of 68	

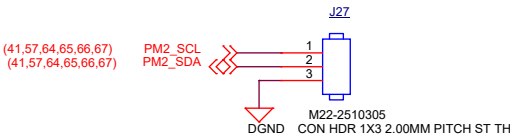
EVM PMIC Support Circuitry

EVM development & evaluation Test circuitry
(TI EVM Only)



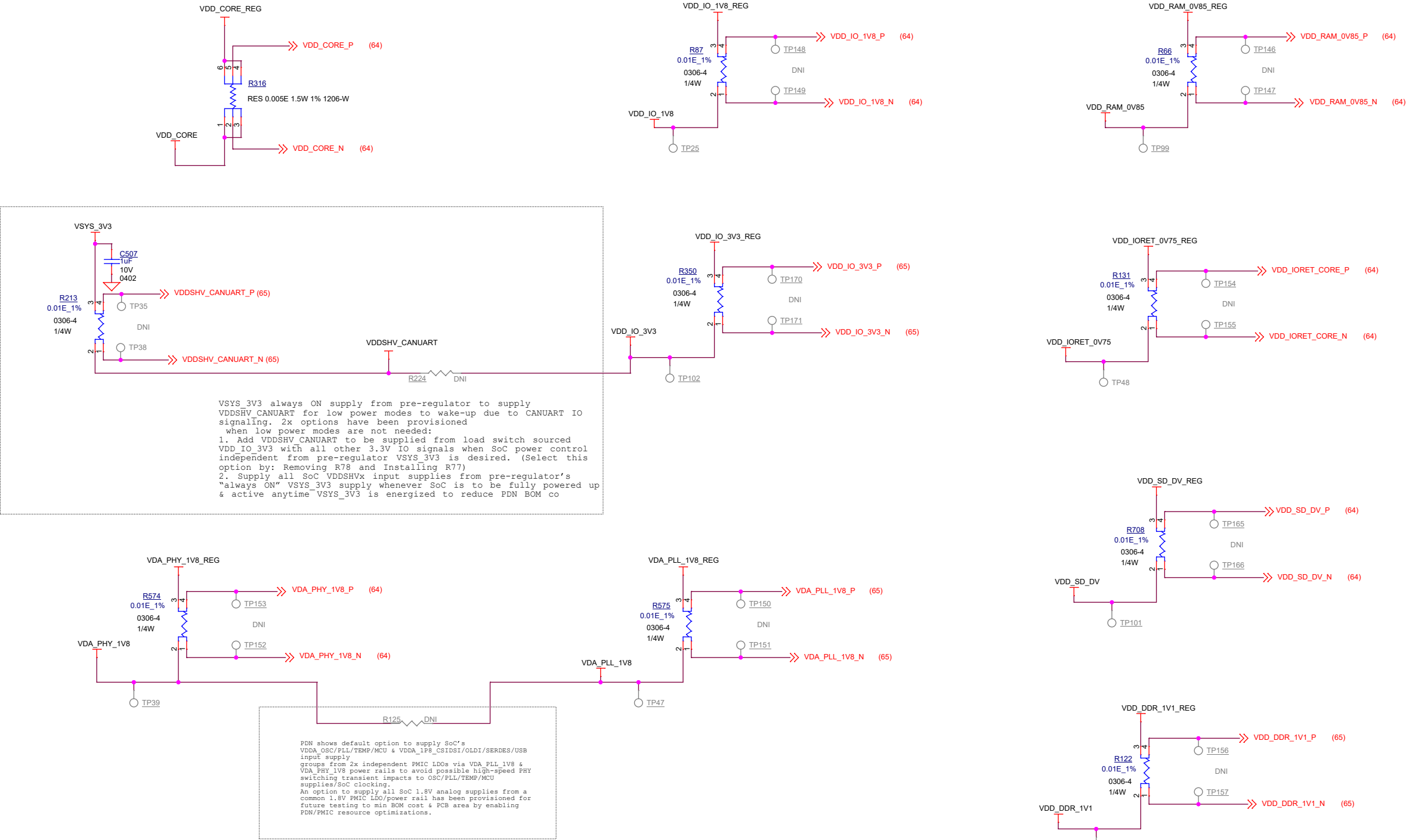
EVM POWER MEASUREMENT I2C BUS ISOLATION

EVM development & evaluation Test circuitry
(TI EVM Only)

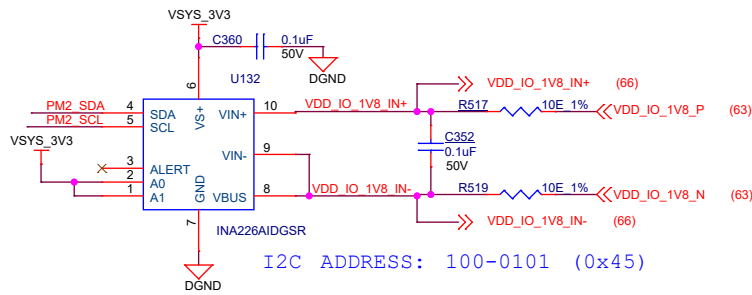
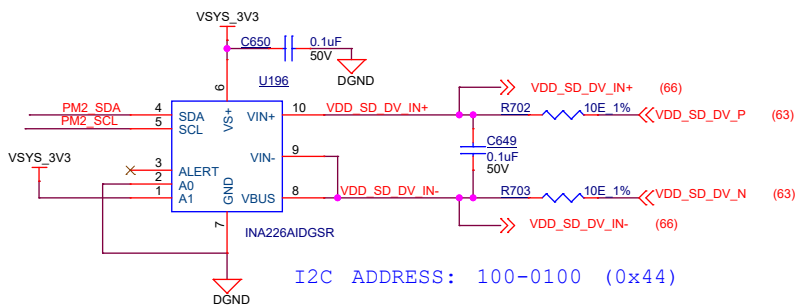
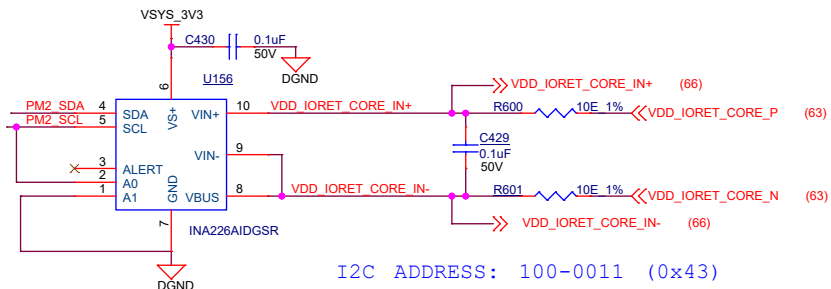
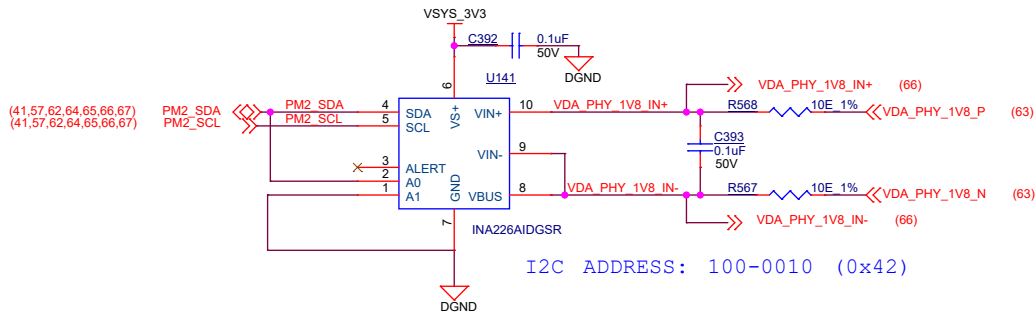
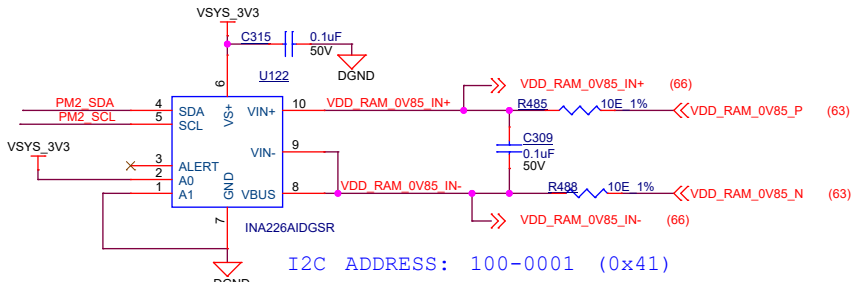
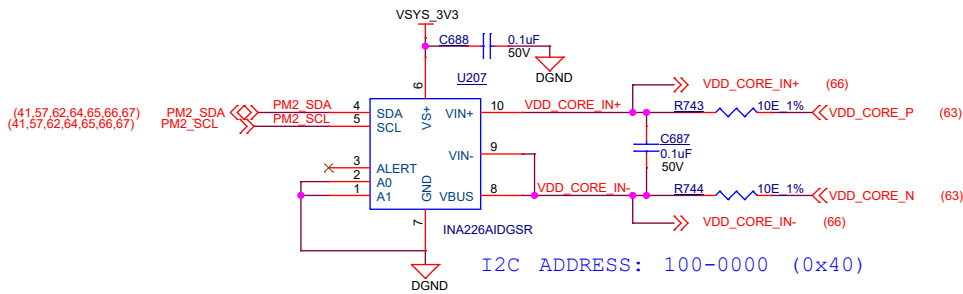


To be updated

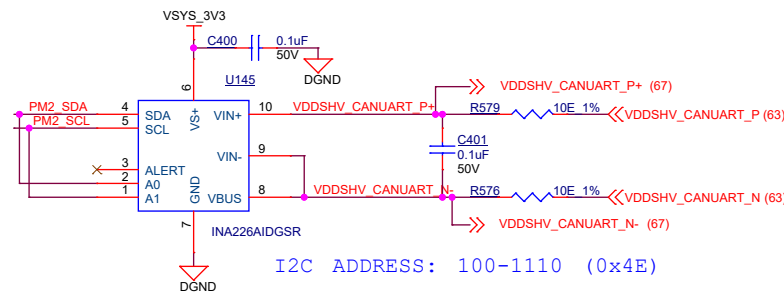
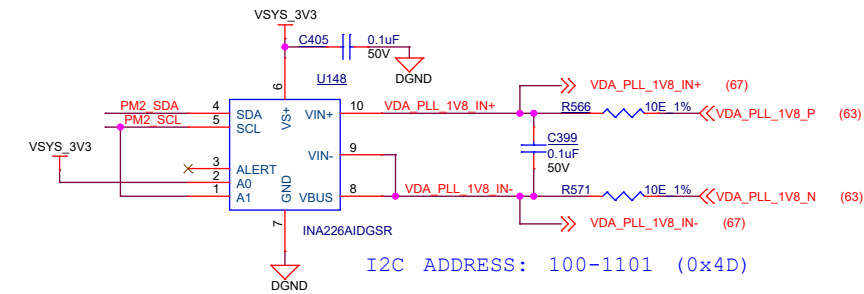
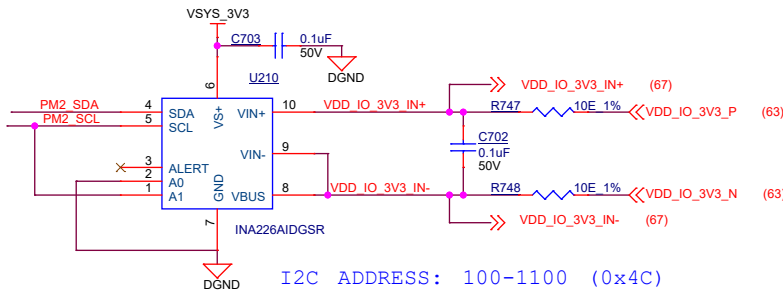
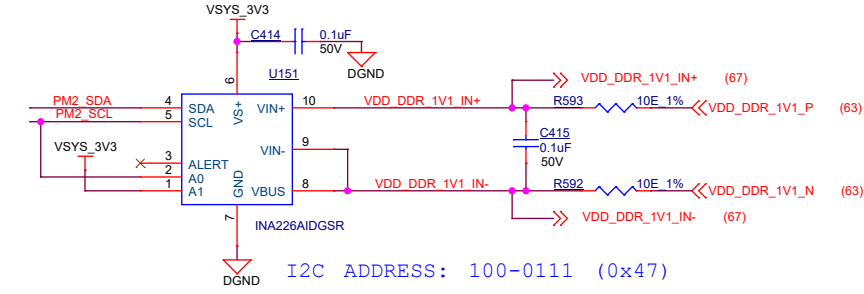
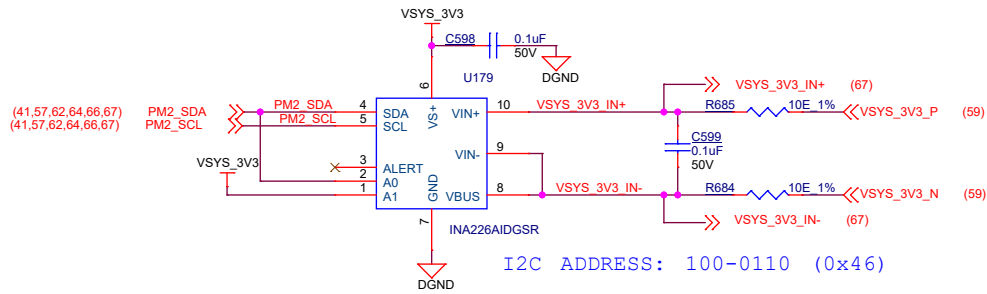
SOC Current Sense Resistors



CURRENT MONITORS #1



CURRENT MONITORS #2



Project :

J7 EVM



Title
CURRENT MONITORS #2

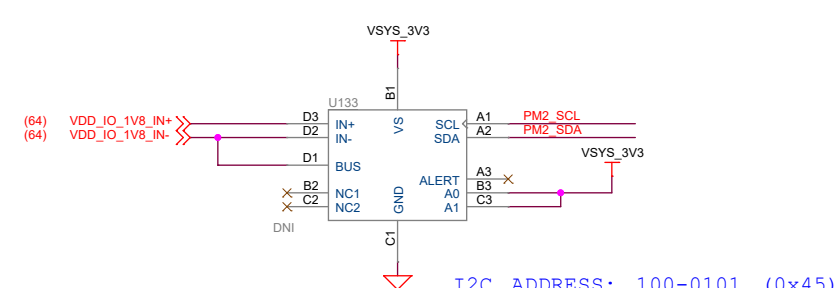
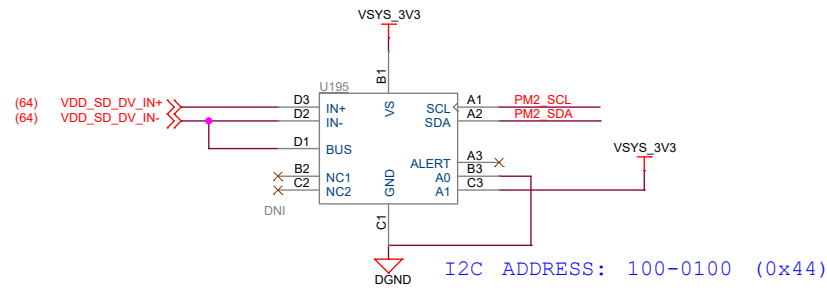
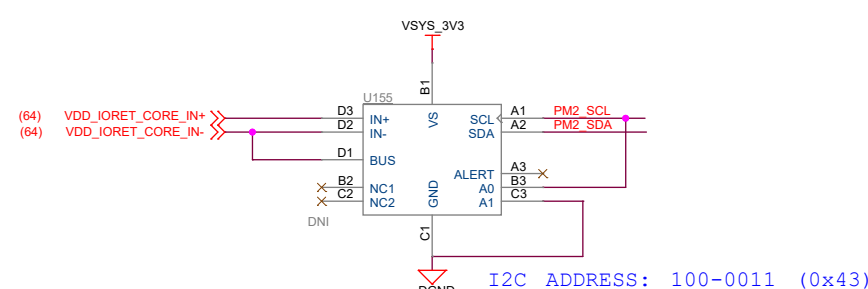
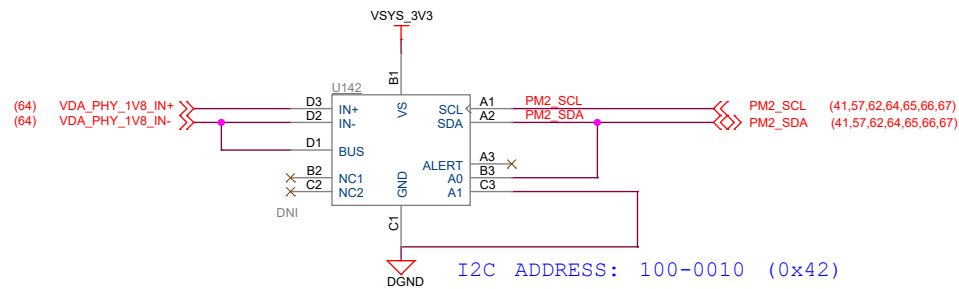
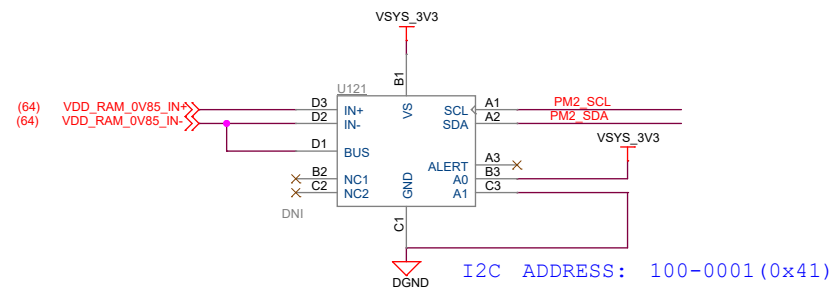
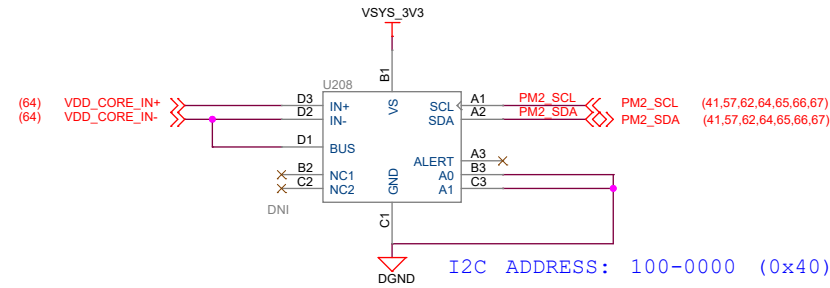
Size
C
PROC170 002 J722S

Date: Thursday, December 14, 2023

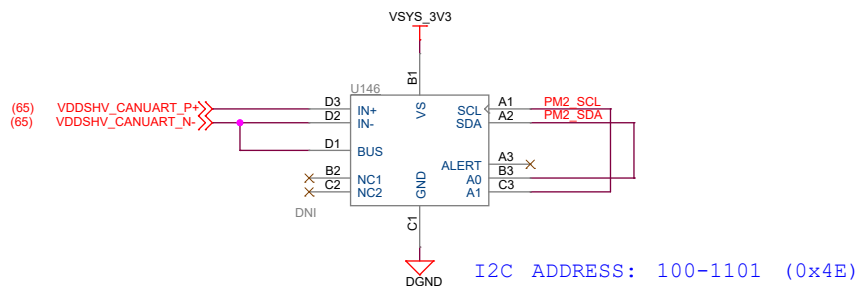
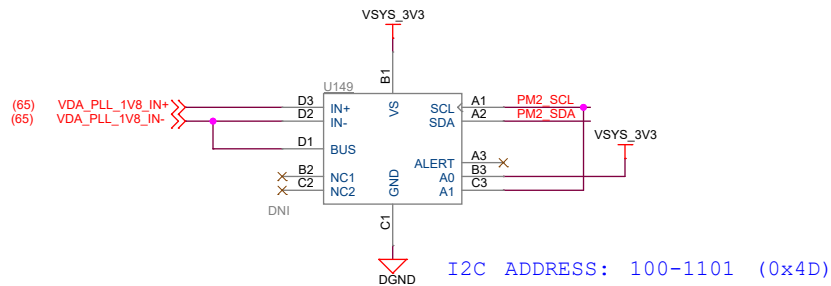
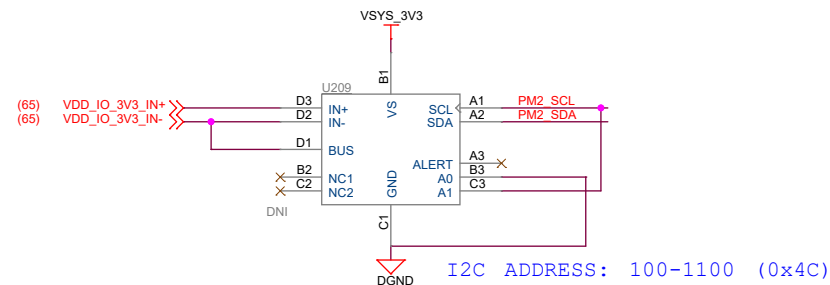
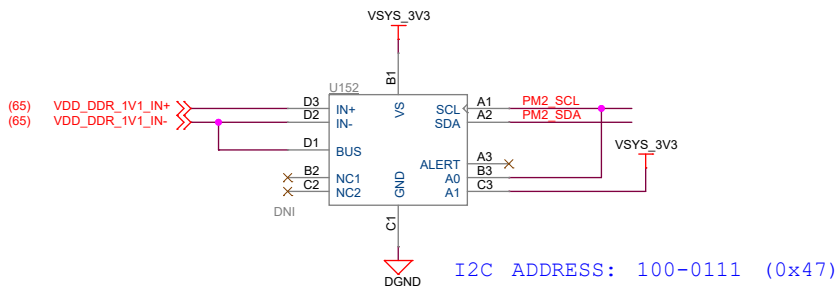
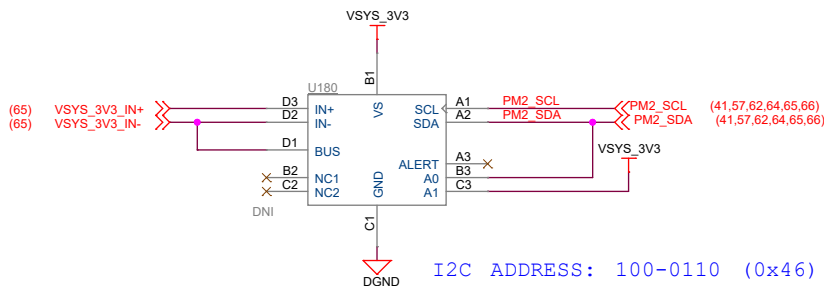
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Rev
E1

CURRENT MONITORS - INA231



CURRENT MONITORS - INA231



NOTES, HW & LABELS

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

LABELS

Board Serial No.



AM6-COMPROCEVM

Assembly Revision.



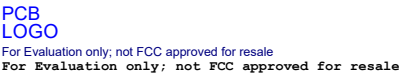
AM6-COMPROCEVM

EVM Orderable Part No.

Orderable Part Numbers

Variant	Label Text
001:Soldered GP SoC	J722SXG01EVM
002:Soldered HS SoC	J722SXH01EVM
003:Socketed SoC	J722SXS01EVM

LOGOs



SCREWS

MH1001



PAN HEAD_M2.5 X 8

MH1002



PAN HEAD_M2.5 X 8

MH1003



PAN HEAD_M2.5 X 8

MH1004



PAN HEAD_M2.5 X 8

MH1005



PAN HEAD_M2.5 X 8

MH1006



PAN HEAD_M2.5 X 8

MH1007



PAN HEAD_M2.5 X 8

STANDOFFs

MH1008



HEX SPACER_M2.5 X 12

MH1009



HEX SPACER_M2.5 X 12

MH1010



HEX SPACER_M2.5 X 12

MH1011



HEX SPACER_M2.5 X 12

MH1012



HEX SPACER_M2.5 X 12

MH1013



HEX SPACER_M2.5 X 12

MH1014



HEX SPACER_M2.5 X 12

WASHER

ACC1



PLAIN WASHER_M2.5

ACC2



PLAIN WASHER_M2.5

ACC3



PLAIN WASHER_M2.5

ACC4



PLAIN WASHER_M2.5

ACC5



PLAIN WASHER_M2.5

ACC6



PLAIN WASHER_M2.5

ACC7



PLAIN WASHER_M2.5

FIDUCIALS



FID1001
FID_40X80



FID1002
FID_40X80



FID1003
FID_40X80



FID1004
FID_40X80



FID1005
FID_40X80



FID1006
FID_40X80

BARE PCB

PCB1



PROC170E2

J7AEN SOC

ACC16



DNI

SOCKET

ACC17



DNI

Project :

J7 EVM



Title
HARDWARE SCHEMATICS

Size
C
PROC170 002 J722S

Date: Friday, January 05, 2024

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Rev

E1