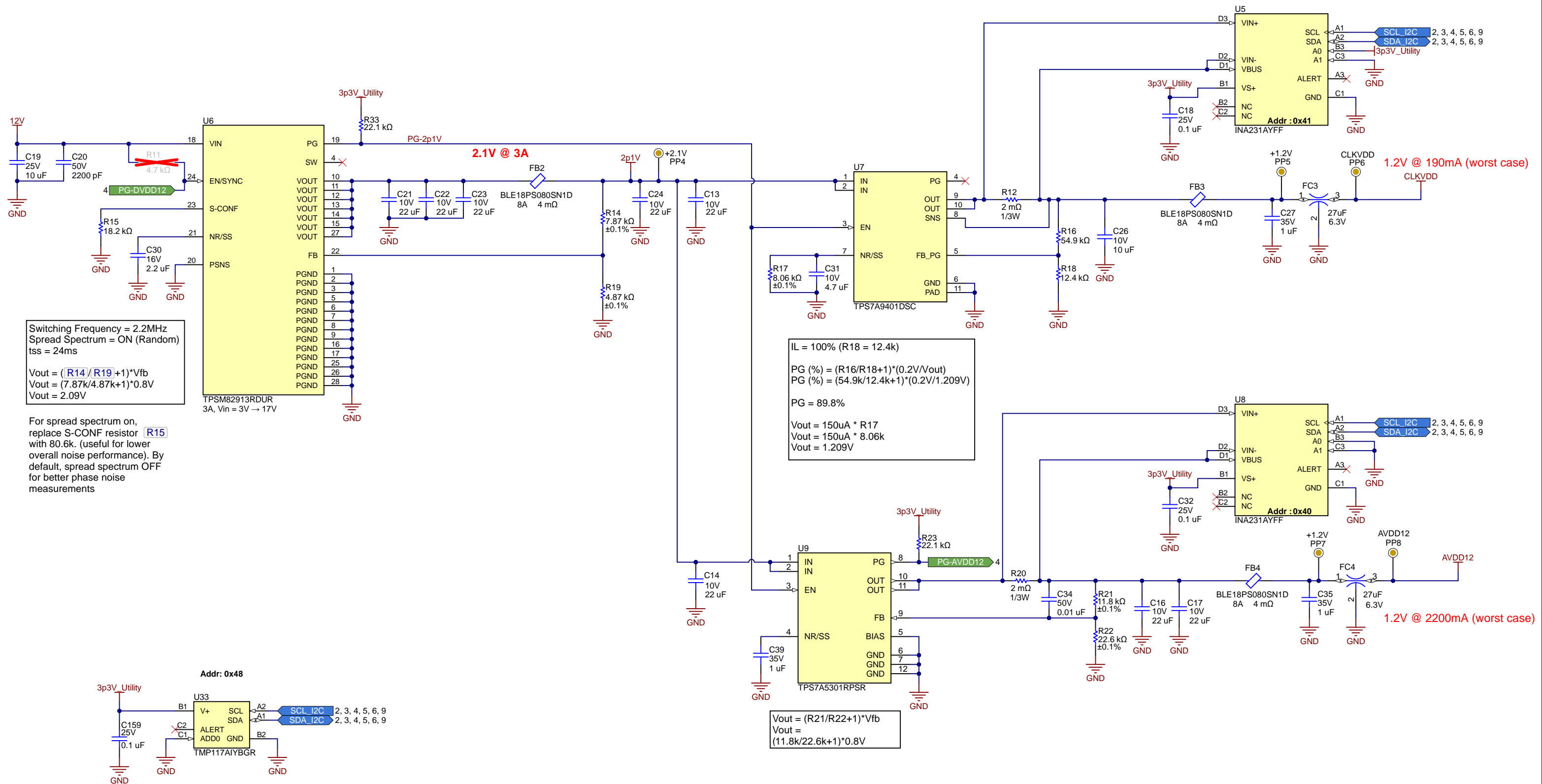







## EVM Power 2



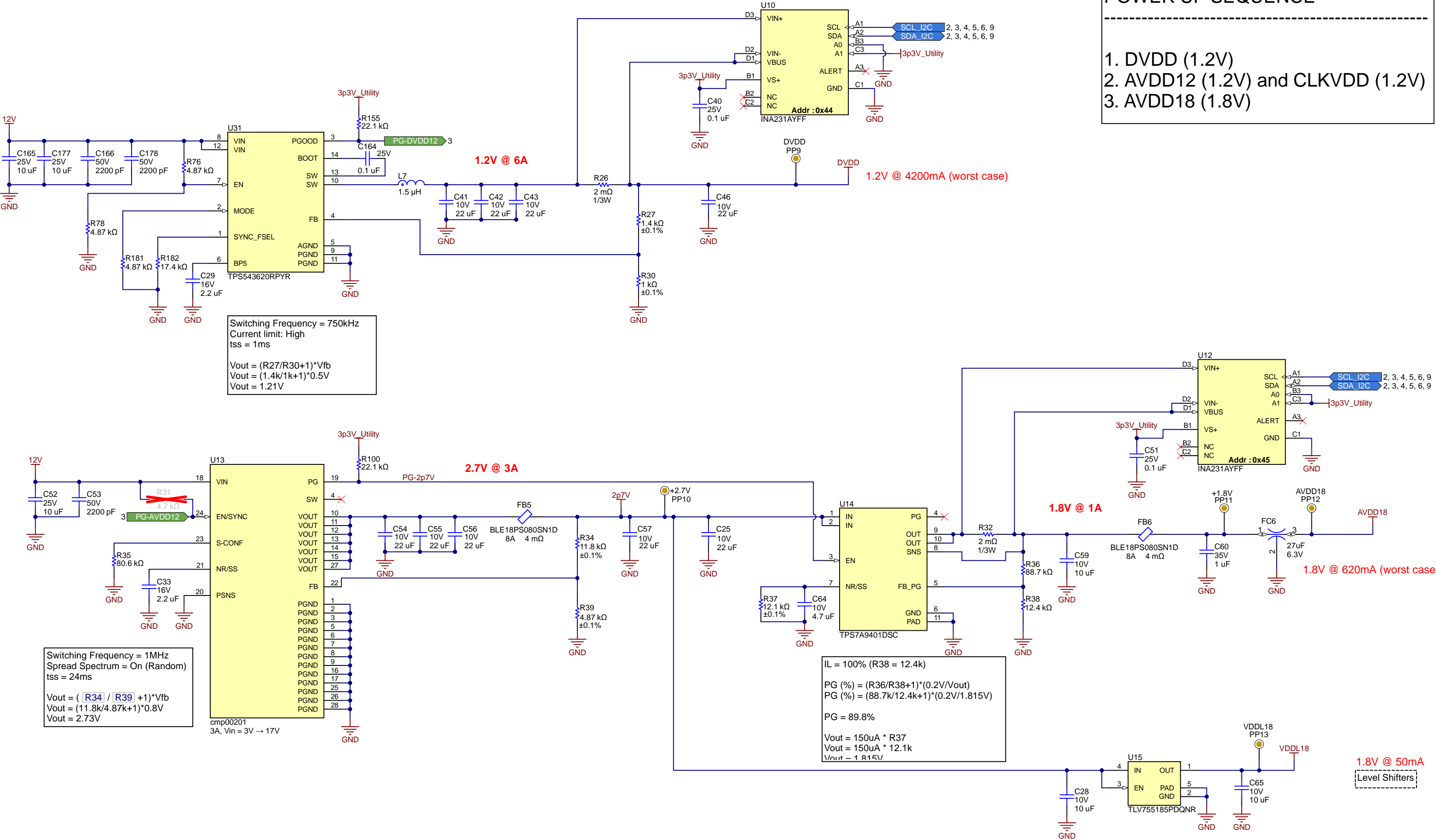
Orderable: <b>ADC32RF55EVM</b>	Designed for: <b>Not For Public Release</b>	Mod. Date: 6/3/2024	 <b>TEXAS INSTRUMENTS</b>  <a href="http://www.ti.com">http://www.ti.com</a> © Texas Instruments 2024
TID #: <b>N/A</b>	Project Title: <b>ADC32RF55EVM</b>		
Number: <b>DC142D</b>	Rev: <b>D1</b>	Sheet Title: <b>EVM Power 2</b>	
SVN Rev:	Assembly Variant: <b>-001</b>		
Drawn By: <b>CW</b>	File: <b>DC142D_ADC32RF55_Power2_RevA1.SchDoc</b>		
Engineer: <b>CW</b>	Contact: <a href="http://www.ti.com">http://www.ti.com</a> support		Sheet: <b>3</b> of <b>13</b> Size: <b>B</b>

POWER UP SEQUENCE

1. DVDD (1.2V)

2. AVDD12 (1.2V) and CLKVDD (1.2V)

3. AVDD18 (1.8V)



USB Interface

A

B

C

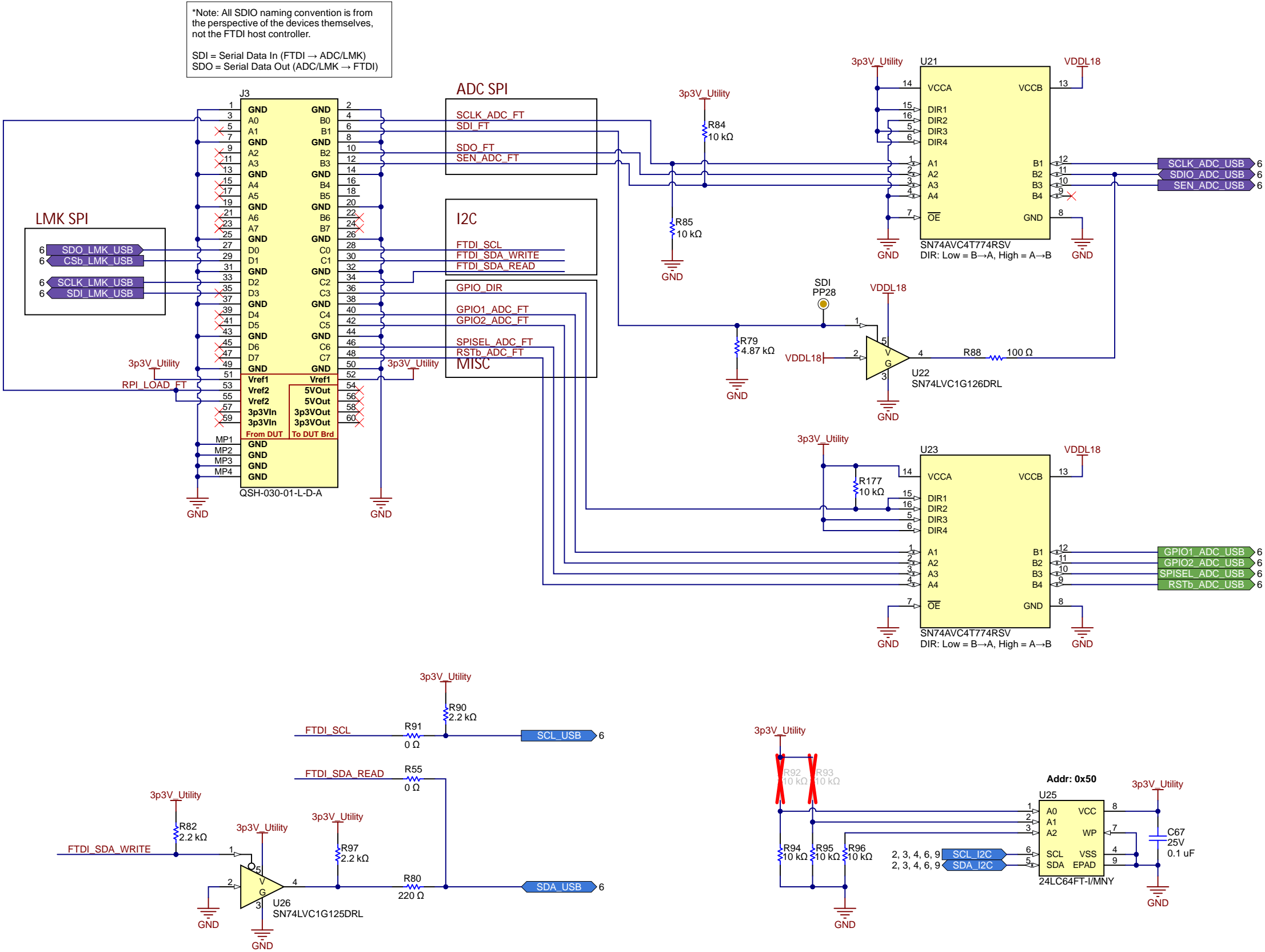
D

A

B

C

D



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Orderable: ADC32RF55EVM	Designed for: Not For Public Release	Mod. Date: 6/3/2024
TID #: N/A	Project Title: ADC32RF55EVM	
Number: DC142D	Rev: D1	Sheet Title: USB Interface
SVN Rev:	Assembly Variant: -001	Sheet: 5 of 13
Drawn By: CW	File: DC142D_ADC32RF55_USB_RevA1.SchDoc	Size: B
Engineer: CW	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

MUXes

A

B

C

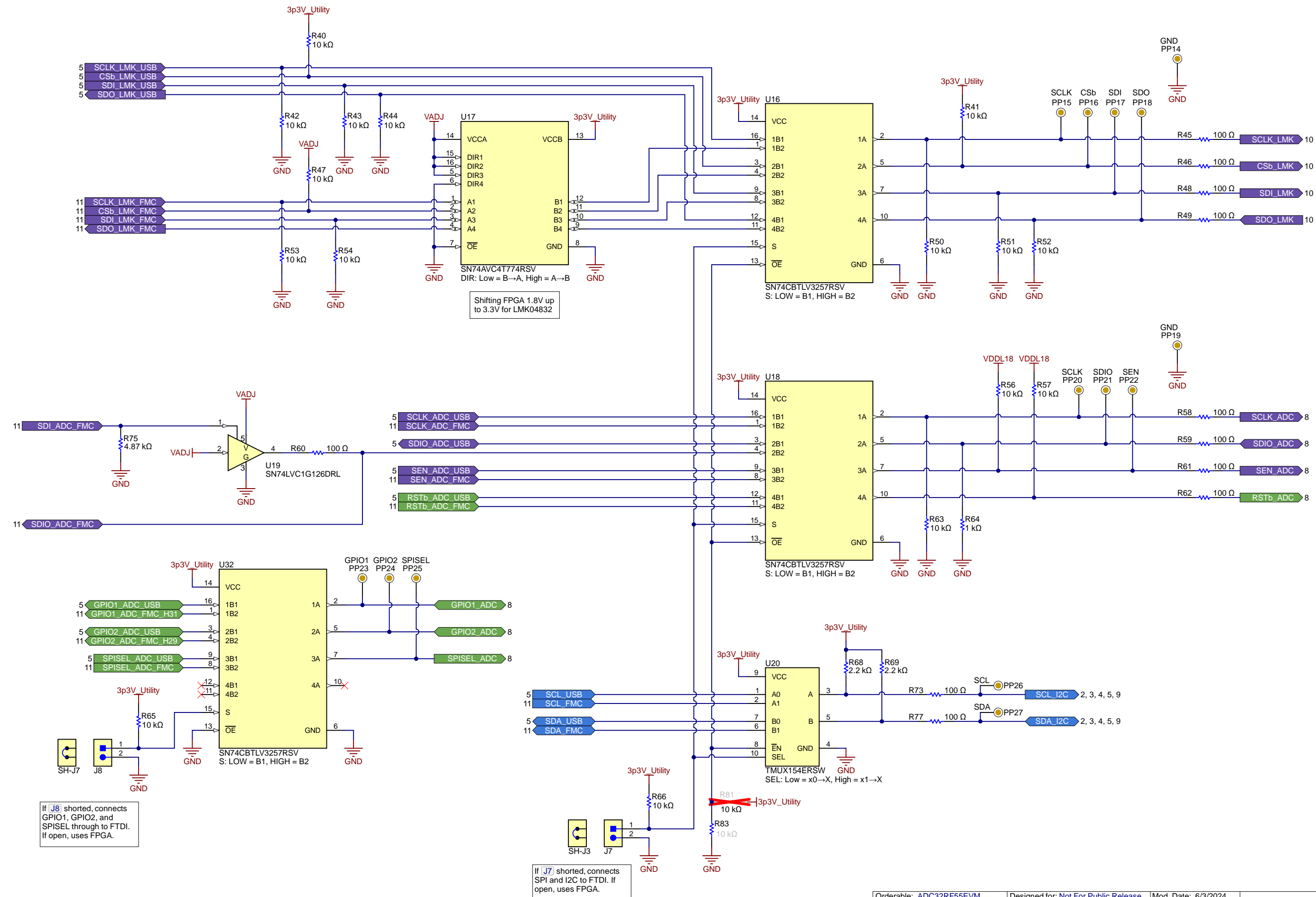
D

A

B

C

D



If **J8** shorted, connects GPIO1, GPIO2, and SPISEL through to FTDI. If open, uses FPGA.

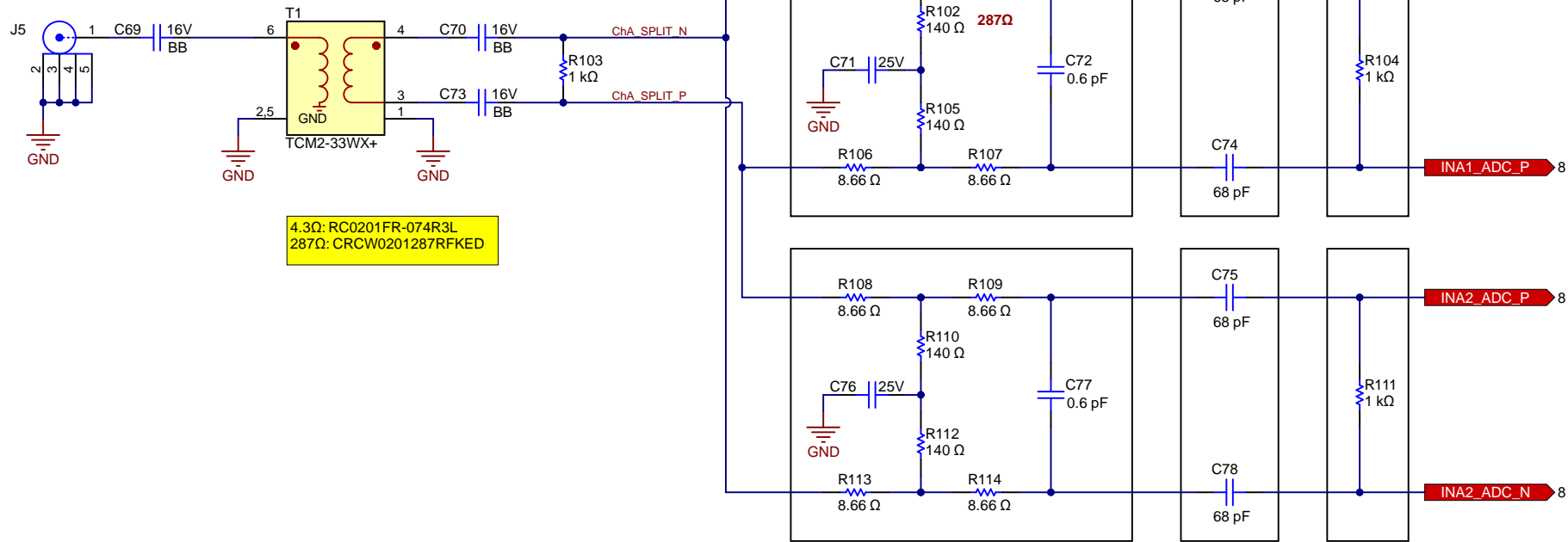
If **J7** shorted, connects SPI and I2C to FTDI. If open, uses FPGA.

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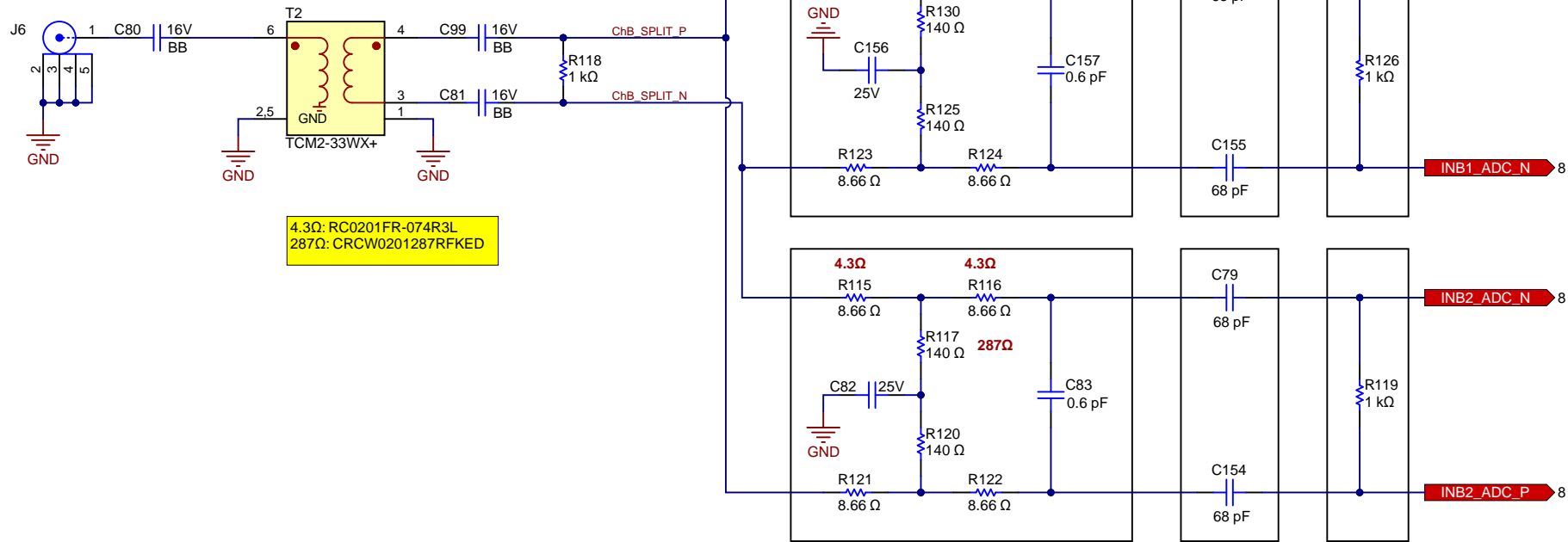
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TID #: N/A	Project Title: ADC32RF55EVM	
Number: DC142D	Rev: D1	Sheet Title: MUXes
SVN Rev:	Assembly Variant: -001	Sheet: 6 of 13
Drawn By: CW	File: DC142D_ADC32RF55_MUX_RevA1.SchDoc	Size: B
Engineer: CW	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	© Texas Instruments 2024



Channel A\_split



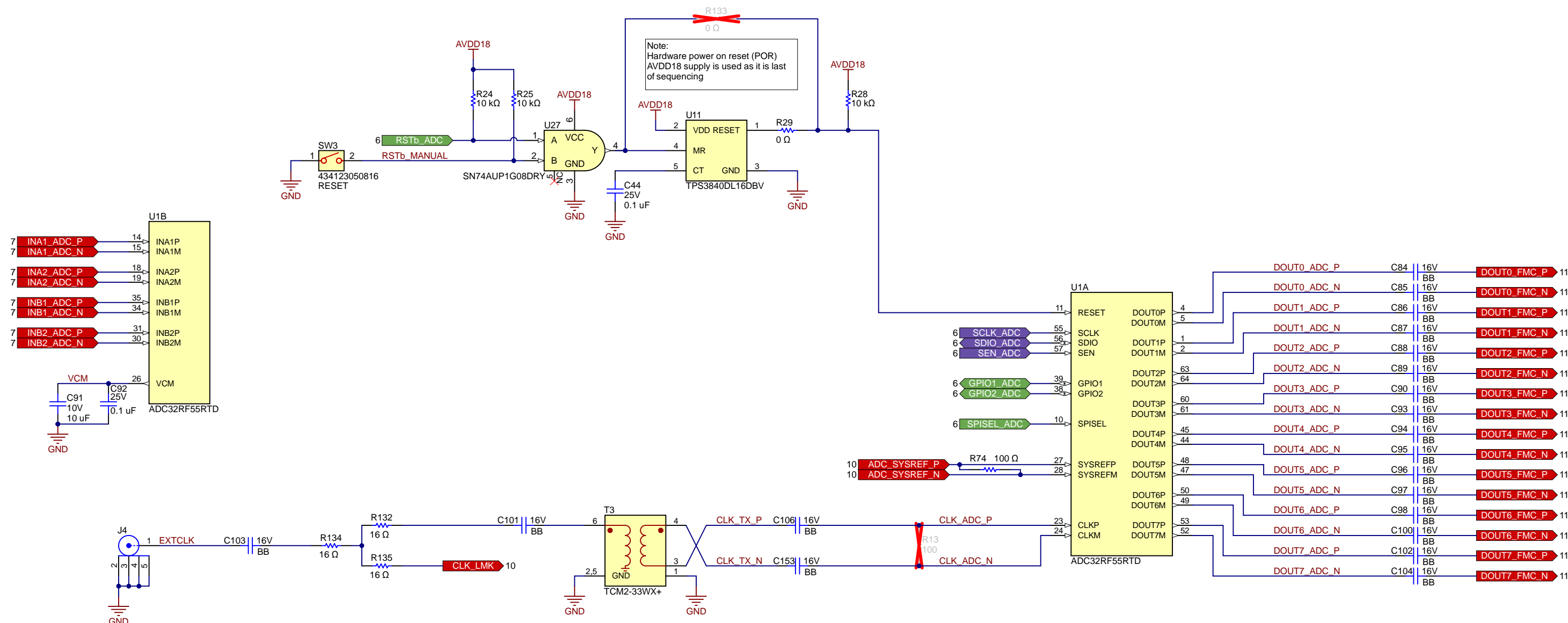
Channel B\_split



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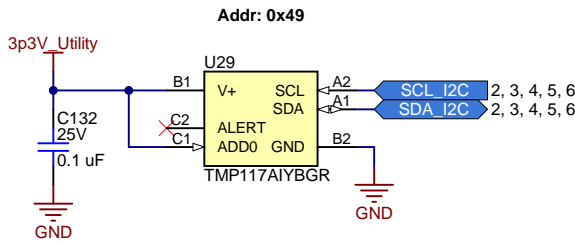
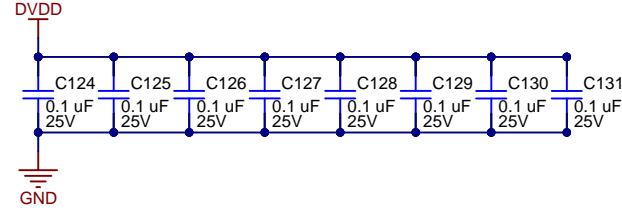
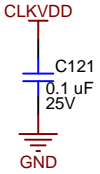
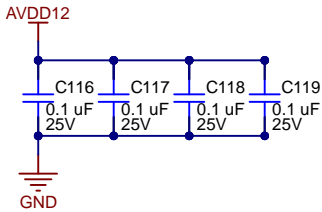
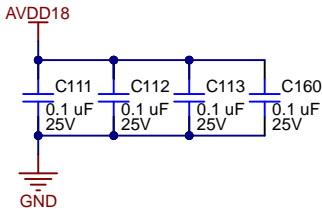
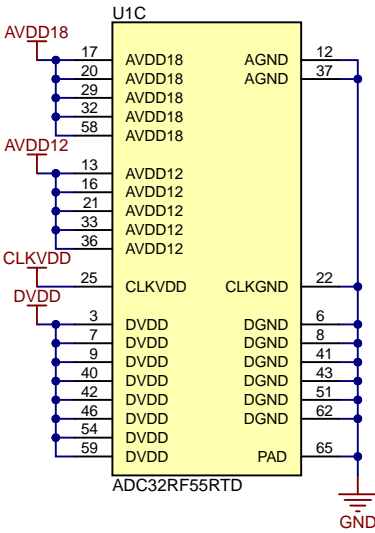
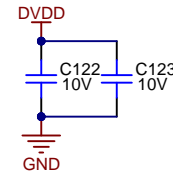
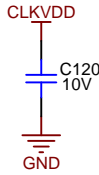
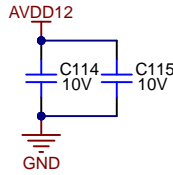
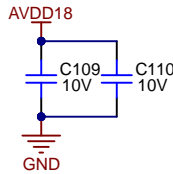
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TID #: N/A	Project Title: ADC32RF55EVM	
Number: DC142D	Rev: D1	Sheet Title: ADC EVM RF Input
SVN Rev:	Assembly Variant: -001	Sheet: 7 of 13
Drawn By: CW	File: DC142D_ADC32RF55_ADC_Input_RevA1.Sch	Size: B
Engineer: CW	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

ADC Input, SERDES and Digital Pins





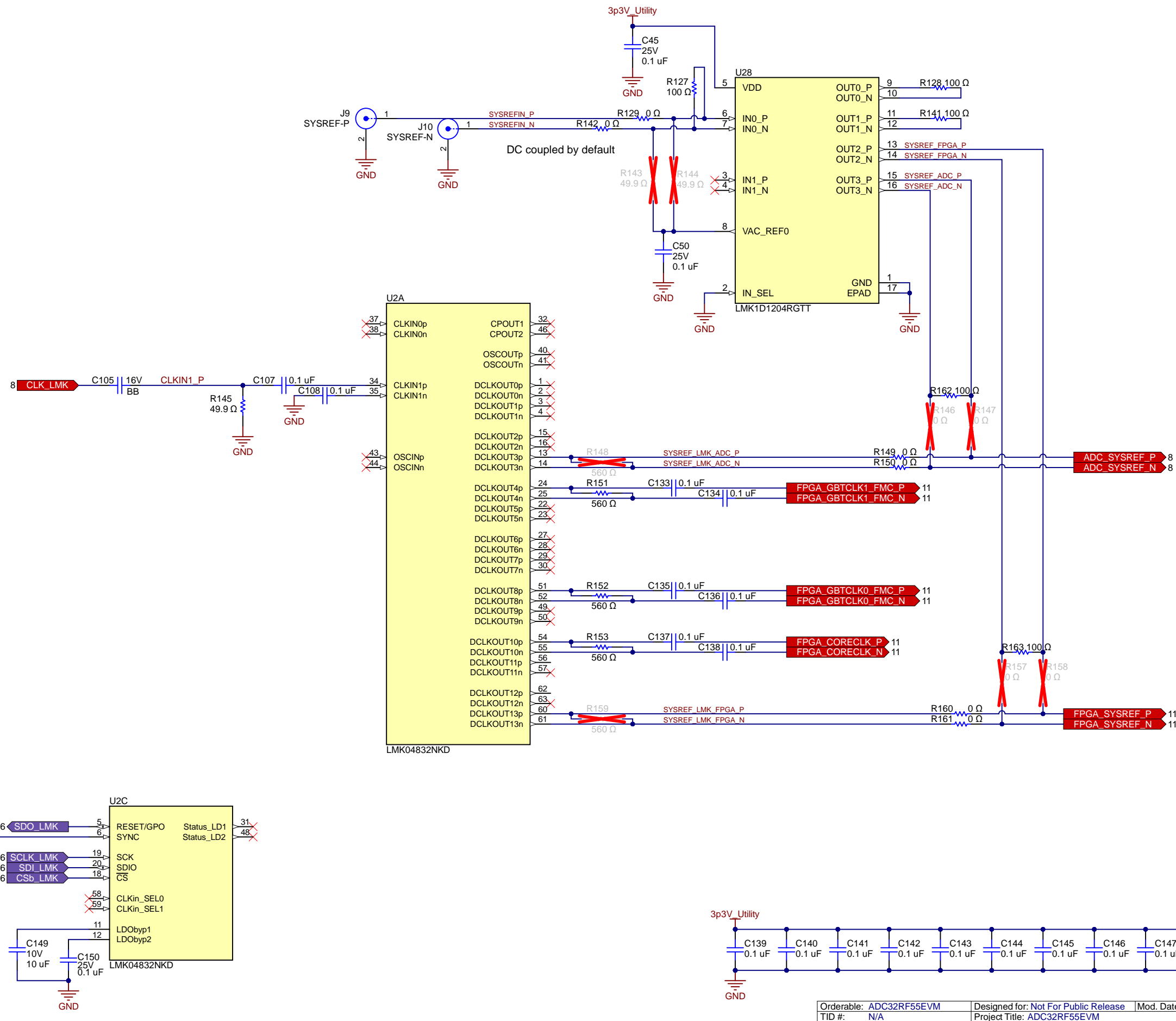
ADC EVM Power



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Orderable: ADC32RF55EVM	Designed for: Not For Public Release	Mod. Date: 6/3/2024
TID #: N/A	Project Title: ADC32RF55EVM	
Number: DC142D	Rev: D1	Sheet Title: ADC EVM Power
SVN Rev:	Assembly Variant: -001	Sheet: 9 of 13
Drawn By: CW	File: DC142D_ADC32RF55_ADC_Power_RevA1.SchDoc	Size: B
Engineer: CW	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

## LMK04832 Clock Fanout



Orderable: <b>ADC32RF55EVM</b>	Designed for: <b>Not For Public Release</b>	Mod. Date: 6/3/2024	 <b>TEXAS INSTRUMENTS</b>  <a href="http://www.ti.com">http://www.ti.com</a> © Texas Instruments 2024
TID #: <b>N/A</b>	Project Title: <b>ADC32RF55EVM</b>		
Number: <b>DC142D</b>	Rev: <b>D1</b>	Sheet Title: <b>LMK04832 Clock Fanout</b>	
SVN Rev:	Assembly Variant: <b>-001</b>	Sheet: 10 of <b>13</b>	
Drawn By: <b>CW</b>	File: <b>DC142D_ADC32RF55_LMK_RevA1.SchDoc</b>   Size: B		
Engineer: <b>CW</b>	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>		

FMC Connector

A

B

C

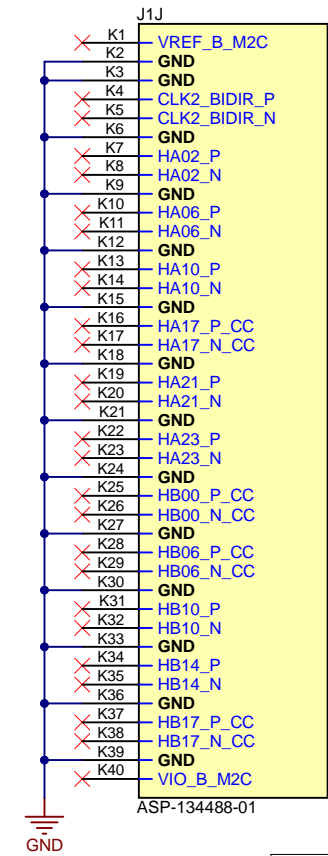
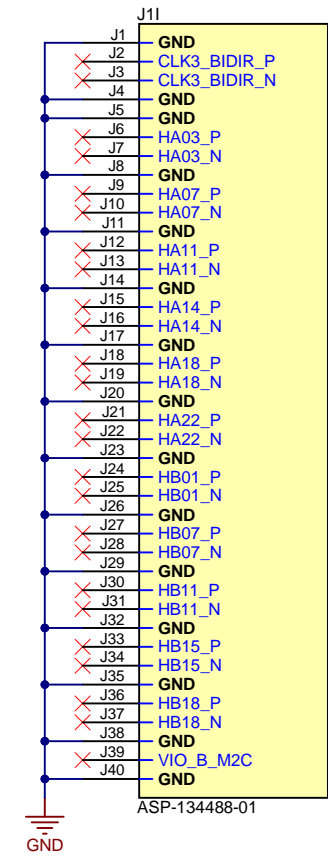
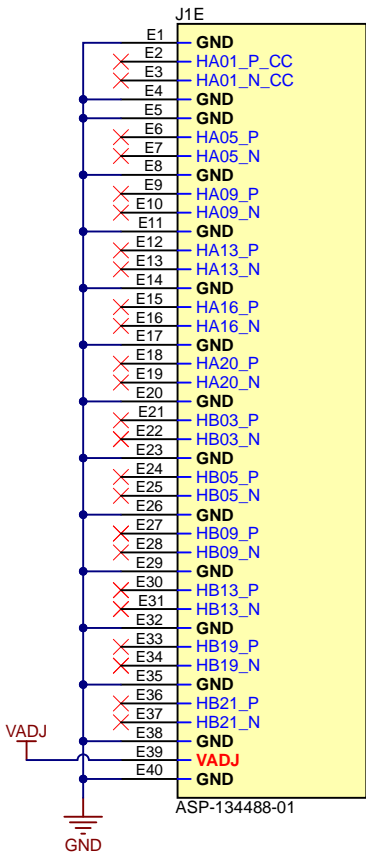
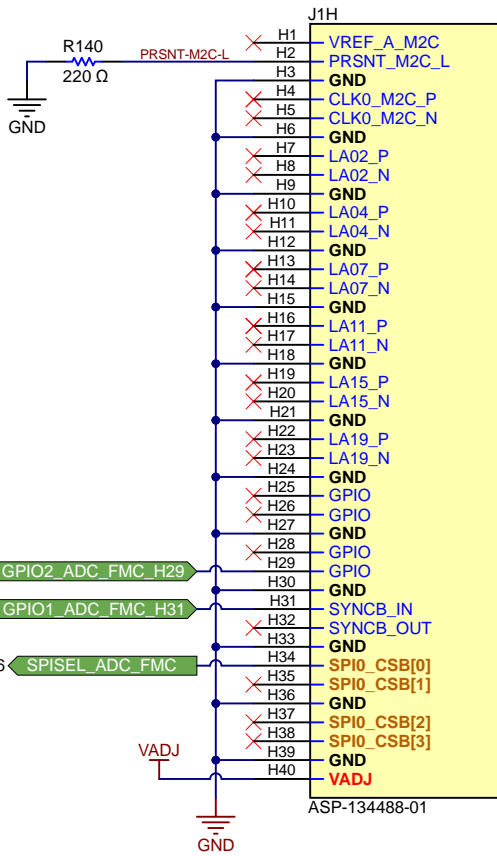
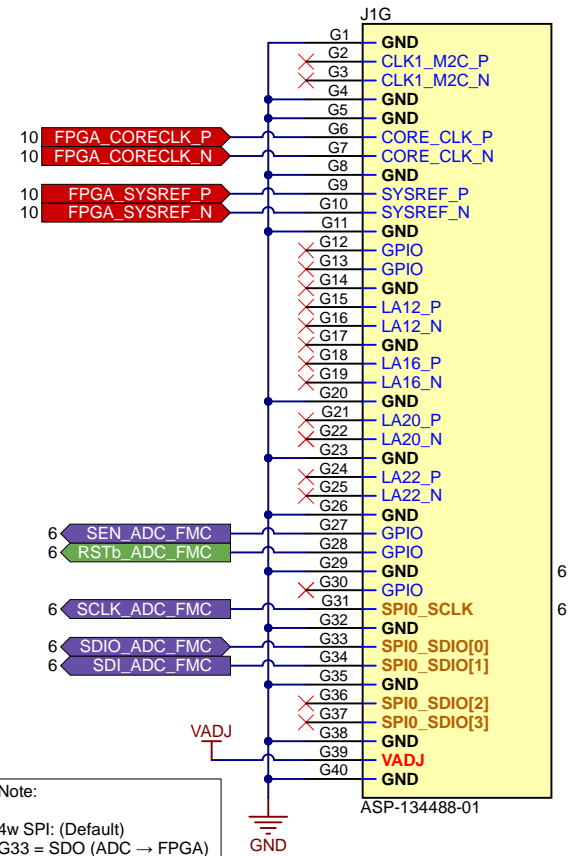
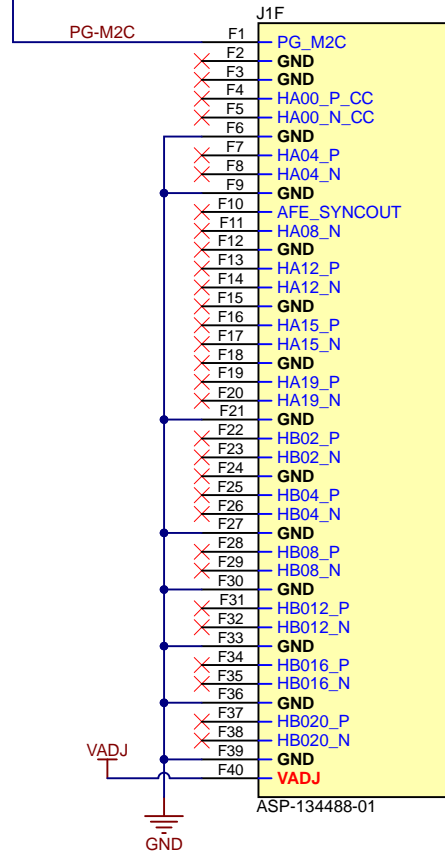
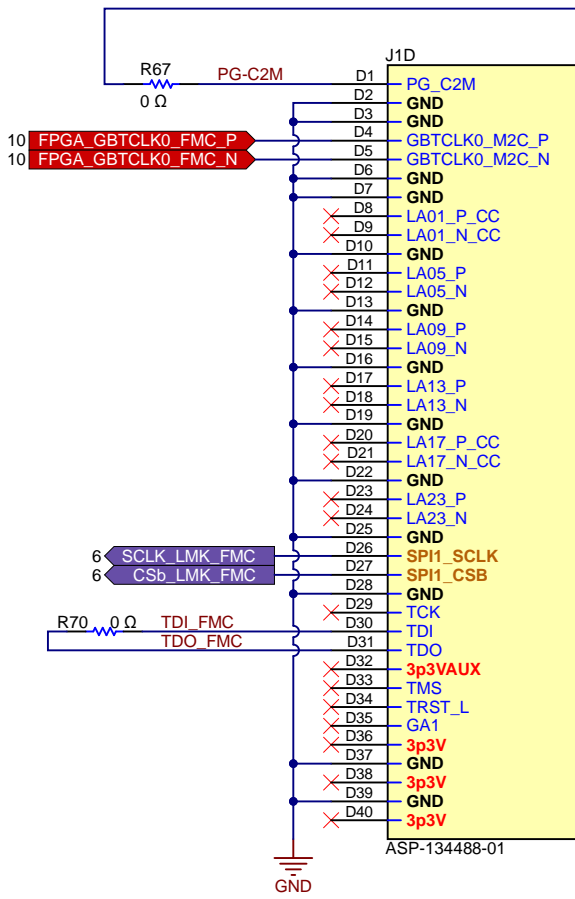
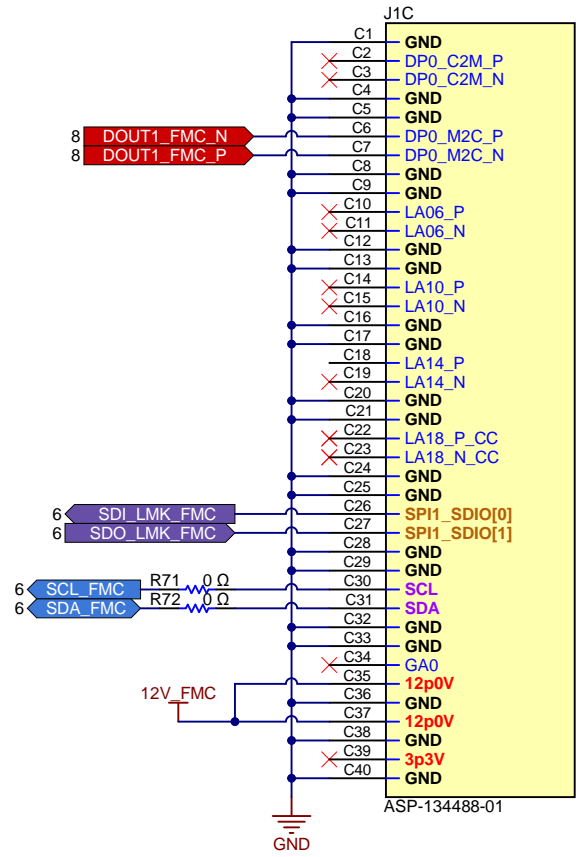
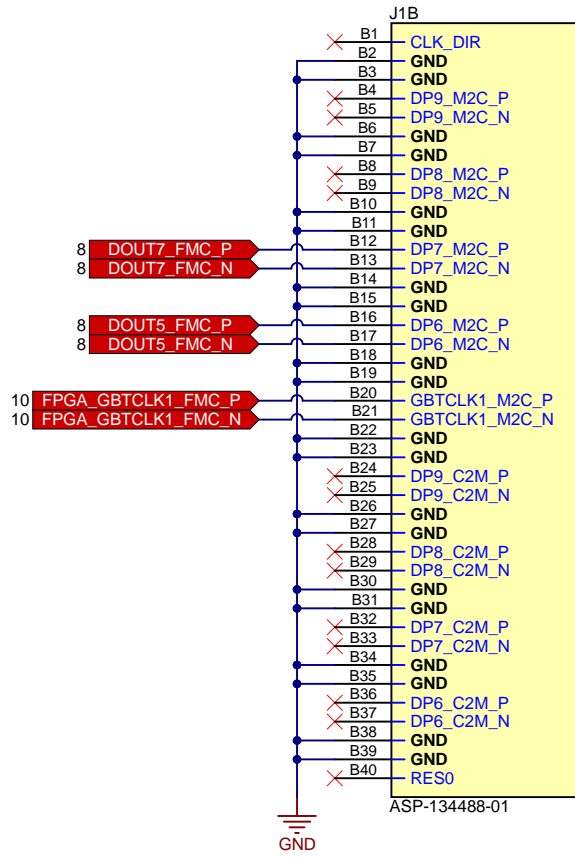
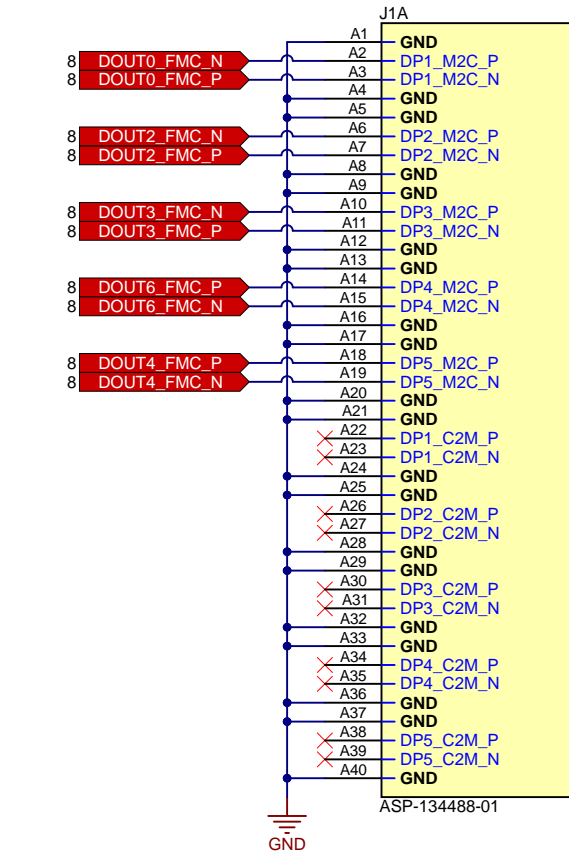
D

A

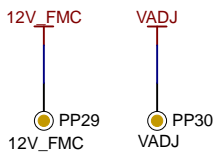
B

C

D



FMC Lane Mapping			
ADC Lane #	FMC Lane #	FMC Pin (+)	Inverted Polarity?
7	7	B12	No
4	6	A14	No
6	5	B16	No
5	4	A18	No
3	3	A11	Yes
2	2	A7	Yes
0	1	C7	Yes
1	0	A3	Yes



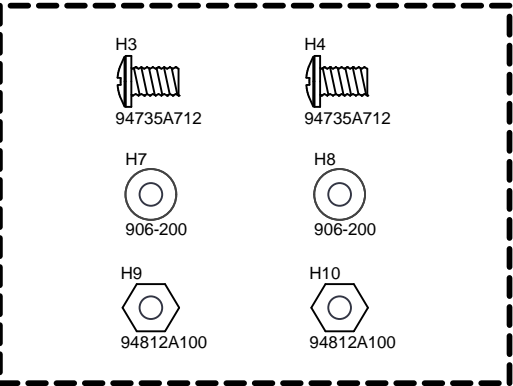
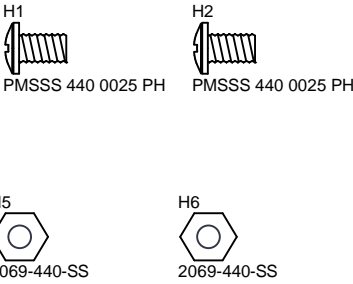
Note:

4w SPI: (Default)  
G33 = SDO (ADC → FPGA)  
G34 = SDI (FPGA → ADC)

3w SPI: Must DNI R60  
G33 = SDIO (ADC ↔ FPGA)  
G34 = Don't Care

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FTDI Dongle Hardware

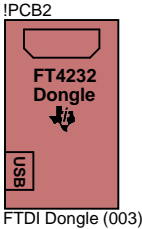


PCB Number: DC142D  
PCB Rev: D1



PCB  
LOGO  
FCC disclaimer

Cannot  
open file  
C:\Users\  
a0864280



LBL1  
PCB Label  
THT-14-423-10  
Size: 0.65"x0.20"

ZZ1  
Label Assembly Note  
This Assembly Note is for PCB labels only. PLACE ON TOP OF BOARD.

ZZ2  
Assembly Note  
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3  
Assembly Note  
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.


ZZ4  
Assembly Note  
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Variant/Label Table	
Variant	Label Text
001	ADC32RF55

1		2		3		4		5		6	
Rev History & Variants											
A	Revision History										
	Rev	Release Date	Notes								
	A	DD-MMM-YYYY	Initial Release								
	B	DD-MMM-YYYY	• GPIO correction • Header change • CLK divider								
	C	04-June-2021	• Updated Inputs to single SMA split to 2 ADC inputs • Added OSC as secondary CLK input option • Fixed issue where LMK was not routed to CLK input as third clock option								
D	01-April-2024	• Updated input split network to improve bandwidth • Removed onboard oscillator • Removed LMK routing to CLK input • Updated power tree • DVDD now on 6A rail to account for 3GSPS bypass, 4x avg • Updated current monitor addresses to avoid using SDA in address									
B	Variant(s)										
	Variant	Notes									
	001	• Original DNI components • Used for production build									
C											
D											

Orderable: <a href="#">ADC32RF55EVM</a>		Designed for: <a href="#">Not For Public Release</a>		Mod. Date: 5/16/2024	
TID #: <a href="#">N/A</a>		Project Title: <a href="#">ADC32RF55EVM</a>			
Number: <a href="#">DC142D</a>		Rev: <a href="#">D1</a>		Sheet Title: <a href="#">Rev History &amp; Variants</a>	
SVN Rev:		Assembly Variant: <a href="#">-001</a>		Sheet: <a href="#">13</a> of <a href="#">13</a>	
Drawn By: <a href="#">CW</a>		File: <a href="#">DC142D_ADC32RF55_Revision History.SchDoc</a>			
Engineer: <a href="#">CW</a>		Contact: <a href="#">http://www.ti.com/support</a>			

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1	2	3	4	5	6
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