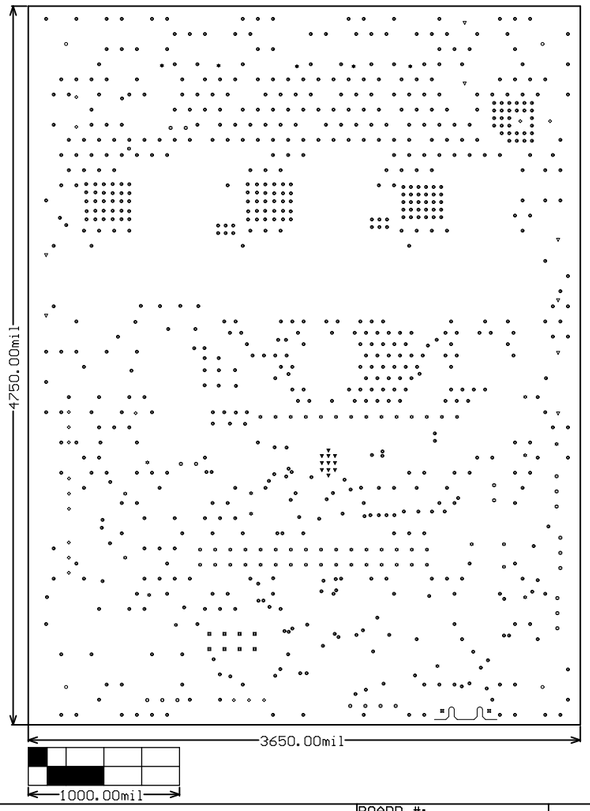
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer	Copper	2.80mil		
	Dielectric 2	FR-4	10.00mil	4.8	
2	GND Layer	Copper	1.40mil		
	Dielectric 1	FR-4	32.80mil	4.2	
3	Power Layer	Copper	1.40mil		
	Dielectric 3	FR-4	10.00mil	4.8	
4	Bottom Layer	Copper	2.80mil		
	Solder Side	Solder Resist	0.40mil	3.5	
	Bottom Overlay				



Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
▽	11	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	
⊙	754	10.00mil (0.254mm)	PTH	Round	Top Layer - Bottom Layer	
◇	17	33.47mil (0.850mm)	PTH	Round	Top Layer - Bottom Layer	
✡	62	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	
◘	8	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer	
✪	22	45.28mil (1.150mm)	PTH	Round	Top Layer - Bottom Layer	
▽	8	51.18mil (1.300mm)	PTH	Round	Top Layer - Bottom Layer	
✽	5	59.06mil (1.500mm)	PTH	Round	Top Layer - Bottom Layer	
○	4	125.98mil (3.200mm)	PTH	Round	Top Layer - Bottom Layer	
⊠	2	23.62mil (0.600mm)	PTH	Slot	Top Layer - Bottom Layer	
	893 Total					

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 30 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER_____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: MCF8329HS_32RRY_EVM
DESIGNED FOR: Public Release
FILE NAME: MCF8329HS 32RRY EVM.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: MCF8329HS_32RRY_EVM	REV: A	SVN REV: Not In VersionControl
LAYER NAME = [illegible]ions	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 25-09-2025 14:23:11		TEXAS INSTRUMENTS

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ENGINEER:	LAYOUT BY:
Venkatadri	Krypton solutions
SCALE: 1.00	ALTIUM DESIGNER VERSION: 19.1.8.144