

The Stackup Legend below this is static.  
If you change the stackup, update the Legend.

Layer Stack Up Detail for: Ref_Design.PcbDoc			
Layer	Material	Copper Thickness	Dielectric Material
Top Solder Mask	C.BTS		Solder Resist
Top Layer	C.BTL>	1.4mil	FR-4
Bottom Layer	C.BBL>	1.4mil	
Bottom Solder Mask	C.BBS		Solder Resist

DESIGN INFORMATION

BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)  
3450MIL X 4950MIL

Number of Layers : 2  
MIN. TRACK WIDTH: 8 MIL  
MIN. CLEARANCE: 8 MIL  
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL  
PER IPC-D-275 CLASS 2 LEVEL C  
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL:  
☐ FR-4 ☒ FR-4 High Tg ☐ OTHER

THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2  
☐ OTHER +/-

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2  
☐ OTHER +/-

COPPER THICKNESS (FINISHED):  
OUTER: ☒ 1.4MIL (1oz) ☐ 2MIL (1.4oz) ☐ 2.8MIL (2oz)  
INNER SIGNAL: ☒ 1.4MIL (1oz) ☐ 2.8MIL (2oz)

DRILLING:  
REFERENCE: ☒ AS SHOWN ☒ NC\_DRILL FILES  
PTH MIN COPPER THICKNESS: ☒ 1MIL ☐ OTHER

BOARD FINISH:  
SILKSCREEN: ☒ TOP ☒ BOTTOM  
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER

SOLDER RESIST COLOR:  
☒ GREEN ☐ BLUE ☐ OTHER

SURFACE FINISH: ☒ IMMERSION GOLD (ENG) ☐ Pb-FREE HASL  
☐ OTHER

ARRAY/PANEL:  
☐ CUT AND TRIM PER MECH LAYER 1  
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3  
☒ UL 94V-0 ☒ RoHS ☐ OTHER PER ORDER

ADDITIONAL REQUIREMENTS:  
MICROSECTION: ☐ YES

BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

MANUFACTURER'S D/LOGO: ☐ RAIL ☒ METAL ☐ SILK



PROJECT TITLE:  
Change me in menu Project/Project Options/Parameters

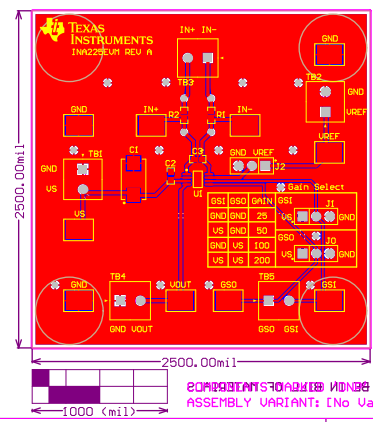
FILE NAME:  
INA225.PcbDoc

FAB DRAWING NUMBER:  
551xxxxxx-001 REV A

DESIGNED FOR:  
Public Release

SCALE: 1.00

ALTIM DESIGNER VERSION:  
10.0.0.24352



A

B

C

D

A

B

C

D

PCB FABRICATOR: TTI PCB FAB		PROJECT NAME: INA225		Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.	
LAYER 1 MATERIAL: FR-4		LAYER 2 MATERIAL: FR-4		REV A	
PRINT NAME: MuEDA-PCB Composer		DESIGNED FOR: Public Release		SCALE: 1.00	
1		2		3	
4		5		6	