

1

2

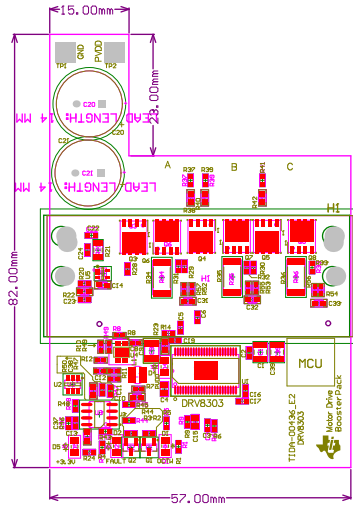
3

4

5

6

Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z22 ■ These assemblies are ESD sensitive. ESD precautions shall be observed.



COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED. TO ORDER, REMOVE 'DNP' FROM PART NUMBER.
ASSEMBLY VARIANT: [No Variations]

ALL INFORMATION HEREON IS UNCLASSIFIED	DATE: 10/10/2013	BY: [Redacted]	REVIEWED BY: [Redacted]	DATE: 10/10/2013	BY: [Redacted]	DATE: 10/10/2013	BY: [Redacted]	DATE: 10/10/2013	BY: [Redacted]
LAYER NAME: ASSEMBLY	DATE: 10/10/2013	BY: [Redacted]	REVIEWED BY: [Redacted]	DATE: 10/10/2013	BY: [Redacted]	DATE: 10/10/2013	BY: [Redacted]	DATE: 10/10/2013	BY: [Redacted]
PLATTINUM	DATE: 10/10/2013	BY: [Redacted]	REVIEWED BY: [Redacted]	DATE: 10/10/2013	BY: [Redacted]	DATE: 10/10/2013	BY: [Redacted]	DATE: 10/10/2013	BY: [Redacted]

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Layer Stack Up Detail for TIDA-00436.PcbDoc			
Layer	Material	Copper Thickness	Solder Resist
Top Solder Mask	(.675)		
Top Layer	(.675)	2.8mil	FR-4
Prepreg	(.675)	2.8mil	FR-4
Core	(.675)	2.8mil	FR-4
Bottom Layer	(.675)	2.8mil	FR-4
Bottom Solder Mask	(.675)		Solder Resist

DESIGN INFORMATION

BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)
2244.09MIL X 3228.34MIL
Number of Layers: 4
MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
It is not an impedance controlled board.
MINIMUM ANNUAL RING 0.127mm (5MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL:
☒ FR-408 ☐ FR-4 High Tg ☐ OTHER
THICKNESS: ☒ 63 MIL (1.6mm) +/-10% ☐ OTHER
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

COPPER THICKNESS (FINISHED):
OUTER: ☐ 1.4MIL (1oz) ☐ 2MIL (1.4oz) ☒ 2.8MIL (2oz)
INNER SIGNAL: ☐ 1.4MIL (1oz) ☒ 2.8MIL (2oz) ☐ N/A

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC DRILL FILES
PTH MIN COPPER THICKNESS: ☒ 1MIL ☐ OTHER

BOARD FINISH:
SLKSCREEN: ☒ TOP ☒ BOTTOM
SLKSCREEN COLOR: ☒ WHITE ☐ OTHER
SOLDER RESIST COLOR:
☒ GREEN ☐ BLUE ☐ OTHER

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER

ARRAY/PANEL: ☐ CUT AND TRIM PER MECH LAYER 1
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS 2 -> ☐ 1 ☒ 2 ☐ 3
☒ UL 94V-0 ☒ RoHS ☐ OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES ☒ NO
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
MANUFACTURER'S UL: ☐ RAL ☐ METAL ☒ SILK



PROJECT TITLE:
TIDA-00436_E2

DESIGNED FOR:

FILE NAME:
TIDA-00436.PcbDoc

ENGINEER: Nelson	LAYOUT BY:
SCALE: 1.00	ALTIM DESIGNER VERSION: 10.0.0.27009

1

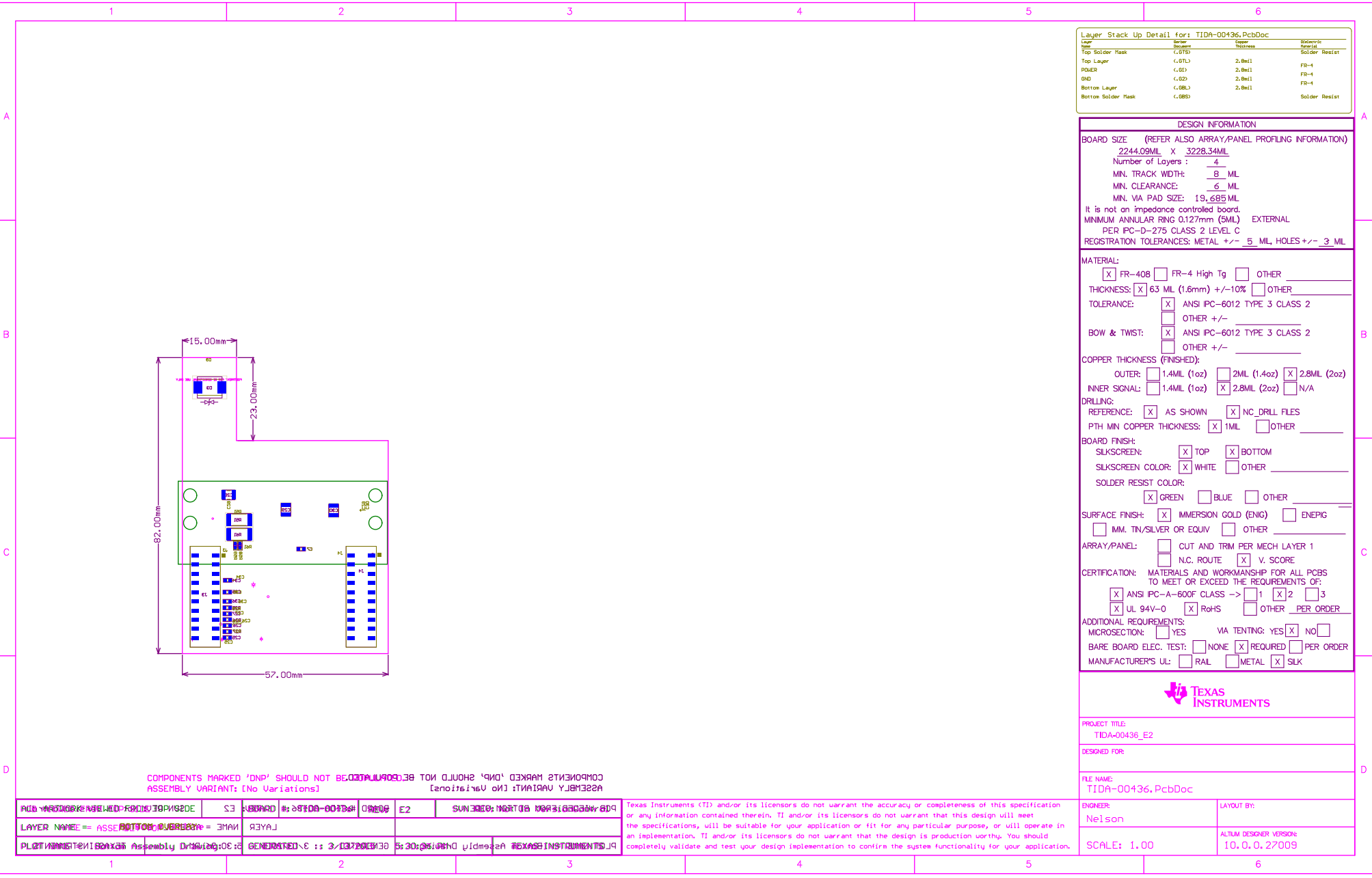
2

3

4

5

6



Layer Stack Up Detail for TIDA-00436.PcbDoc			
Layer Name	Dielectric Material	Copper Thickness	Solder Resist
Top Solder Mask	(.ST5)		
Top Layer	(.BT1)	2.8mil	FR-4
Prepreg	(.BT1)	2.8mil	FR-4
Core	(.BT1)	2.8mil	FR-4
Bottom Layer	(.BT1)	2.8mil	FR-4
Bottom Solder Mask	(.ST5)		Solder Resist

DESIGN INFORMATION

BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)
2244.09MIL X 3228.34MIL
Number of Layers : 4
MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.695 MIL
It is not an impedance controlled board.
MINIMUM ANNUAL RING 0.127mm (5MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL:
☒ FR-408 ☐ FR-4 High Tg ☐ OTHER
THICKNESS: ☒ 63 MIL (1.6mm) +/-10% ☐ OTHER
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

COPPER THICKNESS (FINISHED):
OUTER: ☐ 1.4MIL (1oz) ☐ 2MIL (1.4oz) ☒ 2.8MIL (2oz)
INNER SIGNAL: ☐ 1.4MIL (1oz) ☒ 2.8MIL (2oz) ☐ N/A

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH MIN COPPER THICKNESS: ☒ 1MIL ☐ OTHER

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER
SOLDER RESIST COLOR:
☒ GREEN ☐ BLUE ☐ OTHER

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER

ARRAY/PANEL: ☐ CUT AND TRIM PER MECH LAYER 1
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ UL 94V-0 ☒ RoHS ☐ OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES VIA TENCING: YES ☒ NO
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
MANUFACTURER'S UL: ☐ RAL ☐ METAL ☒ SILK



PROJECT TITLE:
TIDA-00436_E2

DESIGNED FOR:

FILE NAME:
TIDA-00436.PcbDoc

ALL INFORMATION CONTAINED HEREIN IS UNCLASSIFIED EXCEPT WHERE SHOWN OTHERWISE	DATE: 3/13/2013	BY: [REDACTED]
LAYER NAME = ASSEMBLY OVERLAY	DATE: 3/13/2013	BY: [REDACTED]
PLATTINUM DESIGN Assembly Division	DATE: 3/13/2013	BY: [REDACTED]

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER: Nelson	LAYOUT BY:
SCALE: 1.00	ALTIM DESIGNER VERSION: 10.0.0.27009