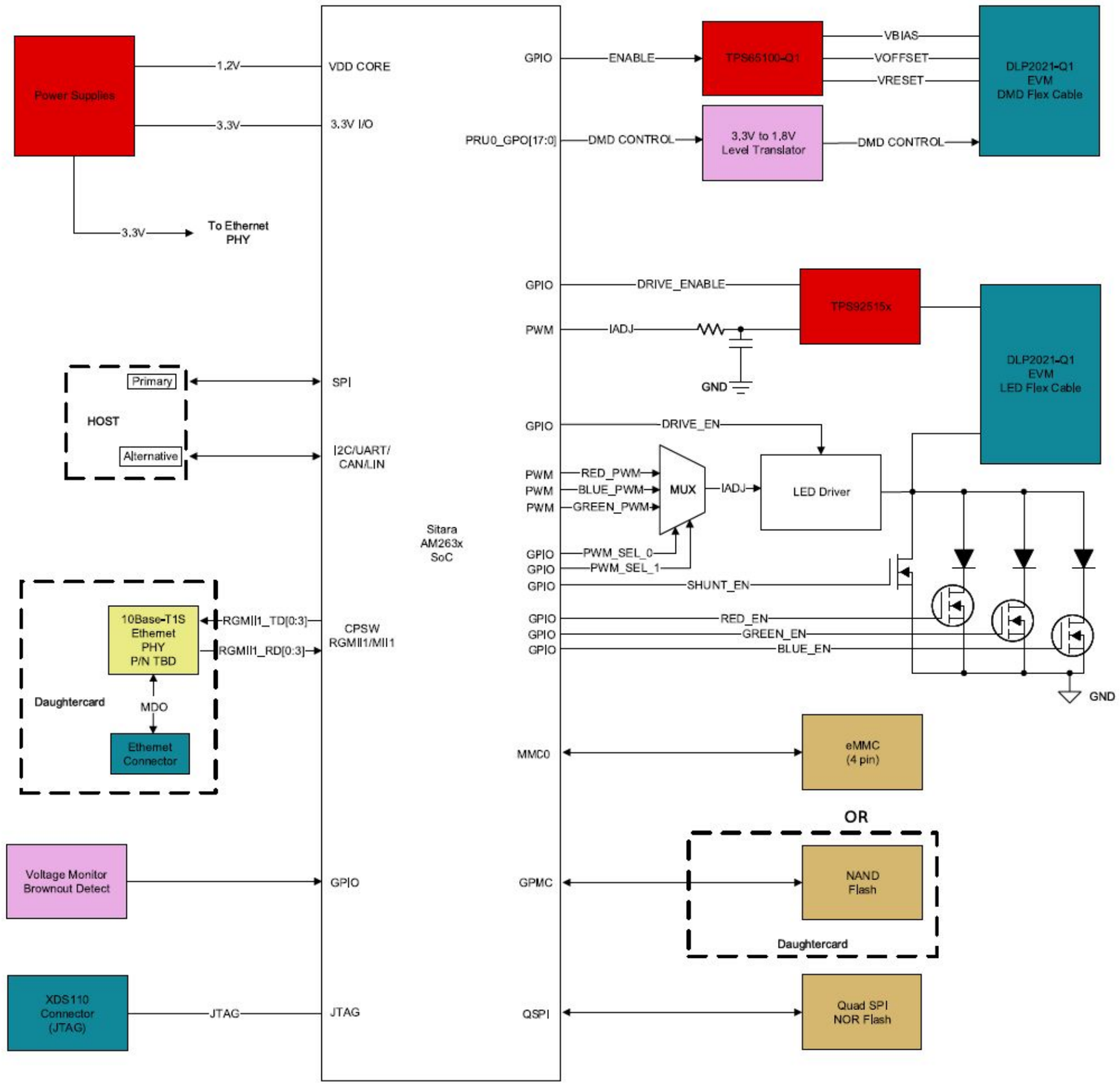

Orderable: DLP2021AM263Q1EVM		Designed for: Public Release	Mod. Date: 5/1/2024
TID #: N/A		Project Title: DLP2021AM263Q1EVM	
Number: DLP096	Rev: B	Sheet Title: Block Diagram	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 1 of 10
Drawn By: A. Whitehead		File: DLP096B_Block_Diagram.SchDoc	Size: B
Engineer: A. Whitehead		Contact: http://www.ti.com/support	

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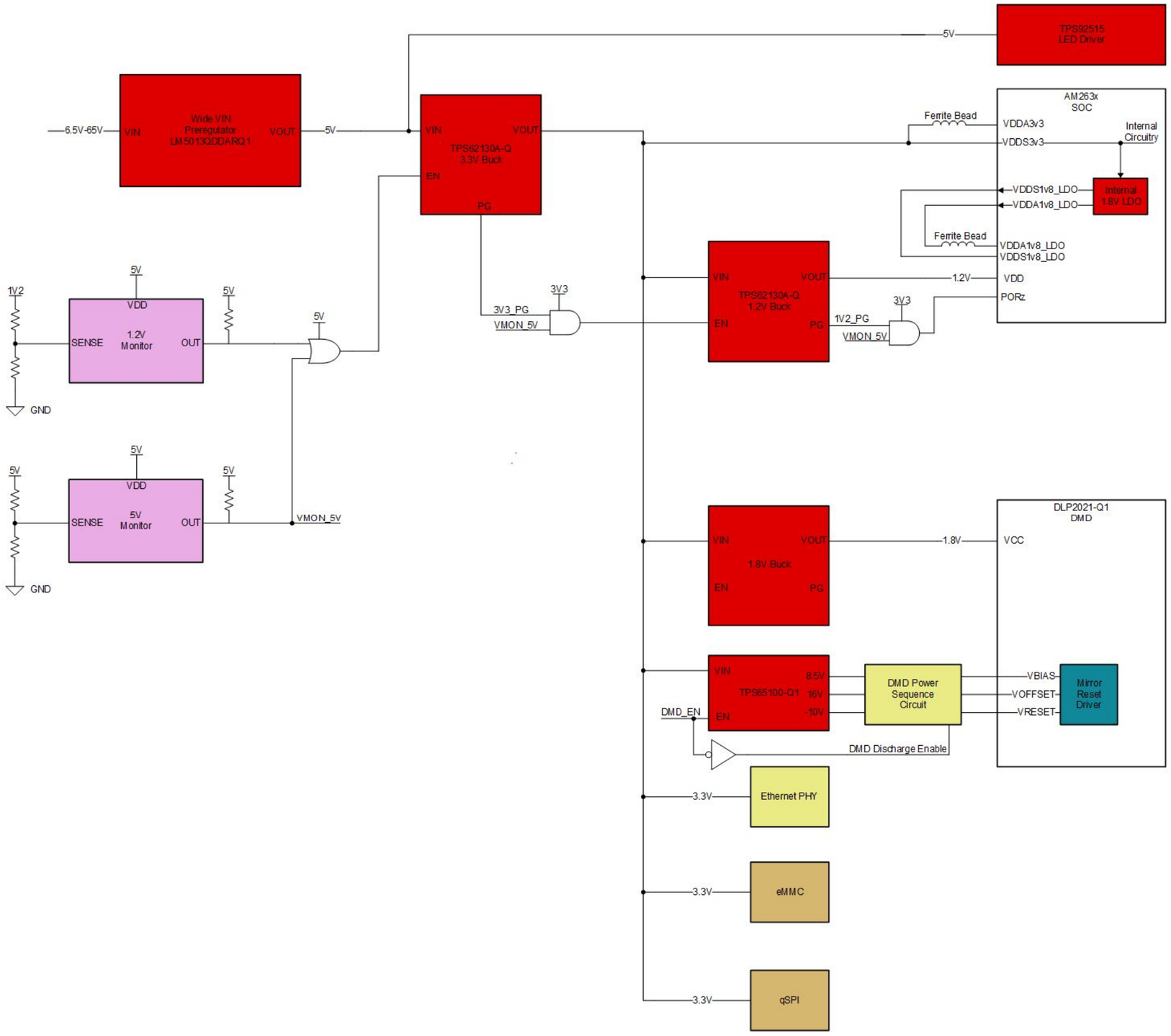
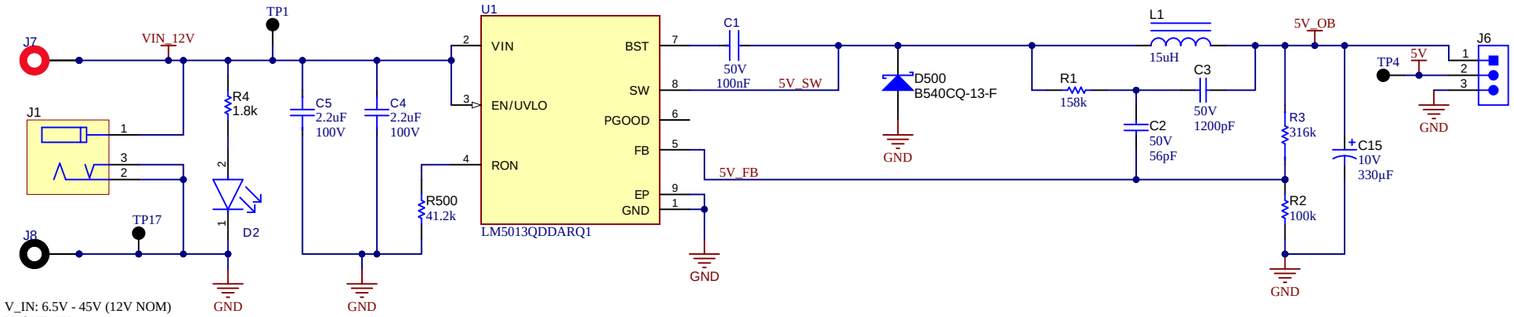


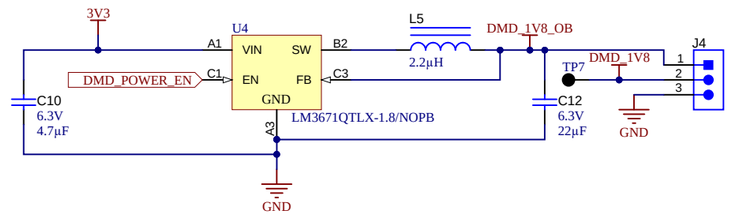
Orderable: DLP2021AM263Q1EVM	Designed for: Public Release	Mod. Date: 5/1/2024
TID #: N/A	Project Title: DLP2021AM263Q1EVM	
Number: DLP096 Rev: B	Sheet Title: Power Tree	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 2 of 10
Drawn By: A. Whitehead	File: DLP096B_Power_Tree.SchDoc	Size: B
Engineer: A. Whitehead	Contact: http://www.ti.com/support	

TEXAS INSTRUMENTS
http://www.ti.com



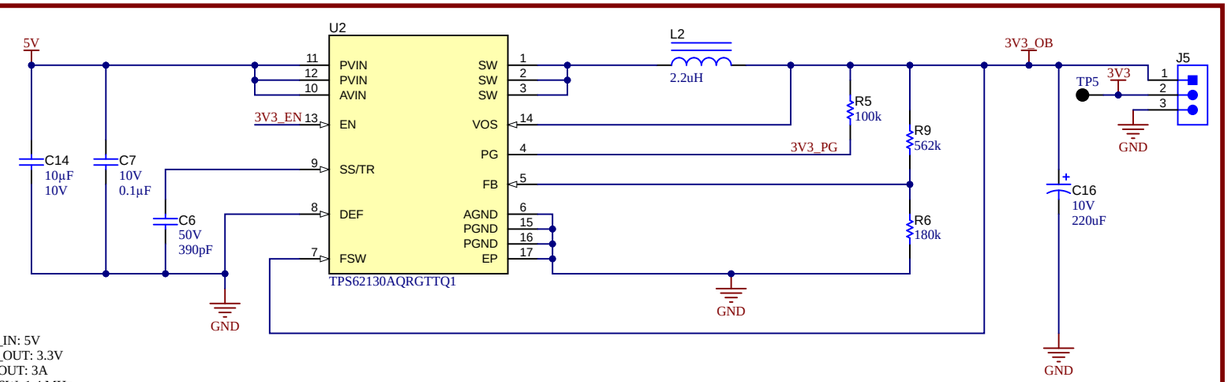
V_IN: 6.5V - 45V (12V NOM)
V_OUT: 5V
I_OUT: 3A
f_SW: 274.82 kHz
V_OUT Ripple: 61.03mV

Pre-regulator: 6.5V to 45V IN



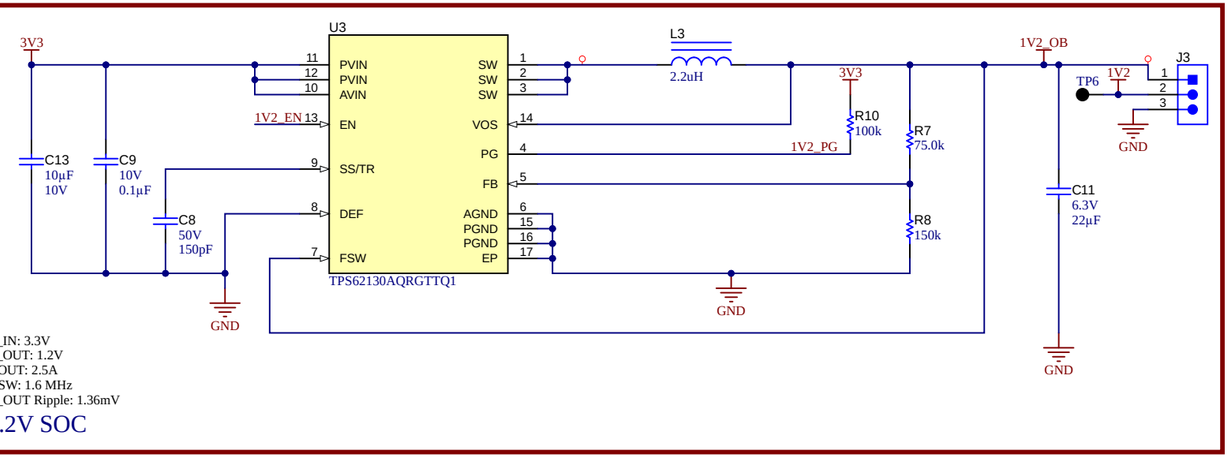
V_IN: 3.3V
V_OUT: 1.8V
I_OUT: 0.2A
f_SW: 2 MHz
V_OUT Ripple: 909uV

1.8V DMD



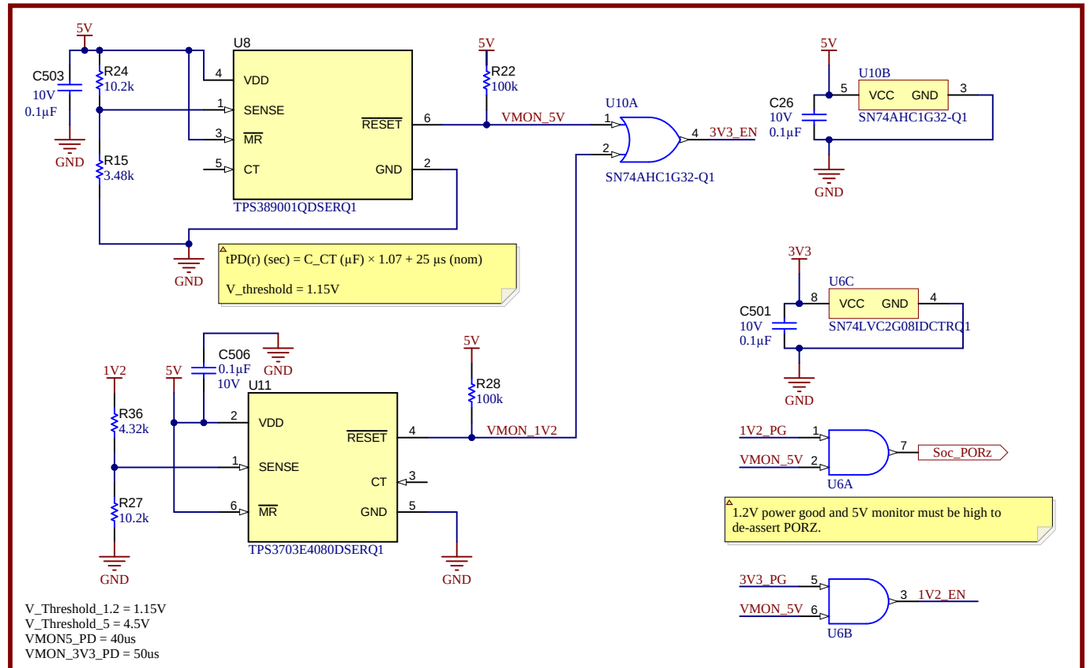
V_IN: 5V
V_OUT: 3.3V
I_OUT: 3A
f_SW: 1.4 MHz
V_OUT Ripple: 4.86mV

3.3V System



V_IN: 3.3V
V_OUT: 1.2V
I_OUT: 2.5A
f_SW: 1.6 MHz
V_OUT Ripple: 1.36mV

1.2V SOC

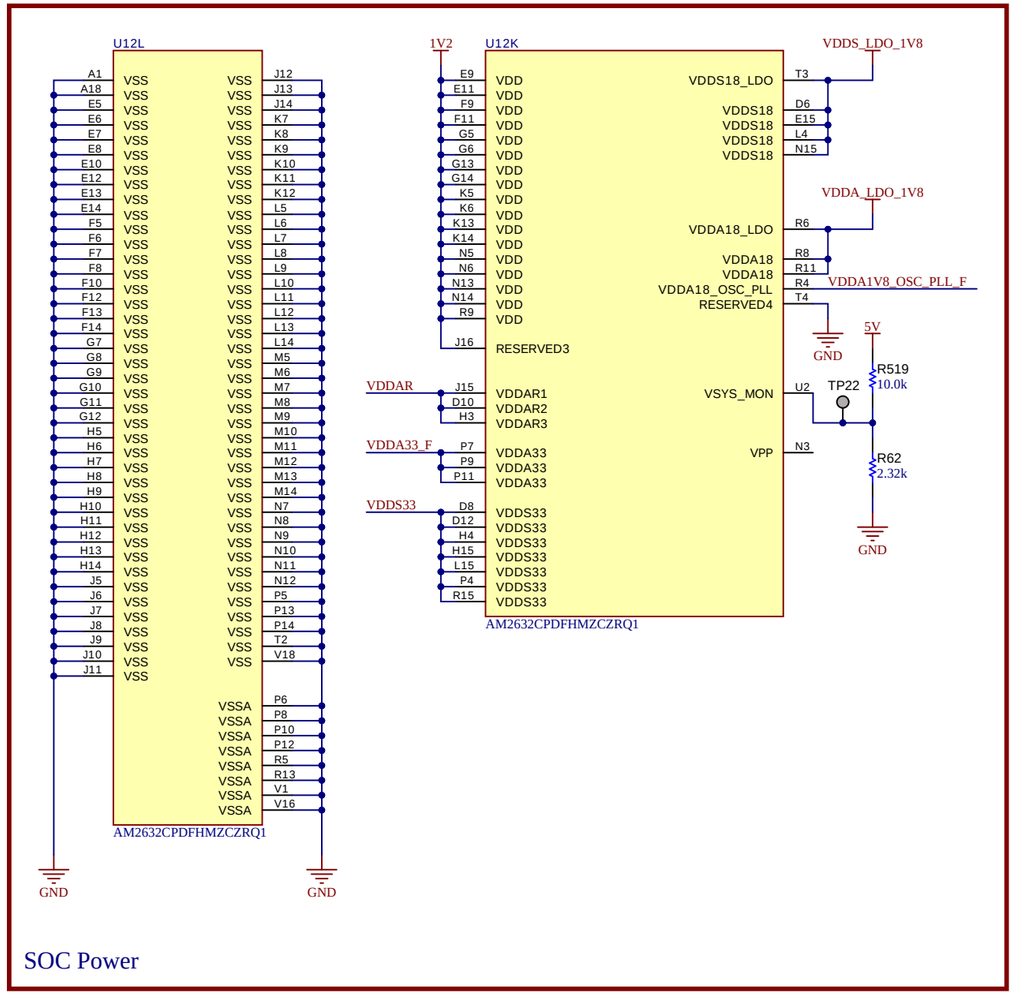


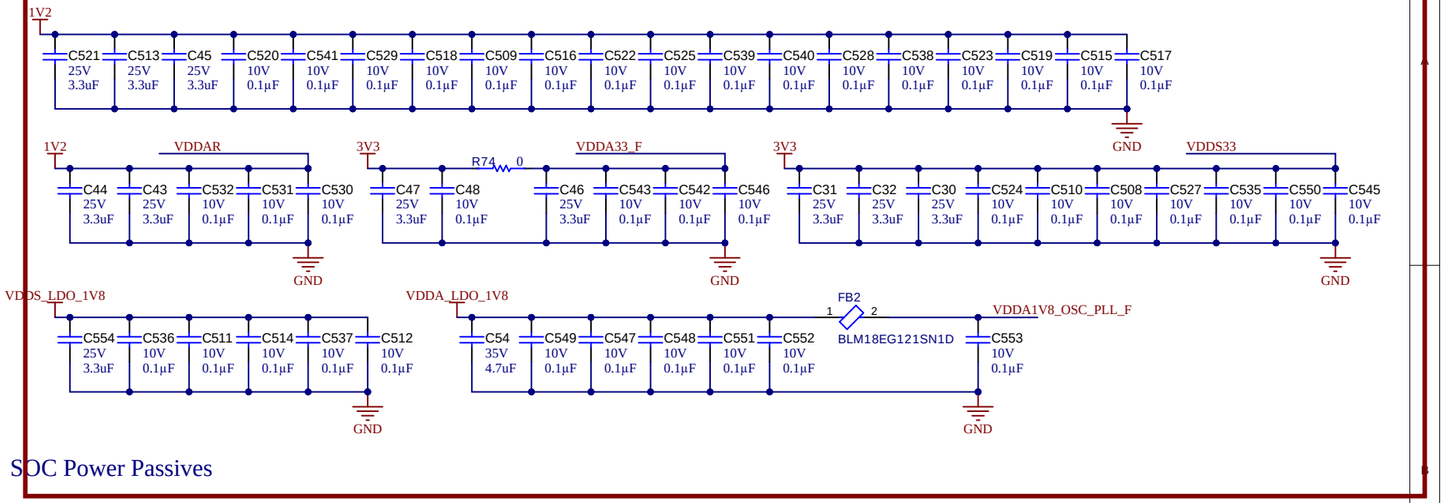
V_Threshold_1.2 = 1.15V
V_Threshold_5 = 4.5V
VMON5_PD = 40us
VMON_3V3_PD = 50us

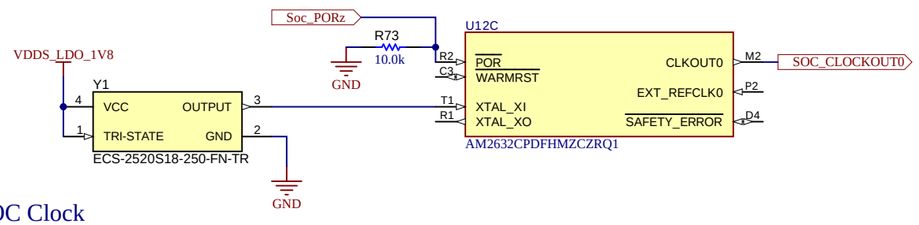
Power Sequencing

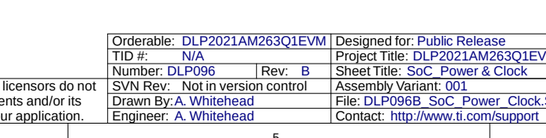
Orderable: DLP2021AM263Q1EVM		Designed for: Public Release	Mod. Date: 5/1/2024
TID #: N/A		Project Title: DLP2021AM263Q1EVM	
Number: DLP096	Rev: B	Sheet Title: System_Power	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 3 of 10
Drawn By: A. Whitehead		File: DLP096B_System_Power.SchDoc	Size: B
Engineer: A. Whitehead		Contact: http://www.ti.com/support	

TEXAS INSTRUMENTS
http://www.ti.com









Orderable: DLP2021AM263Q1EVM		Designed for: Public Release	Mod. Date: 5/1/2024
TID #: N/A		Project Title: DLP2021AM263Q1EVM	
Number: DLP096	Rev: B	Sheet Title: SoC_Power & Clock	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 4 of 10
Drawn By: A. Whitehead		File: DLP096B_SoC_Power_Clock.SchDoc	Size: B
Engineer: A. Whitehead		Contact: http://www.ti.com/support	

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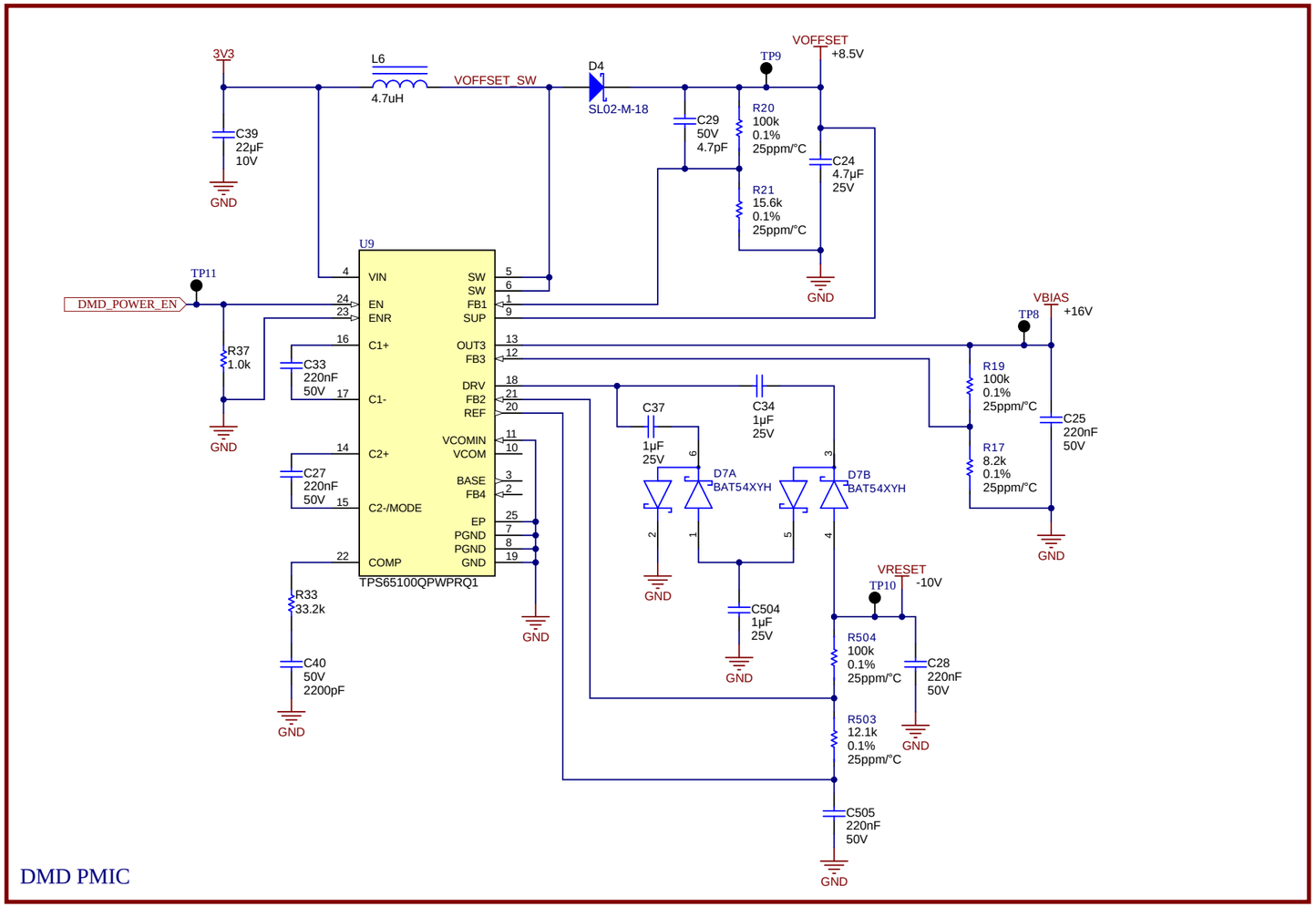
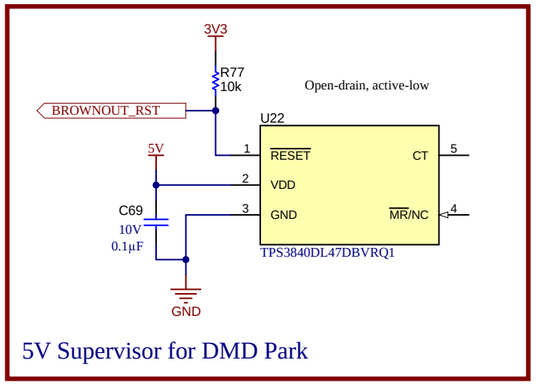
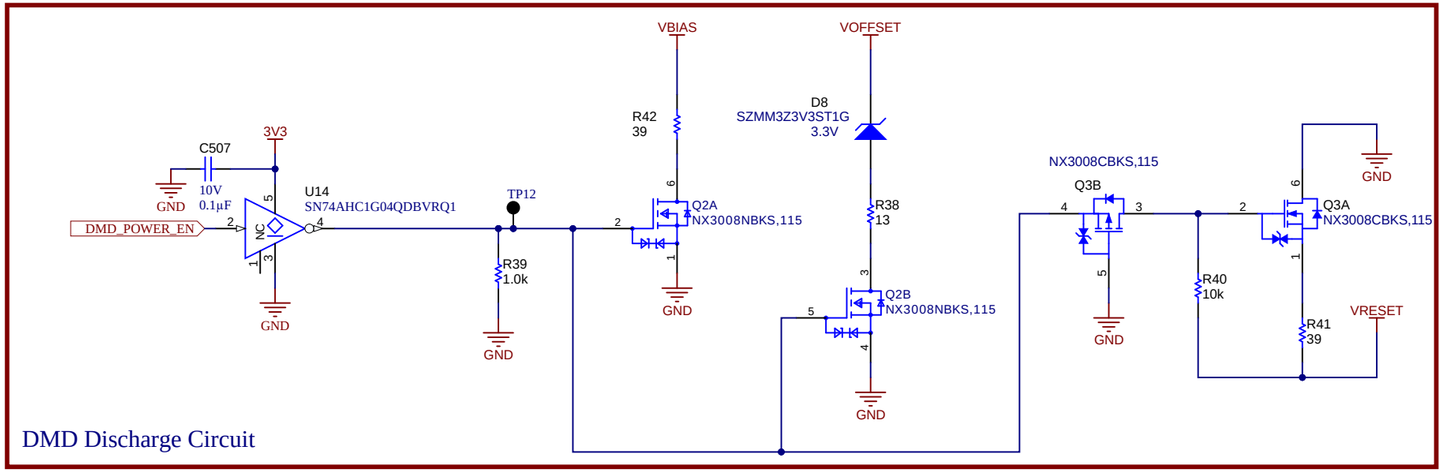


DMD PMIC



5V Supervisor for DMD Park



DMD Discharge Circuit

Orderable: DLP2021AM263Q1EVM		Designed for: Public Release	Mod. Date: 5/1/2024
TID #: N/A		Project Title: DLP2021AM263Q1EVM	
Number: DLP096	Rev: B	Sheet Title: DMD Power	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 5 of 10
Drawn By: A. Whitehead		File: DLP096B_DMD_Power.SchDoc	Size: B
Engineer: A. Whitehead		Contact: http://www.ti.com/support	

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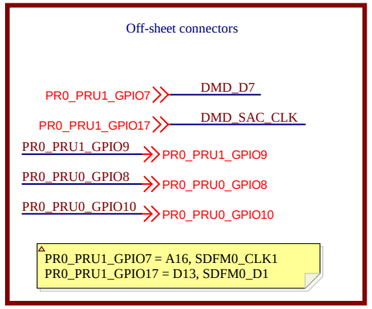
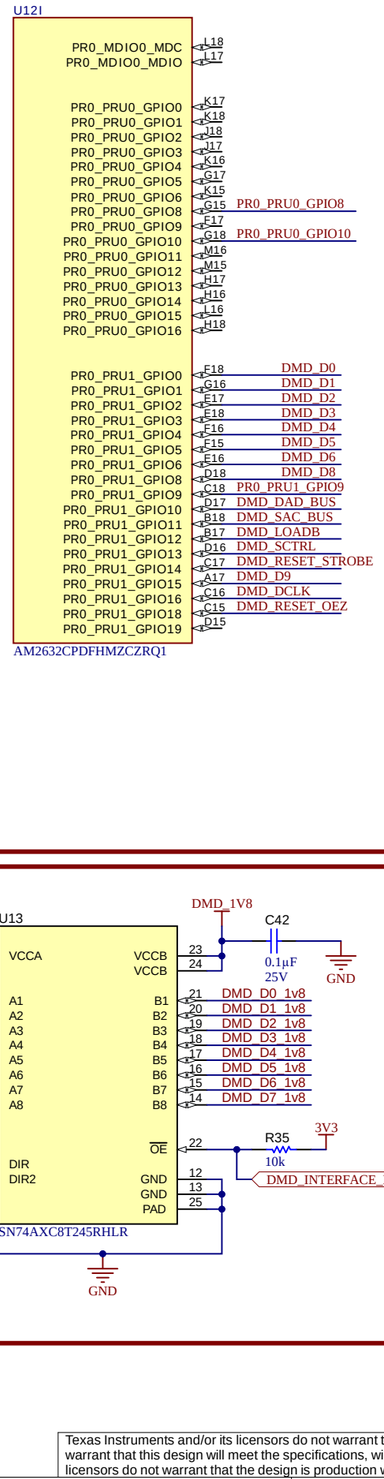
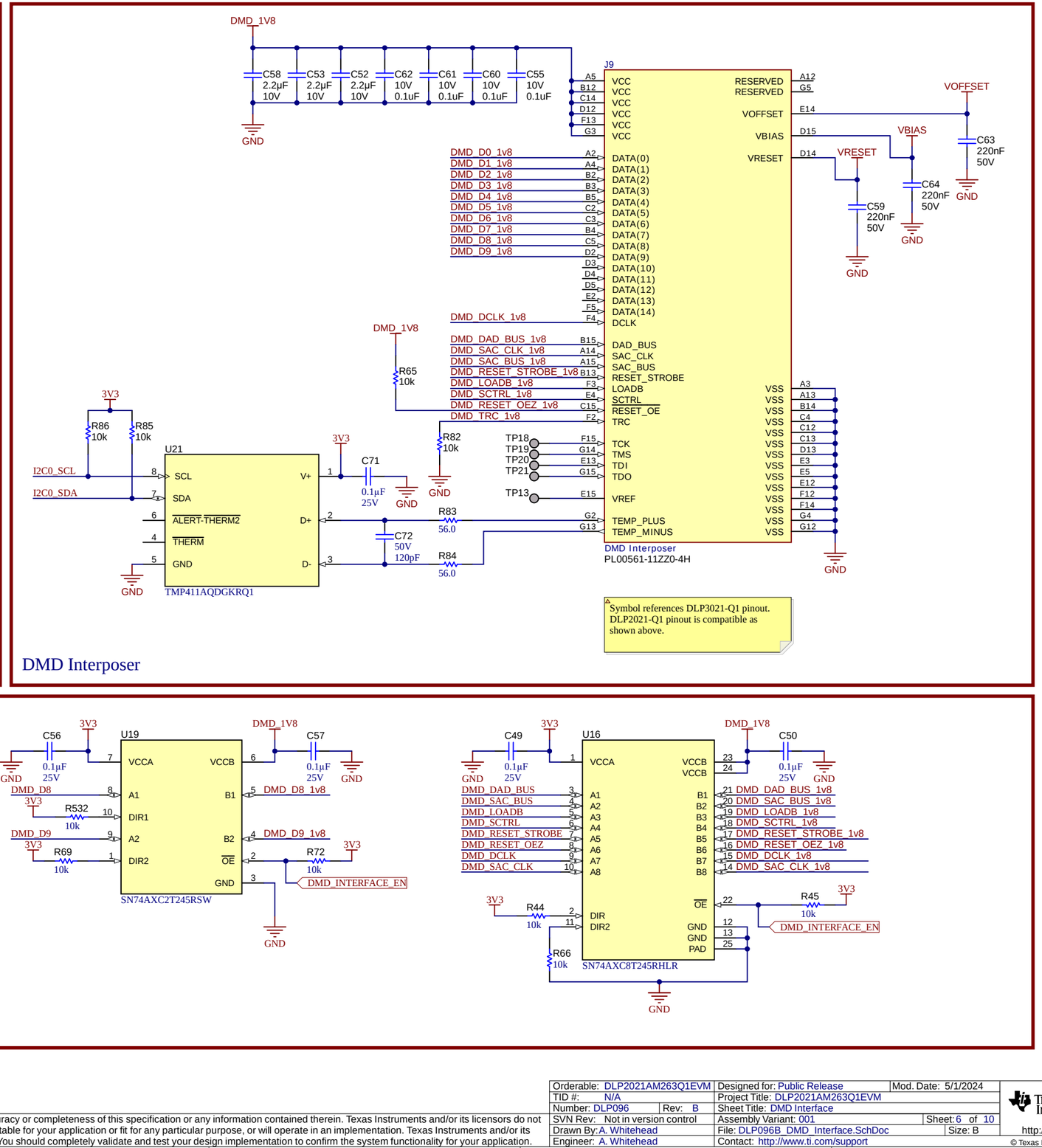




SOC PRU



DMD Interposer

PRU-to-DMD Level Shifters

Orderable: DLP2021AM263Q1EVM	Designed for: Public Release	Mod. Date: 5/1/2024	
TID #: N/A	Project Title: DLP2021AM263Q1EVM		
Number: DLP096 Rev: B	Sheet Title: DMD Interface		
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 6 of 10	
Drawn By: A. Whitehead	File: DLP096B_DMD_Interface.SchDoc	Size: B	
Engineer: A. Whitehead	Contact: http://www.ti.com/support		

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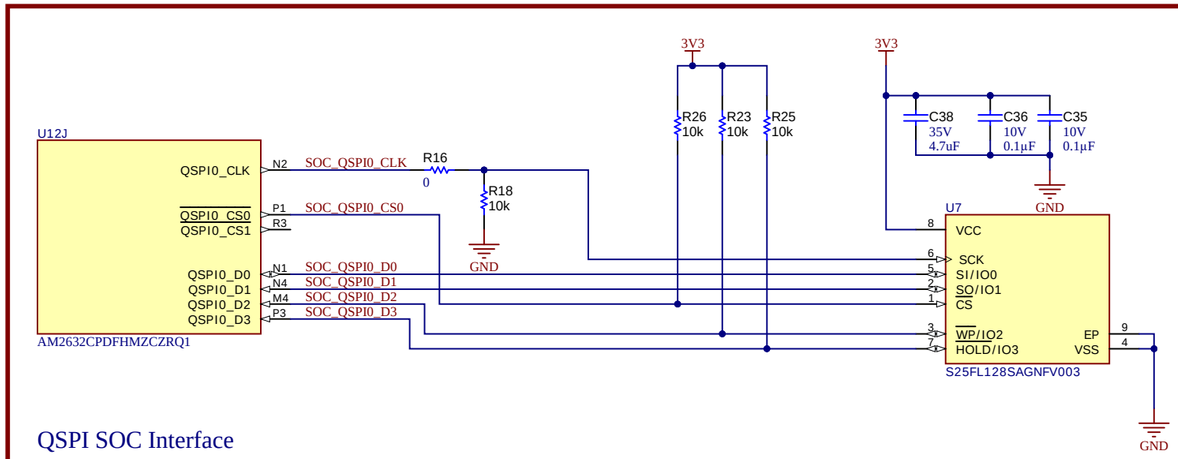


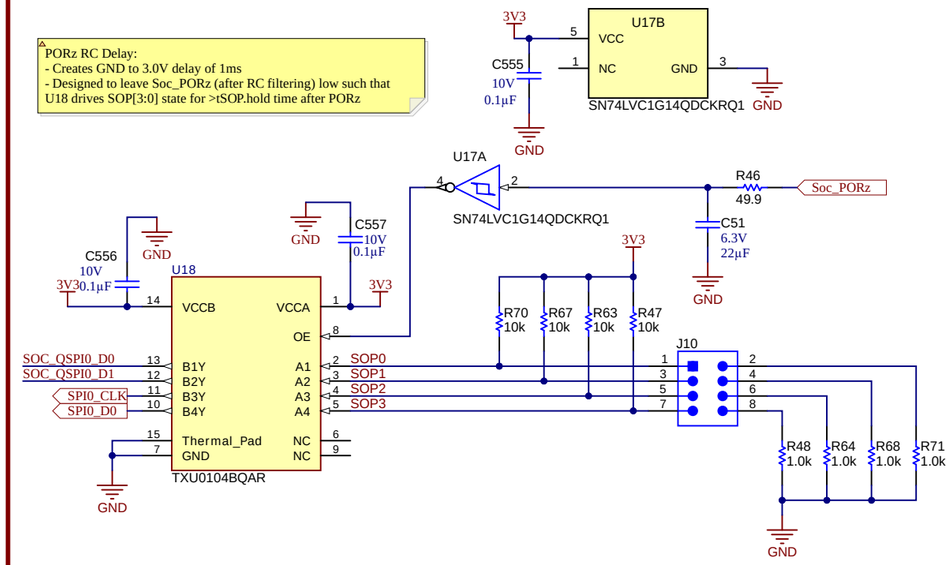
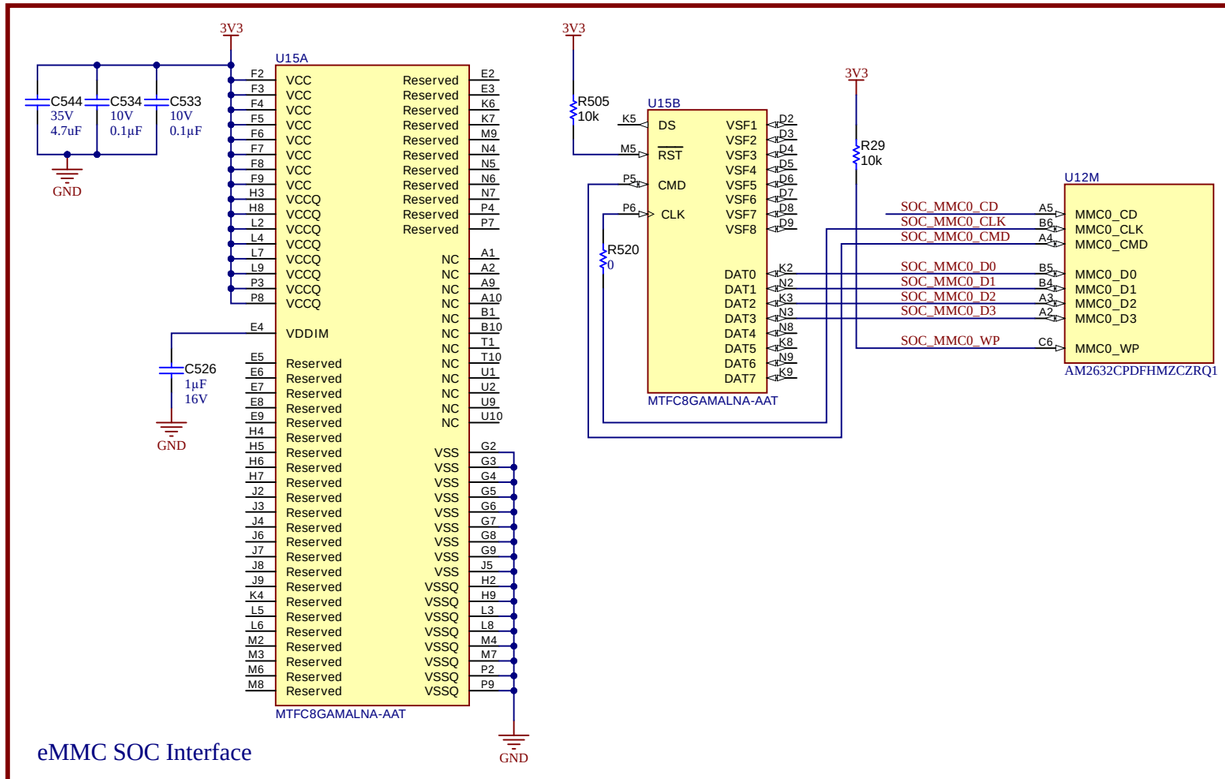


Table 5-2. BOOTMODE Pin Mapping

Boot Mode	SPI0_D0_pad (SOP3)	SPI0_CLK_pad (SOP2)	QSPI_D1 (SOP1)	QSPI_D0 (SOP0)
QSPI (4S) - Quad Read Mode	0	0	0	0
UART	0	0	0	1
QSPI (1S) - Single Read Mode	0	0	1	0
QSPI (4S) - Quad Read UART Fallback Mode	0	1	0	0
QSPI (1S) - Single Read UART Fallback Mode	0	1	0	1
DevBoot	1	0	1	1
Unsupported Boot Mode	All other combinations not defined above			

SOC BOOT MODE



Orderable: DLP2021AM263Q1EVM		Designed for: Public Release	Mod. Date: 5/1/2024
TID #: N/A		Project Title: DLP2021AM263Q1EVM	
Number: DLP096	Rev: B	Sheet Title: SoC Memory	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 7 of 10
Drawn By: A. Whitehead		File: DLP096B_SoC_Memory.SchDoc	Size: B
Engineer: A. Whitehead		Contact: http://www.ti.com/support	

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Raw ONFI NAND Daughtercard Socket

U12E

AM2632CPDFHMZCZRQ1

EPWM0_A	B2	R_W_LED_IADJ_PWM
EPWM0_B	B1	
EPWM1_A	D3	G_LED_IADJ_PWM
EPWM1_B	D2	
EPWM2_A	C2	B_LED_IADJ_PWM
EPWM2_B	C1	
EPWM3_A	E2	PWM_SEL1
EPWM3_B	E3	
EPWM4_A	D1	PWM_SEL2
EPWM4_B	E4	
EPWM5_A	F2	
EPWM5_B	G2	
EPWM6_A	E1	
EPWM6_B	F3	
EPWM7_A	F4	
EPWM7_B	F1	
EPWM8_A	G3	
EPWM8_B	H2	
EPWM9_A	G1	
EPWM9_B	J2	
EPWM10_A	G4	
EPWM10_B	J3	
EPWM11_A	H1	
EPWM11_B	J1	GPMC_OEn_REn
EPWM12_A	K2	GPMC_WEn
EPWM12_B	J4	GPMC_CSn0
EPWM13_A	K4	GPMC_AD0
EPWM13_B	K3	GPMC_AD1
EPWM14_A	V17	GPMC_AD2
EPWM14_B	T16	GPMC_AD3
EPWM15_A	P15	GPMC_AD4
EPWM15_B	R16	GPMC_AD5
EQEP0_A	B14	STAT0_LED
EQEP0_B	A14	STAT1_LED
EQEP0_I	D11	
EQEP0_S	C12	

U12F

AM2632CPDFHMZCZRQ1

SPI1_D1	D9	DMD_INTERFACE_EN
SPI1_D0	B10	
SPI1_CS0	C9	LED_DRV_EN
SPI1_CLK	A10	BROWNOUT_RST
SPI0_D1	B11	SPI0_D1
SPI0_D0	C10	SPI0_D0
SPI0_CS0	C11	SPI0_CS0
SPI0_CLK	A11	SPI0_CLK
MCAN2_TX	B12	MCAN2_TX
MCAN2_RX	A12	MCAN2_RX
MCAN1_TX	K1	SHUNT_ENABLE
MCAN1_RX	L2	RED_WHITE_LED_EN
MCAN0_TX	L1	GREEN_LED_EN
MCAN0_RX	M1	BLUE_LED_EN
LIN2_TXD	A8	LIN2_TXD
LIN2_RXD	B8	LIN2_RXD
LIN1_TXD	B9	
LIN1_RXD	A9	
UART1_TXD	M3	GPMC_AD7
UART1_RXD	L3	GPMC_AD6
UART0_TXD	A6	UART0_TXD
UART0_RXD	A7	UART0_RXD
UART0_RTS	C7	
UART0_CTS	B7	
I2C1_SDA	C8	I2C1_SDA
I2C1_SCL	D7	I2C1_SCL
I2C0_SDA	B13	I2C0_SDA
I2C0_SCL	A13	I2C0_SCL

U12H

AM2632CPDFHMZCZRQ1

SDFM0_CLK0	B16	PR0_PRU1_GPIO7
SDFM0_CLK1	A16	GPMC_ADVn_ALE
SDFM0_CLK2	B15	DMD_POWER_EN
SDFM0_CLK3	A15	
SDFM0_D0	D14	
SDFM0_D1	D13	PR0_PRU1_GPIO17
SDFM0_D2	C13	
SDFM0_D3	C14	

Off-sheet connectors

PR0_PRU1_GPIO7	PR0_PRU1_GPIO7
PR0_PRU1_GPIO17	PR0_PRU1_GPIO17
PR0_PRU1_GPIO9	GPMC_BE0n_CLE
PR0_PRU0_GPIO10	GPMC_WAIT0
PR0_PRU0_GPIO8	GPMC_WPn

J13

Socket to NAND MT29F4G08ABAFAWP-AAT

3V3	1	2	5V
GPMC_AD0	5	6	GPMC_LOCK
GPMC_AD1	7	8	GPMC_CSn0
GPMC_AD2	9	10	GPMC_BE0n_CLE
GPMC_AD3	11	12	GPMC_ADVn_ALE
GPMC_AD4	13	14	GPMC_WEn
GPMC_AD5	15	16	GPMC_OEn_REn
GPMC_AD6	17	18	GPMC_WPn
GPMC_AD7	19	20	GPMC_WAIT0

GND

LED Status

STAT0_LED	R32	1.8k	D6	GND
STAT1_LED	R31	1.8k	D5	GND

CAN / LIN / I2C / UART Daughtercard Socket

J14

3V3	1	2	3V3
MCAN2_TX	3	4	I2C0_SDA
MCAN2_RX	5	6	I2C0_SCL
	7	8	
	9	10	
LIN2_TXD	11	12	UART0_TXD
LIN2_RXD	13	14	UART0_RXD
3V3	15	16	3V3

GND GND

TotalPhase Cheetah USB-to-SPI Adapter

J11A J11B

	1	2	5V
	3	4	
SPI0_D0	5	6	
SPI0_CLK	7	8	SPI0_D1
SPI0_CS0	9	10	

702461002

GND

D0=MISO, D1=MOSI

Ethernet RMII Daughtercard Socket

U12G

AM2632CPDFHMZCZRQ1

MDIO0_MDC	M17	SOC_MDC
MDIO0_MDIO	N16	SOC_MDIO
RGMII1_RD0	U17	RMII1_RXD0
RGMII1_RD1	T17	RMII1_RXD1
RGMII1_RD2	U18	
RGMII1_RD3	T18	
RGMII1_RX_CTL	R18	RMII1_RX_ER
RGMII1_RXC	R17	SOC_CLOCKOUT0
RGMII1_TD0	P16	RMII1_TXD0
RGMII1_TD1	P17	RMII1_TXD1
RGMII1_TD2	P18	RMII1_CRS_DV
RGMII1_TD3	N17	
RGMII1_TX_CTL	M18	RMII1_TX_EN
RGMII1_TXC	N18	

J15

3V3	1	2	5V
	3	4	
SOC_MDC	5	6	RMII1_RX_ER
SOC_MDIO	7	8	RMII1_TX_EN
RMII1_RXD0	9	10	RMII1_CRS_DV
RMII1_RXD1	11	12	SOC_CLOCKOUT0
RMII1_TXD0	13	14	
RMII1_TXD1	15	16	

GND

Socket for Ethernet RMII e.g. DP83TD510E (10BASE-T1L / 10BASE-T1S PHY shown only as example of AM263x expected connections)

JTAG Programming / Debug

J12B J12A

SOC_JTAG_TMS	1	2	
SOC_JTAG_TDI	3	4	
3V3	5		
R75 100			
SOC_JTAG_TDO	7	8	
	9	10	
SOC_JTAG_TCK	11	12	
	13	14	
	15	16	
	17	18	
	19	20	

GND

U12B

AM2632CPDFHMZCZRQ1

SOC_JTAG_TCK	B3	TCK
SOC_JTAG_TDI	C5	TDI
SOC_JTAG_TDO	C4	TDO
SOC_JTAG_TMS	D5	TMS
U1		RESERVED0
U3		RESERVED1
V2		RESERVED2

GND

Orderable: DLP2021AM263Q1EVM		Designed for: Public Release	Mod. Date: 5/1/2024
TID #: N/A		Project Title: DLP2021AM263Q1EVM	
Number: DLP096	Rev: B	Sheet Title: Interfaces_Sockets	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 8 of 10
Drawn By: A. Whitehead		File: DLP096B_Interfaces_Sockets.SchDoc	Size: B
Engineer: A. Whitehead		Contact: http://www.ti.com/support	

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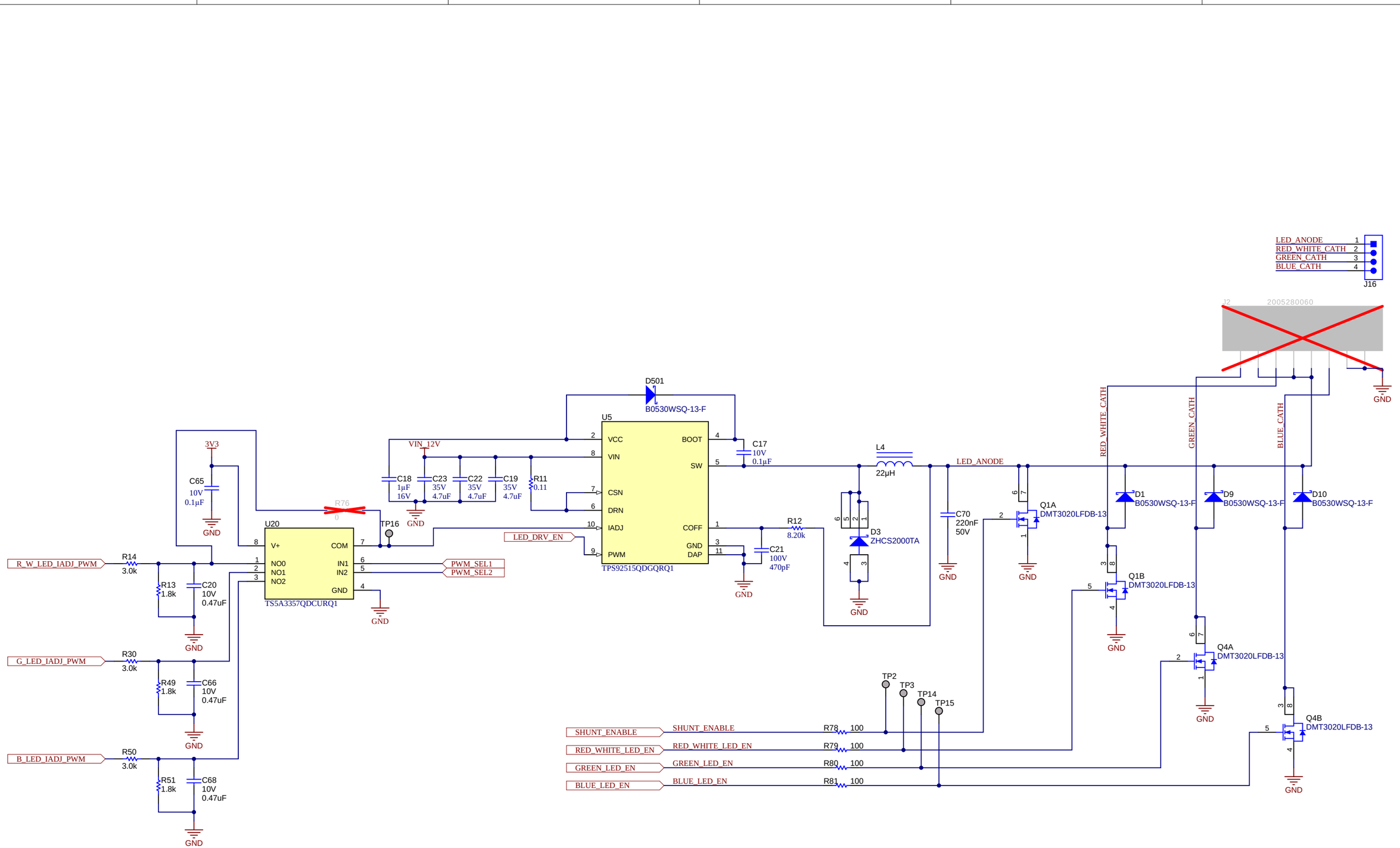
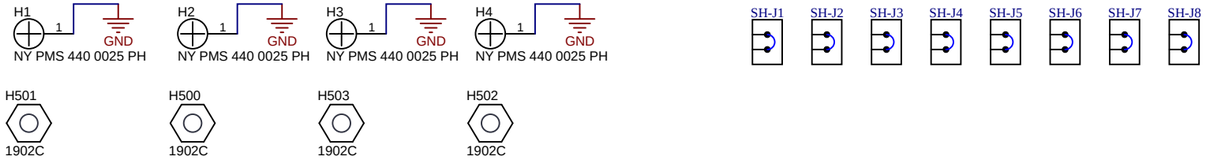


Orderable: DLP2021AM263Q1EVM		Designed for: Public Release	Mod. Date: 5/1/2024
TID #: N/A		Project Title: DLP2021AM263Q1EVM	
Number: DLP096	Rev: B	Sheet Title: LED Driver	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 9 of 10
Drawn By: A. Whitehead		File: DLP096B_LED_Driver.SchDoc	Size: B
Engineer: A. Whitehead		Contact: http://www.ti.com/support	



PCB Number: DLP096
PCB Rev: B

PCB
LOGO
Texas Instruments

CE Mark

PCB
LOGO
FCC disclaimer

PCB
LOGO
WEEE logo

Variant/Label Table	
Variant	Label Text
001	DLP2021AM263Q1EVM

LBL1
PCB Label
THT-14-423-10
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ5
Assembly Note
Indication provided for the D* components at their cathode side.

Orderable: DLP2021AM263Q1EVM		Designed for: Public Release	Mod. Date: 5/1/2024
TID #: N/A		Project Title: DLP2021AM263Q1EVM	
Number: DLP096	Rev: B	Sheet Title: Hardware	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 10 of 10
Drawn By: A. Whitehead		File: DLP096B_Hardware.SchDoc	Size: B
Engineer: A. Whitehead		Contact: http://www.ti.com/support	

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