AM64x GENERAL PURPOSE EVM BOARD
TMDS64GPEVM

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VER	1.05

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TEXAS INSTRUMENTS MISTRAL

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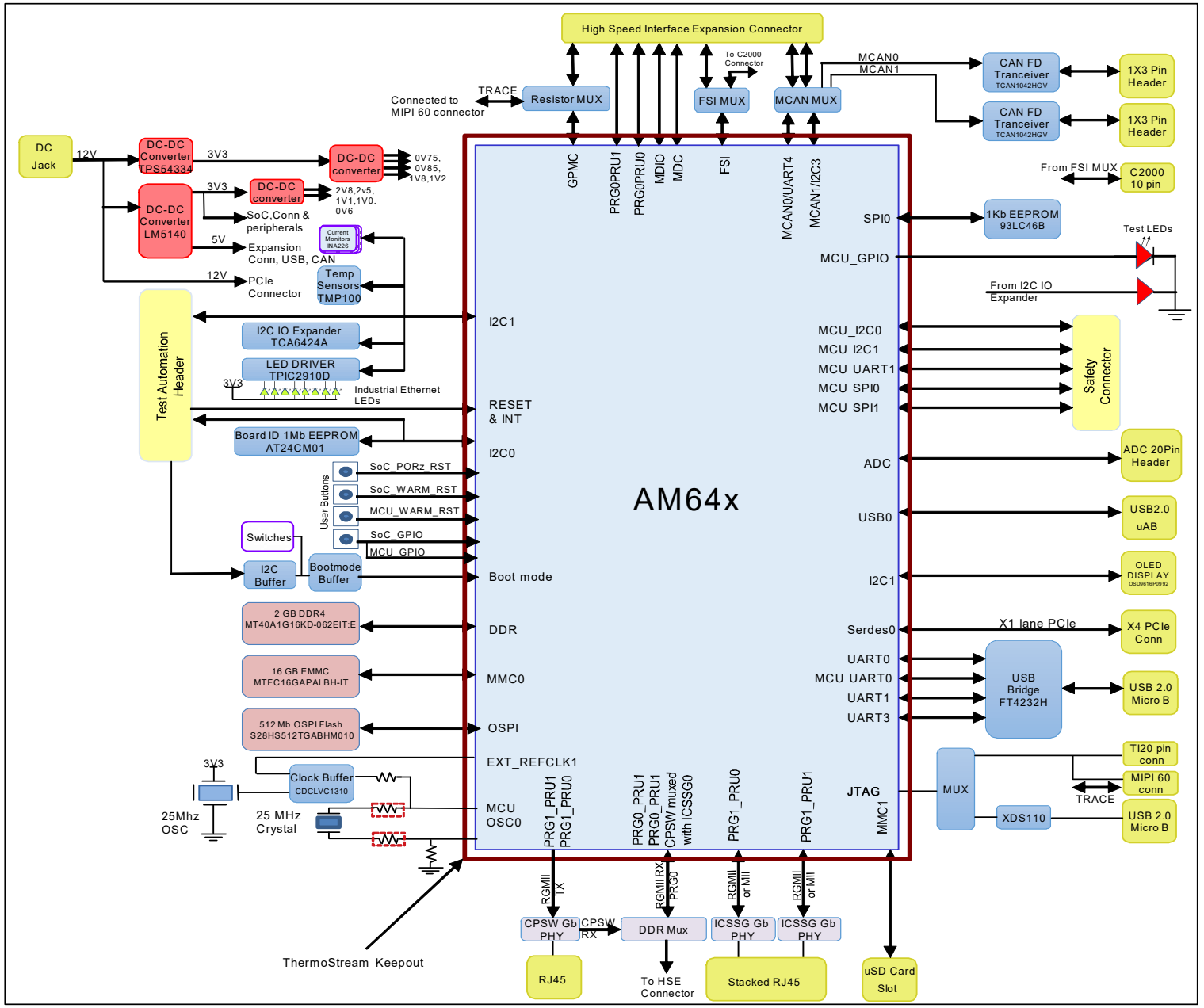
REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
1.0	10th AUGUST 2020	Drafted from "PROC101E1_SCH" document.	Mistral Design Team	AJIT MB	AJIT MB
1.01	11th AUGUST 2020	Power Sequence changed as Per power down sequence mentioned in AM64x Data manual	Mistral Design Team	AJIT MB	AJIT MB
1.02	13th AUGUST 2020	1.U74 Monitoring changed from 12V to 5V 2. U103 OR gate and U104 AND gate added to ensure the power down sequence is followed as mentioned in the data manual 3.R260,R266 values changed to monitor 5V 4.U35 changed to 3 input AND gate 5.Q20 added to provide MCU_PORz to SD enable 6.R131 changed from 100k to 10k resistor 7.C486 , 10uF added to U25 regulator output VCC_CORE 8.R539,R284,R293 removed 9.Inductor Values, Current Sense Resistor Value & compensation circuit changed in LM5140 section	Mistral Design Team	AJIT MB	AJIT MB
1.03	14th AUGUST 2020	1.Added series resistor option for OSPI_LBCLK0 to connect to DS of OSPI Memory 2. Added LPF filters for SoC_I2C0_SCL, SoC_I2C0_SDA, MCU_I2C0_SCL, SoC_I2C0_SDA and PRG1_RGMII_INTn signals 3. Changed C70 470uF capacitor to Electrolytic Polymer CAP 4. Added series resistors R577 to R589 to EN pins of all Power IC's 5. Deleted Net Name CAP_VDDSHV_MMC1 6. Changed Net SoC_PORz to PORz 7. R314 Pull-up changed from VCC3V3_PREREG to VCC_3V3_SYS 8. U72 input voltage changed from VCC_3V3_SYS to VCC3V3_PREREG 9. TEST_LED1 is connected to IO Expander pin P20	Mistral Design Team	AJIT MB	AJIT MB
1.04	2nd SEPTEMBER 2020	1.Enable for U100 changed from VIN_MON_PORz_3V3_PG to VCC3V3_SYS_PG 2.Voltage divider provided to monitor VMAIN and VCC_5V0 for VDDA_SYS_MON 3.Net name VDDA_MCU_ADC changed to VDDA_ADC 4. Series Resistors R592 & R601 for OSPI DQS Removed 5. Resistors RA6, R391 & R392 made DNI	Mistral Design Team	AJIT MB	AJIT MB

BLOCK DIAGRAM_AM64x_EVM



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Title	BLOCK DIAGRAM_CP BOARD	
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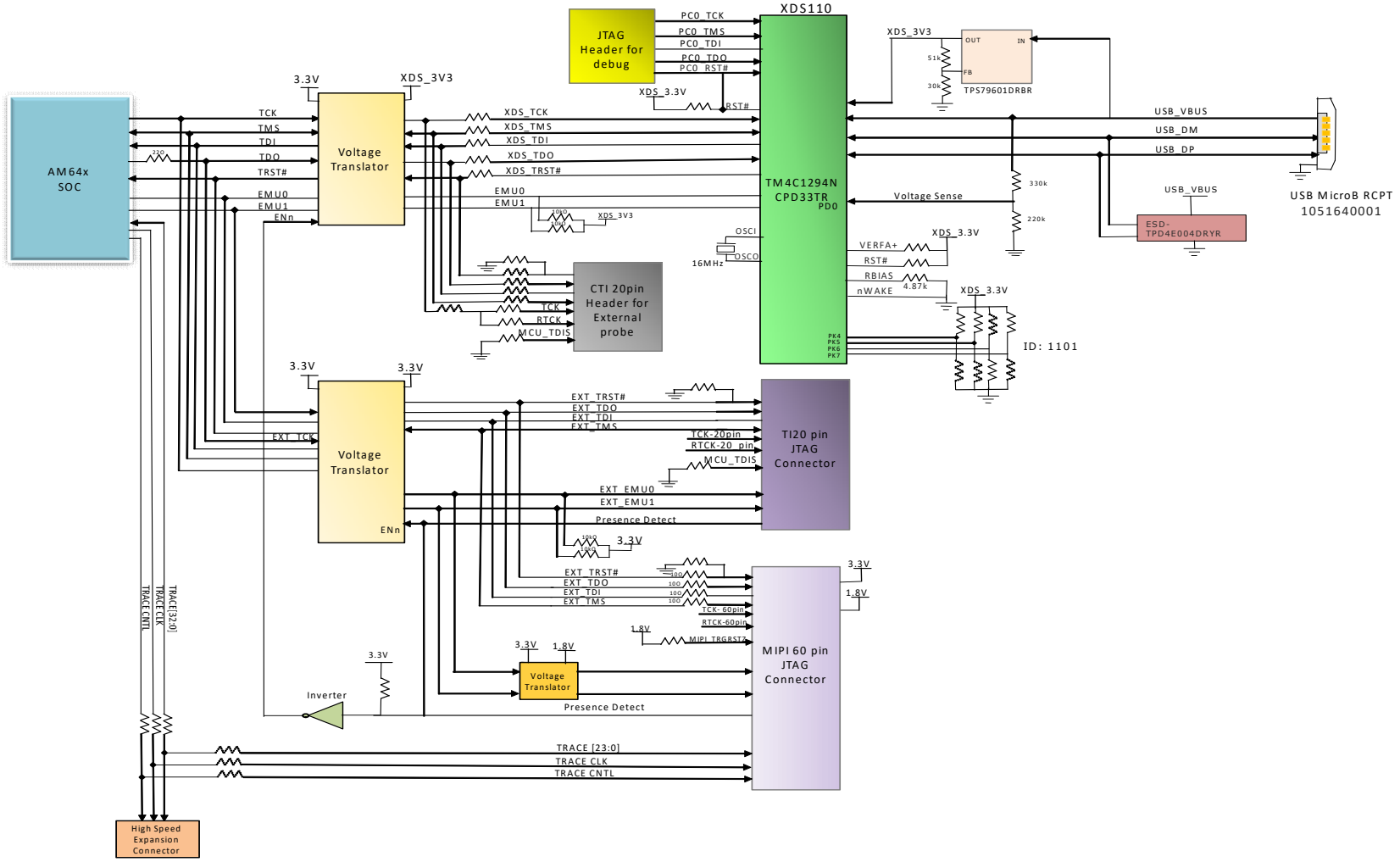
BLOCK DIAGRAM_XDS110



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Title	BLOCK DIAGRAM_XDS110	
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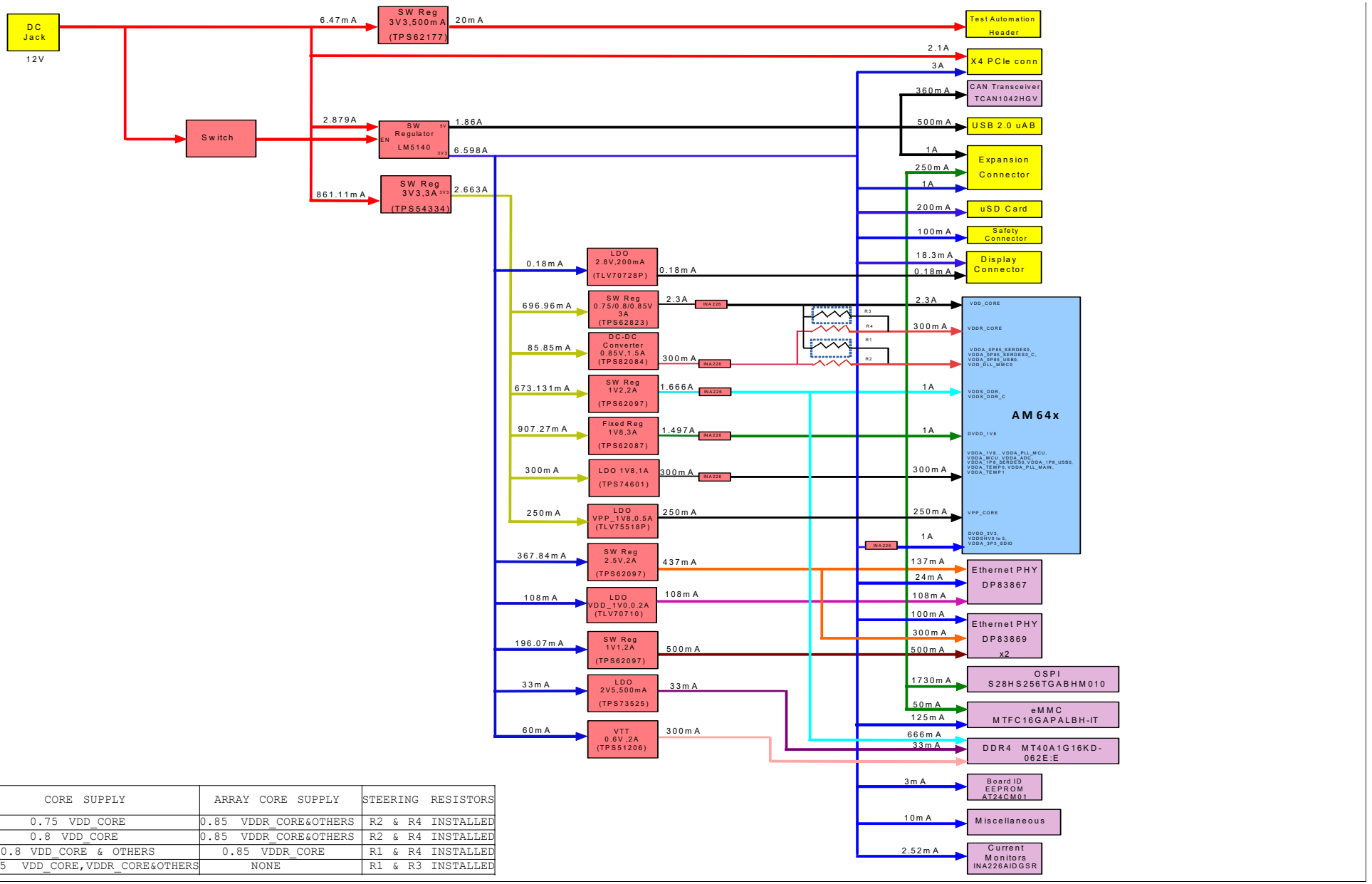
POWER FLOW DIAGRAM



CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE & OTHERS	0.85 VDDR_CORE	R1 & R4 INSTALLED
0.85 VDD_CORE,VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

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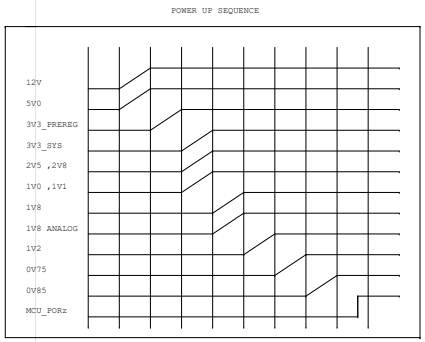
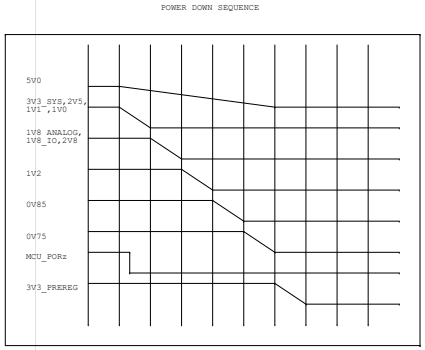
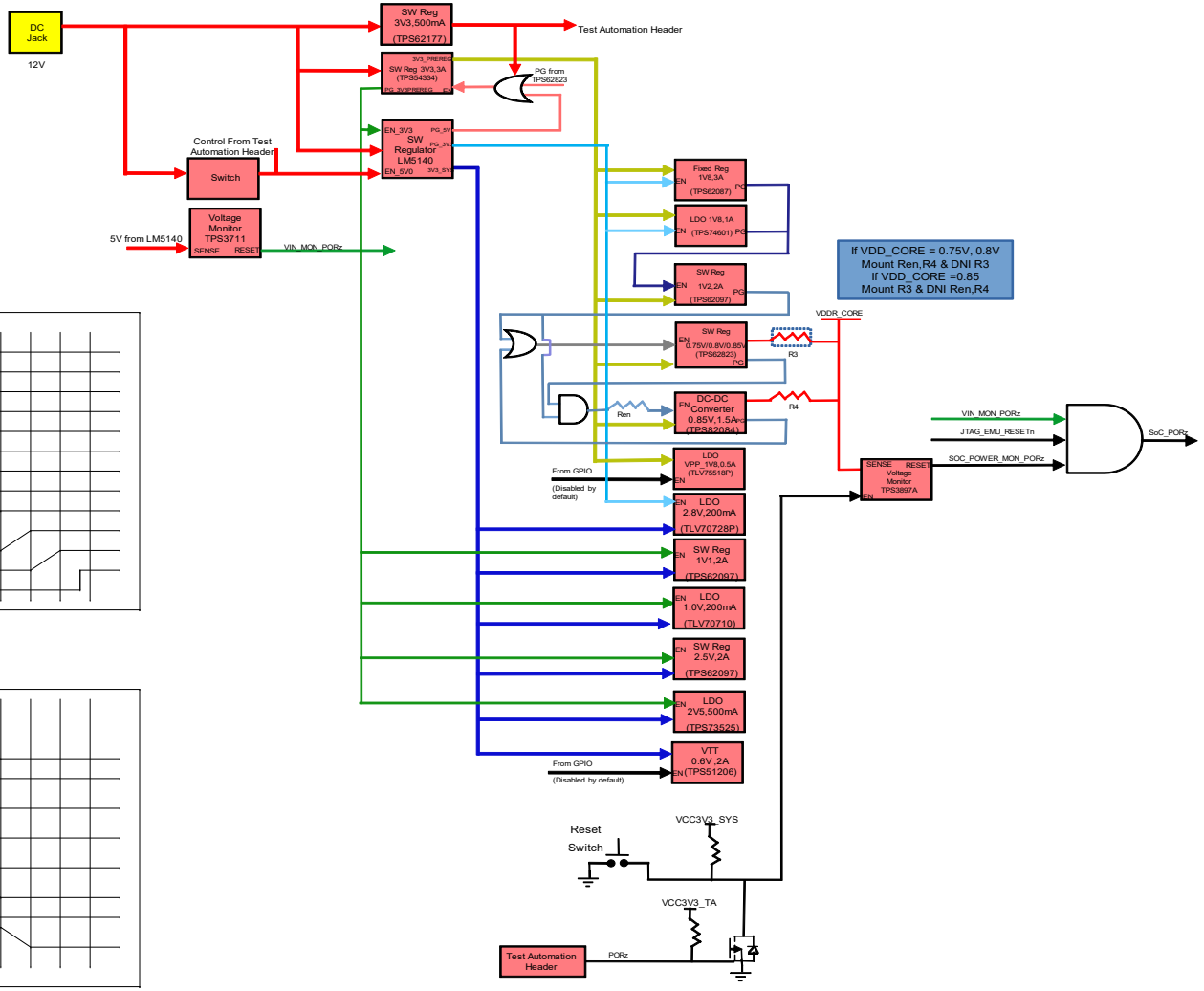
POWER SEQUENCE







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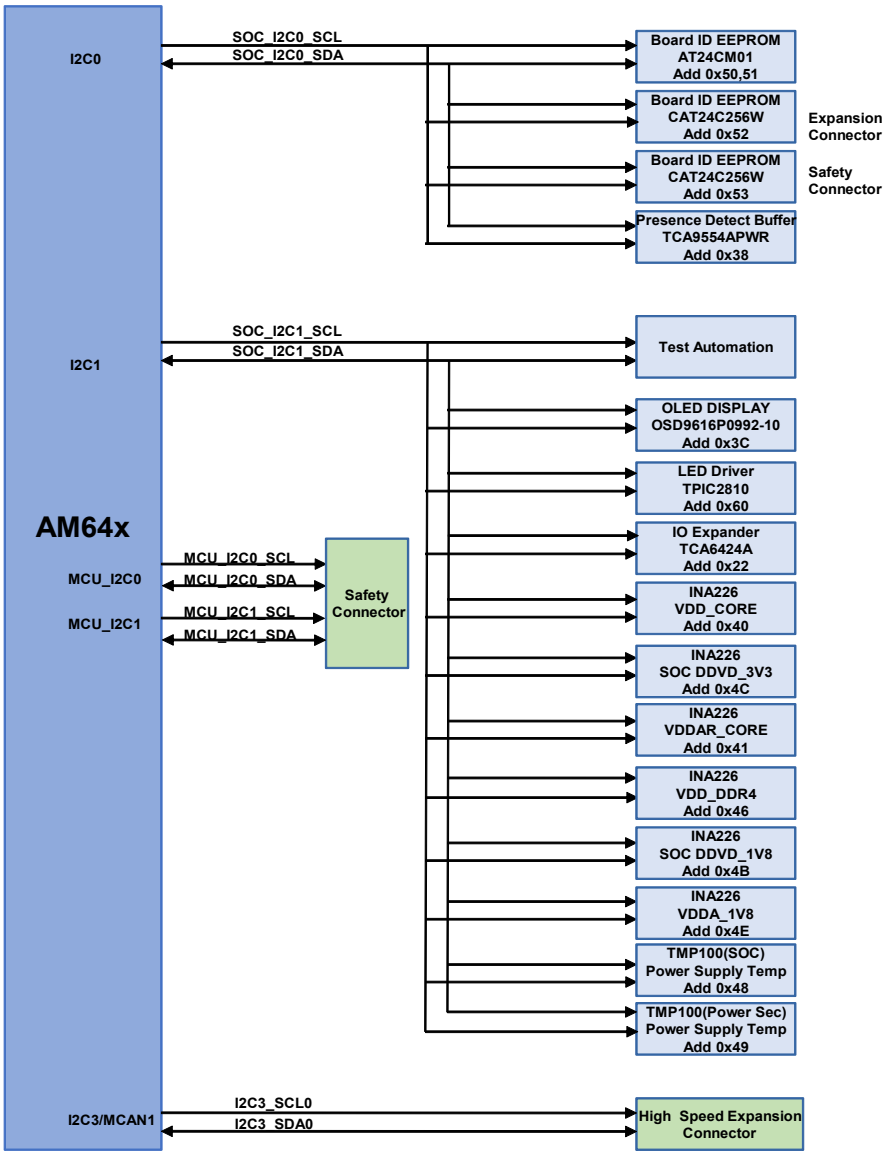
GPIO MAPPING TABLE

S.NO	GPIO DESCRIPTION	GPIO NETNAME	REQUIRED ON	FUNCTIONALITY	GPIO USED	SoC Muxed Signal Name	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE
1	EMMC RESET Control GPIO	GPIO_eMMC_RSTn	GP EVM	Reset	IO EXPANDER- P00		OUTPUT	HIGH	LOW
2	OSPI RESET Control GPIO	GPIO_OSPI_RSTn	GP EVM	Reset	GPIO013	OSPI0_CS2	OUTPUT	HIGH	LOW
3	CPSW RGMII1 RESET Control GPIO	GPIO_CPSW1_RST	GP EVM	Reset	IO EXPANDER- P02		OUTPUT	HIGH	LOW
4	PRG1 RGMII1 Ethernet PHY RESET Control GPIO	GPIO_RGMII1_RST	GP EVM	Reset	IO EXPANDER- P03		OUTPUT	HIGH	LOW
5	PRG1 RGMII2 Ethernet PHY RESET Control GPIO	GPIO_RGMII2_RST	GP EVM	Reset	IO EXPANDER- P04		OUTPUT	HIGH	LOW
6	PRG1 RGMII1 Ethernet PHY Link Detection GPIO	PRG1_ETH1_LED_LINK	GP EVM	Link Detection	PRG1_PRU0_GPO8		INPUT	LOW	HIGH
7	PRG1 RGMII2 Ethernet PHY Link Detection GPIO	PRG1_ETH2_LED_LINK	GP EVM	Link Detection	PRG1_PRU1_GPO8		INPUT	LOW	HIGH
8	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	GP EVM	Interrupt	Connected to PRG1_RGMII_INT via 0E res		INPUT	HIGH	LOW
9	PRG1 Ethernet PHY 1Interrupt	PRG1_RGMII_INT	GP EVM	Interrupt	GPIO1_70	EXTINTn	INPUT	HIGH	LOW
10	PRG1 Ethernet PHY 2Interrupt			Interrupt			INPUT	HIGH	LOW
11	PCIe RESET Control GPIO	GPIO_PCIe_RST_OUT	GP EVM	Reset	IO EXPANDER- P05		OUTPUT	LOW	HIGH
12	SD card load switch enable control	MMC1_SD_EN	GP EVM	Load SW Enable	IO EXPANDER- P06		OUTPUT	HIGH	LOW
13	One GPIO is required to control the Mux select between HSE and FSI Connector	FSI_FET_SEL	GP EVM	Mux Seleection	IO EXPANDER- P07		OUTPUT	PREFERABLE	PREFERABLE
14	One GPIO is required to enable Standby mode in CAN tranceiver	MCAN0_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P10		OUTPUT	LOW	HIGH
15	One GPIO is required to enable Standby mode in CAN tranceiver	MCAN1_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P11		OUTPUT	LOW	HIGH
16	One GPIO is required to control the Mux select between HSE and Ethernet PHY	CPSW_FET_SEL	GP EVM	Mux Seleection	IO EXPANDER- P12		OUTPUT	PREFERABLE	PREFERABLE
17	MDC/MDIO FET Switch Select for Mux	CPSW_FET2_SEL	GP EVM	Mux Selection	IO EXPANDER- P13		OUTPUT	PREFERABLE	PREFERABLE
18	MDC/MDIO FET Switch Select for Mux	PRG1_RGMII2_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P14		OUTPUT	PREFERABLE	PREFERABLE
19	VTT 0.6V regulator Enable	VTT_EN	GP EVM	VTT 0.6V regulator Enable	GPIO0_12	OSPI0_CSn1	OUTPUT	LOW	HIGH
20	TEST GPIO1 from Test Automation Connector/ GPIO for GP board push button	TEST GPIO1/GPIO1_43	GP EVM	GPIO for communications with AM64x	GPIO1_43	SPI0_CS1	INPUT	HIGH	LOW
21	TEST GPIO2 from Test Automation Connector	TEST GPIO2	GP EVM	GPIO for communications with AM64x	IO EXPANDER- P15		INPUT	HIGH	LOW
22	OLED Display RESET GPIO	GPIO_OLED_RESETn	GP EVM	Reset	IO EXPANDER- P16		OUTPUT	LOW	HIGH
23	IO Expander Interrupt	IO_EXP_INTn	GP EVM	Interrupt	GPIO1_78	MMC1_SDWP	INPUT	HIGH	LOW
24	VPP 1.8V regulator Enable	VPP_LDO_EN	GP EVM	VPP 01.8V regulator Enable	IO EXPANDER- P17		OUTPUT	LOW	HIGH
25	One GPIO is required to control the Mux select between HSE and CAN Interface	CAN_MUX_SEL	GP EVM	Mux Seleection	IO EXPANDER- P01		OUTPUT	LOW	HIGH
26	User LED	TEST_LED1	GP EVM	Test	IO EXPANDER- P20		OUTPUT	LOW	HIGH
27	User LED	TEST_LED2	GP EVM	Test	MCU_SPI1_CS0	MCU_GPIO0_5	OUTPUT	LOW	HIGH

I2C TREE



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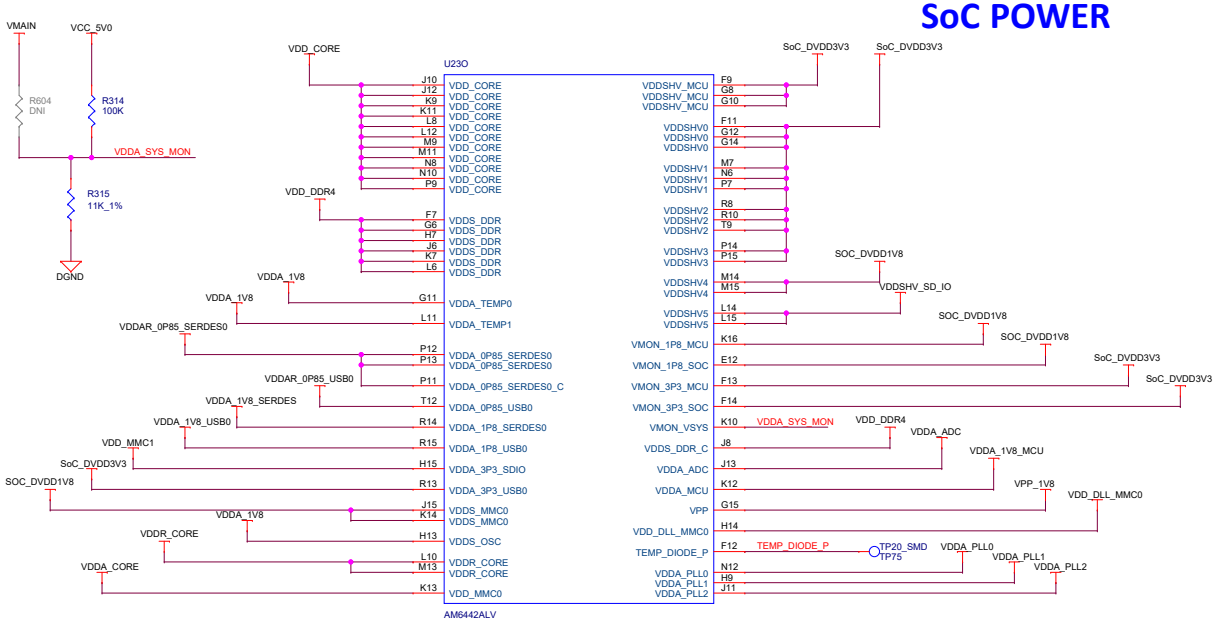
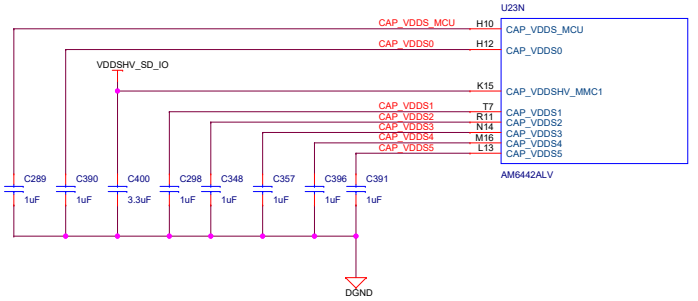
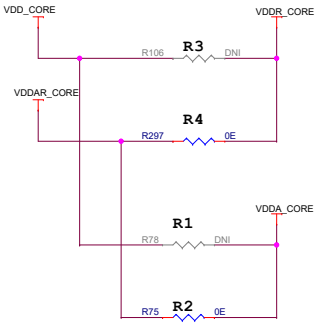
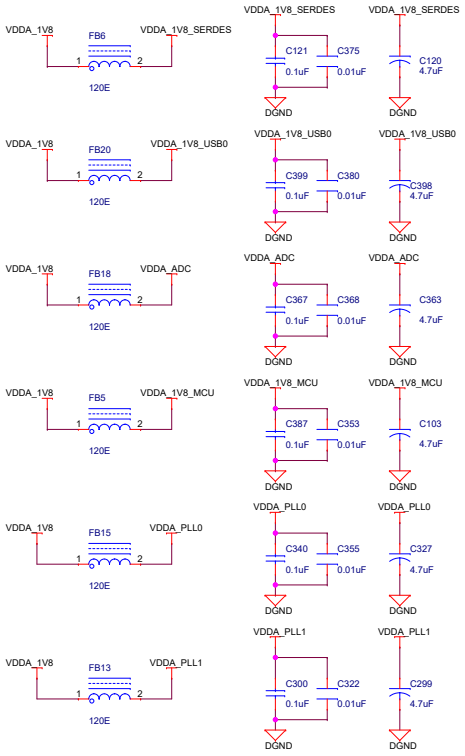
SoC POWER



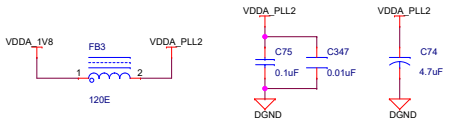




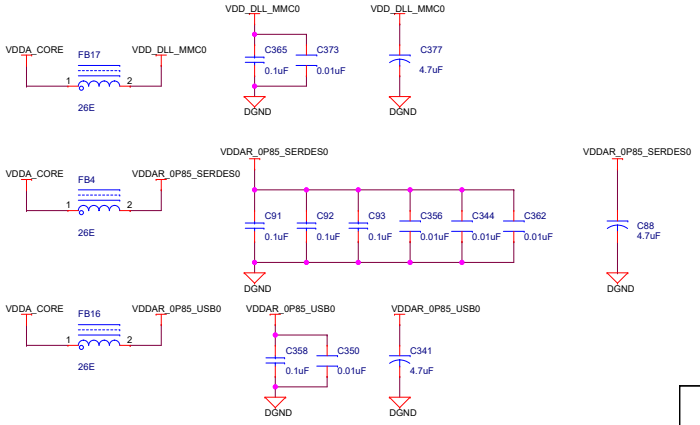
1.8V Analog SUPPLY



1.8V Analog SUPPLY



CORE SUPPLY



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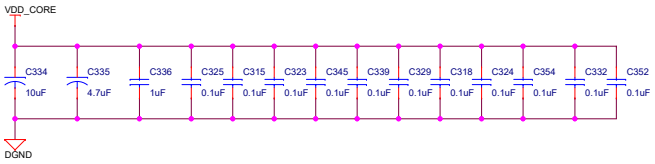
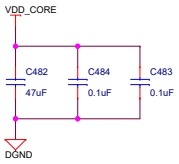
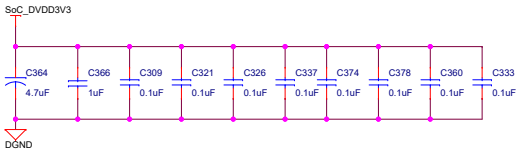
SoC POWER Decaps



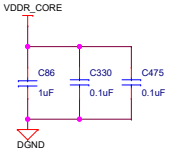
Place one 0.1uF cap near each Pin

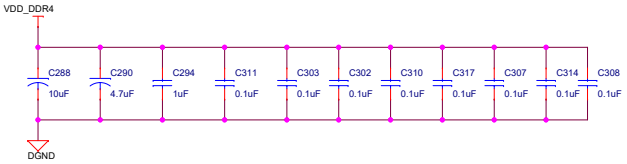


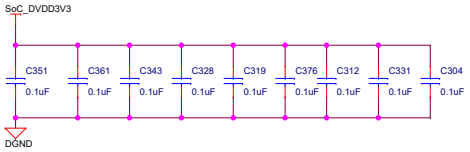
To place after current sense resitor on VDD_CORE plane

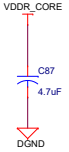


Place one 0.1uF cap near each Pin

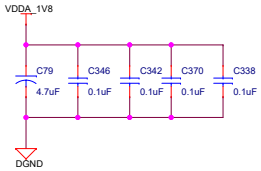




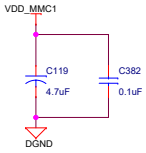




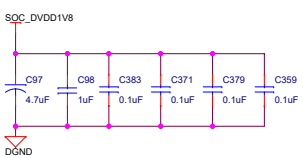
VDD ARRAY CORE

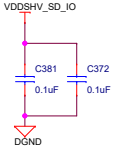


VDDA_3P3_SDIO



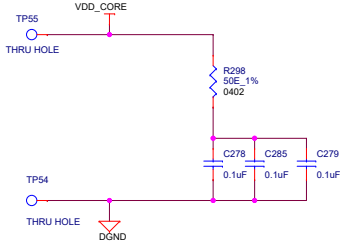
Place one 0.1uF cap near each Pin

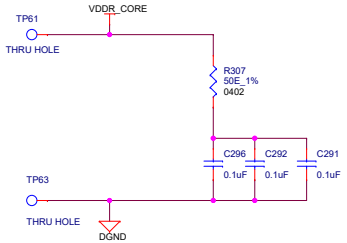




Place one 0.1uF cap near each Pin

Core & Array Core Supply Kelvin Sensing





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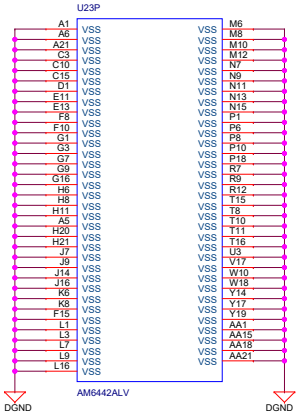
SoC POWER - VSS



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Title	SOC VSS	
Size	Variant Name = PROC101E2 TMDS64GPEVM	Rev
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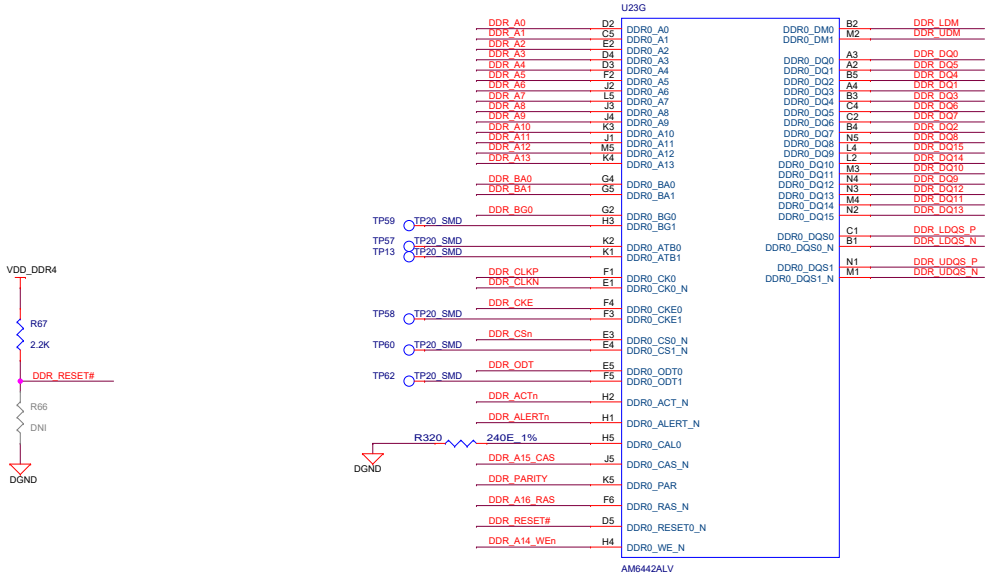
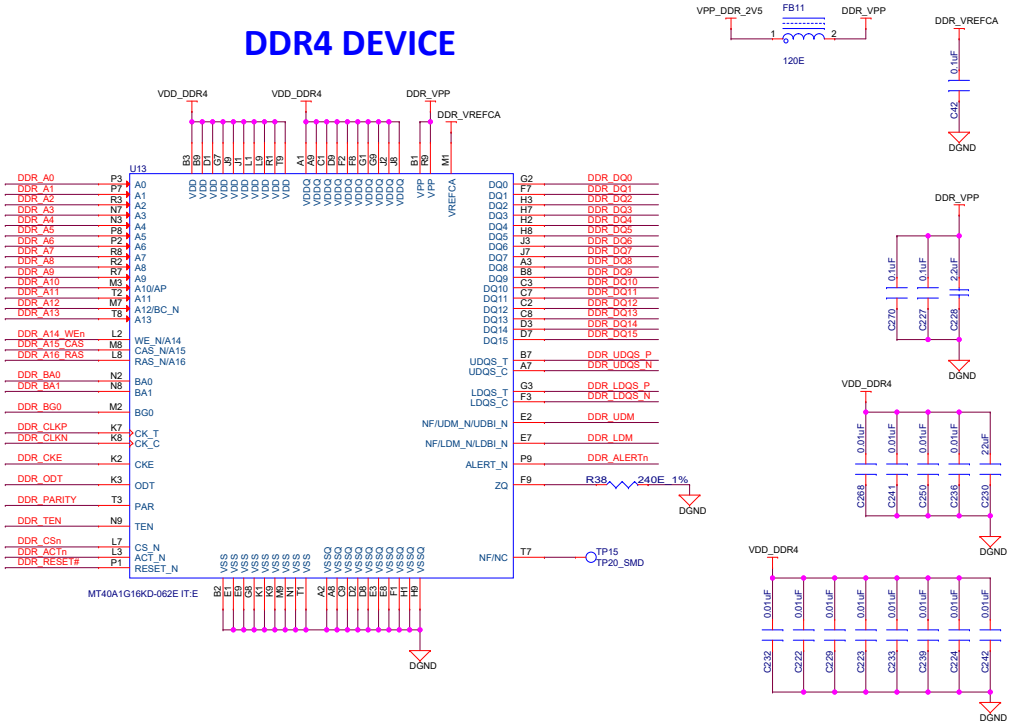
SoC DDR INTERFACE

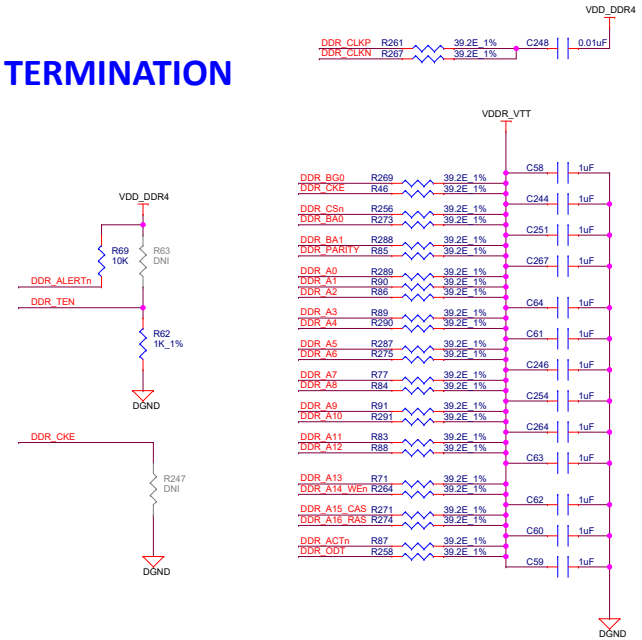


DDR DQ Lines Swapped With Data Byte

DDR4 DEVICE



DDR TERMINATION



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Title	DDR INTERFACE		
Size	Variant Name = PROC101E2 TMDS64GPEVM		Rev
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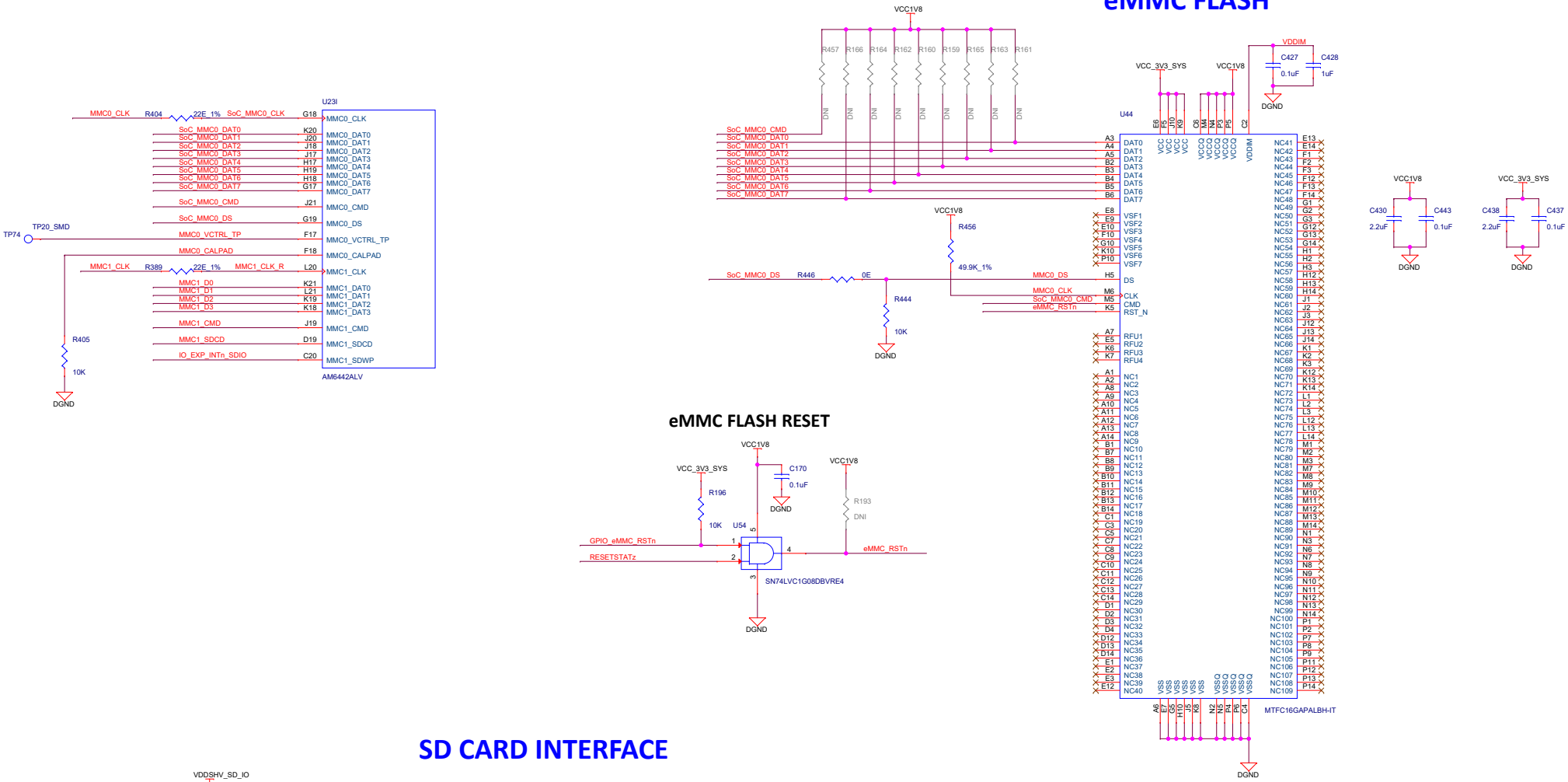
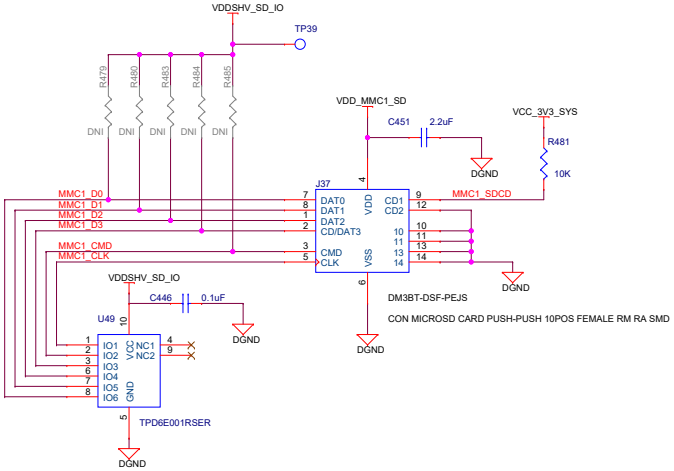
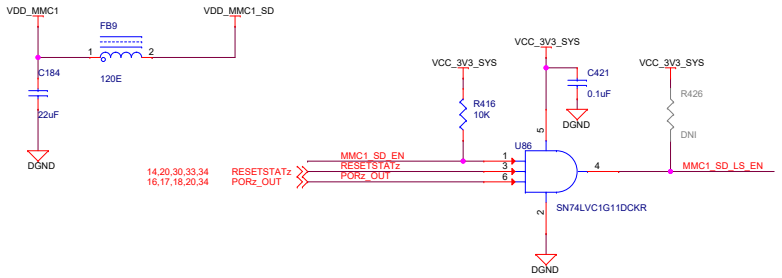
eMMC FLASH

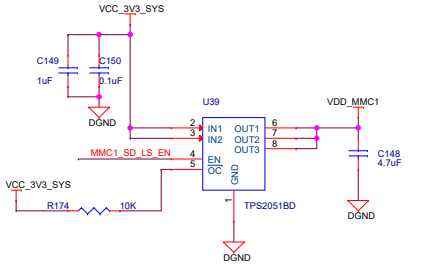


eMMC FLASH RESET

SD CARD INTERFACE







Off Page Connections

From & To IO Expander	33	IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO
	33	GPIO_eMMC_RSTn	GPIO_eMMC_RSTn
	33	MMC1_SD_EN	MMC1_SD_EN

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TEXAS INSTRUMENTS

MISTRAL

Title	eMMC FLASH_SDCARD INTERFACE	
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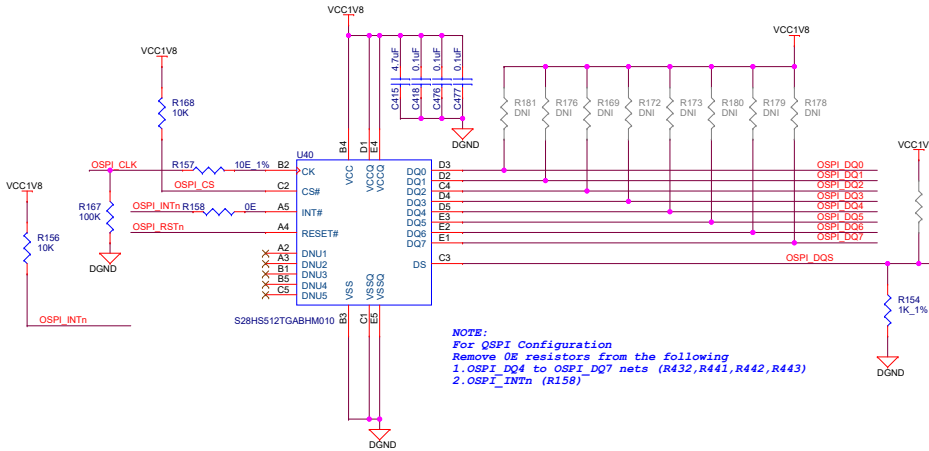
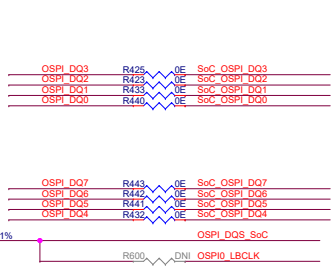
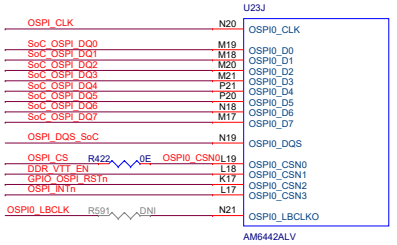
OSPI FLASH



NOTE:
For QSPI Configuration
Remove 0E resistors from the following
1.OSPI_DQ4 to OSPI_DQ7 nets (R432,R441,R442,R443)
2.OSPI_INTn (R158)



Place R600 close to the memory to avoid stub

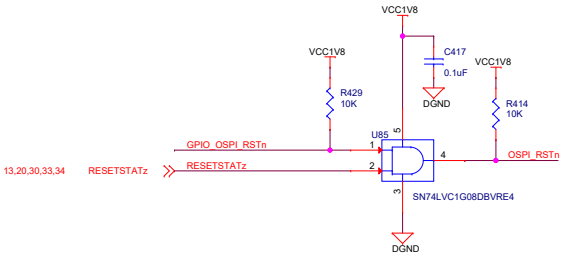


Place R591 close to the ball with as little trace as possible

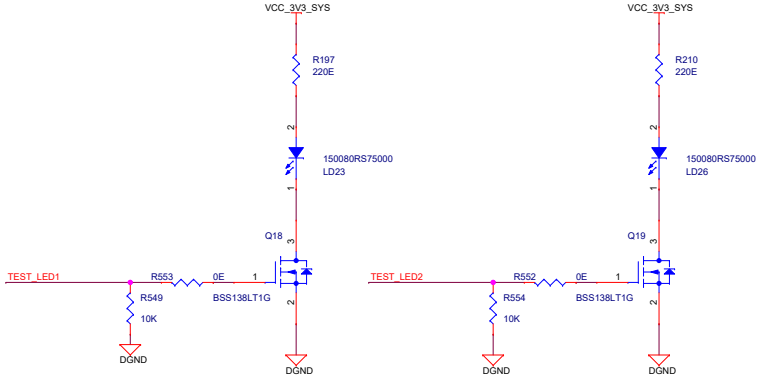
To Route DQS to LBCLK0	To Route DQS to SOC's DQS
Mount R591 & R600	Mount R601 & R592
DNI R601 & R592	DNI R591 & R600

SOC OSPI INTERFACE

OSPI FLASH RESET



USER TEST LED



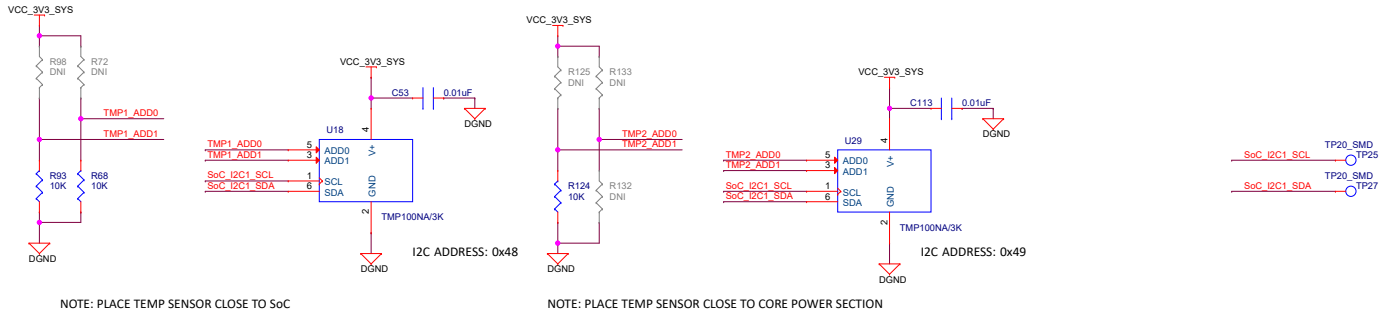
Off Page Connections

TEST_LED1	TEST_LED1	33
TEST_LED2	TEST_LED2	34
To Level Translator	DDR_VTT_EN	DDR_VTT_EN 33

Designed for TI by Mistral Solutions Pvt Ltd

Title	OSPI		
Size	Variant Name = PROC101E2 TMDS64GPEVM		Rev
C			E2
Date:	Thursday, January 28, 2021	Sheet	14 of 40

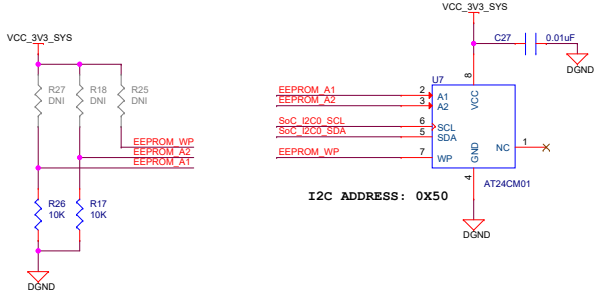
TEMPERATURE SENSOR



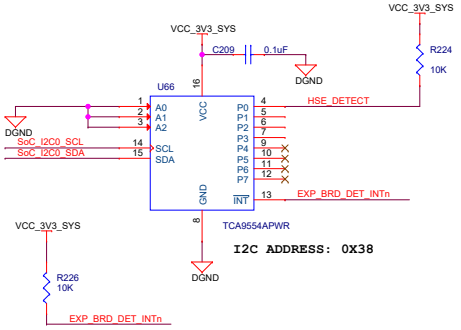
NOTE: PLACE TEMP SENSOR CLOSE TO SoC

NOTE: PLACE TEMP SENSOR CLOSE TO CORE POWER SECTION

BOARD ID EEPROM



BOARD PRESENCE DETECT CIRCUIT



Off Page Connections

HSE_DETECT → HSE_DETECT 27

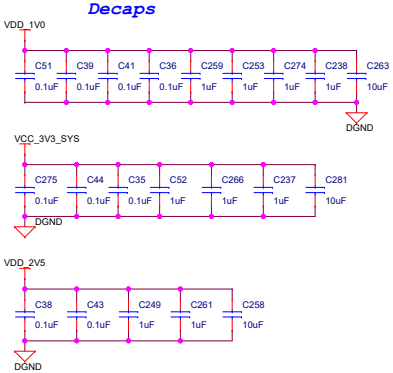
SoC_I2C1_SDA, SoC_I2C1_SCL → SoC_I2C1_SDA 19,21,29,30,32,33; SoC_I2C1_SCL 19,21,29,30,32,33

SoC_I2C0_SDA, SoC_I2C0_SCL → SoC_I2C0_SDA 27,29,33; SoC_I2C0_SCL 27,29,33

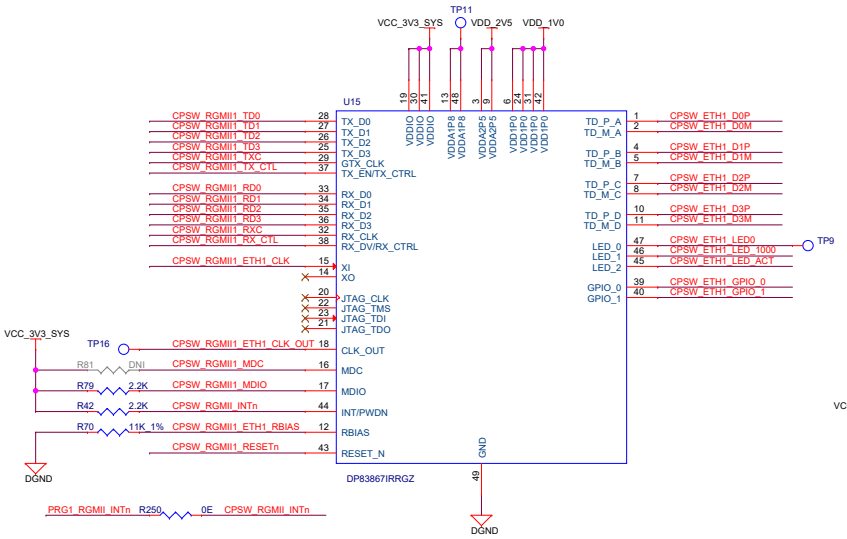
Designed for TI by Mistral Solutions Pvt Ltd

Title	EEPROM,PRESENCE DETECTION & TEMP SENSOR	
Size: C	Variant Name = PROC101E2 TMDS64GPEVM	Rev: E2
Date: Thursday, January 28, 2021	Sheet 15 of 40	

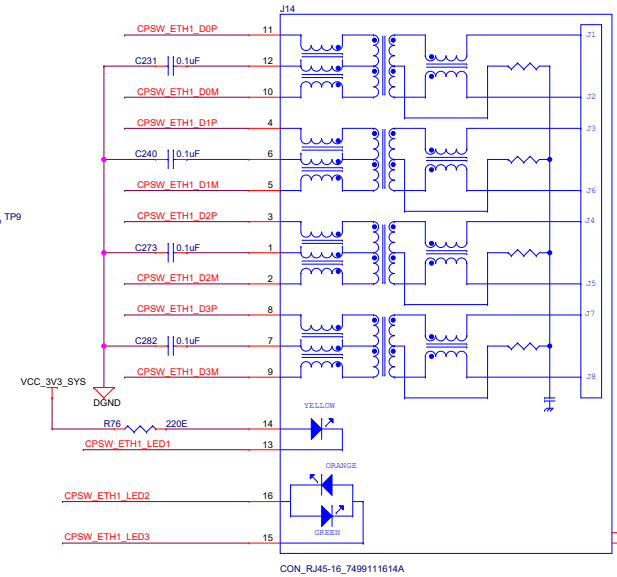
Decaps



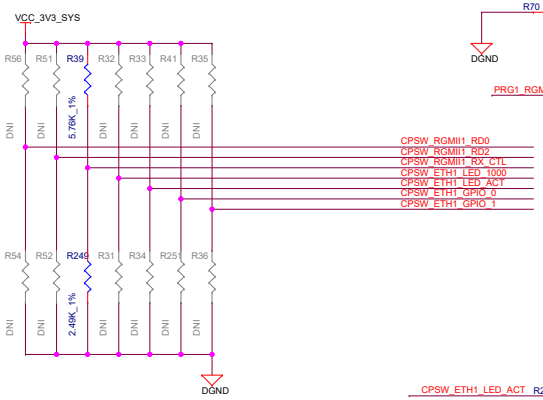
CPSW RGMII 1 - PHY



RJ45 with Integrated Mangnetics

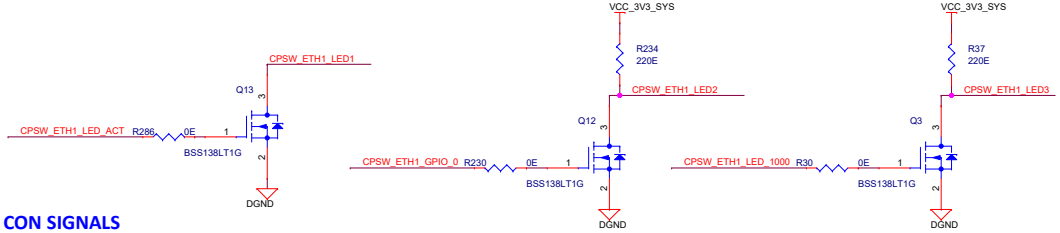


STRAPPING RESISTORS

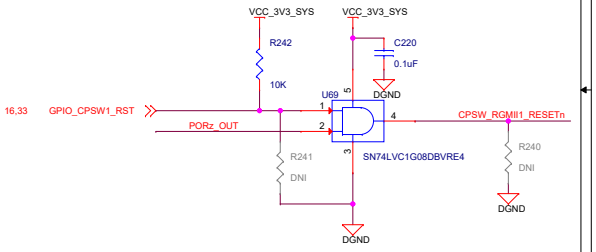


PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx & Rx Clock Skew = 2.0ns

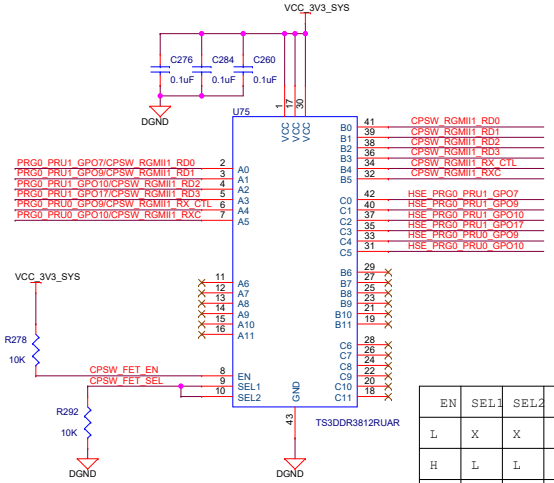
CPSW_ETHERNET PHY- 1 SPEED & ACTIVITY LED 's DRIVERS



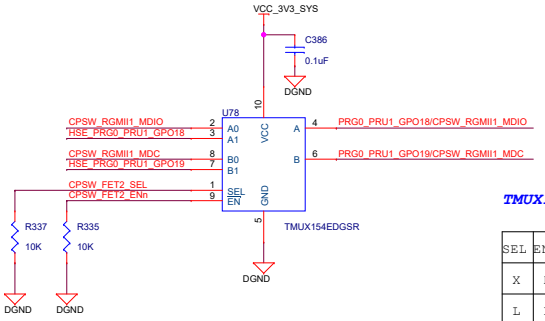
CPSW ETH1 RESET



CPSW RGMII 1 ETHERNET PHY SIGNALS & HSE CON SIGNALS



MDC/MDIO FET SWITCH



TS3DDR3812RUAR Truth Table

EN	SEL1	SEL2	FUNCTION
L	X	X	A0 to A11, B0 to B11, and C0 to C11 are Hi-Z
H	L	L	A0 to A5 = B0 to B5 and A6 to A11 = B6 to B11
H	L	H	A0 to A5 = B0 to B5 and A6 to A11 = C6 to C11
H	H	L	A0 to A5 = C0 to C5 and A6 to A11 = B6 to B11
H	H	H	A0 to A5 = C0 to C5 and A6 to A11 = C6 to C11

TMUX154EDGSR Truth Table

SEL	EN#	FUNCTION
X	H	DISCONNECT
L	L	A=A0 , B=B0
H	L	A=A1 , B=B1

Off Page Connections

From Processor
- 27 PRG0_PRU1_GPO7/CPSW_RGMII1_RD0 → PRG0_PRU1_GPO7/CPSW_RGMII1_RD0
- 27 PRG0_PRU1_GPO9/CPSW_RGMII1_RD1 → PRG0_PRU1_GPO9/CPSW_RGMII1_RD1
- 27 PRG0_PRU1_GPO10/CPSW_RGMII1_RD2 → PRG0_PRU1_GPO10/CPSW_RGMII1_RD2
- 27 PRG0_PRU1_GPO17/CPSW_RGMII1_RD3 → PRG0_PRU1_GPO17/CPSW_RGMII1_RD3
- 27 PRG0_PRU0_GPO9/CPSW_RGMII1_RX_CTL → PRG0_PRU0_GPO9/CPSW_RGMII1_RX_CTL
- 27 PRG0_PRU0_GPO10/CPSW_RGMII1_RXC → PRG0_PRU0_GPO10/CPSW_RGMII1_RXC

From Processor
- 27 CPSW_RGMII1_TD0 → CPSW_RGMII1_TD0
- 27 CPSW_RGMII1_TD1 → CPSW_RGMII1_TD1
- 27 CPSW_RGMII1_TD2 → CPSW_RGMII1_TD2
- 27 CPSW_RGMII1_TD3 → CPSW_RGMII1_TD3
- 27 CPSW_RGMII1_TX_CTL → CPSW_RGMII1_TX_CTL
- 27 CPSW_RGMII1_TXC → CPSW_RGMII1_TXC

- 13,17,18,20,34 PORz_OUT → PORz_OUT
- 17,18,34 PRG1_RGMII_INTn → PRG1_RGMII_INTn

To ICSSG1 ETH FET SW
- 17 CPSW_RGMII1_MDIO → CPSW_RGMII1_MDIO
- 17 CPSW_RGMII1_MDC → CPSW_RGMII1_MDC

From IO Expander
- 16,33 GPIO_CPSW1_RST → GPIO_CPSW1_RST
- 33 CPSW_FET2_SEL → CPSW_FET2_SEL
- 33 CPSW_FET_SEL → CPSW_FET_SEL

From Clock Buffer
- 31 CPSW_RGMII1_ETH1_CLK → CPSW_RGMII1_ETH1_CLK

To HSE Connector
- 27 HSE_PRG0_PRU1_GPO7 → HSE_PRG0_PRU1_GPO7
- 27 HSE_PRG0_PRU1_GPO9 → HSE_PRG0_PRU1_GPO9
- 27 HSE_PRG0_PRU1_GPO10 → HSE_PRG0_PRU1_GPO10
- 27 HSE_PRG0_PRU1_GPO17 → HSE_PRG0_PRU1_GPO17
- 27 HSE_PRG0_PRU0_GPO9 → HSE_PRG0_PRU0_GPO9
- 27 HSE_PRG0_PRU0_GPO10 → HSE_PRG0_PRU0_GPO10

To HSE Connector
- 27 HSE_PRG0_PRU1_GPO18 → HSE_PRG0_PRU1_GPO18
- 27 HSE_PRG0_PRU1_GPO19 → HSE_PRG0_PRU1_GPO19

From Processor
- 27 PRG0_PRU1_GPO18/CPSW_RGMII1_MDIO → PRG0_PRU1_GPO18/CPSW_RGMII1_MDIO
- 27 PRG0_PRU1_GPO19/CPSW_RGMII1_MDC → PRG0_PRU1_GPO19/CPSW_RGMII1_MDC

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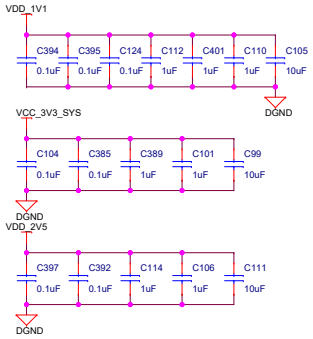
TEXAS INSTRUMENTS MISTRAL

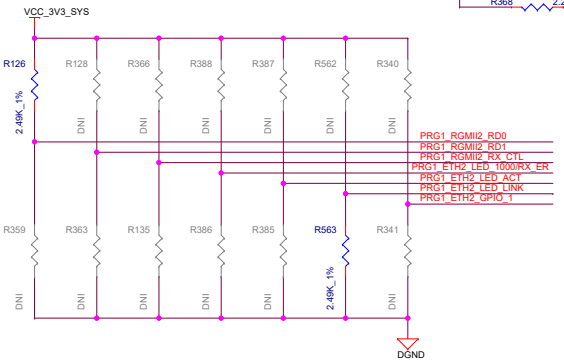
Title	CPSW RGMII_1 ETHERNET PHY	
Size		Rev
C	Variant Name = PROC101E2 TMDS64GPEVM	E2
Date:	Thursday, January 28, 2021	Sheet 16 of 40

ICSSG1 - RGMII 2

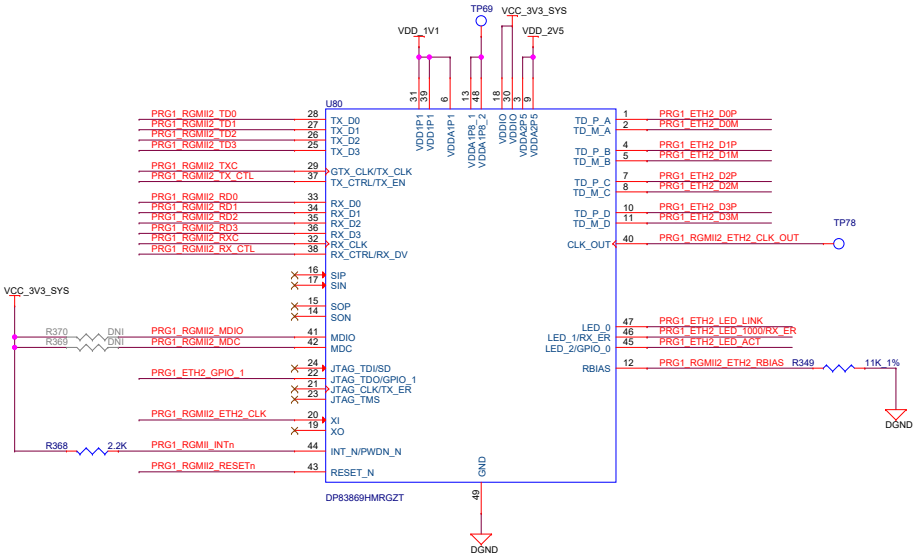
Decaps



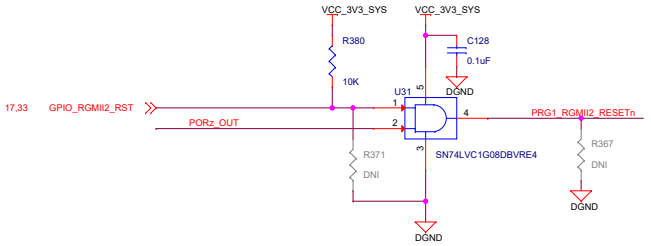
STRAPPING RESISTORS



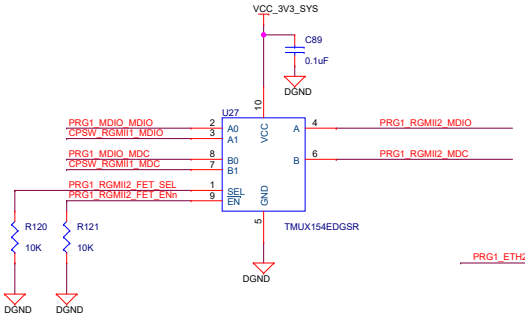
PHY ADDRESS = 00011
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X
RGMII to Copper (1000BaseT/100Base-TX/10Base-Te)



PRG1 ETH2 RESET



PRG1 MDC/MDIO FET SWITCH

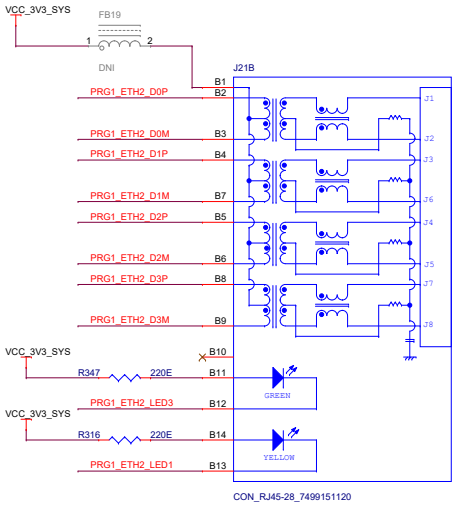


TMUX154EDGSR Truth Table

SEL	$\overline{EN}$	FUNCTION
X	H	Disconnect
L	L	A = A0 B= B0
H	L	A = A1 B = B1

PRG1_ETHERNET - 2 SPEED & ACTIVITY LED 's DRIVERS

Dual RJ45 CON With Integrated Magnetics



Off Page Connections

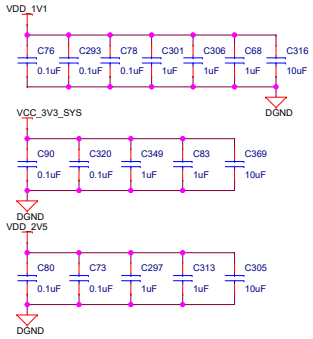
To Processor	16,18,34	PRG1_RGMII_INTn	PRG1_RGMII_INTn
	27	PRG1_RGMII2_RD0	PRG1_RGMII2_RD0
	27	PRG1_RGMII2_RD1	PRG1_RGMII2_RD1
	27	PRG1_RGMII2_RD2	PRG1_RGMII2_RD2
	27	PRG1_RGMII2_RD3	PRG1_RGMII2_RD3
	27	PRG1_RGMII2_RXC	PRG1_RGMII2_RXC
	27	PRG1_RGMII2_RX_CTL	PRG1_RGMII2_RX_CTL
	27	PRG1_ETH2_LED_LINK	PRG1_ETH2_LED_LINK
	27	PRG1_ETH2_LED_1000/RX_ER	PRG1_ETH2_LED_1000/RX_ER
From Processor	27	PRG1_RGMII2_TD0	PRG1_RGMII2_TD0
	27	PRG1_RGMII2_TD1	PRG1_RGMII2_TD1
	27	PRG1_RGMII2_TD2	PRG1_RGMII2_TD2
	27	PRG1_RGMII2_TD3	PRG1_RGMII2_TD3
	27	PRG1_RGMII2_TXC	PRG1_RGMII2_TXC
	27	PRG1_RGMII2_TX_CTL	PRG1_RGMII2_TX_CTL
	13,16,18,20,34	PORz_OUT	PORz_OUT
	18,27	PRG1_MDIO_MDIO	PRG1_MDIO_MDIO
	18,27	PRG1_MDIO_MDC	PRG1_MDIO_MDC
From CPSW SW	16	CPSW_RGMII1_MDIO	CPSW_RGMII1_MDIO
	16	CPSW_RGMII1_MDC	CPSW_RGMII1_MDC
From IO Expander	17,33	GPIO_RGMII2_RST	GPIO_RGMII2_RST
	33	PRG1_RGMII2_FET_SEL	PRG1_RGMII2_FET_SEL
From Clock Buffer	31	PRG1_RGMII2_ETH2_CLK	PRG1_RGMII2_ETH2_CLK

Designed for TI by Mistral Solutions Pvt Ltd

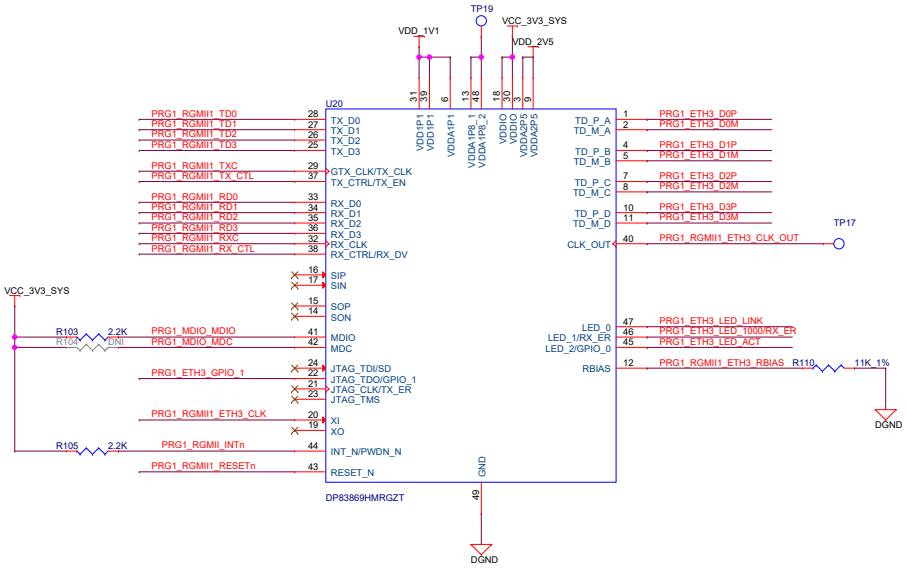
TEXAS INSTRUMENTS MISTRAL

Title	ICSSG1 RGMII_2 ETHERNET PHY	
Size		Rev
C	Variant Name = PROC101E2 TMDS64GPEVM	E2
Date:	Thursday, January 28, 2021	Sheet 17 of 40

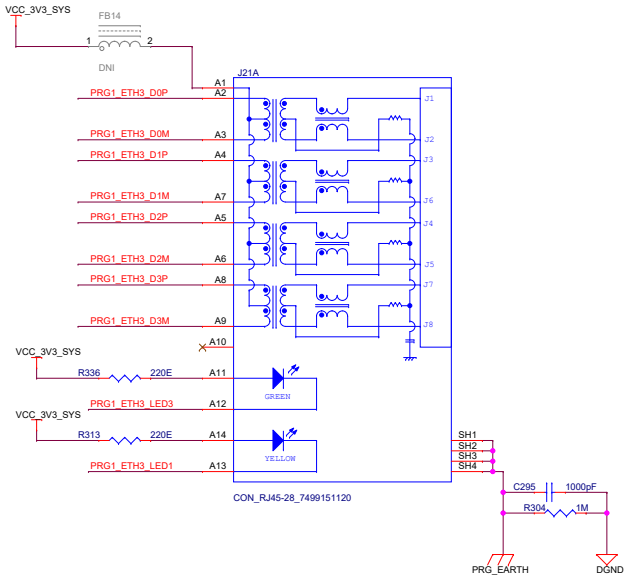
Decaps



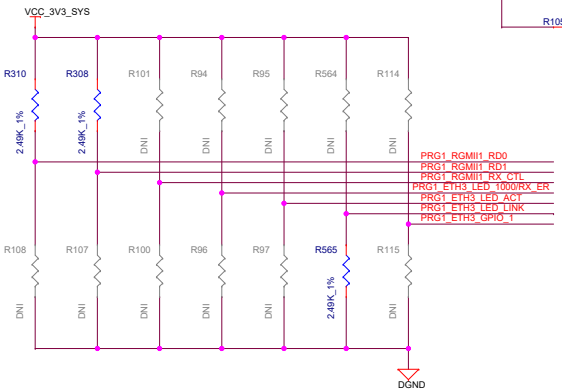
ICSSG1 - RGMII 1



Dual RJ45 CON With Integrated Magnetics

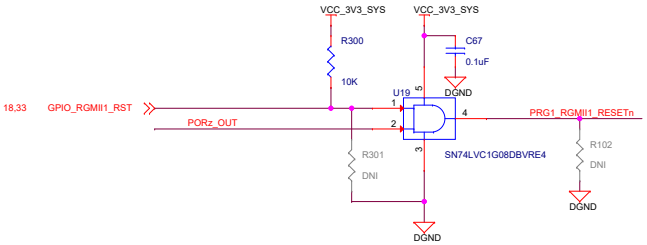


STRAPPING RESISTORS



PHY ADDRESS = 01111
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X
RGMII to Copper (1000BaseT/100Base-TX/10Base-Te)

PRG1 ETH2 RESET



PRG1_ETHERNET - 3 SPEED & ACTIVITY LED 's DRIVERS

Off Page Connections

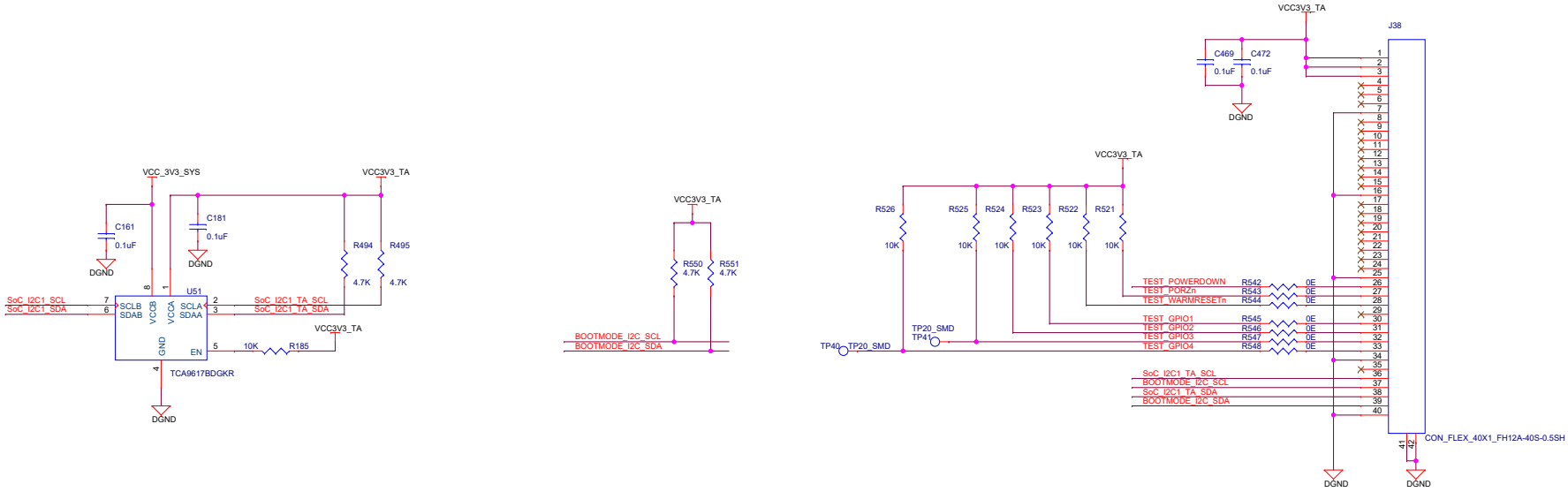
To Processor	16,17,34	PRG1_RGMII_INTn	PRG1_RGMII_INTn
	27	PRG1_RGMII1_RD0	PRG1_RGMII1_RD0
	27	PRG1_RGMII1_RD1	PRG1_RGMII1_RD1
	27	PRG1_RGMII1_RD2	PRG1_RGMII1_RD2
	27	PRG1_RGMII1_RD3	PRG1_RGMII1_RD3
	27	PRG1_RGMII1_RXC	PRG1_RGMII1_RXC
	27	PRG1_RGMII1_RX_CTL	PRG1_RGMII1_RX_CTL
	13,16,17,20,34	PORz_OUT	PORz_OUT
	27	PRG1_ETH3_LED_LINK	PRG1_ETH3_LED_LINK
	27	PRG1_ETH3_LED_1000/RX_ER	PRG1_ETH3_LED_1000/RX_ER
From Processor	27	PRG1_RGMII1_TD0	PRG1_RGMII1_TD0
	27	PRG1_RGMII1_TD1	PRG1_RGMII1_TD1
	27	PRG1_RGMII1_TD2	PRG1_RGMII1_TD2
	27	PRG1_RGMII1_TD3	PRG1_RGMII1_TD3
	27	PRG1_RGMII1_TXC	PRG1_RGMII1_TXC
	27	PRG1_RGMII1_TX_CTL	PRG1_RGMII1_TX_CTL
From Processor (MDC & MDIO Pins are common to both ICSSG PHY, This to be verified)	17,27	PRG1_MDIO_MDIO	PRG1_MDIO_MDIO
	17,27	PRG1_MDIO_MDC	PRG1_MDIO_MDC
From IO Expander	18,33	GPIO_RGMII1_RST	GPIO_RGMII1_RST
From Clock Buffer	31	PRG1_RGMII1_ETH3_CLK	PRG1_RGMII1_ETH3_CLK

Designed for TI by Mistral Solutions Pvt Ltd

Title	ICSSG2 RGMII_1 ETHERNET PHY		
Size	Variant Name = PROC101E2 TMDS64GPEVM		Rev
C			E2
Date:	Thursday, January 28, 2021	Sheet	18 of 40

TEST AUTOMATION

40-PIN AUTOMATION HEADER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO0_13_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to I/O Expander to Communicate with SoC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

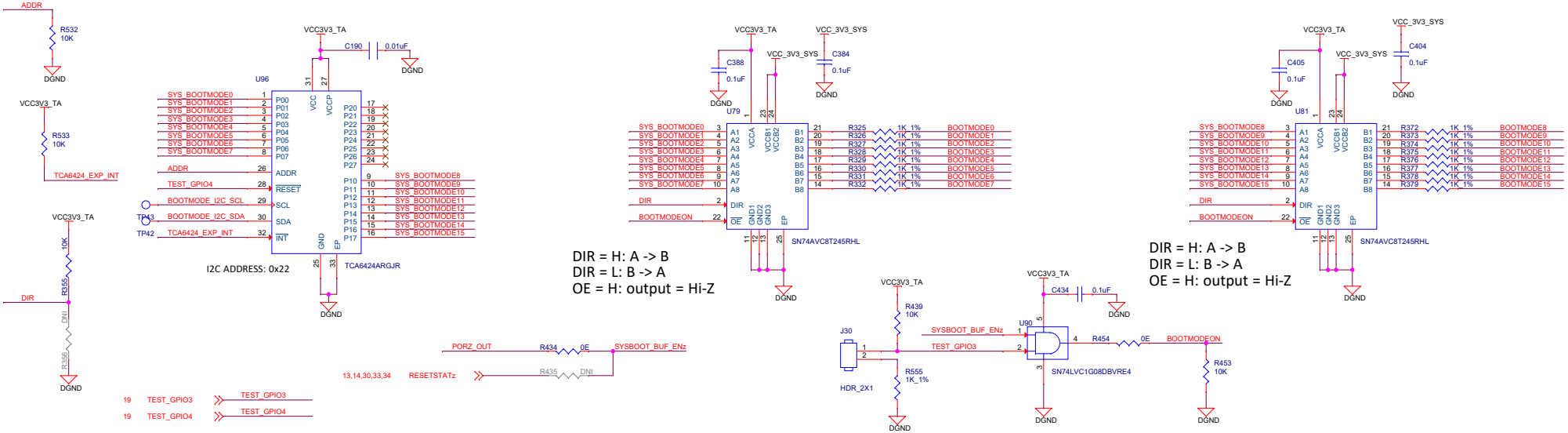
Off Page Connections

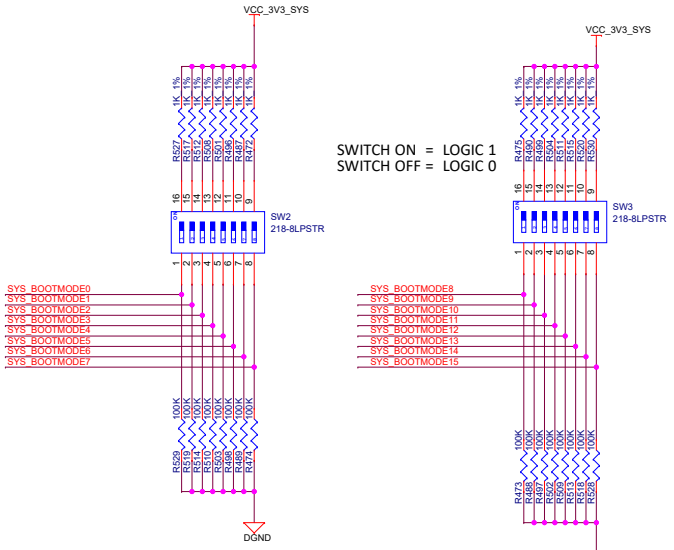
To Processor	15,21,29,30,32,33 SoC_I2C1_SCL 15,21,29,30,32,33 SoC_I2C1_SDA	SoC_I2C1_SCL SoC_I2C1_SDA
To Bootmode Buffer	20 BOOTMODE_I2C_SCL 20 BOOTMODE_I2C_SDA	BOOTMODE_I2C_SCL BOOTMODE_I2C_SDA
To Debounce Ckt	35 TEST_PORZn	TEST_PORZn
To High Side SW	37 TEST_POWERDOWN	TEST_POWERDOWN
To Debounce Ckt	35 TEST_WARMRESETn	TEST_WARMRESETn
To Debounce Ckt	35 TEST_GPIO1	TEST_GPIO1
To IO Expander	33 TEST_GPIO2	TEST_GPIO2
To EN Boot Mode Buffer	20 TEST_GPIO3	TEST_GPIO3
To RST Boot Mode Buffer	20 TEST_GPIO4	TEST_GPIO4

Designed for TI by Mistral Solutions Pvt Ltd

Title	TEST AUTOMATION	
Size C	Variant Name = PROC101E2 TMDS64GPEVM	Rev E2
Date: Thursday, January 28, 2021	Sheet 19 of 40	

BOOT MODE BUFFER & SWITCHES





BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. MMC0 - eMMC
4. CPSW Ethernet Slave
5. USB Host
6. USB Device
7. UART
8. Ethernet

Off Page Connections

From Processor

28	BOOTMODE0
28	BOOTMODE1
28	BOOTMODE2
28	BOOTMODE3
28	BOOTMODE4
28	BOOTMODE5
28	BOOTMODE6
28	BOOTMODE7
28	BOOTMODE8
28	BOOTMODE9
28	BOOTMODE10
28	BOOTMODE11
28	BOOTMODE12
28	BOOTMODE13
28	BOOTMODE14
28	BOOTMODE15
13,16,17,18,34	PORz_OUT

From Test Automation Header

19	BOOTMODE_I2C_SCL
19	BOOTMODE_I2C_SDA

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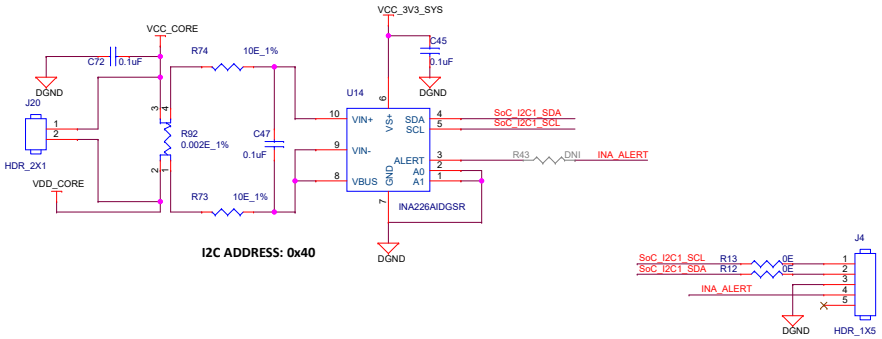
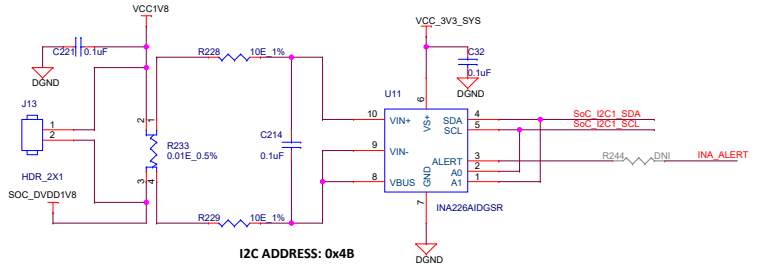
Title	BOOT MODE BUFFER & SWITCHES	
Size C	Variant Name = PROC101E2 TMDS64GPEVM	Rev E2
Date: Thursday, January 28, 2021	Sheet 20 of 40	

CURRENT MONITORING DEVICES

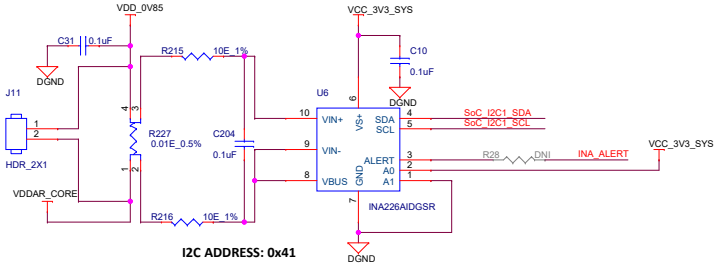
VDD_CORE



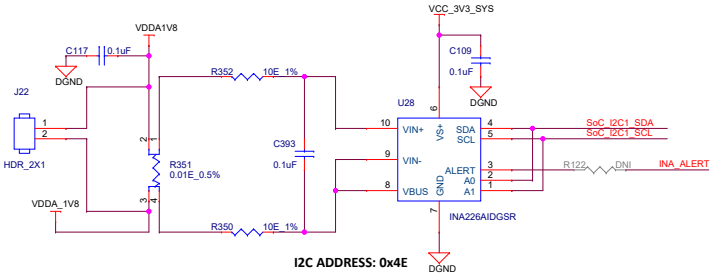
SoC_DVDD1V8



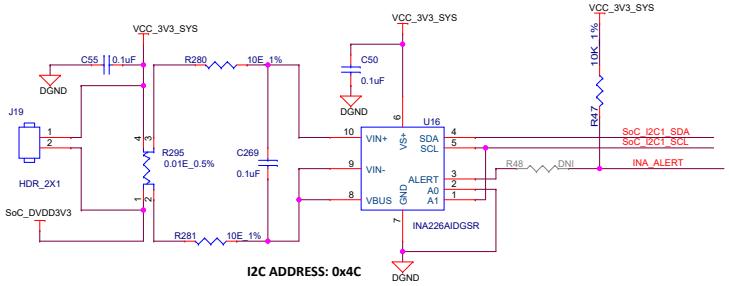
VDDAR_CORE



VDDA_1V8

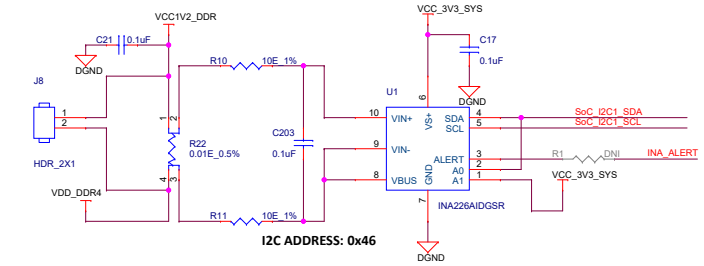


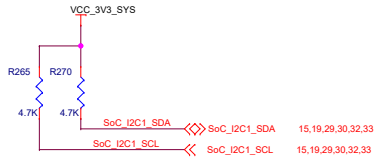
SoC_DVDD3V3



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VDD_0V85	VDDAR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8	SoC_DVDD1V8	4B
VDDA1V8	VDDA_1V8	4E
VCC1V2_DDR	VDD_DDR4	46

VDD_DDR4



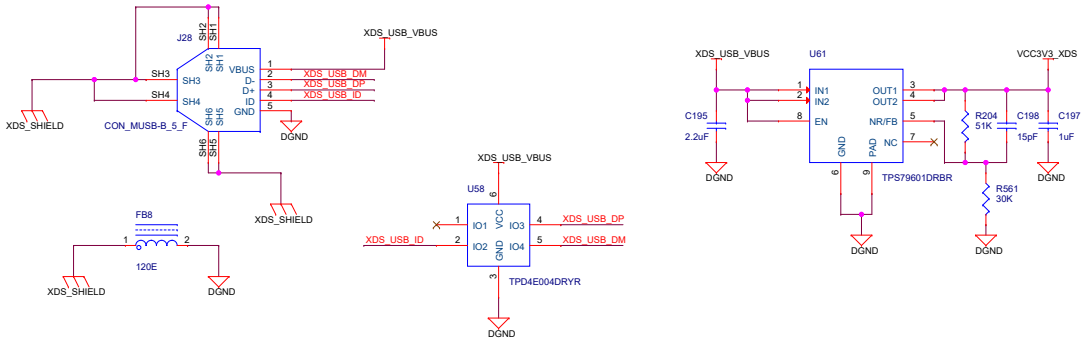


Designed for TI by Mistral Solutions Pvt Ltd

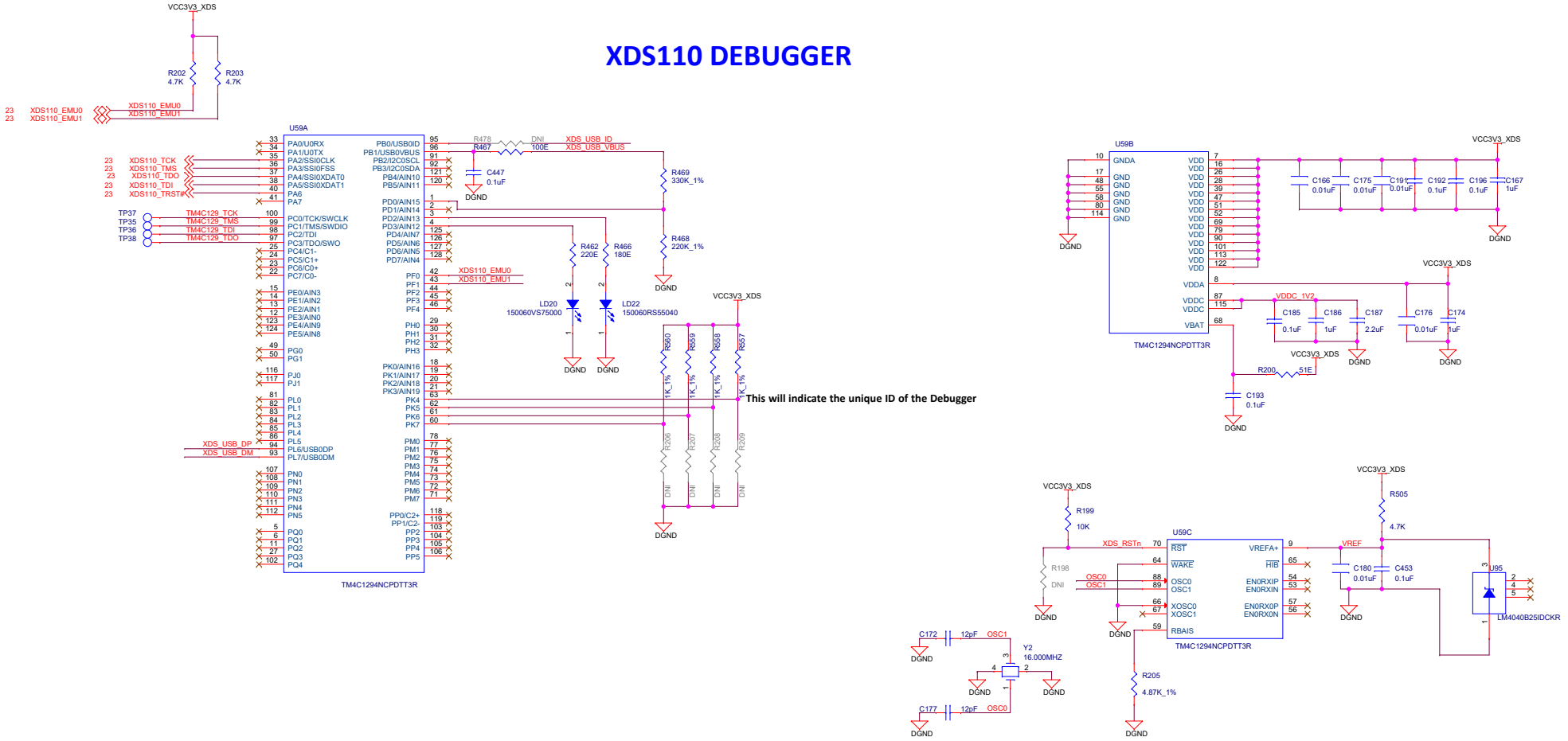
Title	CURRENT MONITORING DEVICES	
Size C	Variant Name = PROC101E2 TMDS64GPEVM	Rev E2
Date: Thursday, January 28, 2021	Sheet 21 of 40	

XDS110 POWER

USB Connector



XDS110 DEBUGGER



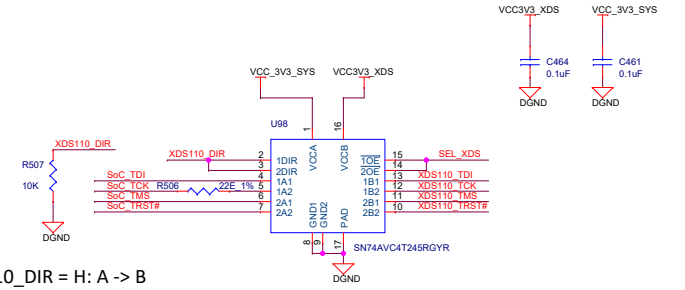
Designed for TI by Mistral Solutions Pvt Ltd

Title	XDS110 DEBUGGER	
Size	Variant Name = PROC101E2 TMDS64GPEVM	Rev
C		E2
Date: Thursday, January 28, 2021	Sheet 22 of 40	

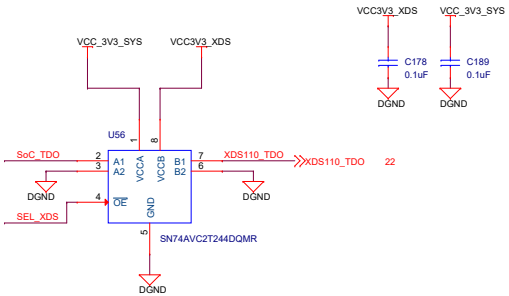
JTAG BUFFER

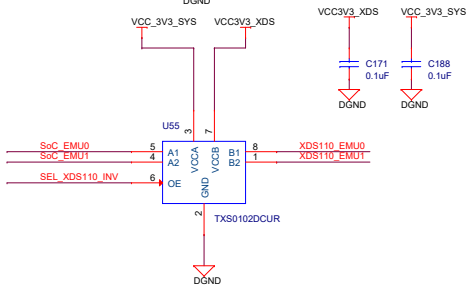
JTAG SoC SECTION

BUFFER XDS110

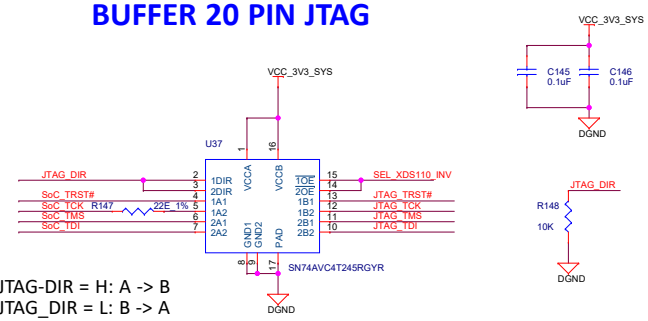


XDS110_DIR = H: A -> B
XDS110_DIR = L: B -> A
OE = H: output = Hi-Z

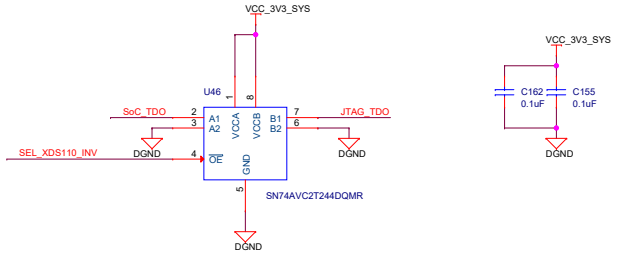


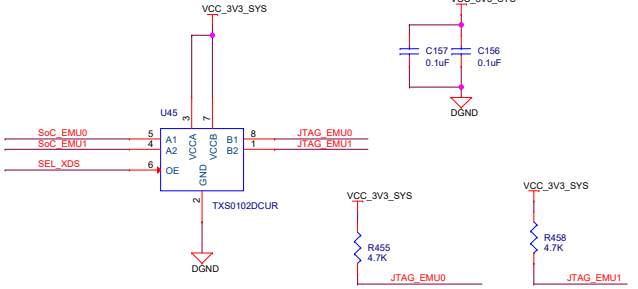


BUFFER 20 PIN JTAG



JTAG-DIR = H: A -> B
JTAG_DIR = L: B -> A
OE = H: output = Hi-Z





Off Page Connections

From XDS1100 Debugger

24	SEL_XDS110_INV	SEL_XDS110_INV
24	JTAG_EMU0	JTAG_EMU0
24	JTAG_EMU1	JTAG_EMU1
22	XDS110_TDI	XDS110_TDI
22	XDS110_TCK	XDS110_TCK
22	XDS110_TMS	XDS110_TMS
22	XDS110_TRST#	XDS110_TRST#
24	JTAG_TDI	JTAG_TDI
24	JTAG_TCK	JTAG_TCK
24	JTAG_TMS	JTAG_TMS
24	JTAG_TRST#	JTAG_TRST#
24	JTAG_TDO	JTAG_TDO
22	XDS110_EMU0	XDS110_EMU0
22	XDS110_EMU1	XDS110_EMU1

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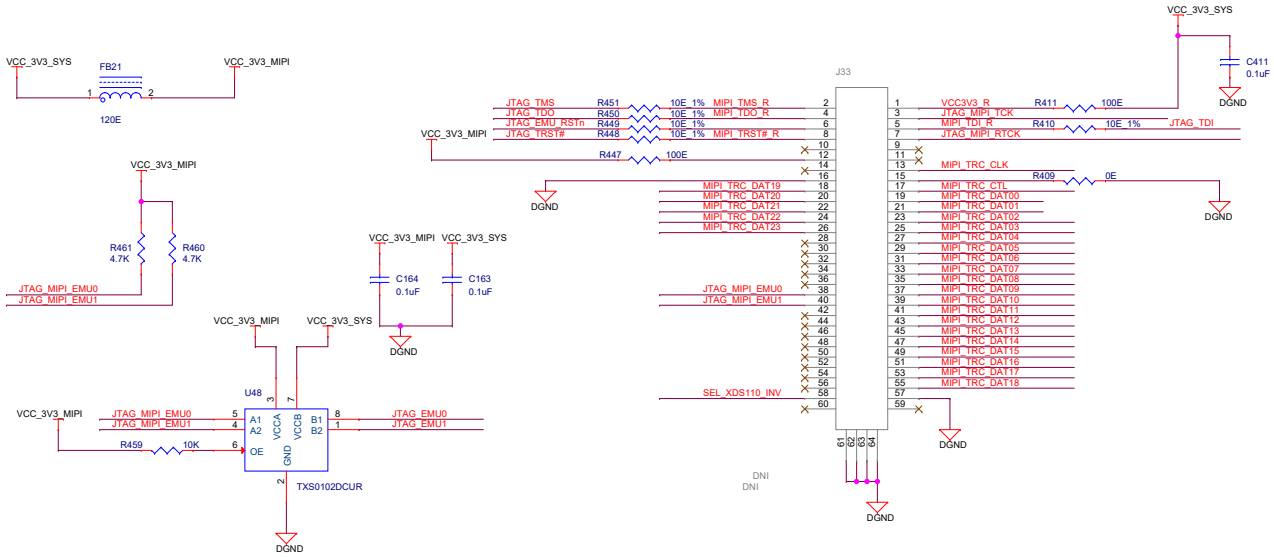
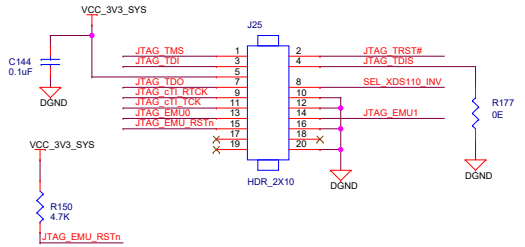
Title	JTAG BUFFER	
Size	Variant Name = PROC101E2 TMDS64GPEVM	Rev
C		E2
Date:	Thursday, January 28, 2021	Sheet 23 of 40

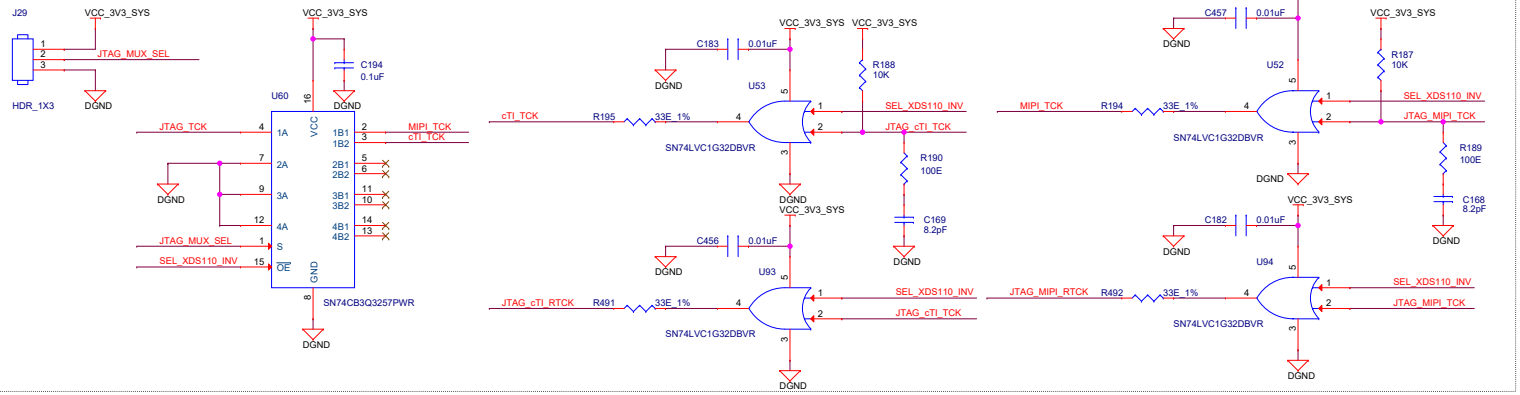
MIPI 60 PIN CONNECTOR



JTAG 20 PIN cTI CONNECTOR



JTAG CLOCK BUFFER



Off Page Connections

From JTAG Buffer

23 SEL_XDS110_INV — SEL_XDS110_INV
23 JTAG_TDO — JTAG_TDO
23 JTAG_EMU0 — JTAG_EMU0
23 JTAG_EMU1 — JTAG_EMU1
23 JTAG_TDI — JTAG_TDI
23 JTAG_TCK — JTAG_TCK
23 JTAG_TMS — JTAG_TMS
23 JTAG_TRST# — JTAG_TRST#
35 JTAG_EMU_RSTn — JTAG_EMU_RSTn

From SoC GPMC

28 MIPI_TRC_DAT05 — MIPI_TRC_DAT05
28 MIPI_TRC_DAT04 — MIPI_TRC_DAT04
28 MIPI_TRC_DAT03 — MIPI_TRC_DAT03
28 MIPI_TRC_DAT02 — MIPI_TRC_DAT02
28 MIPI_TRC_DAT01 — MIPI_TRC_DAT01
28 MIPI_TRC_DAT00 — MIPI_TRC_DAT00
28 MIPI_TRC_CTL — MIPI_TRC_CTL
28 MIPI_TRC_CLK — MIPI_TRC_CLK

28 MIPI_TRC_DAT11 — MIPI_TRC_DAT11
28 MIPI_TRC_DAT10 — MIPI_TRC_DAT10
28 MIPI_TRC_DAT09 — MIPI_TRC_DAT09
28 MIPI_TRC_DAT13 — MIPI_TRC_DAT13
28 MIPI_TRC_DAT12 — MIPI_TRC_DAT12
28 MIPI_TRC_DAT08 — MIPI_TRC_DAT08
28 MIPI_TRC_DAT07 — MIPI_TRC_DAT07
28 MIPI_TRC_DAT06 — MIPI_TRC_DAT06

28 MIPI_TRC_DAT21 — MIPI_TRC_DAT21
28 MIPI_TRC_DAT20 — MIPI_TRC_DAT20
28 MIPI_TRC_DAT19 — MIPI_TRC_DAT19
28 MIPI_TRC_DAT18 — MIPI_TRC_DAT18
28 MIPI_TRC_DAT17 — MIPI_TRC_DAT17
28 MIPI_TRC_DAT16 — MIPI_TRC_DAT16
28 MIPI_TRC_DAT15 — MIPI_TRC_DAT15
28 MIPI_TRC_DAT14 — MIPI_TRC_DAT14

28 MIPI_TRC_DAT23 — MIPI_TRC_DAT23
28 MIPI_TRC_DAT22 — MIPI_TRC_DAT22

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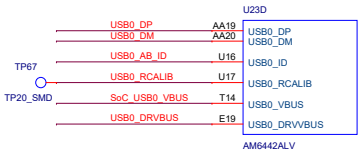
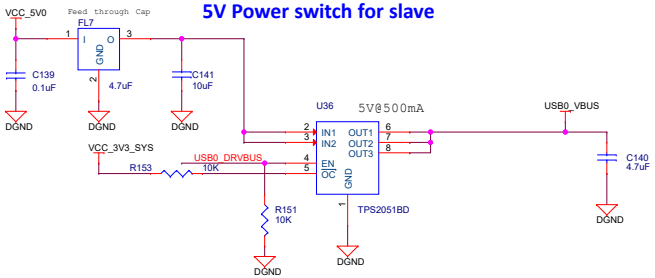
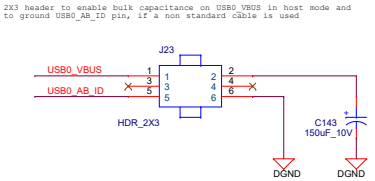
Title	MIPI 60 PIN CONNECTOR	
Size C	Variant Name = PROC101E2 TMDS64GPEVM	Rev E2
Date: Thursday, January 28, 2021	Sheet 24 of 40	

USB 2.0 INTERFACE

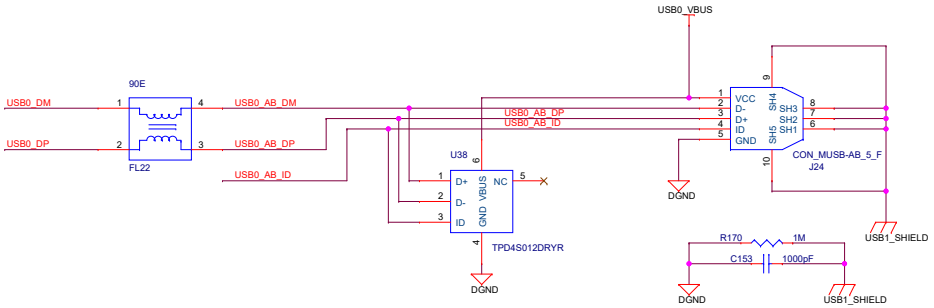


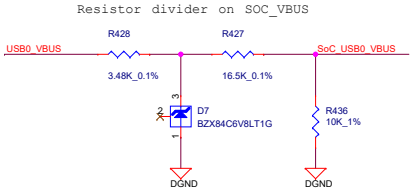
5V Power switch for slave





Micro USB 2.0 AB Connector





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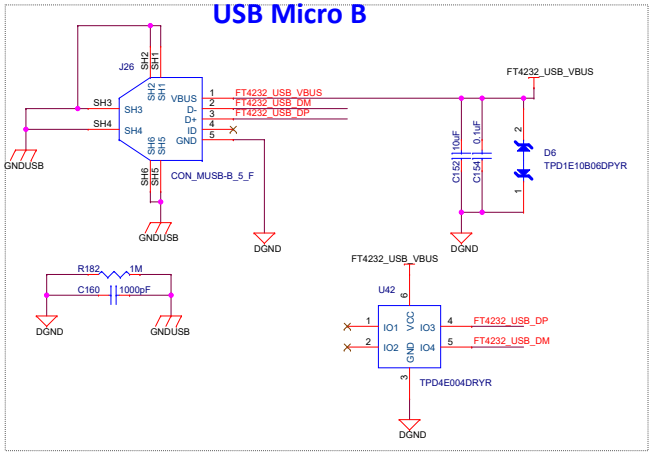
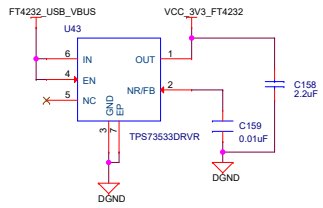
Title	USB 2.0 INTERFACE	
Size: C	Variant Name = PROC101E2 TMDS64GPEVM	Rev: E2
Date: Thursday, January 28, 2021	Sheet 25 of 40	

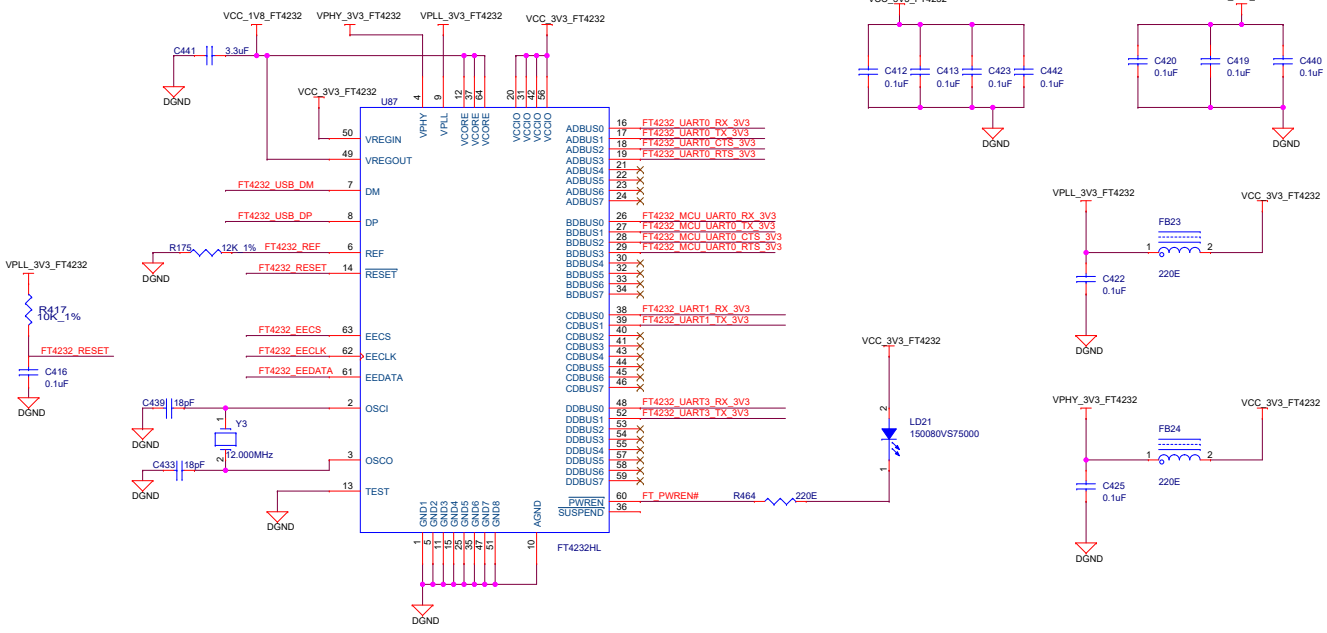
FT4232 UART

USB Micro B

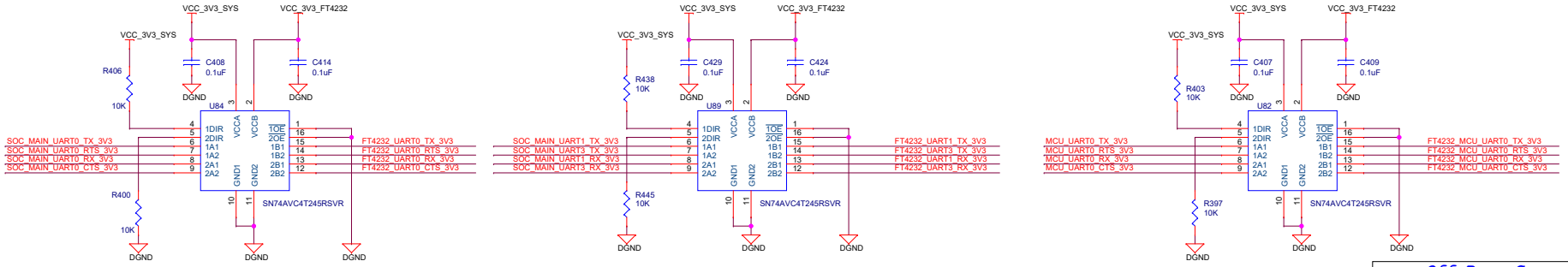


FT4232: 5V to 3.3V@500mA LDO

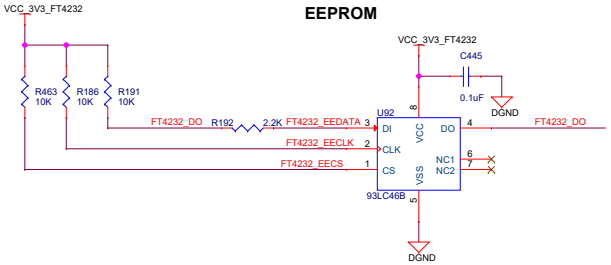




FT4232 LEVEL TRANSLATOR



EEPROM



Off Page Connections

SOC_MAIN_UART0_RX_3V3 → SOC_MAIN_UART0_RX_3V3 29
SOC_MAIN_UART0_TX_3V3 → SOC_MAIN_UART0_TX_3V3 29
SOC_MAIN_UART0_RTS_3V3 → SOC_MAIN_UART0_RTS_3V3 29
SOC_MAIN_UART0_CTS_3V3 → SOC_MAIN_UART0_CTS_3V3 29

MCU_UART0_RX_3V3 → MCU_UART0_RX_3V3 34
MCU_UART0_TX_3V3 → MCU_UART0_TX_3V3 34
MCU_UART0_RTS_3V3 → MCU_UART0_RTS_3V3 34
MCU_UART0_CTS_3V3 → MCU_UART0_CTS_3V3 34

SOC_MAIN_UART1_RX_3V3 → SOC_MAIN_UART1_RX_3V3 29
SOC_MAIN_UART1_TX_3V3 → SOC_MAIN_UART1_TX_3V3 29
SOC_MAIN_UART3_TX_3V3 → SOC_MAIN_UART3_TX_3V3 29
SOC_MAIN_UART3_RX_3V3 → SOC_MAIN_UART3_RX_3V3 29

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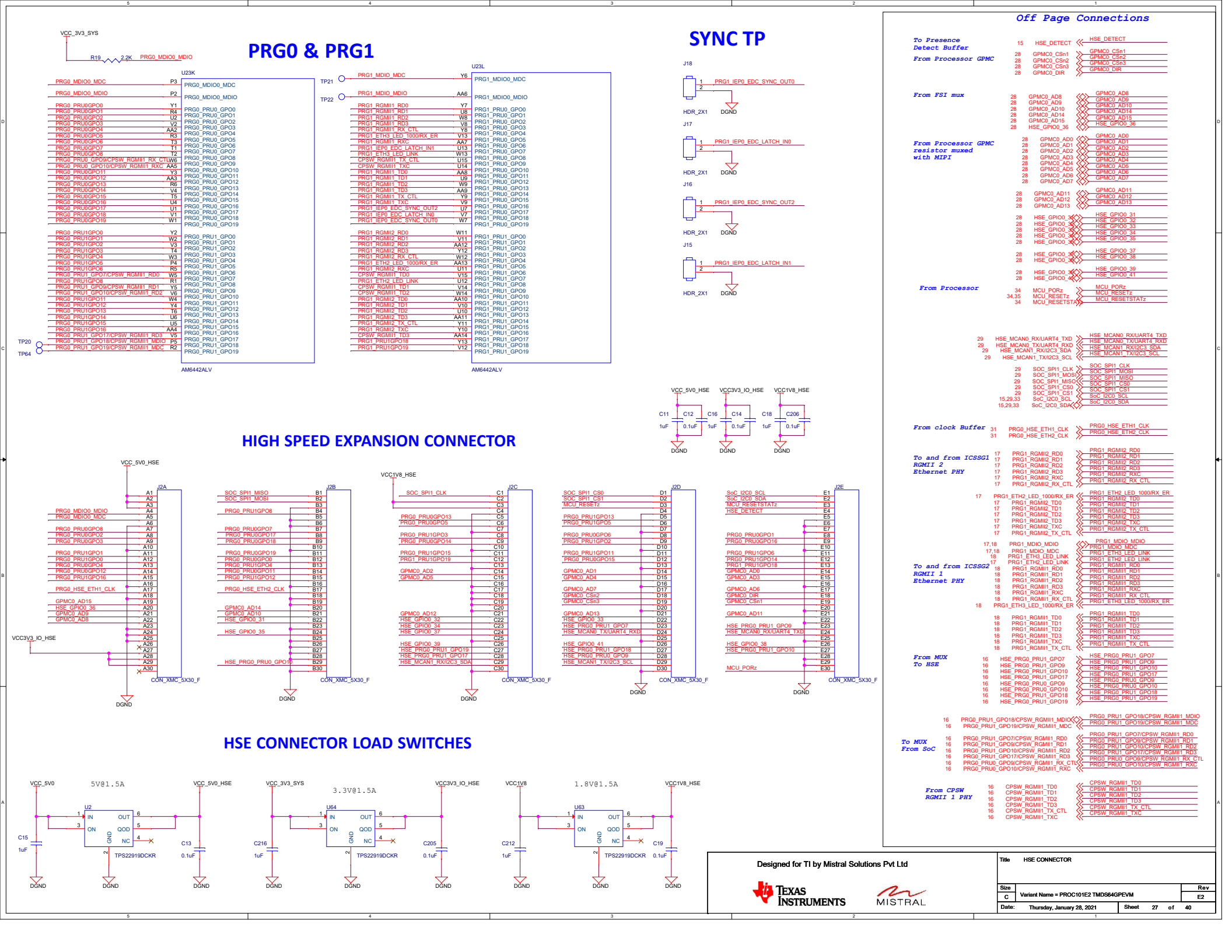
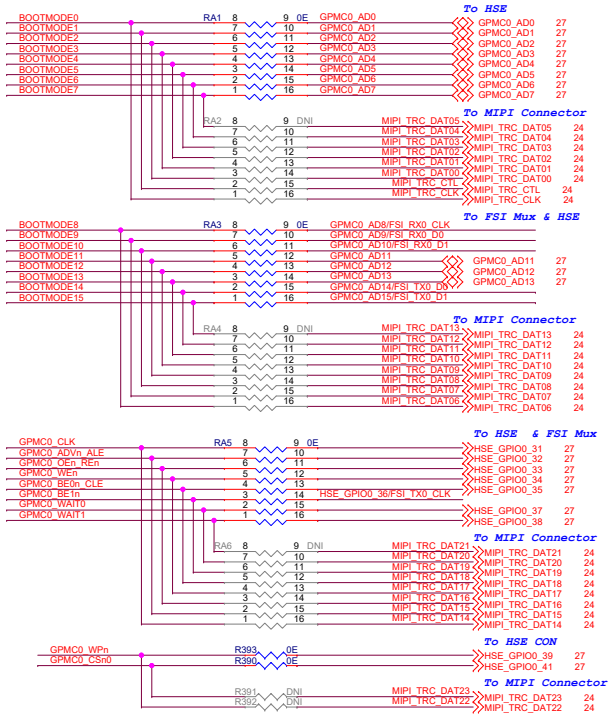
TEXAS INSTRUMENTS MISTRAL

Title	FT4232 UART TO USB BRIDGE	
Size	Variant Name = PROC101E2 TMDS64GPEVM	Rev
C		E2
Date: Thursday, January 28, 2021	Sheet 26 of 40	

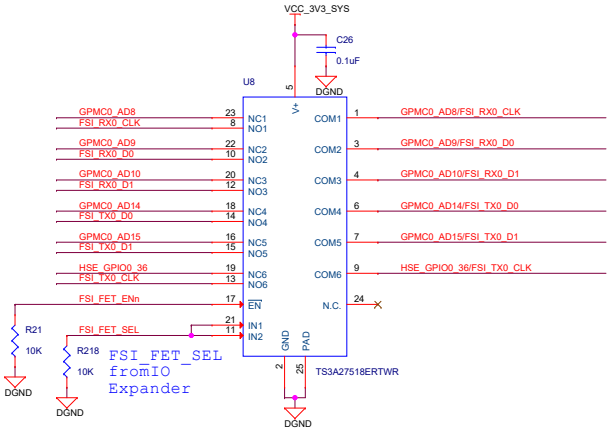

PRG0 & PRG1
SYNC TP
HIGH SPEED EXPANSION CONNECTOR
HSE CONNECTOR LOAD SWITCHES
Off Page Connections
AM6442ALV
CON_XMC_5X30_F
TPS22919DCKR
5V@1.5A
3.3V@1.5A
1.8V@1.5A
Designed for TI by Mistral Solutions Pvt Ltd
TEXAS INSTRUMENTS
MISTRAL
Title HSE CONNECTOR
Size C
Variant Name = PROC101E2 TMDS64GPEVM
Rev E2
Date: Thursday, January 28, 2021
Sheet 27 of 40

GPMC

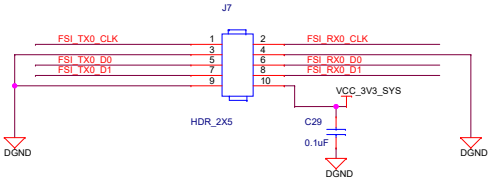
0- Ohm Res MUX between HSE Connector and TRACE Funct i onality
-For HSE Connector RA1 , RA3 , RA5 , R393 & R390 Should be installed and RA2, RA4 ,RA6 , R391& R392 Should be DNI'd.
-For TRACE RA2, RA4 ,RA6 , R391& R392 Should be Installed and RA1 , RA3 , RA5 , R393 & R390 Should be DNI'd.



GPMC TO FSI & HSE CONNECTOR



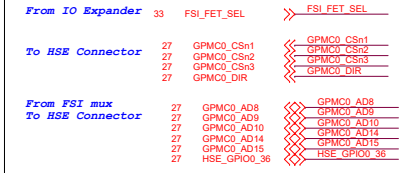
FSI CONNECTOR



TS3A27518ERTWR Truth Table

EN#	IN1	IN2	NC1/2/3 TO COM1/2/3 & COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM14/5/6 & COM4/5/6 TO NC4/5/6	NO1/2/3 TO COM1/2/3 & COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM14/5/6 & COM4/5/6 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

Off Page Connections



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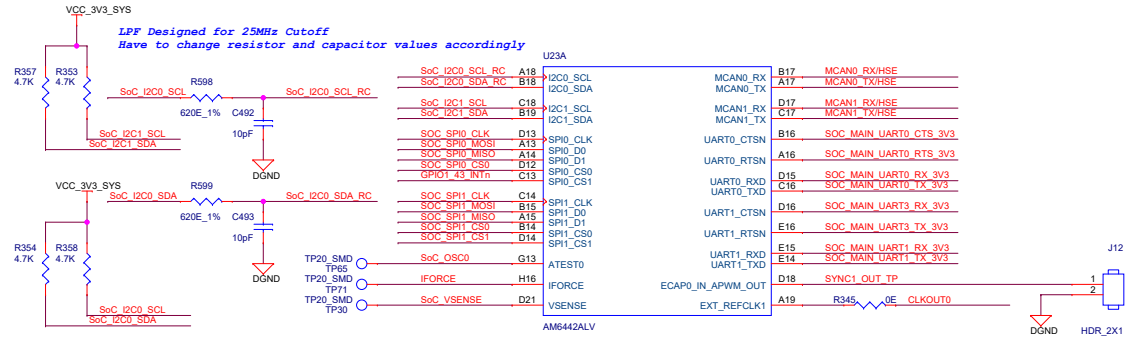
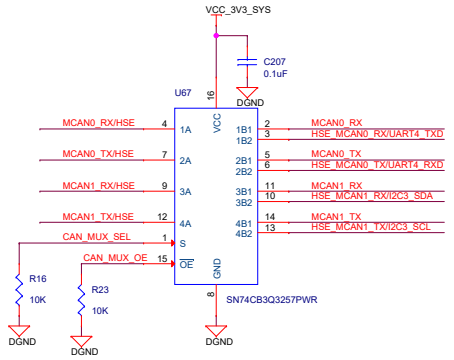
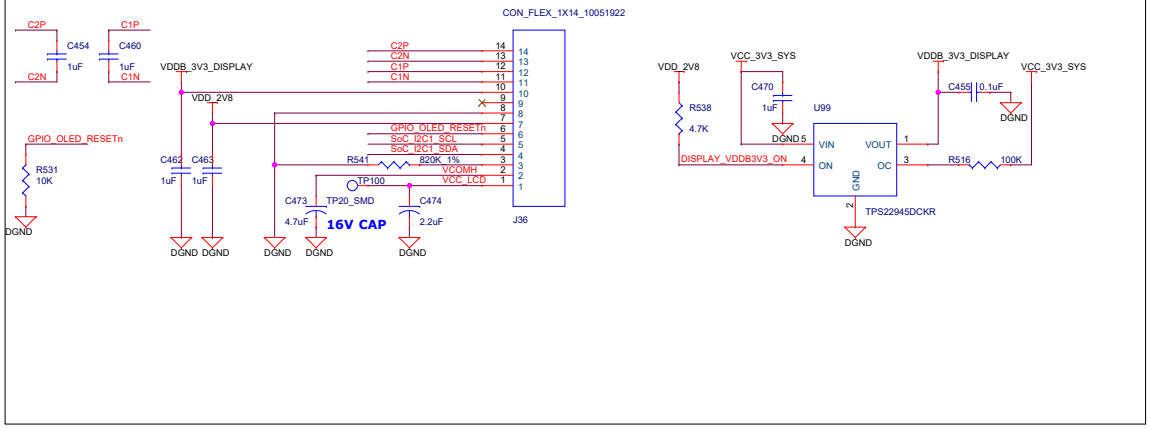
Title	GPMC	
Size C	Variant Name = PROC101E2 TMDS64GPEVM	Rev E2
Date: Thursday, January 28, 2021	Sheet 28 of 40	



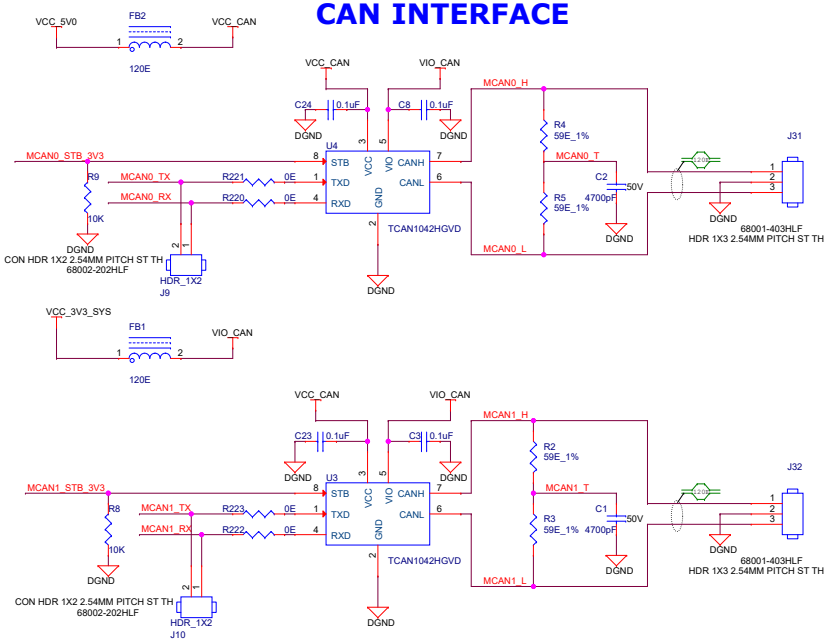
HSE/CAN MUX



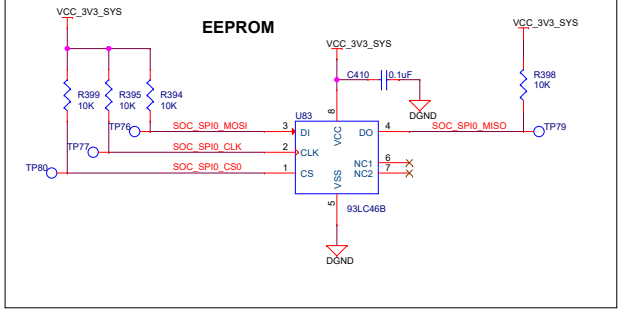
DISPLAY CONNECTOR



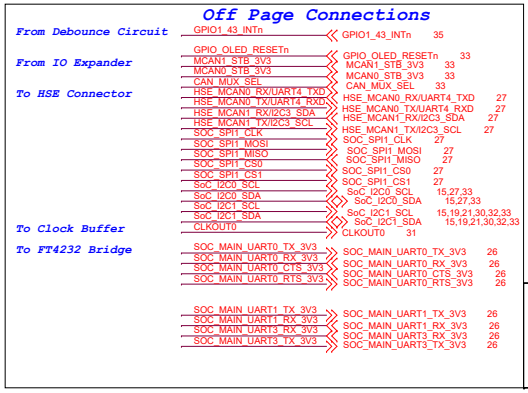
CAN INTERFACE



SPI EEPROM



Off Page Connections



Project :

<Project Name>

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TEXAS INSTRUMENTS

MISTRAL

Title: CAN & DISPLAY INTERFACE

Size	Document Number	Rev
C	MS_TI_MAXIE_APPLICATION_CARD_SCH_REVA	E2
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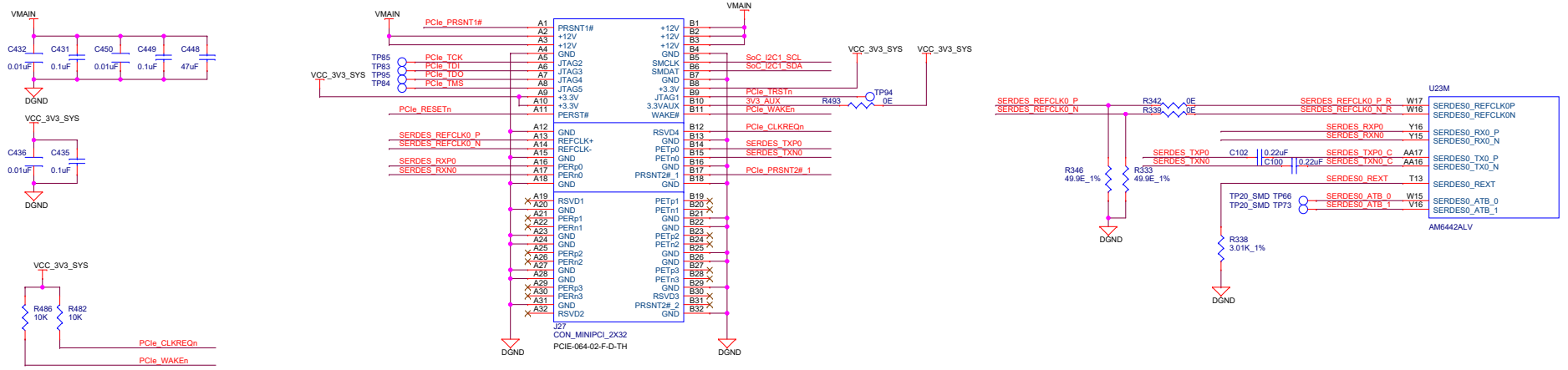
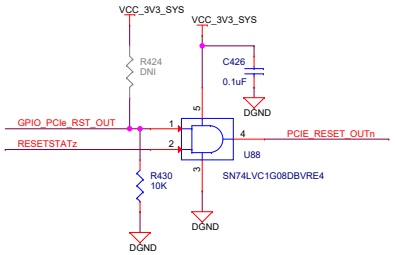
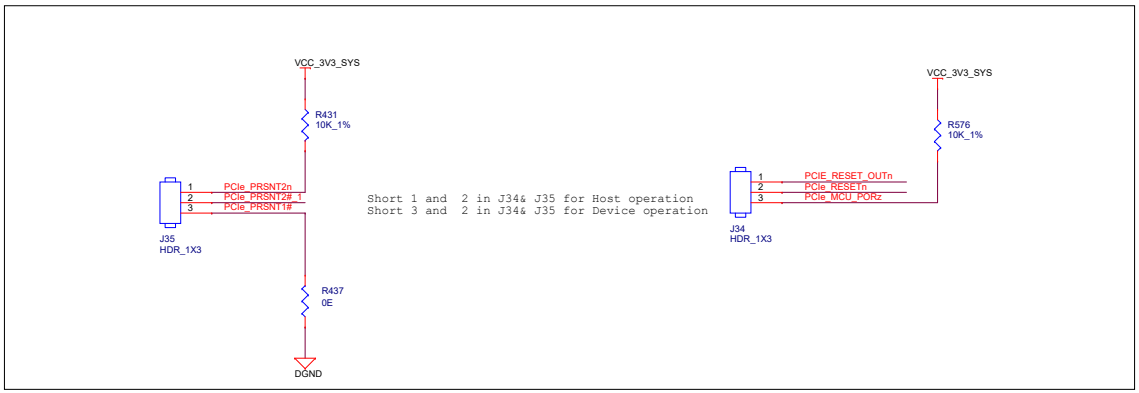
x4 Lane PCIe Connector



PCIe Reset



RC OR EP MODE SELECTION



Off Page Connections

PCIe_MCU_PORz	PCIe_MCU_PORz	34
GPIO_PCIe_RST_OUT	GPIO_PCIe_RST_OUT	33
RESETSTATz	RESETSTATz	13,14,20,33,34
SoC_I2C1_SCL	SoC_I2C1_SCL	15,19,21,29,32,33
SoC_I2C1_SDA	SoC_I2C1_SDA	15,19,21,29,32,33

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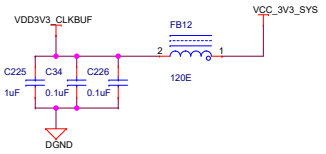
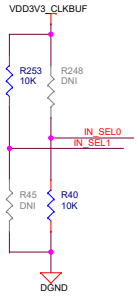
TEXAS INSTRUMENTS MISTRAL

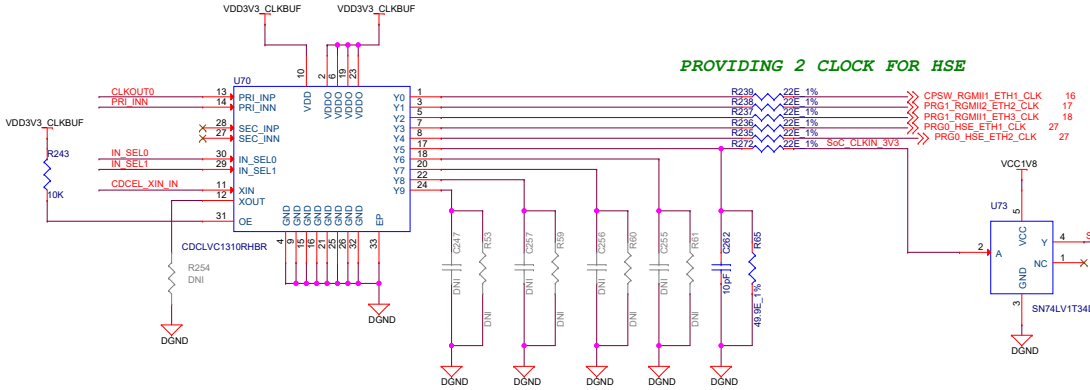
Title	PCIe INTERFACE	
Size C	PROC101E2 TMDS64GPEVM	Rev E2
Date: Thursday, January 28, 2021	Sheet 30 of 40	

ETHERNET PHY CLOCK BUFFER

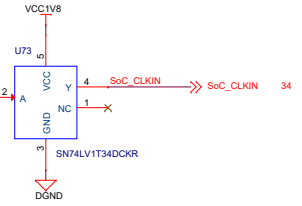


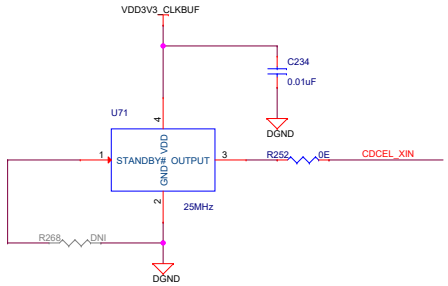
REFERENCE INPUT SELECTION



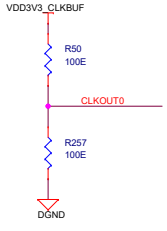


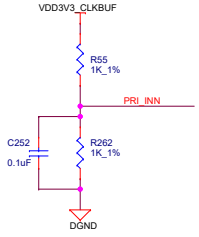
PROVIDING 2 CLOCK FOR HSE

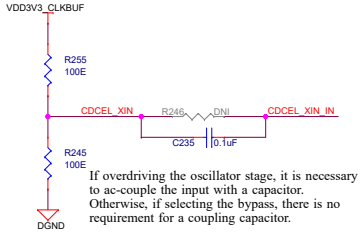




Floating Standby pin enables the oscillator
R268 can be removed to enable the oscillator







If overdriving the oscillator stage, it is necessary to ac-couple the input with a capacitor. Otherwise, if selecting the bypass, there is no requirement for a coupling capacitor.

Off Page Connections

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Title	ETHERNET PHY CLOCK GENERATOR	
Size: C	Variant Name = PROC101E2 TMDS64GPEVM	Rev: E2
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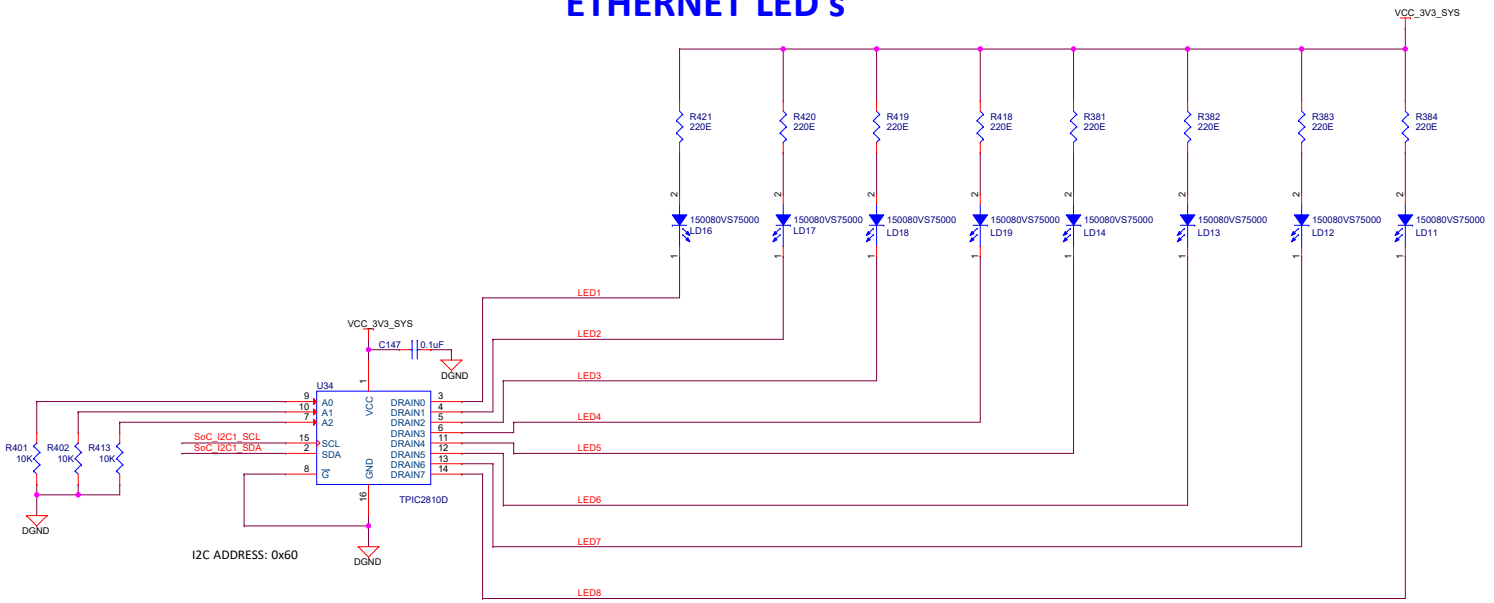
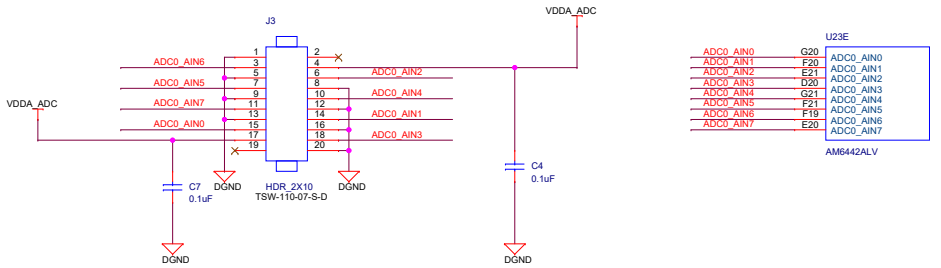
ETHERNET LED's



ADC CONNECTOR



Off Page Connections

SoC_I2C1_SCL — SoC_I2C1_SCL 15,19,21,29,30,33
SoC_I2C1_SDA — SoC_I2C1_SDA 15,19,21,29,30,33

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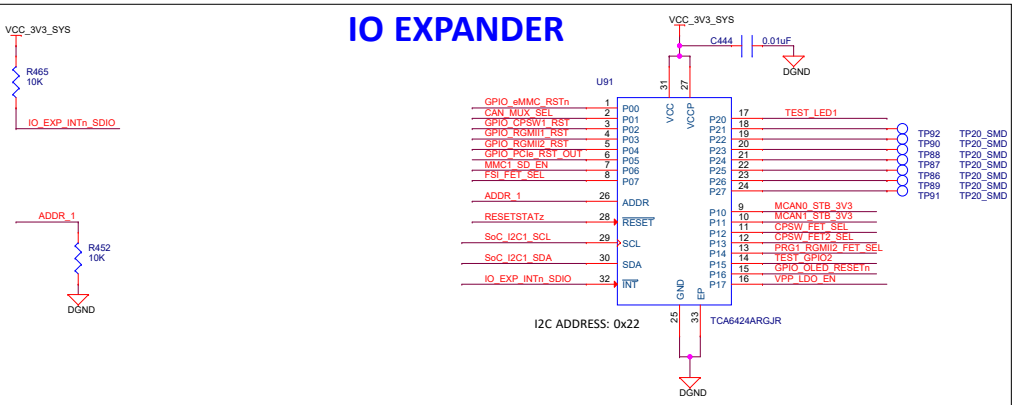
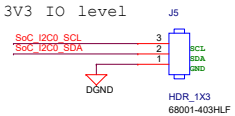
TEXAS INSTRUMENTS MISTRAL

Title	ETHERNET LEDs	
Size	Variant Name = PROC101E2 TMDS64GPEVM	Rev
C		E2
Date: Thursday, January 28, 2021	Sheet 32 of 40	

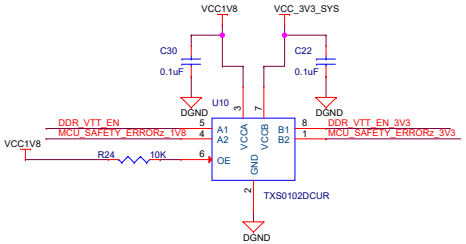
IO EXPANDER



I2C TEST HEADER



LEVEL TRANSLATOR



Off Page Connections

GPIO_eMMC_RSTn → GPIO_eMMC_RSTn 13
GPIO_PCIe_RST_OUT → GPIO_PCIe_RST_OUT 30
GPIO_CPSW1_RST → GPIO_CPSW1_RST 16
GPIO_RGMII1_RST → GPIO_RGMII1_RST 18
GPIO_RGMII2_RST → GPIO_RGMII2_RST 17

MMC1_SD_EN → MMC1_SD_EN 13
FSI_FET_SEL → FSI_FET_SEL 28

MCAN1_STB_3V3 → MCAN1_STB_3V3 29
MCAN0_STB_3V3 → MCAN0_STB_3V3 29
CPSW_FET_SEL → CPSW_FET_SEL 16
CPSW_FET2_SEL → CPSW_FET2_SEL 16
PRG1_RGMII2_FET_SEL → PRG1_RGMII2_FET_SEL 17
TEST_GPIO2 → TEST_GPIO2 19
GPIO_OLED_RESETn → GPIO_OLED_RESETn 29
VPP_LDO_EN → VPP_LDO_EN 38

CAN_MUX_SEL → CAN_MUX_SEL 29
TEST_LED1 → TEST_LED1 14

RESETSTATz → RESETSTATz 13,14,20,30,34

SoC_I2C1_SDA → SoC_I2C1_SDA 15,19,21,29,30,32
SoC_I2C1_SCL → SoC_I2C1_SCL 15,19,21,29,30,32

SoC_I2C0_SDA → SoC_I2C0_SDA 15,27,29
SoC_I2C0_SCL → SoC_I2C0_SCL 15,27,29

From Safety Connector: MCU_SAFETY_ERRORz_3V3 → MCU_SAFETY_ERRORz_3V3 34

From SoC OSPI Section: DDR_VTT_EN → DDR_VTT_EN 14

To Processor, *To VTT Reg*, *To SoC MMC*:
MCU_SAFETY_ERRORz_1V8 → MCU_SAFETY_ERRORz_1V8 34
DDR_VTT_EN_3V3 → DDR_VTT_EN_3V3 39
IO_EXP_INTn_SDIO → IO_EXP_INTn_SDIO 13

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TEXAS INSTRUMENTS

MISTRAL

Title	IO EXPANDER	
Size: C	Variant Name = PROC101E2 TMDS64GPEVM	Rev: E2
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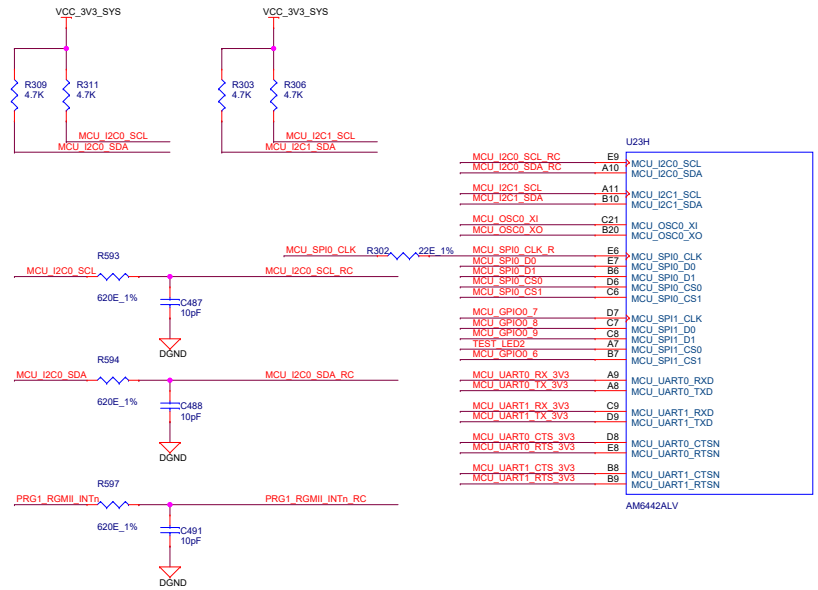
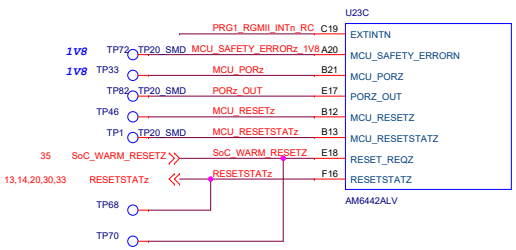
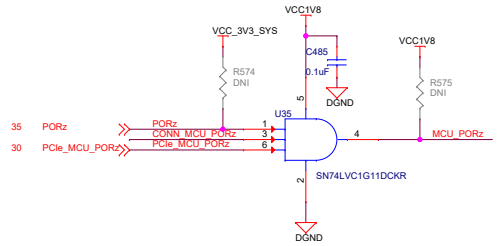
MCU_GENERAL

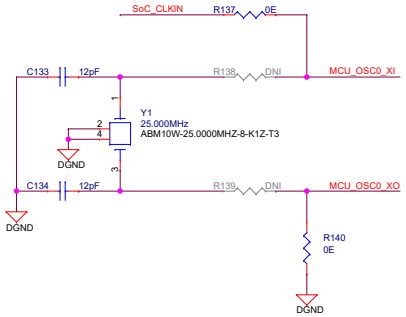


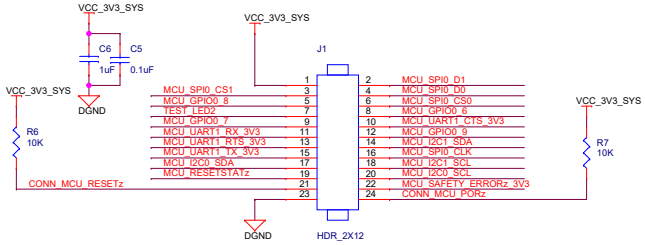


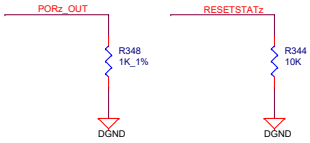


SAFETY CONNECTOR

LPF Designed for 25MHz Cutoff
Have to change resistor and capacitor values accordingly

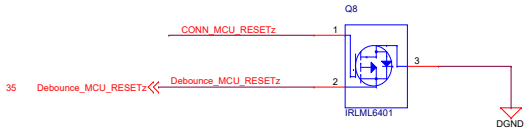


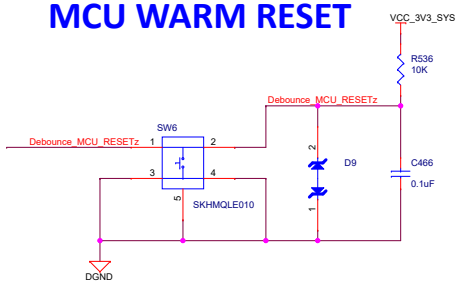




pull-down resistor on PORz_OUT is provided to keep the signal low until the processor is released from reset during the power-up seqence

MCU WARM RESET





Off Page Connections

To HSE Connector	MCU_PORz	MCU_PORz 27
	MCU_RESETz	MCU_RESETz 27,35
	MCU_RESETSTATz	MCU_RESETSTATz 27
To level translator From Level Translator	MCU_SAFETY_ERRORz_3V3	MCU_SAFETY_ERRORz_3V3 33
	MCU_SAFETY_ERRORz_1V8	MCU_SAFETY_ERRORz_1V8 33
To Boot Mode Section	PORz_OUT	PORz_OUT 13,16,17,18,20
From ICSSG Phy1&2	PRG1_RGMII_INTn	PRG1_RGMII_INTn 16,17,18
To User LED From Push button Switch	TEST_LED2	TEST_LED2 14
	MCU_GPIO0_6	MCU_GPIO0_6 35
	SoC_CLKIN	SoC_CLKIN 31
	MCU_UART0_TX_3V3	MCU_UART0_TX_3V3 26
	MCU_UART0_RX_3V3	MCU_UART0_RX_3V3 26
	MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3 26
	MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3 26

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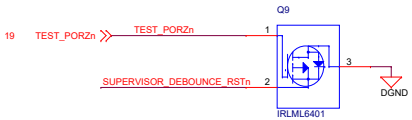
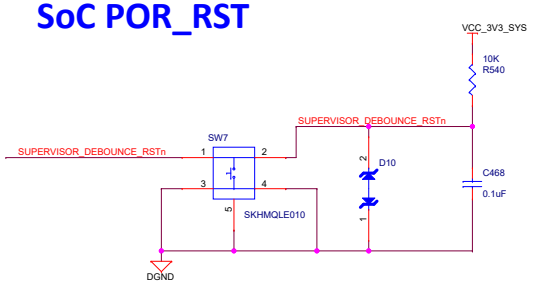
TEXAS INSTRUMENTS MISTRAL

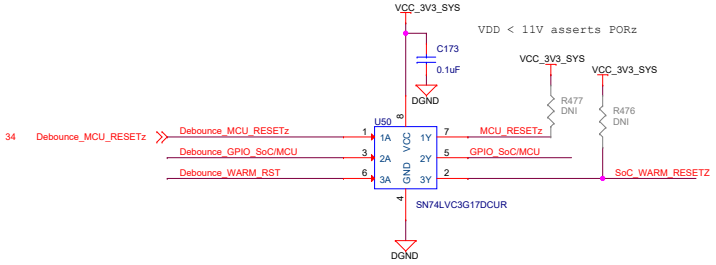
Title	MCU GENERAL & SAFETY CONNECTOR	
Size C	Variant Name = PROC101E2 TMDS64GPEVM	Rev E2
Date: Thursday, January 28, 2021	Sheet 34 of 40	

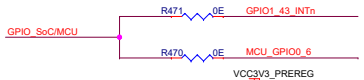
SoC POR_RST



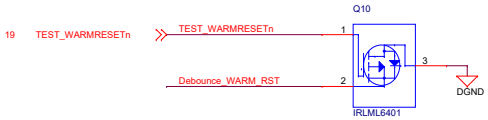


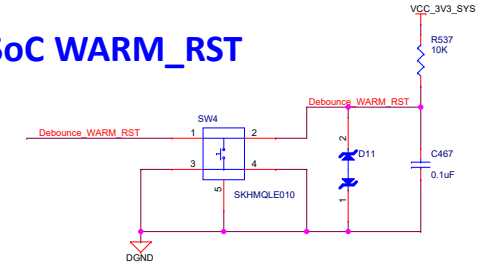
DEBOUNCE CIRCUIT

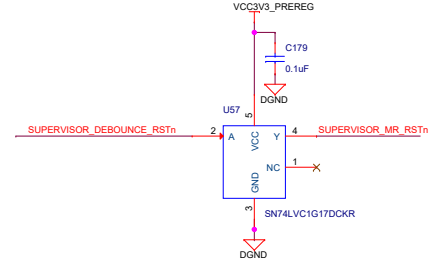


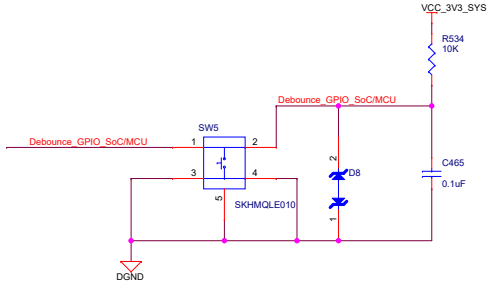


SoC WARM_RST







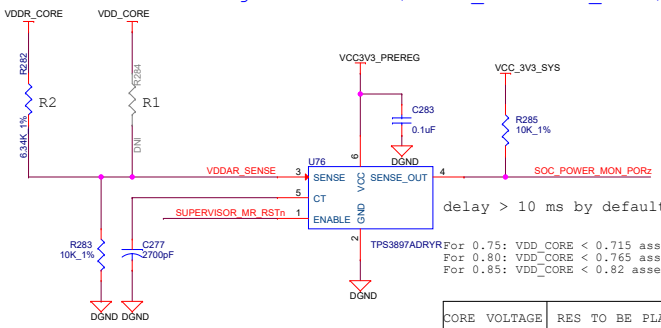


Off Page Connections

To Processor	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG	37,39
	SoC_WARM_RESETZ	SoC_WARM_RESETZ	34
	GPIO1_43_INTn	GPIO1_43_INTn	29
	MCU_RESETz	MCU_RESETz	27,34
	MCU_GPIO0_6	MCU_GPIO0_6	34

VOLTAGE SUPERVISOR

Core Voltage Monitor (VDDAR_CORE/VDD_CORE)

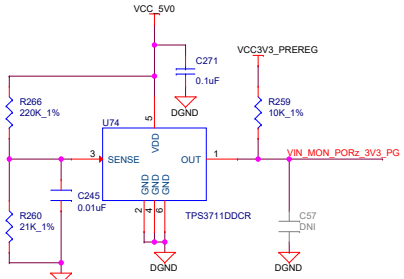


delay > 10 ms by default

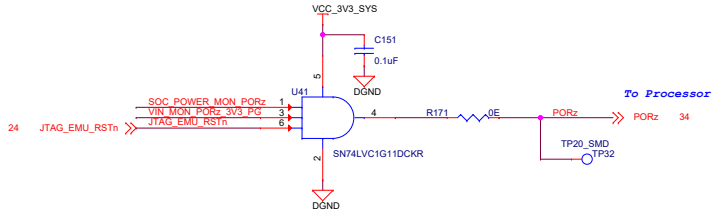
For 0.75: VDD_CORE < 0.715 assert PORz
For 0.80: VDD_CORE < 0.765 asserts PORz
For 0.85: VDD_CORE < 0.82 asserts PORz

CORE VOLTAGE	RES TO BE PLACED
0.75V	R1 = 4.3K
0.80V	R2 = 5.23K
0.85V	R2 = 6.34K

5V OUTPUT MONITOR (VCC_5V0)



40us delay by default
VDD < 4.6 asserts PORz



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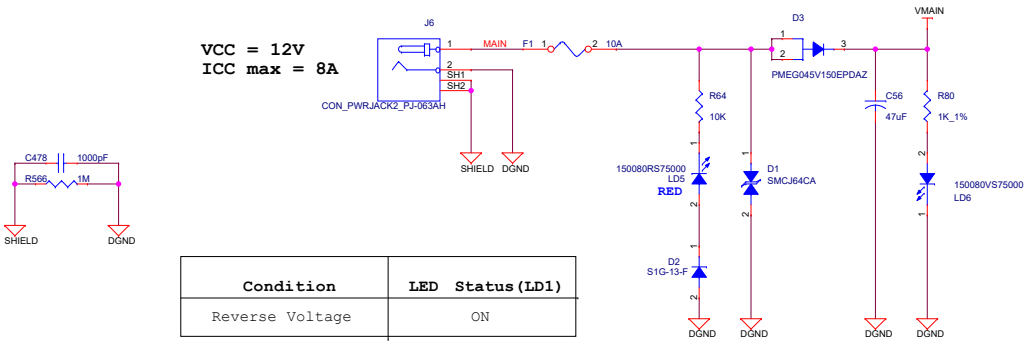
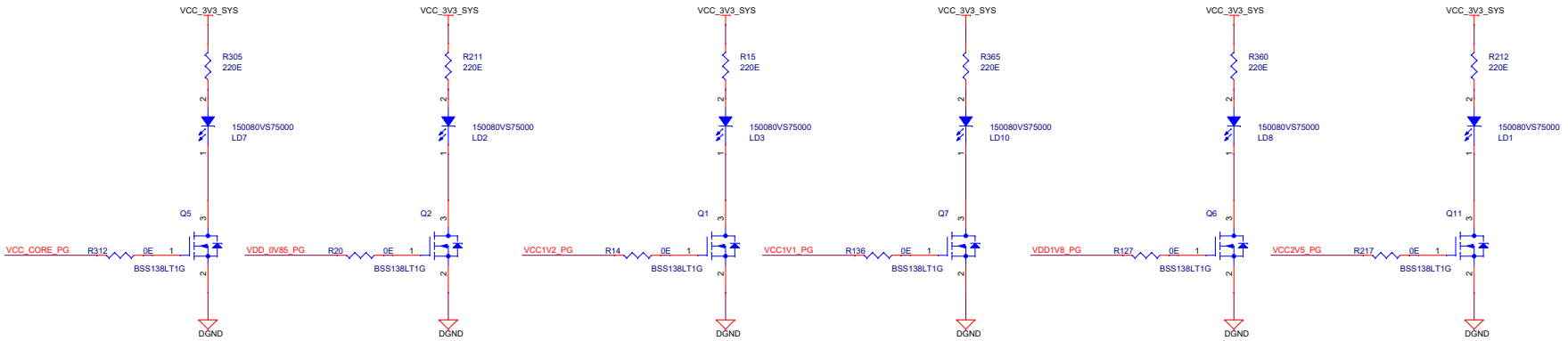
Title	DEBOUNCE CIRCUIT & VOLTAGE SUPERVISOR		
Size	Variant Name = PROC101E2 TMDS64GPEVM		Rev
C			E2
Date:	Thursday, January 28, 2021	Sheet	35 of 40

MAIN INPUT 12V DC



Condition	LED Status(LD1)
Reverse Voltage	ON

POWER INDICATION LED's



Ground test points

Off Page Connections

VCC_CORE_PG	VCC_CORE_PG	37,38
VDD_0V85_PG	VDD_0V85_PG	38
VCC1V2_PG	VCC1V2_PG	38
VCC1V1_PG	VCC1V1_PG	39
VDD1V8_PG	VDD1V8_PG	38
VCC2V5_PG	VCC2V5_PG	39

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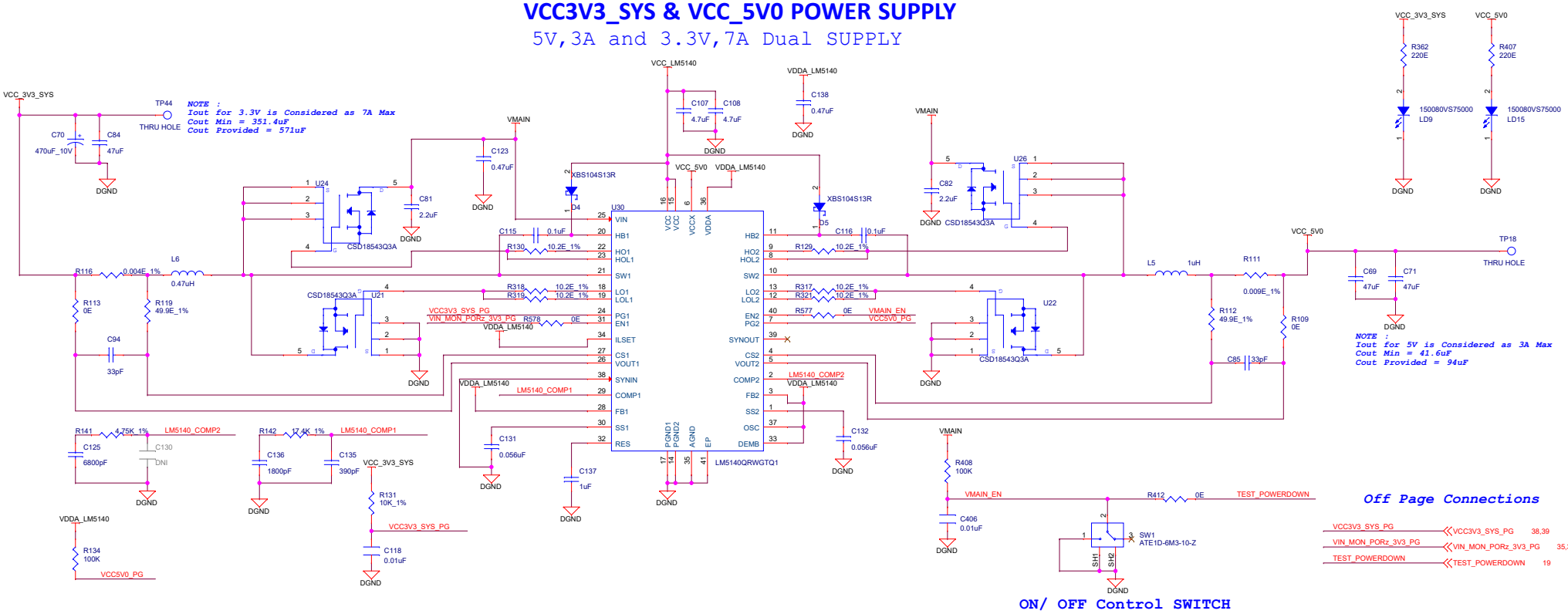
TEXAS INSTRUMENTS MISTRAL

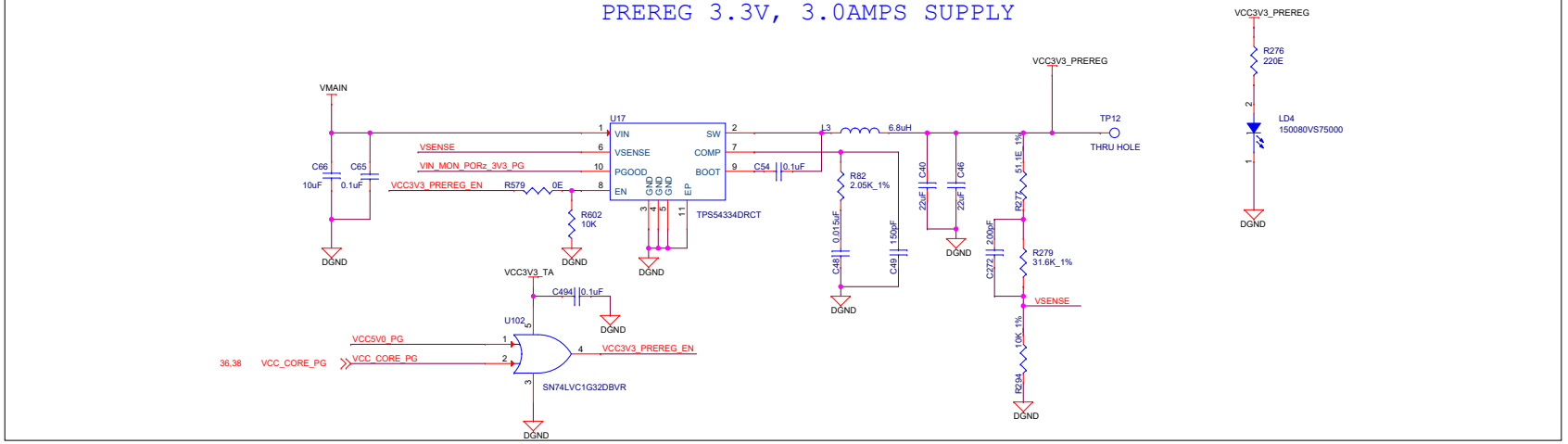
Title	MAIN 12V POWERSUPPLY	
Size	Variant Name = PROC101E2 TMDS64GPEVM	Rev
C		E2
Date: Thursday, January 28, 2021	Sheet 36 of 40	

VCC3V3_SYS & VCC_5V0 POWER SUPPLY

5V, 3A and 3.3V, 7A Dual SUPPLY



PREREG 3.3V, 3.0AMPS SUPPLY



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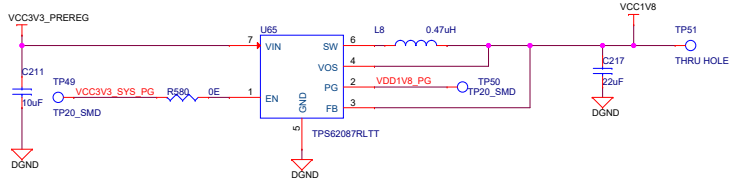
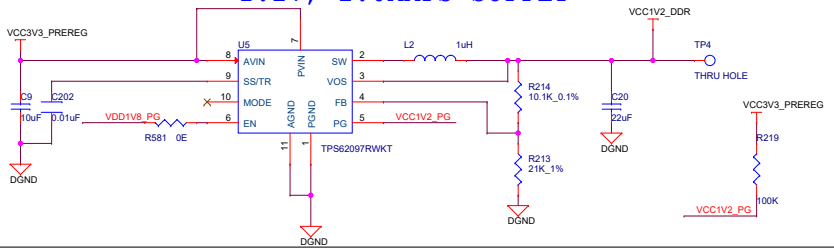
Title	DUAL & PREREG REGULATOR	
Size: C	Variant Name = PROC101E2 TMDS64GPEVM	Rev: E2
Date: Thursday, January 28, 2021	Sheet 37 of 40	

SoC POWER SUPPLY

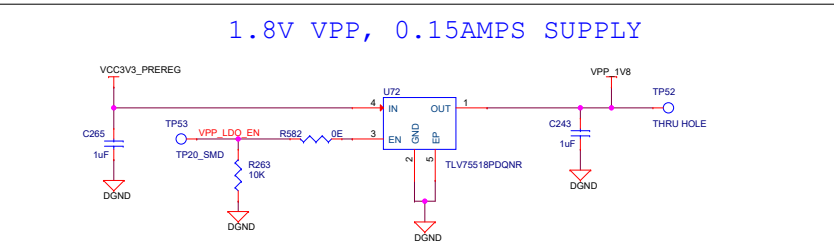
1.8V IO, 3.0AMPS SUPPLY



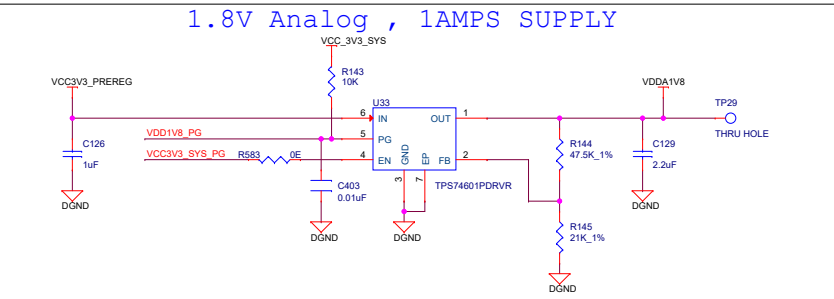
1.2V, 2.0AMPS SUPPLY



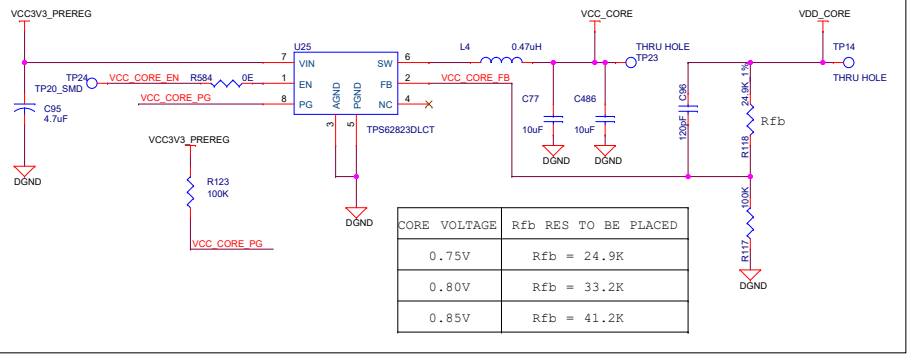
1.8V VPP, 0.15AMPS SUPPLY



1.8V Analog , 1AMPS SUPPLY

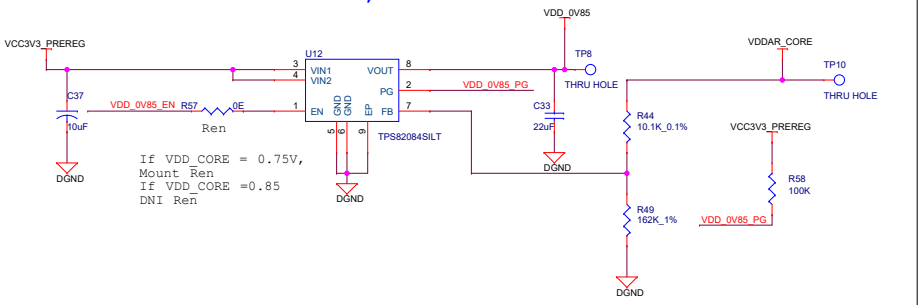


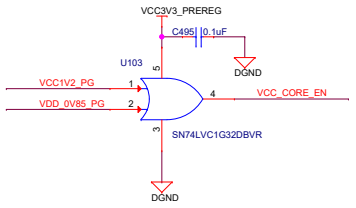
0.75 / 0.8 /0.85V, 3.0AMPS SUPPLY

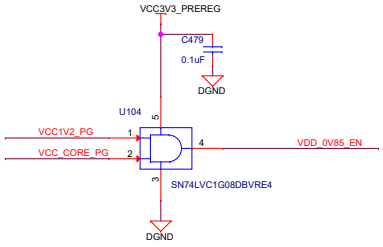


CORE VOLTAGE	Rfb RES TO BE PLACED
0.75V	Rfb = 24.9K
0.80V	Rfb = 33.2K
0.85V	Rfb = 41.2K

0.85 V, 1.5AMPS SUPPLY







Off Page Connections

36,37	VCC_CORE_PG	VCC_CORE_PG
36	VDD_0V85_PG	VDD_0V85_PG
36	VCC1V2_PG	VCC1V2_PG
36	VDD1V8_PG	VDD1V8_PG
33	VPP_LDO_EN	VPP_LDO_EN
35,37,39	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG
37,39	VCC3V3_SYS_PG	VCC3V3_SYS_PG

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TEXAS INSTRUMENTS

MISTRAL

Title	SoC POWER SUPPLY	
Size	Variant Name = PROC101E2 TMDS64GPEVM	Rev
C		E2
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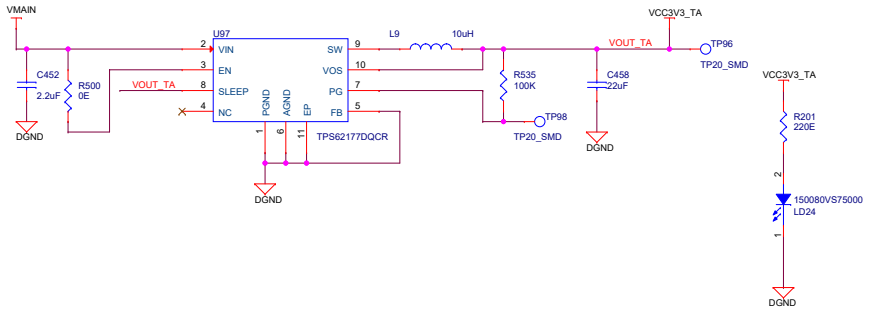
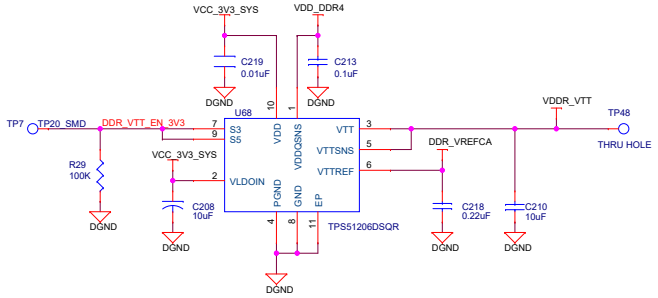
PERIPHERAL POWER SUPPLY

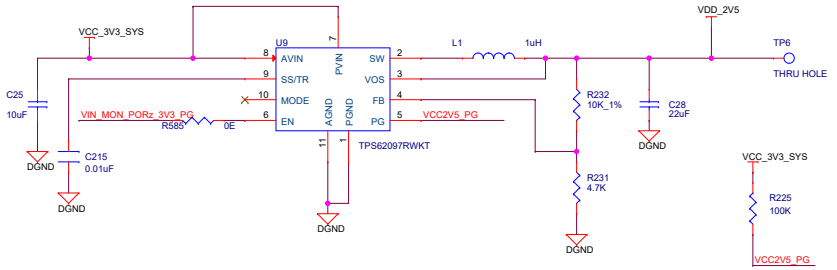
TEST AUTOMATION BOARD POWER



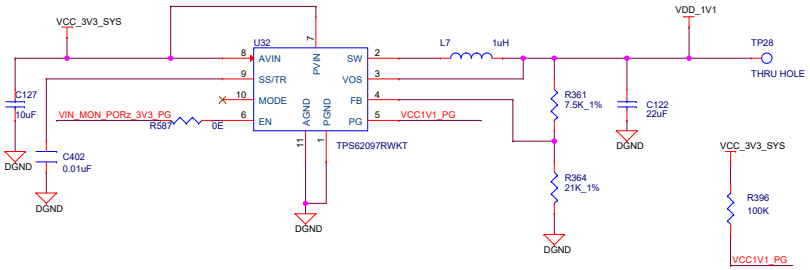
VTT SUPPLY FOR DDR4



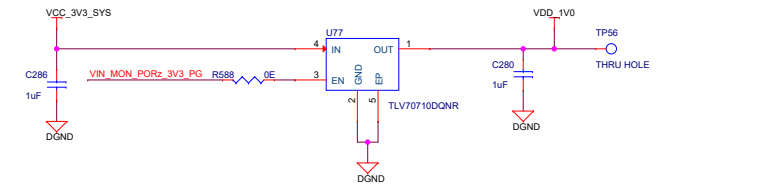
2.5V, 2.0AMPS SUPPLY



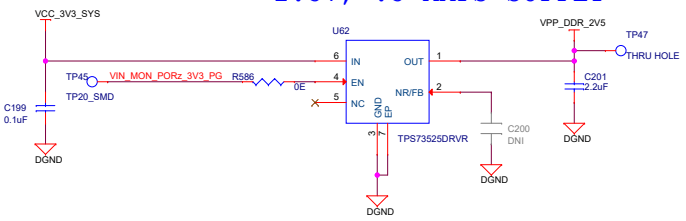
1.1V ETHERNET PHY POWER SUPPLY



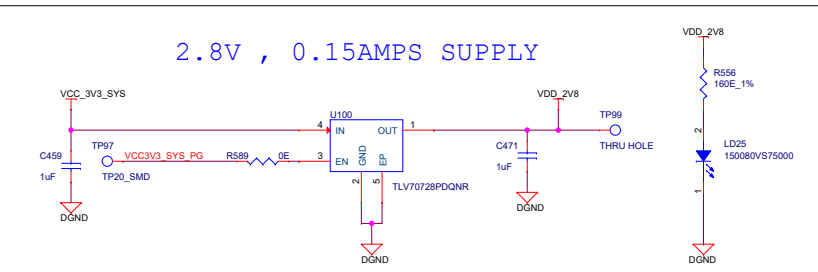
1.0V ETHERNET PHY POWER SUPPLY



2.5V, .5 AMPS SUPPLY



2.8V , 0.15AMPS SUPPLY



Off Page Connections

33	DDR_VTT_EN_3V3	DDR_VTT_EN_3V3
36	VCC2V5_PG	VCC2V5_PG
36	VCC1V1_PG	VCC1V1_PG
37,38	VCC3V3_SYS_PG	VCC3V3_SYS_PG
35,37	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG

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Title	PERIPHERAL POWER SUPPLY	
Size	Variant Name = PROC101E2 TMDS64GPEVM	Rev
C		E2
Date:	Thursday, January 28, 2021	Sheet 39 of 40

HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

STANDOFFs

MH1 MH2 MH3 MH4 MH5 MH6

970300151 970300151 970300151 970300151 970300151 970300151

SCREWS

MH13 MH14 MH15 MH16 MH17 MH18

29300 29300 29300 29300 29300 29300

MH19 MH20 MH21 MH22 MH23 MH24

29304 29304 29304 29304 29304 29304

WASHER's

M10 M11 M12 M13 M14 M19

4692 4692 4692 4692 4692 4692

RUBBER FEET

M1 M2 M3 M4 M5 M6

728 728 728 728 728 728

JUMPERs

ACC1 SPC02SYAN
ACC2 SPC02SYAN
ACC3 SPC02SYAN
ACC8 SPC02SYAN
ACC7 SPC02SYAN
ACC4 MNT-103-BK-G

FIDUCIALS

FID1 FID_40X80
FID2 FID_40X80
FID3 FID_40X80

TI EVM FLYERS

ACC11 SZZC019I
ACC12 SSZZ027

AM64x Socket

ACC10

C19874

BARE PCB

PCB1

PROC101

Assembled PCB

LABELS

Board Serial No.

LBL1 PCB LABEL
THT-103-423-10

Assembly Revision

LBL3 PCB LABEL
THT-103-423-10

ORDERABLE PART NO

LBL2 PCB LABEL
THT-103-423-10

Orderable part number	
Variant	**Label Text**
001	TMDS64GPEVM

LOGOs

PCB LOGO
Texas Intruments
Texas Intruments

PCB LOGO
For Evaluation only; not FCC approved for resale
For Evaluation only; not FCC approved for resale

PCB LOGO
WEEE Mark
WEEE Mark

PCB LOGO
CE Mark
CE Mark

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TEXAS INSTRUMENTS MISTRAL

Title	HARDWARE SCHEMATICS	
Size	Variant Name = PROC101E2 TMDS64GPEVM	Rev
C		E2
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