

# AM62D EVM

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**Note:**  
Verify the DNI components configuration with respect to the EVM schematics (Use PDF) after completion of design before board assembly

BOARD REVISION	E1
SCHEMATIC VERSION	0.11

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## REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	14 NOV 2023	Initial Draft	Mistral Design Team		
0.2	21 NOV 2023	Migrated to Burton PMIC and updated PDN as per AM62D EVM requirement	Mistral Design Team	Nishant	
0.3	27 NOV 2023	Implemented Audio section as per AM62D EVM requirements	Mistral Design Team	Nishant	
0.4	14 DEC 2023	Internally reviewed and shared with TI for review	Mistral Design Team	Nishant	Ajit MB
0.5	27 DEC 2023	1. Implemented Audio Expansions & CPLD 2. Replaced Audio Lineout devices with TAD5212	Mistral Design Team		
0.6	29 DEC 2023	Implemented review comments from TI	Mistral Design Team	Nishant	Ajit MB
0.7	07 FEB 2024	Updated AEC, McASP Muxing, CPLD, Current Monitoring Sections	Mistral Design Team		
0.8	21 FEB 2024	Updated Ethernet Expansion, FET Bus Switch & Voltage level translators	Mistral Design Team		
0.9	03 MAR 2024	Updated Switch for fet selection and implemented TI comments	Mistral Design Team		
0.10	22 MAR 2024	Updated Audio section, CPLD1 and CPLD2 connections removed FET switches as per TI comments.	Mistral Design Team		
0.11	28 MAR 2024	Implemented review comments from TI	Mistral Design Team		
0.12	04 APRIL 2024	Implemented review comments from TI	Mistral Design Team		
0.13	17 APRIL 2024	Implemented modular approach	Mistral Design Team		
1.0	10 MAY 2024	Baselined	Mistral Design Team		

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## LINK TO DESIGN COLLATERALS

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am62x-am62ax-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review>

## FAQs

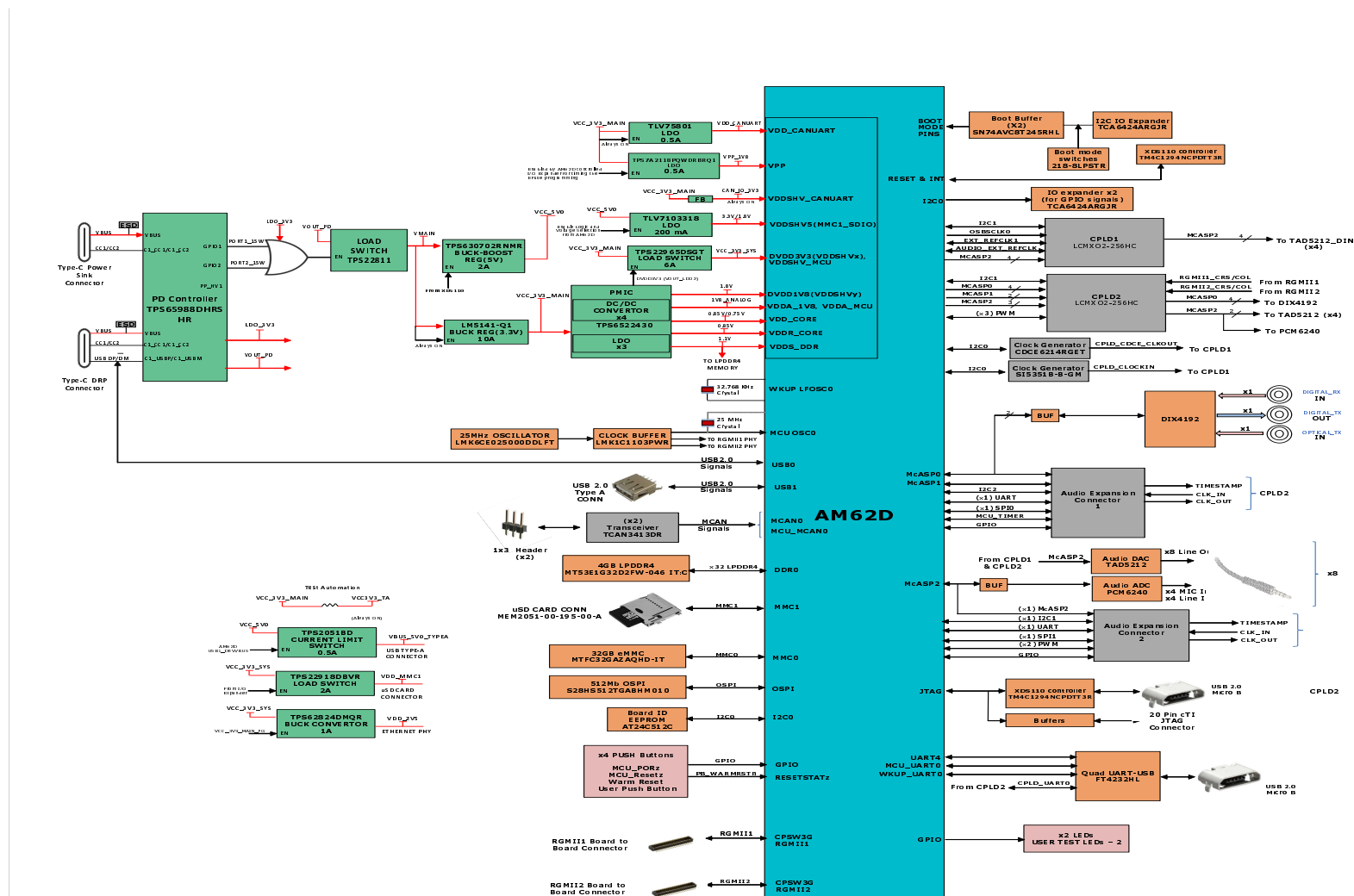
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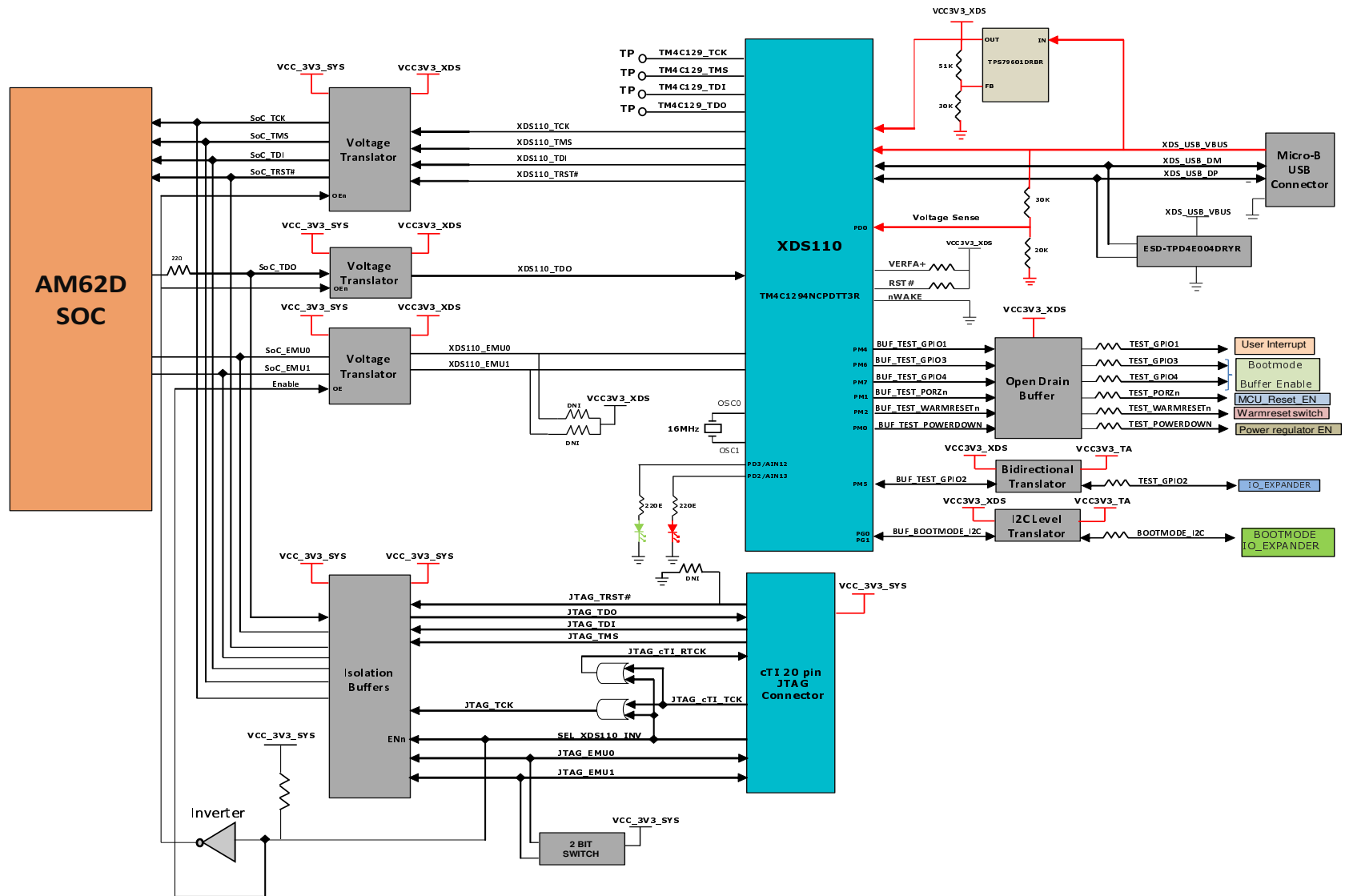
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## BLOCK DIAGRAM AM62D EVM





# BLOCK DIAGRAM\_XDS110



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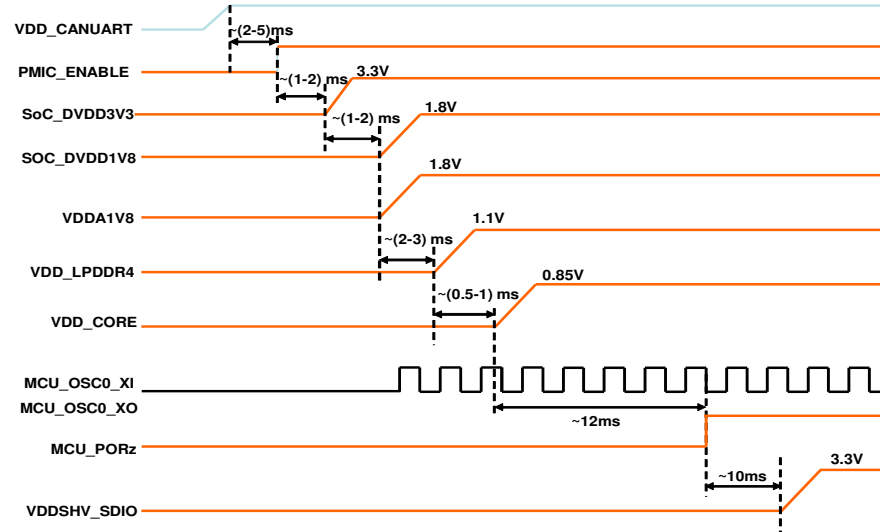


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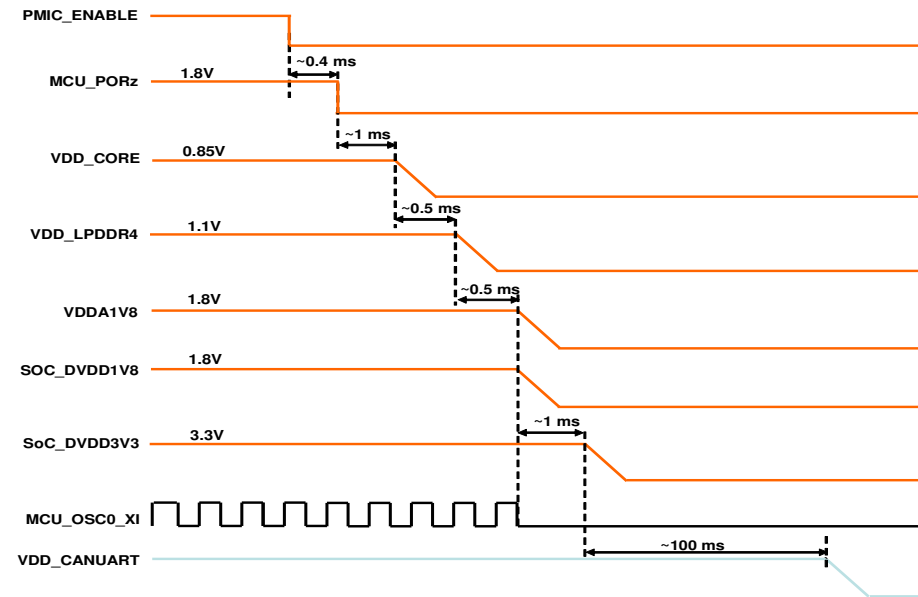
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[illegible]

## POWER UP SEQUENCE



## POWER DOWN SEQUENCE



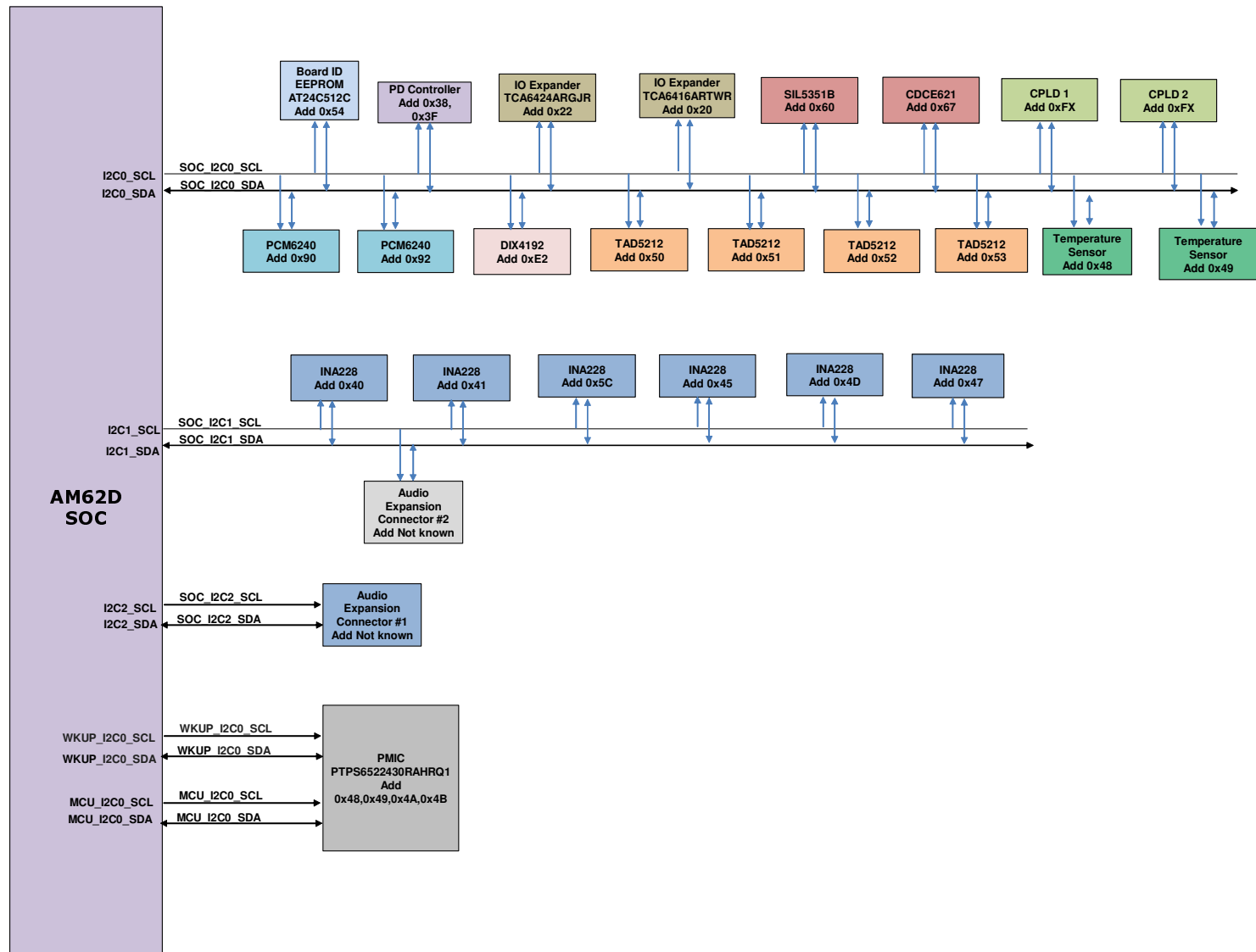
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# I2C TREE



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# GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGESIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE RAIL CONNECTED ON SEWIM
1	Audio Tx pin connector 1	EXF1_GPIO_1	G RO	G RO_1	G PBD_1C1R0	NA	NA	NA	VDDH V1	%L_VDDH V1
2	DIR Transceiver	G PBD_1D1R1	BI TT	G PBD_1D1	G PBD_1D1	INP UT	INB H	LOW	VDDH V1	%L_VDDH V1
3	Audio Tx pin connector 1	EXF1_GPIO_13	G RO	G PBD_1D13	G PBD_1D13	NA	NA	NA	VDDH V1	%L_VDDH V1
4	Audio Tx pin connector 1	EXF1_GPIO_14	G RO	G PBD_1D14	G PBD_1D14	NA	NA	NA	VDDH V1	%L_VDDH V1
5	Audio Tx pin connector 1	EXF1_GPIO_15	G RO	G PBD_1D15	G PBD_1D15	NA	NA	NA	VDDH V1	%L_VDDH V1
6	Audio Tx pin connector 1	EXF1_GPIO_16	G RO	G PBD_1D16	G PBD_1D16	NA	NA	NA	VDDH V1	%L_VDDH V1
7	Micro Header	EXF1_GPIO_17	G RO	G PBD_1D17	G PBD_1D17	NA	NA	NA	VDDH V1	%L_VDDH V1
8	Audio Tx pin connector 1	EXF1_GPIO_18	G RO	G PBD_1D18	G PBD_1D18	NA	NA	NA	VDDH V1	%L_VDDH V1
9	Micro Header	EXF1_GPIO_19	G RO	G PBD_1D19	G PBD_1D19	NA	NA	NA	VDDH V1	%L_VDDH V1
10	Audio Tx pin connector 1	EXF1_GPIO_20	G RO	G PBD_1D20	G PBD_1D20	NA	NA	NA	VDDH V1	%L_VDDH V1
11	Audio Tx pin connector 1	EXF1_GPIO_21	G RO	G PBD_1D21	G PBD_1D21	NA	NA	NA	VDDH V1	%L_VDDH V1
12	Audio Tx pin connector 1	EXF1_GPIO_22	G RO	G PBD_1D22	G PBD_1D22	NA	NA	NA	VDDH V1	%L_VDDH V1
13	Audio Tx pin connector 2	EXF1_GPIO_23	G RO	G PBD_1D23	G PBD_1D23	NA	NA	NA	VDDH V1	%L_VDDH V1
14	Audio Tx pin connector 2	EXF1_GPIO_24	G RO	G PBD_1D24	G PBD_1D24	NA	NA	NA	VDDH V1	%L_VDDH V1
15	Audio Tx pin connector 2	EXF1_GPIO_25	G RO	G PBD_1D25	G PBD_1D25	NA	NA	NA	VDDH V1	%L_VDDH V1
16	Audio Tx pin connector 2	EXF1_GPIO_26	G RO	G PBD_1D26	G PBD_1D26	NA	NA	NA	VDDH V1	%L_VDDH V1
17	Audio Tx pin connector 2	EXF1_GPIO_27	G RO	G PBD_1D27	G PBD_1D27	NA	NA	NA	VDDH V1	%L_VDDH V1
18	Audio Tx pin connector 2	EXF1_GPIO_28	G RO	G PBD_1D28	G PBD_1D28	NA	NA	NA	VDDH V1	%L_VDDH V1
19	Audio Tx pin connector 2	EXF1_GPIO_29	G RO	G PBD_1D29	G PBD_1D29	NA	NA	NA	VDDH V1	%L_VDDH V1
20	Audio Tx pin connector 2	EXF1_GPIO_30	G RO	G PBD_1D30	G PBD_1D30	NA	NA	NA	VDDH V1	%L_VDDH V1
21	Micro Header	EXF1_GPIO_31	G RO	G PBD_1D31	G PBD_1D31	NA	NA	NA	VDDH V1	%L_VDDH V1
22	Micro Header	EXF1_GPIO_32	G RO	G PBD_1D32	G PBD_1D32	NA	NA	NA	VDDH V1	%L_VDDH V1
23	Low power mode enable	EXF1_GPIO_33	G RO	G PBD_1D33	G PBD_1D33	NA	NA	NA	VDDH V1	%L_VDDH V1
24	Micro Header	EXF1_GPIO_34	G RO	G PBD_1D34	G PBD_1D34	NA	NA	NA	VDDH V1	%L_VDDH V1
25	Micro Header	EXF1_GPIO_35	G RO	G PBD_1D35	G PBD_1D35	NA	NA	NA	VDDH V1	%L_VDDH V1
IO EXPANDER - 01										
1	GND_PSW1_RST	GND_PSW1_RST	ENABLE	IO EXPANDER-R01		G UP PUT	INB H	LOW		VCC_VDD1_V1
2	GND_PSW2_RST	GND_PSW2_RST	ENABLE	IO EXPANDER-R02		G UP PUT	INB H	LOW		VCC_VDD1_V1
3	PCMCIA_RST	PCMCIA_RST	DIRECTION CONTROL	IO EXPANDER-R03		G UP PUT	INB H	LOW		VCC_VDD1_V1
4	MCU_RST	MCU_RST	ENABLE	IO EXPANDER-R04		G UP PUT	INB H	LOW		VCC_VDD1_V1
5	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R05		G UP PUT	INB H	LOW		VCC_VDD1_V1
6	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R06		G UP PUT	INB H	LOW		VCC_VDD1_V1
7	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R07		G UP PUT	INB H	LOW		VCC_VDD1_V1
8	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R08		G UP PUT	INB H	LOW		VCC_VDD1_V1
9	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R09		G UP PUT	INB H	LOW		VCC_VDD1_V1
10	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R10		G UP PUT	INB H	LOW		VCC_VDD1_V1
11	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R11		G UP PUT	INB H	LOW		VCC_VDD1_V1
12	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R12		G UP PUT	INB H	LOW		VCC_VDD1_V1
13	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R13		G UP PUT	INB H	LOW		VCC_VDD1_V1
14	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R14		G UP PUT	INB H	LOW		VCC_VDD1_V1
15	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R15		G UP PUT	INB H	LOW		VCC_VDD1_V1
16	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R16		G UP PUT	INB H	LOW		VCC_VDD1_V1
17	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R17		G UP PUT	INB H	LOW		VCC_VDD1_V1
18	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R18		G UP PUT	INB H	LOW		VCC_VDD1_V1
19	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R19		G UP PUT	INB H	LOW		VCC_VDD1_V1
20	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R20		G UP PUT	INB H	LOW		VCC_VDD1_V1
21	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R21		G UP PUT	INB H	LOW		VCC_VDD1_V1
22	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R22		G UP PUT	INB H	LOW		VCC_VDD1_V1
23	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R23		G UP PUT	INB H	LOW		VCC_VDD1_V1
24	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R24		G UP PUT	INB H	LOW		VCC_VDD1_V1
IO EXPANDER - 02										
1	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R01		G UP PUT	INB H	LOW		VCC_VDD1_V1
2	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R02		G UP PUT	INB H	LOW		VCC_VDD1_V1
3	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R03		G UP PUT	INB H	LOW		VCC_VDD1_V1
4	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R04		G UP PUT	INB H	LOW		VCC_VDD1_V1
5	PCMCIA_RST	PCMCIA_RST	ENABLE	IO EXPANDER-R05		G UP PUT	INB H	LOW		VCC_VDD1_V1

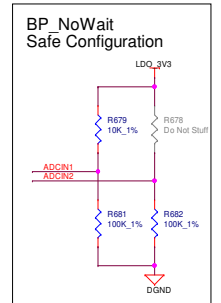
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Title GPIO MAPPING TABLE

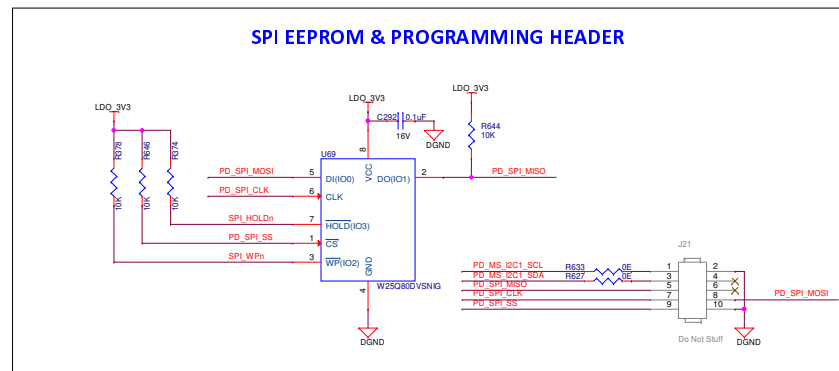
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## TYPE-C DUAL PD CONTROLLER

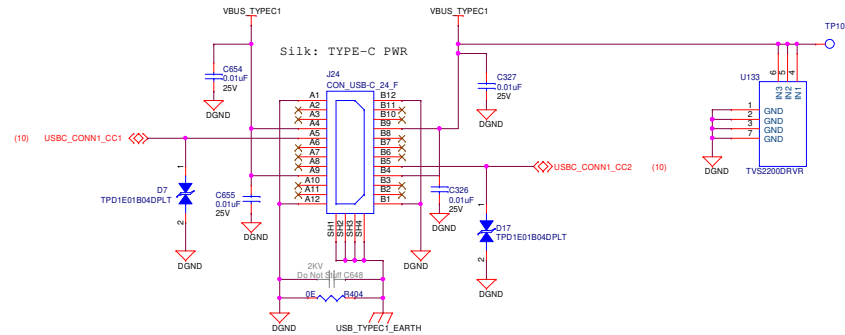


I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

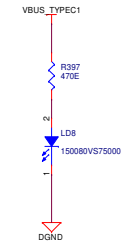
## SPI EEPROM & PROGRAMMING HEADER



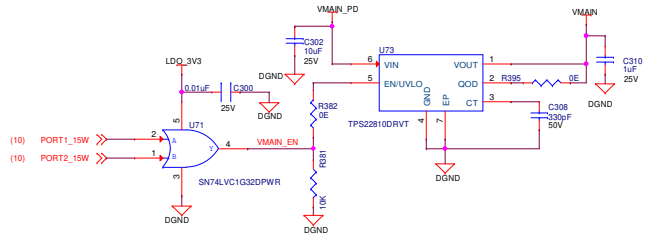
# USB TYPE-C POWER CONNECTOR



## POWER INDICATION LED: VBUS\_TYPEC1



## LOAD SWITCH FOR VMAIN



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Title USB TYPE-C POWER CONNECTOR

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5V, 2.0 AMPS SUPPLY

Diagram showing the connection of TP1, TP2, TP77, TP40, TP85, TP42, TP44, and TP41 to DGND. Each test point is connected to a common ground point labeled DGND.

$V_{inMin} = 4.5V$   
 $V_{inMax} = 15V$   
 $V_{out} = 3.3V @ 10A$

**PCB Note:** Short LMS141\_AGND and DGND at single point

PCB Note: Short LM5141\_AGND and DGND at single point



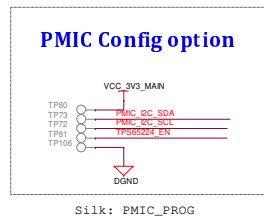
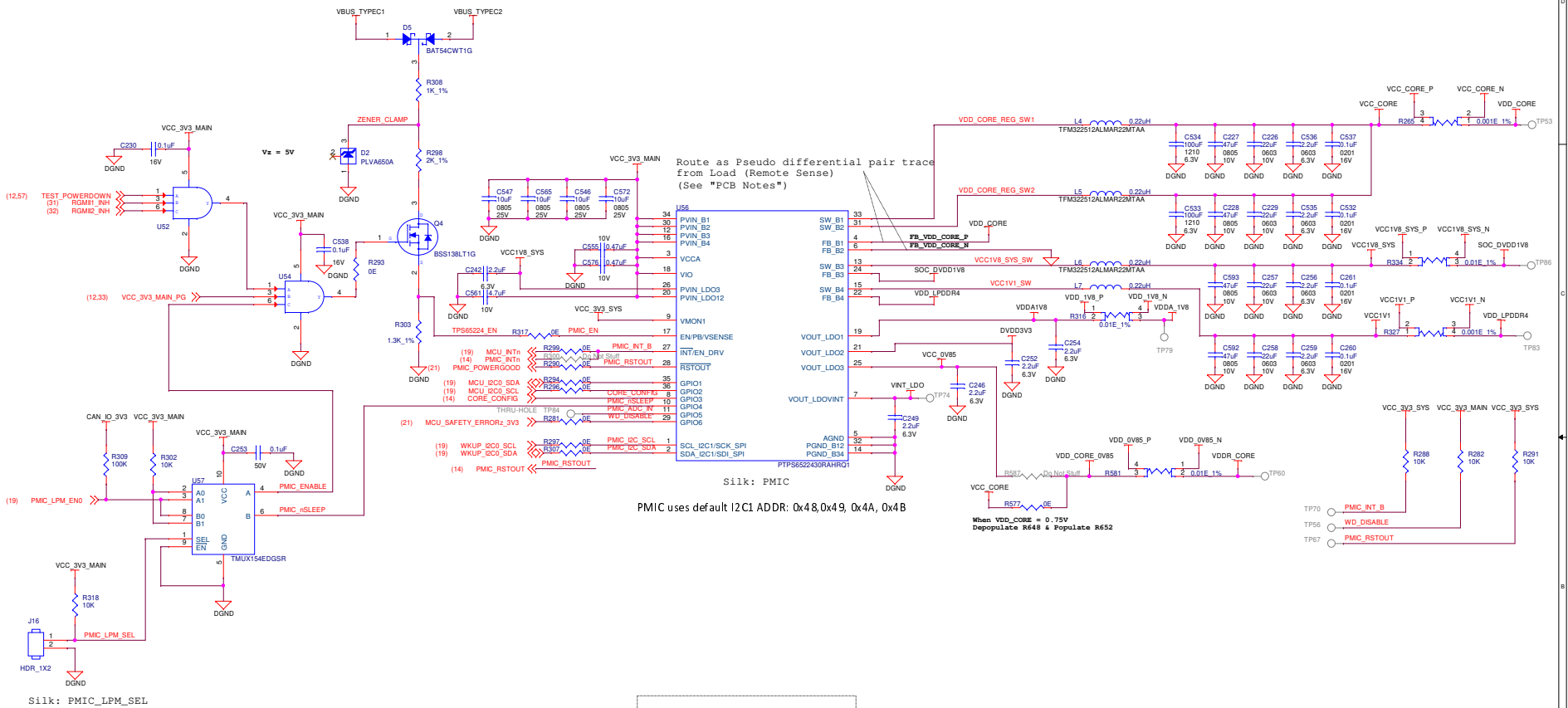
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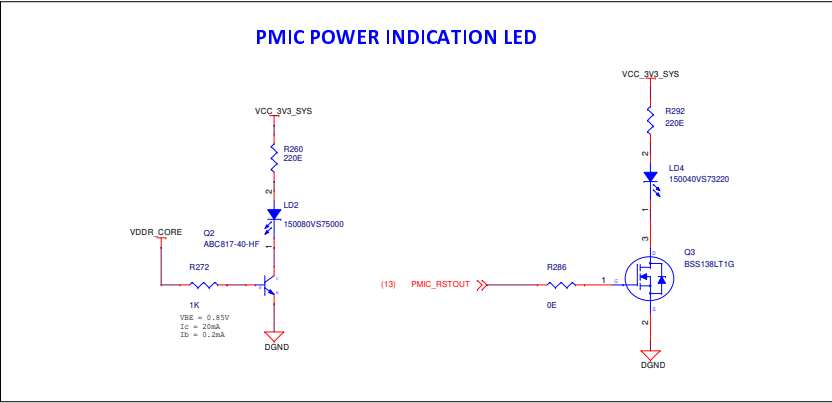


## SOC POWER SUPPLY PMIC - 1

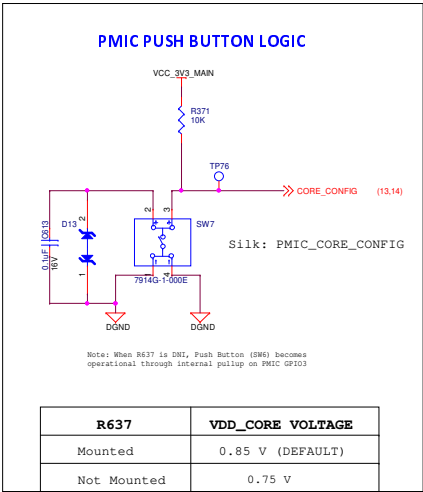


SOC POWER SUPPLY PMIC - 2

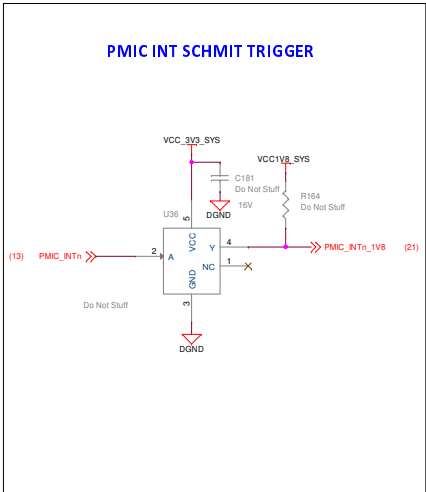
PMIC POWER INDICATION LED



PMIC PUSH BUTTON LOGIC



PMIC INT SCHMIT TRIGGER



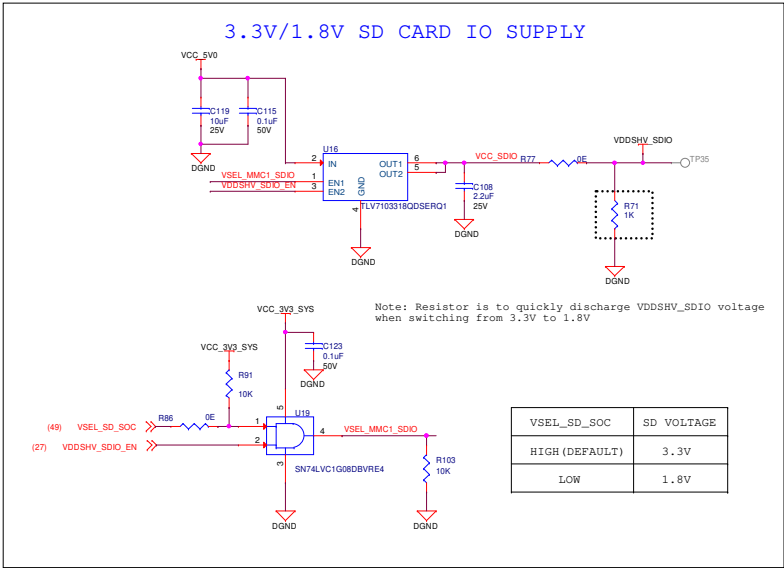
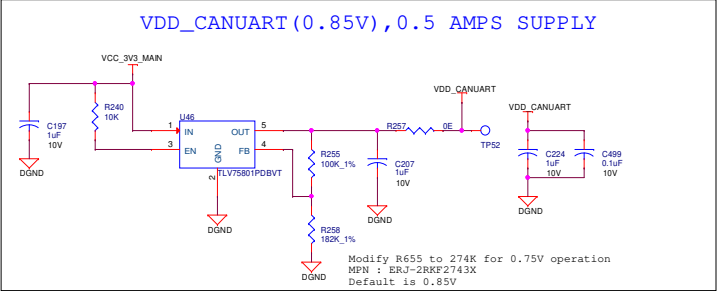
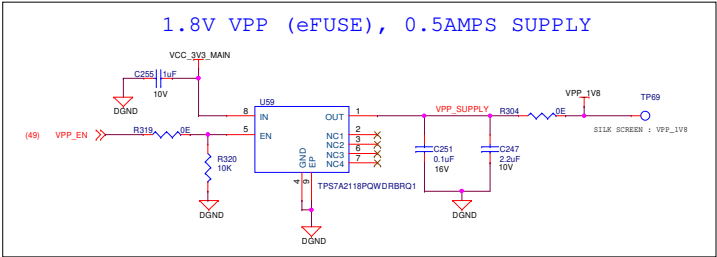
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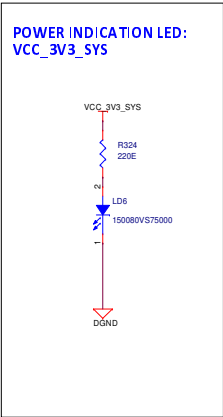
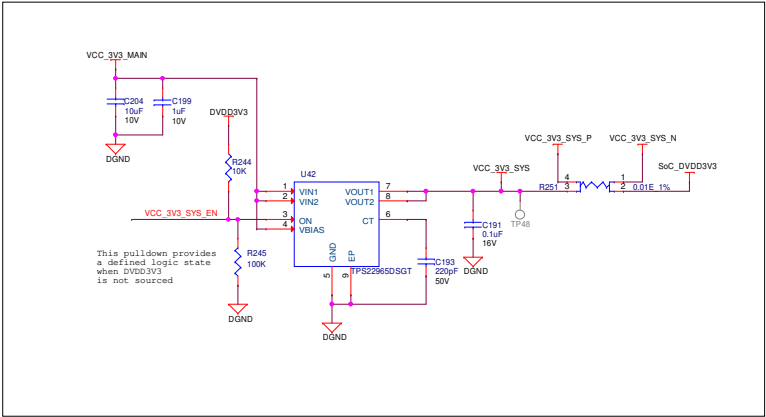
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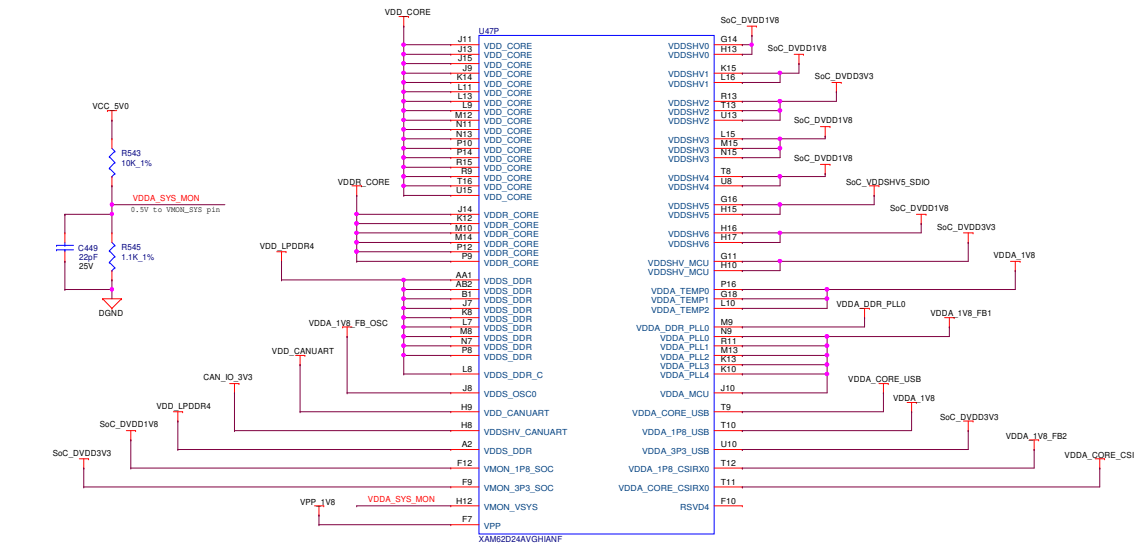
SOC POWER SUPPLIES - LDOs



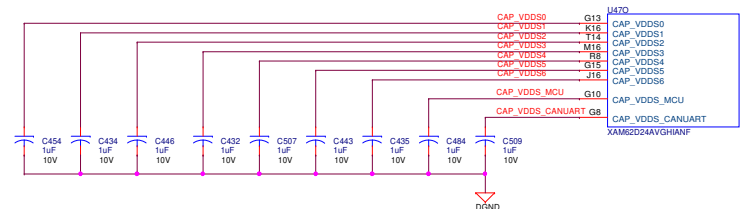
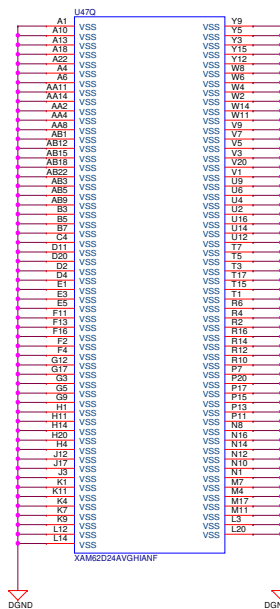
VCC\_3V3\_SYS LOAD SWITCH



# SOC POWER SUPPLIES AND SUPPLY RAILS



## SOC VSS



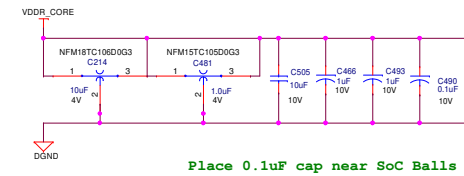
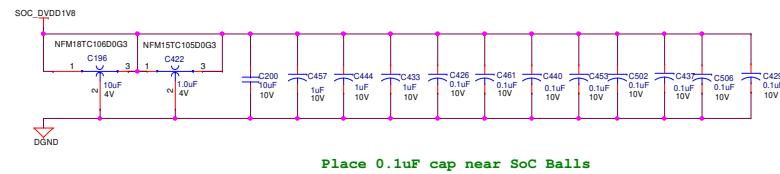
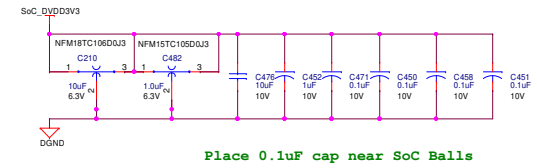
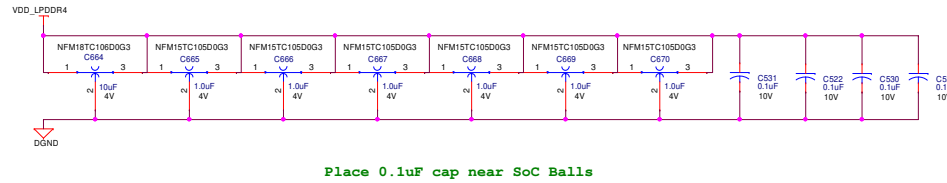
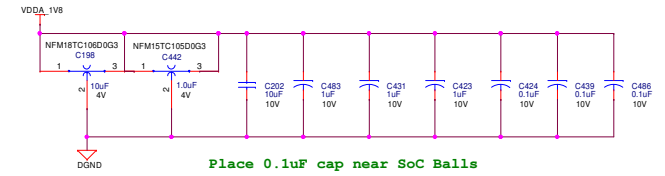
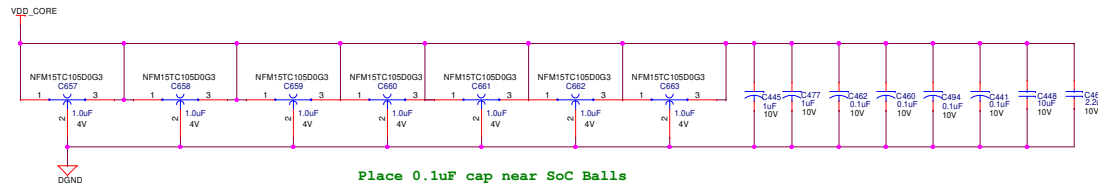
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Title SOC POWER SUPPLIES, SUPPLY RAILS AND SOC GROUND VSS

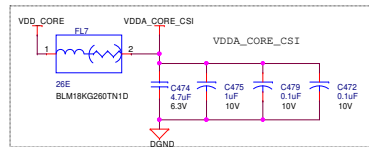
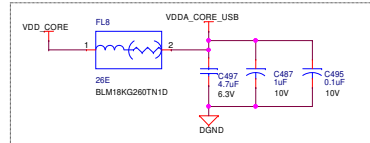
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# SOC POWER SUPPLIES - DECAPS 1

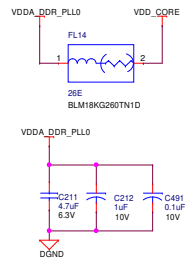


# SOC POWER SUPPLIES - DECAPS 2

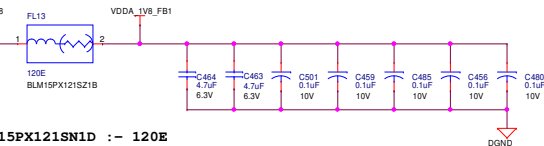
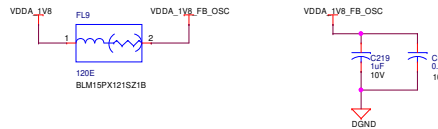
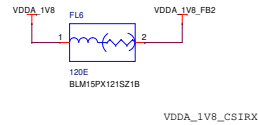
## Peripherals - Core SUPPLY



## VDDA\_DDR\_PLL0

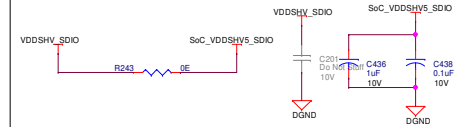


## Peripherals - 1.8V Analog SUPPLY

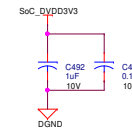
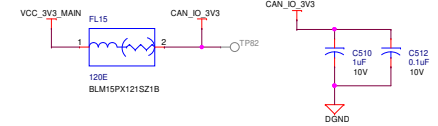


BLM15PX121SN1D :- 120E  
2A @ 85 deg C  
1.1A @ 125 deg C

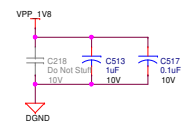
## 3.3V/1.8V MMC1 SUPPLY



## Always ON supply



## VPP\_1V8



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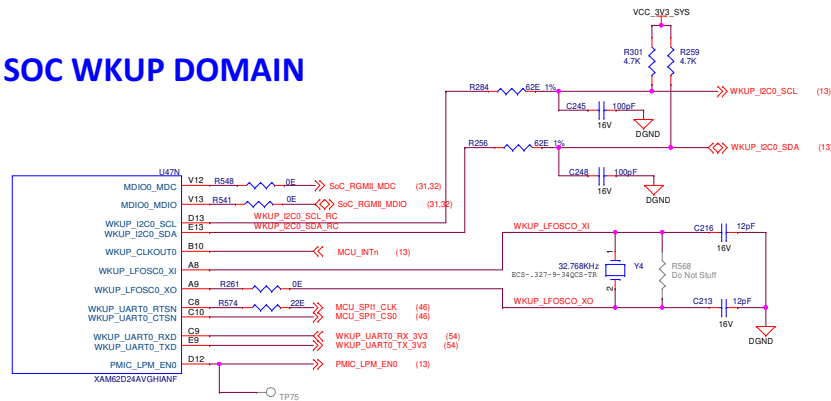


Title SOC POWER SUPPLIES - DECAPS 2

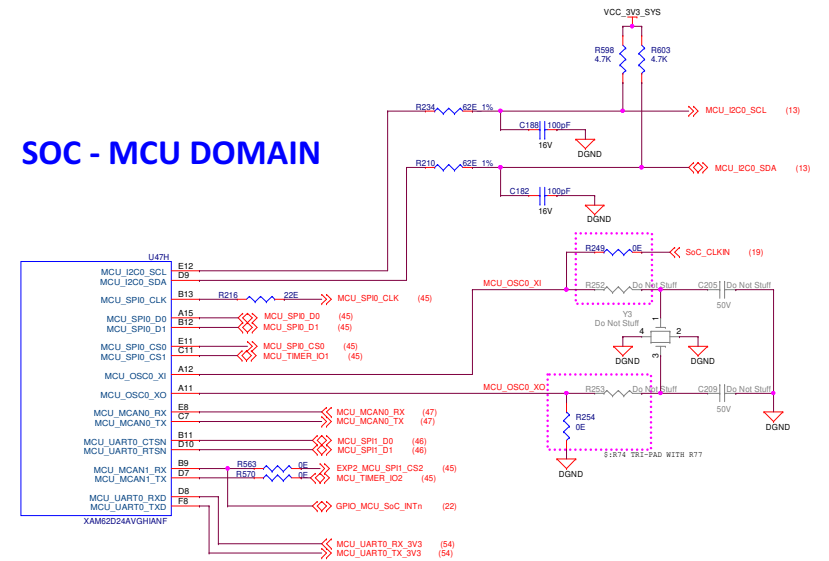
Size	Rev
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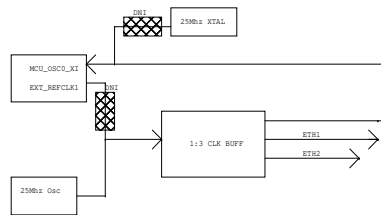
## SOC WKUP DOMAIN



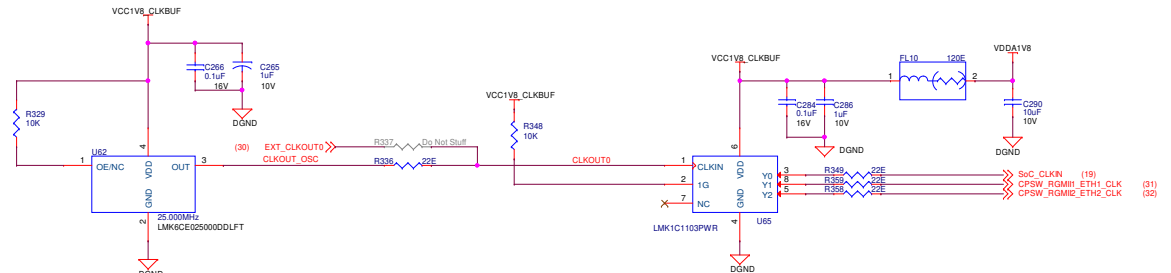
## SOC - MCU DOMAIN



## OSCILLATOR



## SOC & ETHERNET PHY CLOCK BUFFER



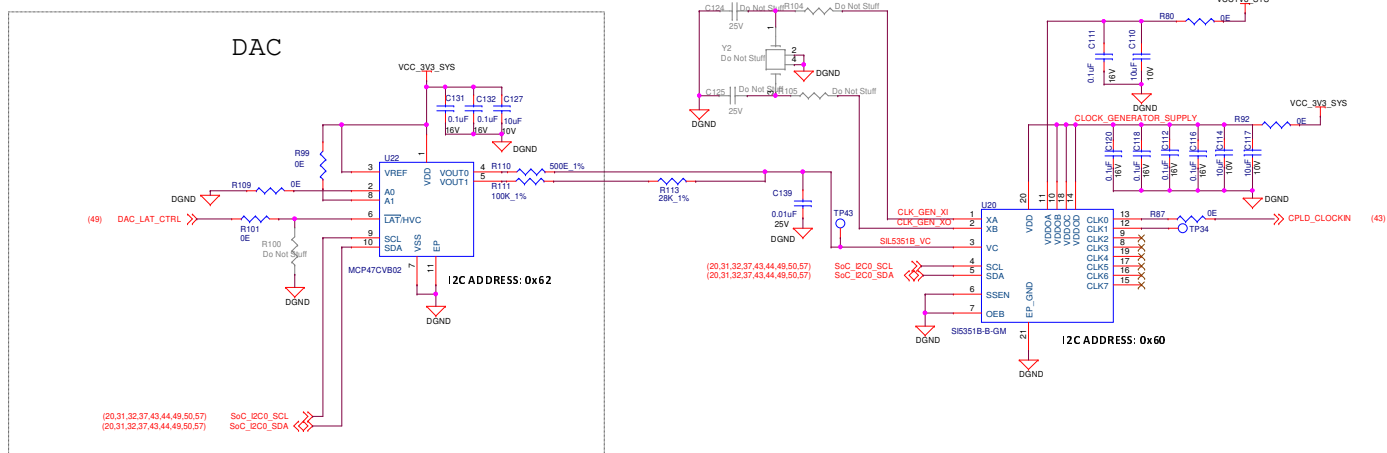
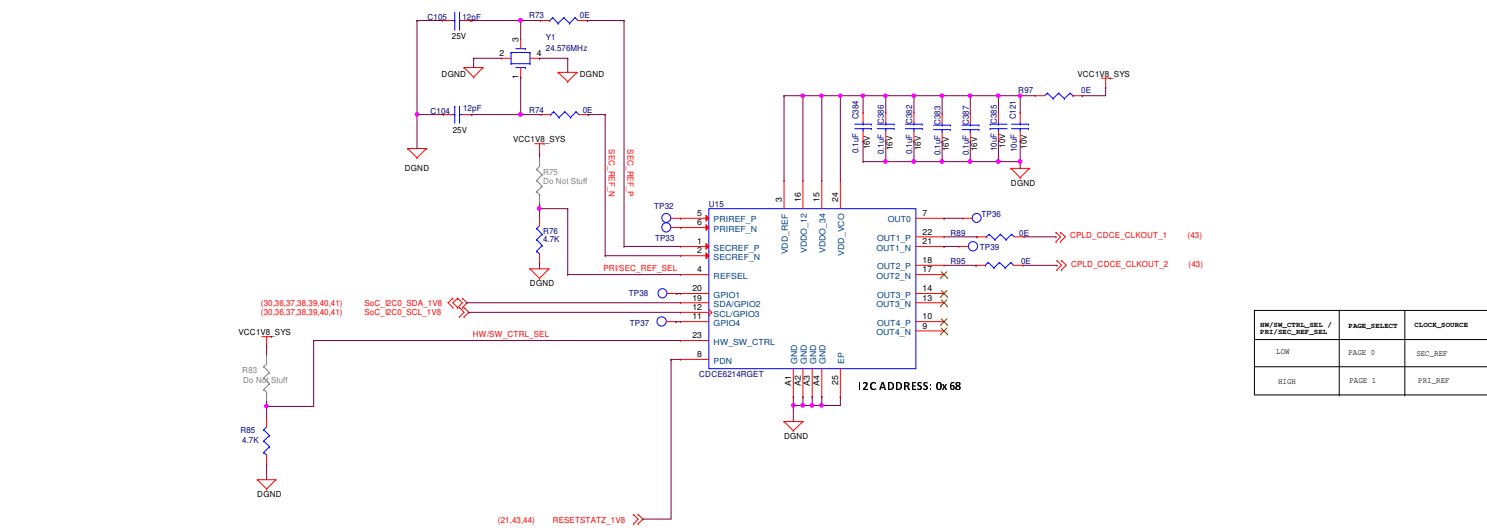
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Title SOC WKUP & GPWC

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# CPLD CLOCK GENERATION



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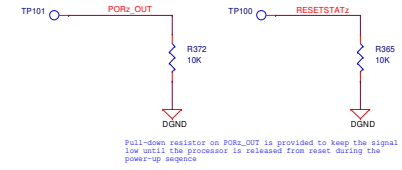
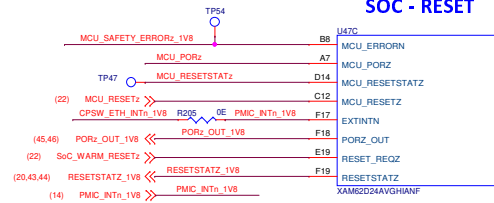
Title CPLD CLOCK GENERATION

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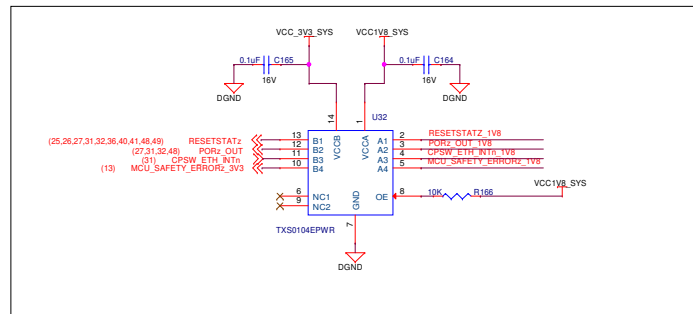


# SOC RESET - 1

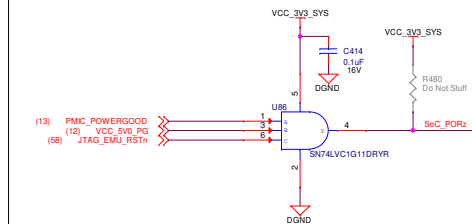
## SOC - RESET



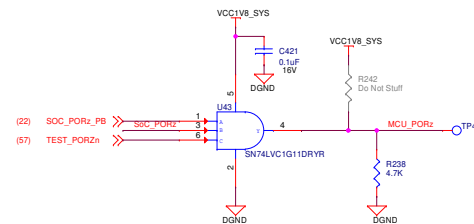
## LEVEL TRANSLATOR



## SOC POWER ON RESET



## MCU POWER ON RESET



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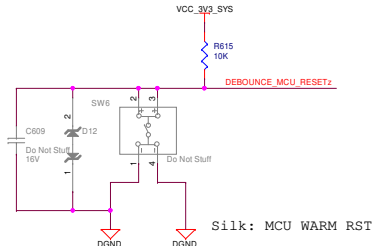


Title SOC RESET - 1

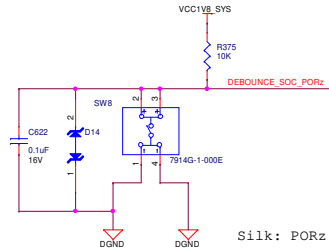
Size	Rev
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Date: Monday, May 13, 2024	Sheet 21 of 59

## SOC RESET - 2

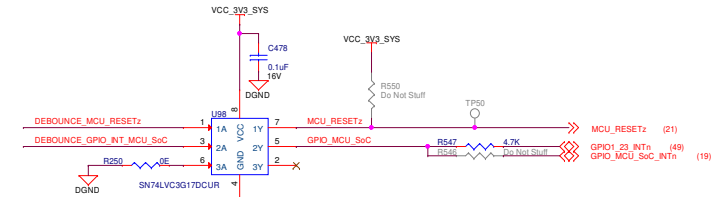
### MCU WARM RESET



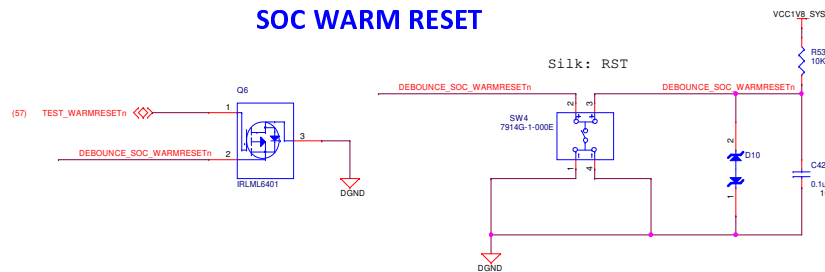
### SOC PORz



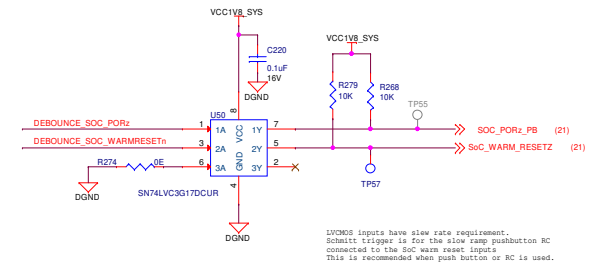
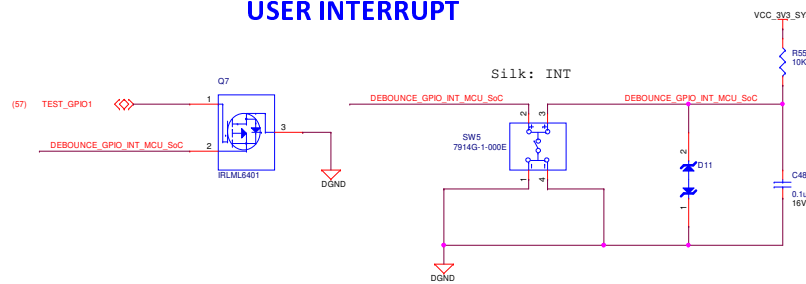
### RESET & INT DEBOUNCE CIRCUIT



### SOC WARM RESET



### USER INTERRUPT



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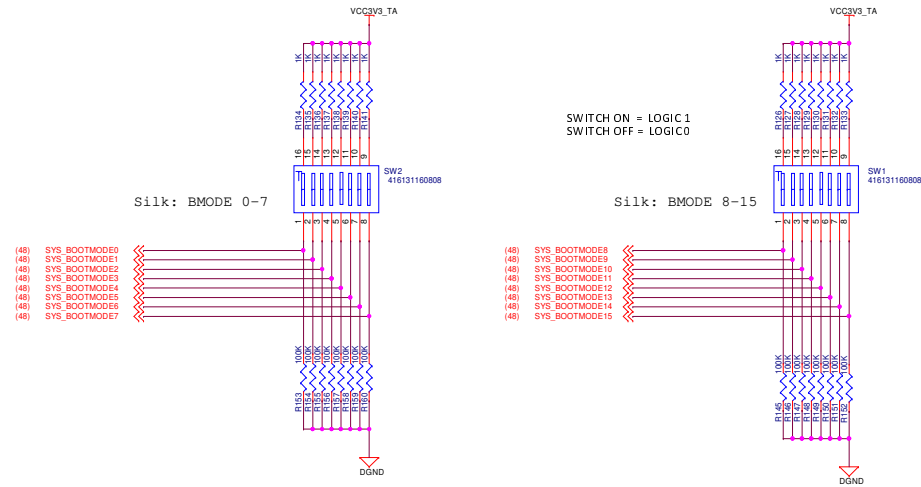


Title SOC RESET - 2

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# BOOT MODE SWITCHES

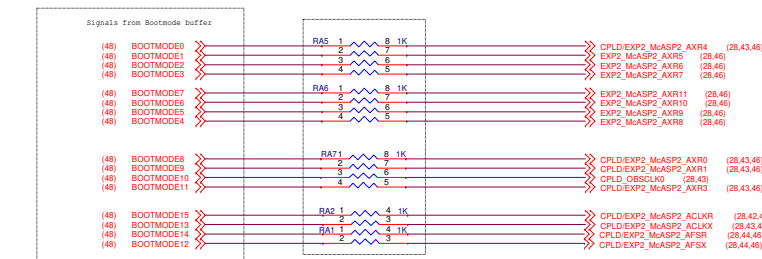
D-Note: VCC3V3\_TA supply is used for test automation.  
Connect: SOC\_0V503V3 in the custom board design when buffers are not used



## BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. USB0 MS

## BOOTMODE PINS



D-Note :  
Connect: SYS\_BOOTMODE signals when  
bootmode buffers are not used

- D-NOTE:
1. 1K Resistor at the output of the buffer is recommended when the bootmode pins are used for alternate functions
  2. Replace 1K Resistor at the output of the buffer with resistor of value 0E when bootmode buffers are not used

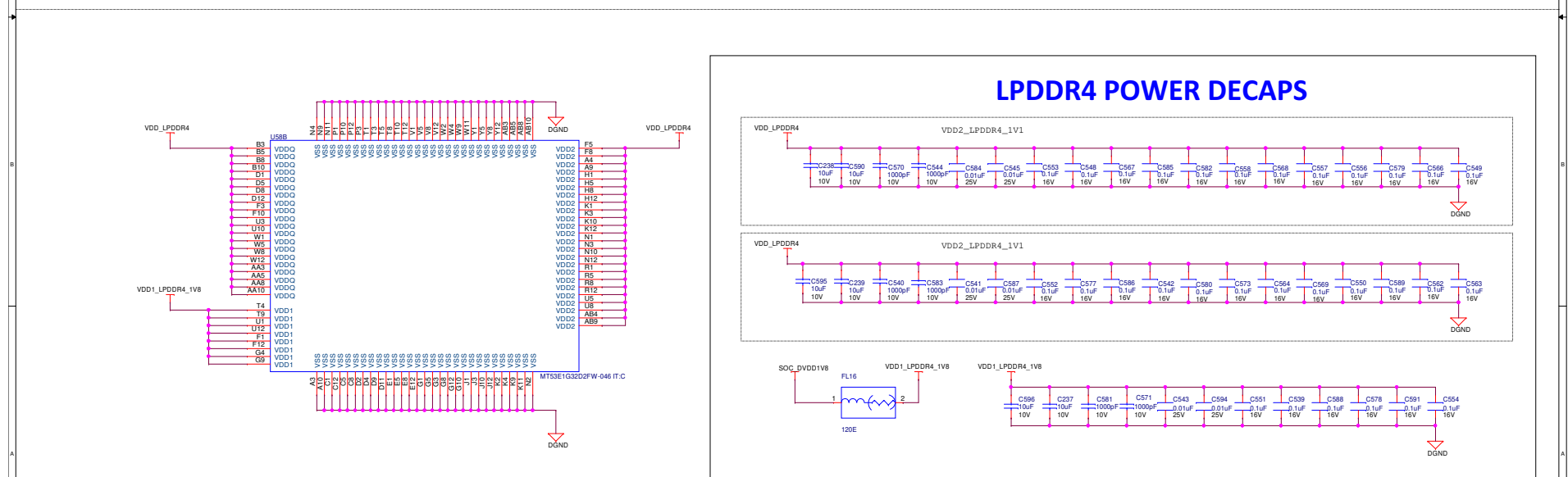
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Title BOOT MODE SWITCHES

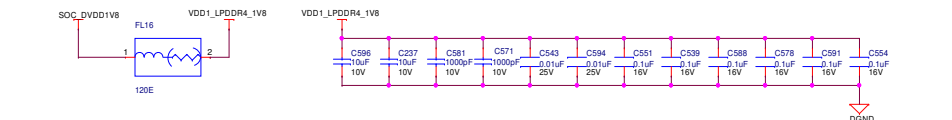
Size	PROC180E1	Rev
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## SOC LPDDR4 INTERFACE



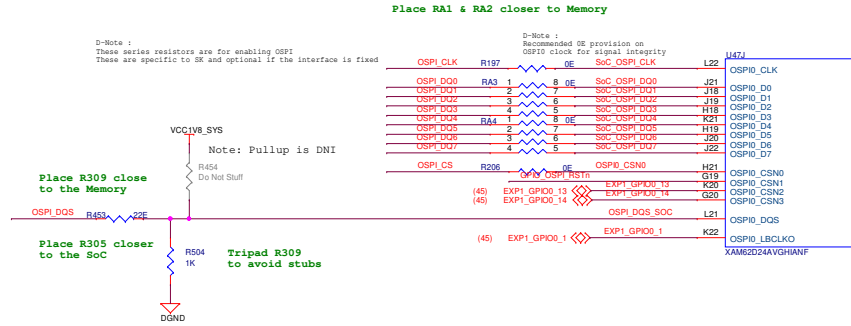
The top diagram shows a decoupling network for VDD2\_LPDDR4\_1V1. It features a series of capacitors connected to VDD2\_LPDDR4\_1V1 and GND. The capacitors are labeled C238, C590, C570, C544, C584, C545, C553, C548, C567, C585, C582, C558, C568, C557, C556, C579, C566, and C549. The values of the capacitors are: C238 (10uF), C590 (10V), C570 (10V), C544 (1000pF), C584 (0.01uF), C545 (0.01uF), C553 (0.1uF), C548 (0.1uF), C567 (0.1uF), C585 (0.1uF), C582 (0.1uF), C558 (0.1uF), C568 (0.1uF), C557 (0.1uF), C556 (0.1uF), C579 (0.1uF), C566 (0.1uF), and C549 (0.1uF). The input is VDD\_LPDDR4 and the output is GND.

The bottom diagram shows a decoupling network for VDD2\_LPDDR4\_1V1. It features a series of capacitors connected to VDD2\_LPDDR4\_1V1 and GND. The capacitors are labeled C595, C239, C540, C583, C541, C587, C552, C577, C586, C542, C580, C573, C564, C569, C550, C589, C562, and C563. The values of the capacitors are: C595 (10uF), C239 (10V), C540 (1000pF), C583 (1000pF), C541 (0.01uF), C587 (0.01uF), C552 (0.1uF), C577 (0.1uF), C586 (0.1uF), C542 (0.1uF), C580 (0.1uF), C573 (0.1uF), C564 (0.1uF), C569 (0.1uF), C550 (0.1uF), C589 (0.1uF), C562 (0.1uF), and C563 (0.1uF). The input is VDD\_LPDDR4 and the output is GND.

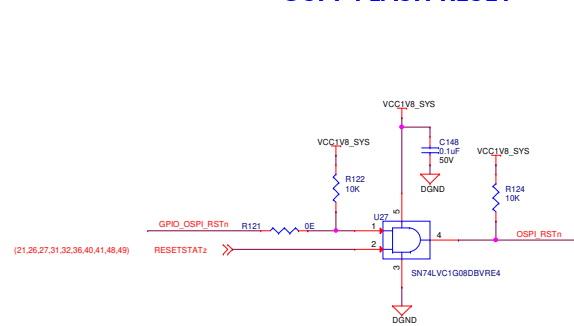


# OSPI INTERFACE

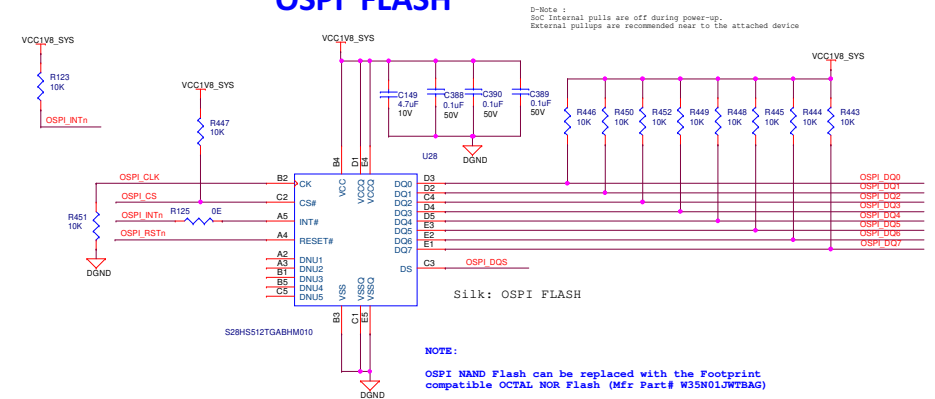
## SOC OSPI INTERFACE



## OSPI FLASH RESET



## OSPI FLASH



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Title OSPI INTERFACE

Size PROC180E1

Date: Monday, May 13, 2024

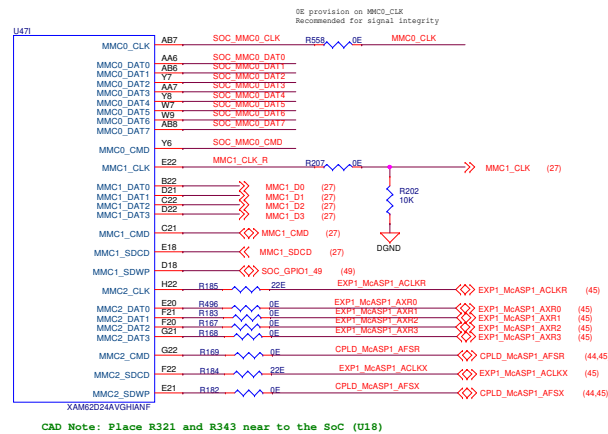
Rev E1

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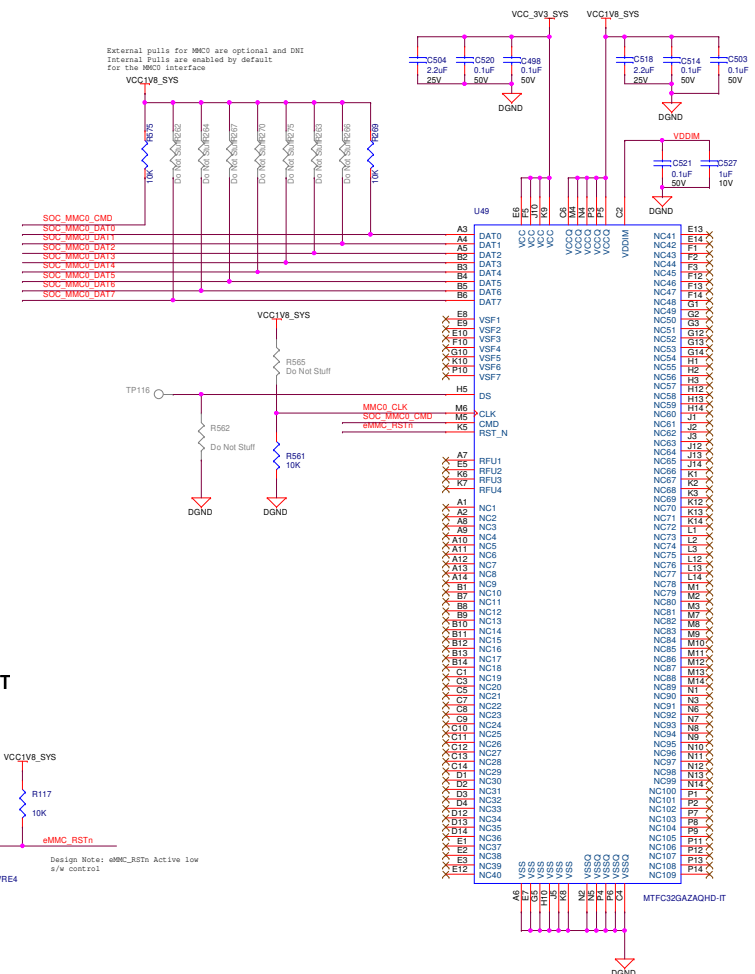
## eMMC INTERFACE

## eMMC FLASH

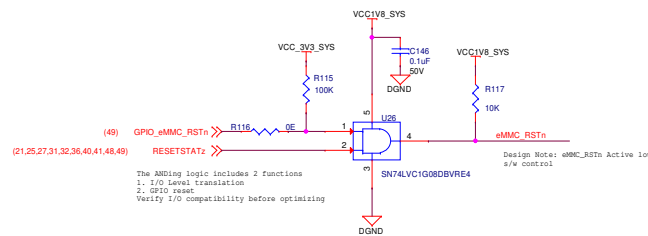
## SOC - MMC Interface



CAD Note: Place R321 and R343 near to the SoC (U18)



## eMMC FLASH RESET



The ANDING logic includes 2 functions

1. I/O Level translation
2. GPIO reset

Verify I/O compatibility before optimizing

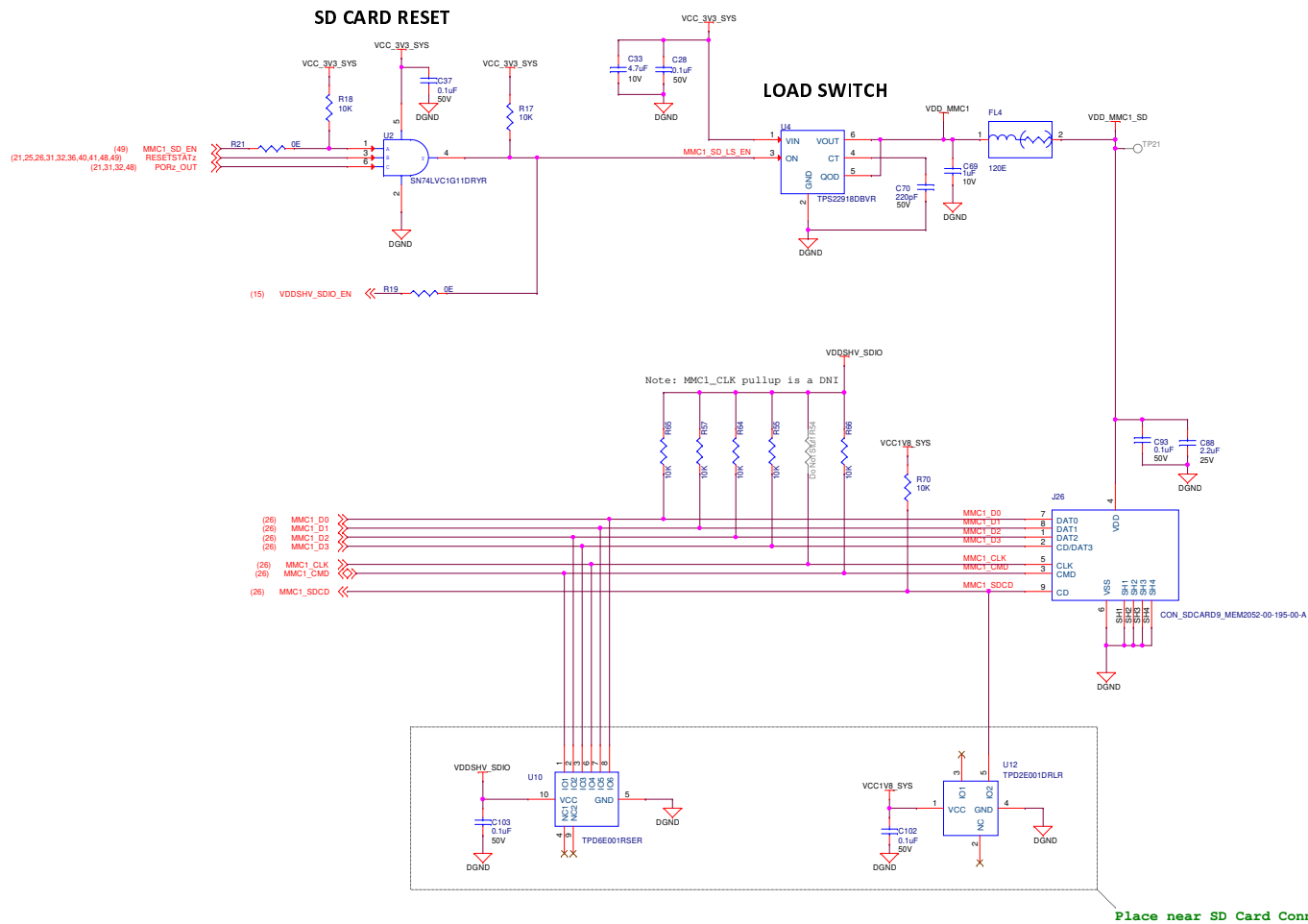
Design Note: eMMC\_RSTn Active low  
s/w control

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Title					eMMC INTERFACE				
Size		PROC180E1					Rev		
C							E1		
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# SD CARD INTERFACE



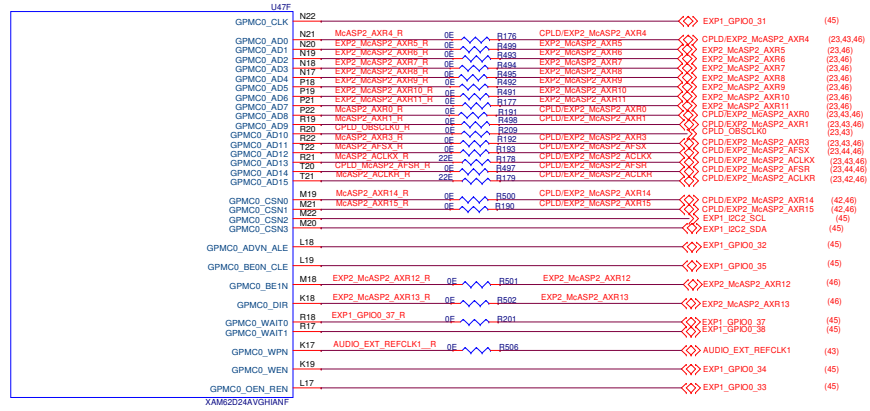
Designed for TI by Mistral Solutions Pvt Ltd



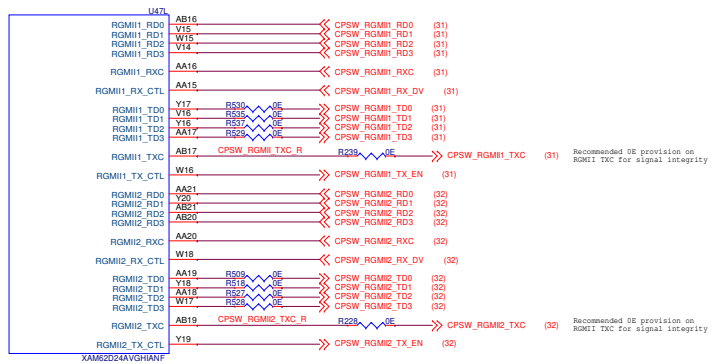
Title SD CARD INTERFACE

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## SOC GPMC



## SOC CPSW3G ETHERNET INTERFACE





U47K	
CSIO_RXP0	W13
CSIO_RXN0	W12
CSIO_RXP1	Y14
CSIO_RXN1	Y13
CSIO_RXP2	AA12
CSIO_RXN2	AA13
CSIO_RXP3	AB10
CSIO_RXN3	AB11
CSIO_RXCLKP	AB13
CSIO_RXCLKN	AB14
RSVD7	V11
RSVD6	U11
CSIO_RXRCALIB	V10

XAM62D24AVGHIANF

L4T2									
MCASP0_AXP10	R20	R188	0E	CPD1/EXPI_MASP0_AXP10		CPD1/EXPI_MASP0_AXP10	(44,45)		
MCASP0_AXP11	R18	R186	0E	EXPI_MASP0_AXP11		EXPI_MASP0_AXP11	(37,45)		
MCASP0_AXP12	R19	R187	0E	EXPI_MASP0_AXP12		EXPI_MASP0_AXP12	(45)		
MCASP0_AXP13	R19	R187	0E	EXPI_MASP0_AXP13		EXPI_MASP0_AXP13	(45)		
MCASP0_AXP14	C19	R171	0E	EXPI_MASP0_AXP14		EXPI_MASP0_AXP14	(45)		
MCASP0_ACLKX	A21	R176	22E	EXPI_MASP0_ACLKX		EXPI_MASP0_ACLKX	(37,45)		
MCASP0_ACLKX	A21	R174	20E	CPD1/EXPI_MASP0_ACLKX		CPD1/EXPI_MASP0_ACLKX	(37,45)		
MCASP0_AFSK	A20	R173	0E	CPD1/EXPI_MASP0_AFSK		CPD1/EXPI_MASP0_AFSK	(44,45)		
MCASP0_AFSK	B21	R189	0E	CPD1/EXPI_MASP0_AFSK		CPD1/EXPI_MASP0_AFSK	(44,45)		
XAM02Q424VGHIANF									

Figure 10 shows the pin connections for the XAM62024VGHIANF. The connections are as follows:

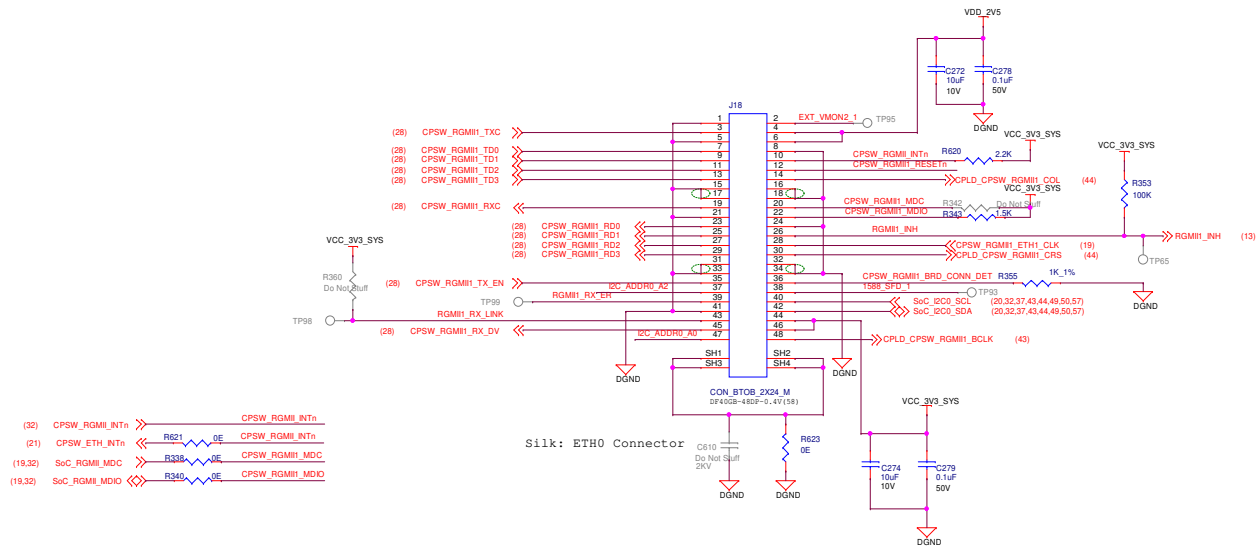
- U47B to Soc\_EMU0 (56,58)
- EMU1 to Soc\_EMU1 (56,58)
- TCK to Soc\_TCK (56,58)
- TDI to Soc\_TDI (56,58)
- TMS to Soc\_TMS (56,58)
- TDO to Soc\_TDO (56,58)
- TRSTN to Soc\_TRST# (56,58)

The Soc\_TRST# signal is also connected to a 4.7k resistor and a DQDN0 pin.

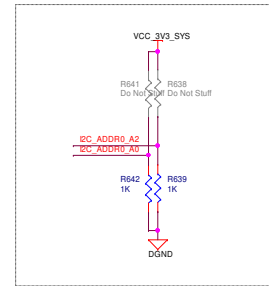
[illegible]

U47M			
GPIO0_45	I22	EXP2_GPIO_45	(46)
GPIO0_46	I21	EXP2_GPIO_46	(46)
GPIO0_47	I19	EXP2_GPIO_47	(46)
GPIO0_48	I20	EXP2_GPIO_48	(46)
GPIO0_49	I18	UART1_RXD	(54)
GPIO0_50	I22	UART1_TXD	(54)
GPIO0_51	I21	UART1_RXD	(45)
GPIO0_52	I20	UART1_TXD	(45)
GPIO0_53	I19	UART1_RXD	(46)
GPIO0_54	I18	UART1_TXD	(46)
GPIO0_55	I22	EXP2_GPIO_56	(46)
GPIO0_56	I21	EXP2_GPIO_57	(46)
GPIO0_57	I20	EXP2_GPIO_58	(46)
GPIO0_58	I19	EXP2_GPIO_59	(46)
GPIO0_59	I18	EXP2_GPIO_60	(46)
GPIO0_60	I17	VSEL_30_S0C_1VB	(43)
GPIO0_61	I16	GPIO1_25_I1VB	(46)
GPIO0_62	I15		
GPIO0_63	I14		
GPIO0_64	I13		

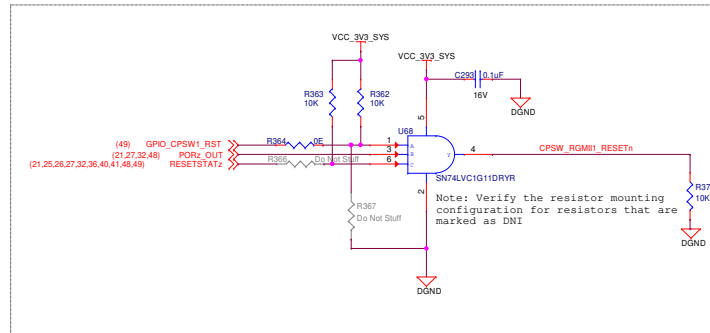
# ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 1



## I2C Address Strap



## CPSW3G RGMII 1 RESET



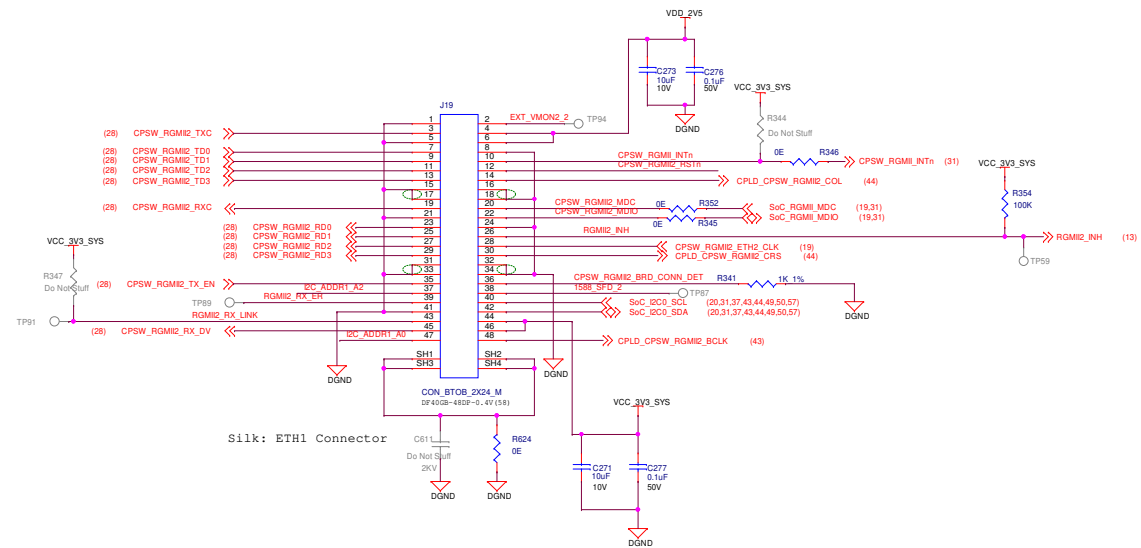
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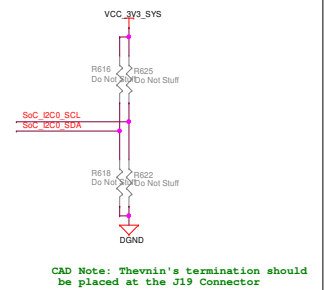
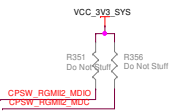
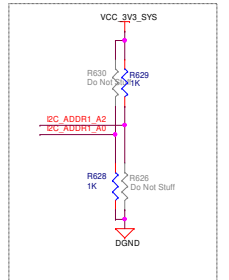
Title: ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 1

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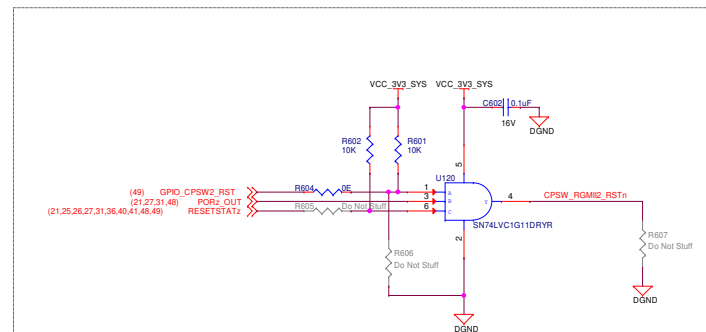
## ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 2



## I2C Address Strap

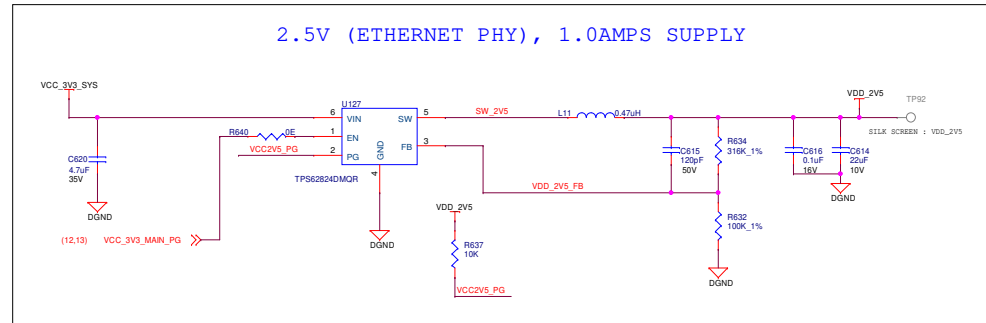


## CPSW3G RGMII 2 RESET



Note: Verify the resistor mounting configuration for resistors that are marked as DNI

## POWER SUPPLY (CORE) FOR ETHERNET PHY



D-Note : 2.5V Power supply for Ethernet PHY is generated by the PMIC

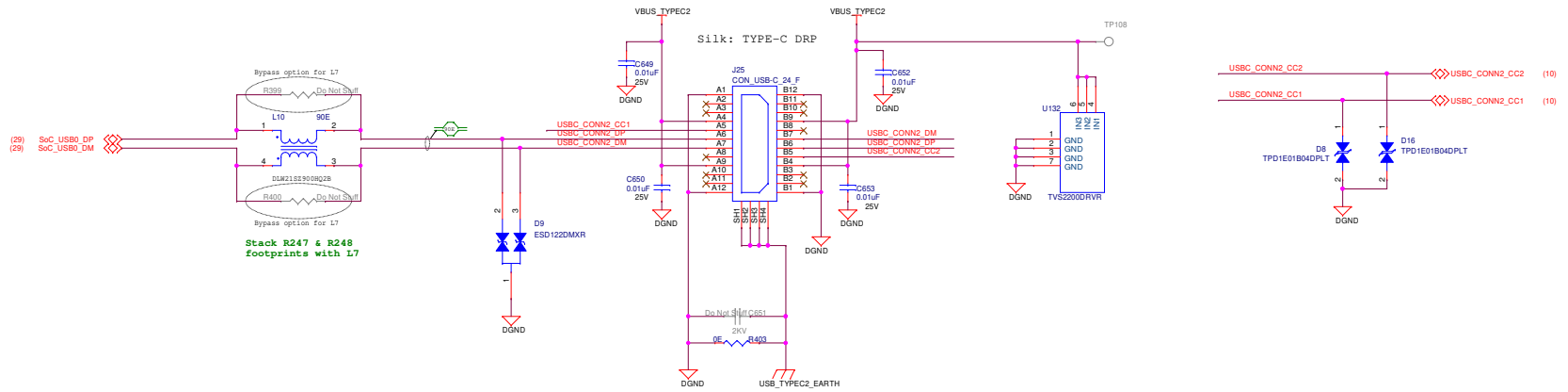
Designed for TI by Mistral Solutions Pvt Ltd



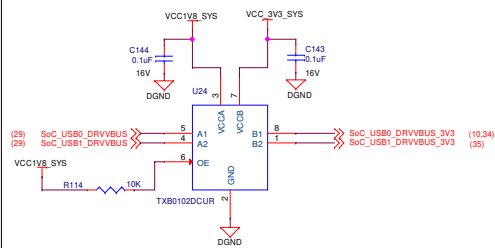
Title POWER SUPPLY (CORE) FOR ETHERNET PHY

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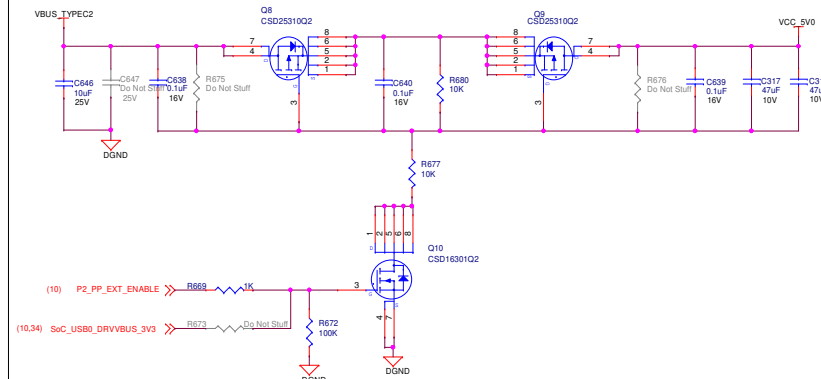
# USB0 TYPE-C DRP



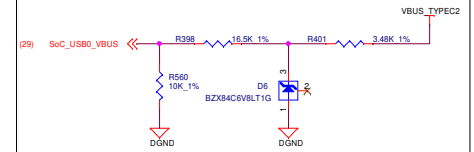
## USB\_DRV BUS LEVEL TRANSLATOR



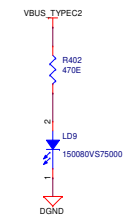
## EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



Note: Refer data sheet USB VBUS Design Guidelines section.



## POWER INDICATION LED: VBUS\_TYPEC2



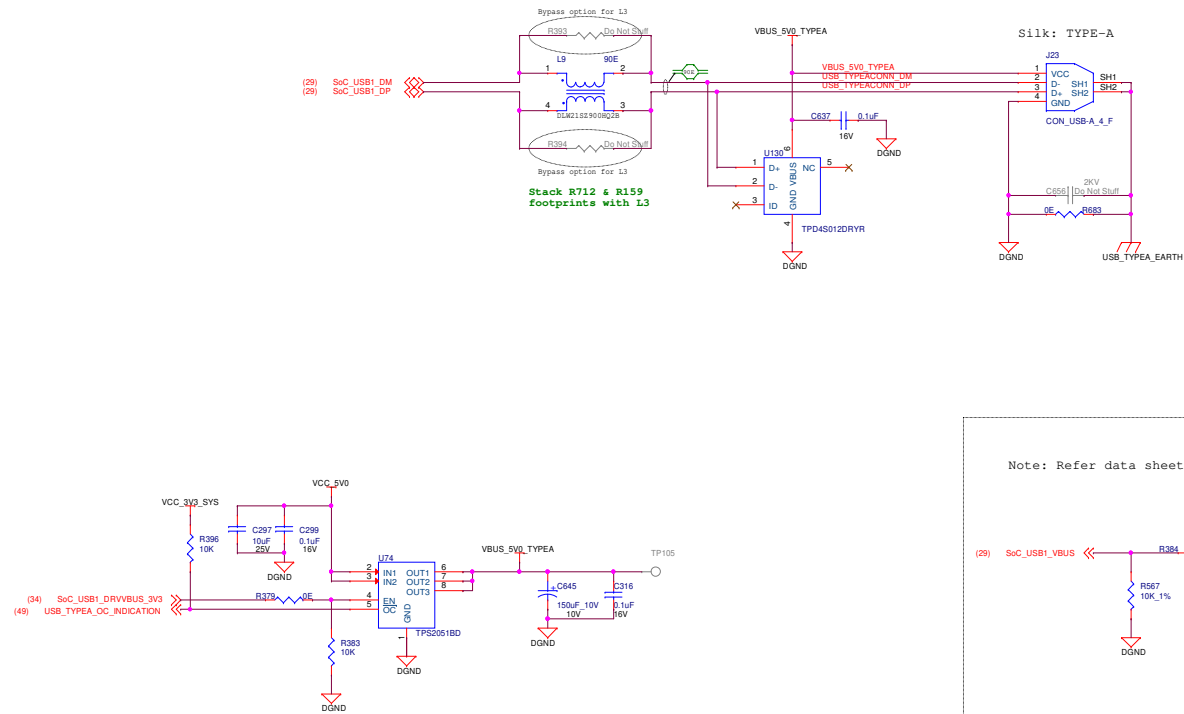
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Title USB0 TYPE-C DRP

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# USB1 TYPE-A



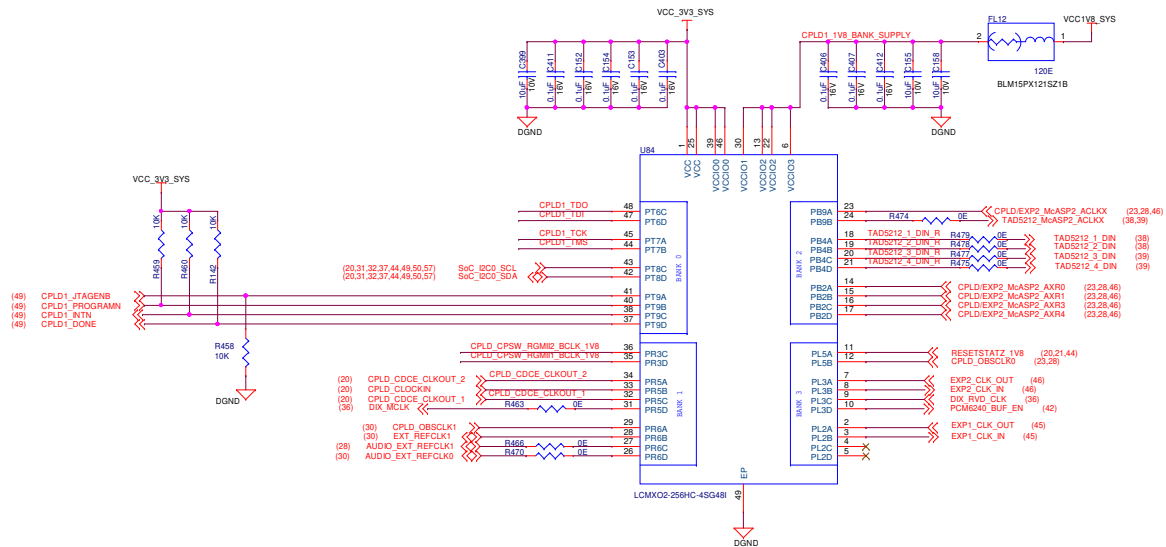
Designed for TI by Mistral Solutions Pvt Ltd



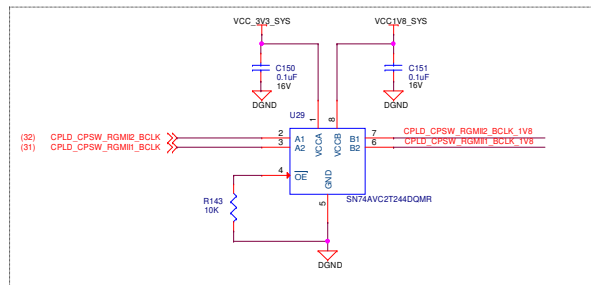
Title USB1 TYPE-A

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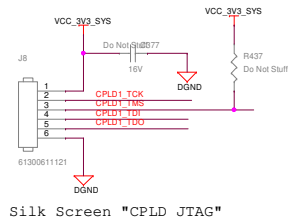
## CPLD 1



## CPLD 1 LEVEL TRANSLATOR



## PROGRAMMING HEADER



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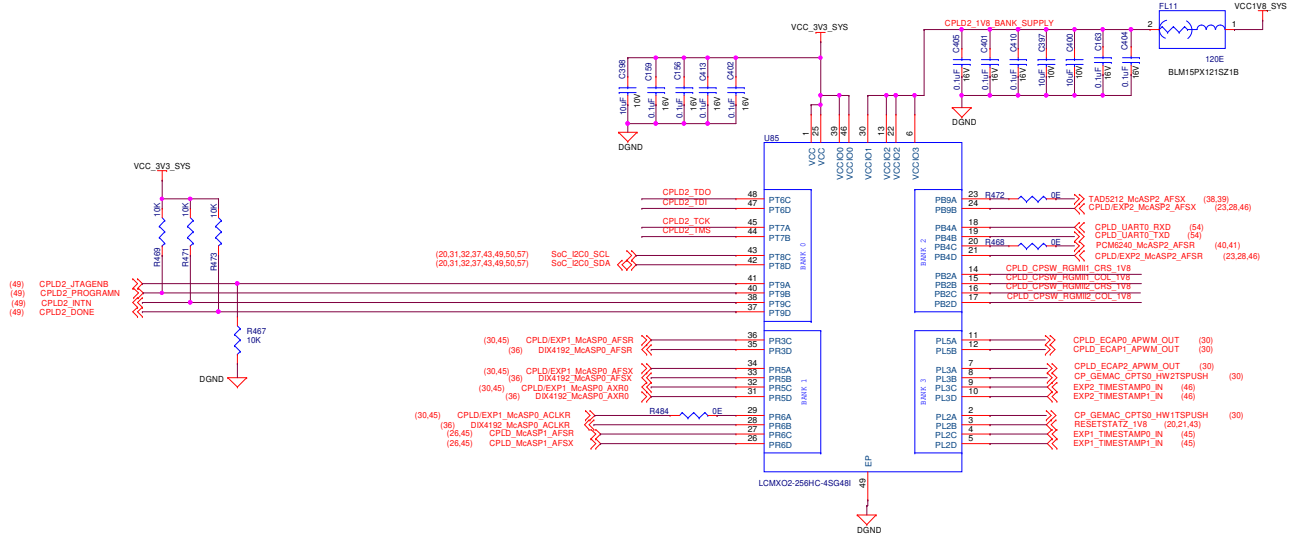


<b>Title</b>	<b>CPLD 1</b>
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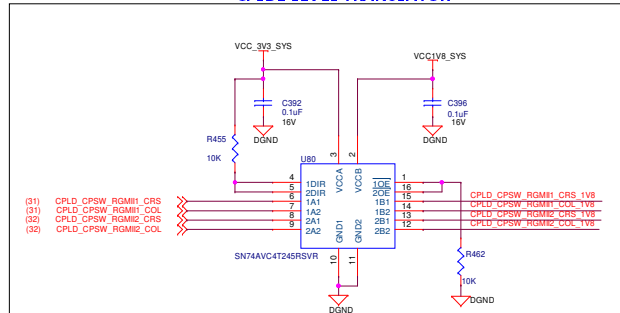
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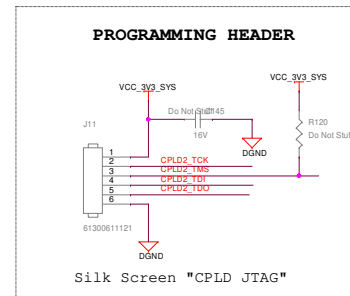
## CPLD 2



## CPLD2 LEVEL TRANSLATOR



## PROGRAMMING HEADER



Silk Screen "CPLD JTAG"

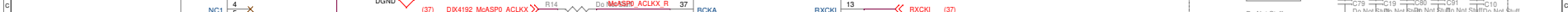
Designed for TI by Mistral Solutions Pvt Ltd



<b>Title</b>	<b>CPLD 2</b>
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Size	PROC180E1	Rev
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Date:	Monday, May 13, 2024	Sheet 37 of 59

5	4	3	2	1
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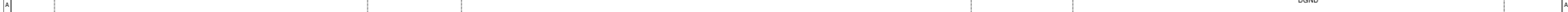


## DIX Supply & Decaps

The diagram illustrates the DIX supply and decoupling circuit. It features two main power supply rails: **VCC1V8\_SYS** and **VCC1V8\_VDD18**. The **VCC1V8\_SYS** rail is connected to pin 1 of a component labeled **FL5**, with a note "Do Not Stuff". The **VCC1V8\_VDD18** rail is connected to pin 2 of **FL5**. A series of decoupling capacitors (**C19**, **C18**, **C88**, **C81**, **C10**) are connected between the **VCC1V8\_VDD18** rail and a common **DGNND** ground. Each capacitor has a value of 10V. Notes "Do Not Stuff" are placed below each capacitor. A second component, **FL3**, is shown with **VCC3V3\_SYS** connected to pin 1 and **DIX3V3\_SYS** connected to pin 2. Decoupling capacitors **C58**, **C39**, **C59**, and **C36** are connected between **DIX3V3\_SYS** and **DGNND**, each with a value of 10V and a "Do Not Stuff" note.



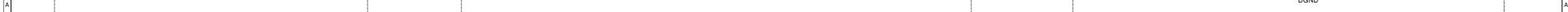
# DEVICE STRAP





## DIX4192 RESET

The schematic diagram illustrates the RESET circuit for the DIX4192 microcontroller (U13). The microcontroller has four pins shown: pin 1, pin 2, pin 4, and pin 5. Pin 1 is connected to the VCC1V8\_VDD18 supply. Pin 2 is connected to a pull-up resistor R79 (10k) to VCC1V8\_VDD18 and to the GPIO\_DIX\_RST signal. Pin 4 is connected to a pull-up resistor R59 (10k) to VCC1V8\_VDD18 and to the DIX\_RESETn signal. Pin 5 is connected to GND. A capacitor C94 (10V) is connected between VCC1V8\_VDD18 and GND. The signals (49) GPIO\_DIX\_RST and (21,25,26,27,31,32,40,41,48,49) RESETStAt2 are shown as inputs to the microcontroller.

## DIT & DIR COAXIAL INPUT



Designed for TI by Mistral Solutions Pvt Ltd		Title		AUDIO - DIGITAL IN & OUT, OPTICAL IN -1	
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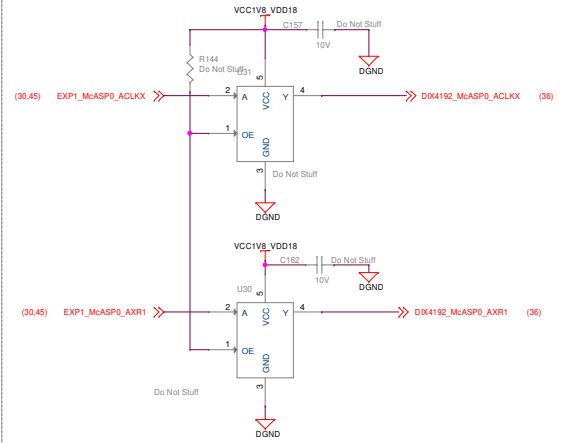


MISTRA

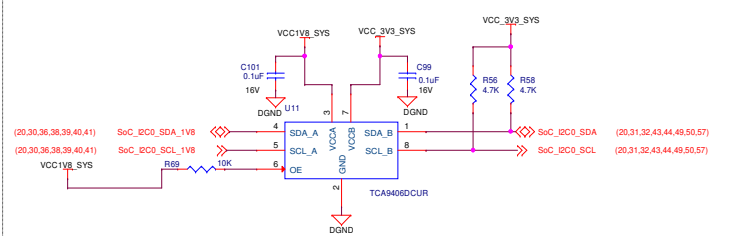
Size	PROC180E1	Rev
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AUDIO - DIGITAL IN & OUT, OPTICAL IN - 2

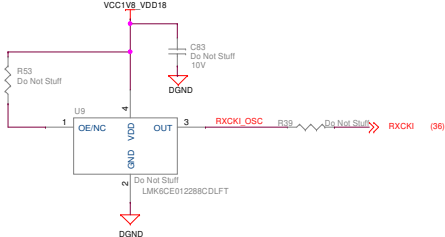
BUFFERS FOR DIX4192



I2C LEVEL TRANSLATOR



DIX4192 CLOCKING



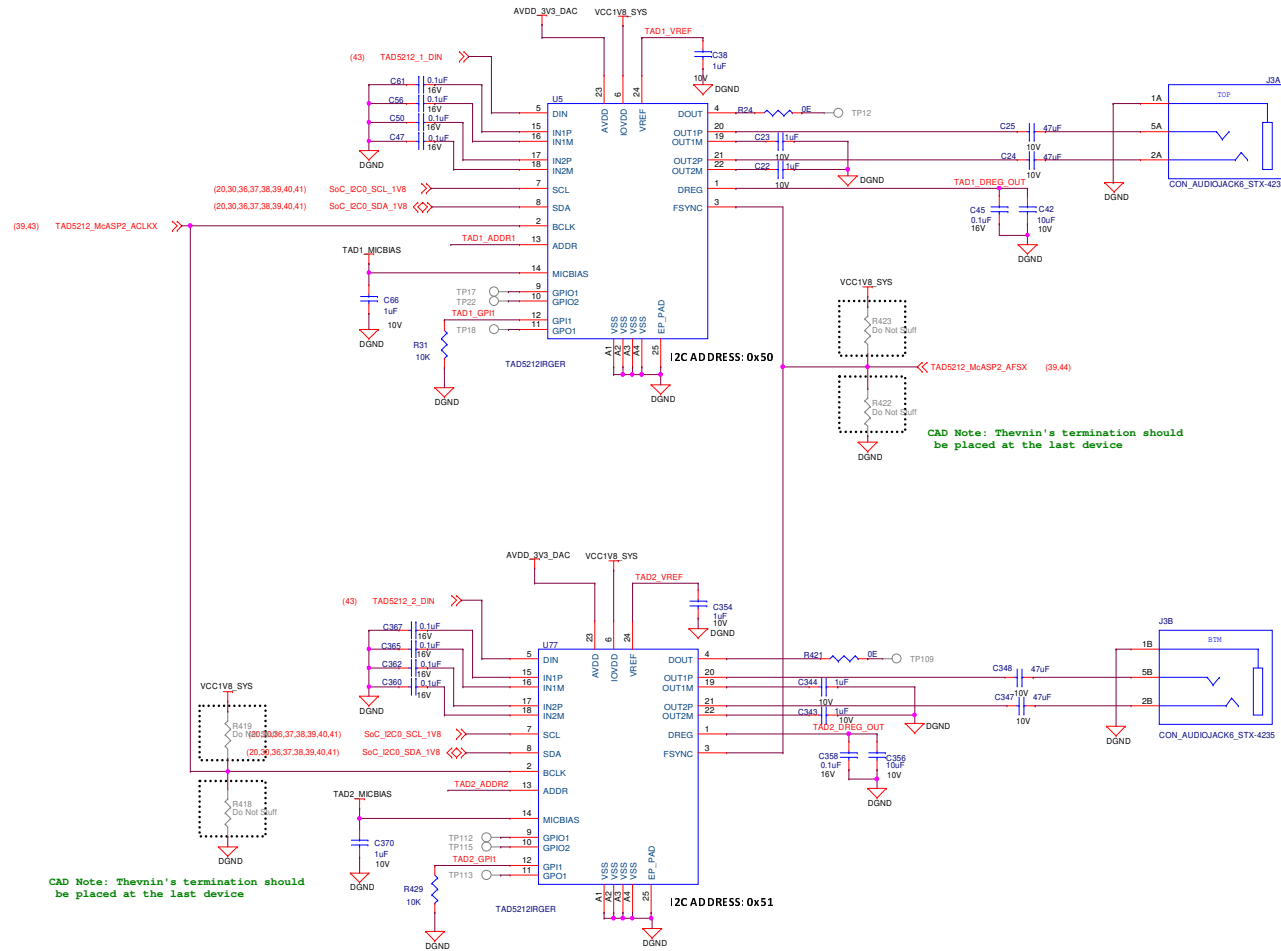
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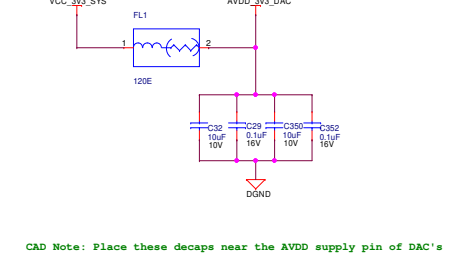
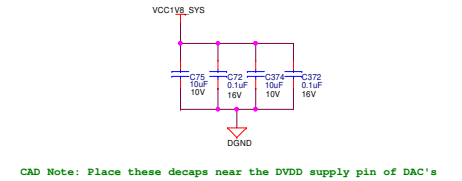
Title AUDIO - DIGITAL IN & OUT, OPTICAL IN - 2

Size	Rev
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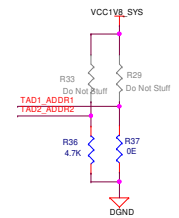
# AUDIO - STEREO LINEOUT - 1



## DAC Supply & Decaps



## DAC I2C Address Straps



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Title AUDIO - STEREO LINEOUT - 1		
Size	PROC180E1	Rev
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## AUDIO - STEREO LINEOUT - 2

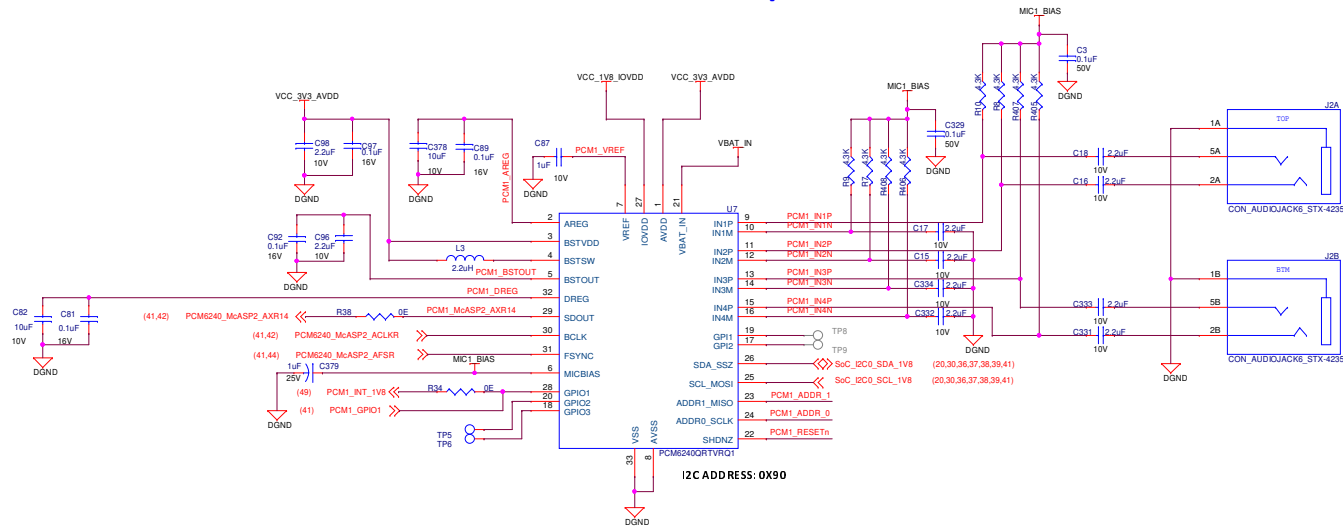
CAD Note: Place these decaps near the DVDD supply pin of DAC's

Title	AUDIO - STEREO LINEOUT - 2
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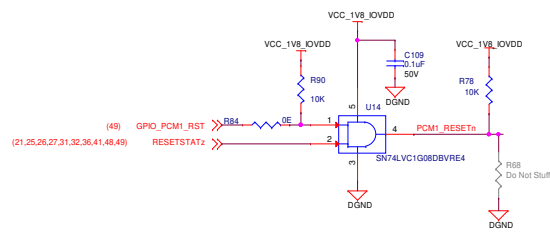


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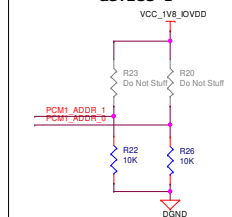
# AUDIO - MICROPHONE/LINE IN 1



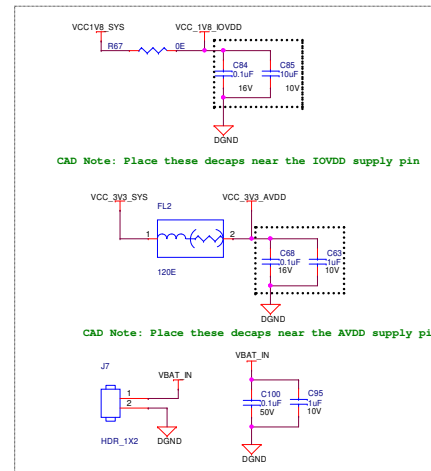
## PCM1 RESET



## I2C address selection device 1



## ADC Supply & Decaps



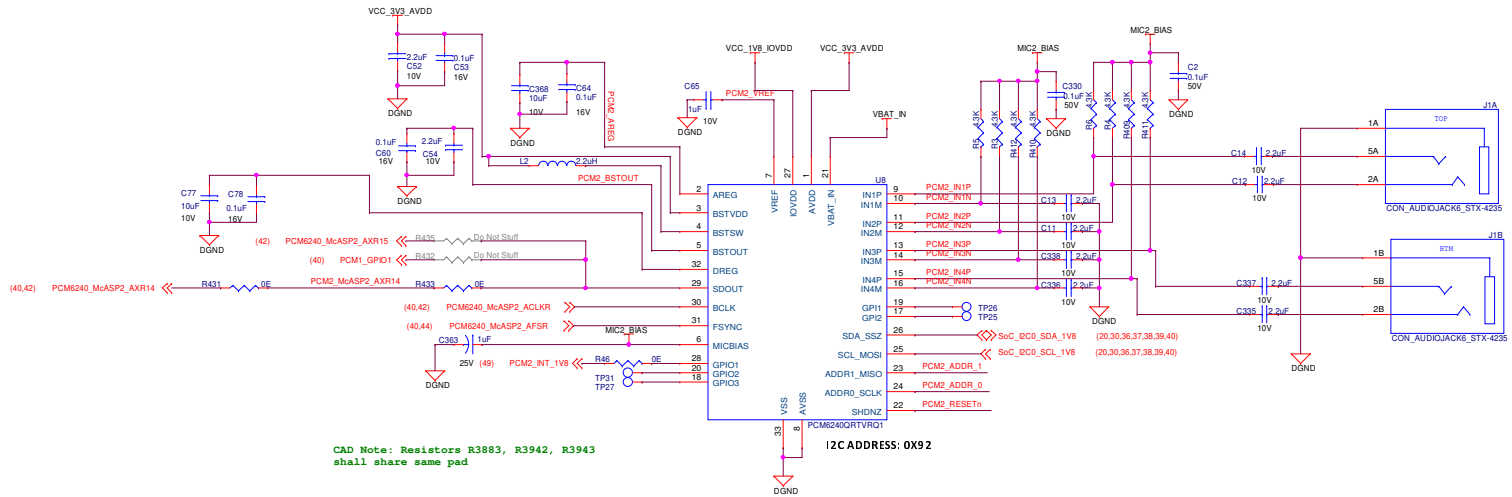
Designed for TI by Mistral Solutions Pvt Ltd



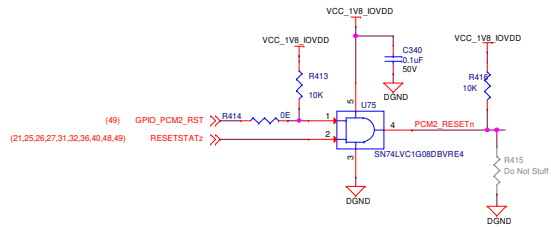
Title AUDIO - MICROPHONE/LINE IN 1

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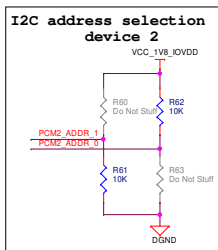
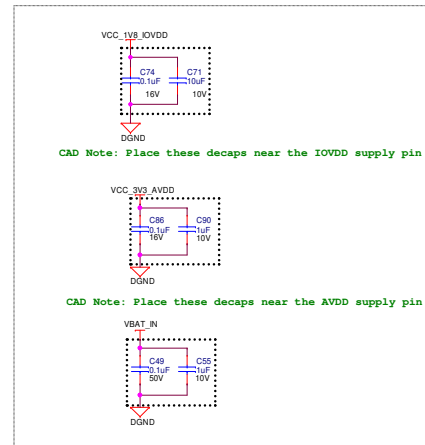
## AUDIO - MICROPHONE/LINE IN 2



## PCM2 RESET



## ADC Supply & Decaps



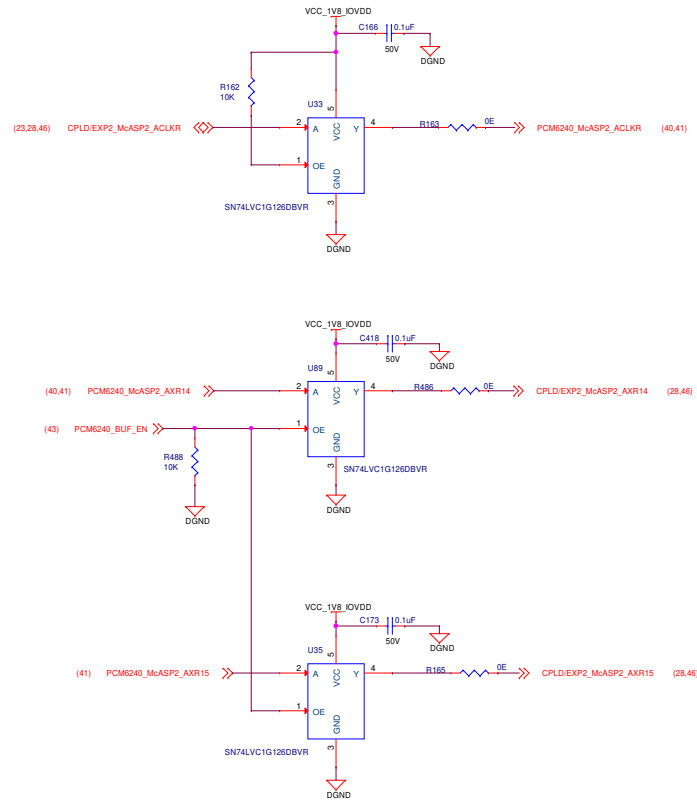
Designed for TI by Mistral Solutions Pvt Ltd



Title	AUDIO - MICROPHONE/LINE IN 2
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## PCM6240 BUFFERS



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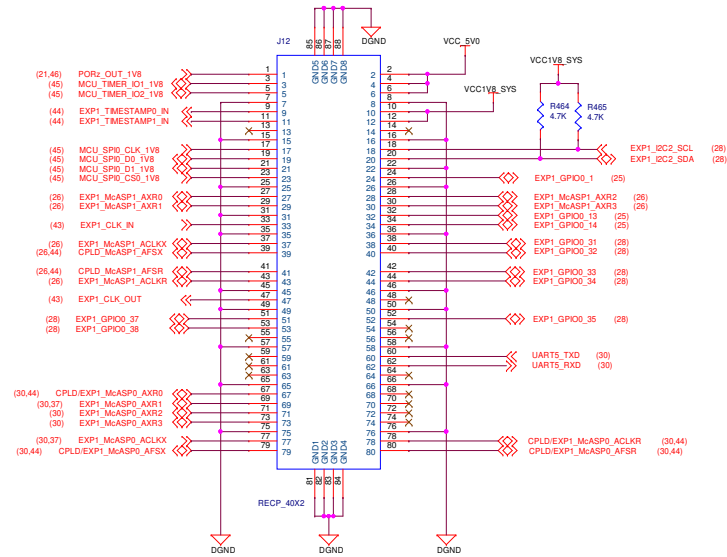


Title PCM6240 BUFFERS

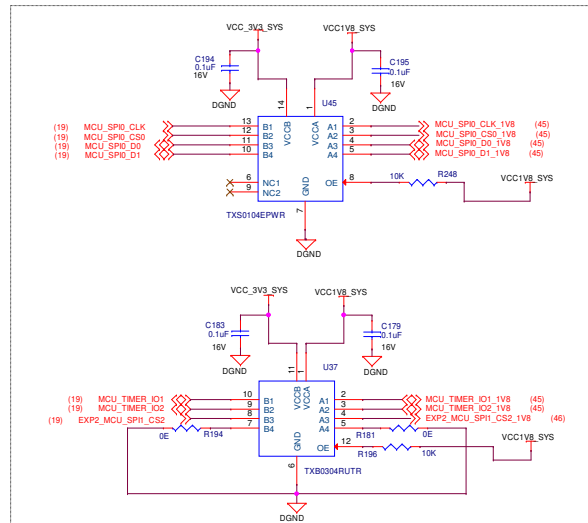
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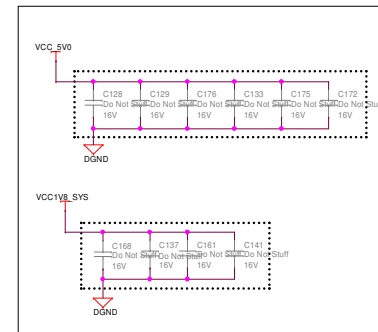
# AUDIO EXPANSION CONNECTOR #1



## AEC1 LEVEL TRANSLATORS



## AUDIO EXPANSION DECAPS



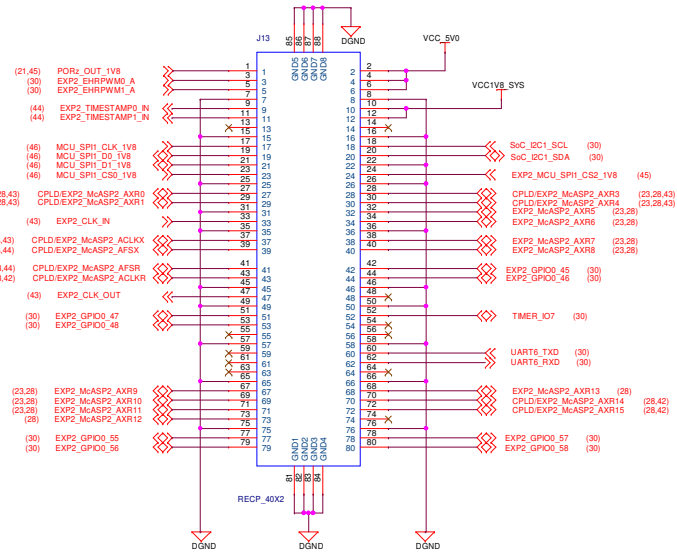
Designed for TI by Mistral Solutions Pvt Ltd



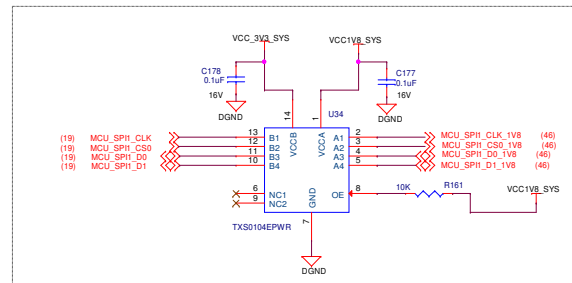
Title AUDIO EXPANSION CONNECTOR #1

Size	Rev
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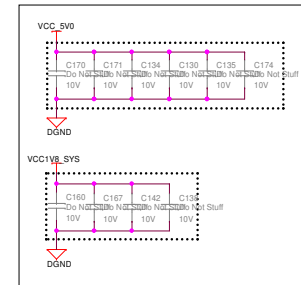
## AUDIO EXPANSION CONNECTOR #2



### AEC2 LEVEL TRANSLATOR



### AUDIO EXPANSION DECAPS



Designed for TI by Mistral Solutions Pvt Ltd



Title AUDIO EXPANSION CONNECTOR #2

Size	Rev
C	E1
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**CAN TRANSCEIVER**

The image displays two circuit diagrams for CAN transceivers, labeled CAN0 and CAN1, both utilizing the TCAN3413DR IC.

**CAN0 Transceiver Diagram:**

- Power Supply:** VCC1V8\_SYS and VCC\_3V3\_SYS are connected to the IC. VCC1V8\_SYS is connected to pin 1 (TXD) and pin 4 (RXD). VCC\_3V3\_SYS is connected to pin 5 (SHDN/VIO) and pin 8 (STB).
- Signal Connections:**
  - MCAN0\_TX (pin 1) is connected to R82 (0E) and MCAN0\_TX\_R (pin 4).
  - MCAN0\_RX (pin 4) is connected to R81 (3E) and MCAN0\_RX\_R (pin 1).
  - IO\_MCAN0\_STB (pin 8) is connected to R162 (0E) and MCAN0\_STB (pin 5).
- Termination and Filtering:** R93 (59E\_1%) and R88 (59E\_1%) are connected to the CAN\_H and CAN\_L pins, respectively. C106 (0.1uF) and C113 (0.1uF) are connected to the VCC pins.
- Output:** The CAN\_H and CAN\_L pins are connected to a differential pair of wires (MCAN0\_CAN\_H and MCAN0\_CAN\_L) which are terminated with R107 (4700pF) and connected to a connector J9.

**CAN1 Transceiver Diagram:**

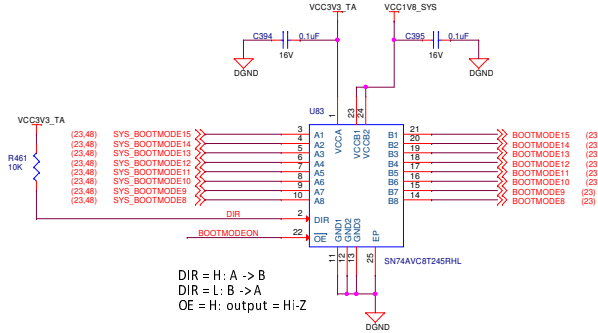
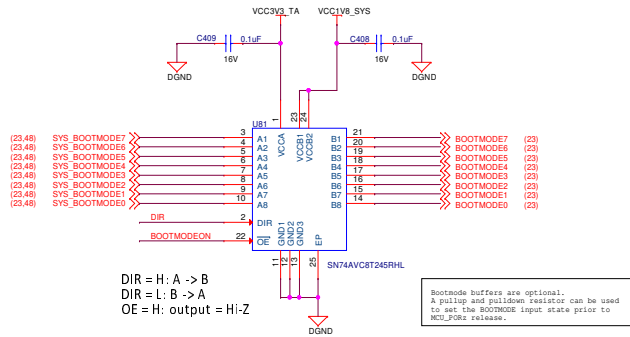
- Power Supply:** VCC\_3V3\_SYS is connected to the IC. VCC\_3V3\_SYS is connected to pin 1 (TXD) and pin 4 (RXD).
- Signal Connections:**
  - MCU\_MCAN0\_TX (pin 1) is connected to R273 (0E) and MCAN1\_TX\_R (pin 4).
  - MCU\_MCAN0\_RX (pin 4) is connected to R189 (3E) and MCAN1\_RX\_R (pin 1).
  - IO\_MCAN1\_STB (pin 8) is connected to R223 (0E) and MCAN1\_STB (pin 5).
- Termination and Filtering:** R215 (59E\_1%) and R208 (59E\_1%) are connected to the CAN\_H and CAN\_L pins, respectively. C184 (0.1uF) and C185 (0.1uF) are connected to the VCC pins.
- Output:** The CAN\_H and CAN\_L pins are connected to a differential pair of wires (MCAN1\_CAN\_H and MCAN1\_CAN\_L) which are terminated with C180 (4700pF) and connected to a connector J15.



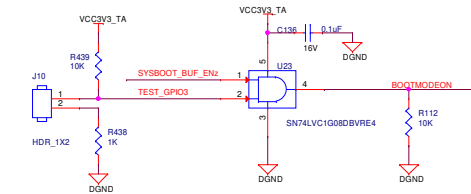
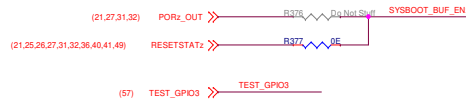
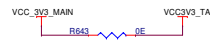
Size	PROC180E1	Rev
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# BOOTMODE BUFFERS AND IO EXPANDERS

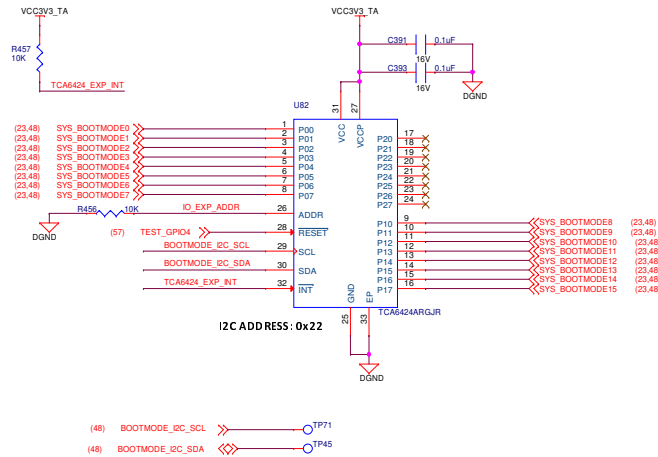
## BOOT MODE BUFFERS



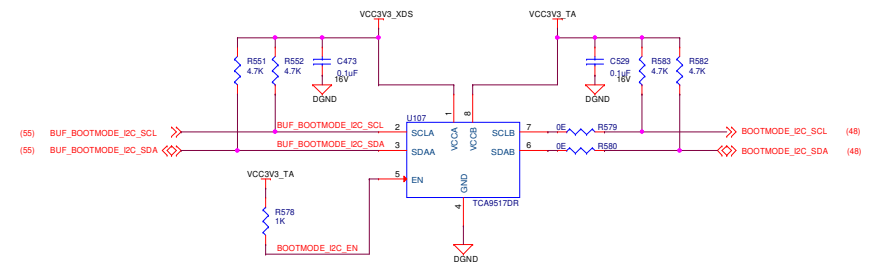
## TEST AUTOMATION SUPPLY



## BOOTMODE IO EXPANDER



## BOOTMODE I2C BUS BUFFER



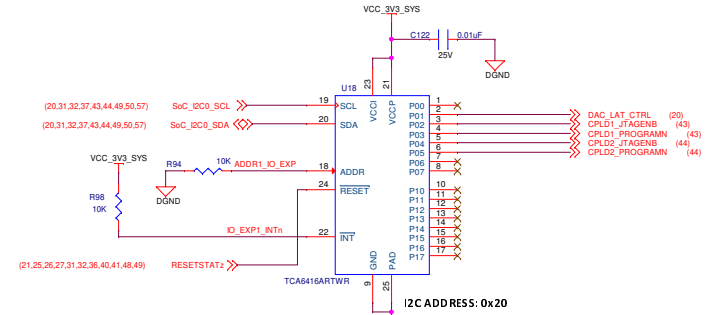
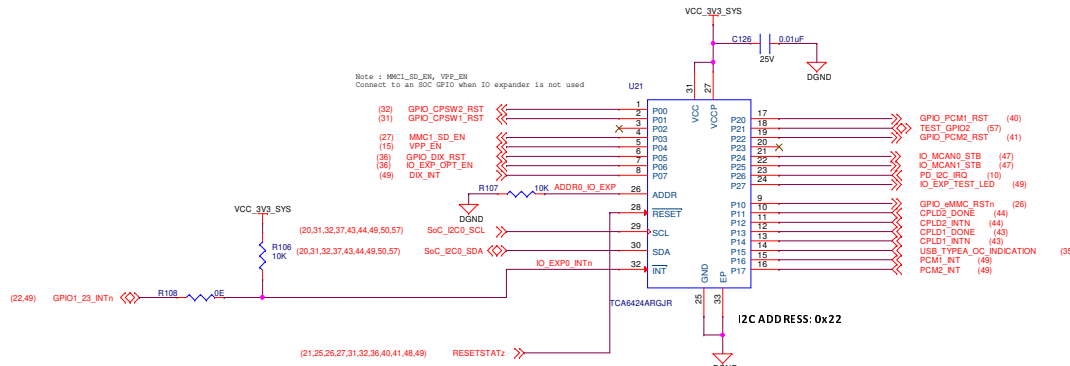
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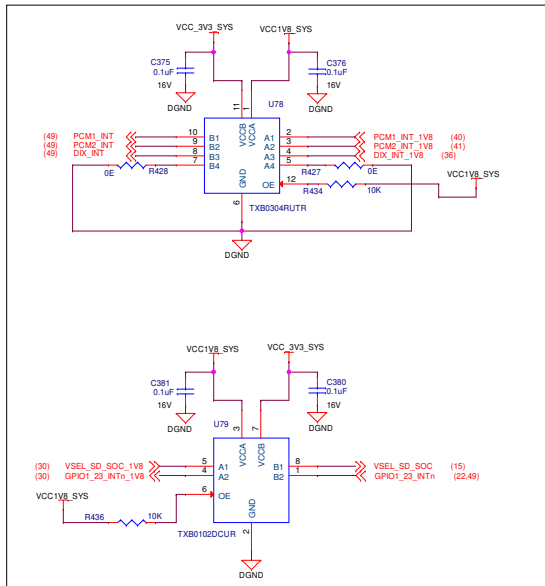
Title BOOT MODE BUFFER & IO EXPANDERS

Size	Rev
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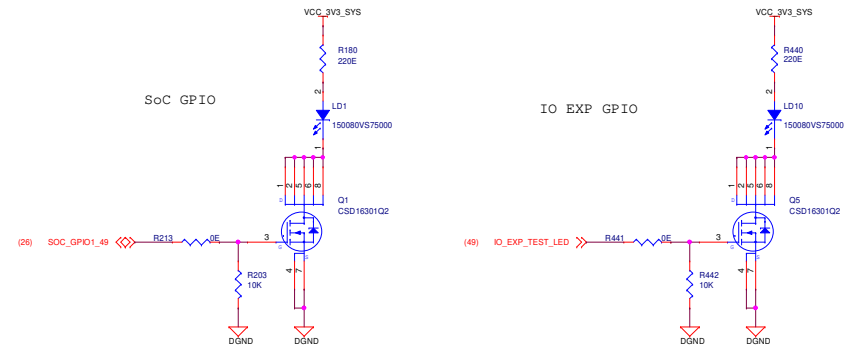
## IO EXPANDER



## LEVEL TRANSLATOR



## USER TEST LEDS



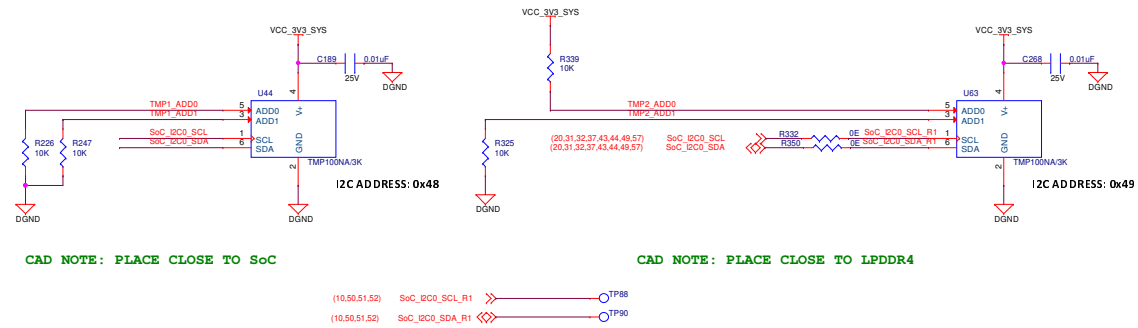
Designed for TI by Mistral Solutions Pvt Ltd



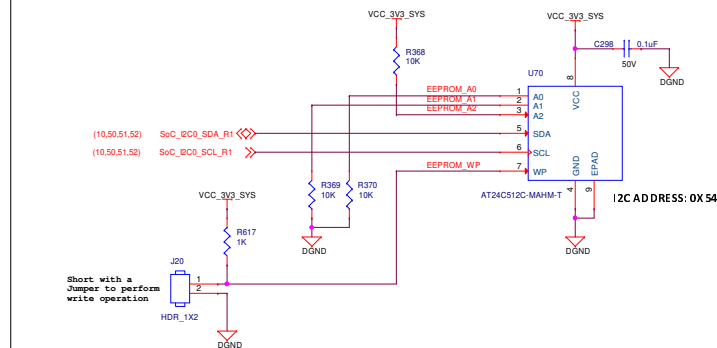
Title IO EXPANDER & USER TEST LEDS

Size	Rev
C	E1
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## TEMPERATURE SENSORS



## BOARD ID EEPROM



PROC180E1

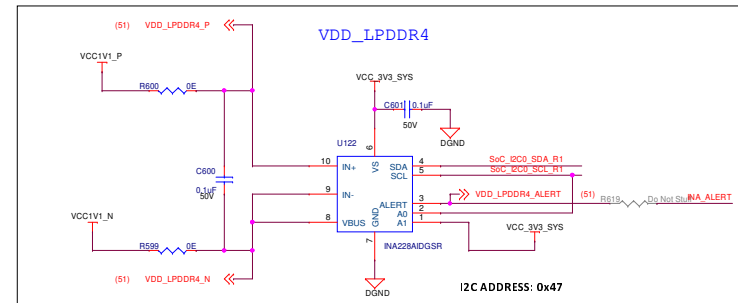
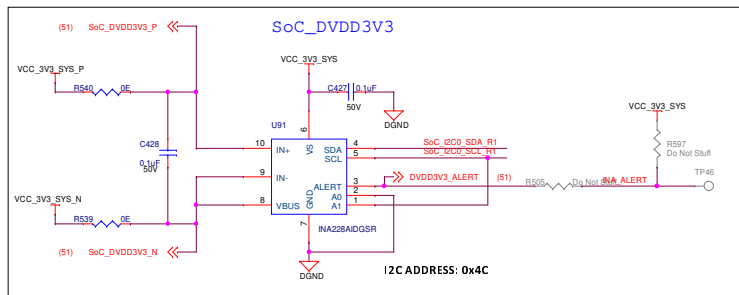
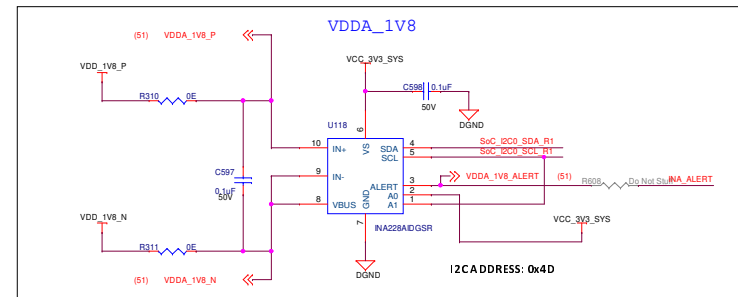
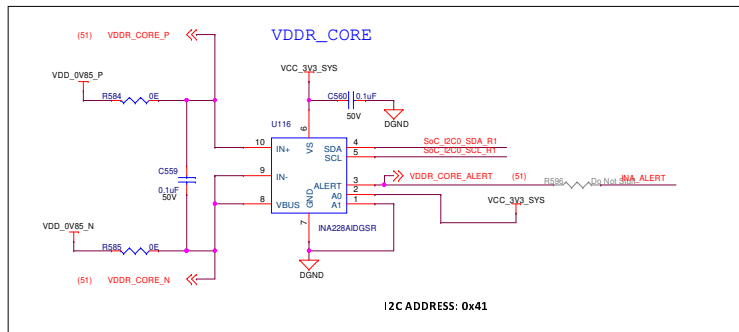
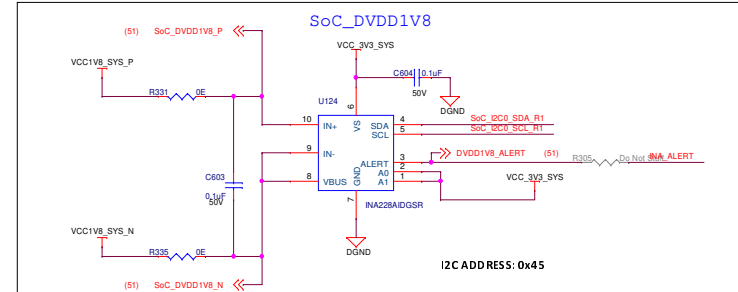
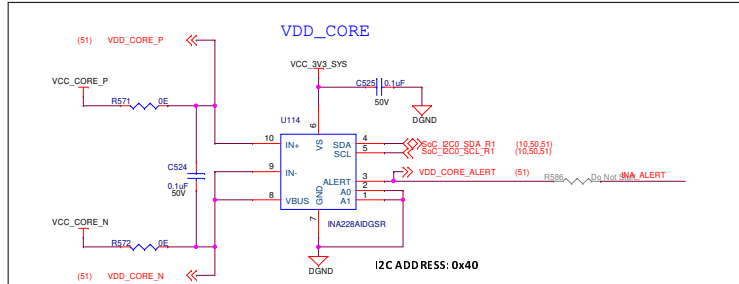
Designed for TI by Mistral Solutions Pvt Ltd



Title: TEMPERATURE SENSORS & BOARD ID EEPROM

Size	Rev
C	E1
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# CURRENT MONITORING DEVICES - 1



Note: The design supports current/voltage measurements using either INA228 or INA231. INA228 will be populated on the the SK (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_OV85	VDDR_CORE	41
VCC3V3_SYS	SoC_DVDD3V3	4C
VCC1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

PROC180E1

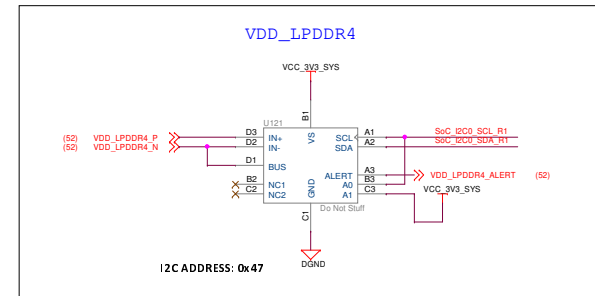
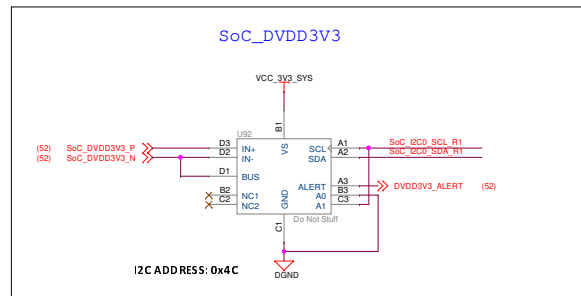
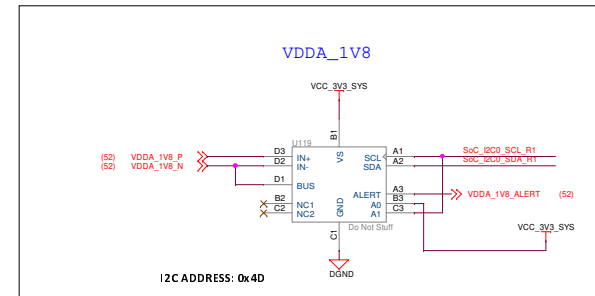
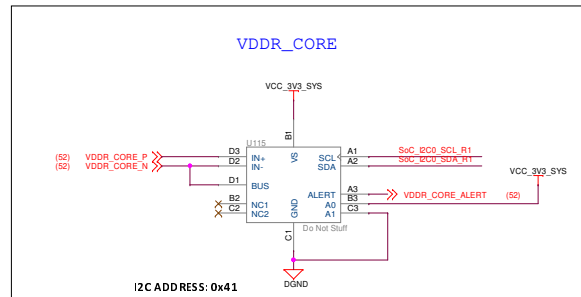
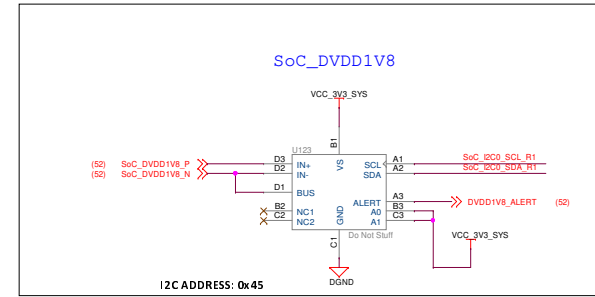
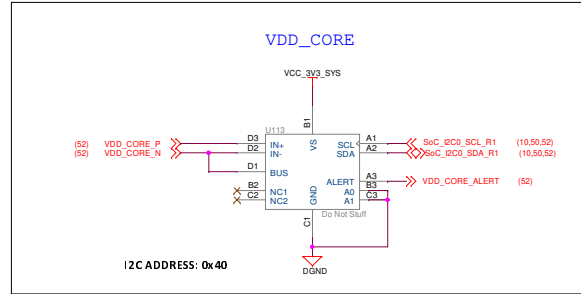
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Title CURRENT MONITORING DEVICES - 1

Size	Rev
C	PROC180E1
Date: Monday, May 13, 2024	Sheet 51 of 59

# CURRENT MONITORING DEVICES - 1



Note: The design supports current/voltage measurements using either INA228 or INA231. INA228 will be populated on the the SK (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_OV85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

PROC180E1

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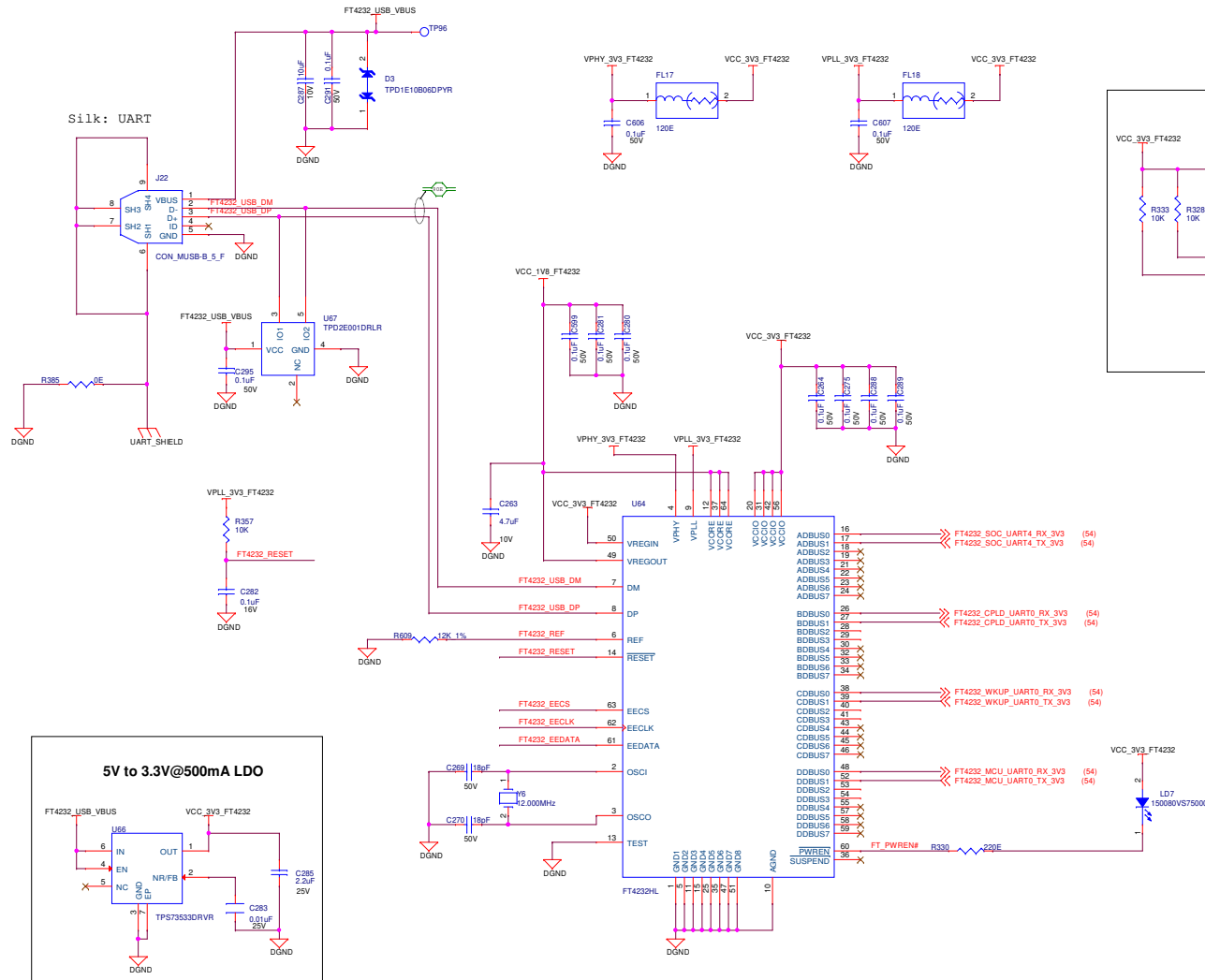


Title CURRENT MONITORING DEVICES - 2

Size	Rev
C	E1
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# USB TO UART BRIDGE



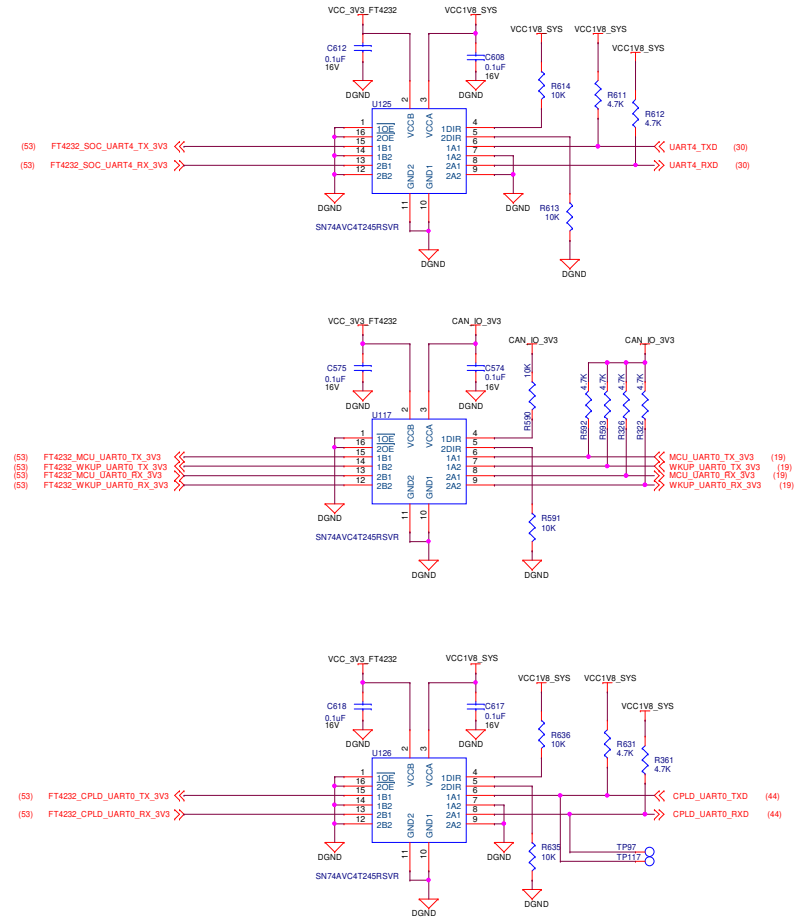
Designed for TI by Mistral Solutions Pvt Ltd



Title FT4232 UART to USB BRIDGE

Size	Rev
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# FT4232 UART BUFFERS



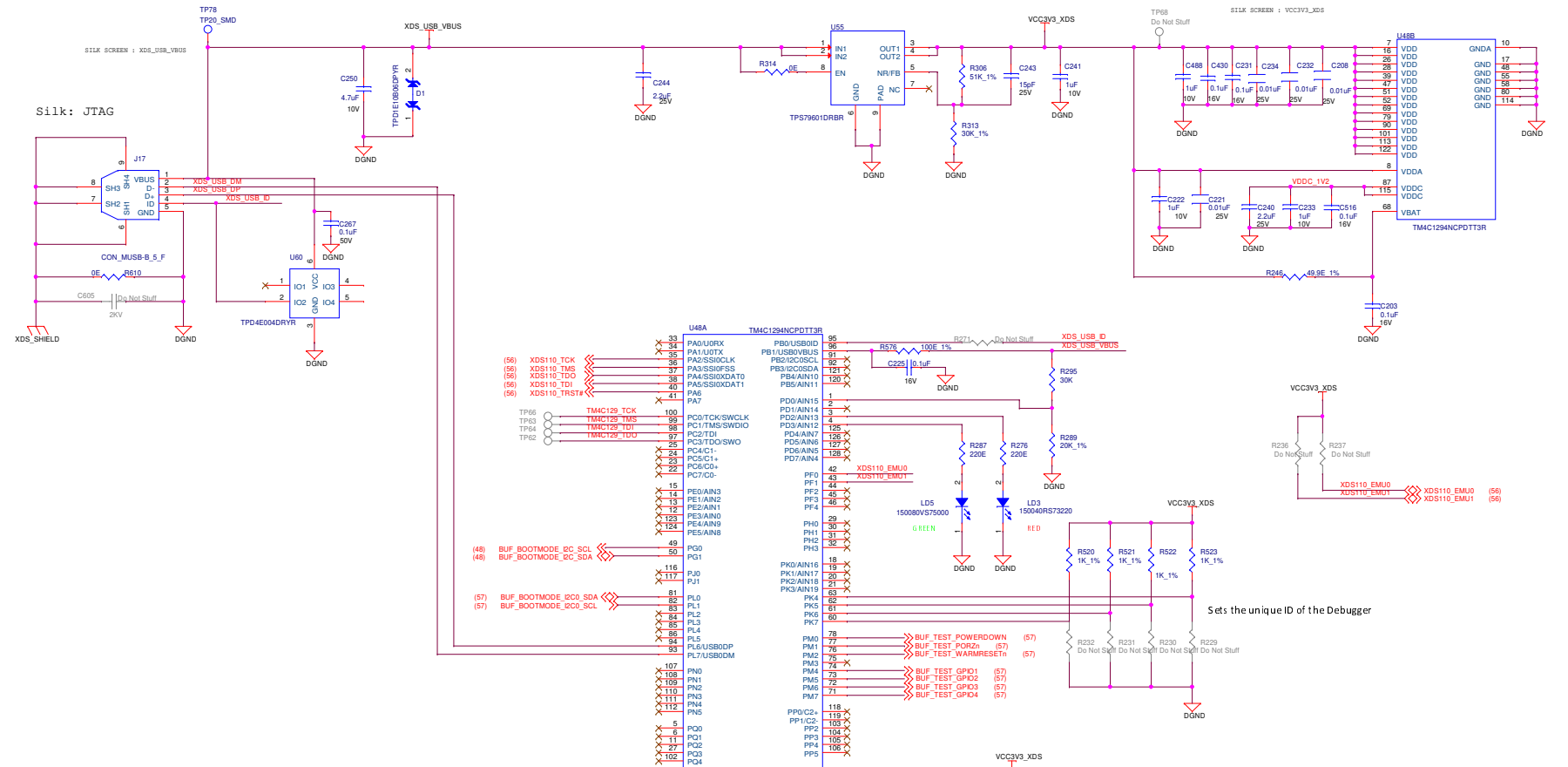
Designed for TI by Mistral Solutions Pvt Ltd



Title FT4232 UART BUFFERS

Size	Rev
C	PROC180E1
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# XDS110 DEBUGGER



## TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SOC_GPIO0_90 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

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**TEXAS INSTRUMENTS**

**MISTRAL**

**Title** XDS110 DEBUGGER

**Size** PROC180E1

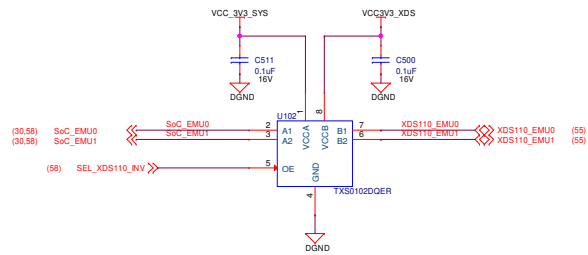
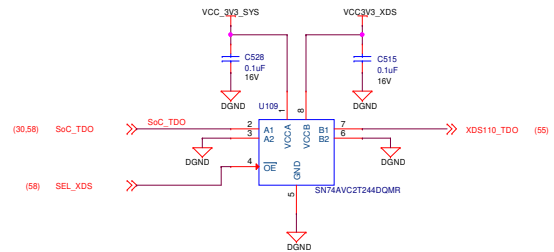
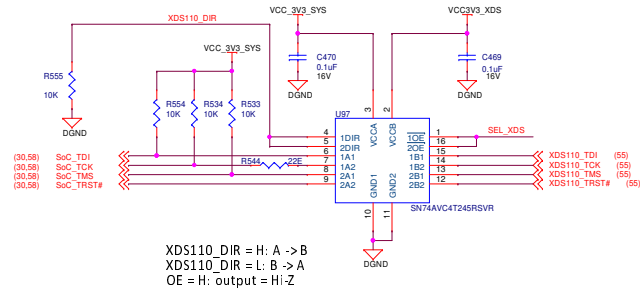
**C**

**Date:** Monday, May 13, 2024

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**Rev** E1

# XDS110 JTAG BUFFER



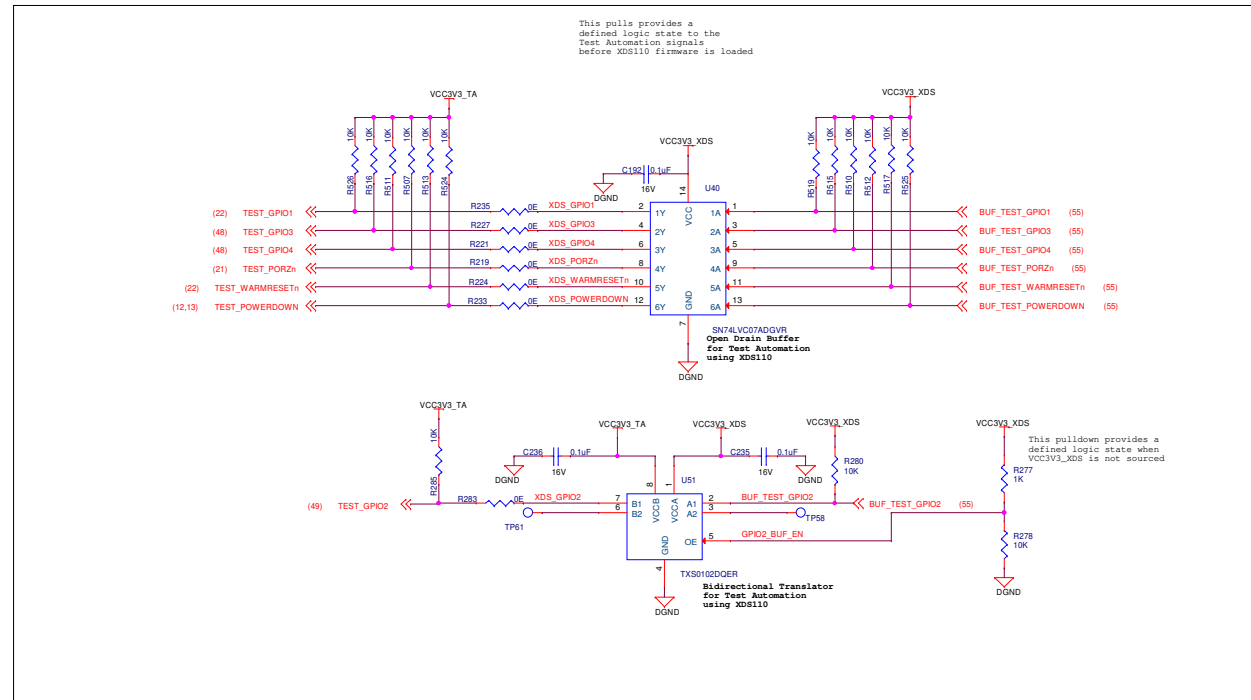
Designed for TI by Mistral Solutions Pvt Ltd



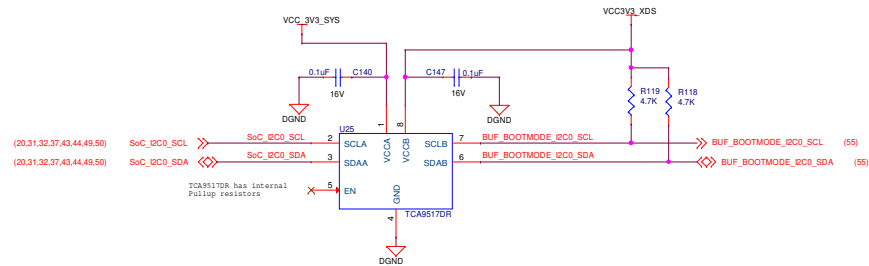
Title XDS110 JTAG BUFFER

Size	Rev
C	PROC180E1
Date:	Monday, May 13, 2024
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## XDS110 TEST AUTOMATION BUFFERS



## SOC I2C BUS BUFFER



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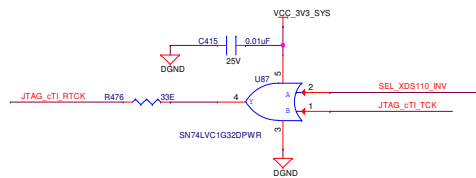
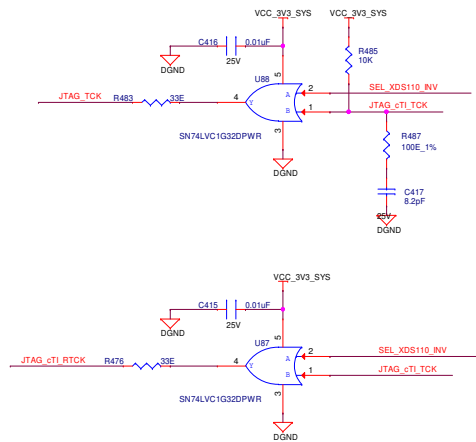
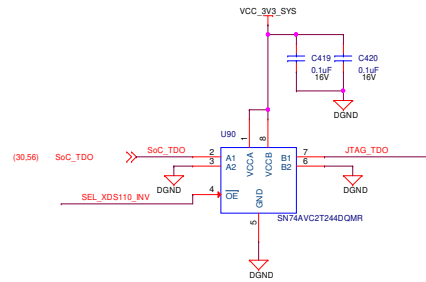
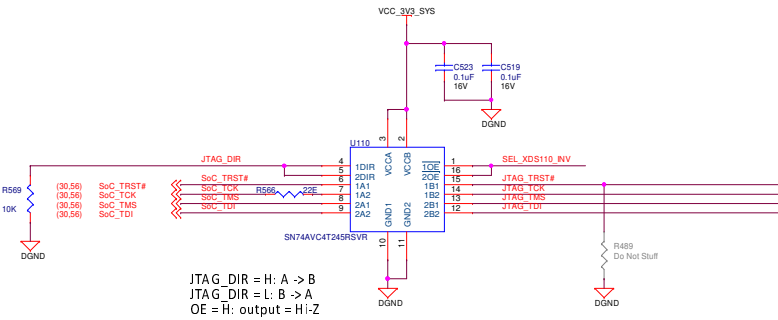


Title XDS110 TEST AUTOMATION BUFFERS

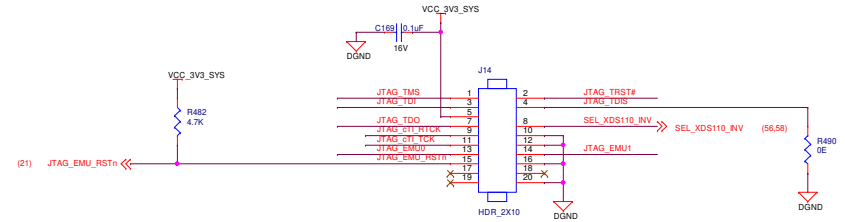
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C	PROC180E1
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## JTAG2 BUFFERS

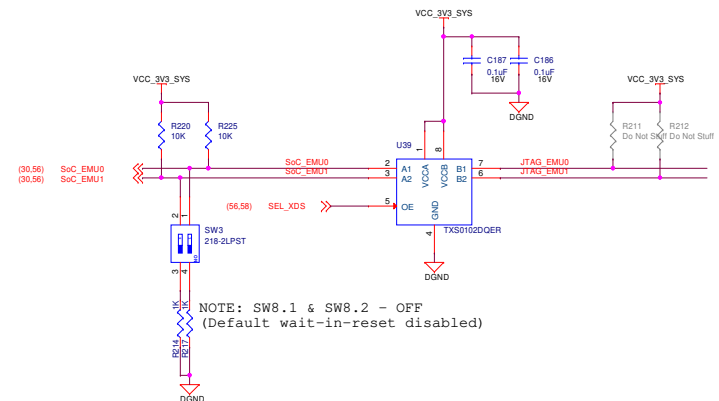
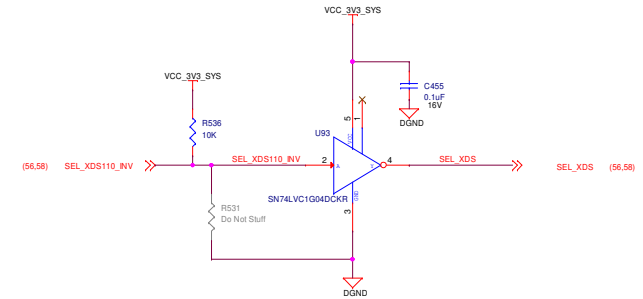


## cTI20 JTAG CONNECTOR



Silk: cTI

Add an external ESD protection to provide system level ESD protection



NOTE: SW8.1 & SW8.2 - OFF  
(Default wait-in-reset disabled)

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Title JTAG 20 PIN cTI CONNECTOR

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MOUNTING HARDWARE

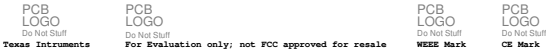
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB



LOGOs



JUMPERS



AM62A SOCKET



FIDUCIALS



LABELS

Board Serial No.



EVM Orderable No.



Assembly Revision



Orderable Part Numbers	
Variant	Label Text
001	AUDIO-AM62D-EVM

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Title MOUNTING HARDWARE

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