

AM62D EVM

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Note:
Verify the DNI components configuration with respect to the EVM schematics (Use PDF) after completion of design before board assembly

BOARD REVISION	E2
SCHEMATIC VERSION	0.1

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REVISION HISTORY

	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	0.1	14 NOV 2023	Initial Draft	Mistral Design Team		
	0.2	21 NOV 2023	Migrated to Burton PMIC and updated PDN as per AM62D EVM requirement	Mistral Design Team	Nishant	
	0.3	27 NOV 2023	Implemented Audio section as per AM62D EVM requirements	Mistral Design Team	Nishant	
	0.4	14 DEC 2023	Internally reviewed and shared with TI for review	Mistral Design Team	Nishant	Ajit MB
	0.5	27 DEC 2023	1. Implemented Audio Expansions & CPLD 2. Replaced Audio Lineout devices with TAD5212	Mistral Design Team		
	0.6	29 DEC 2023	Implemented review comments from TI	Mistral Design Team	Nishant	Ajit MB
	0.7	07 FEB 2024	Updated AEC, McASP Muxing, CPLD, Current Monitoring Sections	Mistral Design Team		
	0.8	21 FEB 2024	Updated Ethernet Expansion, FET Bus Switch & Voltage level translators	Mistral Design Team		
	0.9	03 MAR 2024	Updated Switch for fet selection and implemented TI comments	Mistral Design Team		
	0.10	22 MAR 2024	Updated Audio section, CPLD1 and CPLD2 connections removed FET switches as per TI comments.	Mistral Design Team		
	0.11	28 MAR 2024	Implemented review comments from TI	Mistral Design Team		
	0.12	04 APRIL 2024	Implemented review comments from TI	Mistral Design Team		
	0.13	17 APRIL 2024	Implemented modular approach	Mistral Design Team		
	1.0	10 MAY 2024	Baselined	Mistral Design Team		
E2	0.1	06 SEP 2024	1. ECR/ECN Implemented from E1 Revision 2. Removed RGMII1_INH and RGMII2_INH connection to "PMIC_EN" section 3. TXS0104EPWR(U32) IC replaced with TXB0104PWR 4. Implemented SYNC1_OUT resistor option as per the TI comments 5. Implemented PORT1 and PORT 2_15W_EN Status indication LED logic 6. Connected CPLD JTAG pins to GPIO expander 7. Changed 0.1uF decoupling caps on PMIC output to 0603 package 8. Changed package size for ADC input caps 9. DAC MCP47CVB02 U22 is changed to DAC53002 as per TI comments 10. Bootmode signals net names is been changed and default function of Bootmode is implemented as per the TI comments. 11. LCMX02-256HC-4SG481 (U84 & U85) IC replaced with LCMX02-640HC-4SG481	Shrinivas	Pandiya Rajan	Ajit MB
	1.0	20 SEP 2024	Baselined	Shrinivas	Pandiya Rajan	Ajit MB

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LINK TO DESIGN COLLATERALS

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am62x-am62ax-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review>

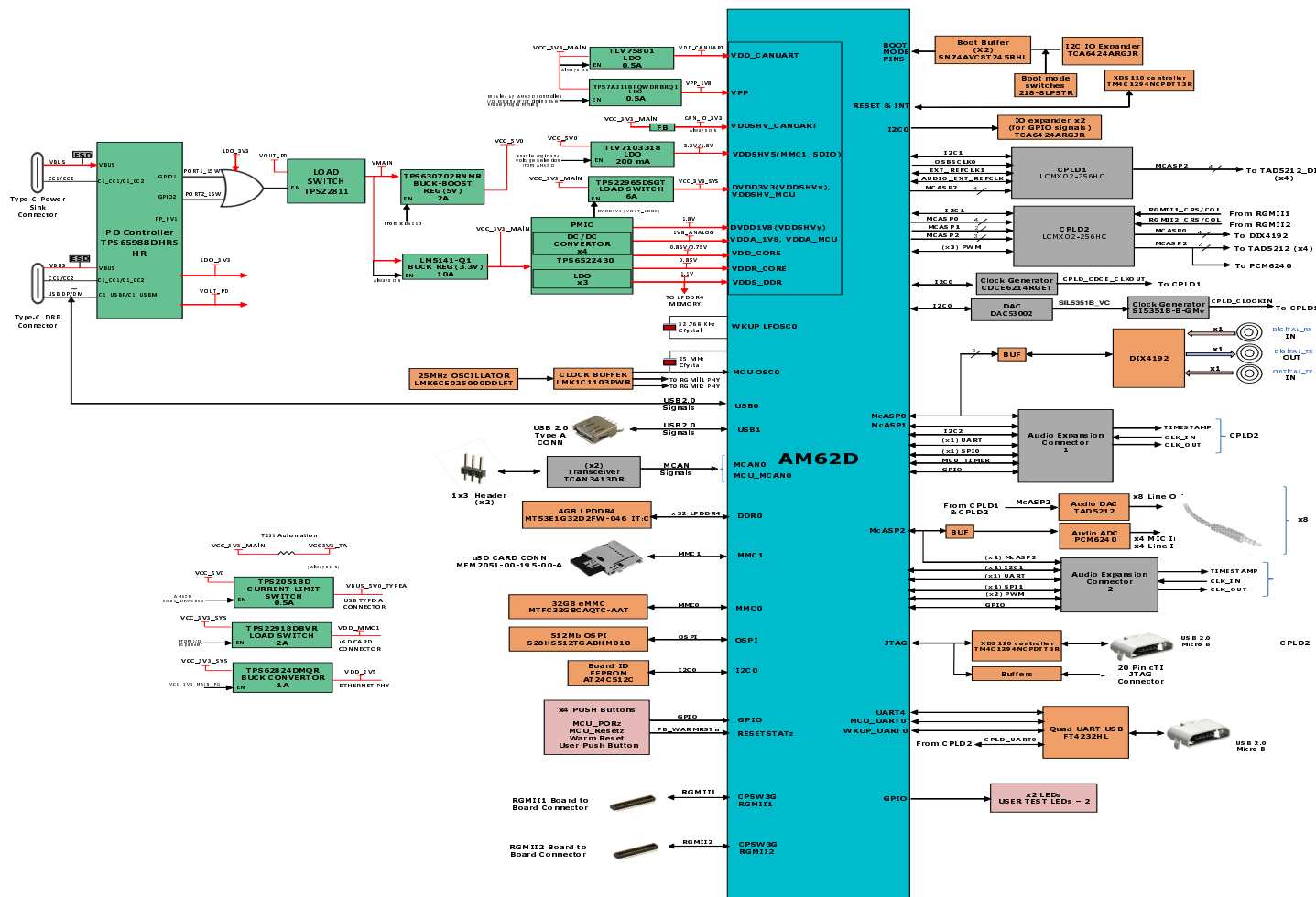
FAQs

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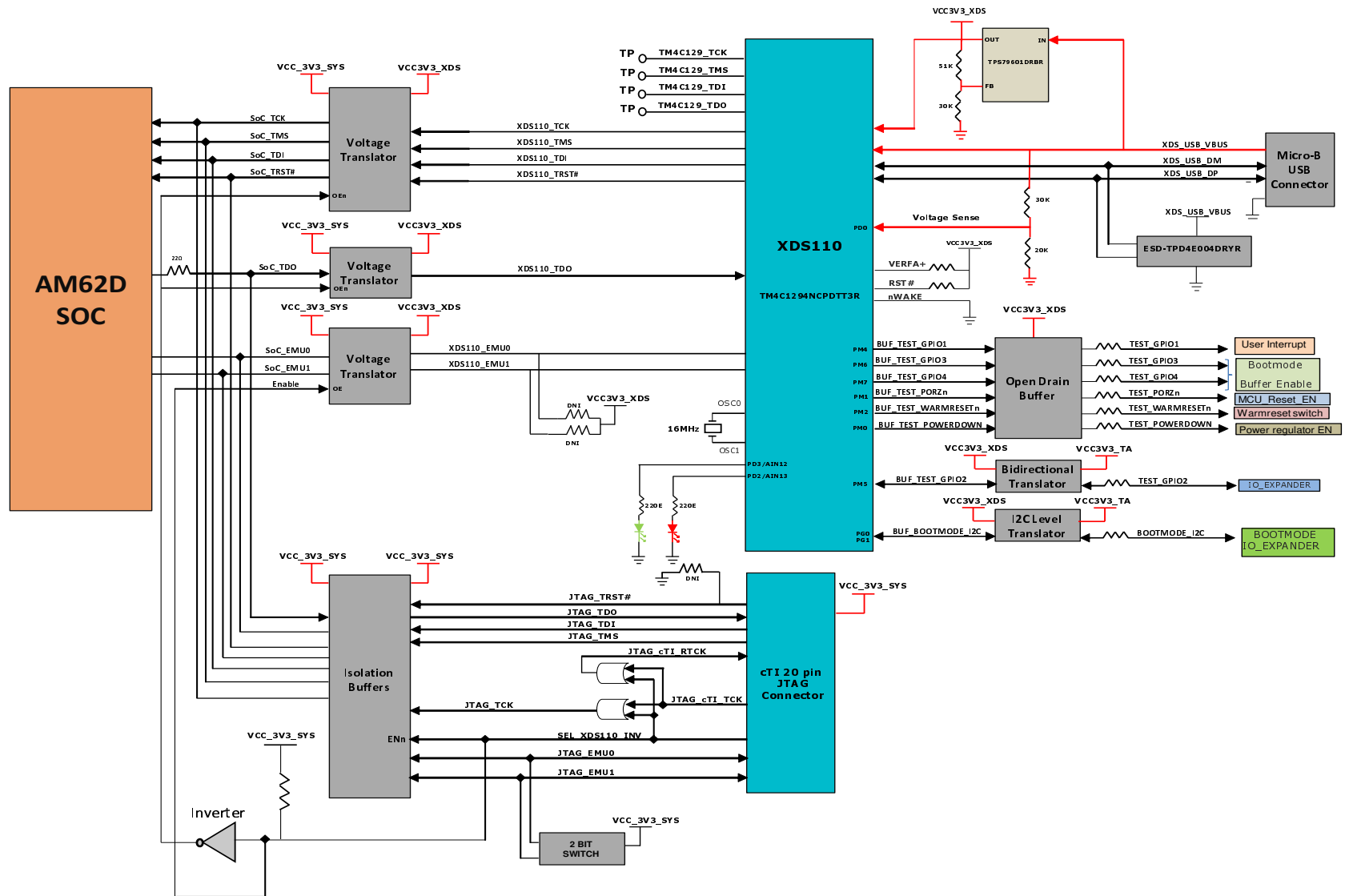


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BLOCK DIAGRAM AM62D EVM



BLOCK DIAGRAM_XDS110



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POWER ARCHITECTURE BLOCK DIAGRAM

POWER ARCHITECTURE BLOCK DIAGRAM

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TEXAS INSTRUMENTS

MISTRAL

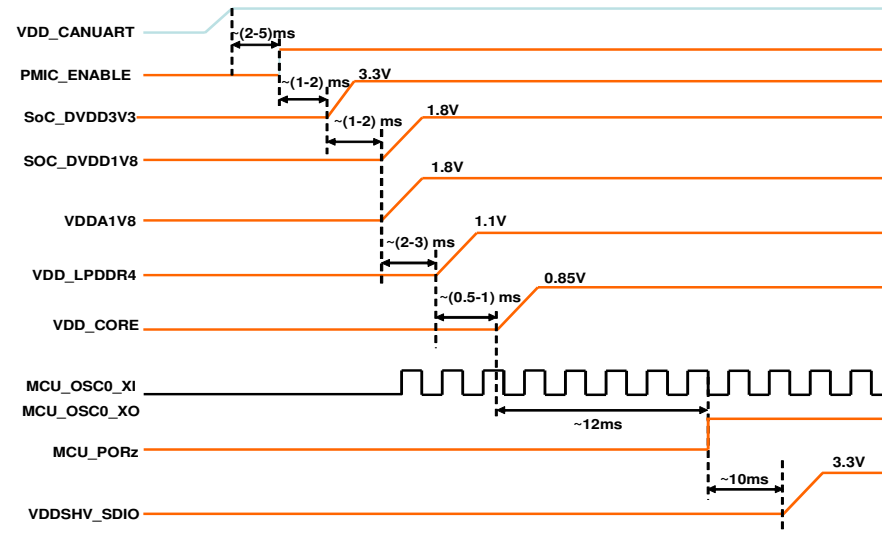
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Size: PROC180E2

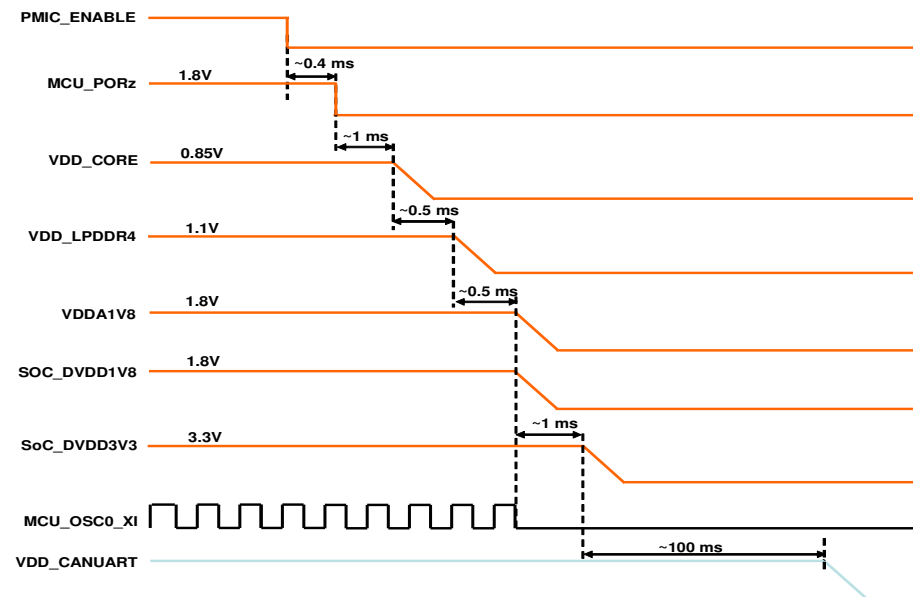
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POWER UP SEQUENCE



POWER DOWN SEQUENCE



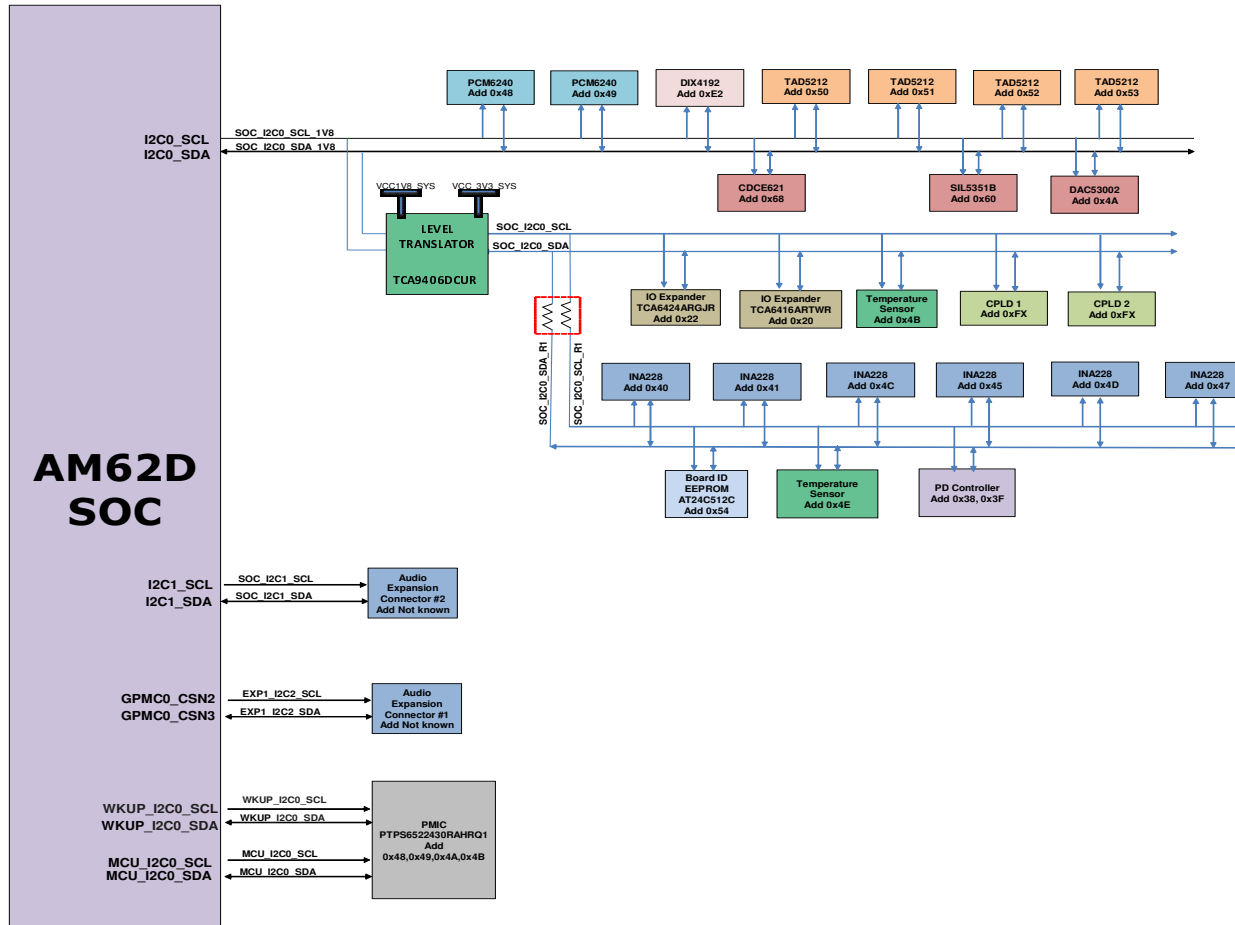
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I2C TREE



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GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE RAIL CONNECTED ON SEVEN
1	Audio Exp Inter Connector 1	EX1_I2_GPIO_1	GPIO	GPIO_1	GM0_M0_L00	NA	NA	NA	VB01HV1	WCT_VDD3.3V6
2	OSR Inter Exp	OSR_I2_GPIO14	RESET	GPIO_14	OSR0_L0_N1	EN/F0T	HS0 H	LS0 W	VB01HV1	WCT_VDD3.3V6
3	Audio Exp Inter Connector 1	EX1_I2_GPIO_3	GPIO	GPIO_3	OSR0_L0_N2	NA	NA	NA	VB01HV1	WCT_VDD3.3V6
4	Audio Exp Inter Connector 1	EX1_I2_GPIO_4	GPIO	GPIO_4	OSR0_L0_N3	NA	NA	NA	VB01HV1	WCT_VDD3.3V6
5	Audio Exp Inter Connector 1	EX1_I2_GPIO_11	GPIO	GPIO_11	GM00_L0_K	NA	NA	NA	VB01HV1	WCT_VDD3.3V6
6	Audio Exp Inter Connector 1	EX1_I2_GPIO_2	GPIO	GPIO_2	GM00_L0_V01	NA	NA	NA	VB01HV1	WCT_VDD3.3V6
7	Micro Exp Header	14C_I2_GPIO_20	GPIO	GPIO_20	GM00_L0_H0N	NA	NA	NA	VB01HV3	WCT_VDD3.3V6
8	Audio Exp Inter Connector 1	14C_I2_GPIO_30	GPIO	GPIO_30	GM00_L0_H0N	NA	NA	NA	VB01HV3	WCT_VDD3.3V6
9	Micro Exp Header	14C_I2_GPIO_36	GPIO	GPIO_36	GM00_L0_H0N	NA	NA	NA	VB01HV3	WCT_VDD3.3V6
10	Audio Exp Inter Connector 1	EX1_I2_GPIO_5	GPIO	GPIO_5	GM00_L0_K011	NA	NA	NA	VB01HV3	WCT_VDD3.3V6
11	Audio Exp Inter Connector 1	EX1_I2_GPIO_7	GPIO	GPIO_7	GM00_L0_W010	NA	NA	NA	VB01HV3	WCT_VDD3.3V6
12	Audio Exp Inter Connector 1	EX1_I2_GPIO_5	GPIO	GPIO_5	VO00_L0_A0A0	NA	NA	NA	VB01HV3	WCT_VDD3.3V6
13	Audio Exp Inter Connector 1	EX1_I2_GPIO_6	GPIO	GPIO_6	VO00_L0_A0A1	NA	NA	NA	VB01HV3	WCT_VDD3.3V6
14	Audio Exp Inter Connector 1	EX1_I2_GPIO_6	GPIO	GPIO_6	VO00_L0_A0A1	NA	NA	NA	VB01HV3	WCT_VDD3.3V6
15	Audio Exp Inter Connector 1	EX1_I2_GPIO_7	GPIO	GPIO_7	VO00_L0_A0A2	NA	NA	NA	VB01HV3	WCT_VDD3.3V6
16	Audio Exp Inter Connector 1	EX1_I2_GPIO_8	GPIO	GPIO_8	VO00_L0_A0A2	NA	NA	NA	VB01HV3	WCT_VDD3.3V6
17	Audio Exp Inter Connector 1	EX1_I2_GPIO_9	GPIO	GPIO_9	VO00_L0_A0A3	NA	NA	NA	VB01HV3	WCT_VDD3.3V6
18	Audio Exp Inter Connector 1	EX1_I2_GPIO_9	GPIO	GPIO_9	VO00_L0_A0A3	NA	NA	NA	VB01HV3	WCT_VDD3.3V6
19	Audio Exp Inter Connector 1	EX1_I2_GPIO_7	GPIO	GPIO_7	VO00_L0_A0A2	NA	NA	NA	VB01HV3	WCT_VDD3.3V6
20	Audio Exp Inter Connector 1	EX1_I2_GPIO_8	GPIO	GPIO_8	VO00_L0_A0A3	NA	NA	NA	VB01HV3	WCT_VDD3.3V6
21	On-chip I/O control signal	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
22	I/O 0 I/O Voltage indicator	WCT_M0_L0_00	ENABLE	GPIO_00	VO00_L0_A0A0	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
23	On-chip I/O control signal	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
24	On-chip I/O control signal	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
25	On-chip I/O control signal	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
IO EXPANDER - 01										
1	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
2	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
3	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
4	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
5	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
6	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
7	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
8	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
9	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
10	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
11	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
12	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
13	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
14	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
15	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
16	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
17	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
18	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
19	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
20	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
21	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
22	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
23	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
24	GPIO_01_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
IO EXPANDER - 02										
1	GPIO_02_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
2	GPIO_02_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
3	GPIO_02_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
4	GPIO_02_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
5	GPIO_02_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
6	GPIO_02_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
7	GPIO_02_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
8	GPIO_02_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
9	GPIO_02_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
10	GPIO_02_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
11	GPIO_02_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
12	GPIO_02_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6
13	GPIO_02_GPIO_01	WCT_M0_L0_00	ENABLE	GPIO_00	MM00_L0_W01	EN/F0T	HS0 H	LS0 W	VB01HV3	WCT_VDD3.3V6

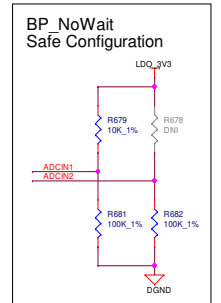
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Title GPIO MAPPING TABLE

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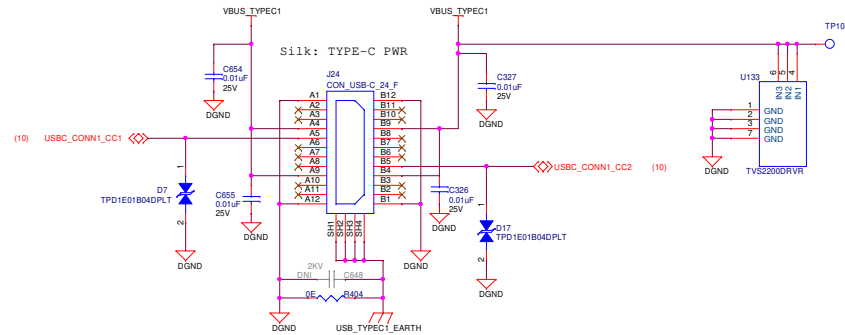
TYPE-C DUAL PD CONTROLLER



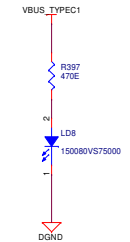
I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

[illegible]

USB TYPE-C POWER CONNECTOR

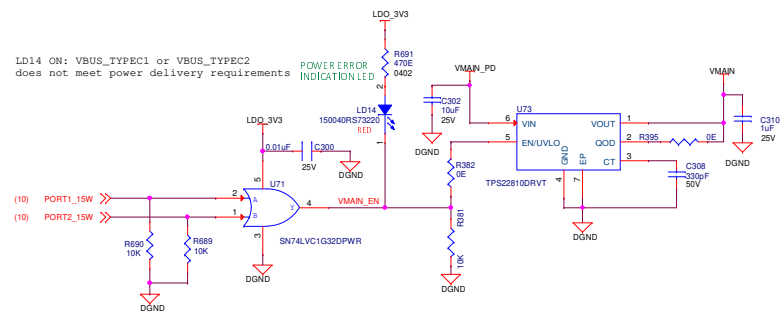


POWER INDICATION LED: VBUS_TYPE1



LOAD SWITCH FOR VMAIN

LD14 ON: VBUS_TYPE1 or VBUS_TYPE2
does not meet power delivery requirements



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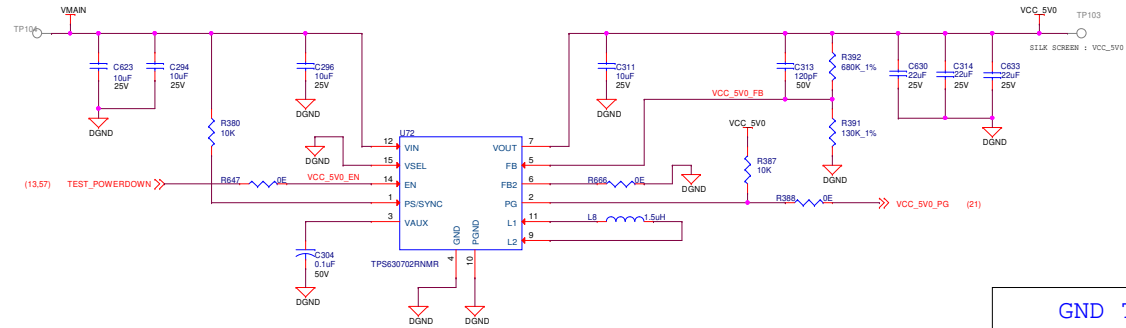
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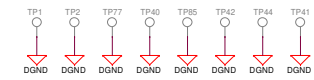
PERIPHERAL POWER SUPPLY - 1

5V, 2.0 AMPS SUPPLY

VinMin = 4.5V
VinMax = 15V
Vout = 5V @ 2A



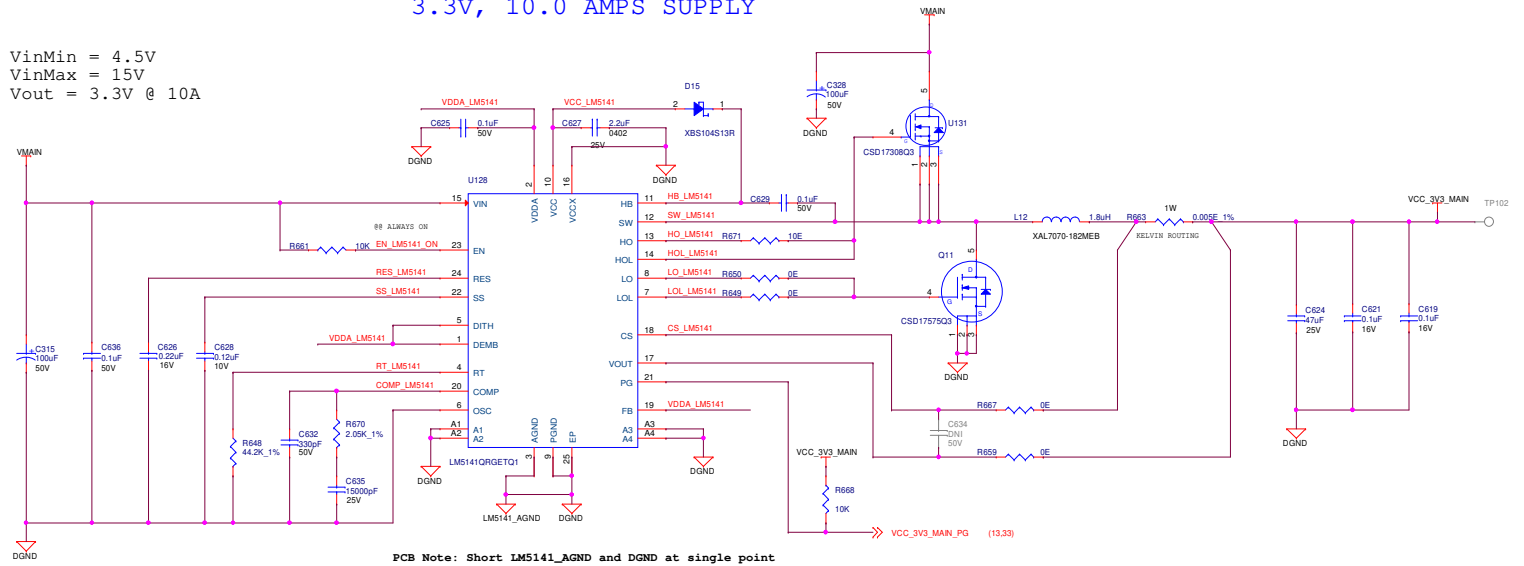
GND TEST POINTS



PERIPHERAL POWER SUPPLY - 2

3.3V, 10.0 AMPS SUPPLY

VinMin = 4.5V
VinMax = 15V
Vout = 3.3V @ 10A



PCB Note: Short LM5141_AGND and DGND at single point

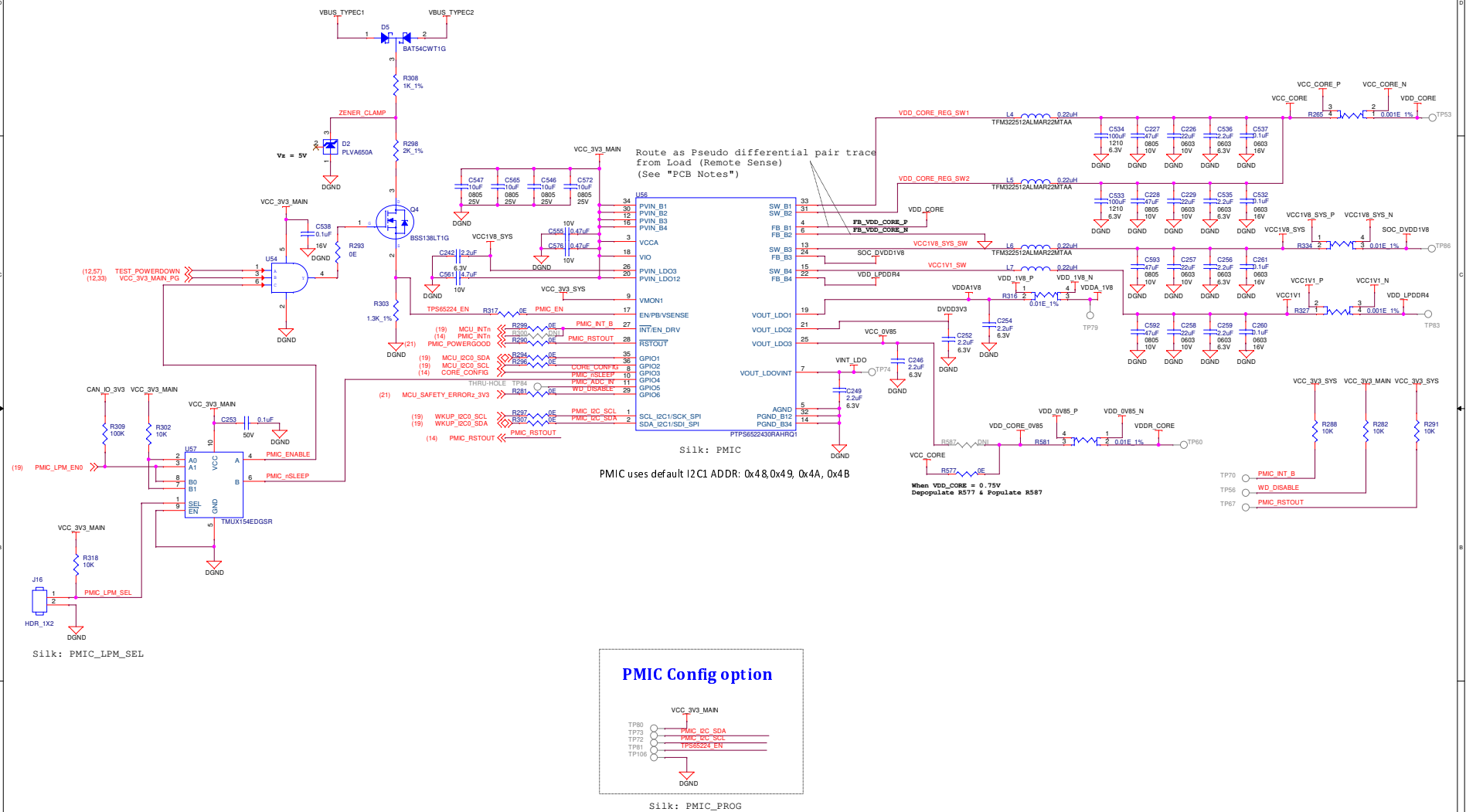
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SOC POWER SUPPLY PMIC - 1



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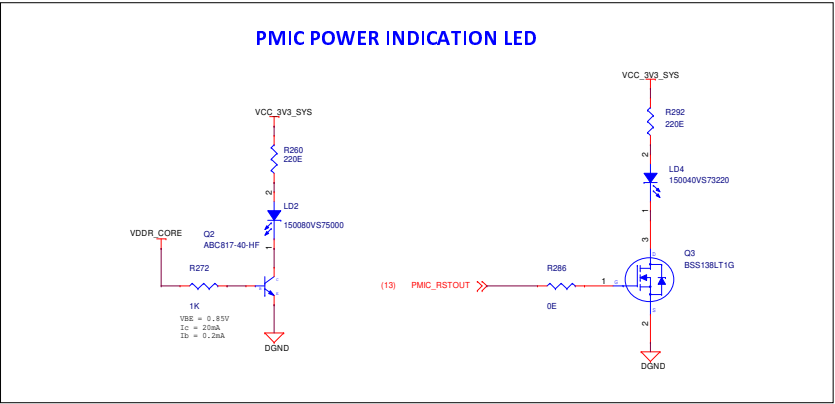


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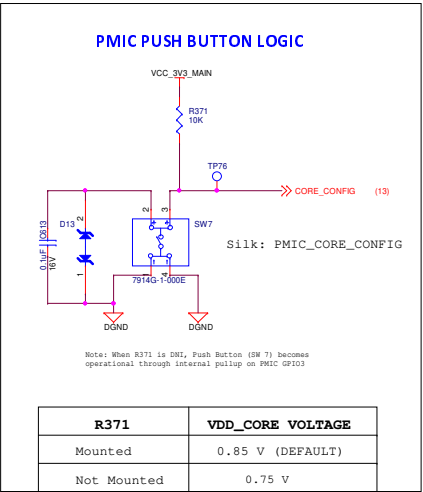
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SOC POWER SUPPLY PMIC - 2

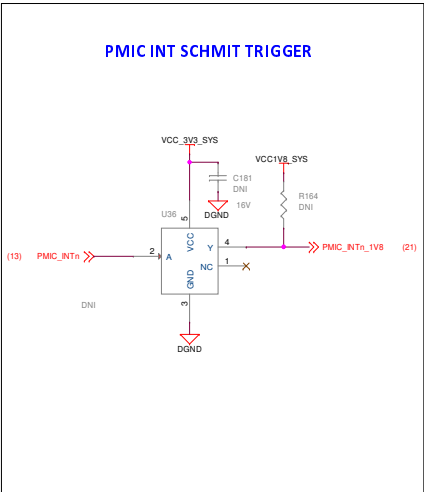
PMIC POWER INDICATION LED



PMIC PUSH BUTTON LOGIC



PMIC INT SCHMIT TRIGGER



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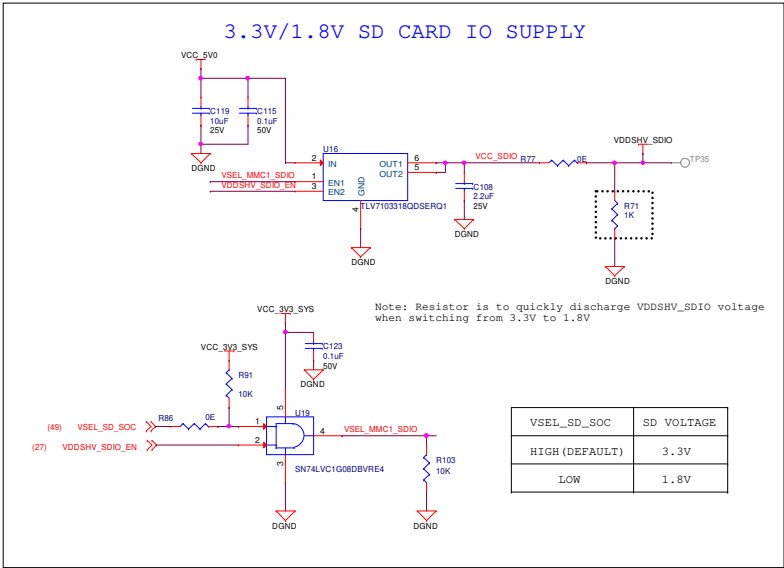
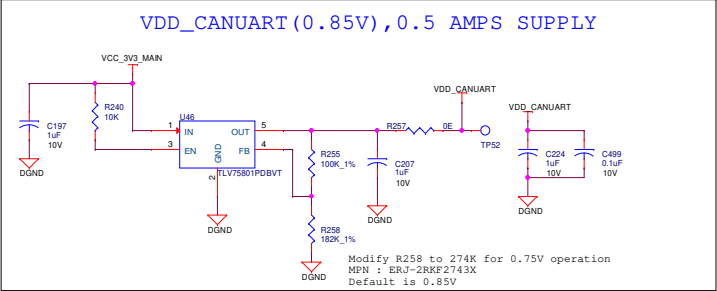
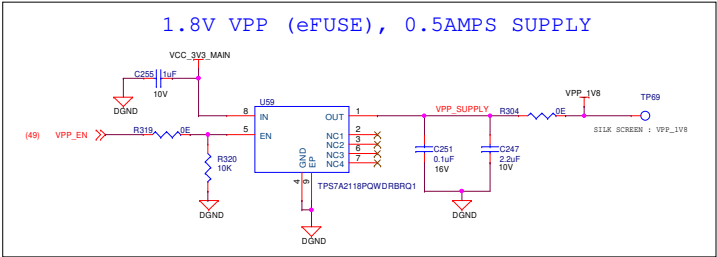


Title SOC POWER SUPPLY PMIC - 2

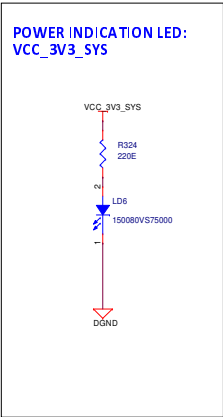
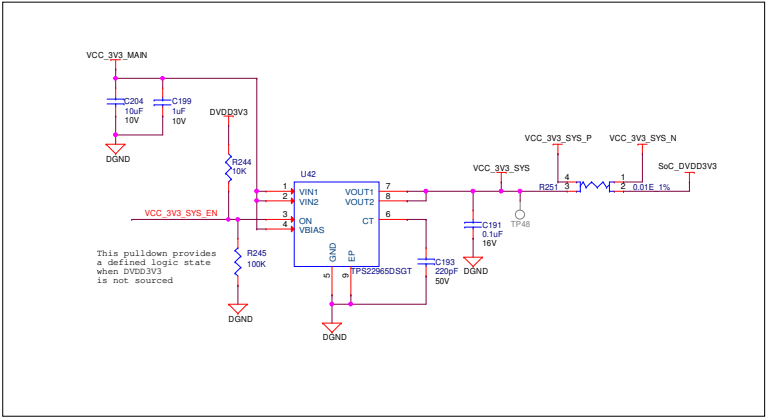
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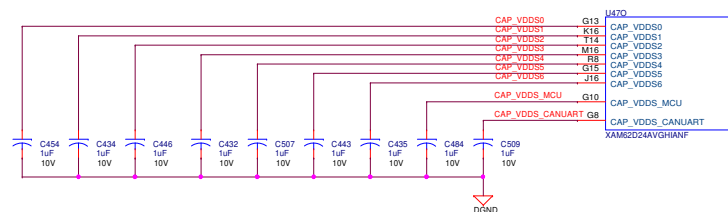
SOC POWER SUPPLIES - LDOs



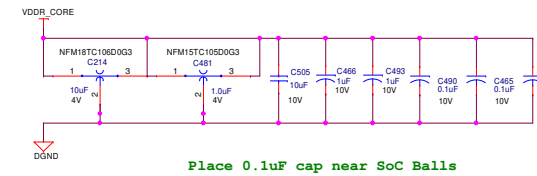
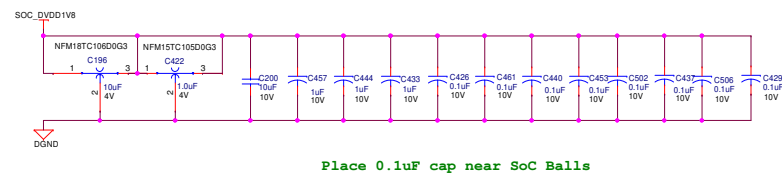
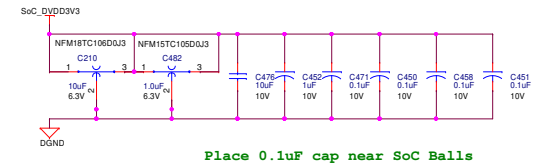
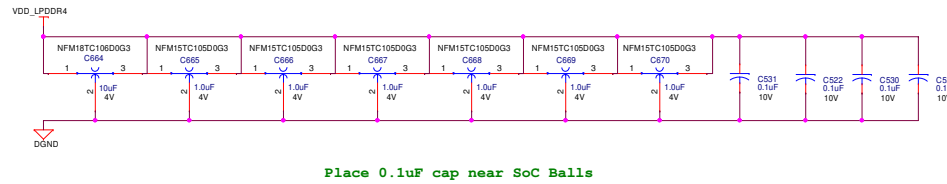
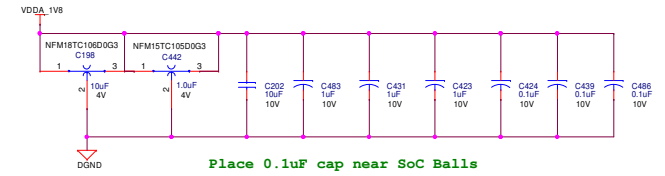
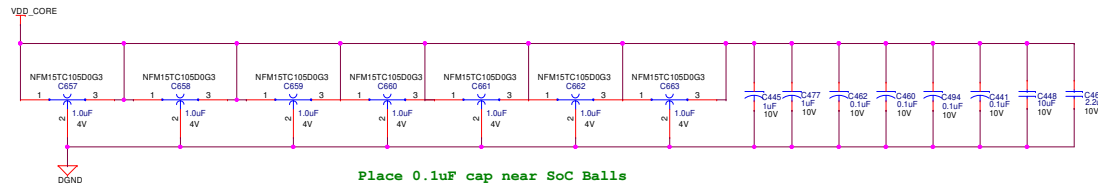
VCC_3V3_SYS LOAD SWITCH



U470			
A1	VSS	Y9	VSS
A10	VSS	Y5	VSS
A19	VSS	Y3	VSS
A15	VSS	Y16	VSS
A18	VSS	Y12	VSS
A22	VSS	W8	VSS
A4	VSS	W6	VSS
A0	VSS	W4	VSS
AX11	VSS	W2	VSS
AX14	VSS	W1	VSS
AA2	VSS	W14	VSS
AA4	VSS	W11	VSS
AA1	VSS	V9	VSS
AB1	VSS	V7	VSS
AB2	VSS	V5	VSS
AB5	VSS	V3	VSS
AB18	VSS	V1	VSS
AB22	VSS	V20	VSS
AB3	VSS	U9	VSS
AB5	VSS	U1	VSS
AB9	VSS	U4	VSS
AB5	VSS	U2	VSS
B5	VSS	U16	VSS
B7	VSS	U14	VSS
C4	VSS	U12	VSS
D11	VSS	T4	VSS
D00	VSS	T5	VSS
D2	VSS	T3	VSS
D4	VSS	T17	VSS
E1	VSS	T16	VSS
E3	VSS	T1	VSS
E5	VSS	R6	VSS
F11	VSS	R4	VSS
F13	VSS	R2	VSS
F19	VSS	R16	VSS
F2	VSS	R14	VSS
F4	VSS	R12	VSS
G12	VSS	R10	VSS
G17	VSS	P7	VSS
G3	VSS	P20	VSS
G5	VSS	P17	VSS
G9	VSS	P15	VSS
H1	VSS	P13	VSS
H11	VSS	N15	VSS
H14	VSS	N8	VSS
H20	VSS	N16	VSS
H4	VSS	N14	VSS
J12	VSS	N12	VSS
J17	VSS	N10	VSS
J9	VSS	N1	VSS
K7	VSS	M7	VSS
K11	VSS	M4	VSS
K4	VSS	M17	VSS
K7	VSS	M11	VSS
K9	VSS	L3	VSS
L10	VSS	L20	VSS
L14	VSS		
AMR022MAVGHIANF			

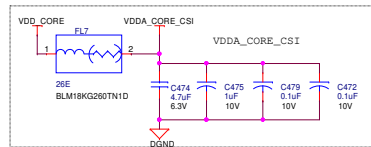
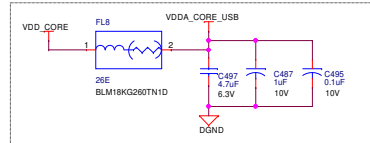


SOC POWER SUPPLIES - DECAPS 1

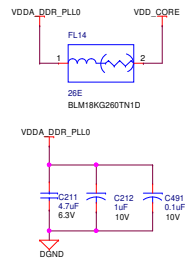


SOC POWER SUPPLIES - DECAPS 2

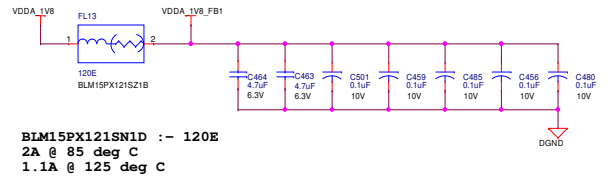
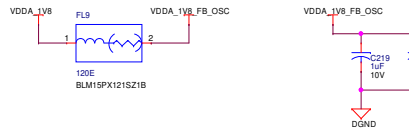
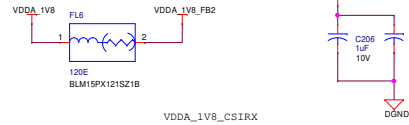
Peripherals - Core SUPPLY



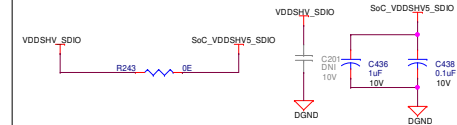
VDDA_DDR_PLL0



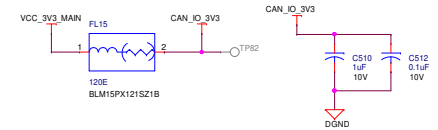
Peripherals - 1.8V Analog SUPPLY



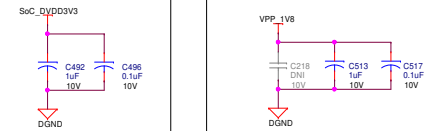
3.3V/1.8V MMC1 SUPPLY



Always ON supply



VPP_1V8



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Title SOC POWER SUPPLIES - DECAPS 2

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SOC WKUP DOMAIN

SOC - MCU DOMAIN

The diagram illustrates the SOC - MCU DOMAIN, showing the connection between the MCU and various peripheral blocks. The MCU is represented by a blue box on the left, and the peripheral blocks are represented by red boxes on the right. The connections are color-coded: blue for MCU signals, red for peripheral signals, and green for power and ground. The MCU signals include MCU_I2C0_SCL, MCU_I2C0_SDA, MCU_SPI0_CLK, MCU_SPI0_D0, MCU_SPI0_D1, MCU_SPI0_CS0, MCU_SPI0_CS1, MCU_TIMER_01, MCU_OSC0_XI, MCU_OSC0_X0, MCU_MCAN0_RX, MCU_MCAN0_TX, MCU_UART0_RTSN, MCU_UART0_CTSN, MCU_MCAN1_RX, MCU_MCAN1_TX, MCU_UART0_RXD, MCU_UART0_TXD, and GPIO_Mcu_Soc_InNtn. The peripheral blocks include MCU_I2C0_SCL, MCU_I2C0_SDA, MCU_SPI0_CLK, MCU_SPI0_D0, MCU_SPI0_D1, MCU_SPI0_CS0, MCU_SPI0_CS1, MCU_TIMER_01, MCU_OSC0_XI, MCU_OSC0_X0, MCU_MCAN0_RX, MCU_MCAN0_TX, MCU_UART0_RTSN, MCU_UART0_CTSN, MCU_MCAN1_RX, MCU_MCAN1_TX, MCU_UART0_RXD, MCU_UART0_TXD, and GPIO_Mcu_Soc_InNtn. The connections are labeled with pin numbers and component values.

MCU Signals (Left):

- MCU_I2C0_SCL (D9)
- MCU_I2C0_SDA (B13)
- MCU_SPI0_CLK (A15)
- MCU_SPI0_D0 (B12)
- MCU_SPI0_D1 (A15)
- MCU_SPI0_CS0 (C11)
- MCU_SPI0_CS1 (A12)
- MCU_TIMER_01 (A11)
- MCU_OSC0_XI (E8)
- MCU_OSC0_X0 (D7)
- MCU_MCAN0_RX (B11)
- MCU_MCAN0_TX (D10)
- MCU_UART0_RTSN (B9)
- MCU_MCAN1_RX (D7)
- MCU_MCAN1_TX (D8)
- MCU_UART0_RXD (F8)
- MCU_UART0_TXD (F8)
- GPIO_Mcu_Soc_InNtn (XAMR20244VGH1NF)
- MCU_UART0_RX_V3 (S4)
- MCU_UART0_TX_V3 (S4)

Peripheral Signals (Right):

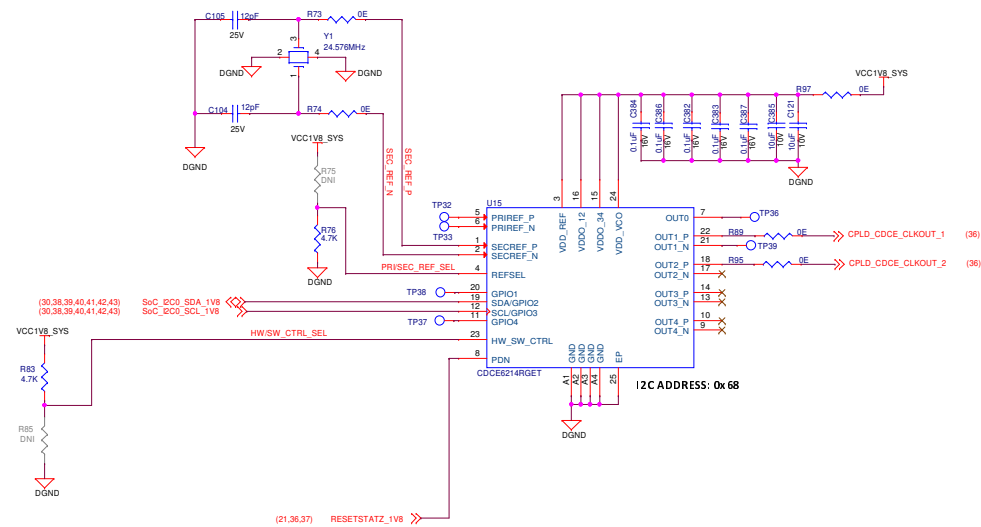
- MCU_I2C0_SCL (19)
- MCU_I2C0_SDA (19)
- MCU_SPI0_CLK (45)
- MCU_SPI0_D0 (45)
- MCU_SPI0_D1 (45)
- MCU_SPI0_CS0 (45)
- MCU_SPI0_CS1 (45)
- MCU_TIMER_01 (45)
- MCU_OSC0_XI (45)
- MCU_OSC0_X0 (45)
- MCU_MCAN0_RX (47)
- MCU_MCAN0_TX (47)
- MCU_UART0_RTSN (46)
- MCU_MCAN1_RX (46)
- MCU_MCAN1_TX (46)
- MCU_UART0_RXD (45)
- MCU_UART0_TXD (45)
- GPIO_Mcu_Soc_InNtn (22)
- MCU_UART0_RX_V3 (54)
- MCU_UART0_TX_V3 (54)

Power and Ground Connections:

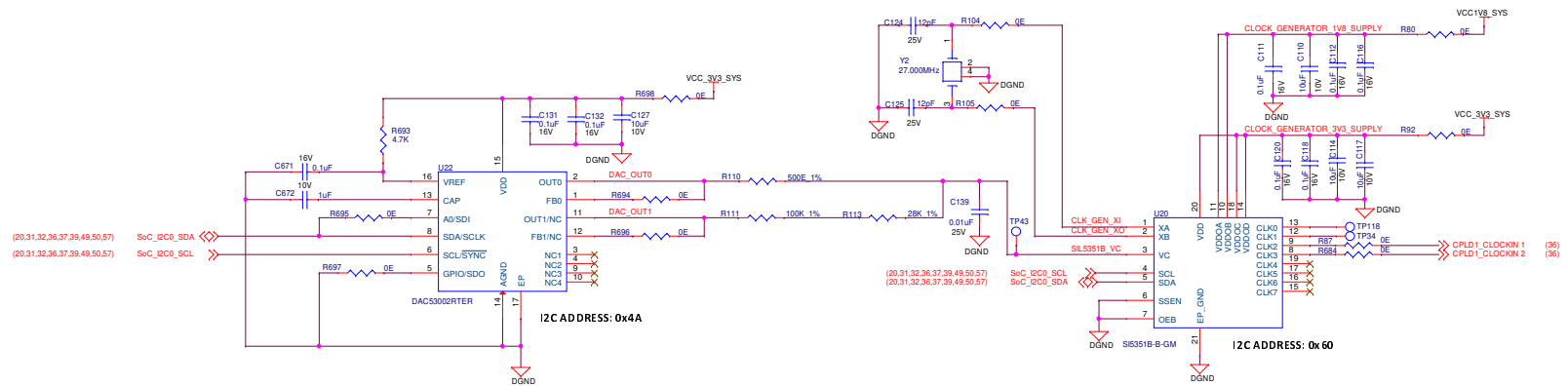
- MCU_I2C0_SCL (19)
- MCU_I2C0_SDA (19)
- MCU_SPI0_CLK (45)
- MCU_SPI0_D0 (45)
- MCU_SPI0_D1 (45)
- MCU_SPI0_CS0 (45)
- MCU_SPI0_CS1 (45)
- MCU_TIMER_01 (45)
- MCU_OSC0_XI (45)
- MCU_OSC0_X0 (45)
- MCU_MCAN0_RX (47)
- MCU_MCAN0_TX (47)
- MCU_UART0_RTSN (46)
- MCU_MCAN1_RX (46)
- MCU_MCAN1_TX (46)
- MCU_UART0_RXD (45)
- MCU_UART0_TXD (45)
- GPIO_Mcu_Soc_InNtn (22)
- MCU_UART0_RX_V3 (54)
- MCU_UART0_TX_V3 (54)

The schematic diagram illustrates the clock distribution network. It features two clock buffers, U62 and U65, connected to a 25.000MHz LMK6CE025000DULF clock source. U62 is connected to VCC1V8_CLKBUF and has an output EXT_CLKOUT0 connected to U65. U65 is connected to VCC1V8_CLKBUF and has an output CLKOUT0 connected to U65. The diagram also shows a 120Ω termination resistor (FL10) connected to VDDA1V8. Various resistors (R329, R337, R336, R348, R349, R350, R358) and capacitors (C265, C284, C285, C290) are shown, along with a 120Ω termination resistor (FL10). The diagram is labeled with component values and connections.

CPLD CLOCK GENERATION



HW/SW_CTRL_SEL / PR1/SEC_REF_SEL	PAGE_SELECT	CLOCK_SOURCE
LOW	PAGE 0	SEC_REF
HIGH	PAGE 1	PR1_REF



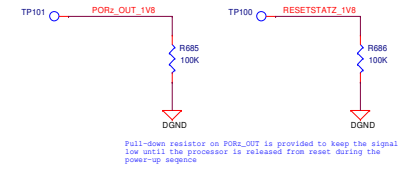
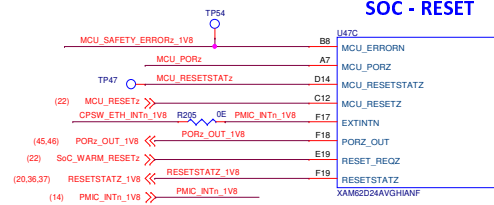
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Title CPLD CLOCK GENERATION

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SOC - RESET



SOC POWER ON RESET

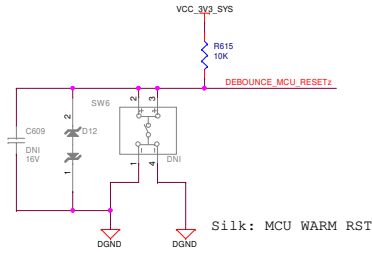
The diagram illustrates the SOC Power On Reset (POR) circuit. It features a Schmitt trigger inverter (SN74VHC1G11DRYR) configured as a voltage divider. The input of the inverter is connected to a network of resistors and capacitors that monitor the VCC_3V3 supply. The output of the inverter is connected to the PORz pin of the SoC. The input of the inverter is also connected to a 0.1uF capacitor to GND. The input of the inverter is also connected to a 10k resistor to VCC_3V3 and a 15k resistor to GND. The input of the inverter is also connected to a 10k resistor to VCC_3V3 and a 15k resistor to GND. The input of the inverter is also connected to a 10k resistor to VCC_3V3 and a 15k resistor to GND.

MCU POWER ON RESET

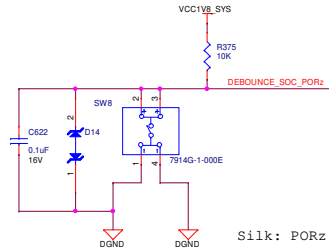
The diagram illustrates the MCU Power On Reset circuit. It shows a 5V regulator (U43) connected to VCC1V8_SYS. A 0.1uF capacitor (C421) is connected between VCC1V8_SYS and GND. The reset pin (pin 4) of the MCU (SH74LVC1G11DRYR) is connected to the output of the 5V regulator through a resistor (R242, 1k). The reset pin is also connected to GND through a resistor (R238, 4.7k). The reset pin is labeled 'MCU_PORz' and 'TP49'. The reset pin is also connected to the output of the 5V regulator through a resistor (R242, 1k). The reset pin is also connected to GND through a resistor (R238, 4.7k). The reset pin is labeled 'MCU_PORz' and 'TP49'.

SOC RESET - 2

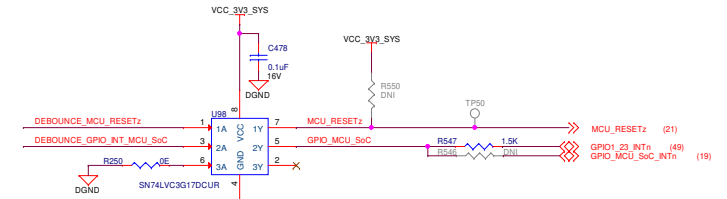
MCU WARM RESET



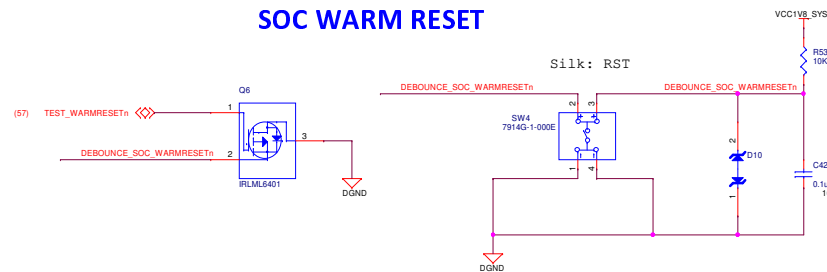
SOC PORz



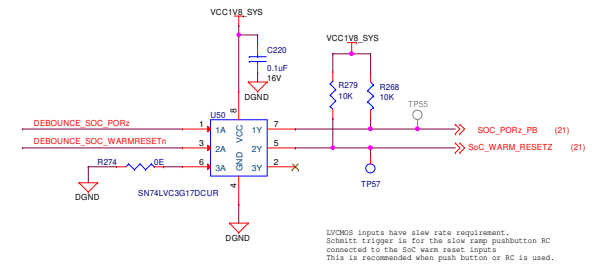
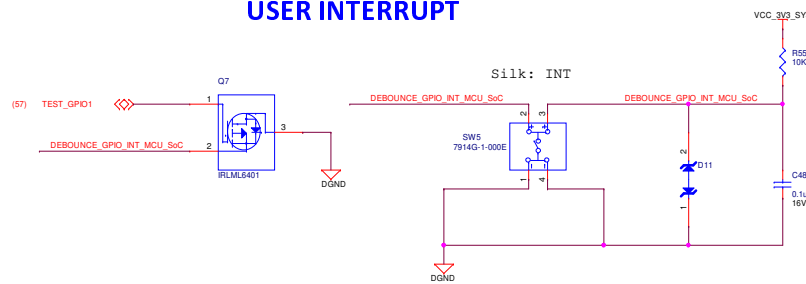
RESET & INT DEBOUNCE CIRCUIT



SOC WARM RESET



USER INTERRUPT



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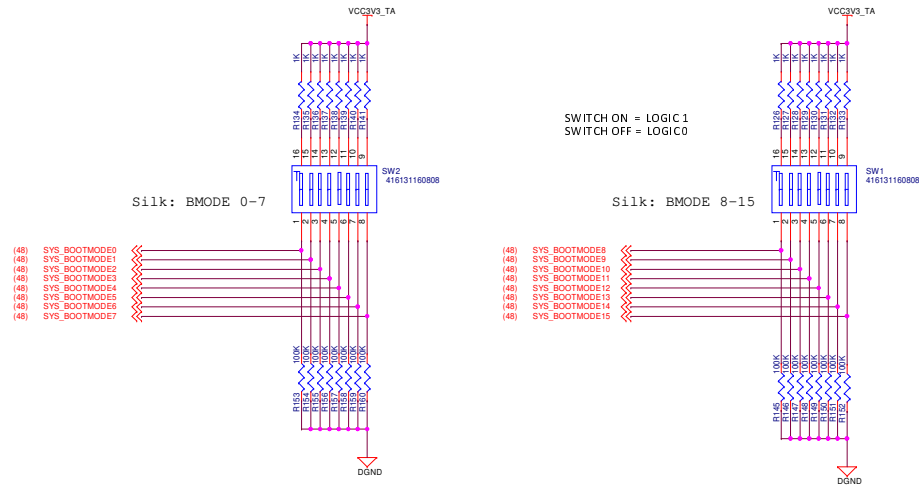


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BOOT MODE SWITCHES

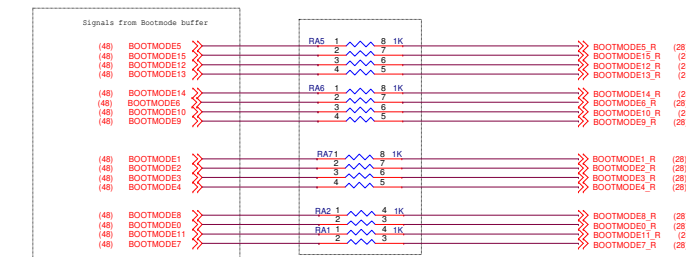
D-Note: VCC3V3_TA supply is used for test automation.
Connect SOC_RESET3V3 in the custom board design when buffers are not used



BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. USB0 MS

BOOTMODE PINS



- D-NOTE:
1. 1K Resistor at the output of the buffer is recommended when the bootmode pins are used for alternate functions
 2. Replace 1K Resistor at the output of the buffer with resistor of value 0E when bootmode buffers are not used

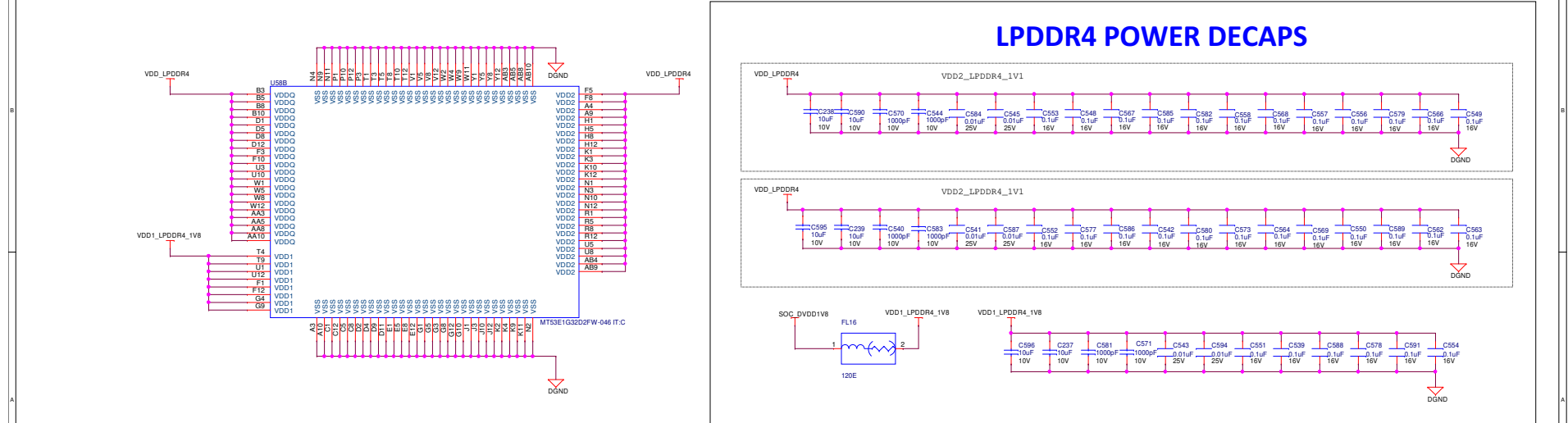
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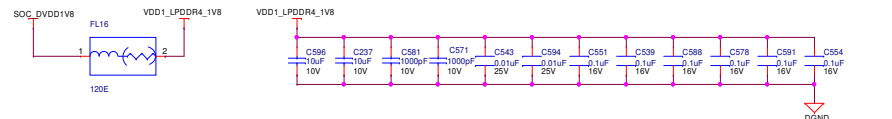
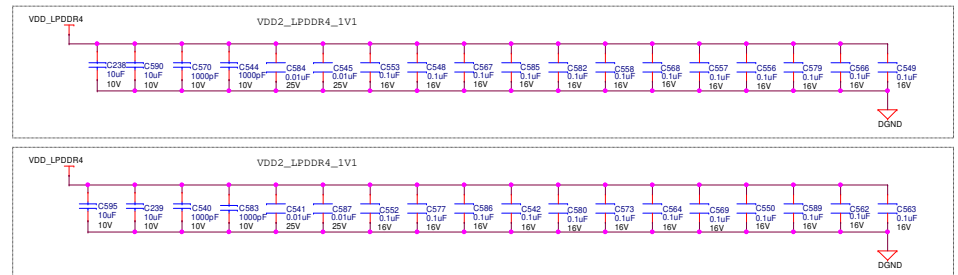
Title BOOT MODE SWITCHES

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SOC LPDDR4 INTERFACE

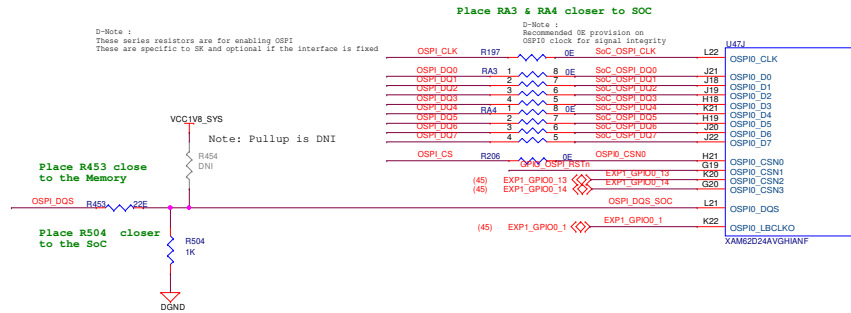


LPDDR4 POWER DECAPS

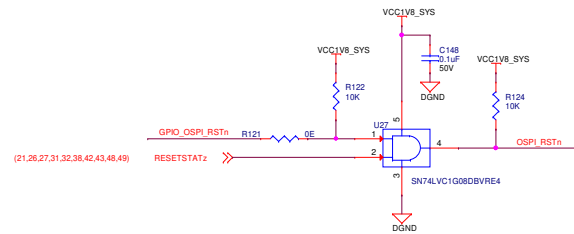


OSPI INTERFACE

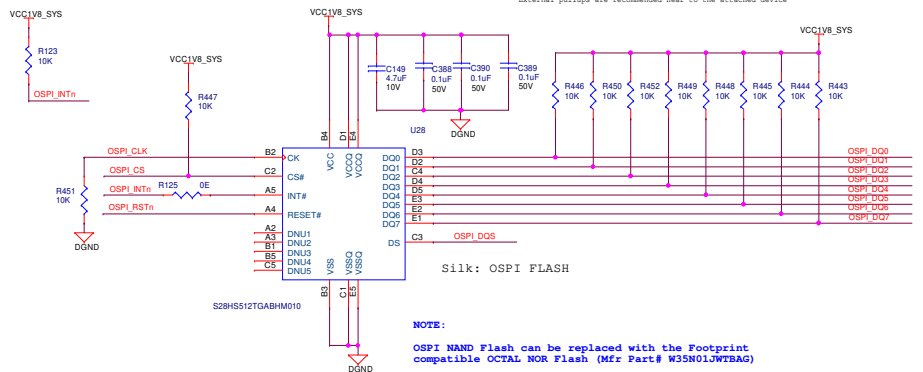
SOC OSPI INTERFACE



OSPI FLASH RESET



OSPI FLASH



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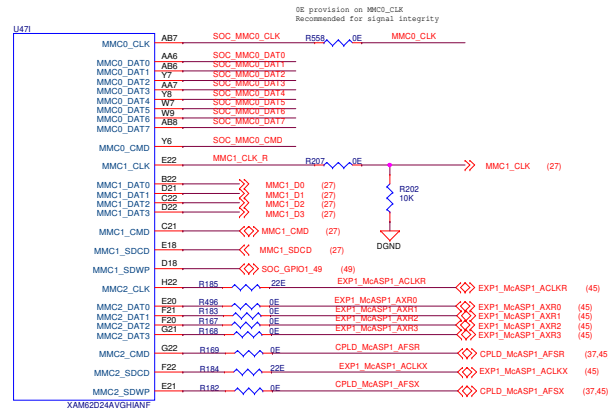
Title OSPI INTERFACE

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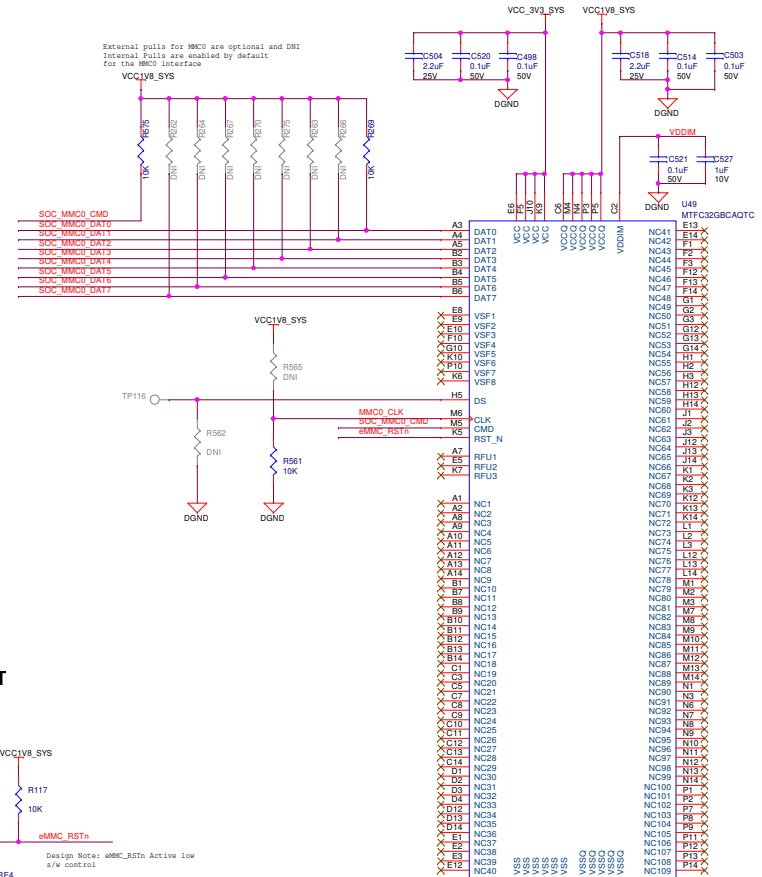
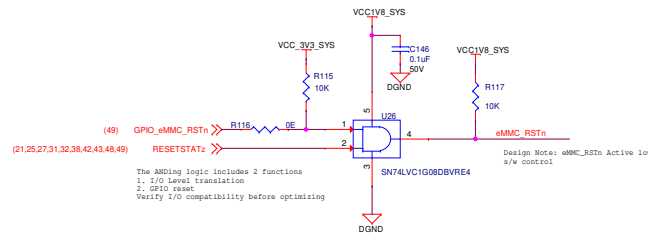
eMMC INTERFACE

eMMC FLASH

SOC - MMC Interface



eMMC FLASH RESET

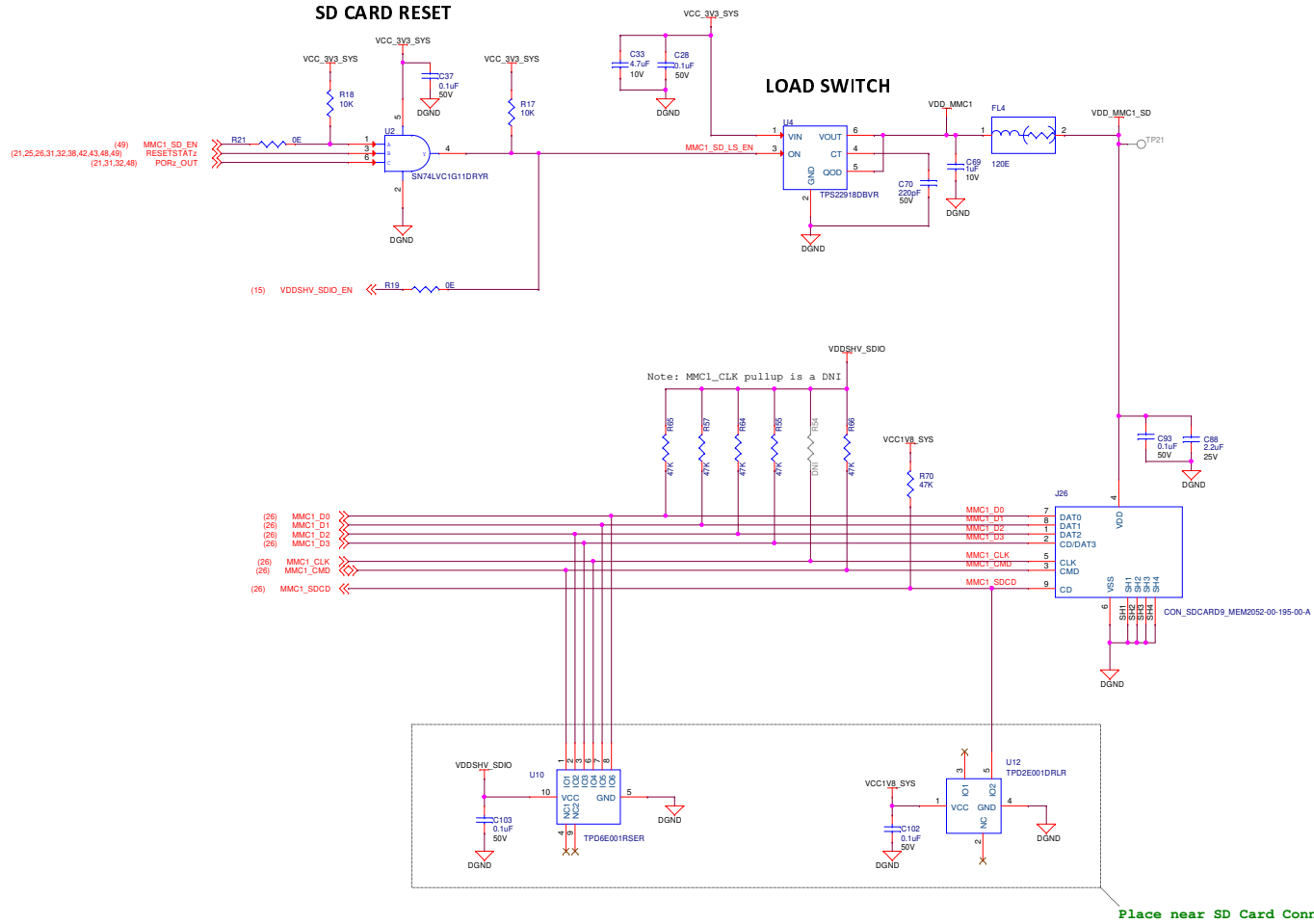


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Title		
eMMC INTERFACE		
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SD CARD INTERFACE



Place near SD Card Connector

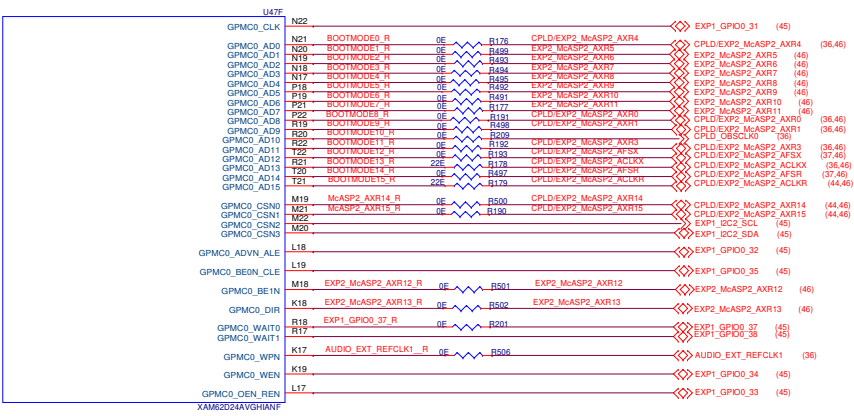
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Title	SD CARD INTERFACE
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SOC GPMC



(23) BOOTMODE0_R
(23) BOOTMODE1_R
(23) BOOTMODE2_R
(23) BOOTMODE3_R
(23) BOOTMODE4_R
(23) BOOTMODE5_R
(23) BOOTMODE6_R
(23) BOOTMODE7_R
(23) BOOTMODE8_R
(23) BOOTMODE9_R
(23) BOOTMODE10_R
(23) BOOTMODE11_R
(23) BOOTMODE12_R
(23) BOOTMODE13_R
(23) BOOTMODE14_R
(23) BOOTMODE15_R

(23) BOOTMODE0_R
(23) BOOTMODE1_R
(23) BOOTMODE2_R
(23) BOOTMODE3_R
(23) BOOTMODE4_R
(23) BOOTMODE5_R
(23) BOOTMODE6_R
(23) BOOTMODE7_R
(23) BOOTMODE8_R
(23) BOOTMODE9_R
(23) BOOTMODE10_R
(23) BOOTMODE11_R
(23) BOOTMODE12_R

SOC CPSW3G ETHERNET INTERFACE



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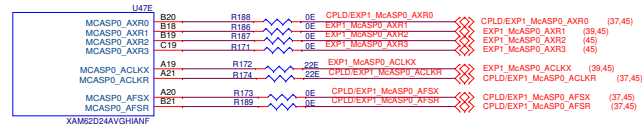
Title SOC PERIPHERALS 1

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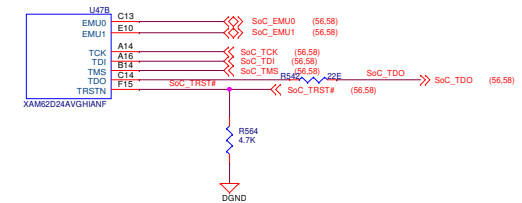
U47K	
CSIO_RXP0	W13
CSIO_RXN0	W12
CSIO_RXP1	Y14
CSIO_RXN1	Y13
CSIO_RXP2	AA12
CSIO_RXN2	AA13
CSIO_RXP3	AB10
CSIO_RXN3	AB11
CSIO_RXCLKP	AB13
CSIO_RXCLKN	AB14
RSVD7	V11
RSVD6	U11
CSIO_RXRCALIB	V10

XAM6D24AVGHIANF

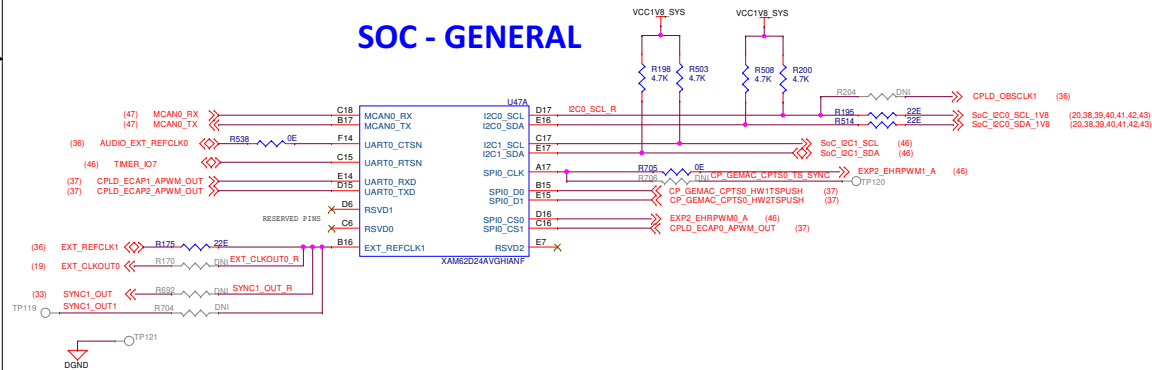
SOC - MCASP



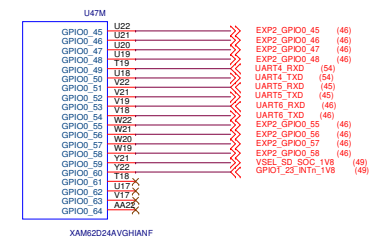
SOC - JTAG



SOC - GENERAL



SOC - UART , GPIOs



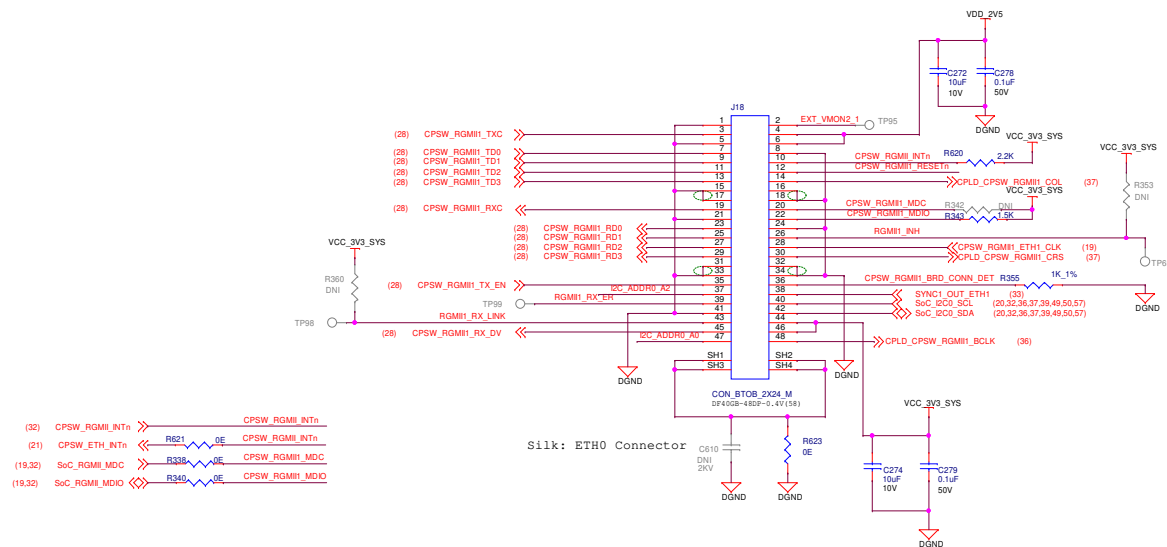
Designed for TI by Mistral Solutions Pvt Ltd



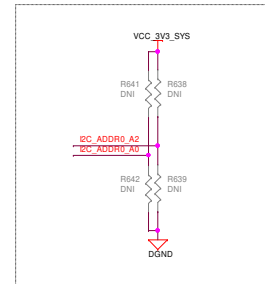
Title SOC PERIPHERALS 3

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Date: Friday, November 29, 2024	Sheet 30 of 59

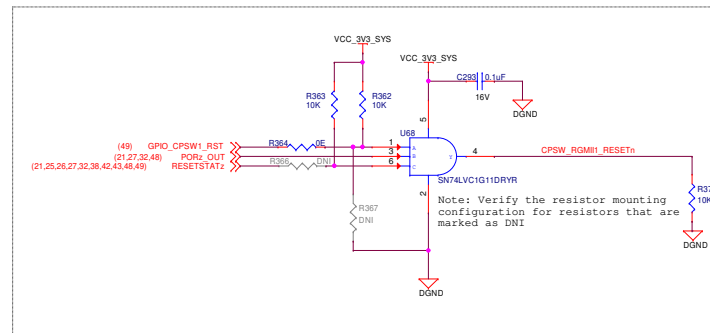
ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 1



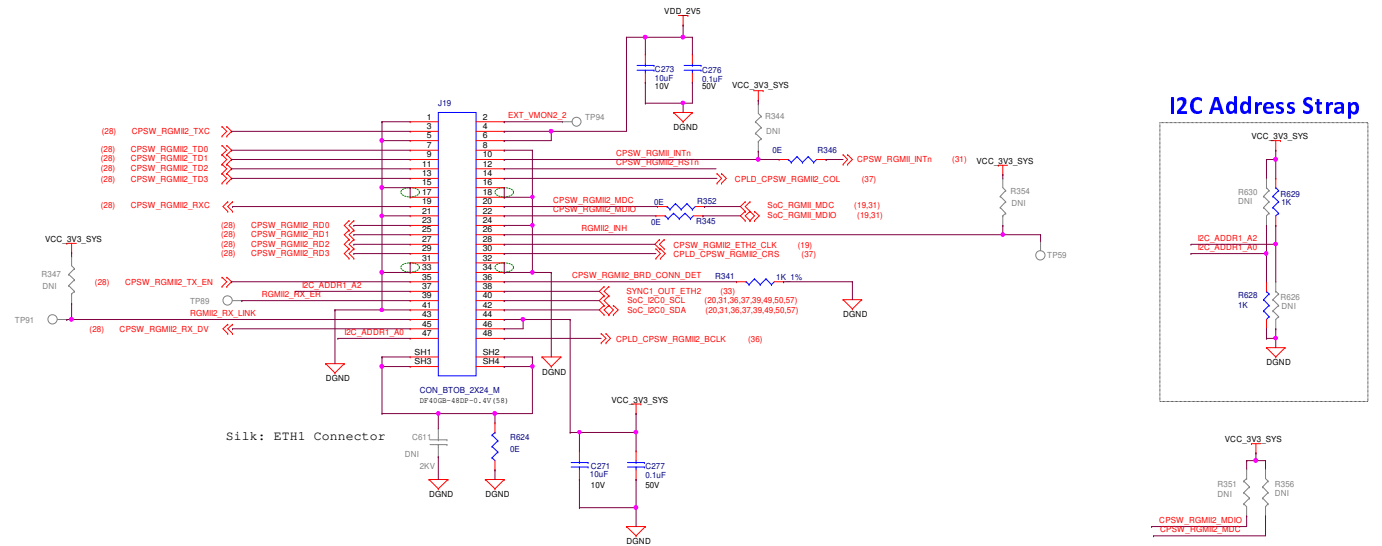
I2C Address Strap



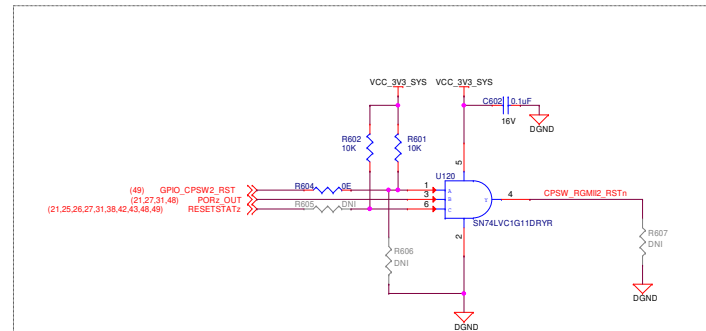
CPSW3G RGMII 1 RESET



ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 2

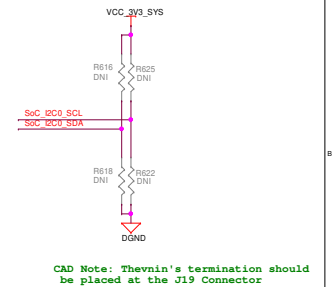
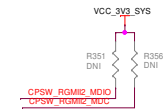
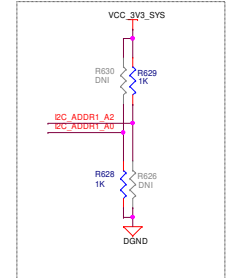


CPSW3G RGMII 2 RESET



Note: Verify the resistor mounting configuration for resistors that are marked as DNI

I2C Address Strap



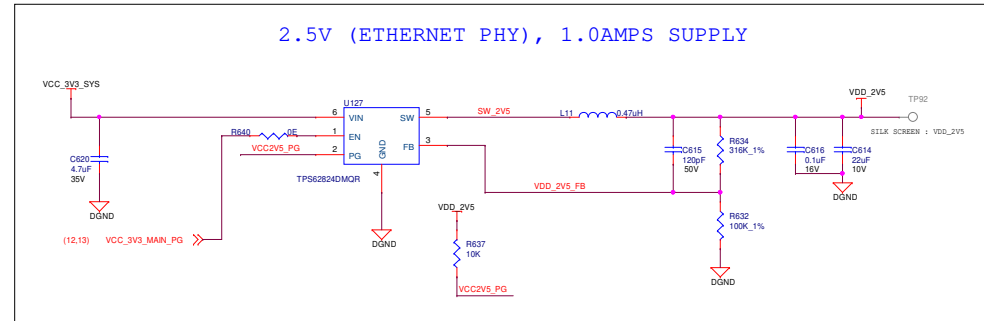
Designed for TI by Mistral Solutions Pvt Ltd



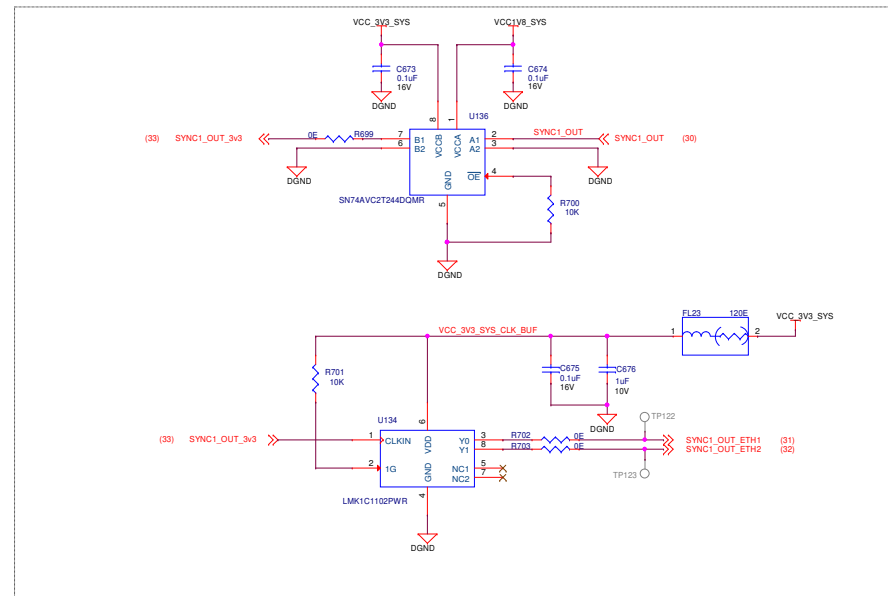
Title: ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 2

Size	Rev
C	PROC180E2
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POWER SUPPLY (CORE) FOR ETHERNET PHY



D-Note : 2.5V Power supply for Ethernet PHY is generated by the PMIC



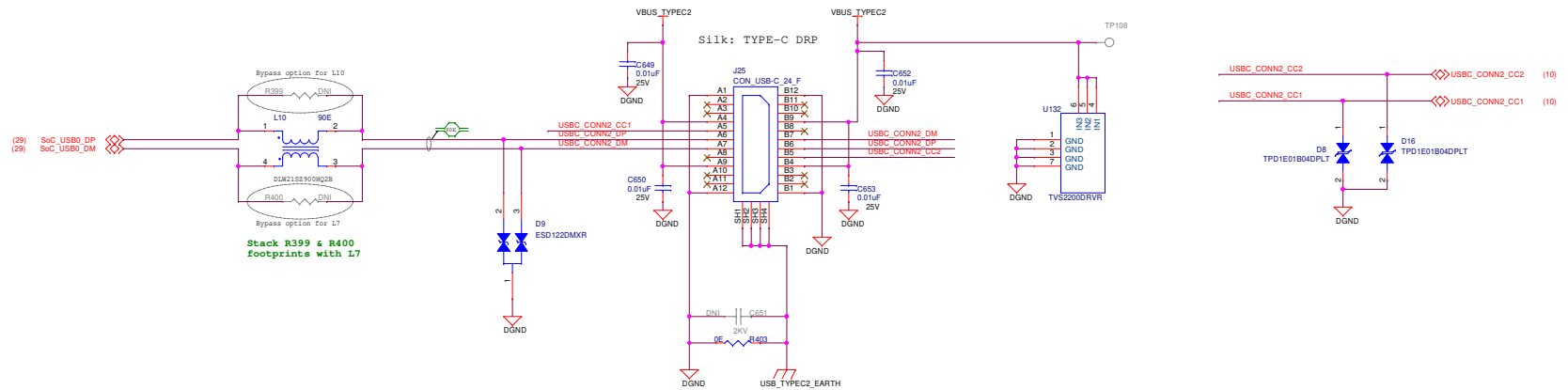
Designed for TI by Mistral Solutions Pvt Ltd



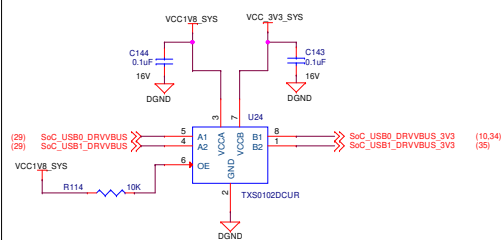
Title POWER SUPPLY (CORE) FOR ETHERNET PHY

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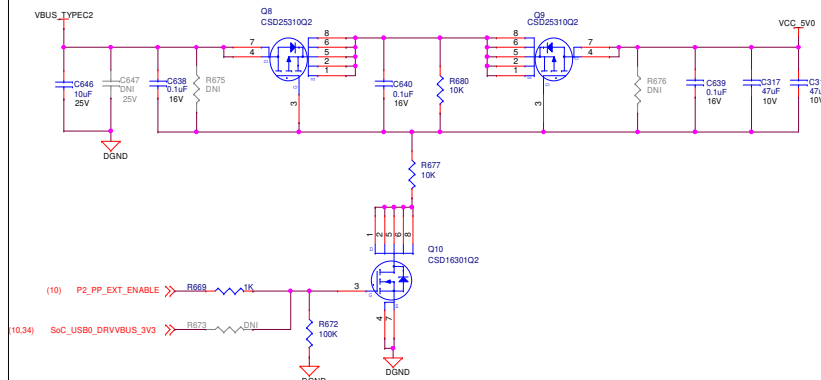
USB0 TYPE-C DRP



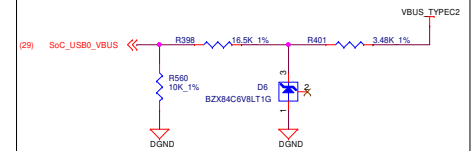
USB_DRV BUS LEVEL TRANSLATOR



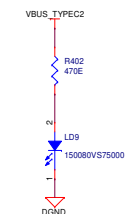
EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



Note: Refer data sheet USB VBUS Design Guidelines section.



POWER INDICATION LED: VBUS_TYPEC2



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Title	USB0 TYPE-C DRP
-------	-----------------

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Note: Refer data sheet USB VBUS Design Guidelines section.

(29) SoC_USB1_VBUS

R384 16.5K 1%

R567 10K 1%

DGND

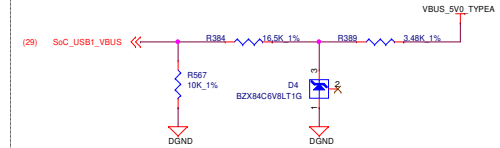
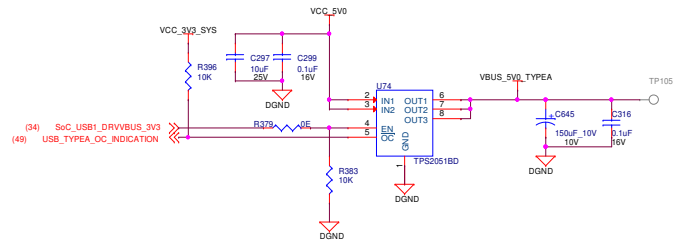
D4 BZX84C6V8LT1G

R385 3.48K 1%

R568 10K 1%

DGND

VBUS_5V0_TYPEA



The schematic diagram illustrates the internal structure and connections of the CPLD1 component. It is divided into three main banks: BANK 0, BANK 1, and BANK 2. BANK 0 contains the CPLD1_TDO, CPLD1_TDI, CPLD1_TCK, and CPLD1_TMS pins, along with the CPLD1_TAGENB, CPLD1_PROGRAM, CPLD1_N7N, and CPLD1_DONE pins. BANK 1 contains the CPLD1_TDO, CPLD1_TDI, CPLD1_TCK, and CPLD1_TMS pins, along with the CPLD1_TAGENB, CPLD1_PROGRAM, CPLD1_N7N, and CPLD1_DONE pins. BANK 2 contains the CPLD1_TDO, CPLD1_TDI, CPLD1_TCK, and CPLD1_TMS pins, along with the CPLD1_TAGENB, CPLD1_PROGRAM, CPLD1_N7N, and CPLD1_DONE pins. The diagram also shows the connection of the CPLD1 to the LCMXO2-640HC-45G481 component, which is connected to the VCC3V3_SYS and VCC1V8_SYS power rails. The LCMXO2-640HC-45G481 component is connected to the CPLD1 via a 40-pin connector. The diagram also shows the connection of the CPLD1 to the VCC3V3_SYS and VCC1V8_SYS power rails. The VCC3V3_SYS rail is connected to the CPLD1 via a 10k resistor (R458) and a 10k resistor (R459). The VCC1V8_SYS rail is connected to the CPLD1 via a 10k resistor (R458) and a 10k resistor (R459). The diagram also shows the connection of the CPLD1 to the VCC3V3_SYS and VCC1V8_SYS power rails. The VCC3V3_SYS rail is connected to the CPLD1 via a 10k resistor (R458) and a 10k resistor (R459). The VCC1V8_SYS rail is connected to the CPLD1 via a 10k resistor (R458) and a 10k resistor (R459).

PROGRAMMING HEADER

VCC_3V3_SYS

0.1uF C377

16V

GND

J8

1 2 3 4 5 6

CPLD1_TCK

CPLD1_TMS

CPLD1_RST

CPLD1_TDO

61300811121

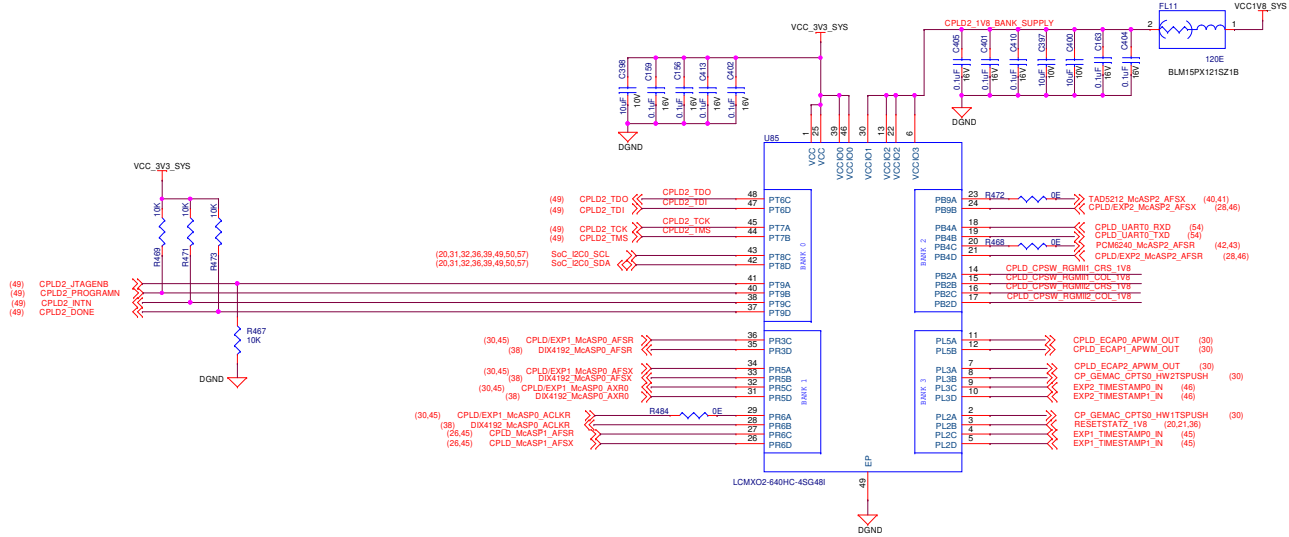
GND

R437 4.7K

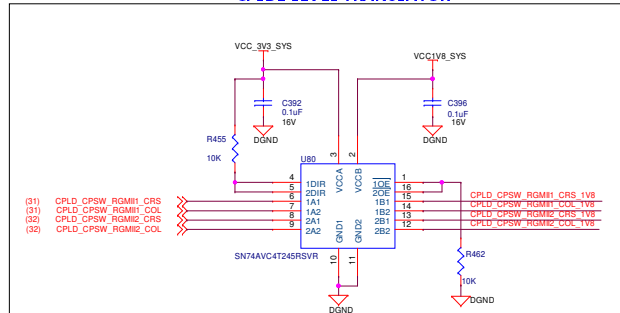
VCC_3V3_SYS

Silk Screen "CPLD JTAG"

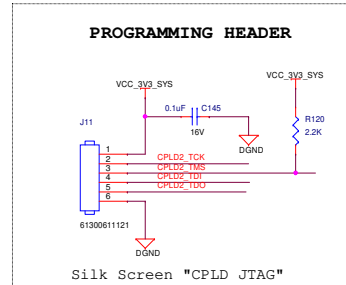
CPLD 2



CPLD2 LEVEL TRANSLATOR



PROGRAMMING HEADER



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Title	CPLD 2
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AUDIO - DIGITAL IN & OUT, OPTICAL IN -1

DIR: FIBER OPTIC RECEIVER MODULE

DIX Supply & Decaps

DEVICE STRAP

DIX4192 RESET

DIT & DIR COAXIAL INPUT

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TEXAS INSTRUMENTS

MISTRAL

PROC180E2

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Rev E2

DEVICE STRAP

VCC1V8_VDD18

R425
DNI

MODE_SELECT

R426
DNI

GND

VCC1V8_VDD18

R47
DNI

R50
DNI

R48
DNI

DIX_ADDR1
VCC_ADDR1

GND

DIX4192 RESET

(49) GPIO_DIX_RST
RESETSTATz

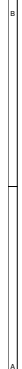
(21,25,26,27,31,32,42,43,48,49)

DIT & DIR COAXIAL INPUT

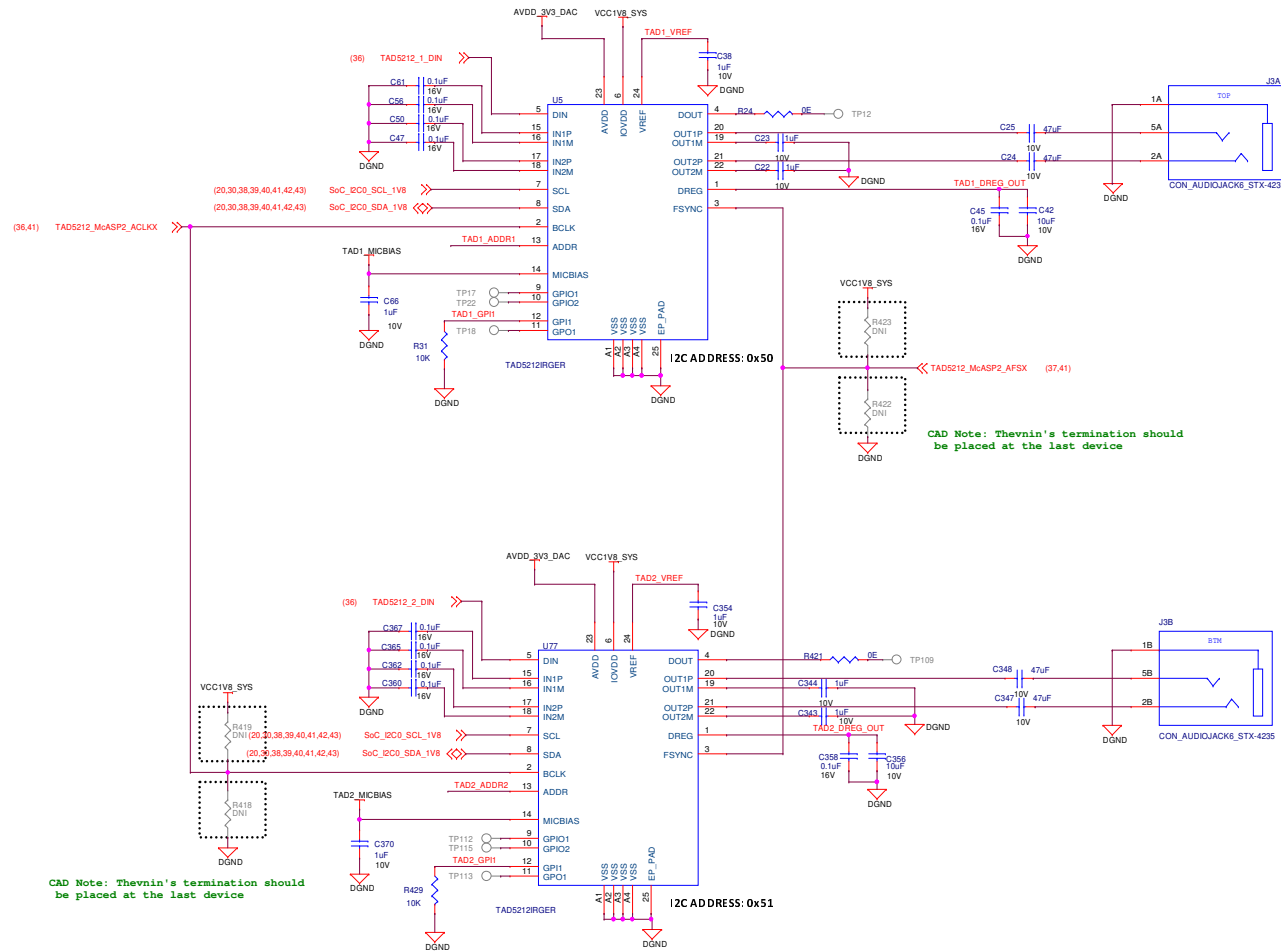


Size		Rev	
C	PROC180E2	E2	
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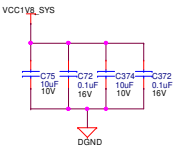
A vertical bar divided into four segments labeled A, B, C, and D from bottom to top. Segment B contains a right-pointing arrow.



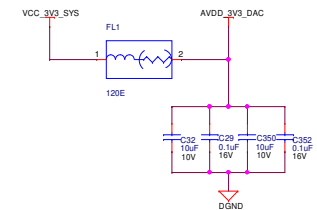
AUDIO - STEREO LINEOUT - 1



DAC Supply & Decaps

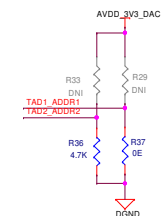


CAD Note: Place these decaps near the DVDD supply pin of DAC's



CAD Note: Place these decaps near the AVDD supply pin of DAC's

DAC I2C Address Straps



AUDIO - STEREO LINEOUT - 2

DAC Supply & Decaps

CAD Note: Place these decaps near the DVDD supply pin of DAC's

Device Straps

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Title	
AUDIO - STEREO LINEOUT - 2	
Size	PROC180E2
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Rev
E2

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Title	
AUDIO - STEREO LINEOUT - 2	
Size	PROC180E2
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Rev
E2

AUDIO - STEREO LINEOUT - 2

I2C ADDRESS: 0x52

I2C ADDRESS: 0x53

DAC Supply & Decaps

CAD Note: Place these decaps near the DVDD supply pin of DAC's

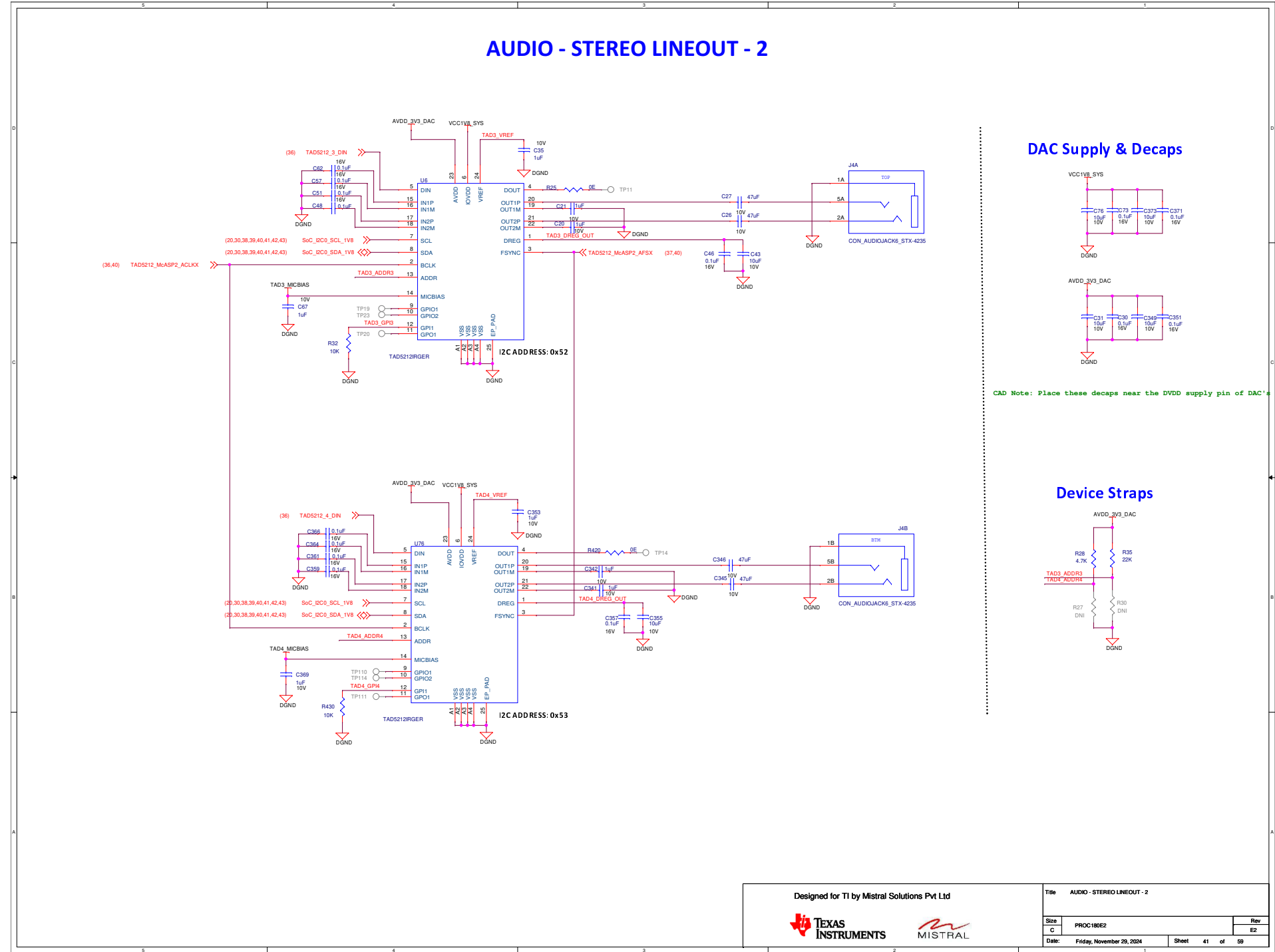
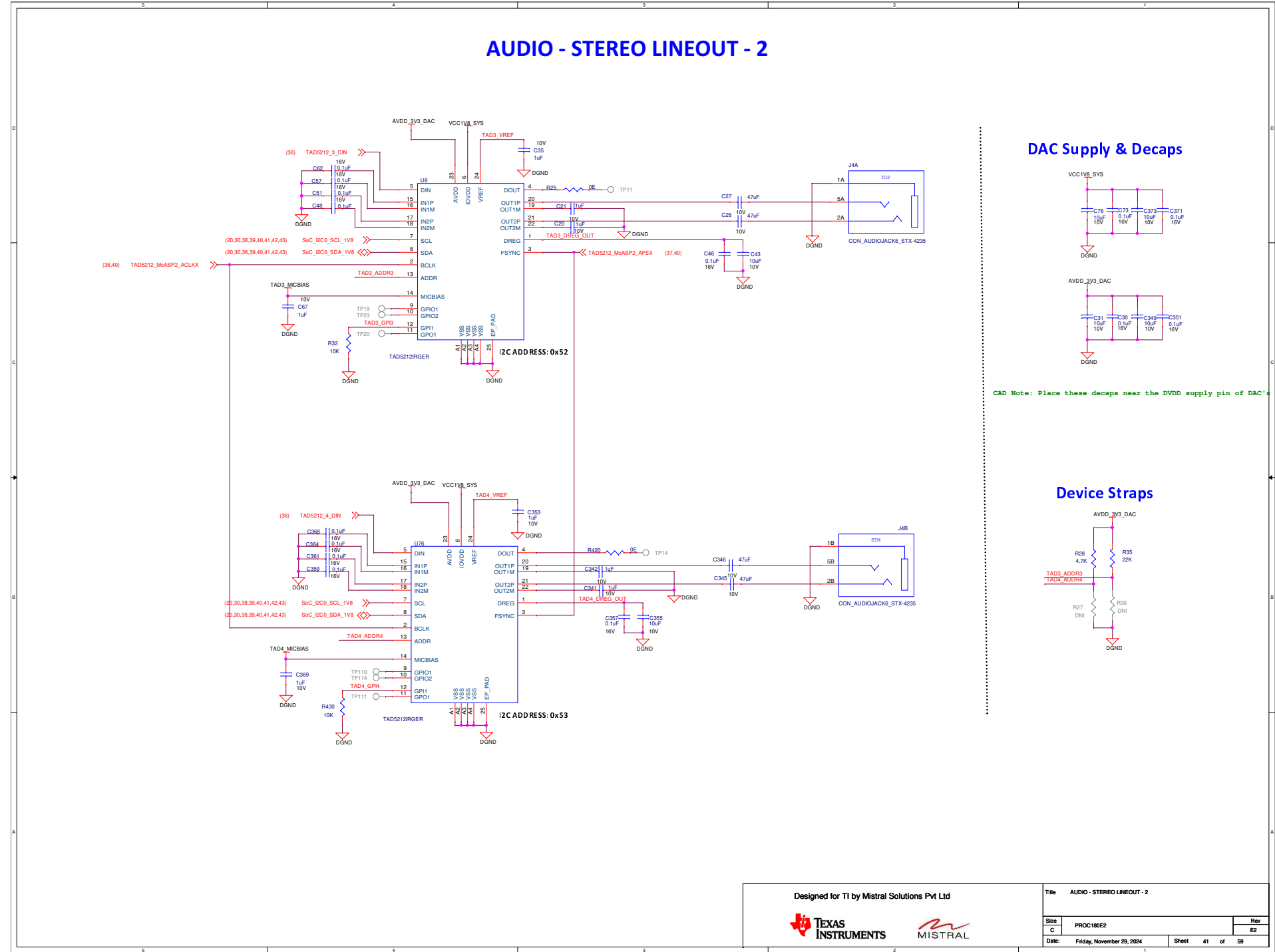
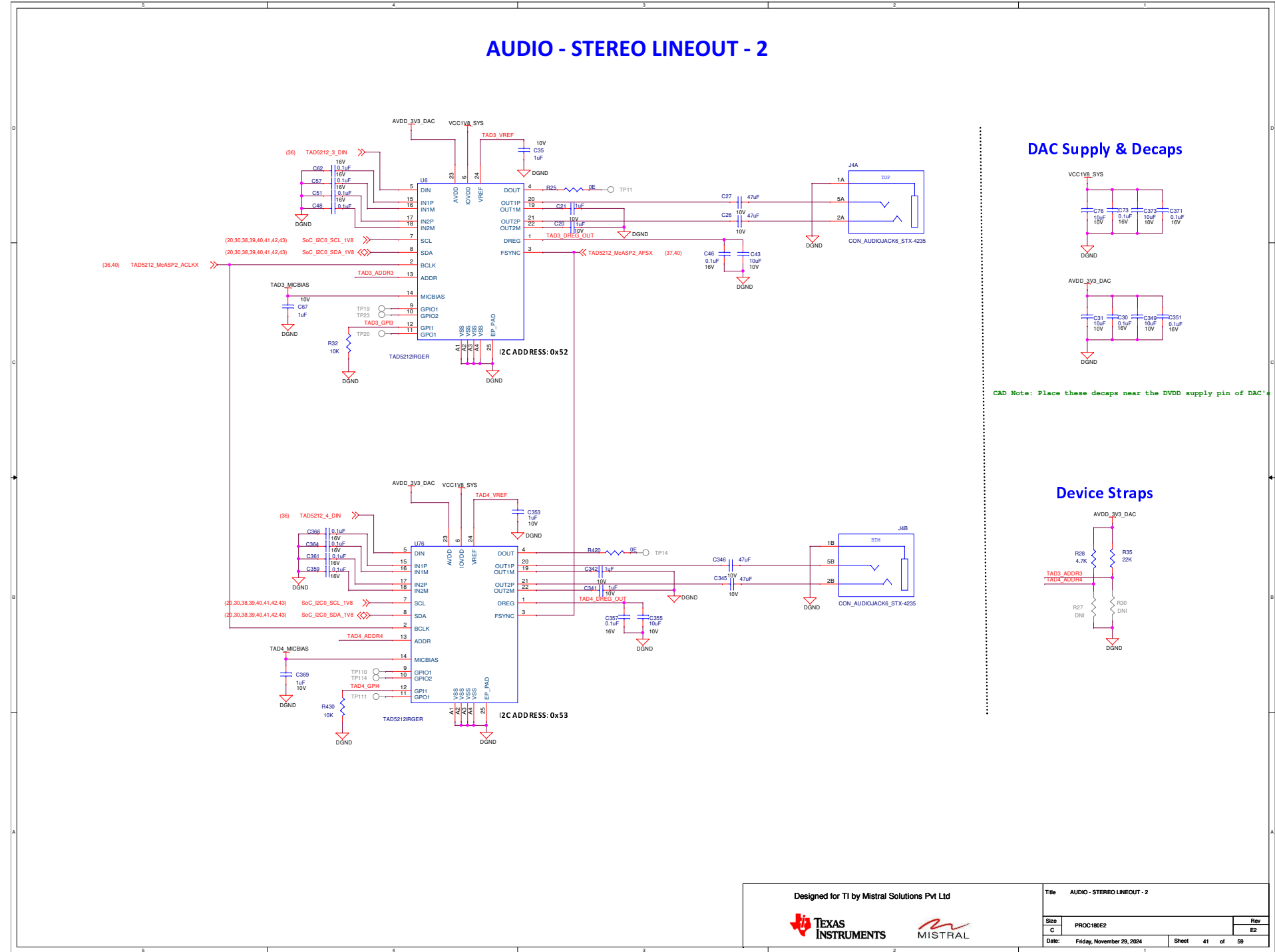
Device Straps

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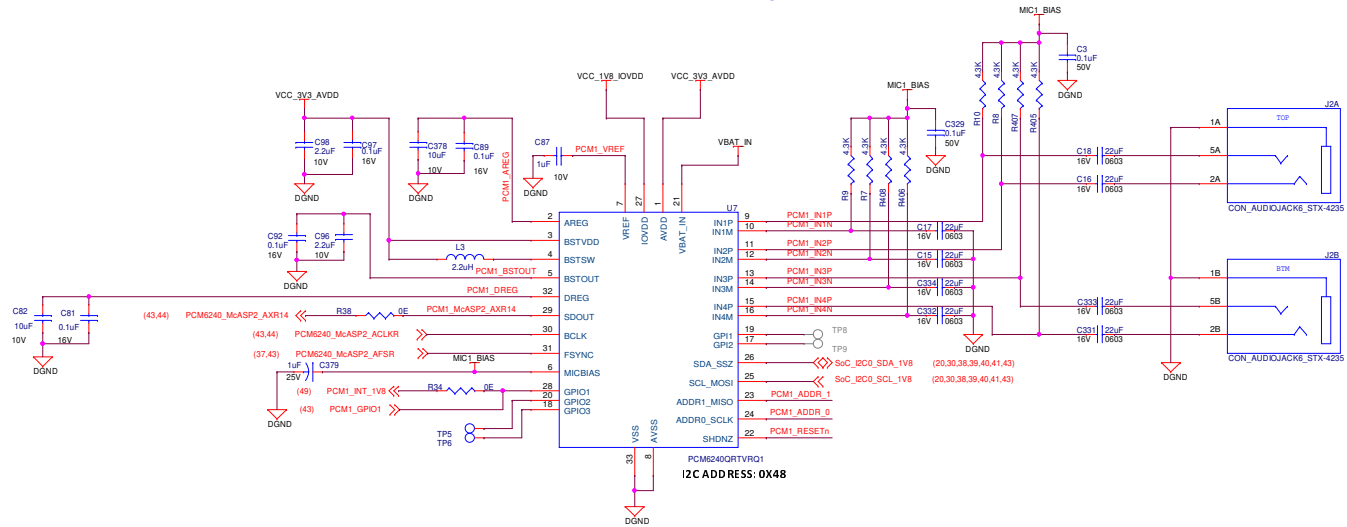
TEXAS INSTRUMENTS MISTRAL

Title	
AUDIO - STEREO LINEOUT - 2	
Size	PROC180E2
Date	Friday, November 29, 2024

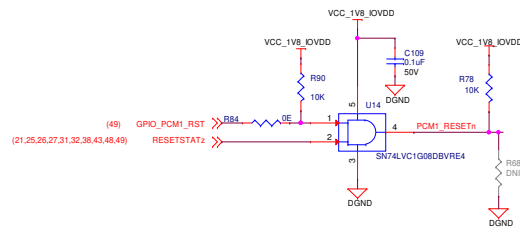
Rev	Rev
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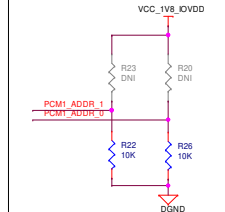
AUDIO - MICROPHONE/LINE IN 1



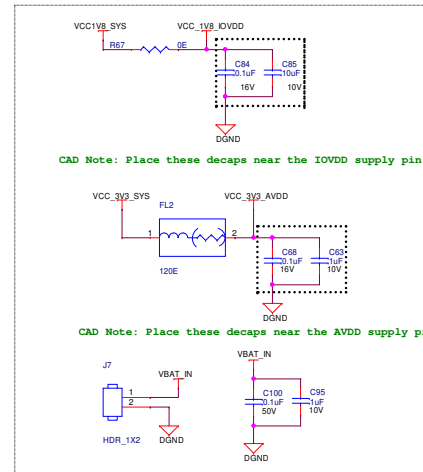
PCM1 RESET



I2C address selection device 1



ADC Supply & Decaps

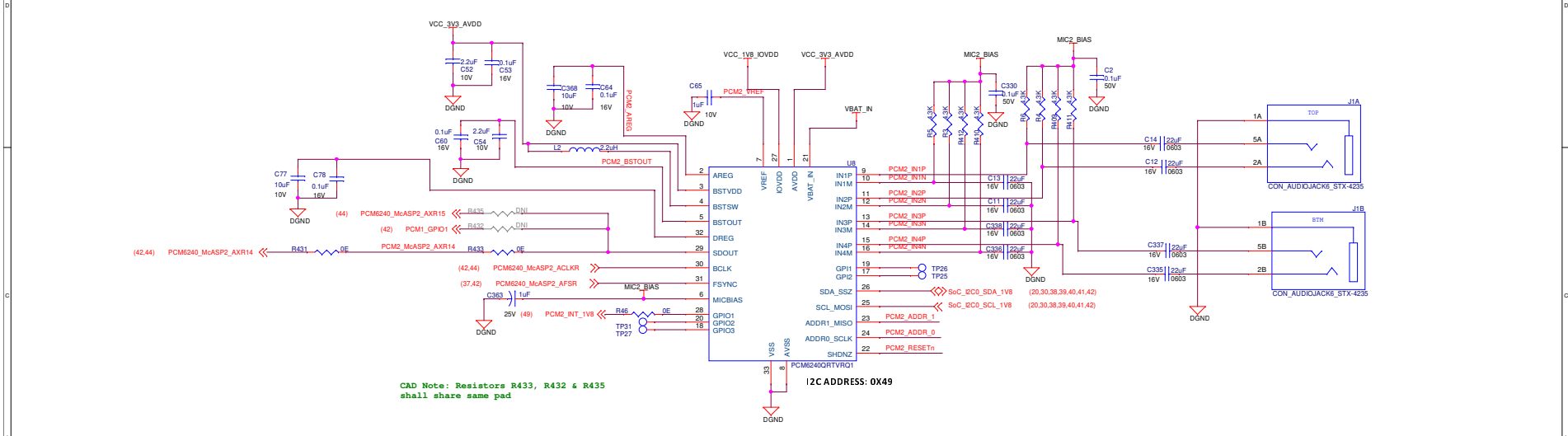


Designed for TI by Mistral Solutions Pvt Ltd

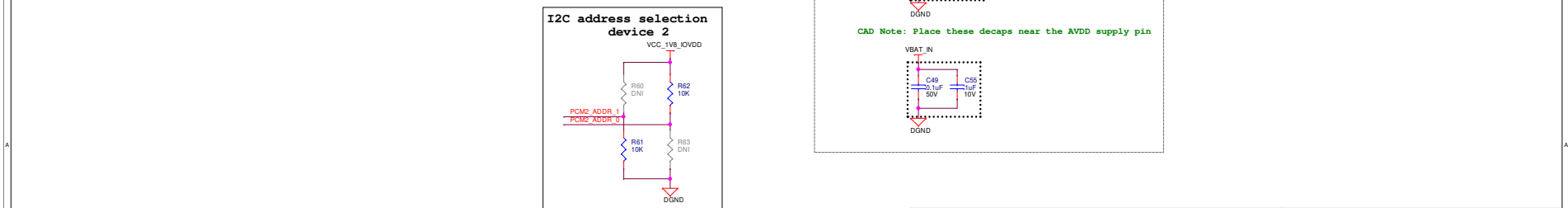
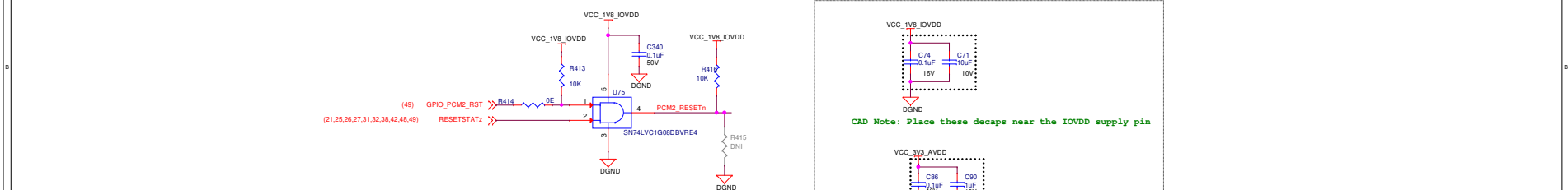


Title AUDIO - MICROPHONE/LINE IN 1

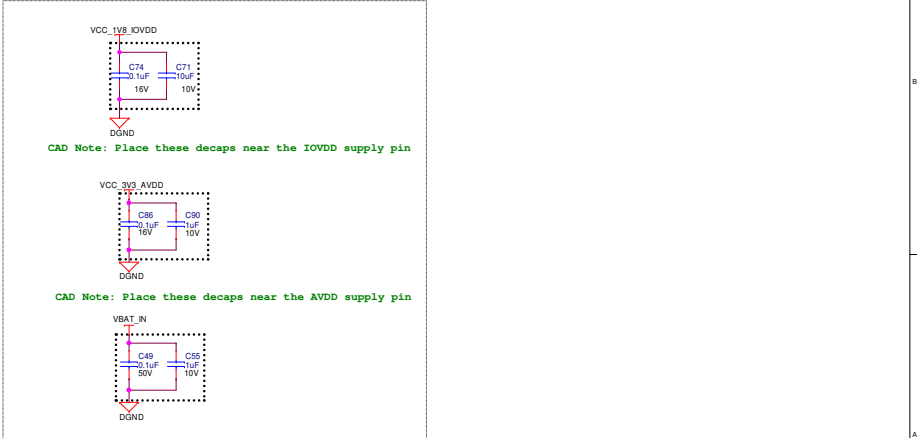
Size	Rev
C	PROC180E2
Date:	Friday, November 29, 2024
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PCM2 RESET ADC Supply & Decaps



ADC Supply & Decaps



Designed for TI by Mistral Solutions Pvt Ltd		Title: AUDIO - MICROPHONE/LINE IN 2	
		Size	Rev
		C	E2
Date: Friday, November 29, 2024		Sheet	43 of 59



MISTRA

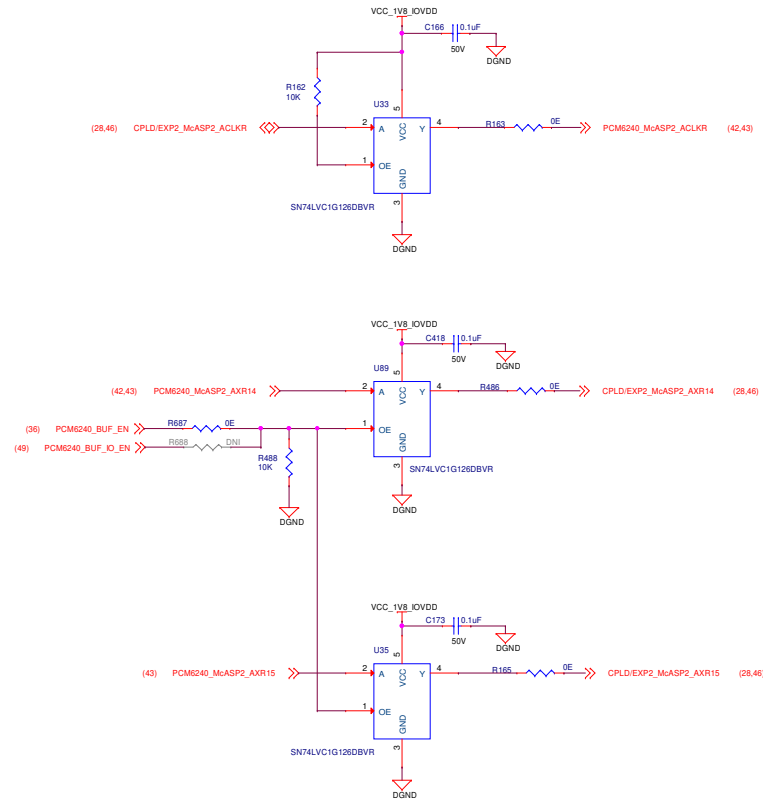
Title				AUDIO - MICROPHONE/LINE IN 2			
Size		PROC180E2				Rev	
C						E2	
Date:			Friday, November 29, 2024		Sheet 43 of 59		

Rev

E2

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PCM6240 BUFFERS



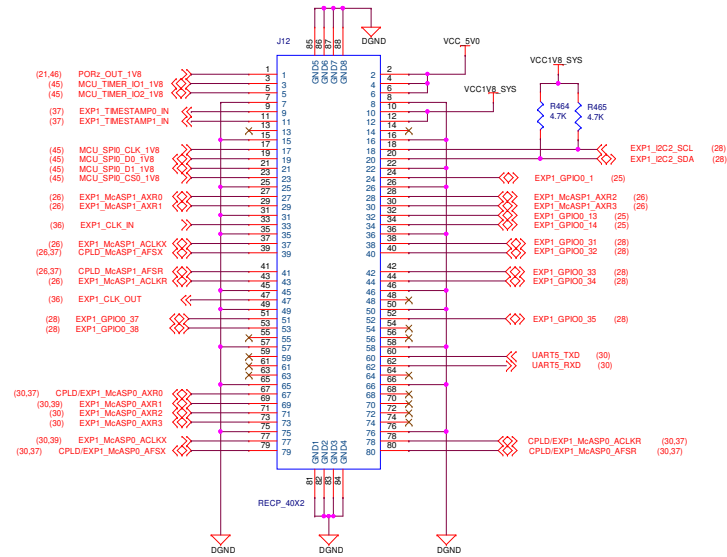
Designed for TI by Mistral Solutions Pvt Ltd



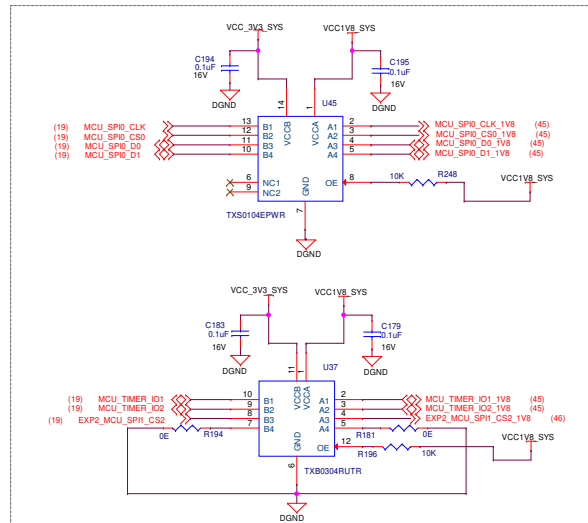
Title PCM6240 BUFFERS

Size	Rev
C	E2
Date:	Friday, November 29, 2024
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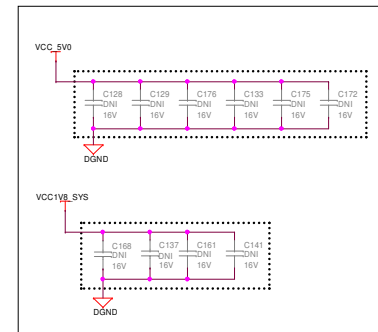
AUDIO EXPANSION CONNECTOR #1



AEC1 LEVEL TRANSLATORS



AUDIO EXPANSION DECAPS



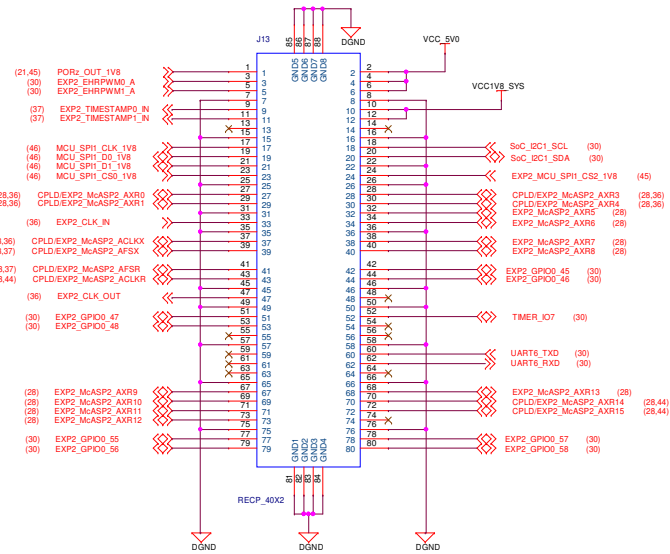
Designed for TI by Mistral Solutions Pvt Ltd



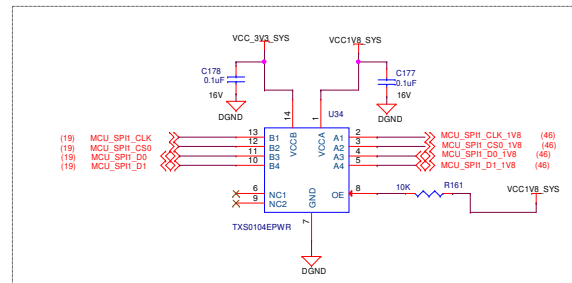
Title AUDIO EXPANSION CONNECTOR #1

Size	Rev
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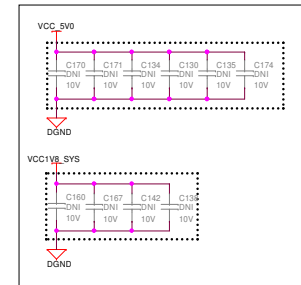
AUDIO EXPANSION CONNECTOR #2



AEC2 LEVEL TRANSLATOR



AUDIO EXPANSION DECAPS



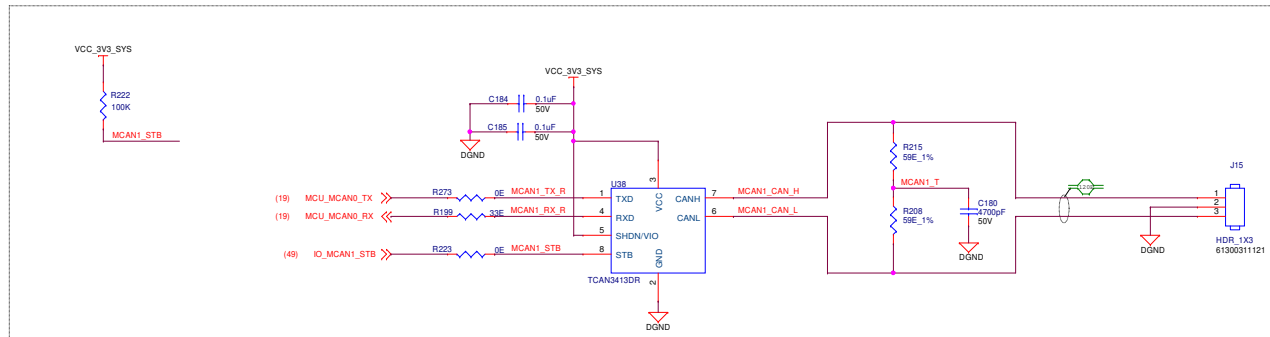
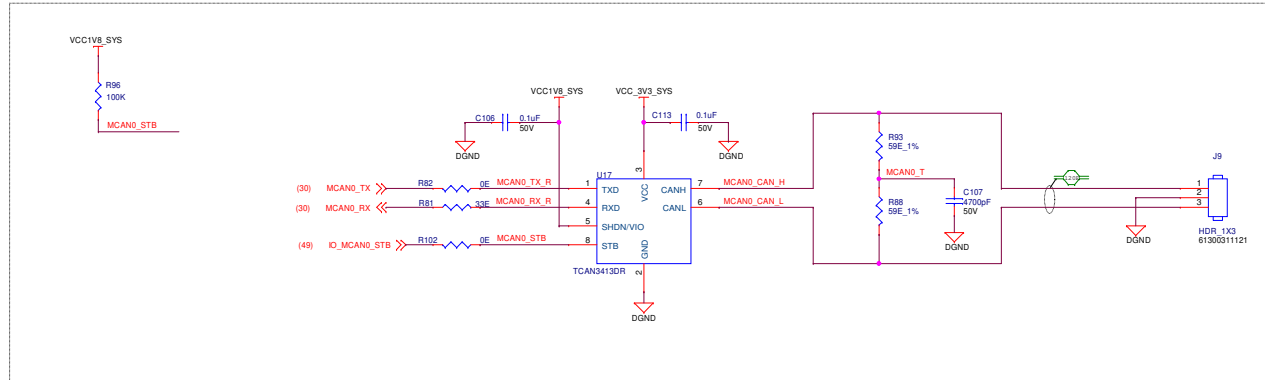
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Title AUDIO EXPANSION CONNECTOR #2

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Date: Friday, November 29, 2024	Sheet 46 of 59

CAN TRANSCEIVER



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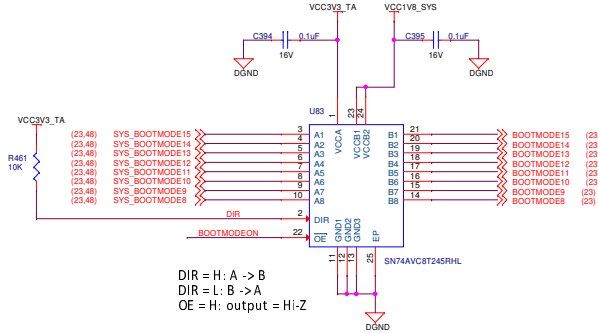
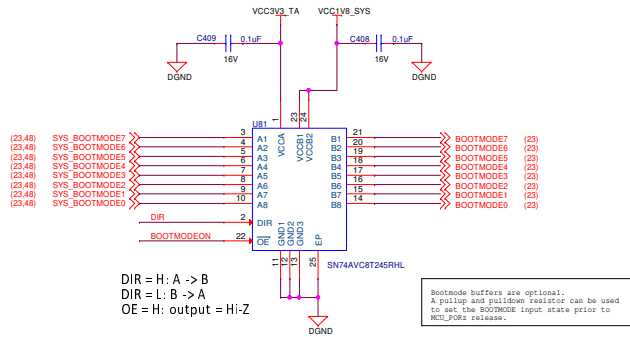


Title CAN TRANSCEIVER

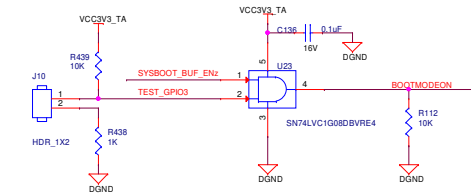
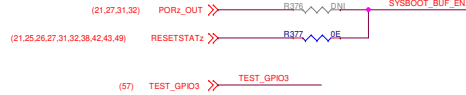
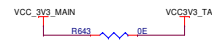
Size	Rev
C	E2
Date:	Friday, November 29, 2024
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BOOTMODE BUFFERS AND IO EXPANDERS

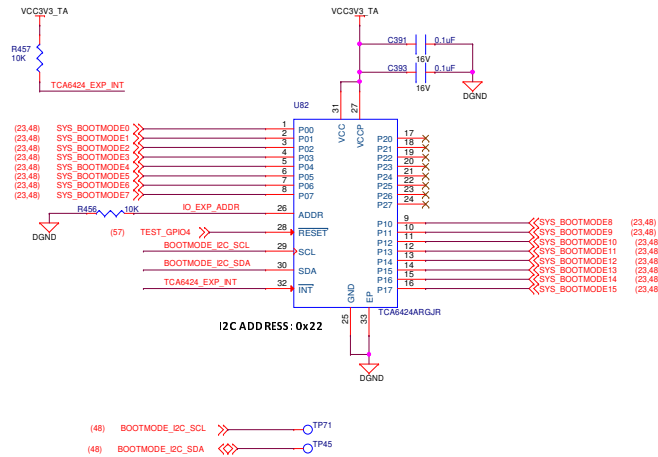
BOOT MODE BUFFERS



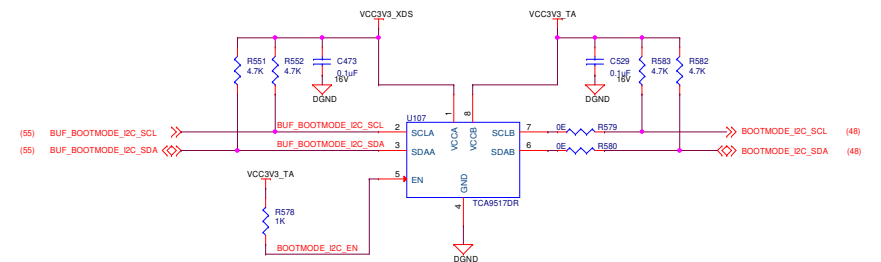
TEST AUTOMATION SUPPLY



BOOTMODE IO EXPANDER



BOOTMODE I2C BUS BUFFER



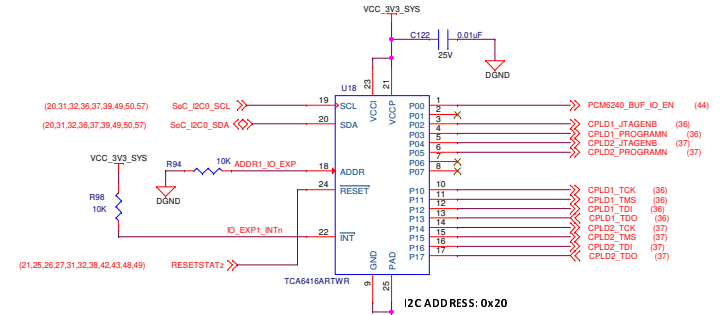
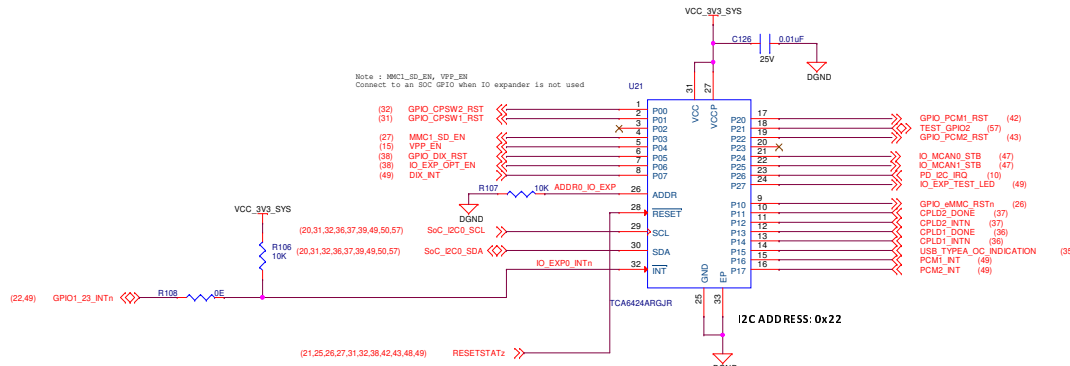
Designed for TI by Mistral Solutions Pvt Ltd



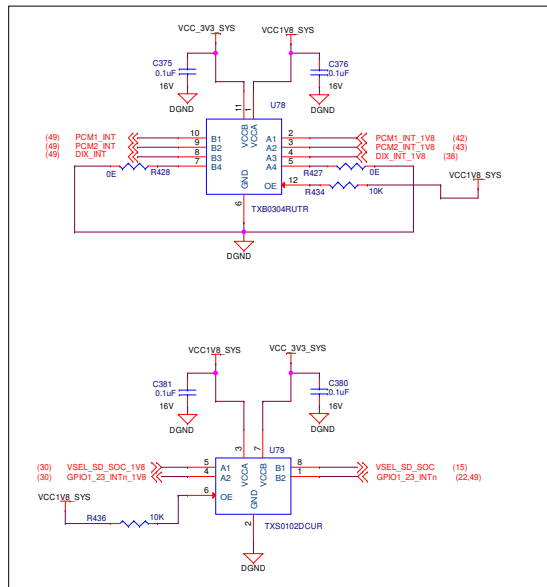
Title BOOT MODE BUFFER & IO EXPANDERS

Size	Rev
C	PROC180E2
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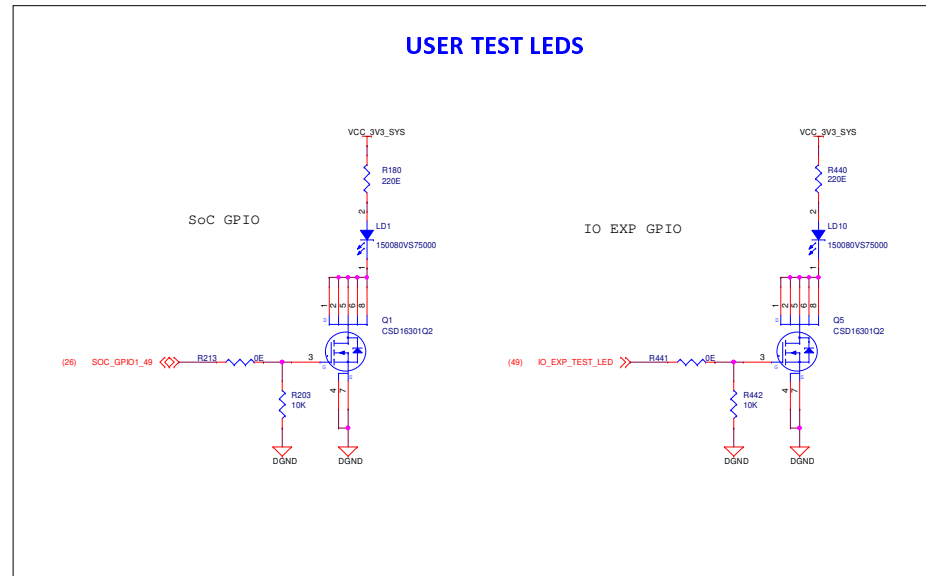
IO EXPANDER



LEVEL TRANSLATOR



USER TEST LEDS



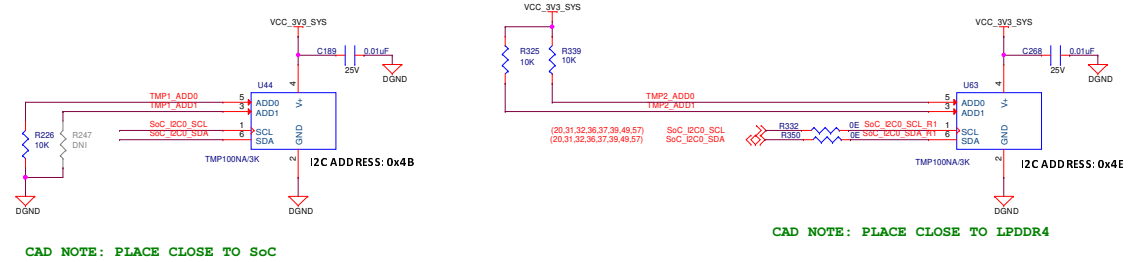
Designed for TI by Mistral Solutions Pvt Ltd



Title IO EXPANDER & USER TEST LEDS

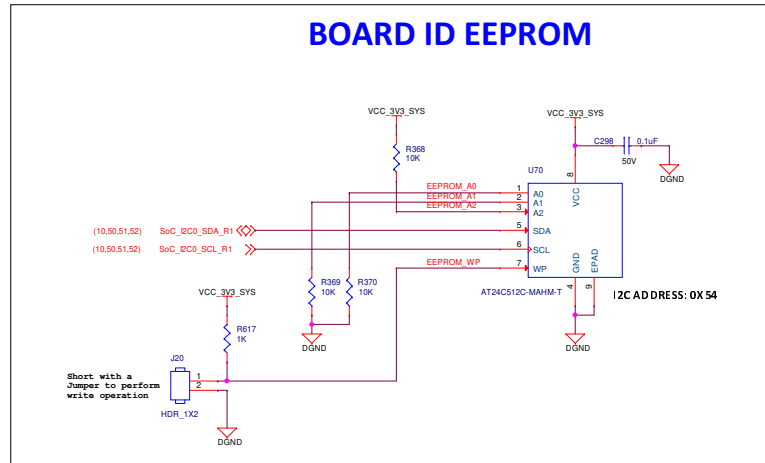
Size	Rev
C	PROC180E2
Date:	Friday, November 29, 2024
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TEMPERATURE SENSORS



(10,50,51,52) SoC_I2C0_SCL_R1 >> TP88
(10,50,51,52) SoC_I2C0_SDA_R1 << TP90

BOARD ID EEPROM



PROC180E2

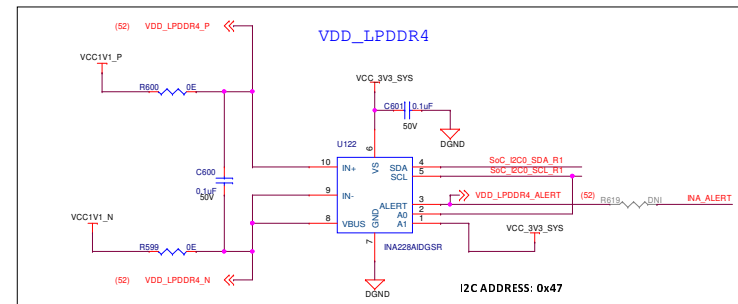
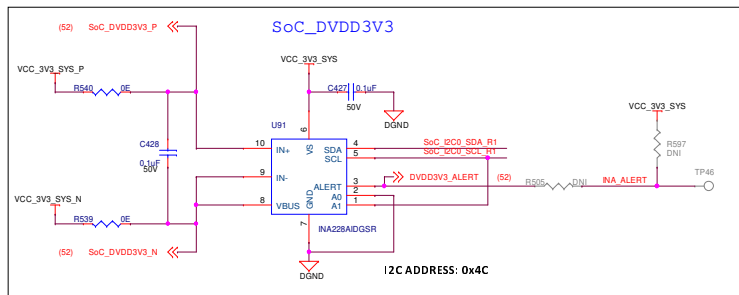
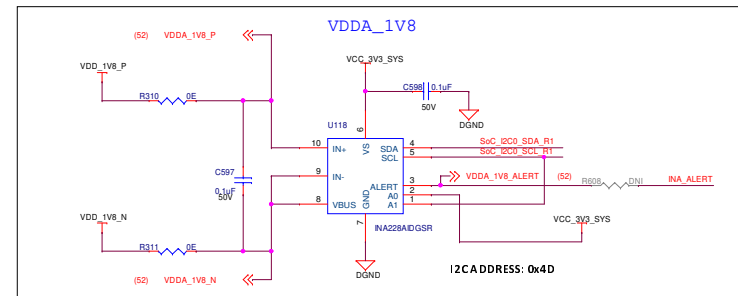
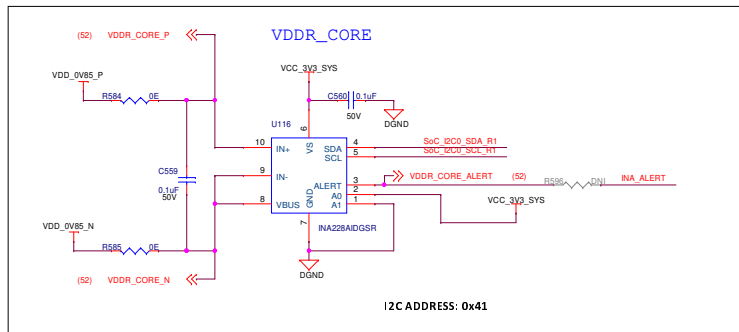
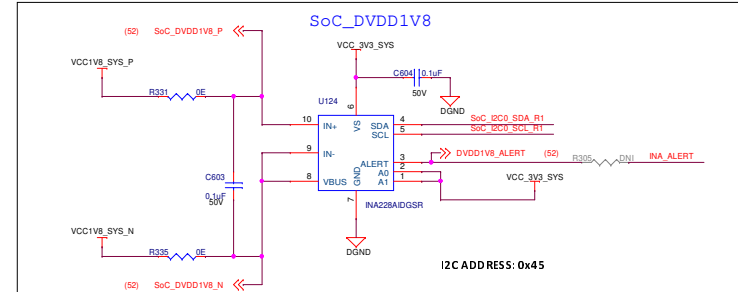
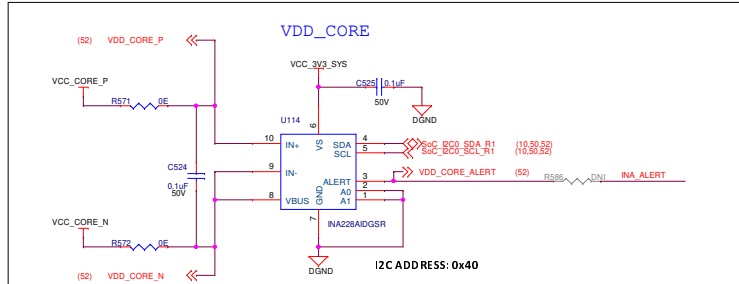
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Title TEMPERATURE SENSORS & BOARD ID EEPROM

Size	Rev
C	E2
Date: Friday, November 29, 2024	Sheet 50 of 59

CURRENT MONITORING DEVICES - 1



Note: The design supports current/voltage measurements using either INA228 or INA231. (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_OV85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

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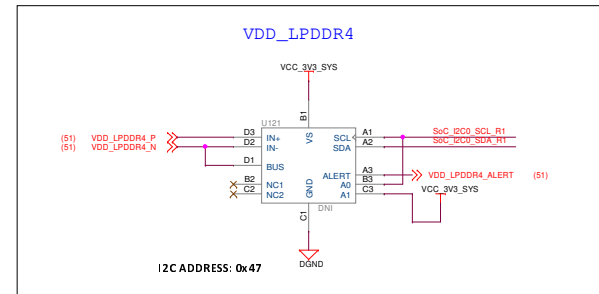
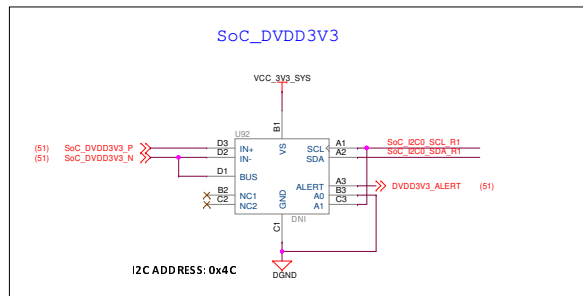
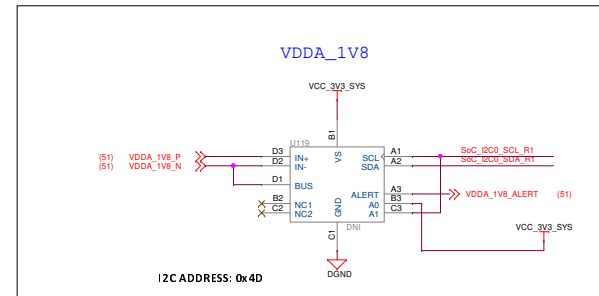
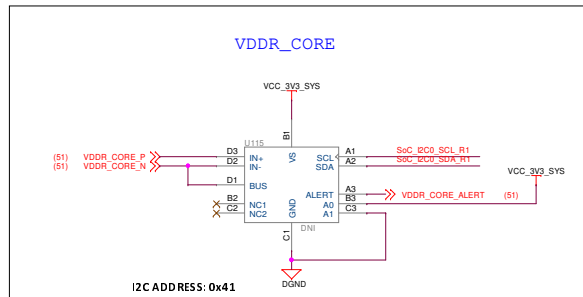
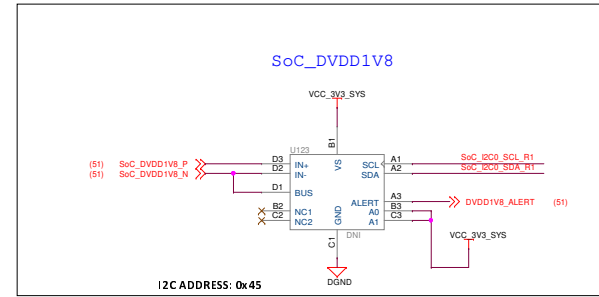
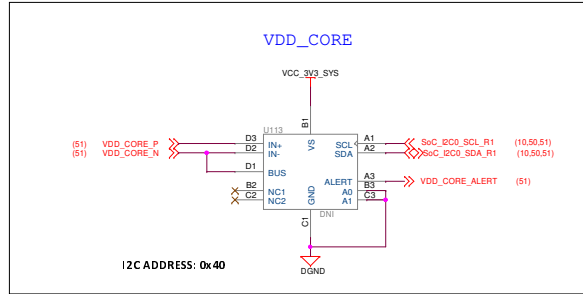


Title CURRENT MONITORING DEVICES - 1

Size	Rev
C	PROC180E2_SCH
Date:	Friday, November 29, 2024

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CURRENT MONITORING DEVICES - 1



Note: The design supports current/voltage measurements using either INA228 or INA231. (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

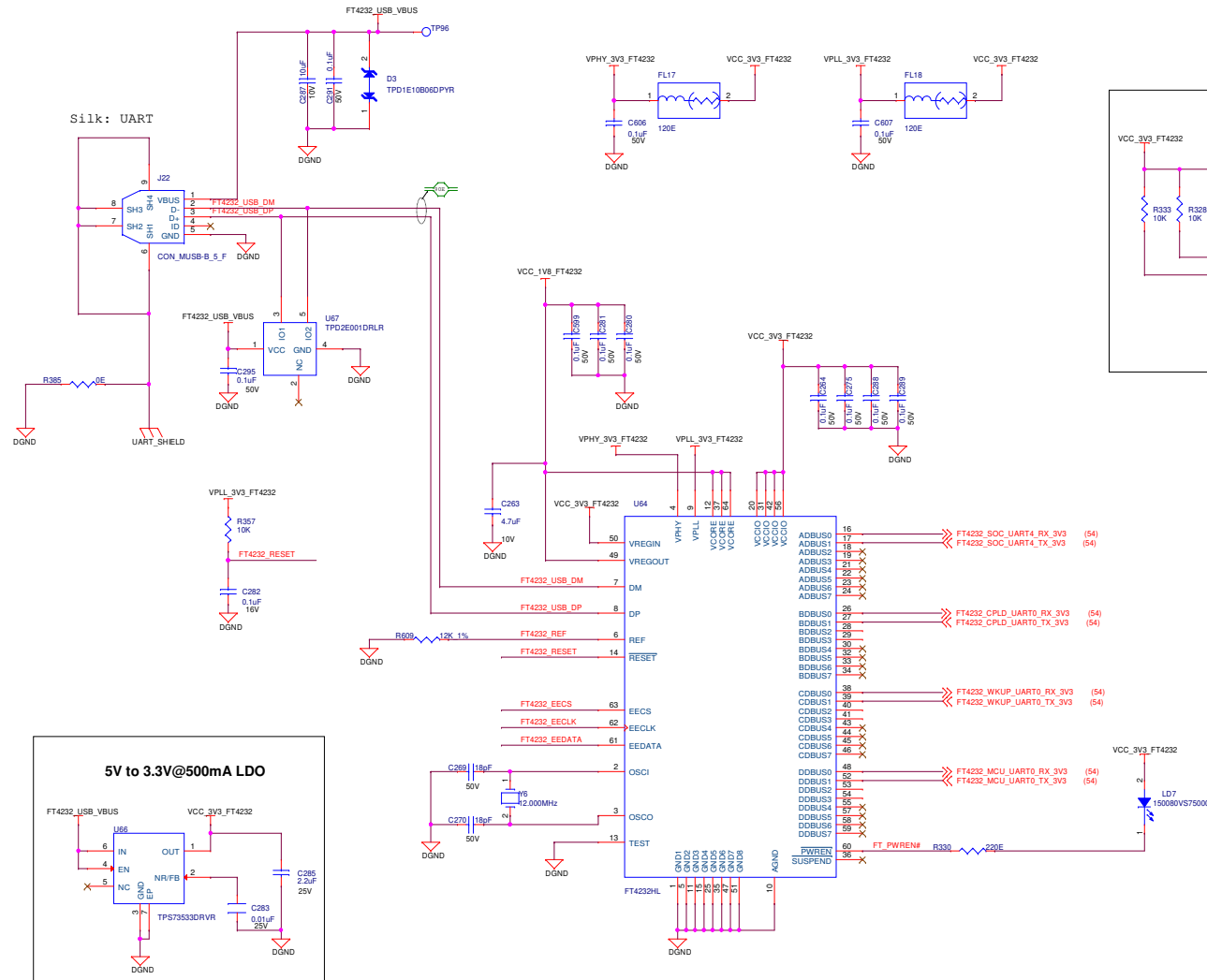
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Title CURRENT MONITORING DEVICES - 2

Size	Rev
C	E2
Date: Friday, November 29, 2024	Sheet 52 of 59

USB TO UART BRIDGE



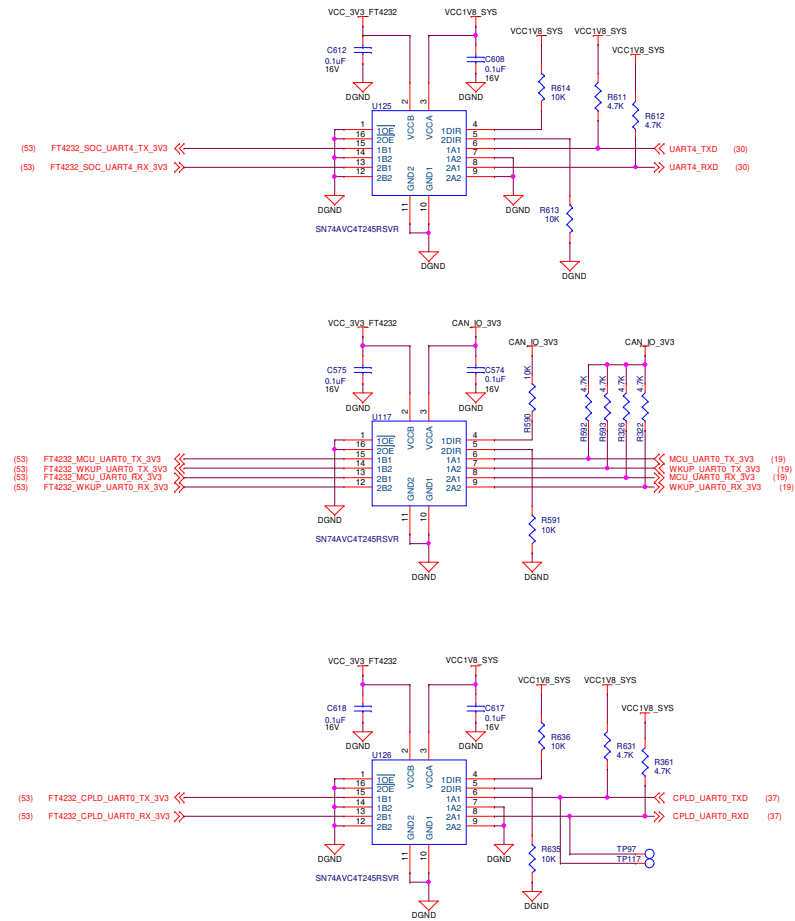
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Title FT4232 UART to USB BRIDGE

Size	Rev
C	PROC180E2
Date:	Friday, November 29, 2024
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FT4232 UART BUFFERS



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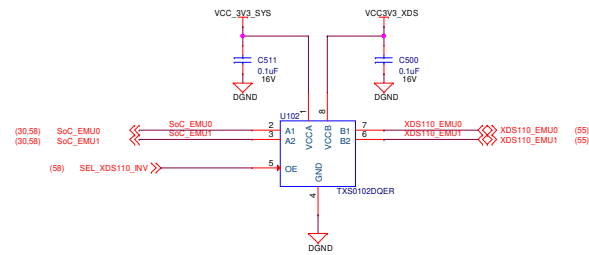
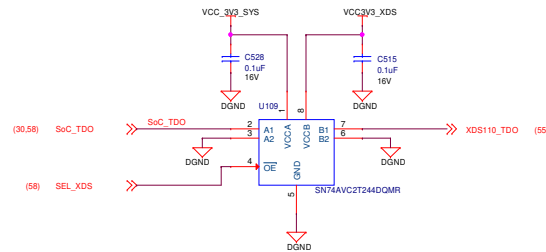
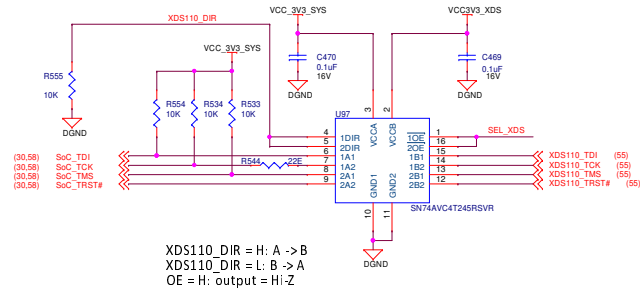
Title FT4232 UART BUFFERS

Size	Rev
C	E2
Date: Friday, November 29, 2024	Sheet 54 of 59

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SOC_GPIO0_60 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPI01	Used to Generate the interrupt on SOC_GPI0_60 Pin	OUTPUT	External Pullup
TEST_GPI02	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPI03	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPI04	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

XDS110 JTAG BUFFER



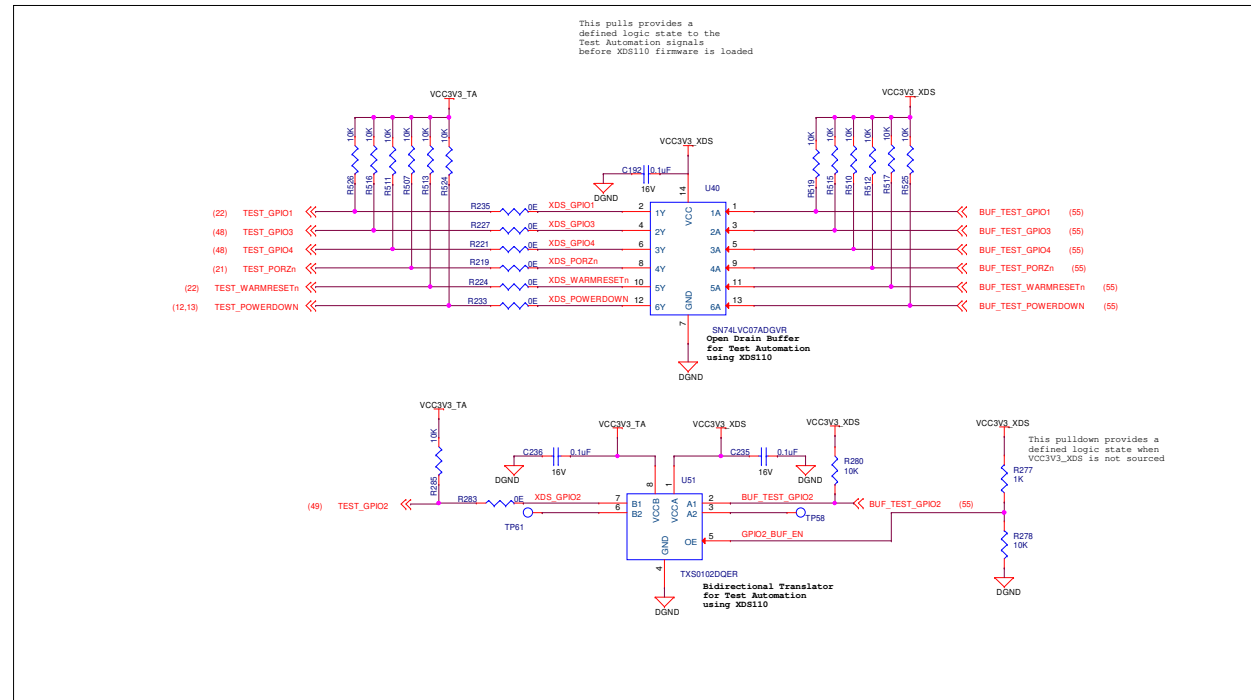
Designed for TI by Mistral Solutions Pvt Ltd



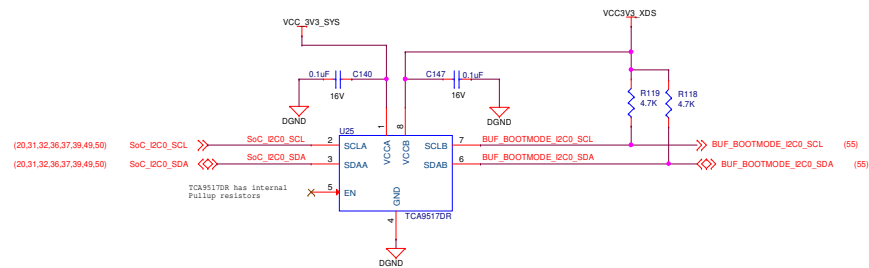
Title XDS110 JTAG BUFFER

Size	Rev
C	PROC180E2
Date:	Friday, November 29, 2024
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XDS110 TEST AUTOMATION BUFFERS



SOC I2C BUS BUFFER



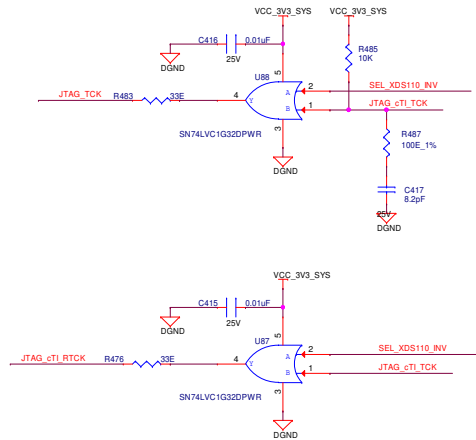
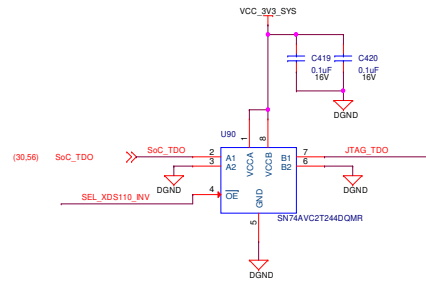
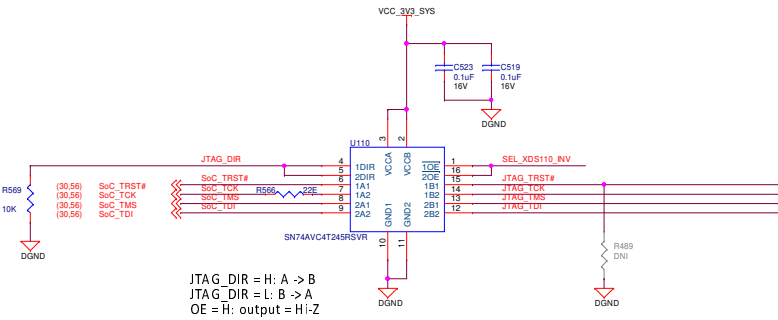
Designed for TI by Mistral Solutions Pvt Ltd



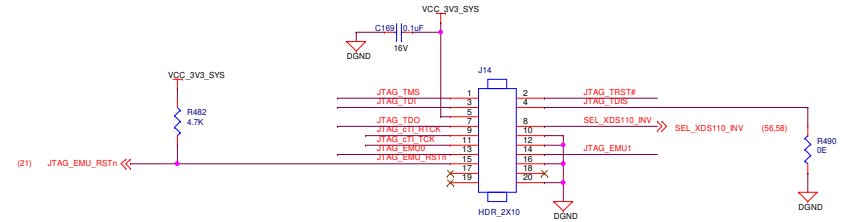
Title XDS110 TEST AUTOMATION BUFFERS

Size	Rev
C	PROC180E2
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JTAG2 BUFFERS

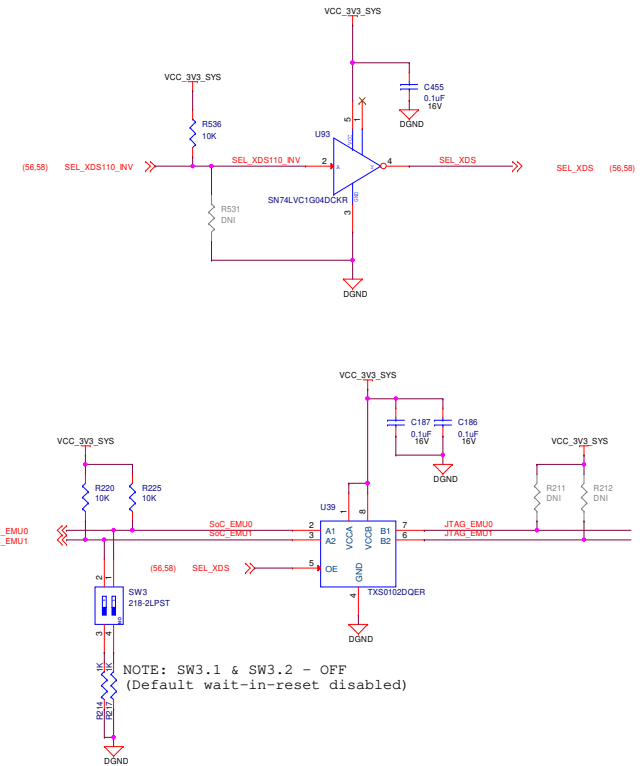


cTI20 JTAG CONNECTOR



Silk: cTI

Add an external ESD protection to provide system level ESD protection



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Title JTAG 20 PIN cTI CONNECTOR

Size	Rev
C	PROC180E2
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MOUNTING HARDWARE

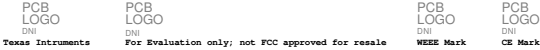
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB



LOGOs



AM62D SOCKET

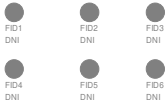


JUMPERS



Socket PART number need to be updated

FIDUCIALS



LABELS

Board Serial No.



EVM Orderable No.



Assembly Revision



Orderable Part Numbers

Variant	Label Text
001	AUDIO-AM62D-EVM

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Title MOUNTING HARDWARE

Size	Rev
C	E2
Date:	Friday, November 29, 2024

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