

Boundary scan (BSCAN), is a common method for testing interconnects (wire lines) on printed circuit boards (PCBs) or sub-blocks inside an integrated circuit. It is widely used as a debugging method to watch integrated circuit pin states, measure voltage, or analyze sub-blocks inside an integrated circuit. Boundary Scan register (BSR), as the name suggests is the main register specifically added at the boundary of the device, between its functional core and the pins by which it is connected to a board.

This readme file describes the conditions and files that need to be used to operate boundary scan (BSCAN) on the following 1st generation TI mmWave devices:

- AWR1243
- xWR1443
- xWR1642
- xWR1843
- xWR1843AOP
- xWR2243
- xWR6x43
- xWR6x43AOP
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Hardware and Software Description

Hardware and Software needed

- mmWave Device on custom board or TI EVM
- JTAG Emulator/setup and or customer in-circuit tester (ICT)

Package Contents

The BSDL zip package contains the following files apart from the readMe_BSDL.txt :

1. <device>-preinit-SVF.txt file

Serial Vector Format (SVF) is the file format for exchanging descriptions of high-level IEEE 1149.1 bus operations. The standard consists of scan operations and movements between different stable states on the IEEE 1149.1 state diagram.

This SVF file provided by TI runs through a series of register initializations to set the device into BSCAN mode (i.e. enables visibility of the 12-bit Instruction Register which supports the BSCAN operation).

Most ICT software suites will accept SVF or use translation tools to import this format. SVF specification is available at the following location - <http://www.asset-intertech.com/eresources/svf-serial-vector-format-specification-jtag-boundary-scan>

2. <device>.bsdl file

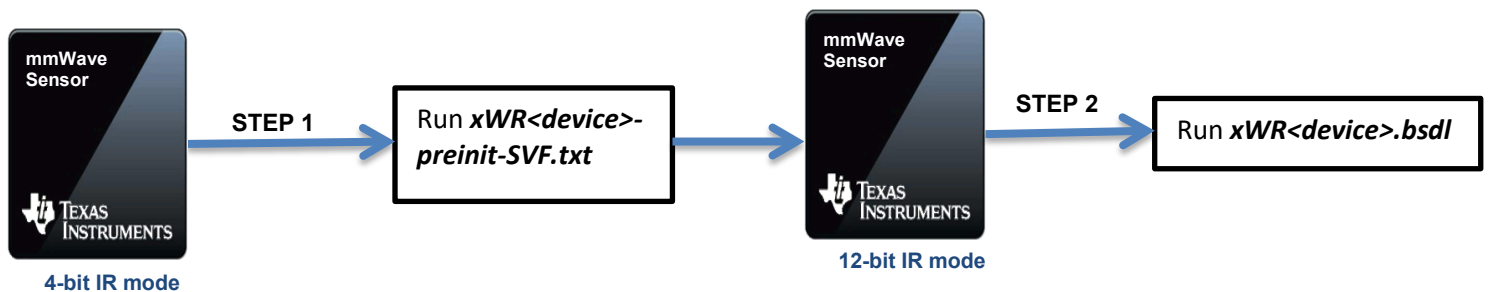
The BSDL file describes the device's BSCAN configuration i.e. Test Access port and boundary register descriptions. It is used to define the data transport characteristics of the device, i.e. how it captures, shifts, and updates scanned data which is further used in defining the test capability.

Modes

There are essentially two working states for the TI GEN1 mmWave device Test Access Port (TAP) configuration:

1. **4-bit Instruction Register (IR) mode:** This is the working state of the device after reset and as such no BSCAN is available in this state.
 - a. In this state, the Data Register (DR) is of length 1, and hence the device is in BYPASS mode.
 - b. Working instructions in this mode: IDCODE/BYPASS
2. **12-bit Instruction Register (IR) mode:** This is the working state where BSCAN capability is available in the device.
 - a. It is achieved after the running the *<device>-preinit-SVF.txt* file
 - b. Working instructions in this mode: SAMPLE/PRELOAD/EXTEST

Sequence of operations



The figure represents the sequence of operations to be followed to use the files present in TI BSDL package file.

- **STEP 1:** In order to proceed with any BSCAN testing, the user is required to run the *xWR<device>-preinit-SVF.txt* to move to 12-Bit IR mode i.e. the BSCAN mode. This script does an IDCODE check and then sets up the device to expose the 12bit IR, multi-bit DR registers which matches the description in the BSDL file.
- **STEP 2:** After successful execution of the above step, the user can now use the *xWR<device>.bsdl* file for their BSCAN testing.

Limitations

Normally ICT programs perform an infrastructure check, which may or may not include some or all of the below tests. Accordingly, manufacturers of ICT software will have a method of removing these checks from their standard infrastructure setup, if not known already.

Due to the BSCAN implementation on the 1st generation TI mmWave devices, there are some JTAG BSR functions that are not implemented via the BSDL file:

- **IDCODE:** This instruction will not work after the SVF pre-init i.e. after STEP 1 in the above sequence. We recommend using *IDCODE read* for identification purposes in the

SVF as included. Before STEP 1, an IDCODE read shall be done on the device (in 4-bit IR mode). A successful execution of the SVF file will also mean successful device identification. If the instruction does not pass, then the SVF execution should flag an error state.

- **BYPASS:** There is no BYPASS instruction available after the STEP 1 execution i.e. SVF pre-init. Any BYPASS operations should be completed just after the device has been reset.
- **INSTRUCTION_CAPTURE:** There is no guaranteed bit pattern available from the IR-capture state. However, this statement is still included in the BSDL file for reference with wild-card as the expected value. According to JTAG specification, the lsb's of the IR-capture state output should be b01, but for the afore-mentioned devices, this is not guaranteed. Hence, it is recommended to bypass this check.
- **IR length check:** Although, the IR will decode and operate as a 12bit register (after SVF execution), reading the length of the IR will not result in length = 12 due to some additional logic in the path. Hence, this check should be avoided and removed from the Infrastructure test.