

QUAD-PORT ETHERNET EXPANSION BOARD

TABLE OF CONTENTS

PAGE	CONTENTS
01	TABLE OF CONTENTS
02	REVISION HISTORY
03	BLOCK DIAGRAM
04	QSGMII_PHY & EXP_CONN
05	RJ45_CONNECTORS
06	QSGMII_POWER & EEPROM
07	QSGMII_CLOCK_GENERATOR
08	HARDWARE SCHEMATICS

REV	E2
VER	1.3

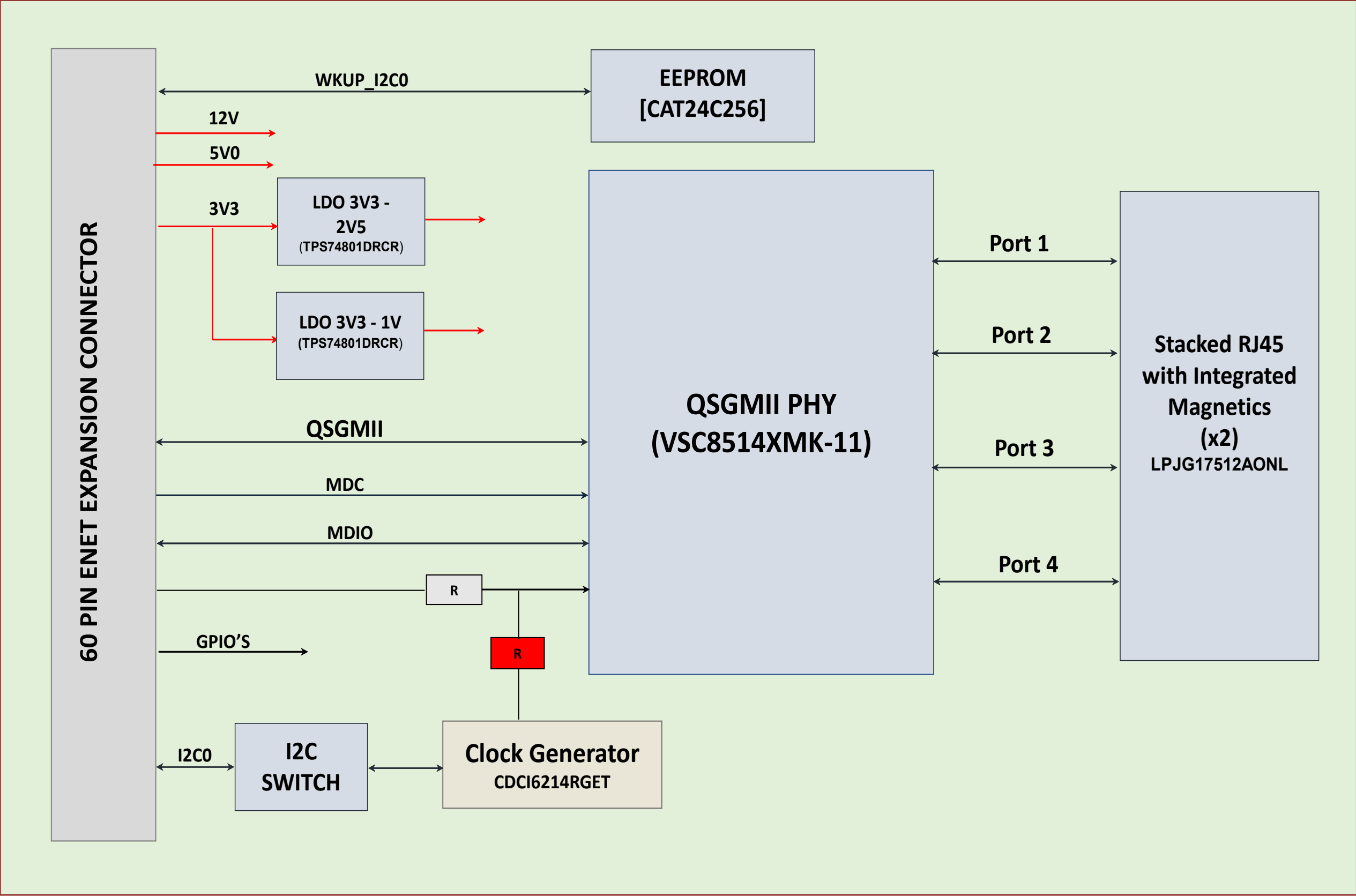
Preliminary

REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	29 JAN 2019	Drafted from "PROC080E1_SCH., VER:2.0" Updated Expansion connector (J3) pinout as recommended in datasheet	Mistral Design Team		
0.2	05 MAR 2019	Updated Expansion connector (J3) Part# to 171450-5106	Mistral Design Team		
0.3	06 MAR 2019	Added the LED Mosfet Drivers for RJ45 LEDs (Q1-Q8) PU Resistor R32 from EEPROM_WP DNI'd	Mistral Design Team		
0.4	06 MAR 2019	Replaced the single Mosfet IC with Dual Mosfet Part# BSS138PS	Mistral Design Team	TI	
1.0	15 MAR 2019	Baselined	Mistral Design Team		
1.1	04 APR 2019	Added Hardware schematics Page	Mistral Design Team		
1.2	04 APR 2019	Added Ground Post (Part# 5002) to TP19	Mistral Design Team		
1.3	05 APR 2019	Added Text "Preliminary" to all the Pages Updated Hardware Schematic Page	Mistral Design Team		

Preliminary

BLOCK DIAGRAM



Expansion Connector

Note 2 CLOCK SOURCE SELECTION

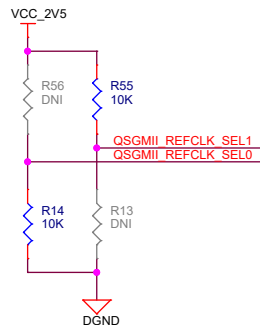
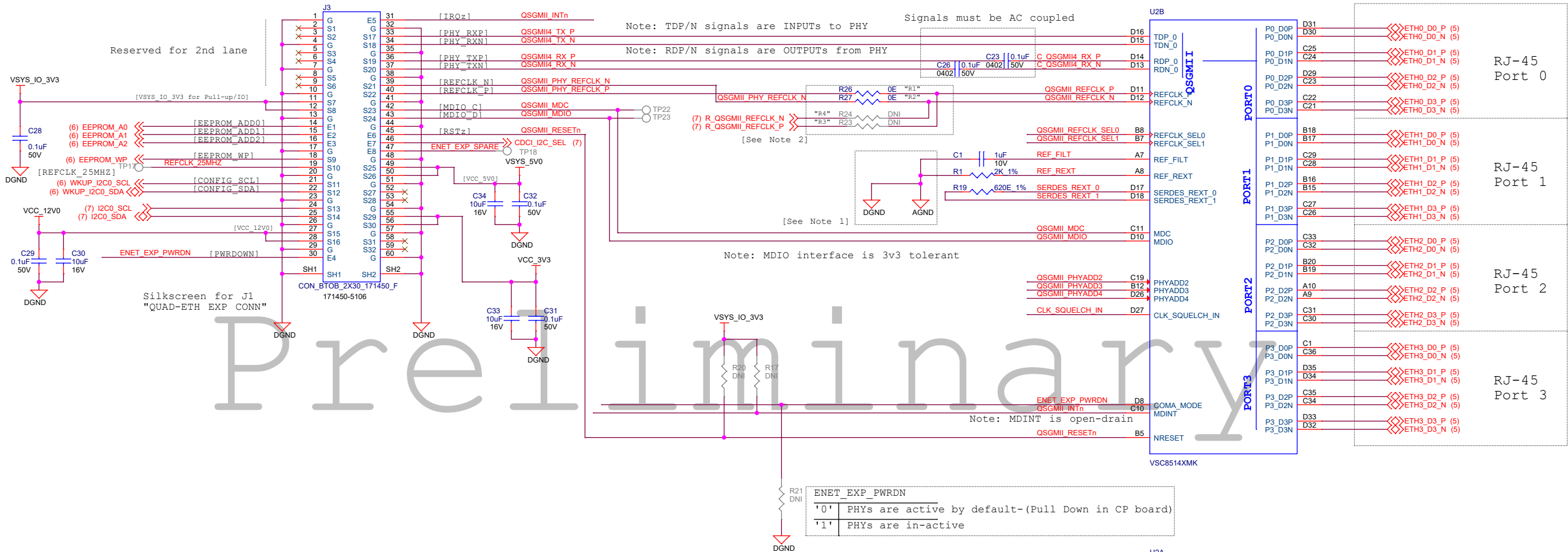
	Install	Remove
From on board Clock Generator	R3,R4	R1,R2
From CP Board	R1,R2	R3,R4

```
(default)
```

PCB Note: Place C23 and C26 near to IC pins

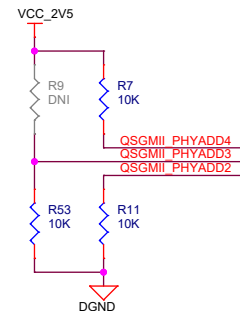
QSGMII PHY

Signals must be AC coupled



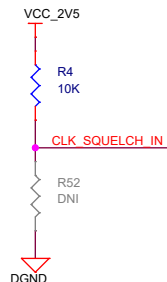
Reference Clock Selection

REFCLK_SEL1	REFCLK_SEL0	Frequency
0	0	125MHz
1	0	156.25MHz (default)



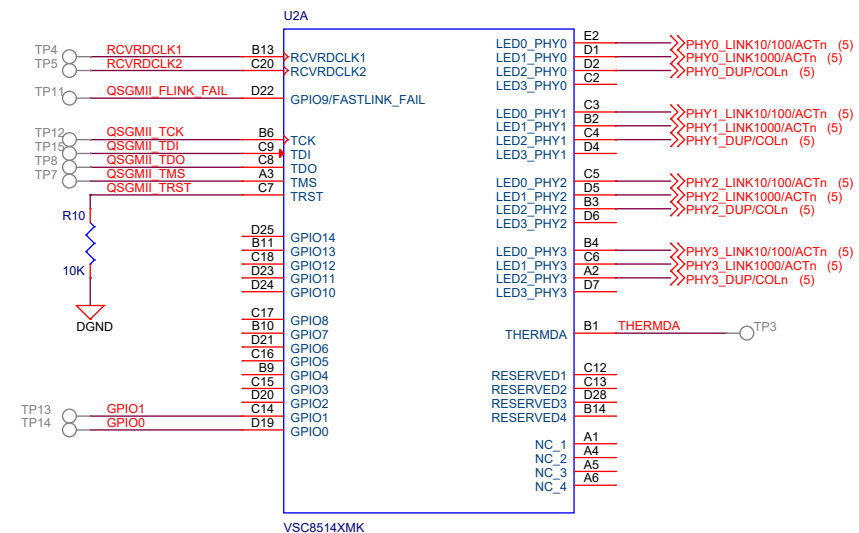
PHY Address Selection

PHY	Address	
PHY0	10000	0x10
PHY1	10001	0x11
PHY2	10010	0x12
PHY3	10011	0x13



Squelch Selection

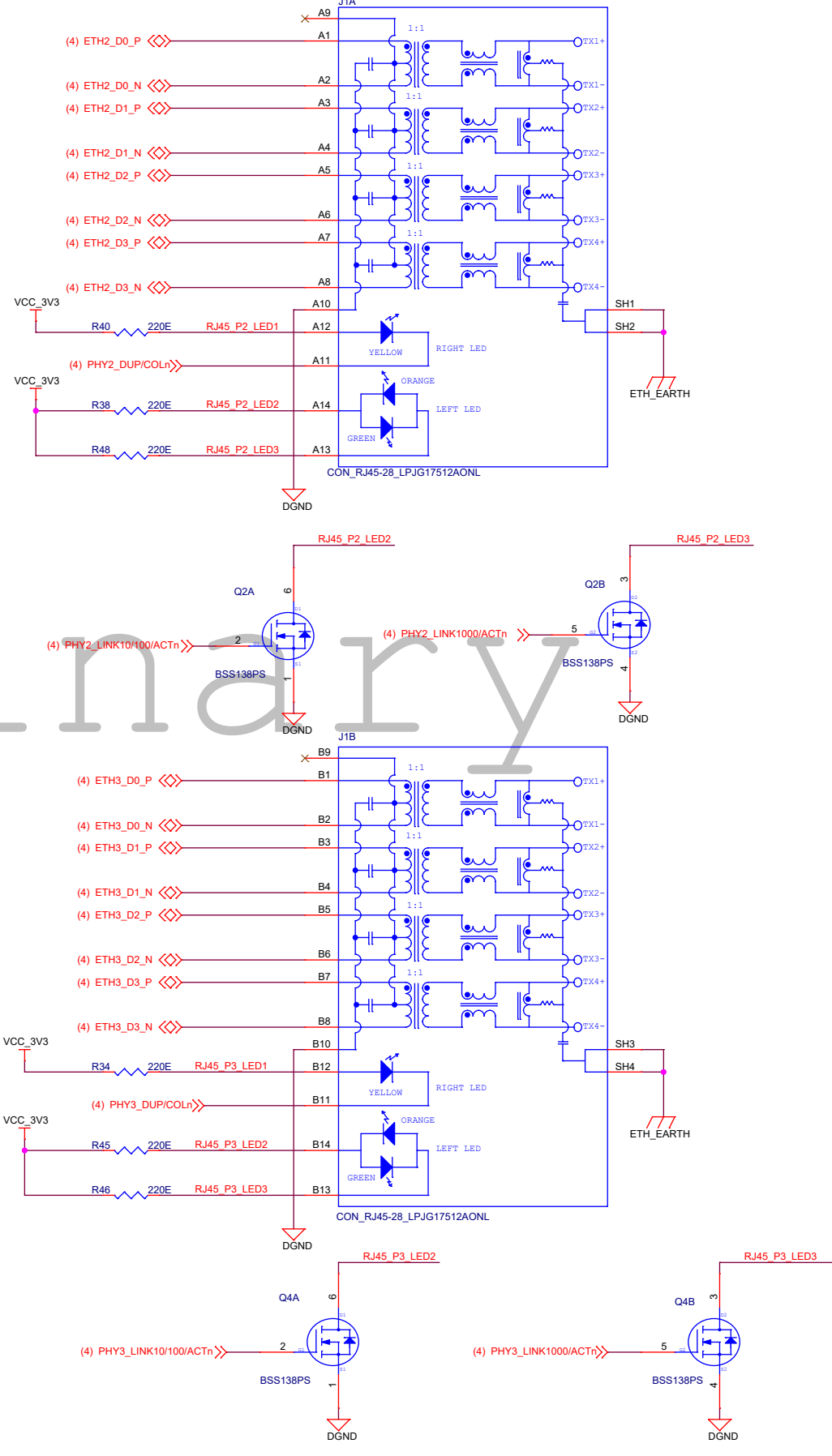
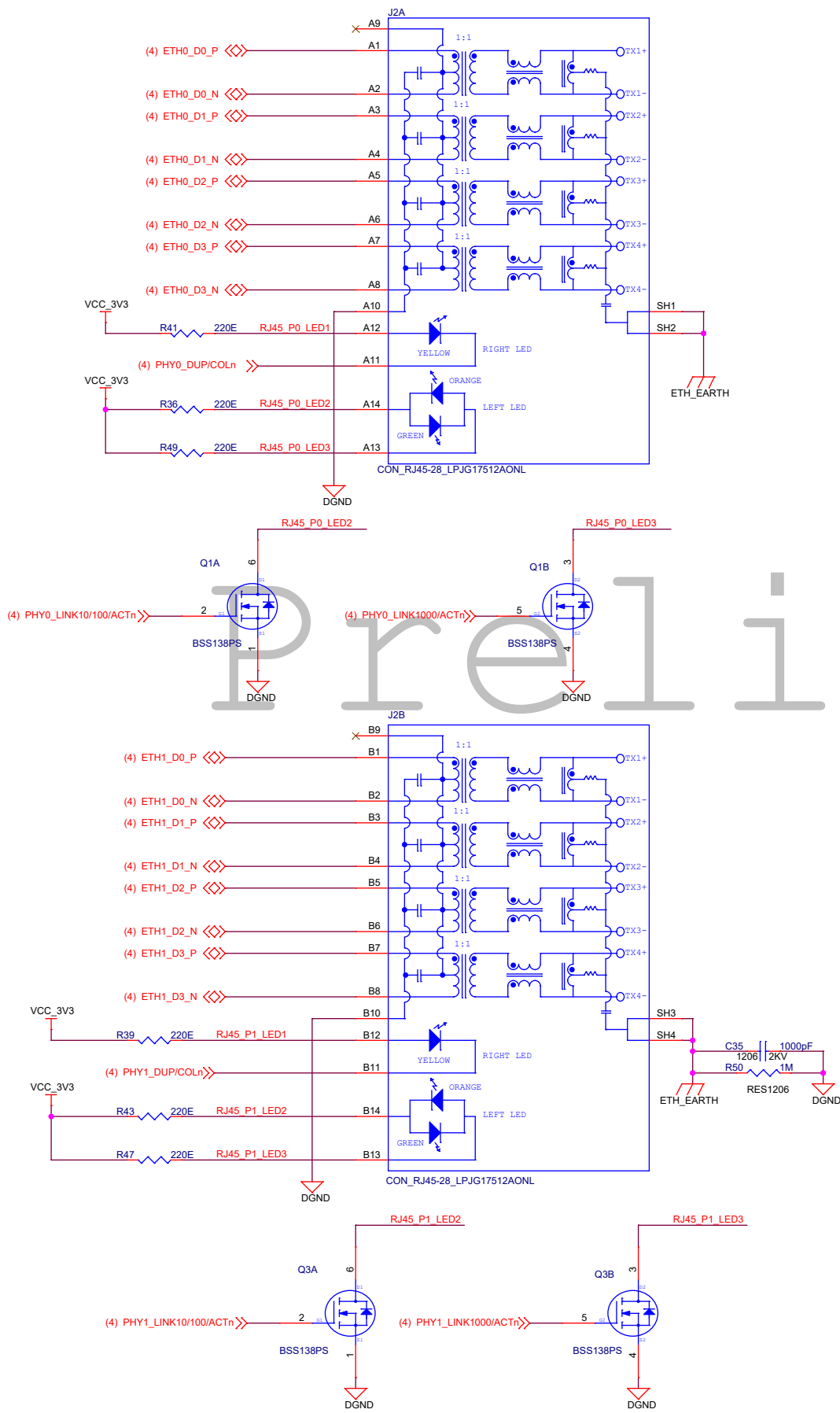
	CLK_SQUELCH
0	RCVRD Clock Output
1	No RCVRD Clock (default)



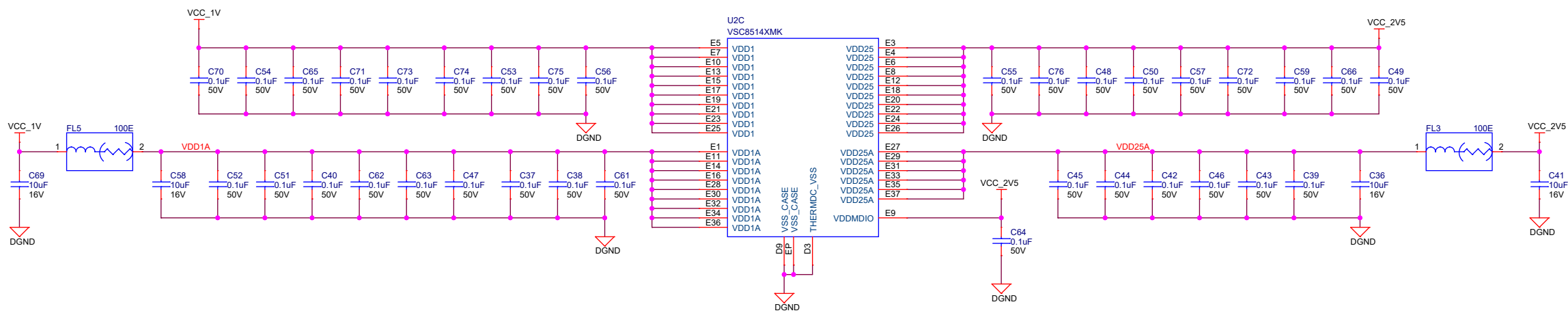
Notes:

NOTE1: The ground connections of the resistor and the capacitor should each be connected to a shared PCB signal trace. (rather than being connected individually to a common ground plane). This PCB signal trace should then be connected to a ground plane at a single point.

RJ45 Connectors



QSGMII PHY POWER

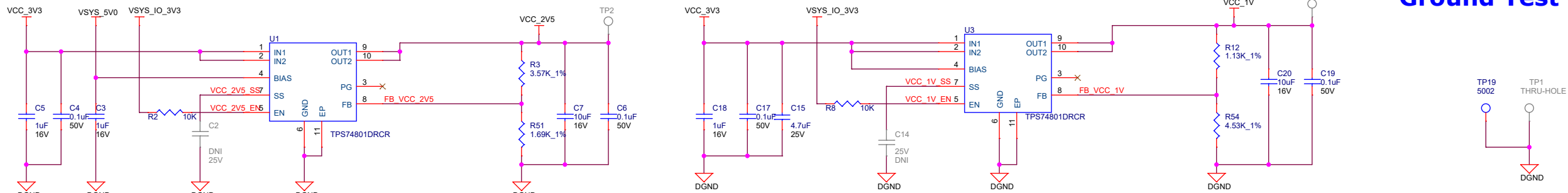


Preliminary

3.3V to 2.5V

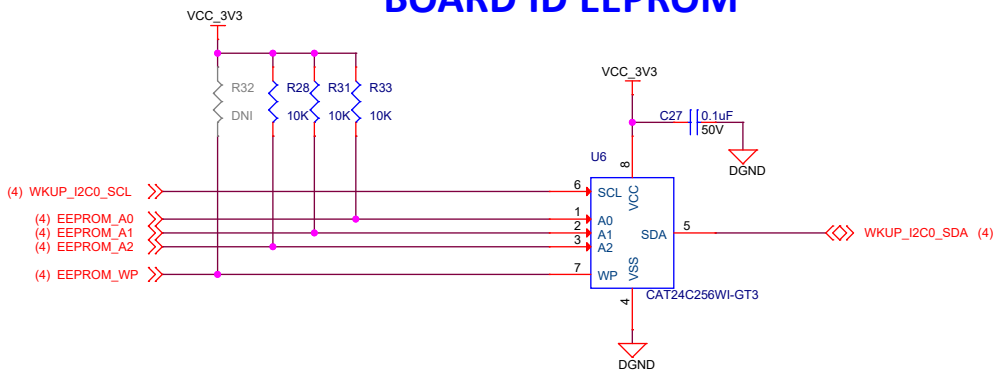
3.3V to 1V

Ground Test Points



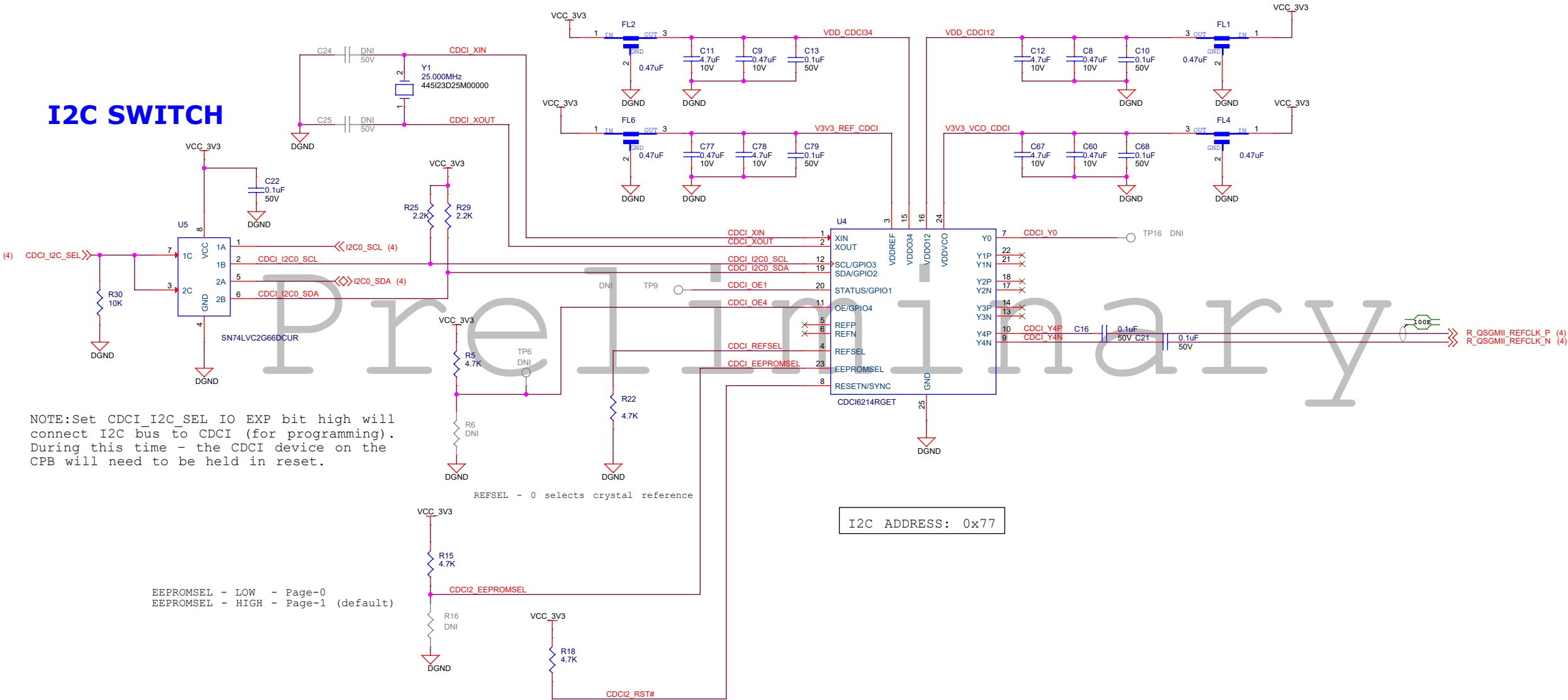
PCB NOTE:Keep 4.7uF capacitor close to BIAS pin.

BOARD ID EEPROM



QSGMII CLOCK GENERATOR

I2C SWITCH



NOTE:Set CDCI_I2C_SEL IO EXP bit high will connect I2C bus to CDCI (for programming). During this time - the CDCI device on the CPB will need to be held in reset.

EEPROMSEL - LOW - Page-0
EEPROMSEL - HIGH - Page-1 (default)

REFSEL - 0 selects crystal reference

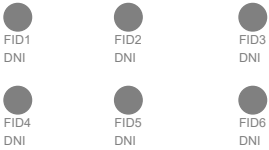
I2C ADDRESS: 0x77

HARDWARE SCHEMATICS

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

FIDUCIALS



Refer CP Board (J721EXCP01EVM) for Mechanical Parts

Preliminary

LABELS

Board Serial No.



EVM Orderable No.



BARE PCB



LOGOs

