

# J7VCL SOM - TPS65941x + LP8764x PMICs

## TABLE OF CONTENTS

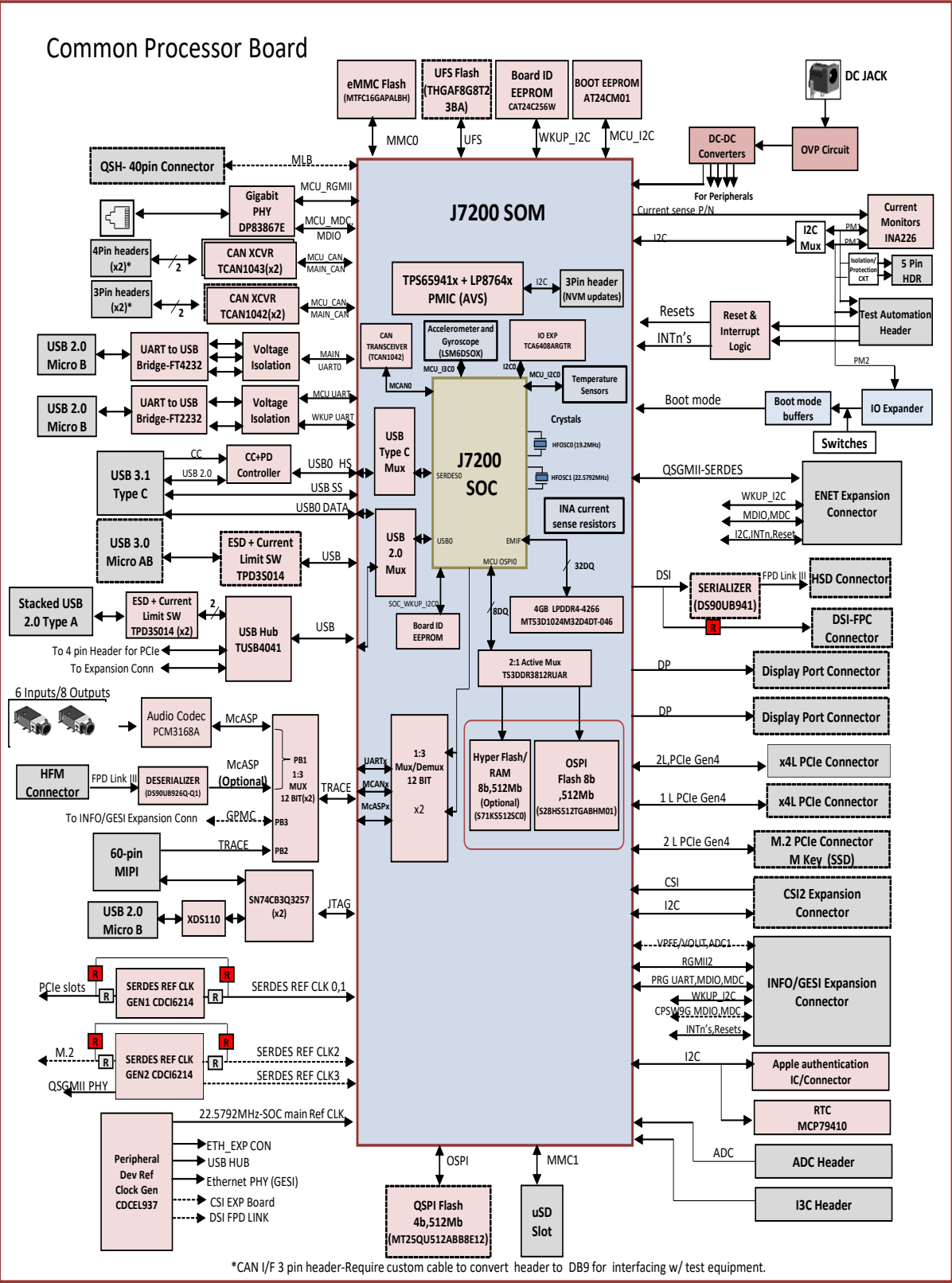
PAGE	CONTENTS
01	TABLE OF CONTENTS
02	REVISION HISTORY
03	SoM: SYSTEM BLOCK DIAGRAM
04	SoM: Dual TPS65941x-Q1 POWER FLOW DIAGRAM
05	SoM: I2C Tree Diagram
06	SoM: I2C Address Table
07	SoC: GPIO MAPPING TABLE
08	SoC: Reserved
09	SoC: SERDES INTERFACES
10	SoC: MMC INTERFACES
11	SoC: EMIF & LPDDR4
12	SoC: MCU FLASH
13	FLASH: OSPI-FLASH, HYPER-FLASH & RAM
14	SOC: MCU & MAIN GENERAL IO, OSC CLKS
15	SOC: GENERAL & USB
16	SOC: MCU_RGMII, MCU_ADC & MCU_I3C
17	SOC: CANUART Interfaces
18	SOC: ANALOG POWER 1
19	SOC: DIGITAL POWER 2
20	SOC: DIGITAL POWER 3
21	SOC: GROUND
22	SOM: PMIC A
23	SOM: PMIC B
24	SOM: LOAD SWITCHES
25	SOM: SOM to COMM PROC SERDES CONNECTORS
26	SOM: SOM to COMM PROC PRIMARY CONN #1
27	SOM: SOM to COMM PROC PRIMARY CONN #2
28	EVM: BOARD ID EEPROM & TEMP SENSORS
29	EVM: SOC CURRENT SENSE RESISTORS
30	EVM: PERIPHERAL CURRENT SENSE RESISTORS

PAGE	CONTENTS
31	EVM: CAN TRANSCEIVER
32	EVM: ALTERNATE LPDDR4x POWER RESOURCE OPTION
33	EVM: NOTES, HARDWARE & LABELS
34	EVM: SI_SIM_COUPON BD

REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E7A	20 JUL 2021	Drafted from PROC105E7 DNI'd components for Kelvin measurement	Mistral Design Team		
E8	04 NOV 2021	Changed C201 and C264 to 22uF Mfr. Part GCM21BD70J226ME36L Added resistor R646 to support Hera PMIC 2.0 change Added two 0.1uF capacitors C631 and C632 to VDDA_0P8_SERDES supply Added one 0.1uF capacitor C633 to VDDA_1P8_USB supply Added one 0.1uF capacitor C634 to VDDA_1P8_SERDES0 supply	Mistral Design Team		
	16 DEC 2021	Updated PMIC part numbers	Mistral Design Team		
	18 FEB 2022	Changed PMIC part numbers Changed C37,C38, C39 and C40 to NON-DNI	Mistral Design Team		

SYSTEM BLOCK DIAGRAM



**Recommended for Superset Use Case max power**

v0.01      05/06/2020      Initial PDN.

### Features Supported:

6. Improved USB 2.0 data eye performance
7. Octal SPI Flash memory
8. eMMC Flash memory
9. Hyper Flash & RAM memory
10. I2C EEPROM memory
11. Efuse on-board programming



## J7 EVM



Title

TPS65941+ LP8764x-Q1 POWER FLOW DIAGRAM

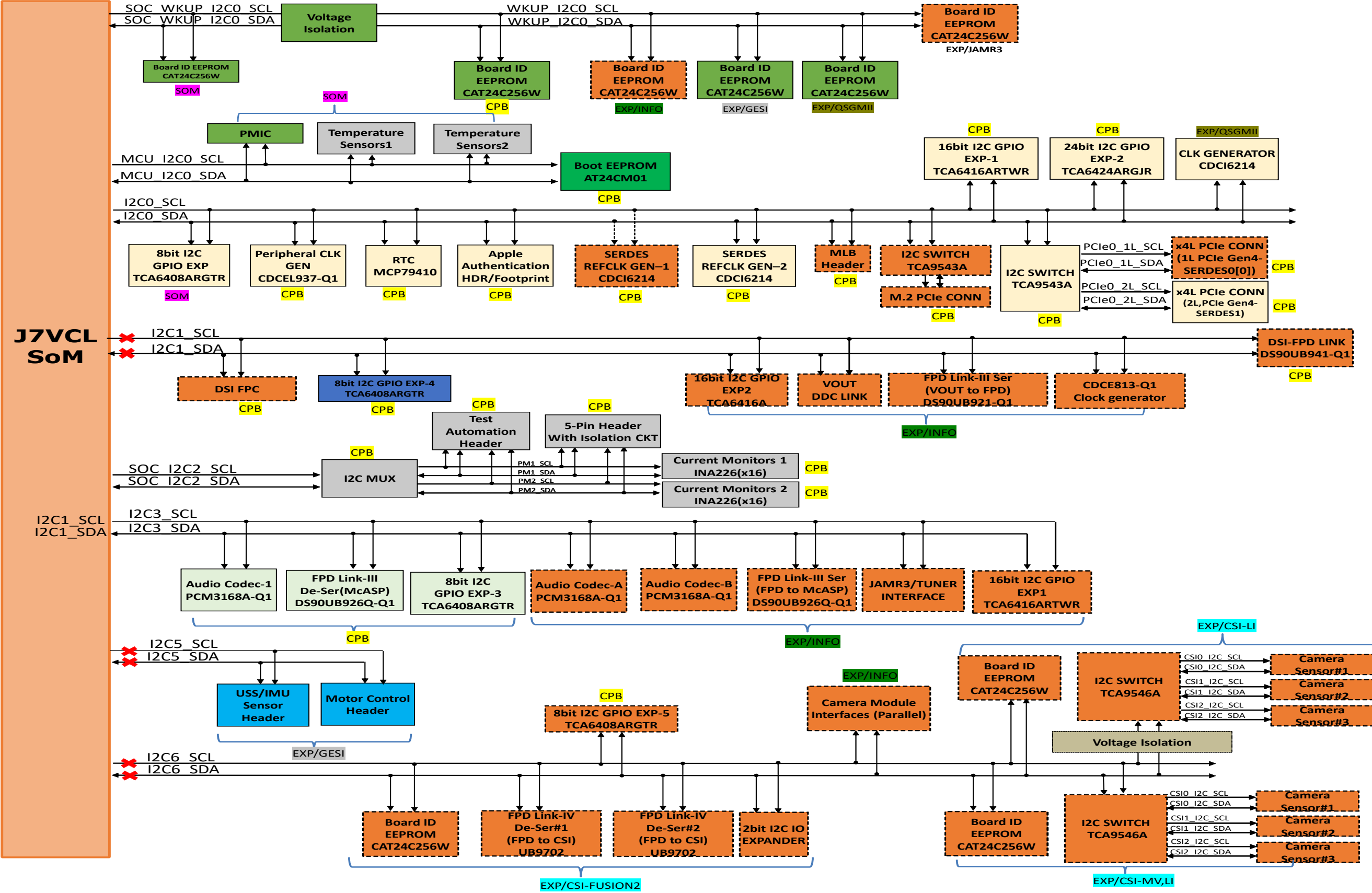
Size	PROC105 001 J7200XSOMG01EVM
------	-----------------------------

C	
---	--


--	--

Sheet 4 of 34

SoM I2C TREE DIAGRAM






SoM I2C ADDRESS TABLE

J7200 SoM I2C mapping						
SL NO.	Board	Interface name	Part#	Address	J721E/CPB Port mapping	J7200 Port mapping
1	EVM/SoM	Board ID EEPROM	CAV24C256WE-GT3	0x50	WKUP_I2C0	WKUP_I2C0
2	EVM/CPB	Board ID EEPROM	CAT24C256W	0x51		
3	EXP/GESI	Board ID EEPROM	CAT24C256W	0x52		
4	EXP/QSGMII	Board ID EEPROM	CAT24C256W	0x54		
5	EVM/SoM	PMICs	PMIC A: TPS659414F3 PMIC B: LP8764-Q1	PMIC A: 0x48 to 4B PMIC B: 0x4C to 4F	MCU_I2C0	MCU_I2C0
6	EVM/SoM	Temperature Sensors	TMP100NA/3K	0x48, 0x49		
7	EVM/CPB	Boot EEPROM	AT24CM01	0x50, 0x51	Main I2C0	Main I2C0
8	EVM/SoM	8-bit I2C GPIO Expander	TCA6408ARGTR	0x21		
9	EVM/CPB	SerDes Clock gen #2	CDCI6214	0x77,0x76		
10	EVM/CPB	Peripheral Clock Gen	CDCEL937-Q1	0x6D		
11	EVM/CPB	16bit I2C GPIO EXPANDER1	TCA6416ARTWR	0x20		
12	EVM/CPB	24bit I2C GPIO EXPANDER2	TCA6424ARGJR	0x22		
13	EVM/CPB	Apple Authentication Header	2214BR-10G	0x10, 0x11		
14	EVM/CPB	RTC 7'b	MCP79410	0x57, 0x6F		
15	EVM/CPB	I2C MUX for both x2LANE and x1LANE PCIe Interface	TCA9543APWR	0x70		
16	EXP/QSGMII	QSGMII PHY Ref Clock Generator (QPENET Board)	CDCI6214	0x77		
17	EVM/CPB	I2C Switch for Automation header	NA	0x22	Main I2C2	Main I2C2
18	EVM/CPB	Current Monitors and Header	NA	0x40 to 0x4F (PM1 and PM2 via I2C Switch)		
19	EVM/CPB	8bit GPIO Expander3	TCA6408ARGTR	0x20	Main I2C3	Main I2C1
20	EVM/CPB	FPD Link iii Deserializer	DS90UB926Q-Q1	0x2C		
21	EVM/CPB	AUDIO IF Codec	PCM3168A-Q1	0x44		

GPIO MAPPING TABLE

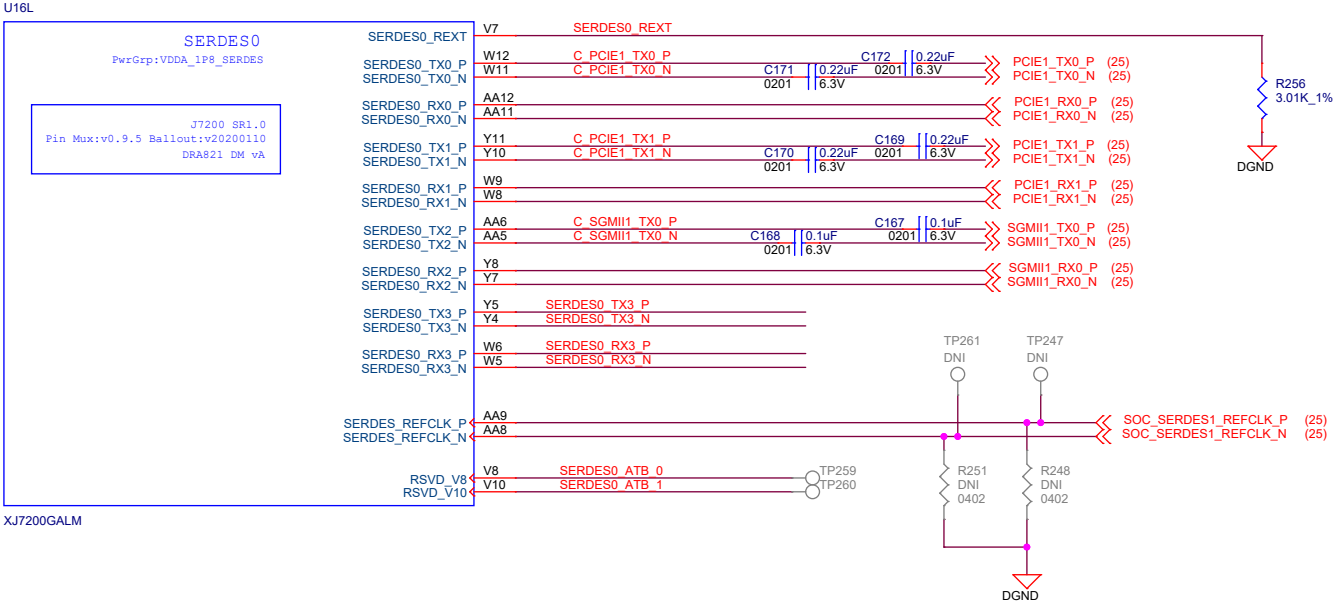
WKUP Domain						
Package Signal Name	GPIO Number	Net name	Input/Output	Default	State	Remarks
WKUP_GPIO0_0	WKUP_GPIO0_0	MCU_MCAN0_EN	Output	BOOTMODE	Active High	MCU CAN0 Enable
WKUP_GPIO0_1	WKUP_GPIO0_1	BOOT_EEPROM_WP	Output	BOOTMODE	Active High	Boot EEPROM Write protect
WKUP_GPIO0_2	WKUP_GPIO0_2	MCU_CAN1_STB	Output	BOOTMODE	Active High	MCU CAN1 Standby
WKUP_GPIO0_3	WKUP_GPIO0_3	GPIO_MCU_RGMII1_RST#	Output	PU	Active low	MCU_RGMII1_Reset
WKUP_GPIO0_6	WKUP_GPIO0_6	OSPI/HYPER_MUX_SEL	Output	DIP_SEL	NA	Flash Memory Selection ('0' - OSPI0, '1' - Hyperflash + HyperRam)
WKUP_GPIO0_7	WKUP_GPIO0_7	SYS_IRQz	Input	PU	Active low	Push-button Interrupt, User Defined/Wake S2R ('0>1' - interrupt pending, '1' - normal operation)
MCU_OSPI0_LBCLKO	WKUP_GPIO0_17	MCU_OSPI0_ECC_FAIL	Output	NA	Active High	OSPI_ECC_FAIL (Mux option w/ HYPERBUS_CKn), MCU_OSPI0_ECC_FAIL is DNI resistor option.
MCU_SPIO_CLK	WKUP_GPIO0_56	PROFI_UART_SEL	Output	BOOTMODE	Active High	Signal Mux Control ('0' - Profibus, '1' - BP/MC UART)
MCU_SPIO_D0	WKUP_GPIO0_57	SYS_MCU_PWRDN	Output	BOOTMODE	Active low	System Power Down ('0' - normal operation, '1' - system power down)
MCU_SPIO_D1	WKUP_GPIO0_58	MCU_CAN0_STBz	Output	BOOTMODE	Active low	MCU CAN0 Standby
MCU_SPIO_CS0	WKUP_GPIO0_59	MCU_RGMII1_INT#	Input	PU	Active Low	MCU Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
WKUP_GPIO0_77	WKUP_GPIO0_77	LEOB_GPIO7	Output	BOOTMODE	NA	Spare GPIO of PMIC. Function TBD
WKUP_GPIO0_78	WKUP_GPIO0_78	H_MAIN_GPIO_A	Output	BOOTMODE	NA	GPIO10 of PMIC B. Function TBD
WKUP_GPIO0_80	WKUP_GPIO0_80	LSM6DSOX_INT	Output	BOOTMODE	NA	Interrupt from I3C Gyroscope sensor
WKUP_GPIO0_84	WKUP_GPIO0_84	H_MCU_INT#	Input	PU	Active low	Interrupt from PMIC
Main Domain						
EXTINTn	GPIO0_0	SOC_EXTINTN	Input	PU	Active low	Push-button Interrupt, User Defined
MCAN1_RX	GPIO0_12	CANIO_RET_WAKE	Input	PU	NA	Push-button wake signal,
MCAN9_RX	GPIO0_28	GPIO_RGMII2_RST	I/O	NA	NA	Routed to INFO/GESI expansion connector. GESI - Used for GPIO_PRG0_RGMII_RST; INFO - Not used
MCAN7_RX	GPIO0_24	C_MCASPO_AFSR	NA	PU	Active low	I2C0 IO expander interrupt. ('0' - interrupt pending, '1' - no interrupt) (I2C0_IOEXP_INT#) Note: GPIO only available from Trace/GPMC Mux
SPIO_D1	GPIO0_55	SEL_SDIO_3V3_1V8n	Output	NA	Active low	SW controls & transition SD card to high speed 1.8V signalling if card type supports
GPMC0_CLK	GPIO0_44	PM_I2C_SEL	Output	PD	NA	CP Board - PM I2C Mux selection. ('0' - SOC_I2C2_SCL/SDA -> PM1_SCL/SDA, '1' - SOC_I2C2_SCL/SDA -> PM2_SCL/SDA) GESI - Boosterpack_GPIO1
RMII1_CRS_DV	GPIO0_4	ENET_EXP_INTB	Input	PU	Active low	Ethernet Expansion Interrupt. ('0' - interrupt pending, '1' - no interrupt)
MCAN9_TX	GPIO0_27	GPIO_RGMII2_INT#	Input	PU	Active low	Interrupt function. ('0' - interrupt pending, '1' - no interrupt) GESI - Used for PRG0_RGMII_INT#; INFO - AUDEXP_INTB

RESERVED

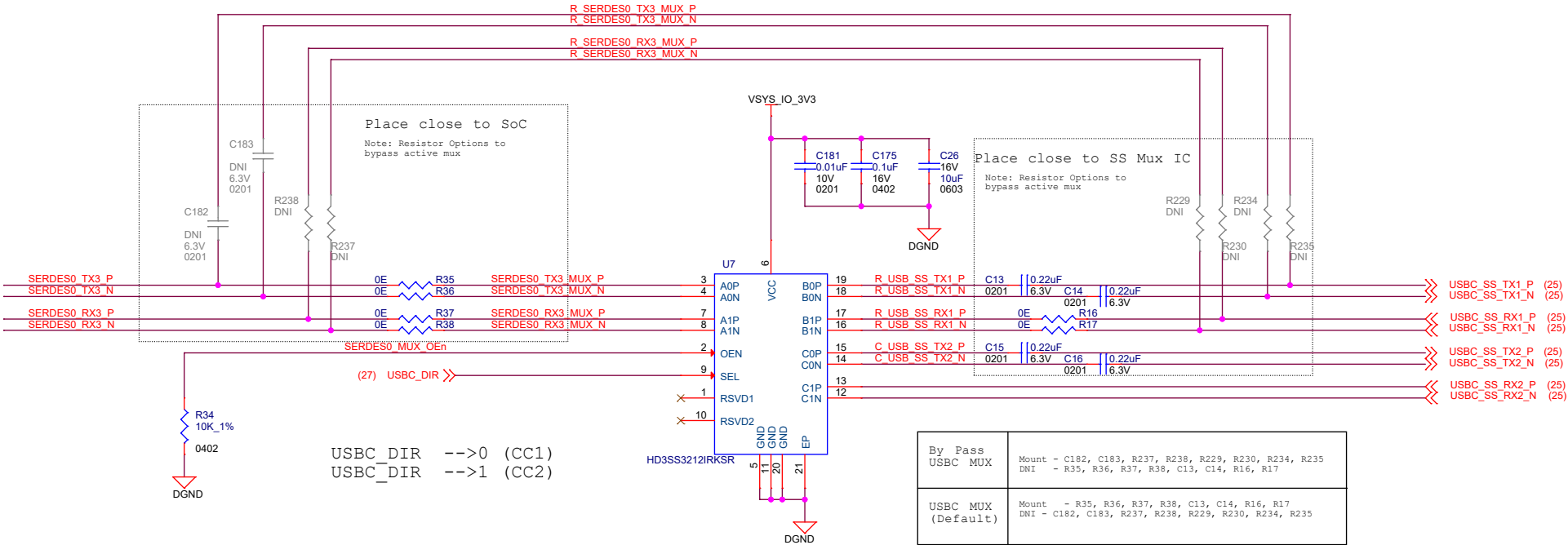
Project :  J7 EVM		Title MLB,CSI&DSI_INTERFACE			
		Size	PROC105 001 J7200XSOMG01EVM	Rev	
		C		E8	
		Date: Thursday, December 16, 2021		Sheet	8



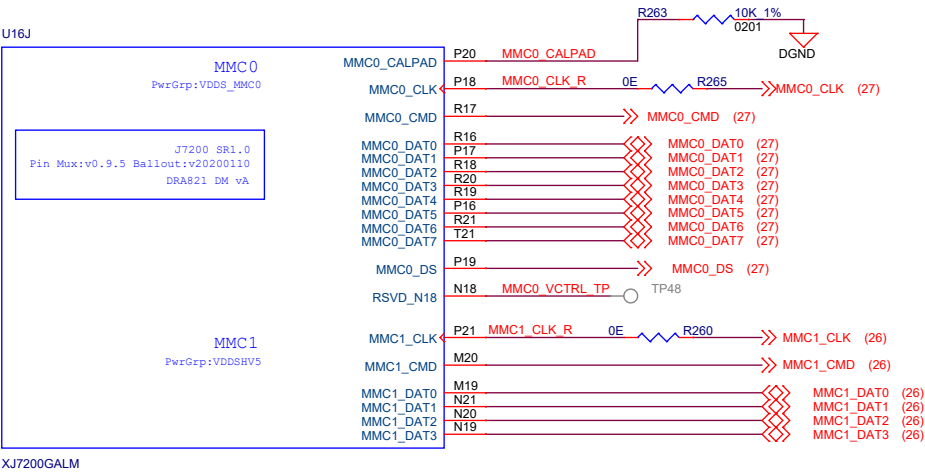
SERDES



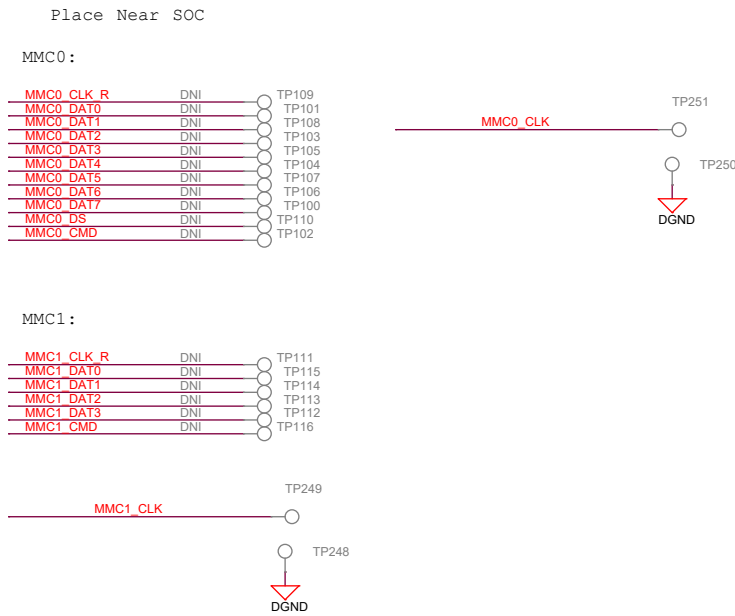
USB Type C MUX

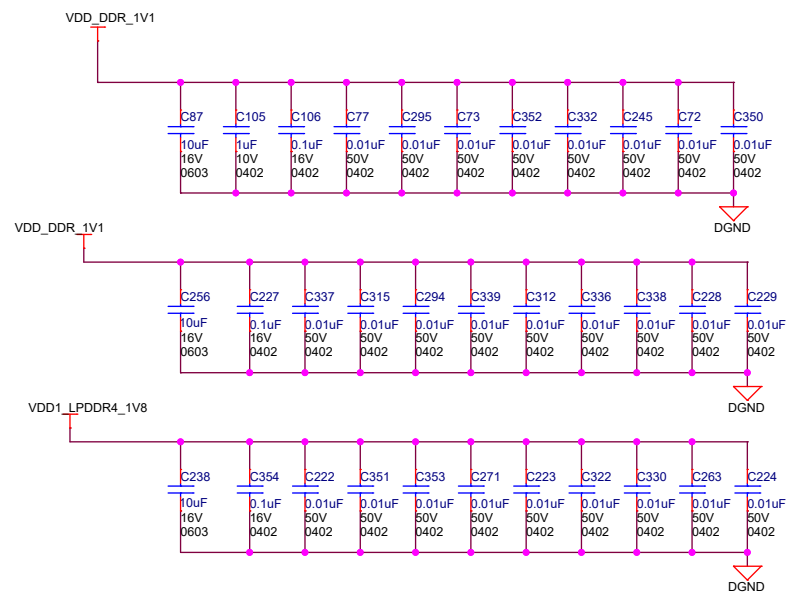



# MMC Interface



## Via Probe Test Points



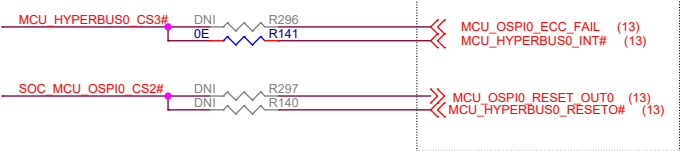
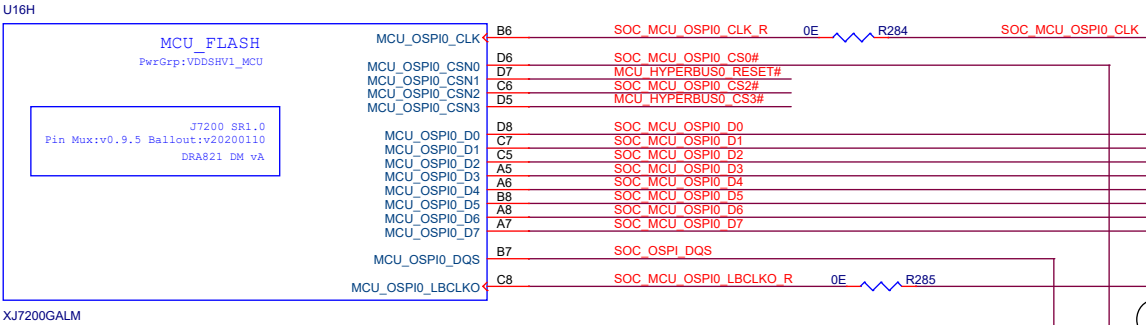


Project :  J7 EVM		Title LPDDR4		
		Size C	PROC105 001 J7200XSOMG01EVM	Rev E8
		Date: Thursday, December 16, 2021		
		Sheet 11 of 34		

EVM development & evaluation test circuitry  
(TI EVM Only)

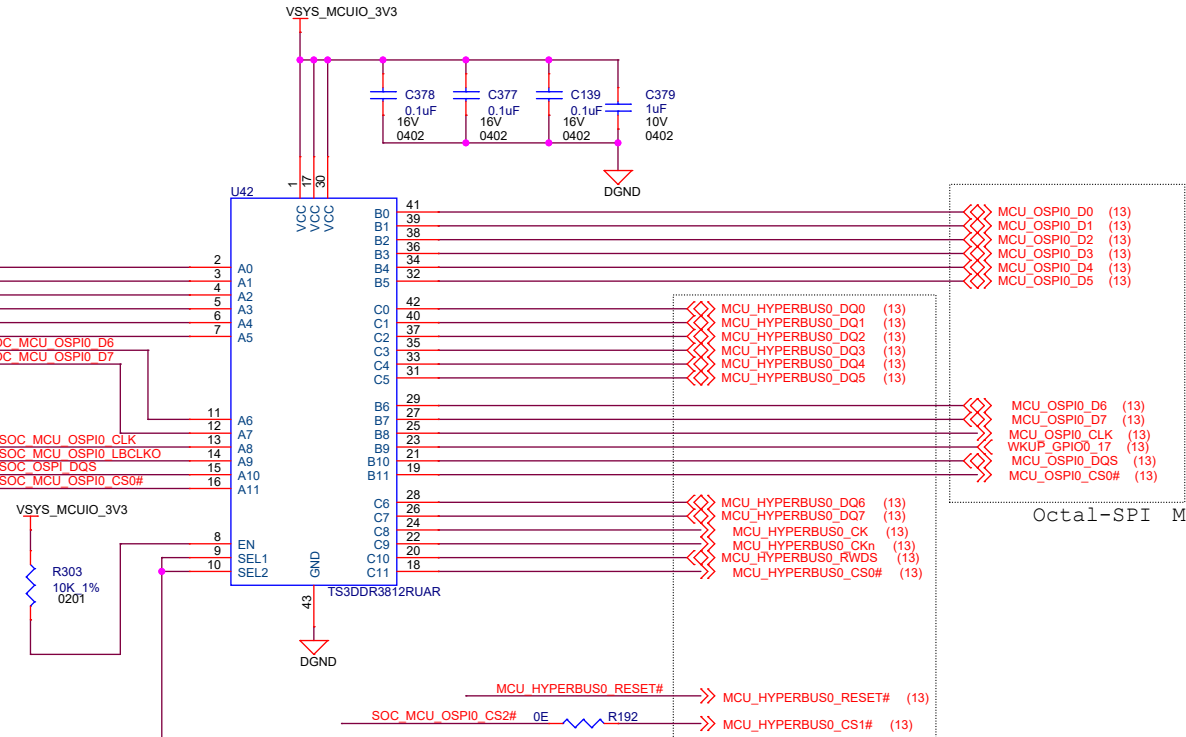
2:1 Mux for OSPI/HYBERBUS

MCU FLASH



Note: Optional OSPI/Hyperbus Signals

Route SOC\_MCU\_OSPI0\_CLK & SOC\_MCU\_OSPI0\_LBCLKO as differential pair



Octal-SPI Memory Interface

Hyperflash + HyperRAM Memory Interface

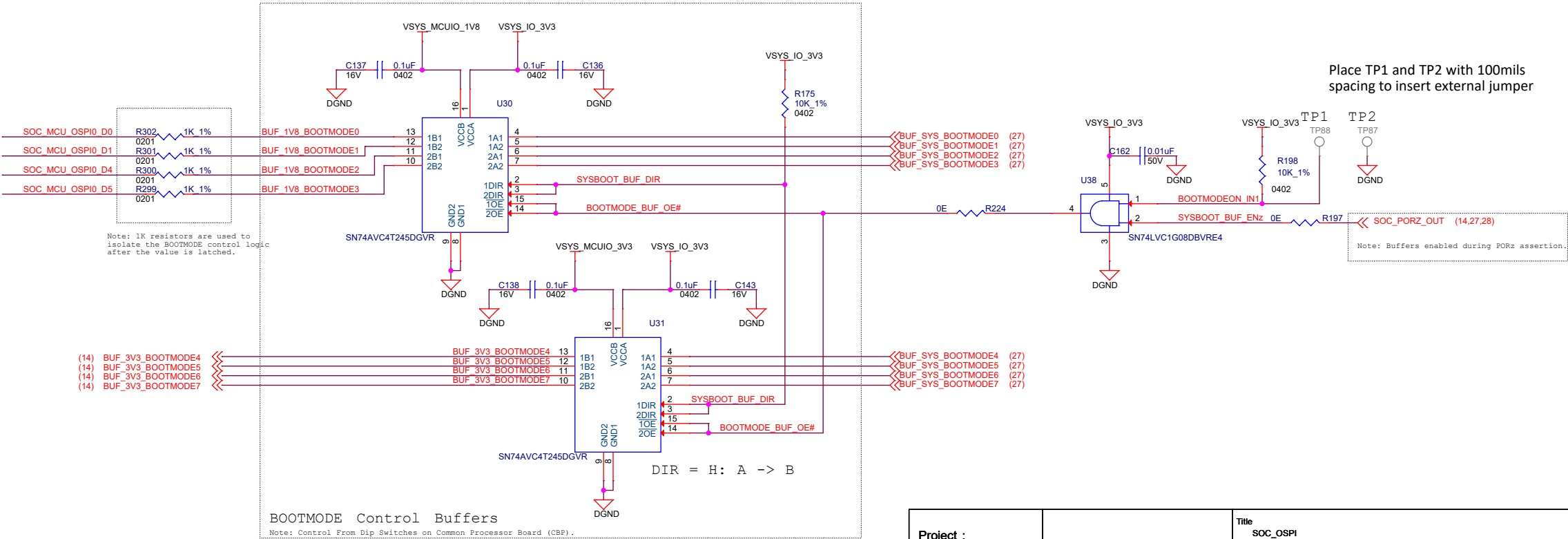
OSPI/HYPER\_MUX\_SEL Selection

OSPI/HYPER\_MUX\_SEL (14,27)

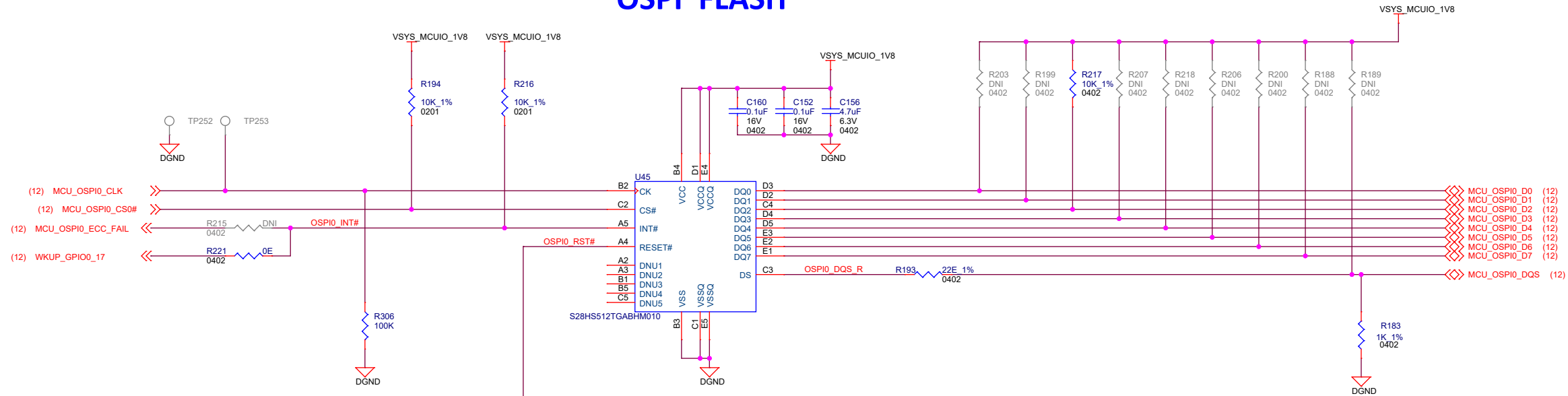
'0' - (A --> B) OSPI Flash

'1' - (A --> C) Hyperflash + HyperRAM

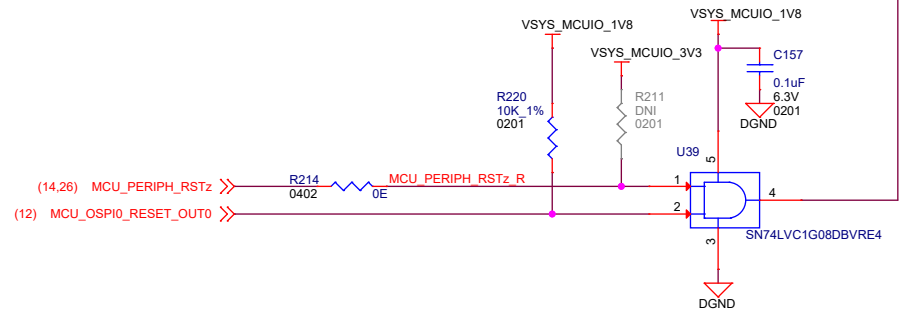
Note: Default set by dip switch



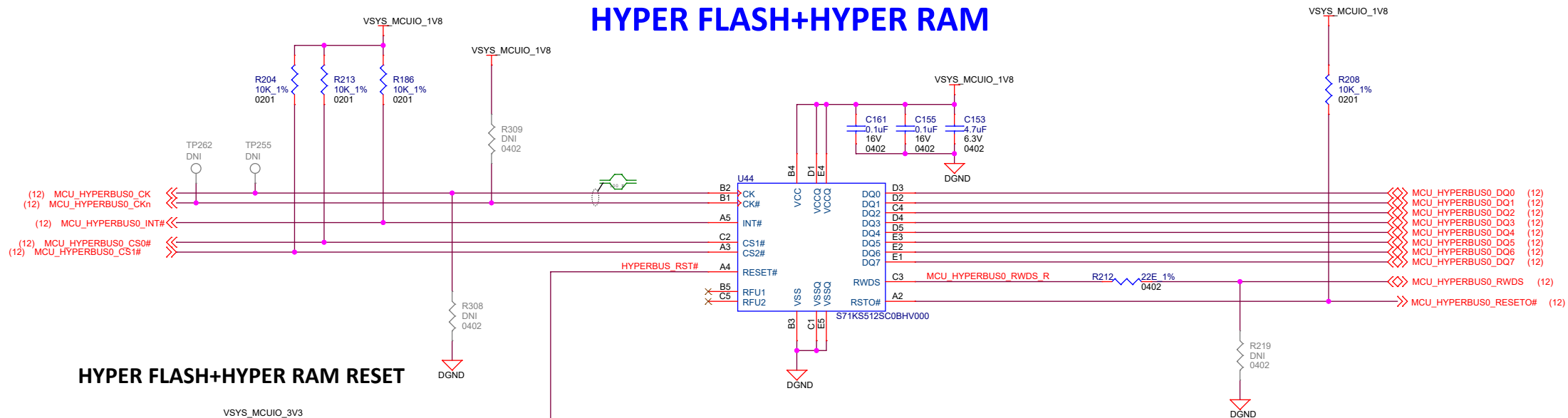
## OSPI FLASH



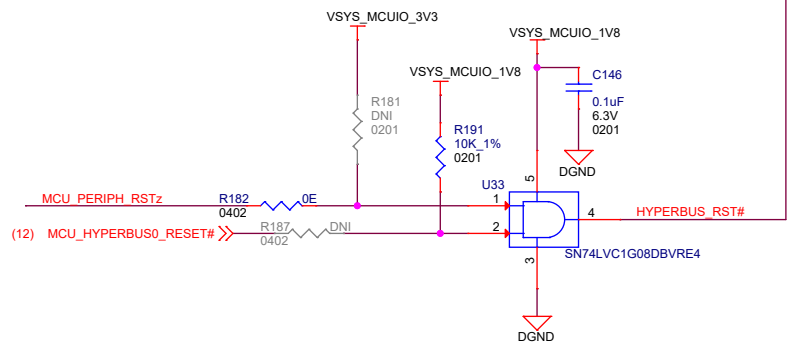
### OSPI FLASH RESET



## HYPER FLASH+HYPER RAM

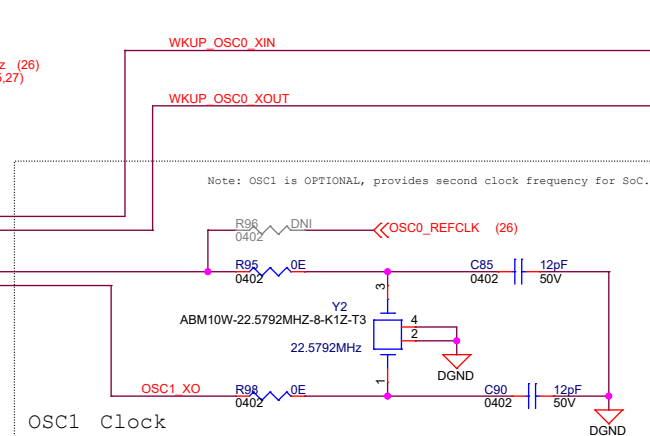
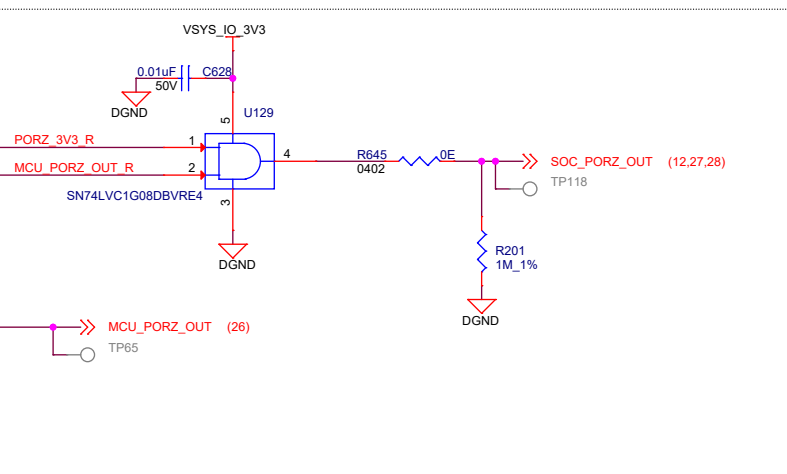
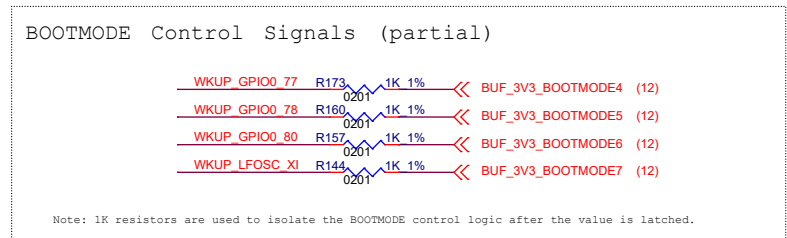
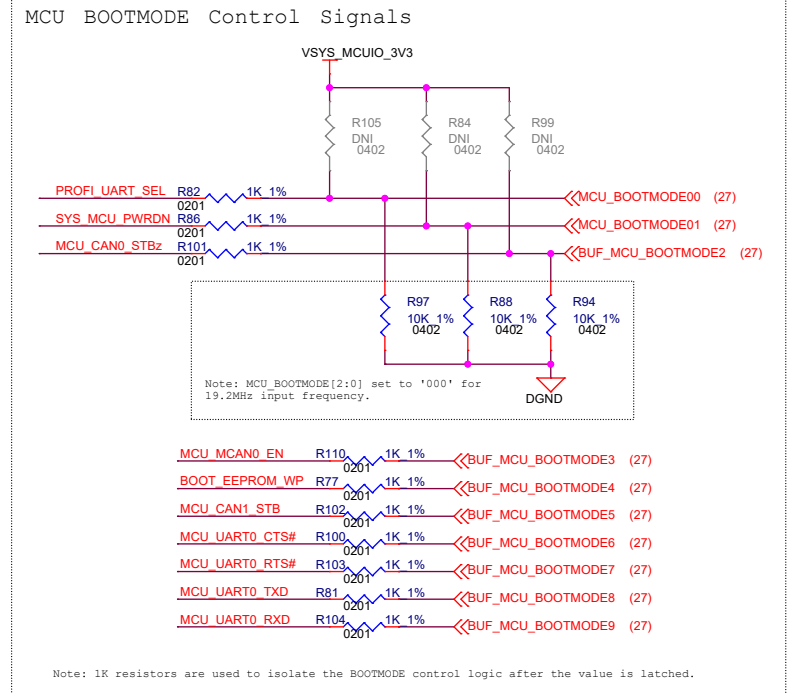
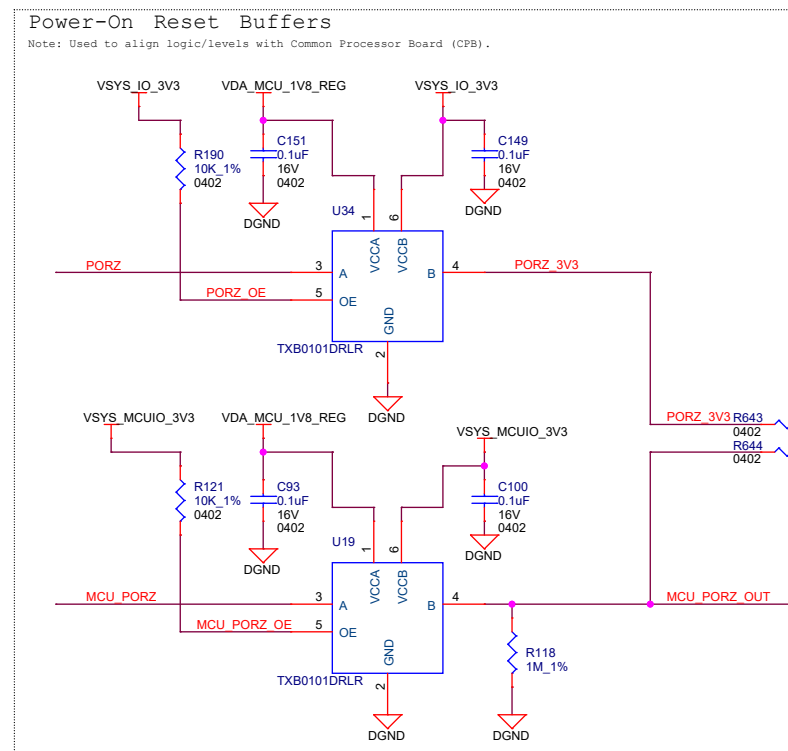
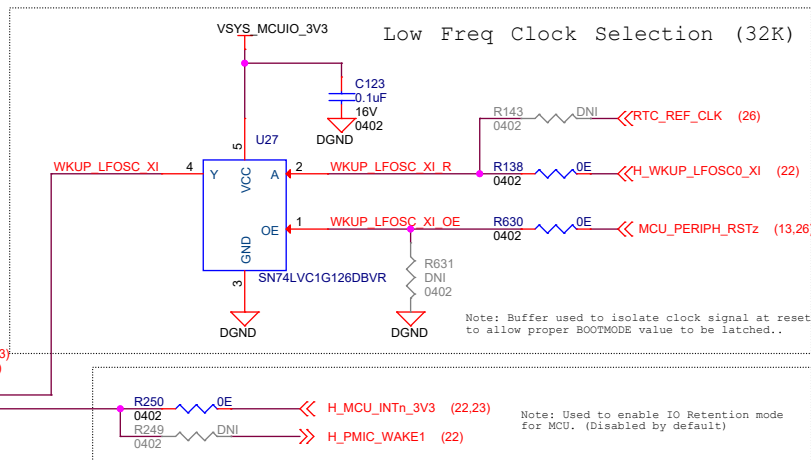
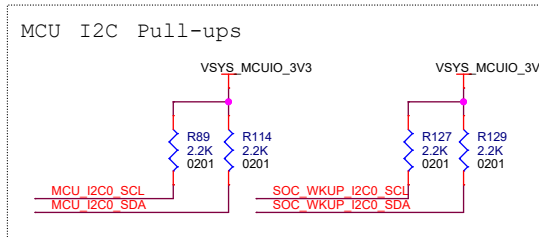
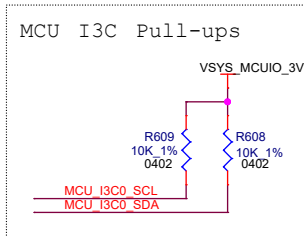
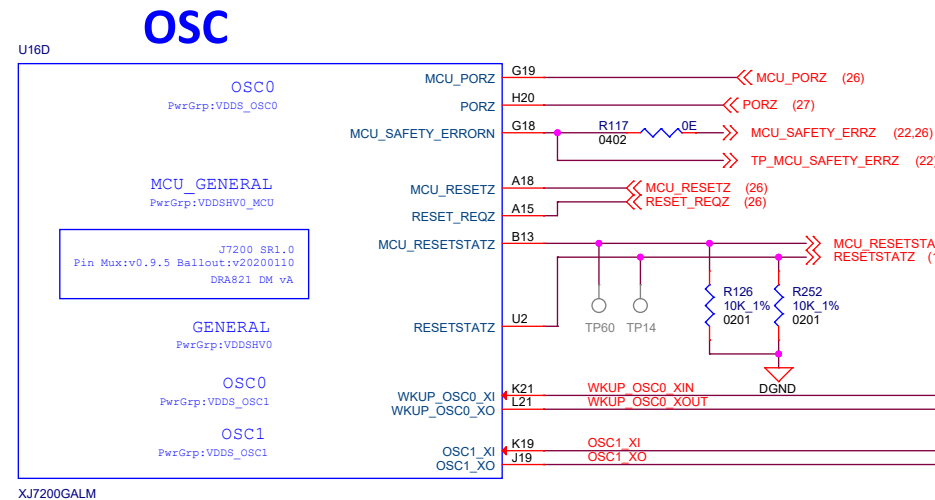
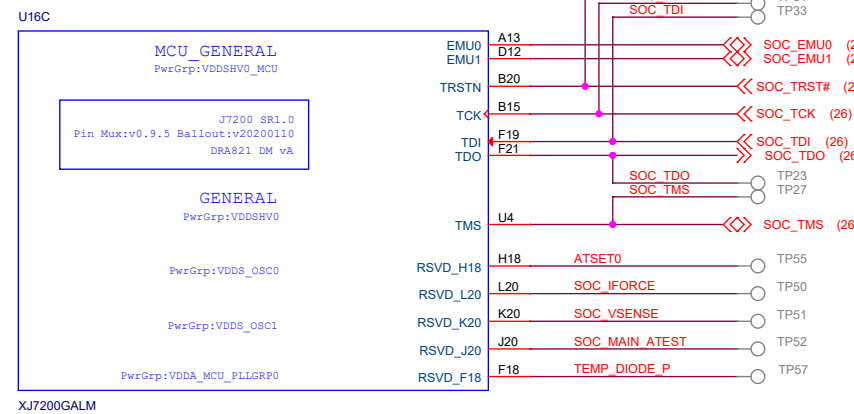
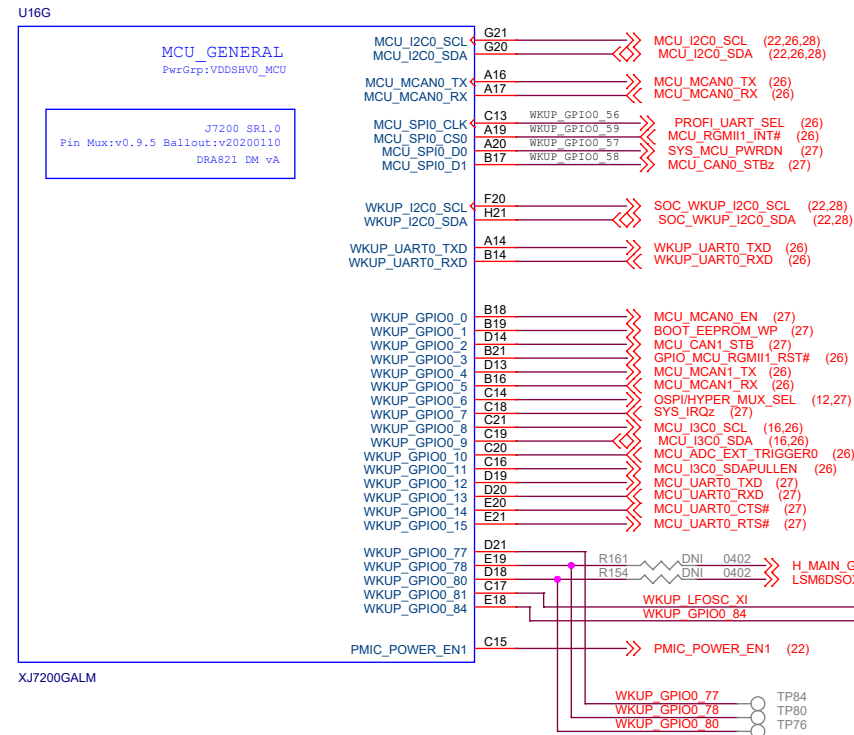


### HYPER FLASH+HYPER RAM RESET

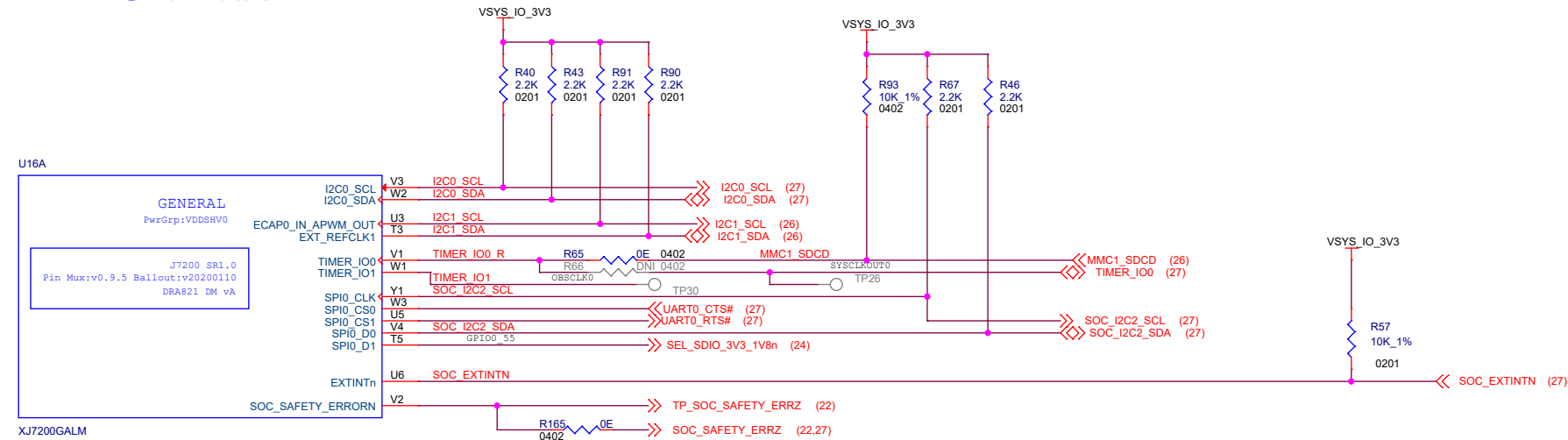




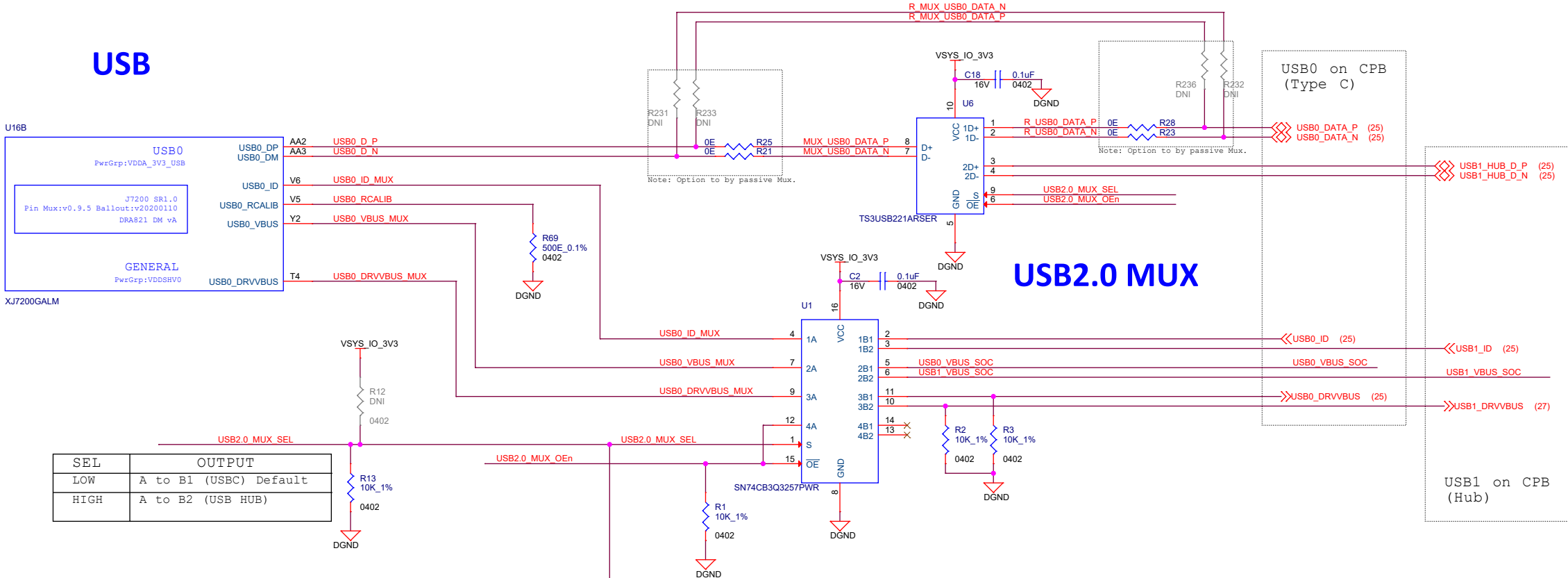
# MCU & MAIN GENERAL IO, OSC CLKS



# GENERAL

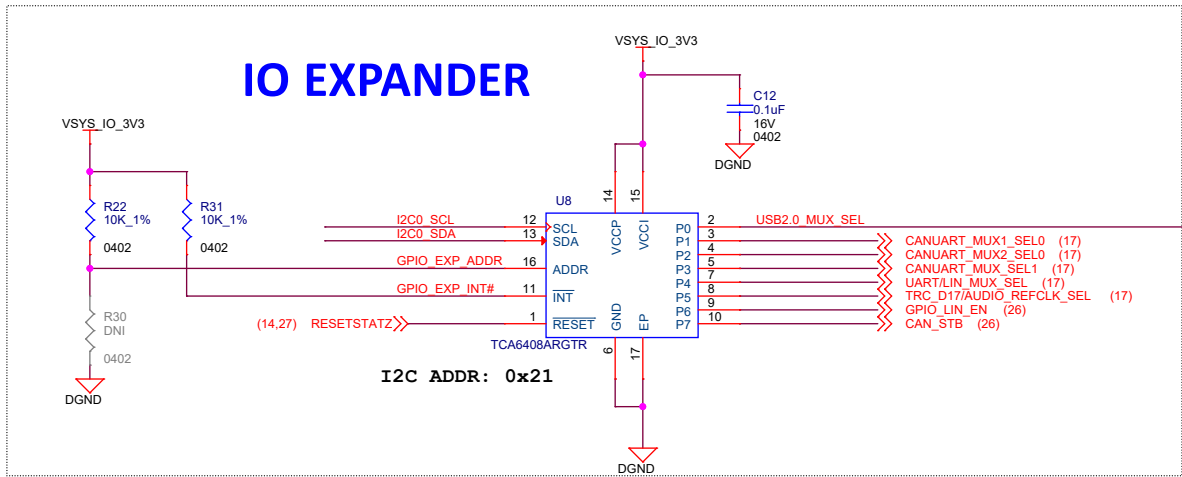


# USB

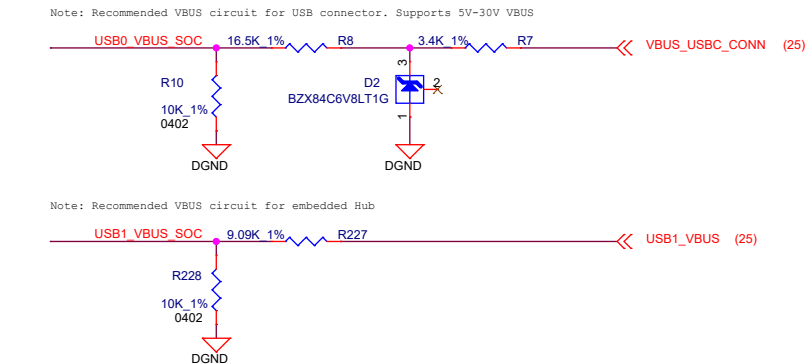


SEL	OUTPUT
LOW	A to B1 (USBC) Default
HIGH	A to B2 (USB HUB)

# IO EXPANDER



## USB VBUS Resistor divider circuit



Project :

J7 EVM



Title

GENERAL\_USB

Size

PROC105 001 J7200XSOMG01EVM

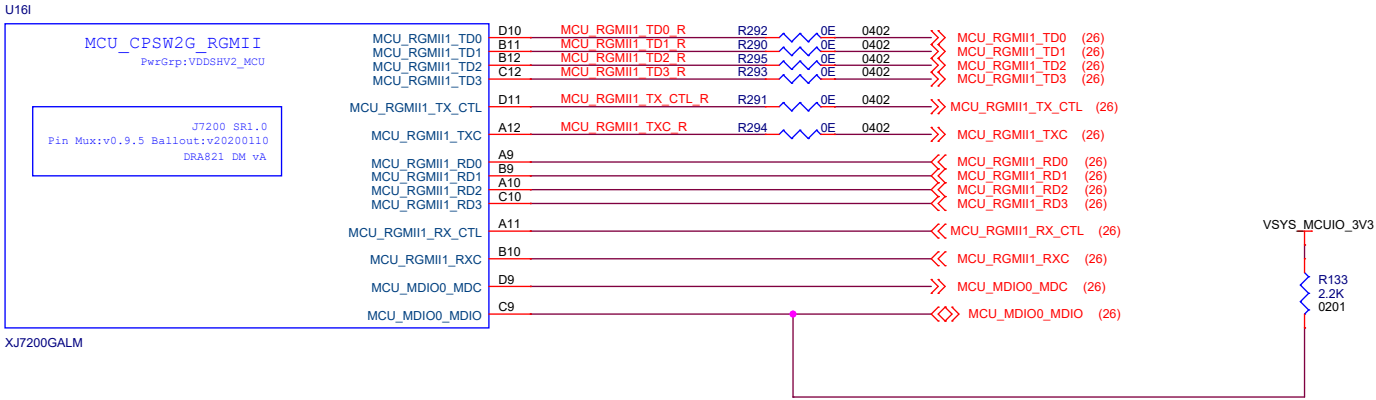
Rev

E8

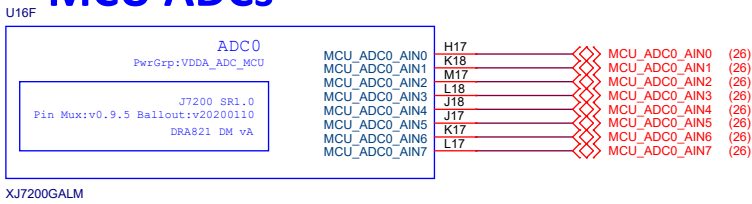
Date: Thursday, December 16, 2021

Sheet 15 of 34

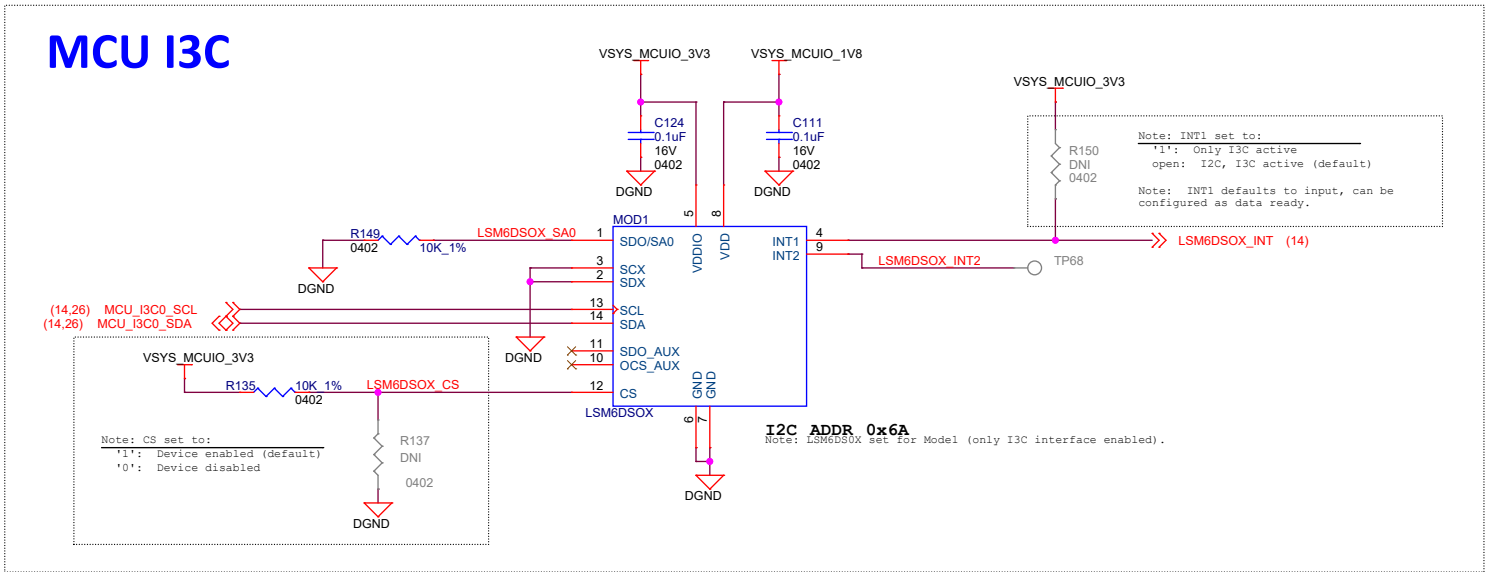
## MCU\_RGMII



## MCU ADCs



## MCU I3C



Project :

J7 EVM



Title  
MCU\_RGMII, MCU\_ADC & MCU\_I3C

Size  
C PROC105 001 J7200XSOMG01EVM

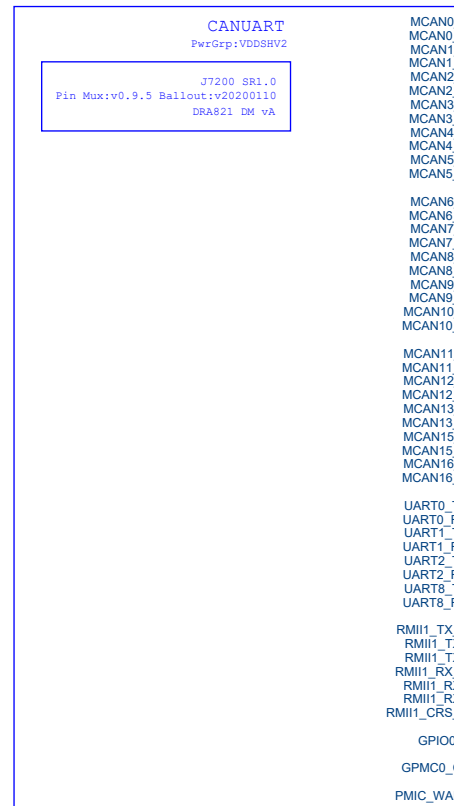
Date: Thursday, December 16, 2021

Sheet 16 of 34

Rev  
E8

# CAN/UART IO

U16K

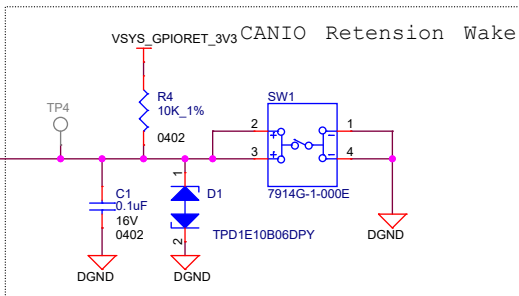
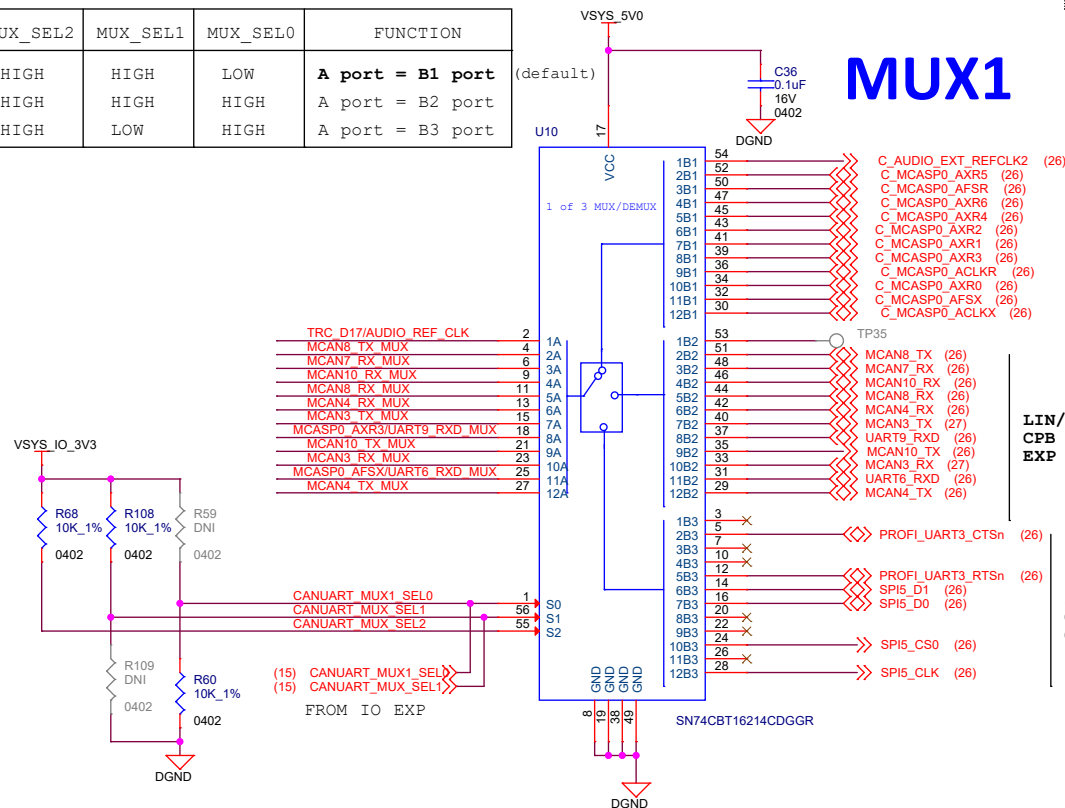


XJ7200GALM

SEL	OUTPUT
LOW	A to B1 (TRC/McASP) Default
HIGH	A to B2 (LIN/MCAN)

MCASP/TRAC/MCAN/LIN - 1:3 MUX : Truth Table

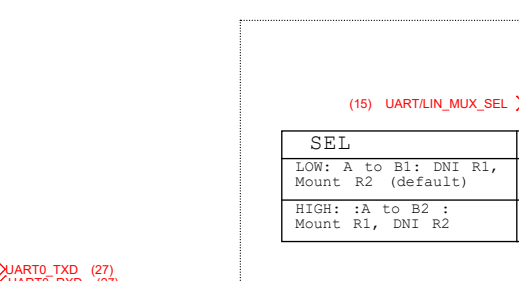
MUX_SEL2	MUX_SEL1	MUX_SEL0	FUNCTION
HIGH	HIGH	LOW	A port = B1 port
HIGH	HIGH	HIGH	A port = B2 port
HIGH	LOW	HIGH	A port = B3 port



**RGMI2**

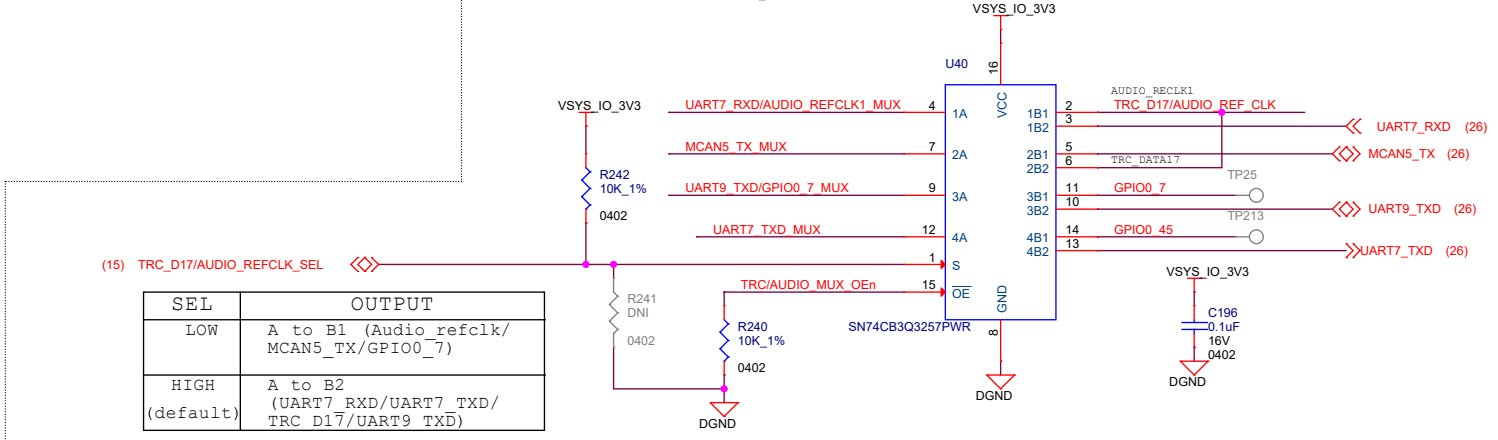
Note: Supported on CPB-EXP.

SEL	OUTPUT
LOW	A to B1: DNI R1, Mount R2 (default)
HIGH	:A to B2 : Mount R1, DNI R2



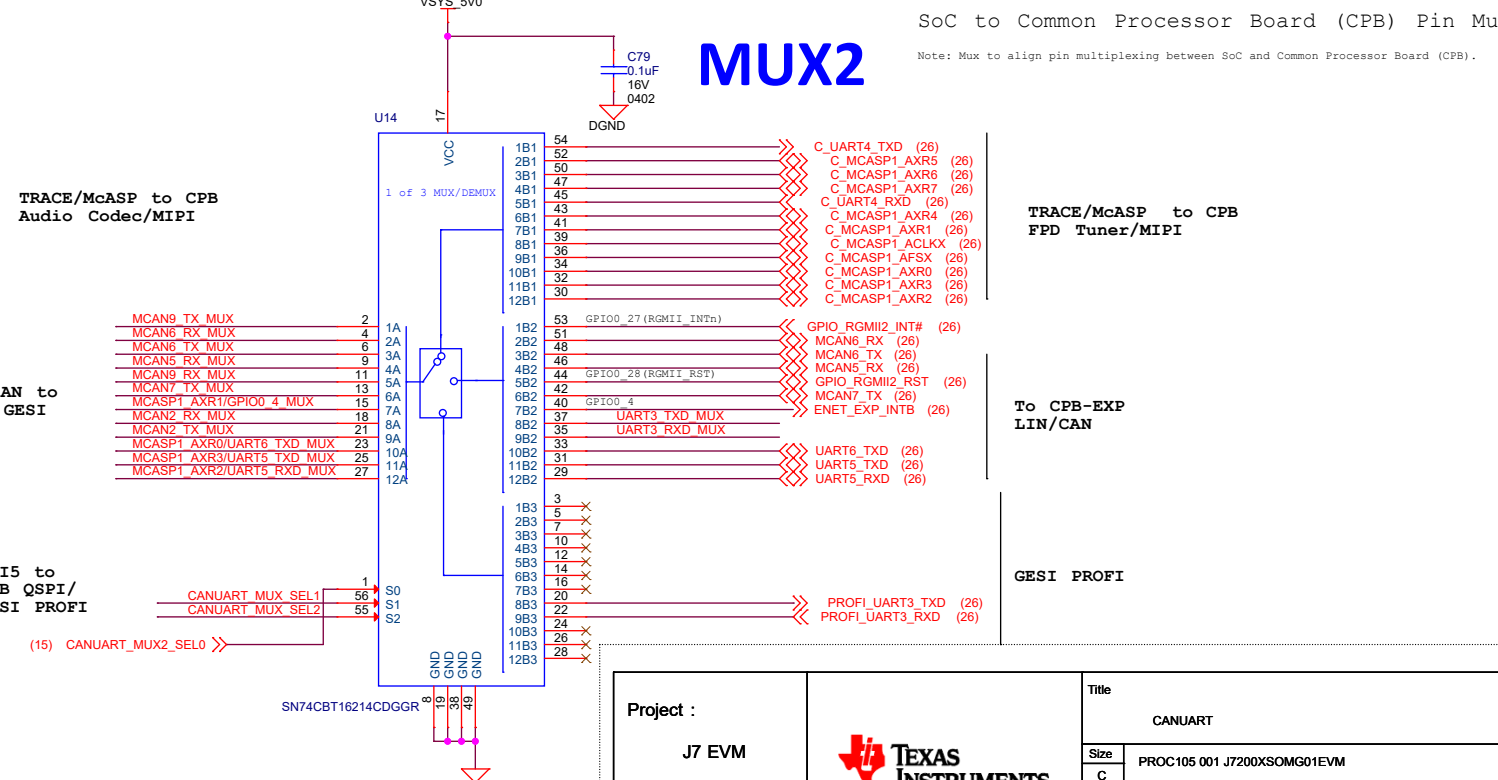
SoC to Common Processor Board (CPB) Pin Mux

Note: Mux to align pin multiplexing between SoC and Common Processor Board (CPB).  
(Specifically new location of AUDIO\_REFCLK)

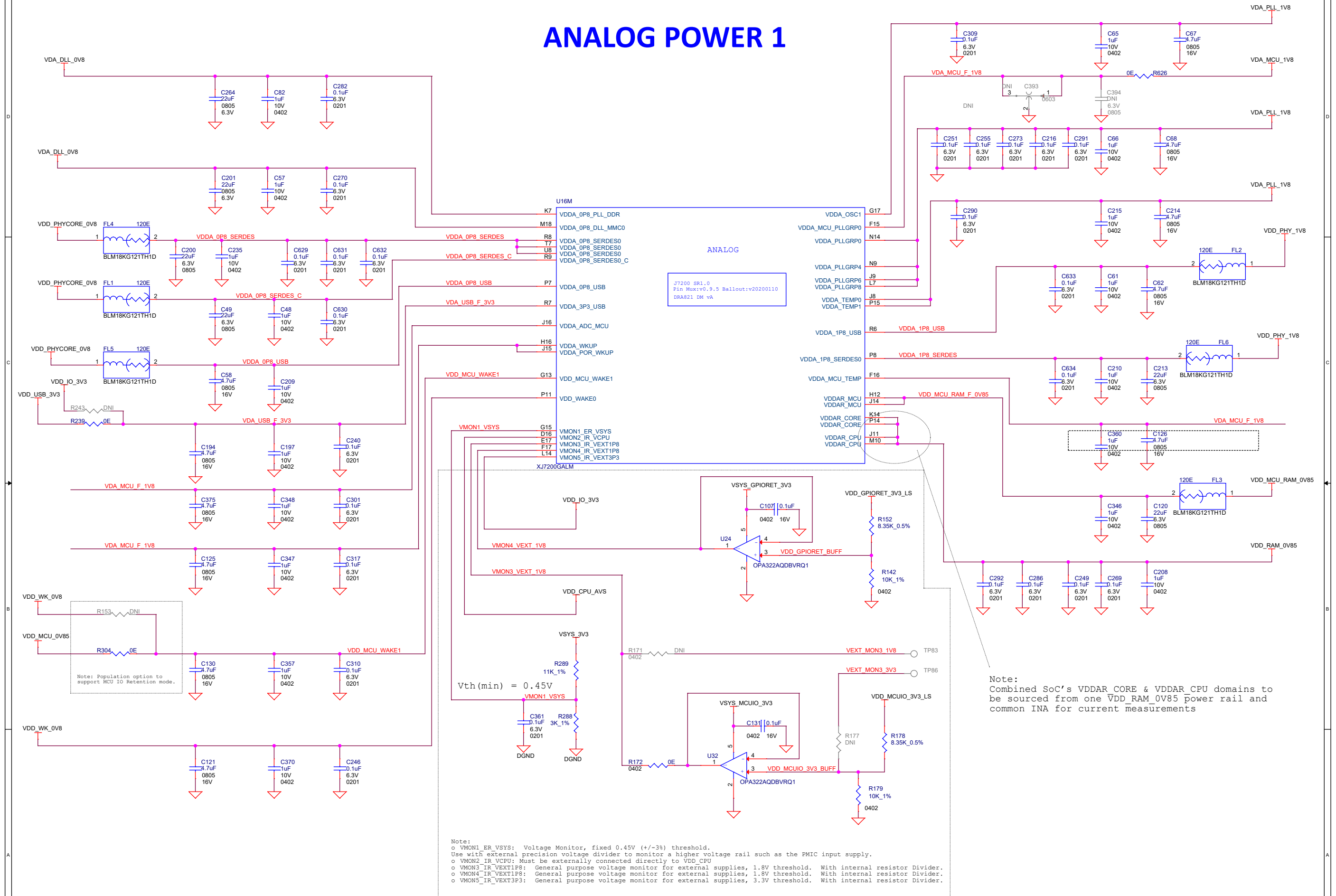


SoC to Common Processor Board (CPB) Pin Mux

Note: Mux to align pin multiplexing between SoC and Common Processor Board (CPB).



# ANALOG POWER 1



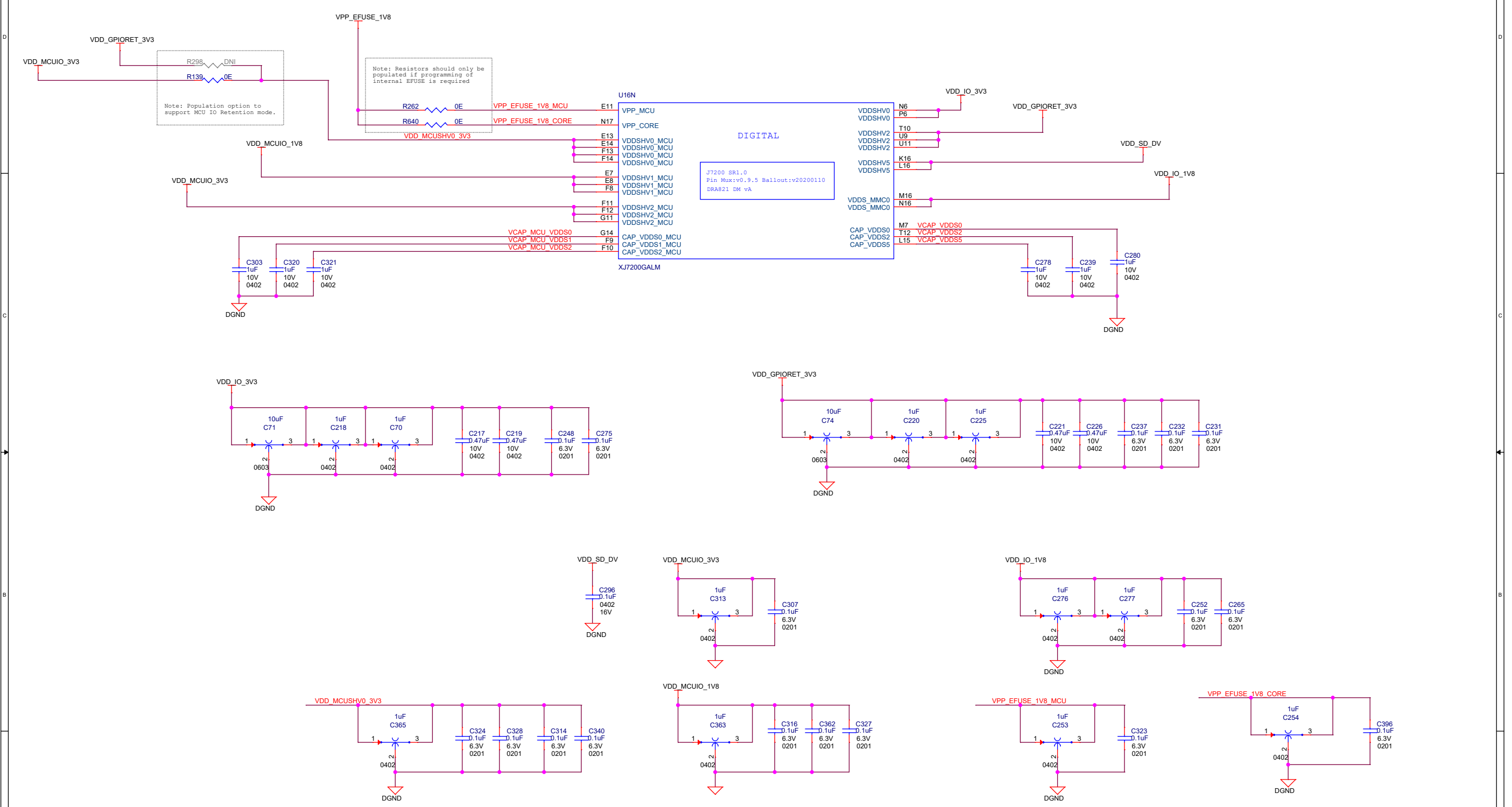
Note:  
Combined SoC's VDDAR CORE & VDDAR CPU domains to  
be sourced from one VDD\_RAM\_0V85 power rail and  
common INA for current measurements

Note:

- o VMON1\_ER\_VSUS: Voltage Monitor, fixed 0.45V (+/-3%) threshold.  
Use with external precision voltage divider to monitor a higher voltage rail such as the PMIC input supply.
- o VMON2\_IR\_VCPU: Must be externally connected directly to VDD\_CPU
- o VMON3\_IR\_VEXT1P8: General purpose voltage monitor for external supplies, 1.8V threshold. With internal resistor Divider.
- o VMON4\_IR\_VEXT1P8: General purpose voltage monitor for external supplies, 1.8V threshold. With internal resistor Divider.
- o VMON5\_IR\_VEXT3P3: General purpose voltage monitor for external supplies, 3.3V threshold. With internal resistor Divider.




DIGITAL POWER 2

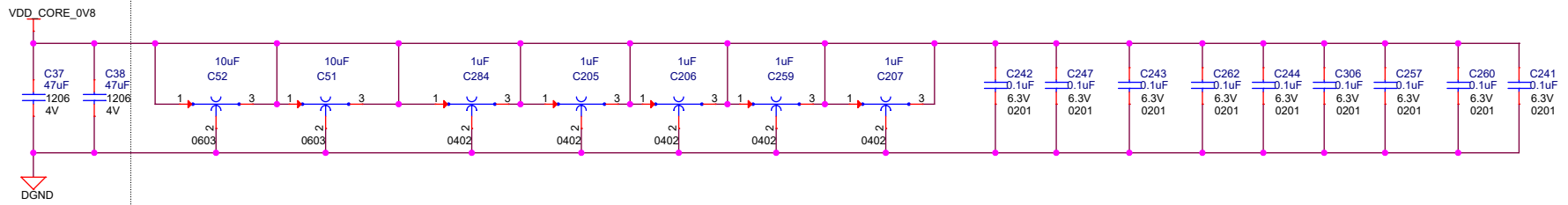
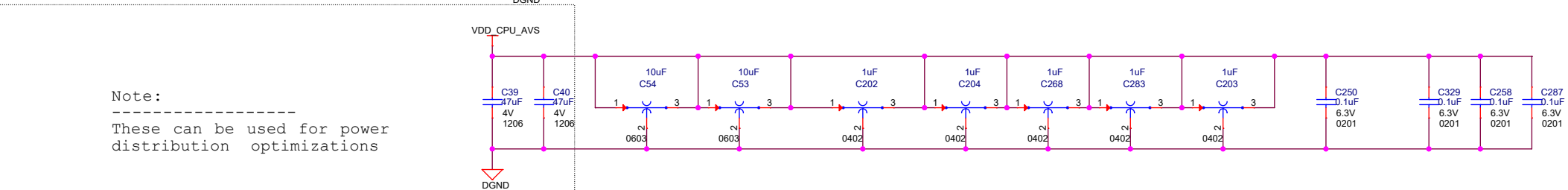
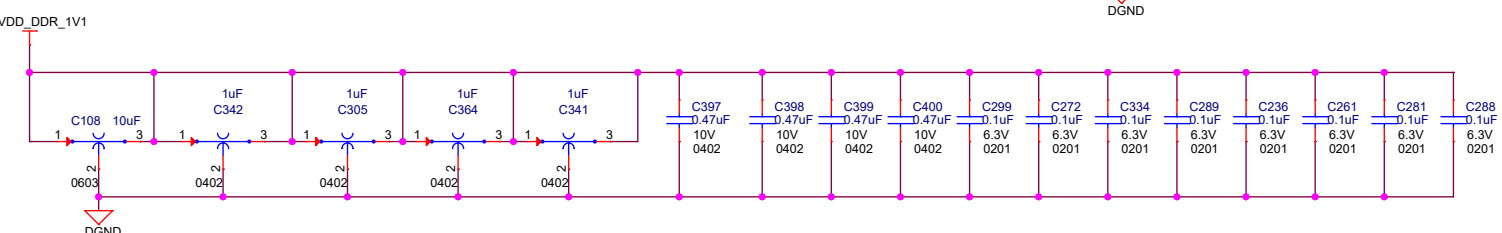
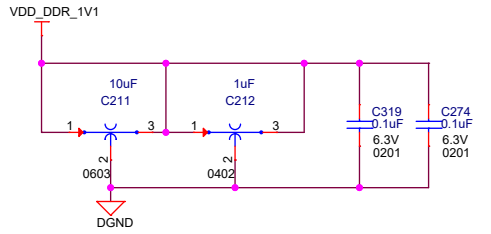
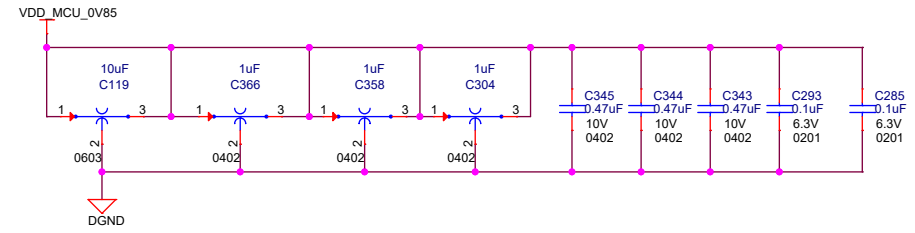
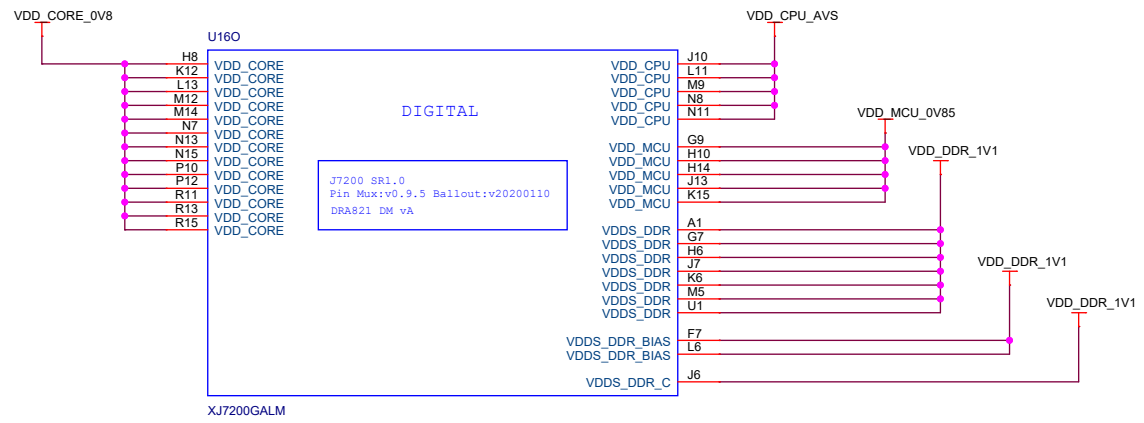


Note:  
-----  
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Project :  J7 EVM		Title SOC POWER 2			
		Size	PROC105 001 J7200XSOMG01EVM	Rev	
		C		E8	
		Date:	Thursday, December 16, 2021	Sheet	19

DIGITAL POWER 3

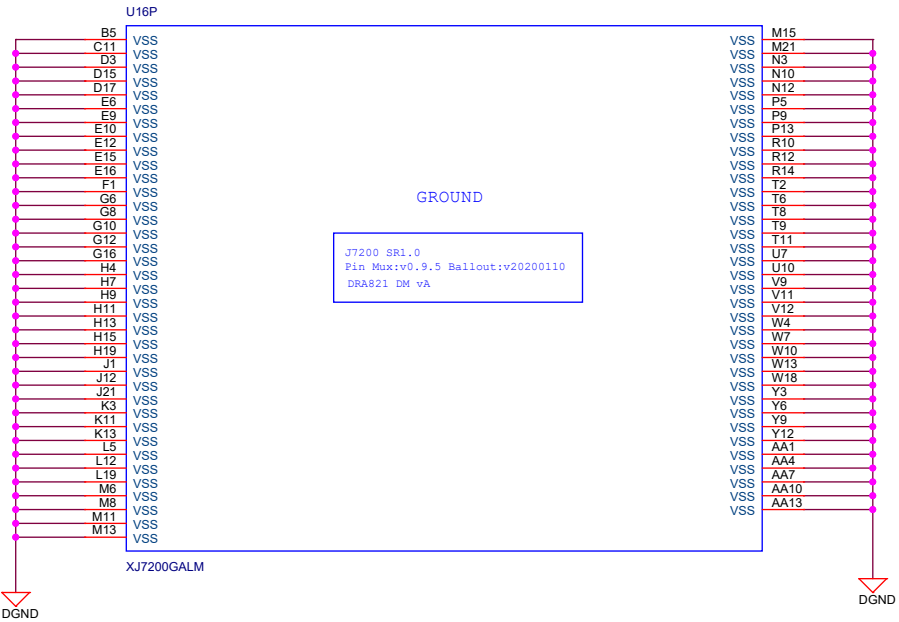


Note:  
-----  
These can be used for power distribution optimizations

Note:  
-----  
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

SOC GROUND

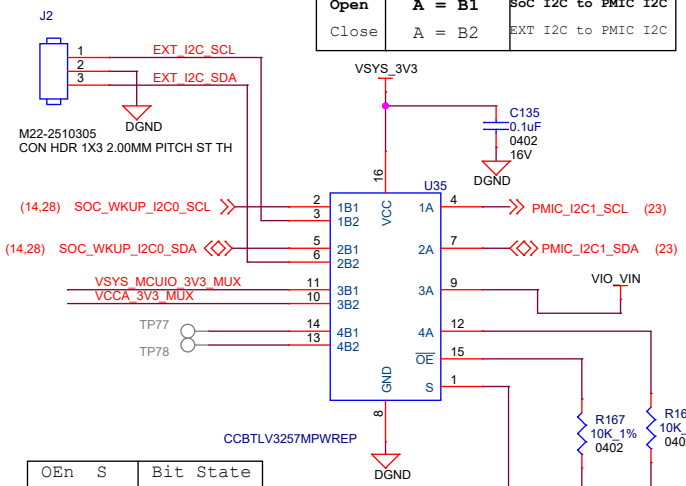


# EVM development & evaluation Test circuitry

(TI EVM Only)

(EVM Bd Default Setting):

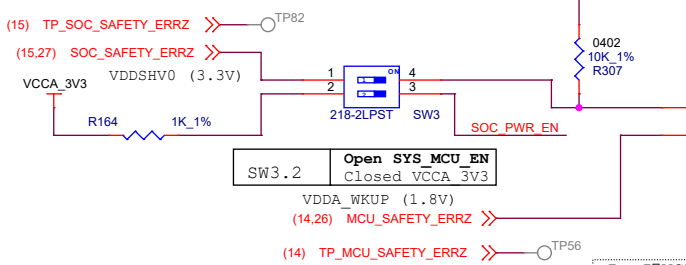
SW4.2	Port State	Function
Open	A = B1	SoC I2C to PMIC I2C
Close	A = B2	EXT I2C to PMIC I2C



OEn	S	Bit State
0	0	A = B1
0	1	A = B2
1	X	Open

(EVM Bd Setting & Leo NVM Default):

SW3.1	SYS SAFETY_ERRn
Open	MCU SAFETY_ERRn
Closed	Active low, SoC ERRn or MCU ERRn



In J7VCL SOM DIP Switch Operation:  
SWITCH ON = LOGIC 1  
SWITCH OFF = LOGIC 0

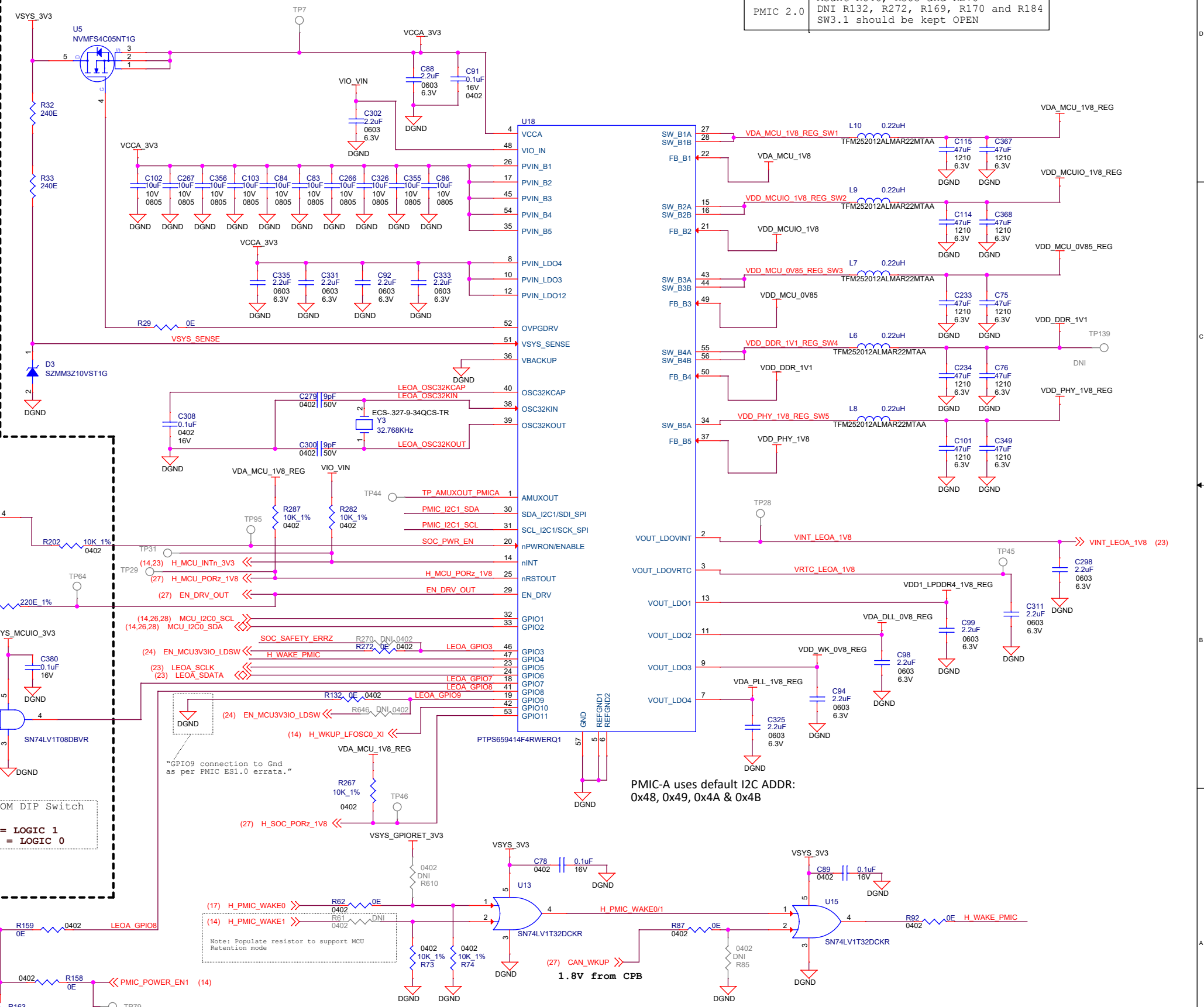
(EVM Bd Setting & Leo NVM Default):

SW2		GPIO: Type	NVM Funtion
-1 = Open (Low) = Closed (High)	NA	NA	NA
-2 = Closed (High) = Open (Low)	Disable WDOG Timer Enable WDOG Timer	In In	Disable WDOG Enable WDOG

## PMIC- A(1.0)

### PMIC Version

PMIC 1.0	Mount R132, R272, R169 and R184 DNI R270, R646, R170 and R305
PMIC 2.0	Mount R646, R305 and R270 DNI R132, R272, R169, R170 and R184 SW3.1 should be kept OPEN



PMIC-A uses default I2C ADDR:  
0x48, 0x49, 0x4A & 0x4B

Project :  
J7 EVM

TEXAS  
INSTRUMENTS

Title  
POWER SUPPLY 1

Size  
C

Date: Friday, February 18, 2022

Rev  
E8

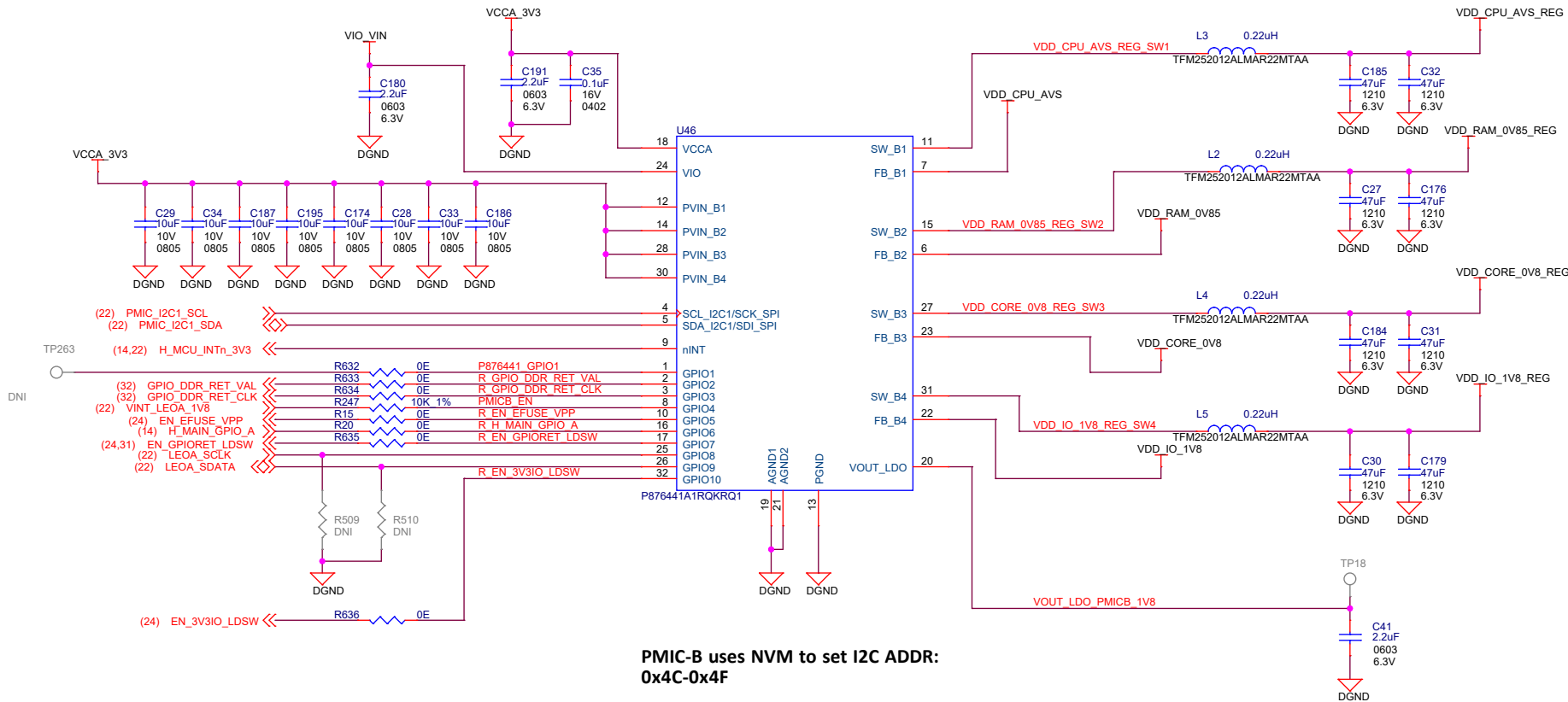
Sheet 22 of 34

PMIC - B(1.0)

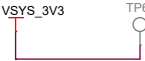
"PCB Notes:

For single-phase Buck converters, route remote sense feedback as follows:

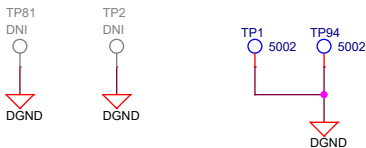
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"



Power Test Point

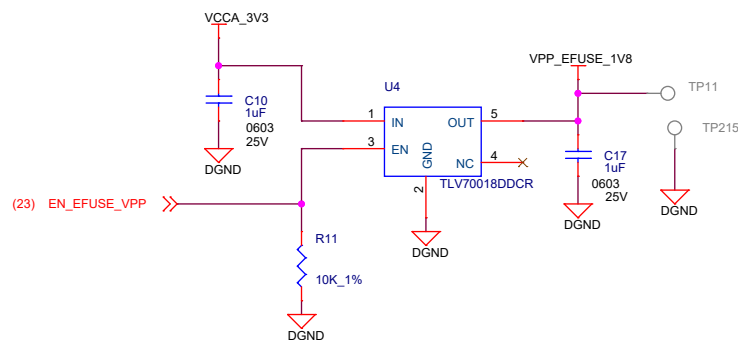
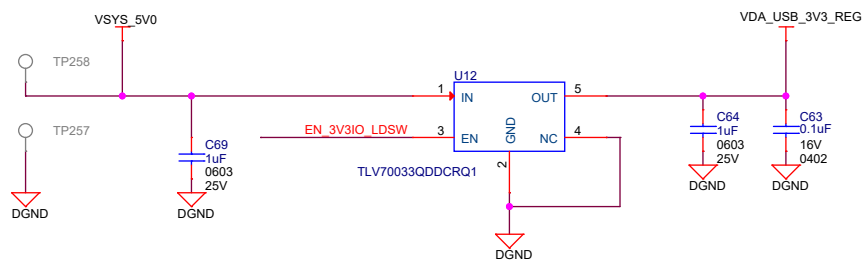
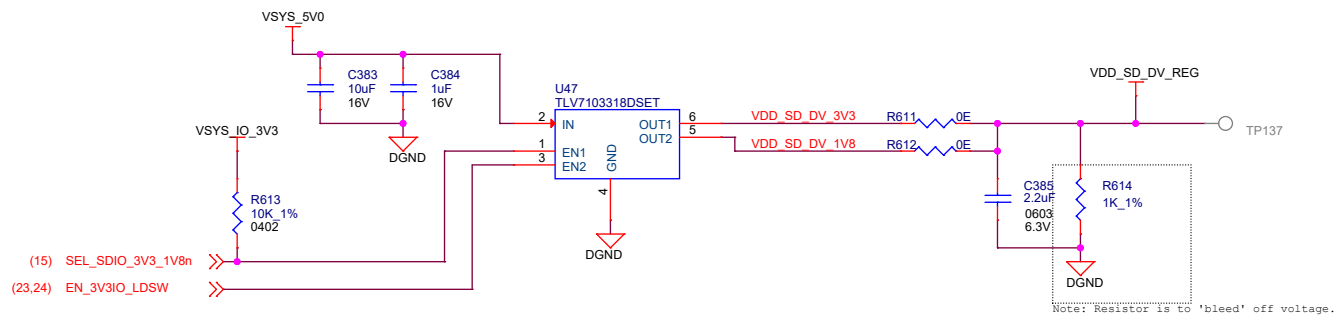
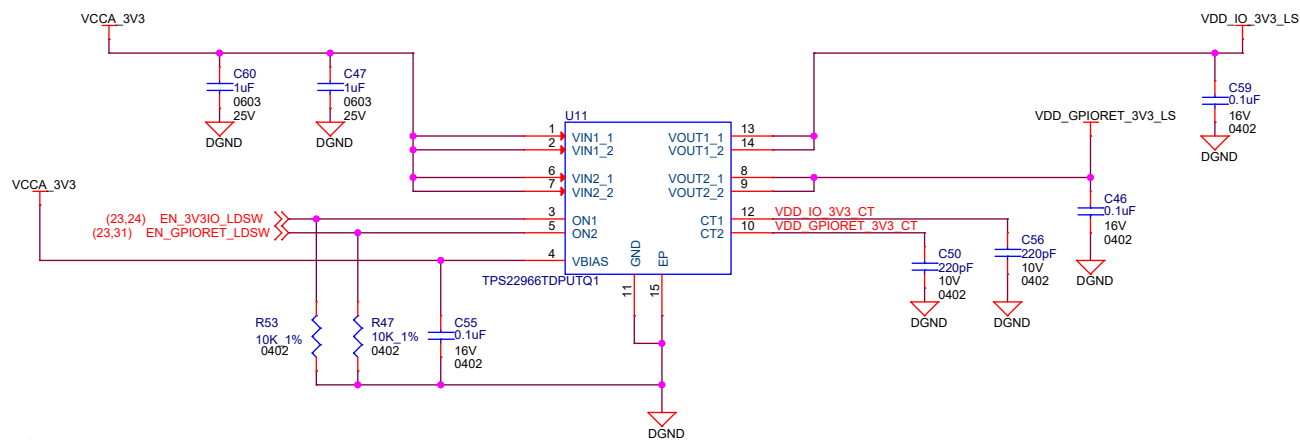
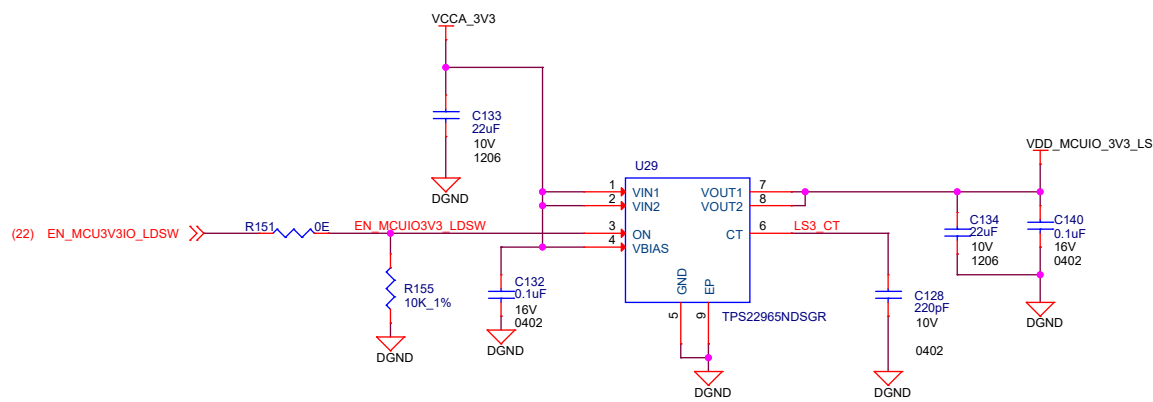


Ground Test Points

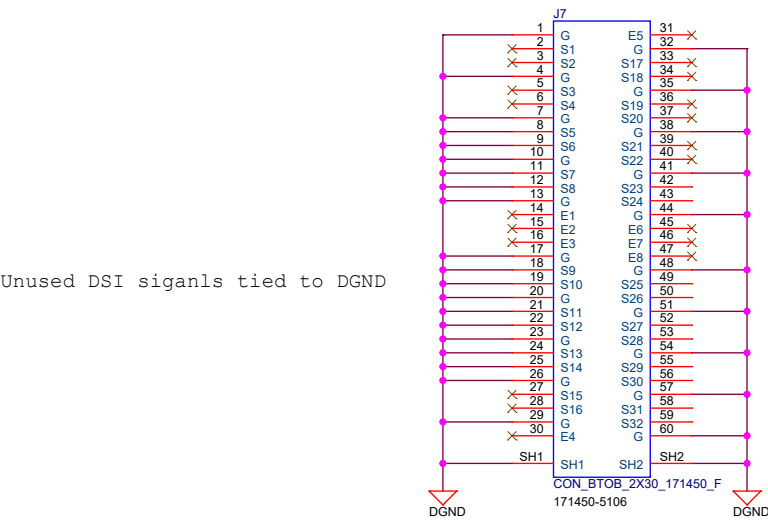
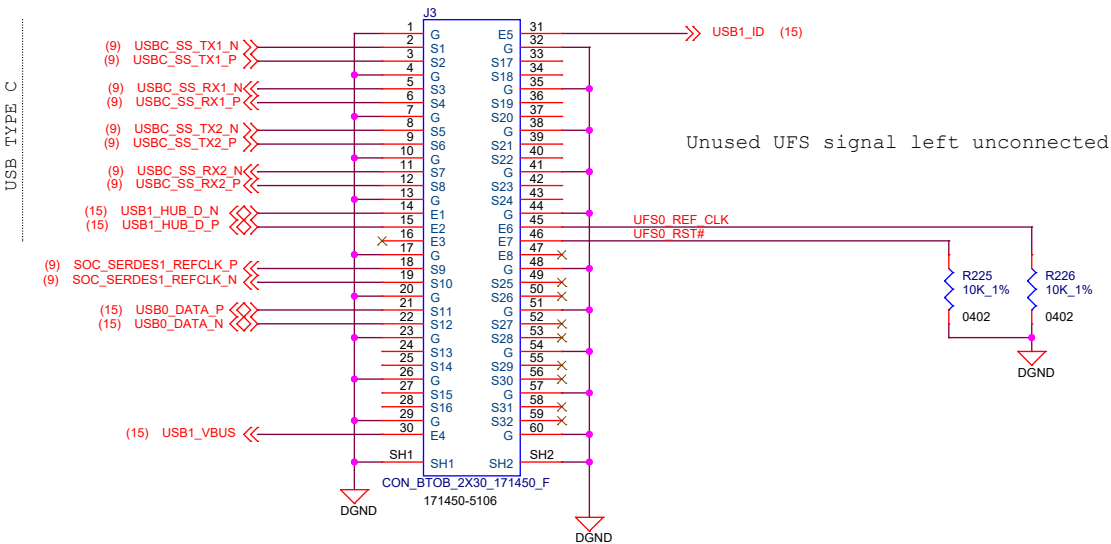
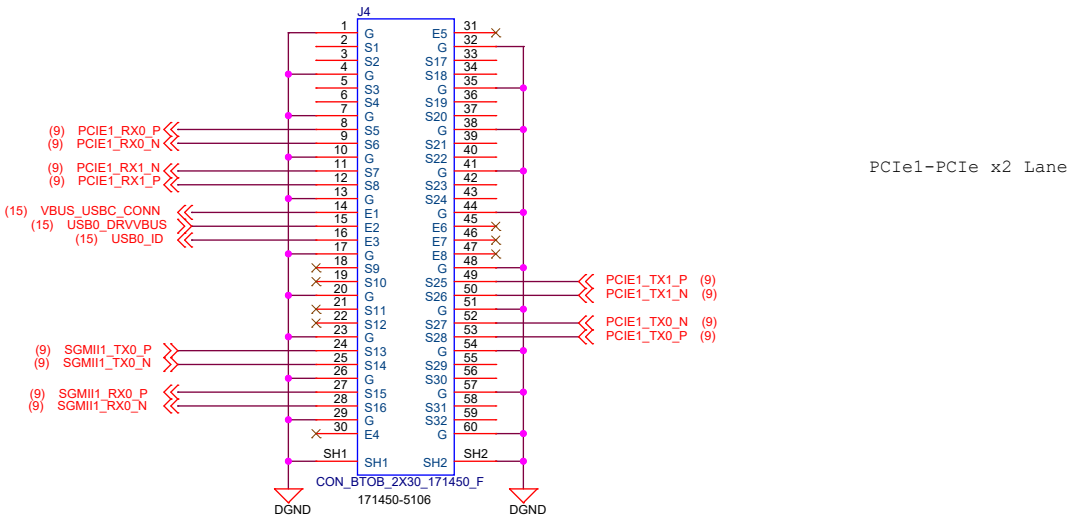




LOAD SWITCHES



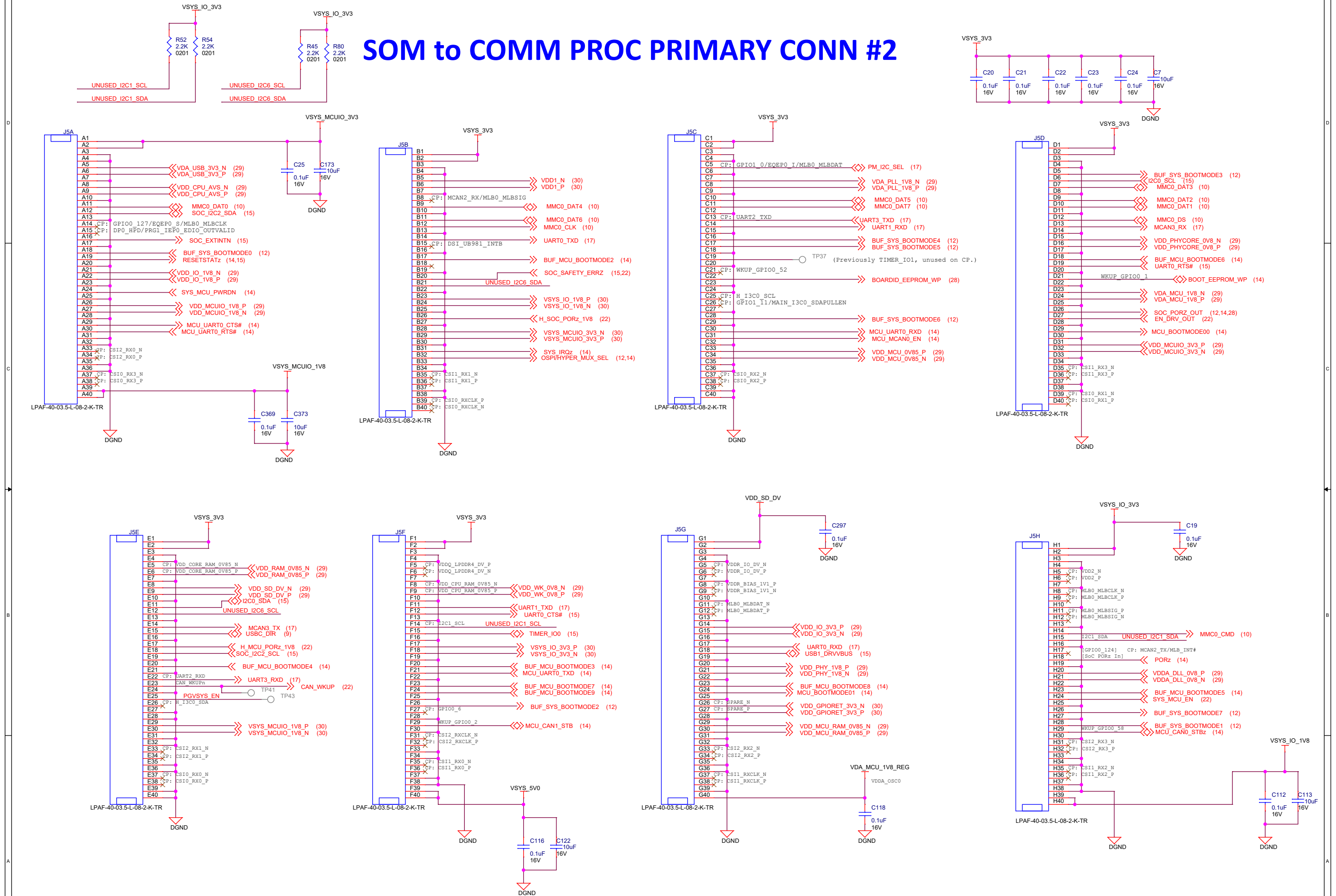
SOM to COMM PROC SERDES CONNECTORS



SOM to COMM PROC PRIMARY CONN #1

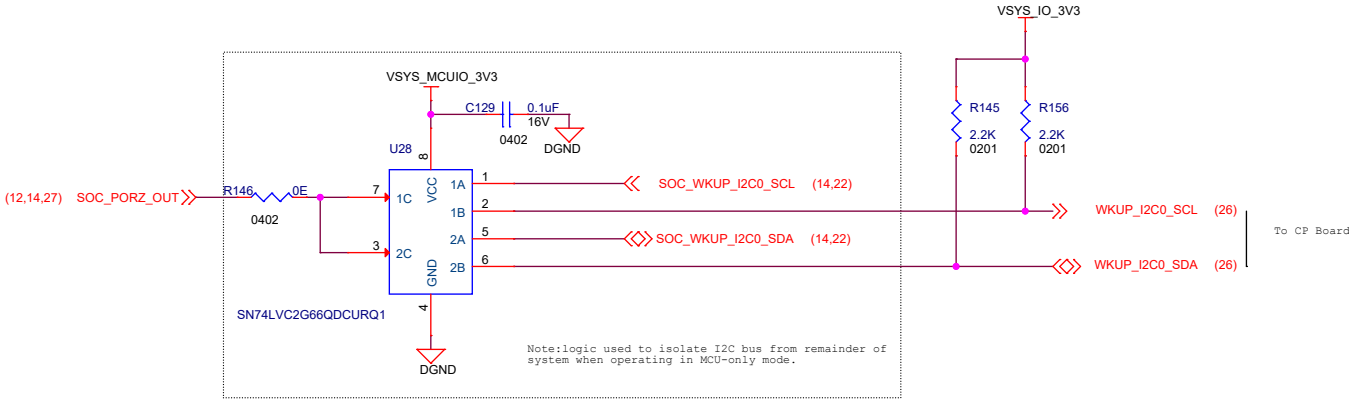


## SOM to COMM PROC PRIMARY CONN #2

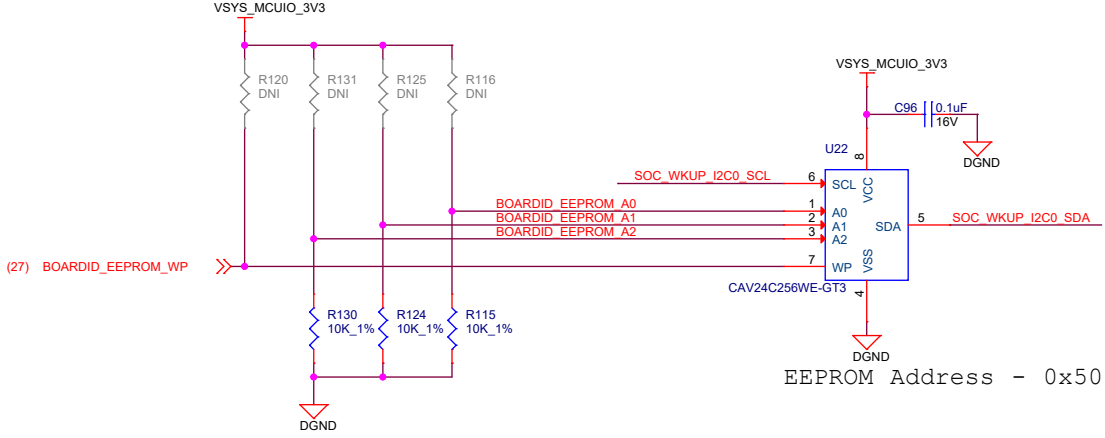


(TI EVM Only)

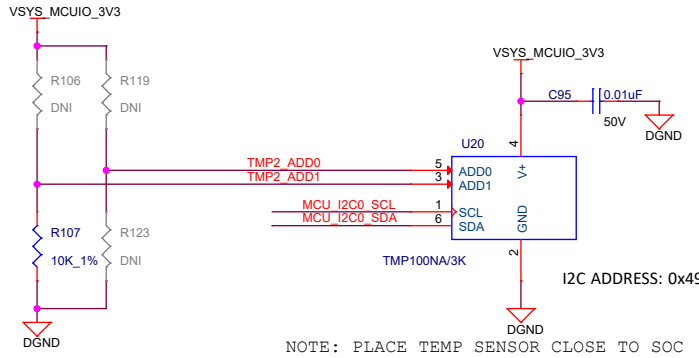
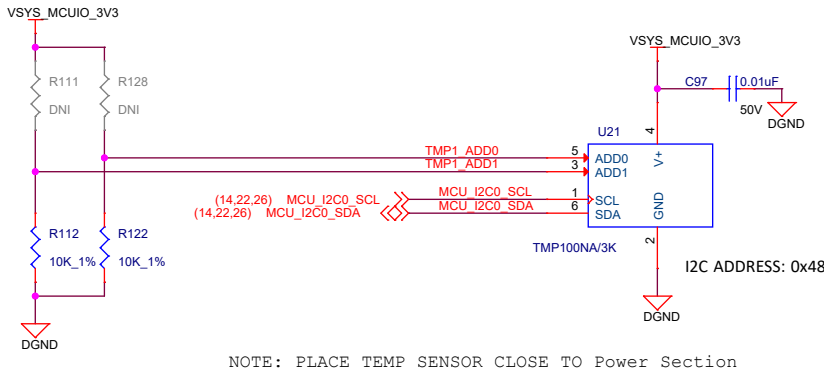
## I2C for BOARD ID EEPROMs



## BOARD ID EEPROM (TI EVM Only)



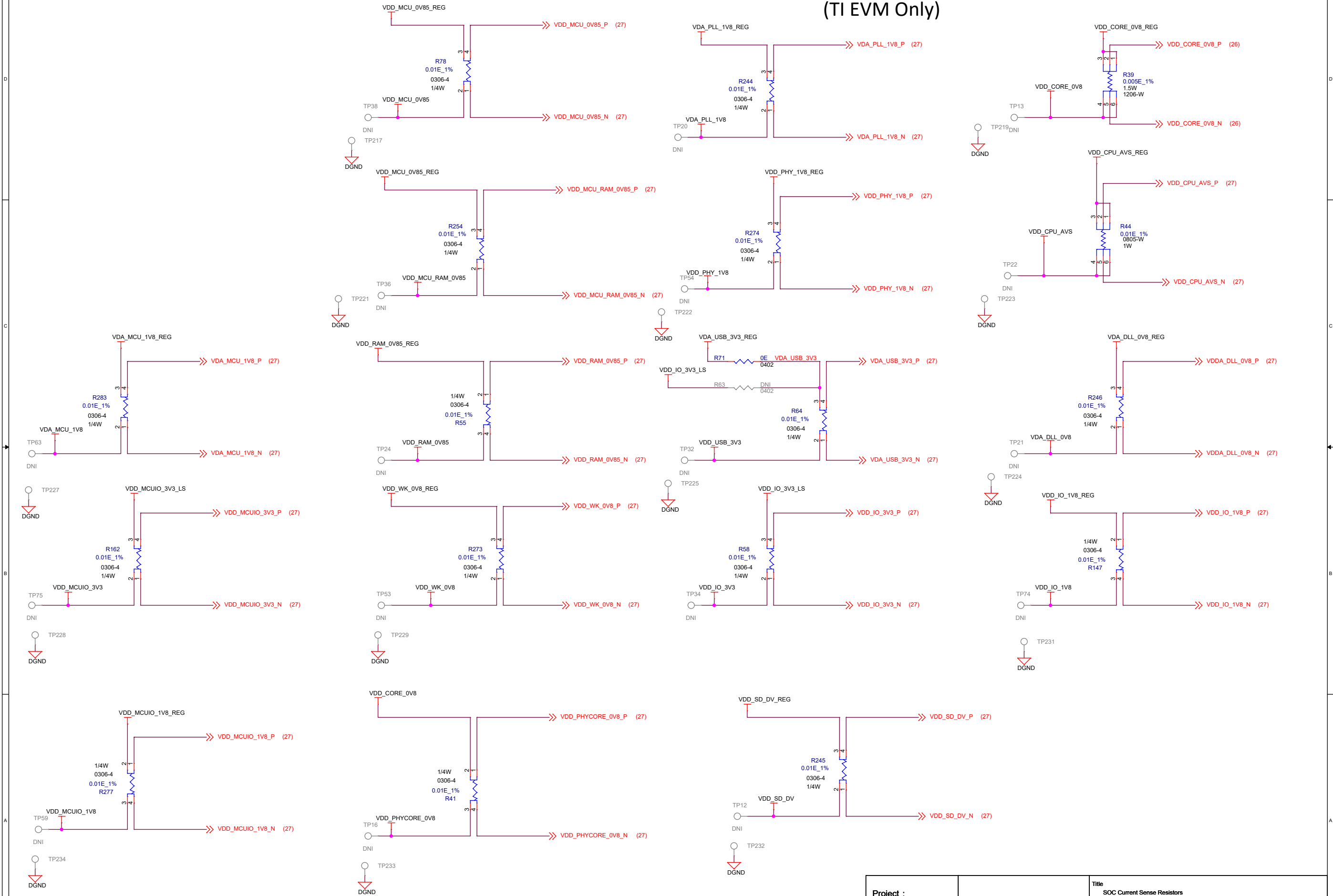
## TEMPERATURE SENSORS (TI EVM Only)





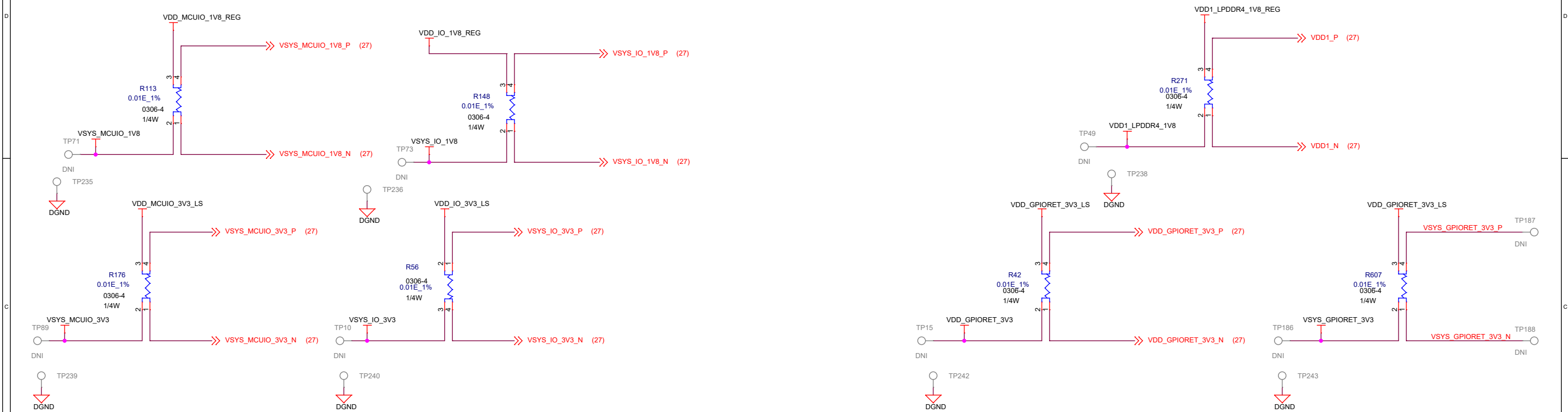
SOC Current Sense Resistors

EVM development & evaluation test circuitry  
(TI EVM Only)

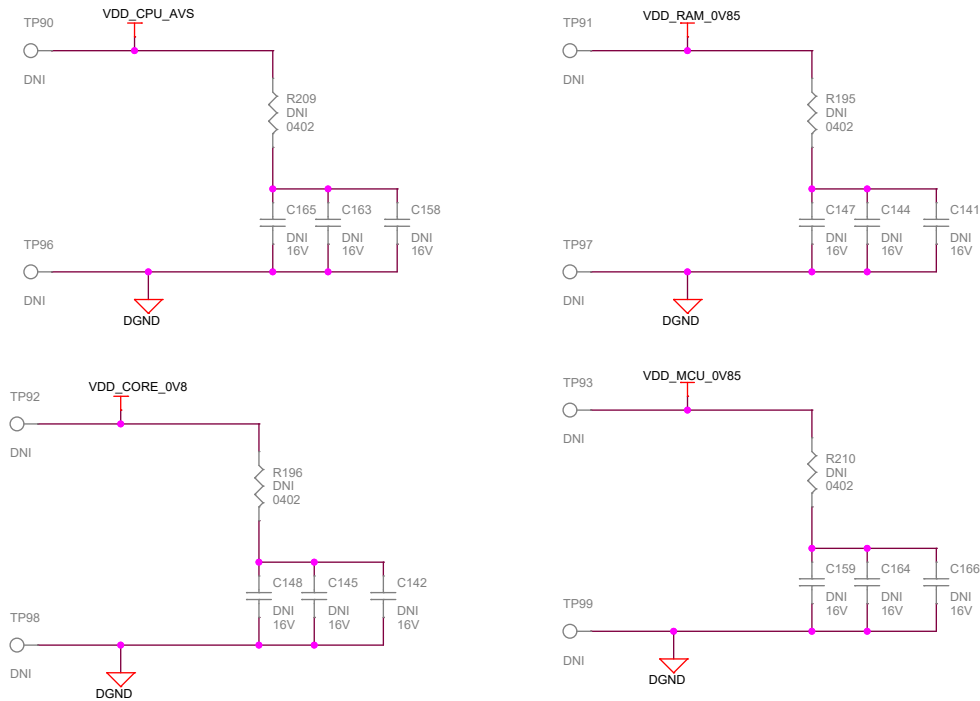


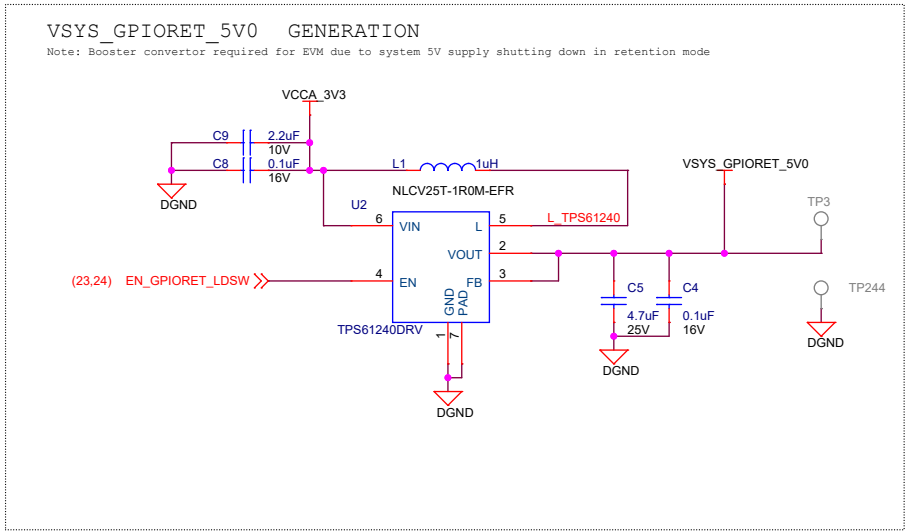
EVM development & evaluation test circuitry  
(TI EVM Only)

Peripheral Current Sense Resistors

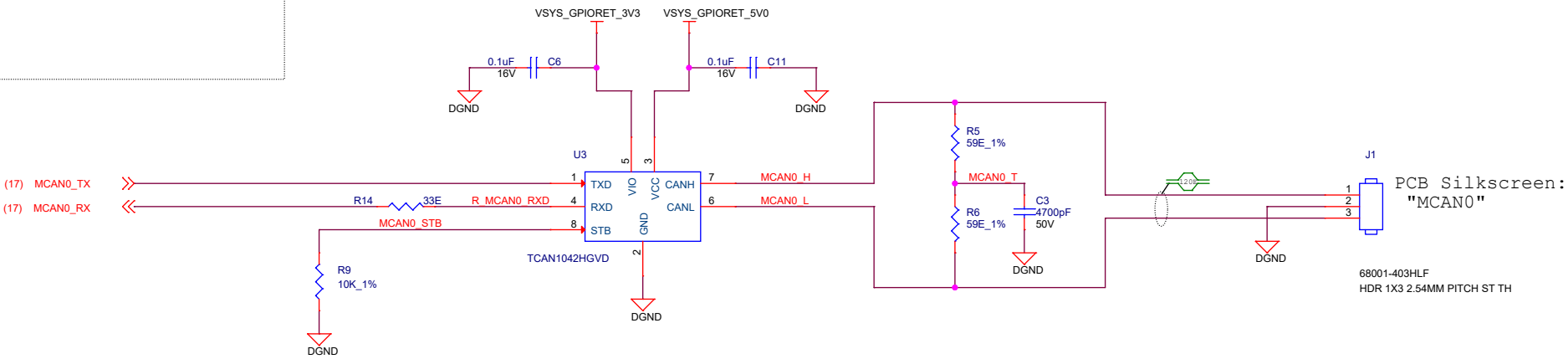


Supply Rail Kelvin Sensing





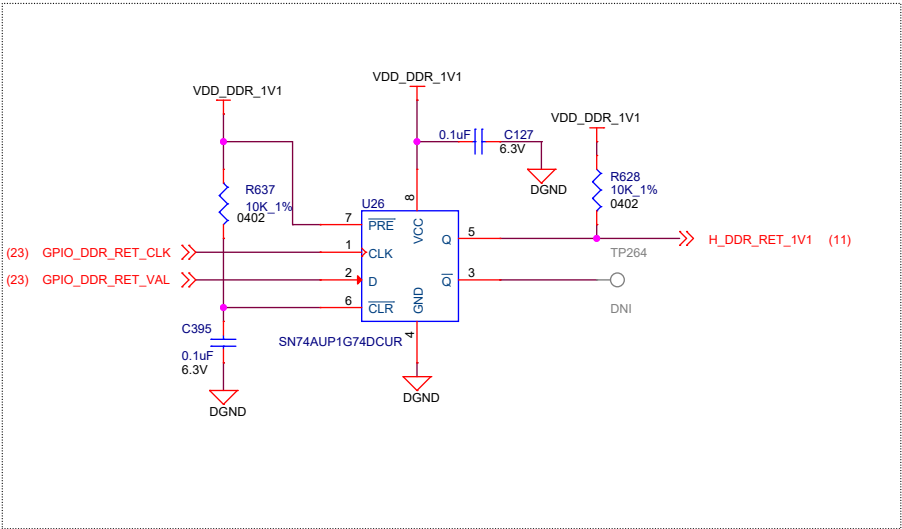
# CAN TRANSCEIVER



# EVM development & evaluation test circuitry

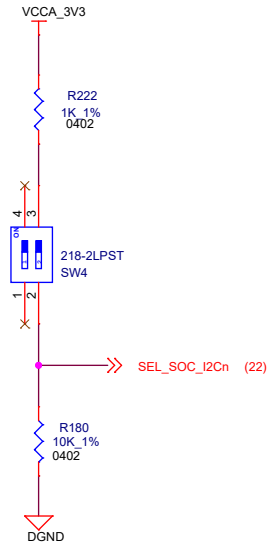
## (TI EVM Only)

LPDDR4X NOT SUPPORTED



To Enter DDR Retention:  
Set D to '1'  
Set CLK to '1'  
Set CLK to '0'

To Leave DDR Retention:  
Set D to '0'  
Set CLK to '1'  
Set CLK to '0'



SW4  
Pos1 - UNUSED  
Pos2 - ON/High = PMIC I2C to Ext header I2C (optional)  
OFF/Low = PMIC I2C to SoC WKUP I2C (default)

EVM Development & Evaluation test circuitry

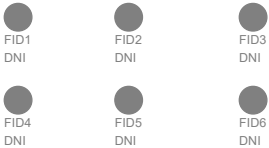
(TI EVM Only)

NOTES, HW & LABELS

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

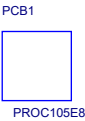
FIDUCIALS



SOCKET & PROCESSOR AS ACCESSORIES



BARE PCB



LABELS

Board Serial No.



Assembly Revision.



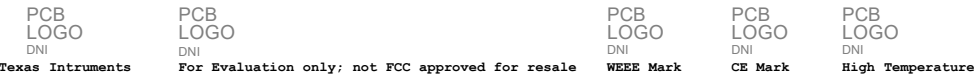
EVM Orderable No.



Orderable Part Numbers

Variant	Label Text
001 = Soldered GP SoC	J7200XSOMG01EVM
002 = Soldered HS SoC	J7200XSOMH01EVM
003 = Socketed SoC	J7200XSOMS01EVM

LOGOs



Project :

J7 EVM



Title  
HARDWARE SCHEMATICS

Size  
C  
PROC105 001 J7200XSOMG01EVM

Rev

E8

Date: Thursday, December 16, 2021

Sheet 33 of 34

# SI\_SIMULATION\_COUPON\_BD

Note: Test coupon not part of EVM design, to be used for TI test only

