REVISIONS		
REV #	DESCRIPTION	DATE
REV #	CCN #	DDMMYY

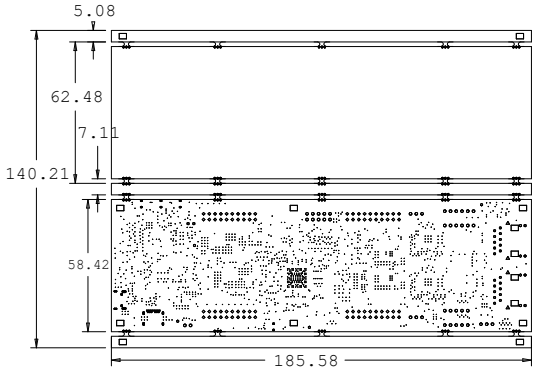
FABRICATION NOTES:

1. FABRICATE PCB IN ACCORDANCE WITH IPC-6012D, CLASS 2; PER IPC-6011.
2. MATERIALS:
   1. LAMINATE AND PREPREG SHALL BE IT-180A OR EQUIVALENT.
   2. COPPER FOIL TO BE IN ACCORDANCE WITH IPC-MF-150. UNLESS OTHERWISE SPECIFIED, ALL COPPER WEIGHT FOR INNER SIGNAL LAYERS AND INNER PLANE LAYERS TO BE 35UM (1 OZ.). FOR OUTER LAYERS 53UM (1.5 OZ). COPPER WEIGHT IS TO BE CONSIDERED "FINISHED". THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 6012B TABLE NO.3-7 AND 3-8.
3. ALL HOLES SHALL BE LOCATED WITHIN 0.15MM DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.125MM.
4. BOW AND TWIST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTH.
5. CONDUCTOR WIDTH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCASE FOR MATCHING IMPEDANCE MISTRAL SHALL APPROVE THE MODIFIED WIDTHS AND SPACING. TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
6. BOARD FINISHED SHALL BE ACCORDING TO IPC-6012D CLASS 2.
7. AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
8. FINISH:
   1. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG, ELECTROLESS NICKEL/IMMERSION GOLD, ELECTROLESS NICKEL SHALL BE 3-6 MICRONS, TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.04-0.06 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
   2. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-SM-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. VIA HOLES SHALL BE FILLED WITH NON CONDUCTIVE INK AND COVERED WITH SOLDER MASK. ONLY SOLDER MASK IMAGES THAT ARE 0.08(0.003") PER SIDE SHALL BE REDUCED IF REQUIRED. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED.SOLDER MASK SHALL BE RED.
   3. SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERABLE AREAS.
   4. SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 20UM [0.00079"], INCASE OF LASER VIA'S, BLIND VIA'S SHALL NOT BE LESS THAN 12UM [0.00047"] AND BURIED VIA'S SHALL NOT BE LESS THAN 15UM [0.0006"].
   5. ALL HOLES SURROUNDED BY LAND <=0.010" SHALL BE COMPLIANCE TO IPC6012, CLASS 2.
9. MARKING:
   1. BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
10. TEST REQUIREMENTS:
    1. 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-D-356 NET LIST FOR OPENS AND SHORTS.
11. THIEVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
12. TEAR DROPS SHALL BE ADDED ON VIA'S AND THROUGH HOLE PADS IN ALL INTERNAL AND OUTER LAYERS.
13. ALL UNCONNECTED VIA'S SHALL BE SUPPRESSED IF REQUIRED.
14. FINISHED PCB THICKNESS SHALL BE 0.0631" +/-10%.
15. MIN TRACE WIDTH/SPACING ON BOARD IS 0.0040"/0.0040".
16. FOR DETAILED STACK-UP, PROC109_STACK_UP.pdf SHALL BE REFERRED
17. ENSURE THAT UL REGISTERED E-FILE NUMBER SHALL BE PRINTED ON PCB SILKSCREEN.

DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILS

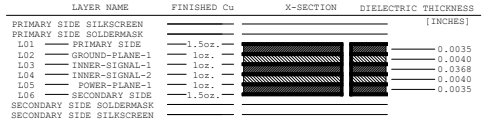
FIGURE	SIZE	TOLERANCE	PLATED	QTY
·	8.0	+3.0/-3.0	PLATED	1494
•	16.0	+3.0/-3.0	PLATED	14
•	36.0	+3.0/-3.0	PLATED	20
•	40.0	+3.0/-3.0	PLATED	14
⊙	44.0	+2.0/-2.0	PLATED	43
◆	46.0	+3.0/-3.0	PLATED	80
▲	66.0	+3.0/-3.0	PLATED	4
•	32.0	+2.0/-2.0	NON-PLATED	8
•	32.0	+3.0/-3.0	NON-PLATED	92
□	126.0	+3.0/-3.0	NON-PLATED	14
▬	48.0x22.0	+3.0/-3.0	PLATED	2
▮	48.0x24.0	+3.0/-3.0	PLATED	4
▬	68.0x34.0	+3.0/-3.0	PLATED	2



IMPEDANCE SPECIFICATIONS

SL#	TYPE	LAYER	TRACEWIDTH(Mils)	SPACING(Mils)	IMPEDANCE(Ohms)	REF LAYER
01	EDGE COUPLED MICROSTRIP	L6	4.1	6.8	120	L4
02	EDGE COUPLED MICROSTRIP	L1,L6	4.0	7.7	100	L2
03	EDGE COUPLED MICROSTRIP	L1,L6	4.2	5	90	L2
04	EDGE COUPLED STRIPLINE	L3	4.0	6	90	L2
05	STRIPLINE	L3	4.75	NA	50	L2
06	MICROSTRIP	L1,L6	5.3	NA	50	L2,L5

LAYER STACKUP



SIGNATURES		DATE
LAYOUT BY	PA	19-11-21
REVIEWED BY	EA	19-11-21
APPROVED BY	AMB	19-11-21

TEXAS INSTRUMENTS

PROC109E3

AM243x LP EVM

SIZE D

Rev E3

SCALE: NONE

SHEET 1 OF 13