

TDA4VM Edge AI Kit - DUAL TPS65941x PMICs

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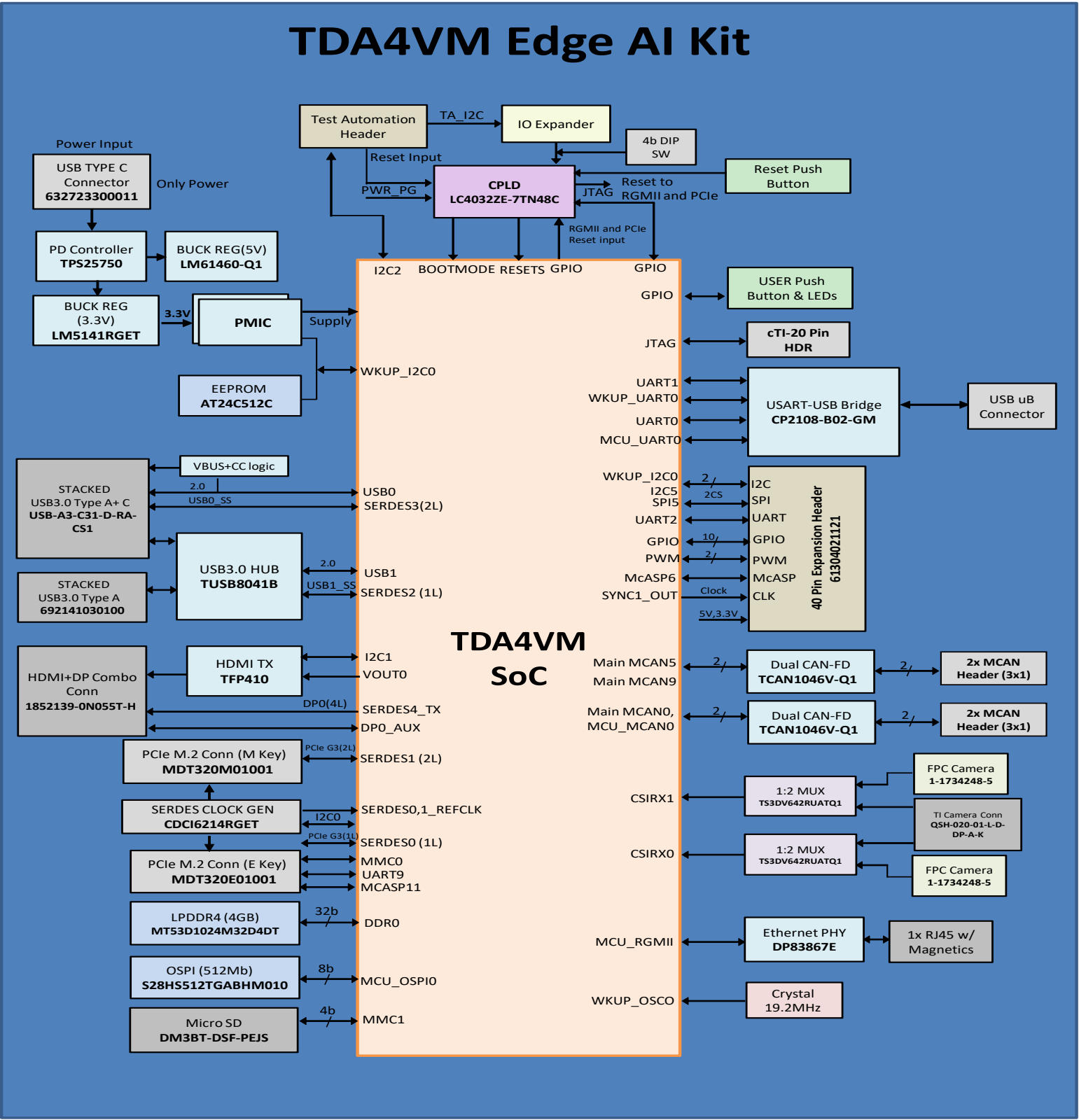
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REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E2	08 APR 2021	Drafted from E1 version	Mistral Design Team		
	08 APR 2021	Pin swapping done for D17 and D18	Mistral Design Team		
	30 APR 2021	Part# updated for Capacitor C356 from GCM155R71C104JA55D to GCM155R71C104KA55D DNI'd the Test points TP2 and TP6	Mistral Design Team		
	25 MAY 2021	Added Buffer U61 for OSPI reset signal Added Buffer U62 for PCIe M.2 E key Reset and wake signals Updated the PMIC-B, Buck-5 FB to "VDD_RAM_0V85_REG" before FL6/FL18 Changed the supply of CPLD device U38 and CPLD Programming header J7 to VSYS_MCUIO_1V8 Updated MCU Ethernet RJ45 connector J8 Mfr.Part # to LPJG16314A4NL and Added Indication LED circuit for 100Mbps speed	Mistral Design Team		
	27 MAY 2021	Connected MCU_PORz_OUT signal to CPLD Updated 25Mhz Crystal Y1 connected to Ethernet PHY to Mfr.Part# ECS-250-18-23A-JGN-TR Added Test points TP66,TP67,TP68 and TP69 for reset signals to RGMII, PCIe M.2 E and M key signals	Mistral Design Team		
	31 MAY 2021	Updated USB Stacked TYPE 3.0 Conn to Mfr.Part# 484060003 Updated for Internal Review Comments	Mistral Design Team		
	01 JUN 2021	Updated USB 3.0 Hub Upstream port super speed lines	Mistral Design Team		
	02 JUN 2021	Updated for TI review comments(Partiallly)	Mistral Design Team		
	03 JUN 2021	Updated for internal review comments	Mistral Design Team		
	04 JUN 2021	Added Serdes reference clock generator for PCIe	Mistral Design Team		
	07 JUN 2021	Updated for internal review comments	Mistral Design Team		
	10 JUN 2021	Component package optimized for CDCI SEDES Clock section for PCB routing ease	Mistral Design Team		
	11 JUN 2021	Updated the Part# for FL26, FL27, FL28 FL29 to NFM15PC474R0J3D	Mistral Design Team		
	17 JUN 2021	Replaced 2-T, 0.1uF 0201 cap C409 to 3-T, 1uF 0402 Removed 2-T, 0.1uF 0201 cap C414	Mistral Design Team		
	22 JUN 2021	Updated notes for Silkscreen Connected VDDA_1P8_DSITX filtered supply to VDDA_1P8_MLB power group Connected VDDA_0P8_USB filtered supply to VDDA_0P8_UFS power group	Mistral Design Team		
	23 JUN 2021	Pin Swapping done for HDMI common mode choke and ESD diode U28 for routing ease	Mistral Design Team		
	25 JUN 2021	Updated part GCM31CD70G476ME to complete part number GCM31CD70G476ME02 Updated part GCM033C70J104K to complete part number GCM033C70J104KE02D Changed part RCA04060000Z0EALS alternate part RCL04060000Z0EA Changed part PNM0402E5000BST1 (500E) to RC0402FR-07499RL Pin Swapping done for HDMI common mode choke and ESD diode U28 for routing ease	Mistral Design Team		
	06 JUL 2021	Changed I2C Bootmode buffer address to 0x20h (R152 connected to GND) DNI'd decaps C655 and C656	Mistral Design Team		
	13 JUL 2021	Updated power flow block diagram	Mistral Design Team		
	21 JUL 2021	Baselined	Mistral Design Team		
E3	14 OCT 2021	Changed R249 and R261 from 22E to 0E resistor Added Test points for VDA_MCU_1V8, VDA_USB_3V3, VDA_PLL_1V8, VDD_RAM_0V85_REG supplies Added TVS2200 at USB Type C input for ESD protection Changed C155,C148, C149 to 22uf Populated C150 with 10uf tripad cap of Mfr.Part# NFM18HC106D0G Populated C147,C154 with 10uf 0603 cap of Part# GRT188C81C106ME13D	Mistral Design Team		
	15 OCT 2021	Changed C150 to Mfr.Part# GRT188C81C106ME13D	Mistral Design Team		
A	20 OCT 2021	Changed C625 and C626 to HHXA500ARA680MHA0G Changed Board Revision to REV A	Mistral Design Team		
	25 OCT 2021	Changed C625 and C626 to UT107M050HFKTA Changed 9774015243R to accessory Baselined	Mistral Design Team		
A1	04 APR 2022	Changed L15 , R134, R123, C268, C272 for increased load current	Mistral Design Team		

SYSTEM BLOCK DIAGRAM



3-Phase DUAL PMIC Recommended for New Designs
(3-Phase Buck supplying VDD_CPU)

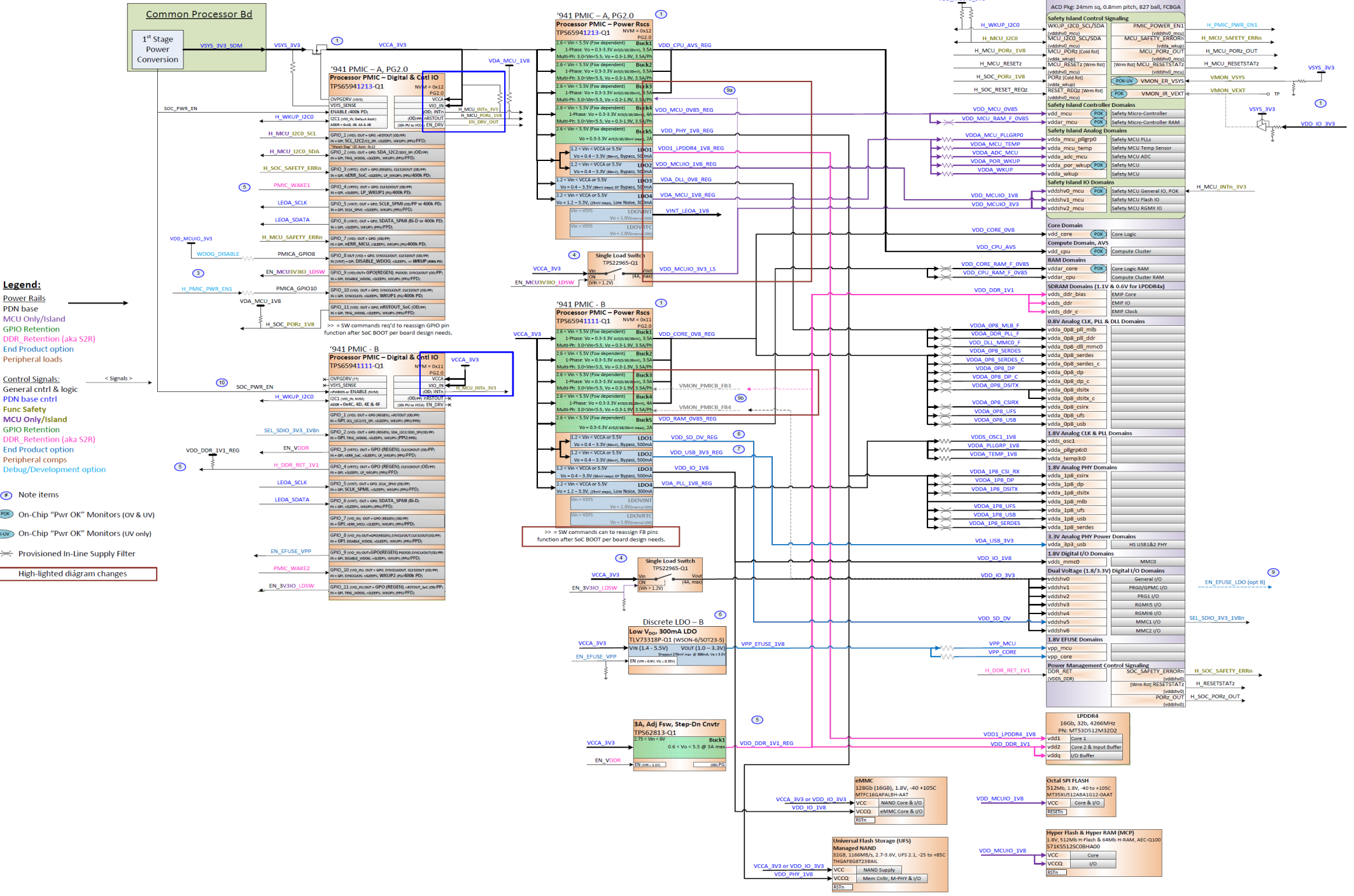
DRA829/TDA4VM 3-Phase Dual Leo2.0 PDN-OC
(Power Rail & GPIO Mapping Overview)

Leo PMIC-A, PN TPS65941213RWERQ1 (TI PN ID = 1, MP Buck Rails = 2, NVM ID = 13, PG2.0)
Leo PMIC-B, PN TPS65941111RWERQ1 (TI PN ID = 1, MP Buck Rails = 2, NVM ID = 12, PG2.0)

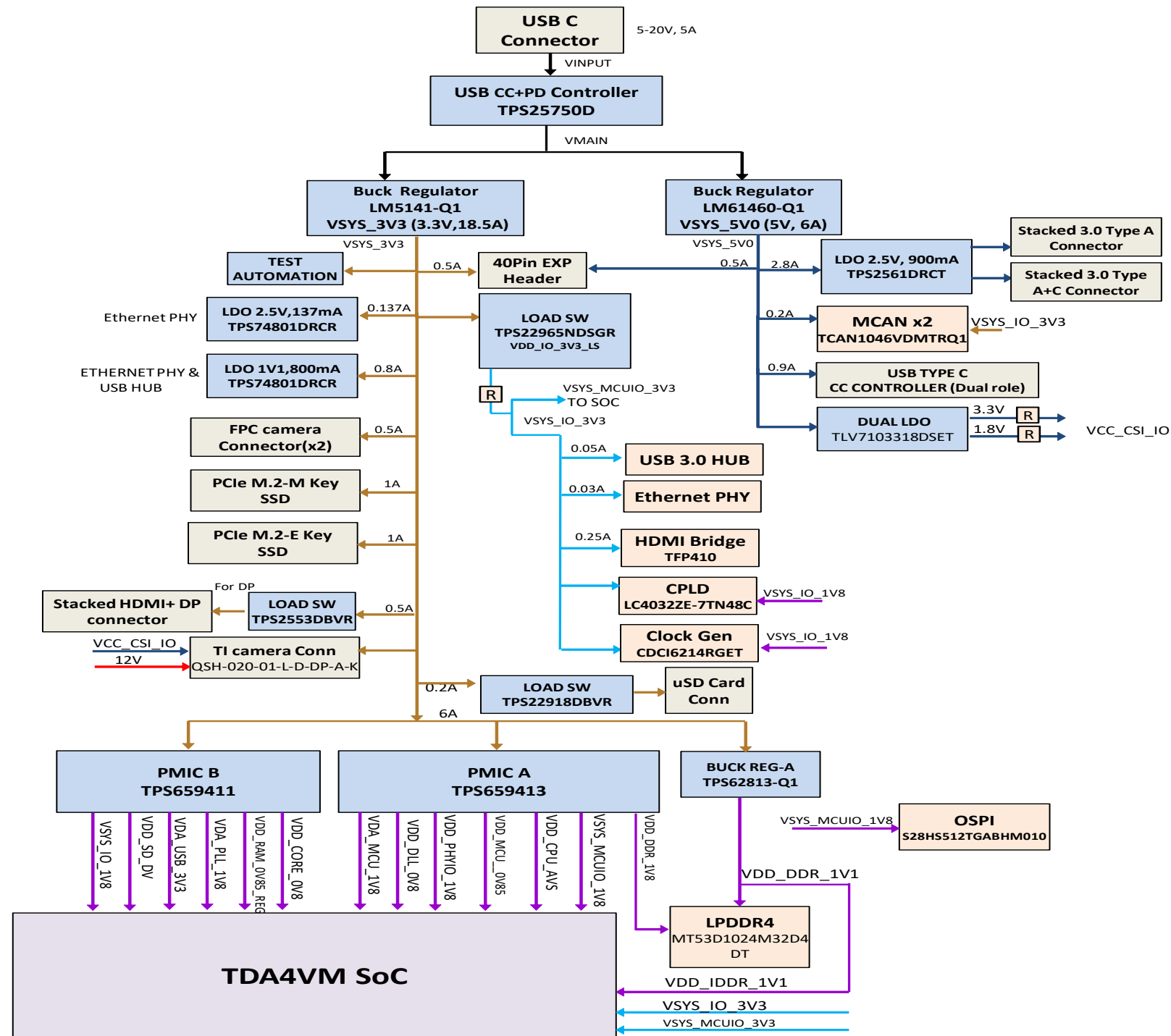
Features Supported (EVM Max Features):

- 1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
- 2. Functional Safety: ASIL-D capable system with independent MCU & Main power for FFI
- 3. SDRAM: 32Gb, 4-Die, 32b, 4266MTs, LPDDR4 mode
- 4. Boot & Mass Flash: Octal SPI or Hyperflash (SR1.1 only) & eMMC, UFS
- 5. Low power modes: MCU Only & DDR Retention
- 6. Signaling Levels: MCU & Main Dual VIO
- 7. End Product Options:
a. Compliant high-speed SD Card
b. Compliant USB 2.0 data eye
c. HS SoC Efuse programming on-board

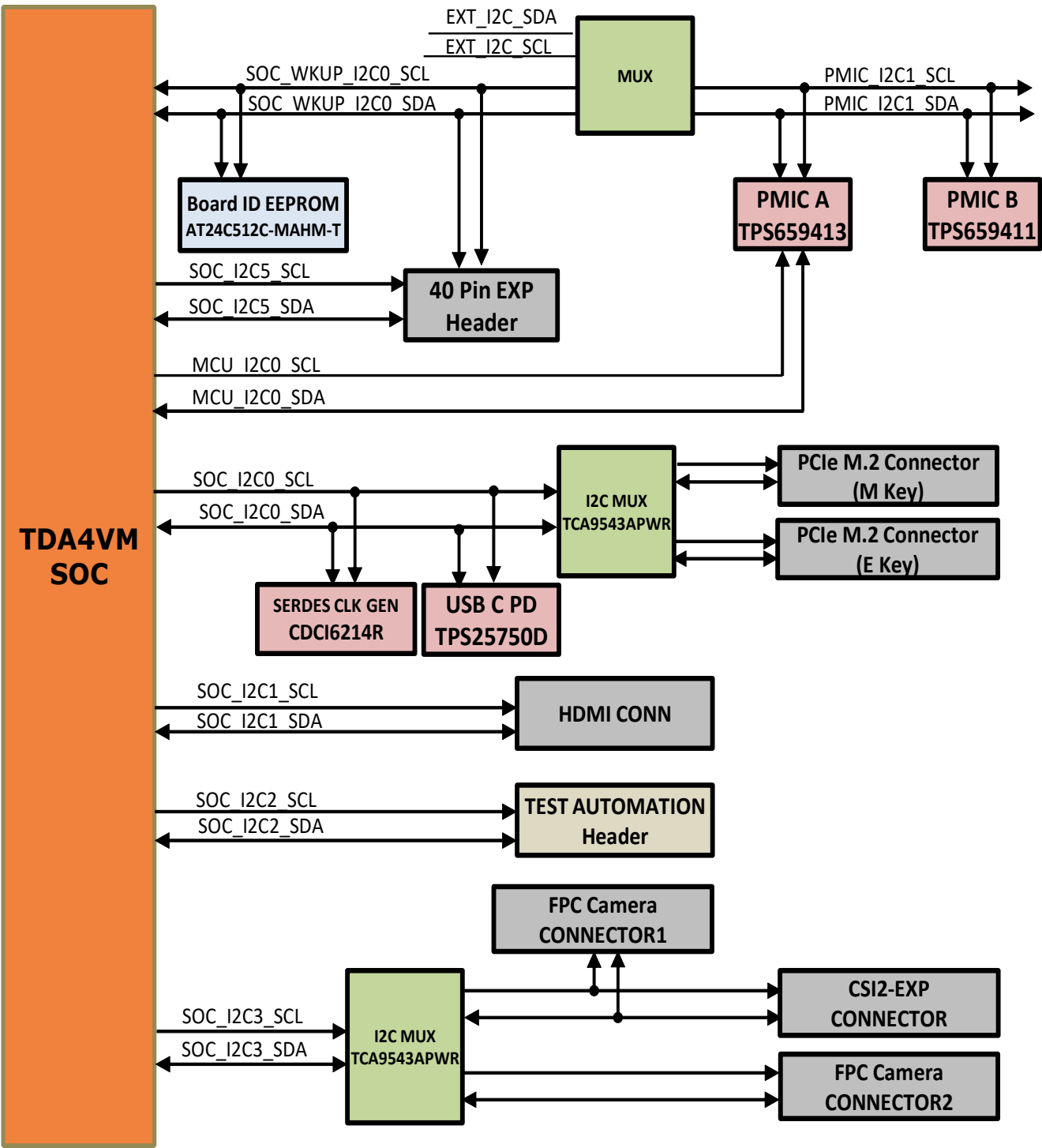
- VO.14 1/27/2021
1. Added example of VDD_IO_3V3 OV/UV monitoring by SoC's VMON_IR_VEXT input connection option to voltage buffer & voltage R-div needed to interface with SoC's internal R-div network optimized for monitoring 1.8V power rails.
2. Added 2x ext voltage monitoring inputs options for OV/UV monitoring by Hera PMIC of any safety critical system power rails. Hera's quad buck config can reassign remote sense feedback inputs (FB3 & FB4) for power rail monitoring.
3. Updated notes 1 & 9 accordingly.
- VO.15 2/13/2021
Following final PMIC NVM review for defining new common PN ("1213") for Leo PG2.0 used in PDN-OC & -1A:
1. Update notes
2. Changed PMIC-A FB3 VMON input to be connected to VCCA_3V3 since VDD_MCUIO_3V3 rail is not supported, see note 9a.
3. Added PMIC-B FB3 & FB4 assignment for VMON by SW after SoC boot for ext power rail monitoring options, see note 9b.
- VO.16 3/2/2021
1. Removing discrete load switch from supplying PMIC's VIO_IN since PG2.0 PMICs validation testing confirms no excessive glitches on GPIO or reset signals during of NVM initialization. Related "Note #2" has been removed.



POWER FLOW DIAGRAM



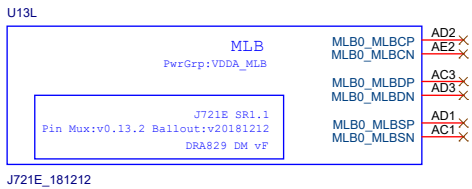
I2C TREE



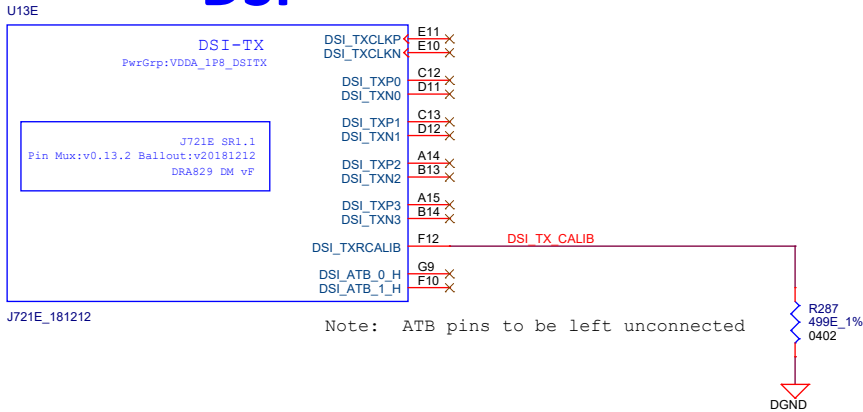
GPIO MAPPING TABLE

GPIO Mapping							
Package Signal Name	GPIO	Net name	Input/Output	IO Level	Default	State	Remarks
WKUP Domain							
WKUP_GPIO0_3	WKUP_GPIO0_3	MCU_MCAN0_STB	Output	3.3V	NA	Active High	MCU CAN0 Standby
WKUP_GPIO0_4	WKUP_GPIO0_4	SOC_WAKE	Input	3.3V	PU	NA	SoC wake signal
WKUP_GPIO0_5	WKUP_GPIO0_5	BOARDID_EEPROM_WP	Output	3.3V	PD	Active High	Boot EEPROM Write protect
WKUP_GPIO0_6	WKUP_GPIO0_6	SOC_INT2z	Input	3.3V	PU	Active low	SOC Interrupt
WKUP_GPIO0_7	WKUP_GPIO0_7	H_MCU_INT#	Input	3.3V	PU	NA	MCU domain Interrupt
WKUP_GPIO0_8	WKUP_GPIO0_8	GPIO_uSD_PWR_EN	Output	3.3V	PU	Active High	GPIO for micro SD card power load switch power enable
WKUP_GPIO0_9	WKUP_GPIO0_9	SEL_SDIO_3V3_1V8n	Output	3.3V	PU	Active low	VDD_SD_DV 1.8V or 3.3V selection control
MCU_OSPI1_DQS	WKUP_GPIO0_31	MCU_OSPI0_INT#	Output	1.8V	PU	Active low	OSPI Interrupt Pin
WKUP_GPIO0_10	WKUP_GPIO0_10	GPIO_RGMII3_RST#	Output	3.3V	NA	Active low	Used as a reset signal for PRG0 Ethernet PHY Chip
WKUP_GPIO0_11	WKUP_GPIO0_11	SOC_PCl_e1_M.2_RTSz	Output	3.3V	NA	NA	PCle M.2 M key reset signal
MCU_OSPI1_D0	WKUP_GPIO0_32	CPLD_TCK	I/O	1.8V	PD	NA	JTAG Signals for CPLD
MCU_OSPI1_D1	WKUP_GPIO0_33	CPLD_TDI	I/O	1.8V	NA	NA	JTAG Signals for CPLD
MCU_OSPI1_D2	WKUP_GPIO0_34	CPLD_TDO	I/O	1.8V	NA	NA	JTAG Signals for CPLD
MCU_OSPI1_D3	WKUP_GPIO0_35	CPLD_TMS	I/O	1.8V	PU	NA	JTAG Signals for CPLD
MCU_OSPI1_CSN0	WKUP_GPIO0_36	M2_SDIO_RESET#	Output	1.8V	PU	Active low	Reset to SDIO(WiFi) Interface for PCle M.2 E key
MCU_OSPI1_CSN1	WKUP_GPIO0_37	M2_SDIO_WAKE#	Output	1.8V	PU	Active low	Wake to SDIO(WiFi) Interface for PCle M.2 E key
MCU_SPI0_CS0	WKUP_GPIO0_55	SYS_MCU_PWRDN	Output	3.3V	PD	Active High	System Power Down ('0' - normal operation, '1' - system power down)
PMIC_POWER_EN0	WKUP_GPIO0_66	RGMII_INT#	Input	3.3V	PU	NA	Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
Main Domain							
PRG1_PRU0_GPO4	GPIO0_5	40 Pin EXP Hdr - GPIO1	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
PRG1_PRU0_GPO6	GPIO0_7	40 Pin EXP Hdr - GPIO2	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
PRG1_PRU0_GPO7	GPIO0_8	40 Pin EXP Hdr - GPIO3	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
PRG1_PRU0_GPO10	GPIO0_11	40 Pin EXP Hdr - GPIO4	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
PRG0_PRU1_GPO8	GPIO0_71	40 Pin EXP Hdr - GPIO5	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
PRG0_PRU1_GPO19	GPIO0_82	40 Pin EXP Hdr - GPIO6	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
RGMII6_TX_CTL	GPIO0_97	40 Pin EXP Hdr - GPIO7	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
SPI0_D1	GPIO0_115	40 Pin EXP Hdr- GPIO8	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
PRG0_PRU0_GPO18	GPIO0_61	M.2_W_DISABLE1#	Output	3.3V	PU	Active low	WiFi disable1 signal for PCle M.2 E key
PRG0_PRU0_GPO19	GPIO0_62	M.2_W_DISABLE2#	Output	3.3V	PU	Active low	WiFi disable2 signal for PCle M.2 E key
PRG0_PRU1_GPO1	GPIO0_64	USER_LED1	Output	3.3V	PD	Active High	USER LED enable signal
PRG0_PRU1_GPO2	GPIO0_65	MCAN0_STB	Output	3.3V	NA	Active High	MCAN0 Standby
PRG0_PRU1_GPO3	GPIO0_66	MCAN5_STB	Output	3.3V	NA	Active High	MCAN5 Standby
PRG0_PRU1_GPO4	GPIO0_67	MCAN9_STB	Output	3.3V	NA	Active High	MCAN9 Standby
PRG0_PRU1_GPO9	GPIO0_72	SOC_PCl_e0_M.2_RTSz	Output	3.3V	NA	NA	PCle M.2 E key reset signal
PRG0_PRU1_GPO11	GPIO0_74	GPIO0_74	Output	3.3V	NA	NA	CSI2 Expansion Board Specific.
PRG0_PRU1_GPO12	GPIO0_75	GPIO0_75	Output	3.3V	NA	NA	CSI2 Expansion Board Specific.
PRG0_PRU1_GPO13	GPIO0_76	GPIO0_76	Output	3.3V	NA	NA	CSI2 Expansion Board Specific.
PRG0_PRU1_GPO14	GPIO0_77	GPIO0_77	Output	3.3V	NA	NA	CSI2 Expansion Board Specific.
PRG0_PRU1_GPO15	GPIO0_78	GPIO0_78	Output	3.3V	NA	NA	CSI2 Expansion Board Specific.
PRG0_PRU1_GPO16	GPIO0_79	GPIO0_79	Output	3.3V	NA	NA	CSI2 Expansion Board Specific.
SPI0_CS0	GPIO0_111	DP0_3V3_EN	Output	3.3V	PD	Active High	Display Port Load Switch enable
SPI1_CS0	GPIO0_116	SOC_CAM0_GPIO1	I/O	3.3V	NA	NA	FPC Camera0 GPIO
SPI1_CS1	GPIO0_117	SOC_CAM0_GPIO2	I/O	3.3V	NA	NA	FPC Camera0 GPIO
SPI1_CLK	GPIO0_118	CSI_VIO_SEL	Output	3.3V	PD	Active High	CSI Dual IO selection
SPI1_D0	GPIO0_119	SOC_CAM1_GPIO1	I/O	3.3V	NA	NA	FPC Camera1 GPIO
SPI1_D1	GPIO0_120	SOC_CAM1_GPIO2	I/O	3.3V	NA	NA	FPC Camera1 GPIO
UART1_CTSN	GPIO0_127	HDMI_PDN	Output	3.3V	PD	Active low	HDMI power down signal
UART1_RTSN	GPIO1_0	HDMI_HPD	Input	3.3V	NA	NA	HDMI hot plug detect
RGMII5_TD2	GPIO0_88	CSI_MUX_SEL_2	Output	3.3V	PD	NA	CSI I2C MUX select(default 1.8V)
RGMII5_TD3	GPIO0_87	HDMI_LS_OE	Output	3.3V	PU	Active low	Enable signal for supply load switch for HDMI Connector
RGMII5_RD1	GPIO0_95	BT_UART_WAKE#	Output	3.3V	PU	Active low	Wake signal for Bluetooth(PCle M.2 E key)
MCAN1_RX	GPIO1_3	USBC_DIR	Input	3.3V	PU	NA	USB C direction indication(Low-Position 1,High-Position 2)

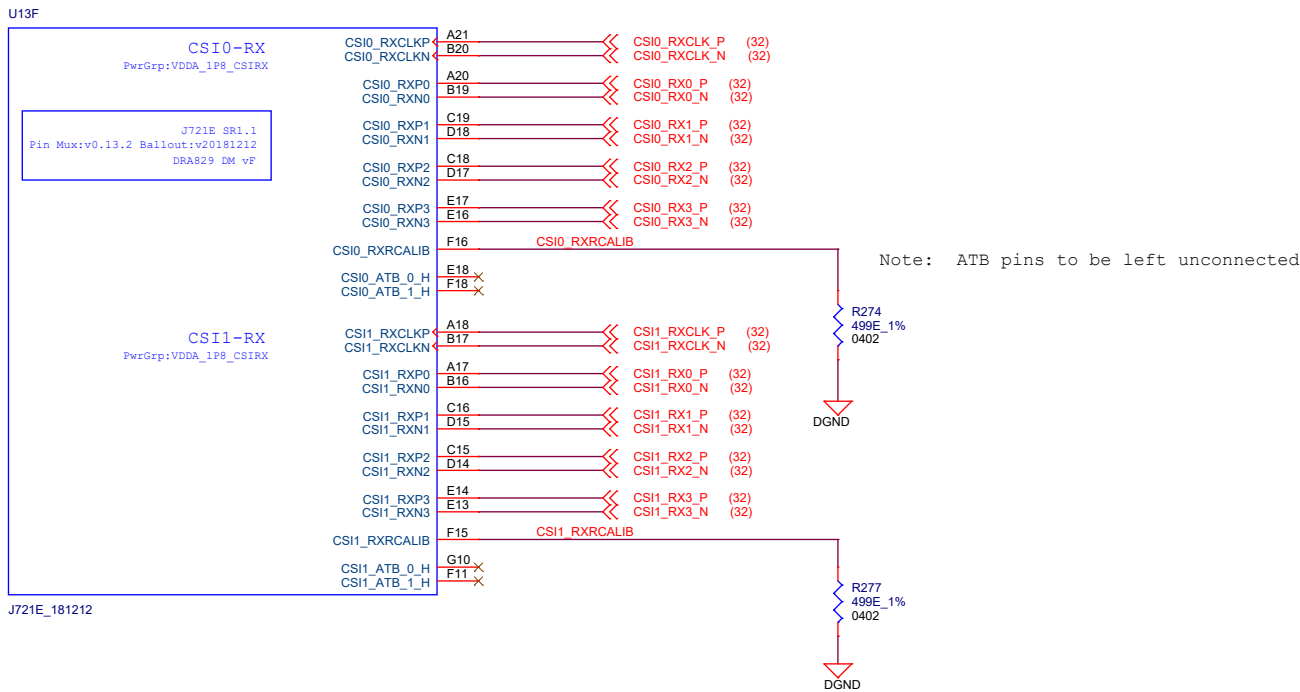
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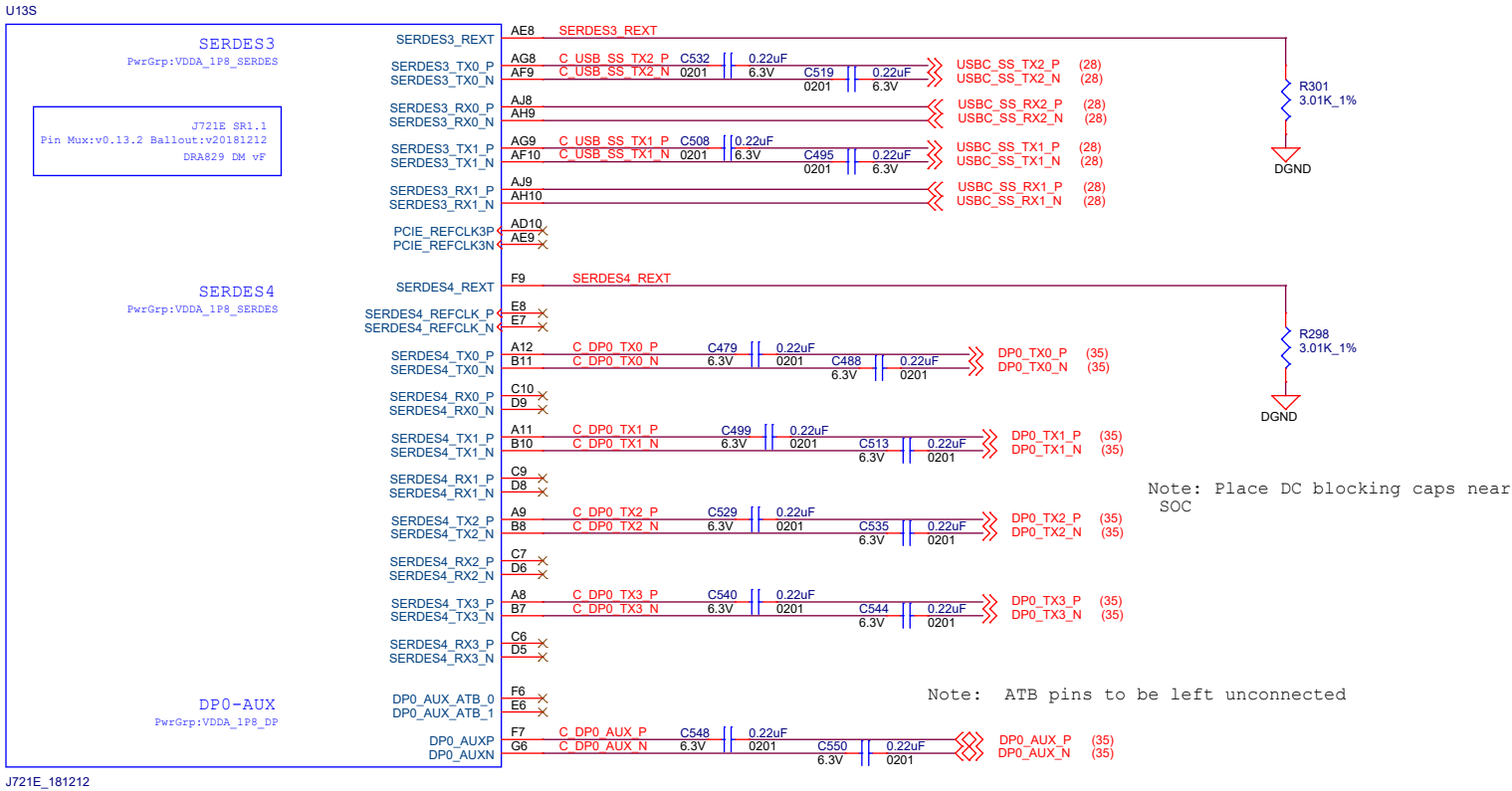
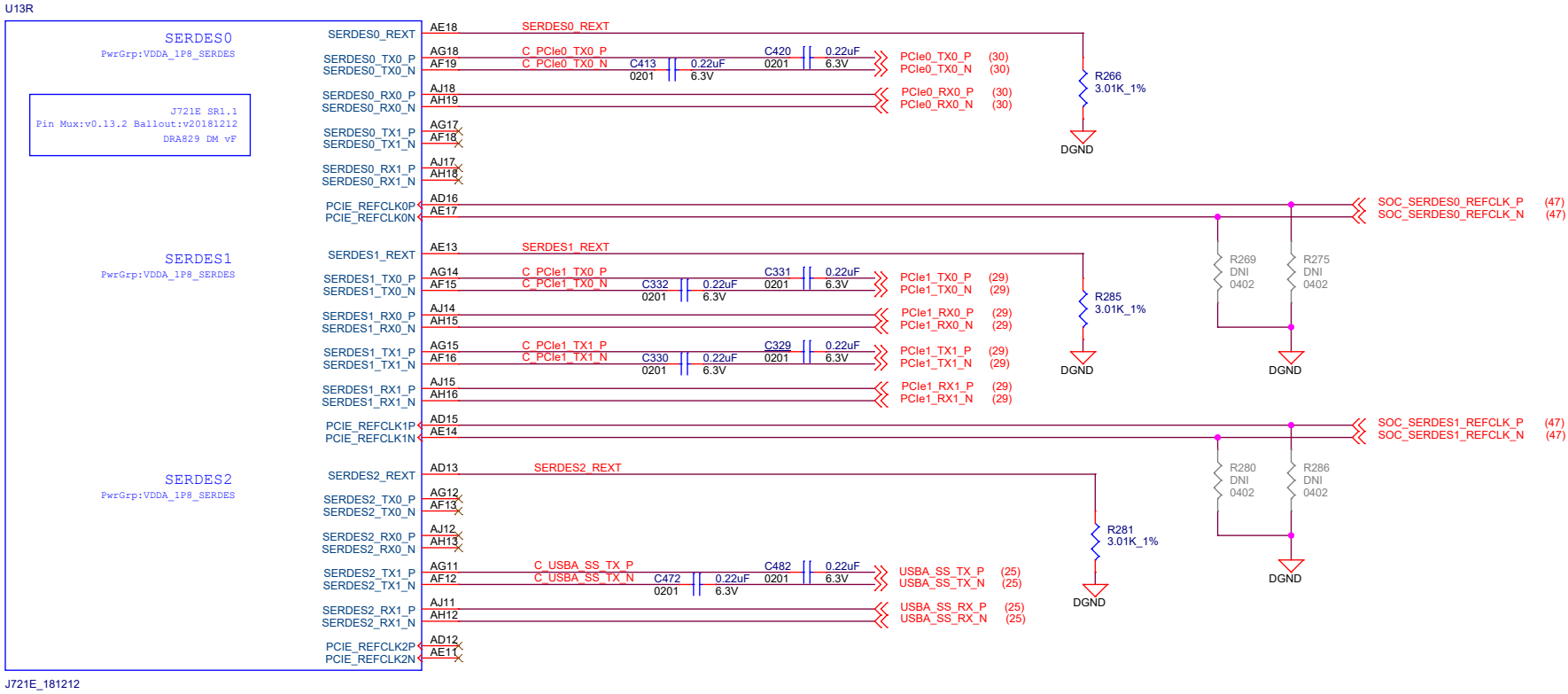
DSI



CSI Interface



SERDES



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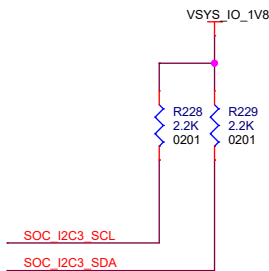
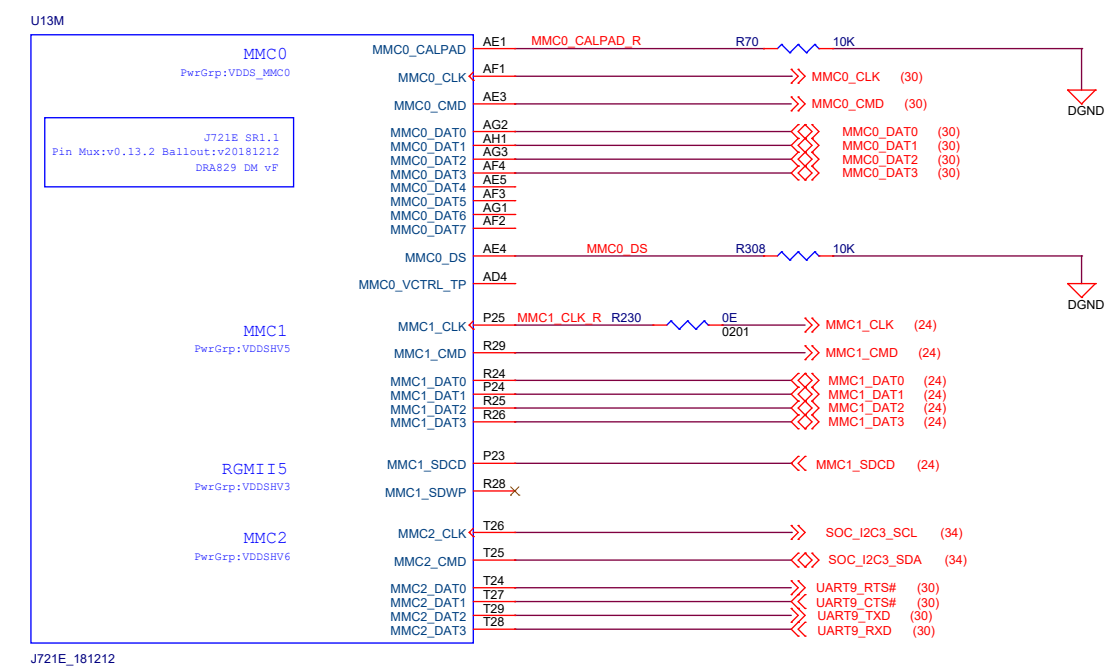
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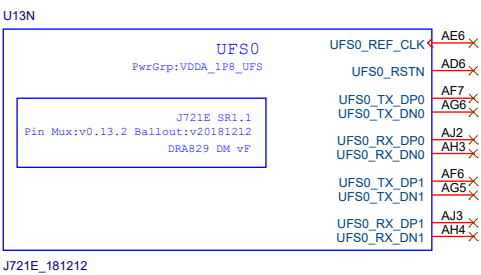
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MMC Interface



UFS Interface



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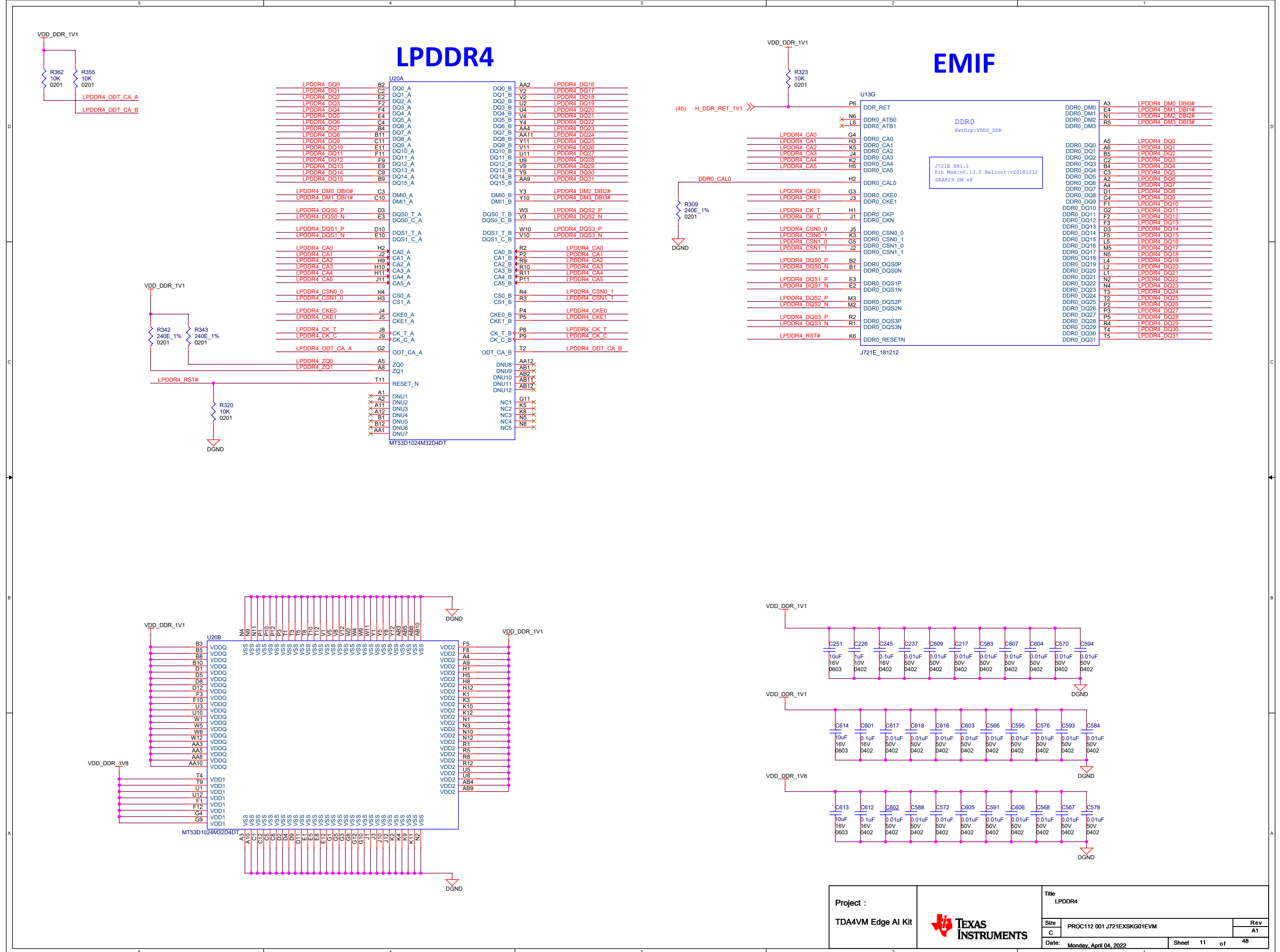
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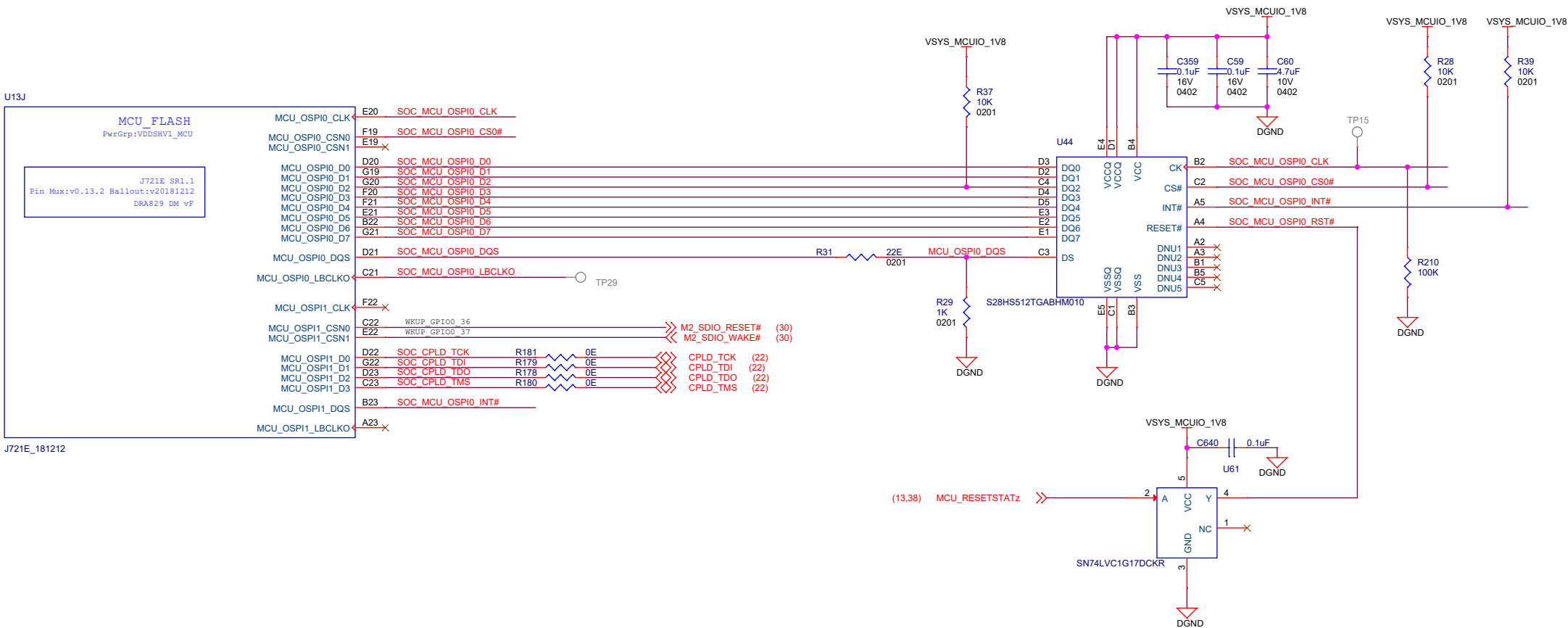
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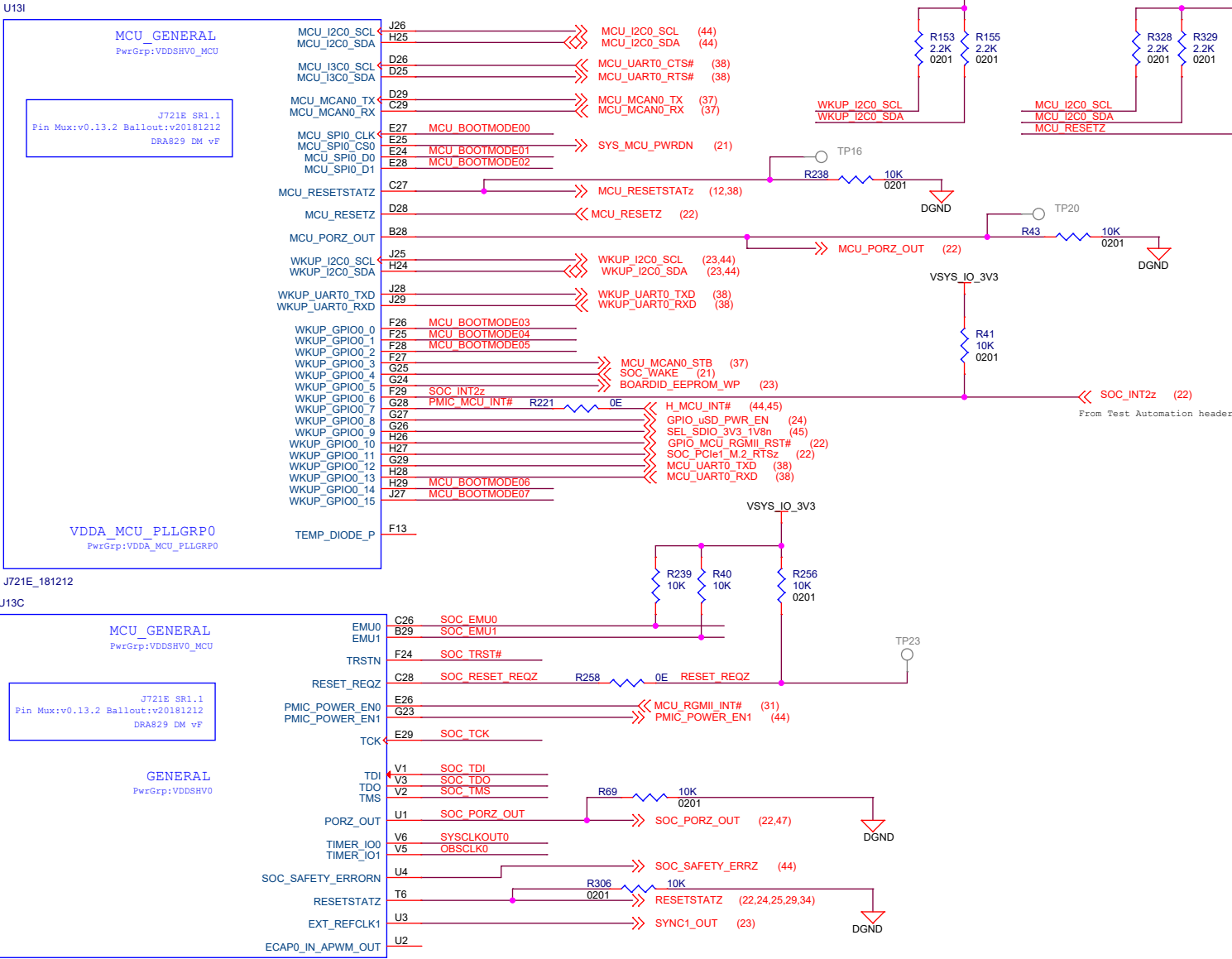


MCU FLASH

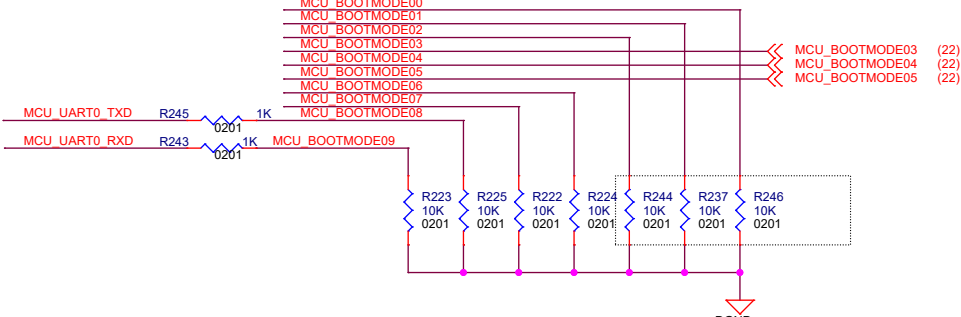
OSPI FLASH



MCU & MAIN GENERAL IO, OSC CLKS

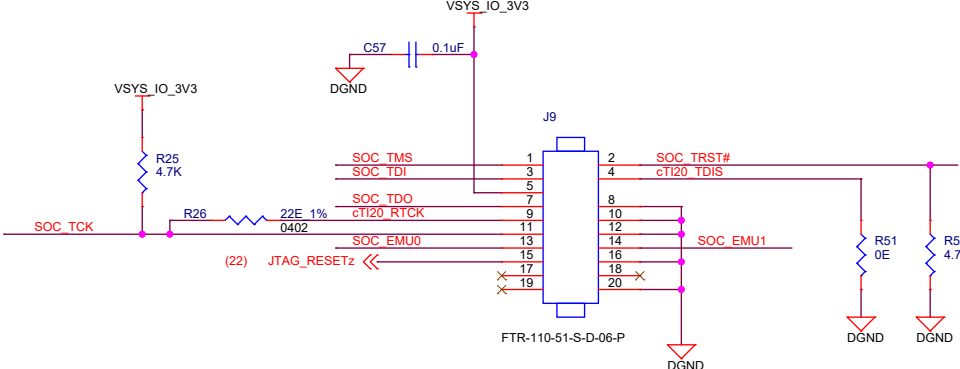


Default state of the bootmode pins from CPLD are pulled down

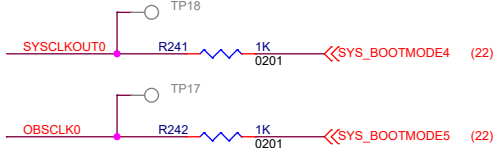
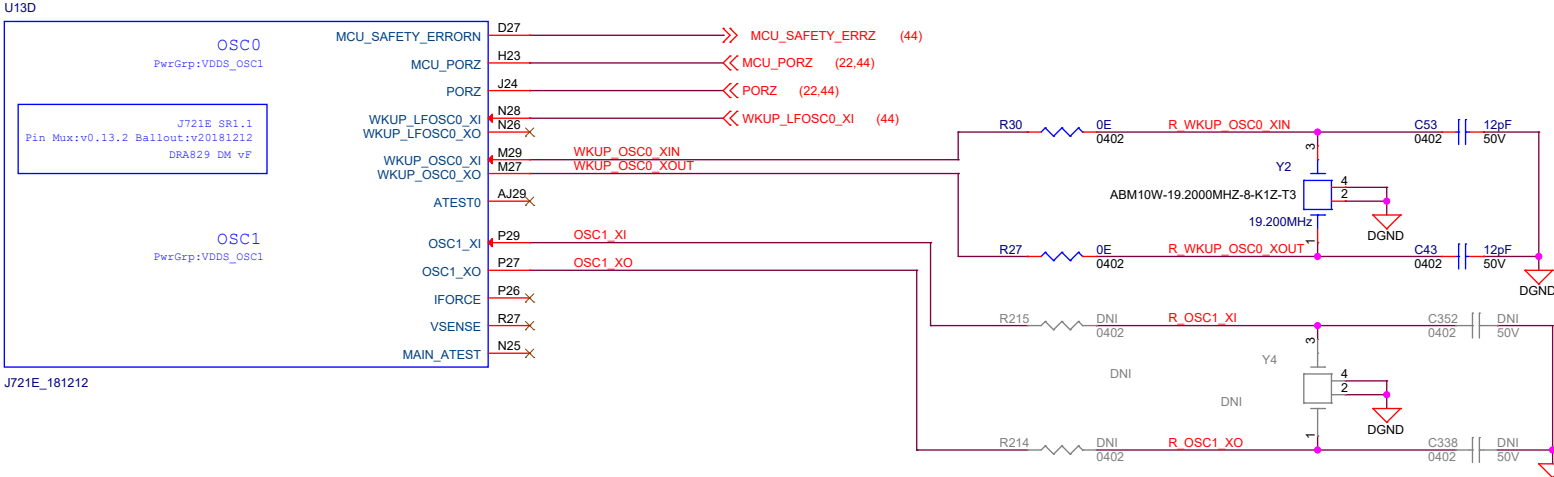


Note: MCU_BOOTMODE[2:0] set to '000' for 19.2MHz input frequency.

cTI 20PIN JTAG HEADER



OSC



SOC PORZ OUT
RESETSTATZ

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TDA4VM Edge AI Kit



SOC_GENERAL&MCU_GENERAL

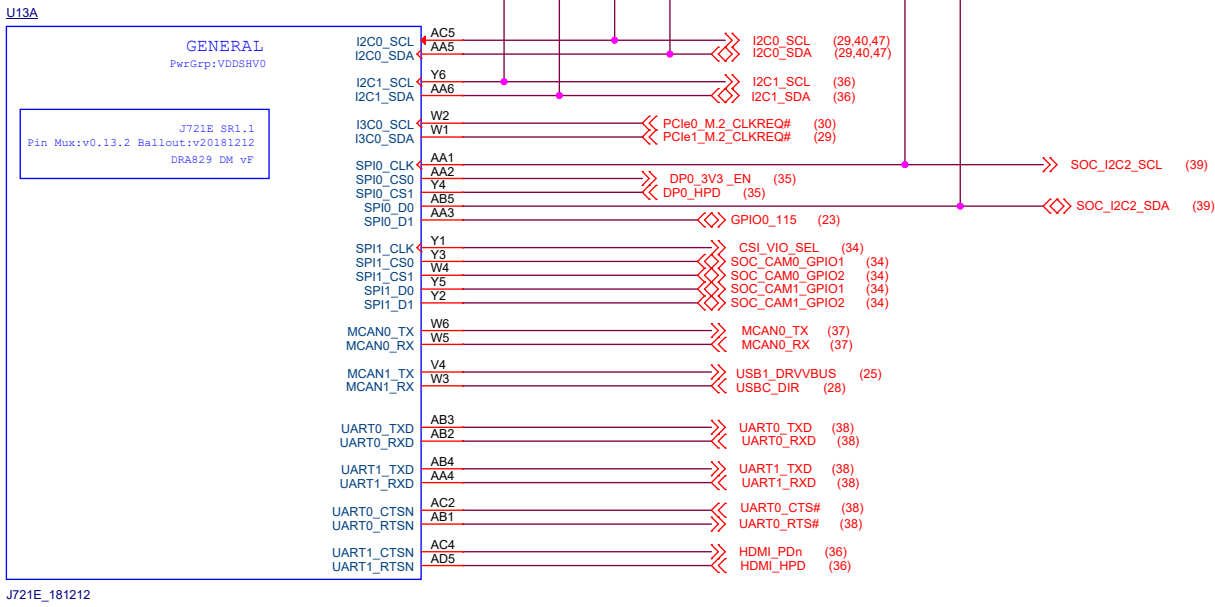
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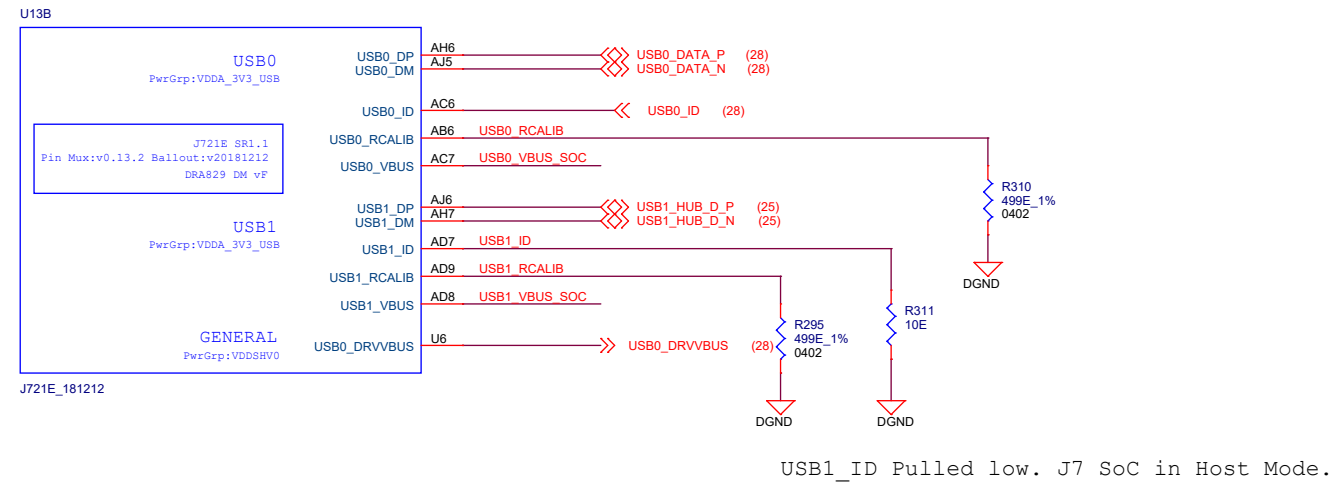
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GENERAL

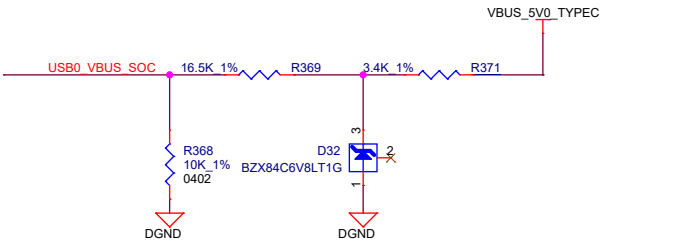


USB

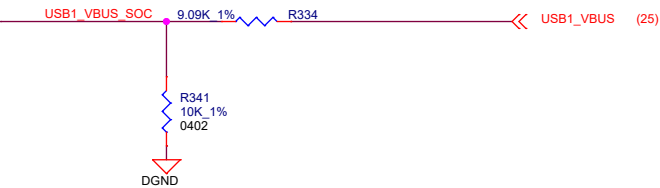


USB VBUS Resistor divider circuit

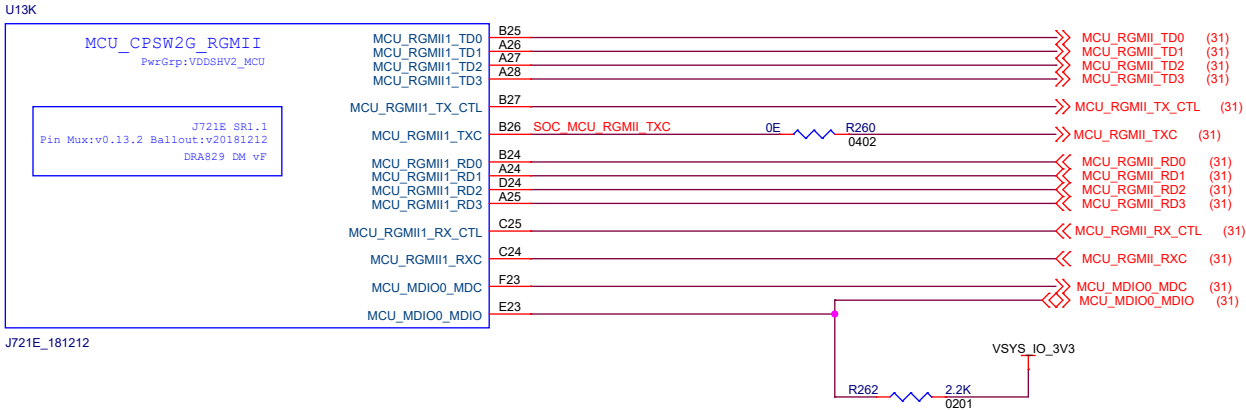
Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS



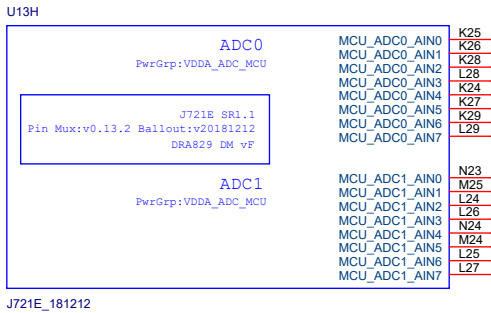
Note: Recommended VBUS circuit for embedded Hub



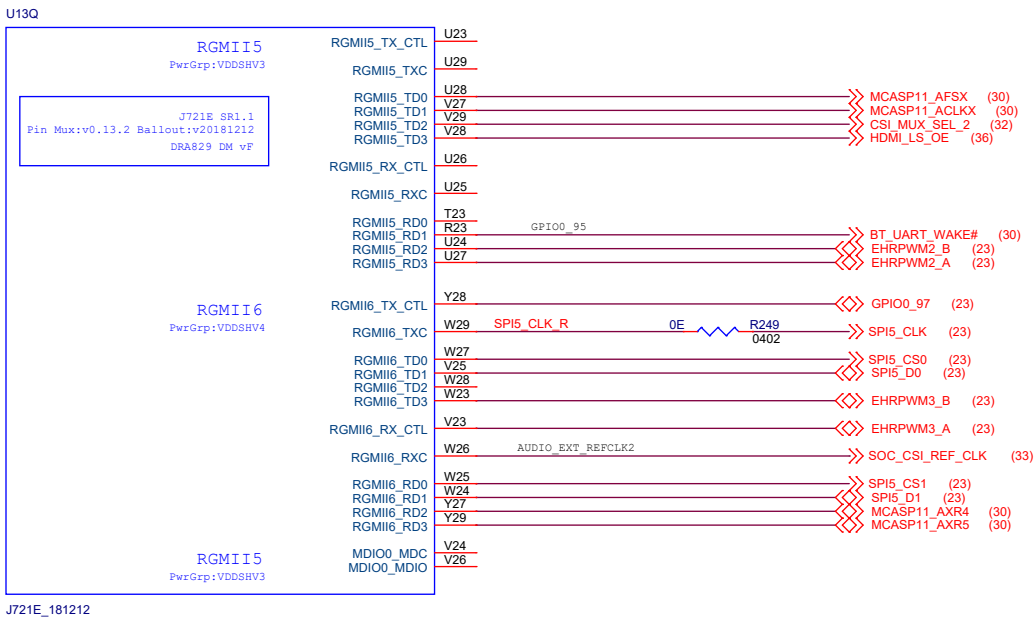
MCU_RGMII



MCU ADCs



MAIN RGMII

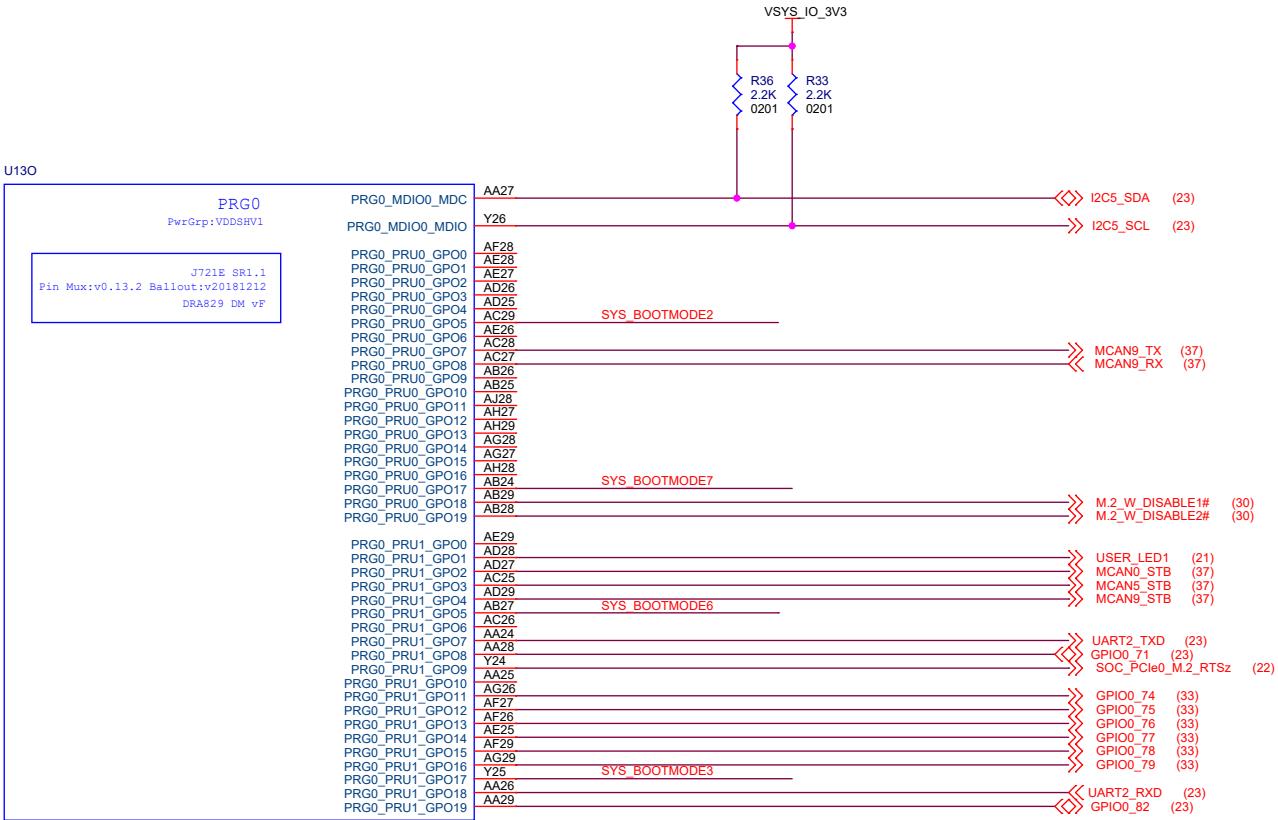


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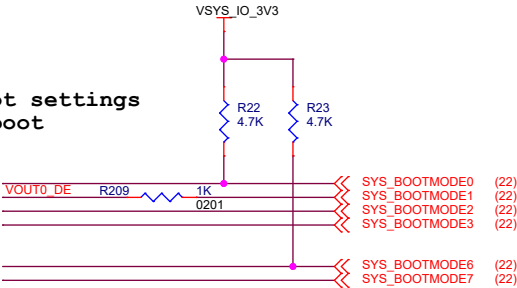


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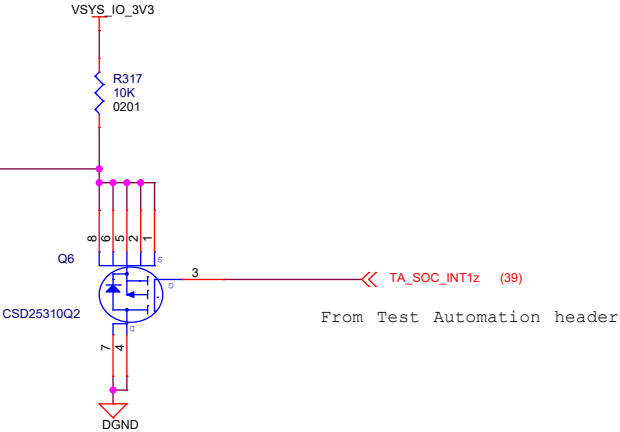
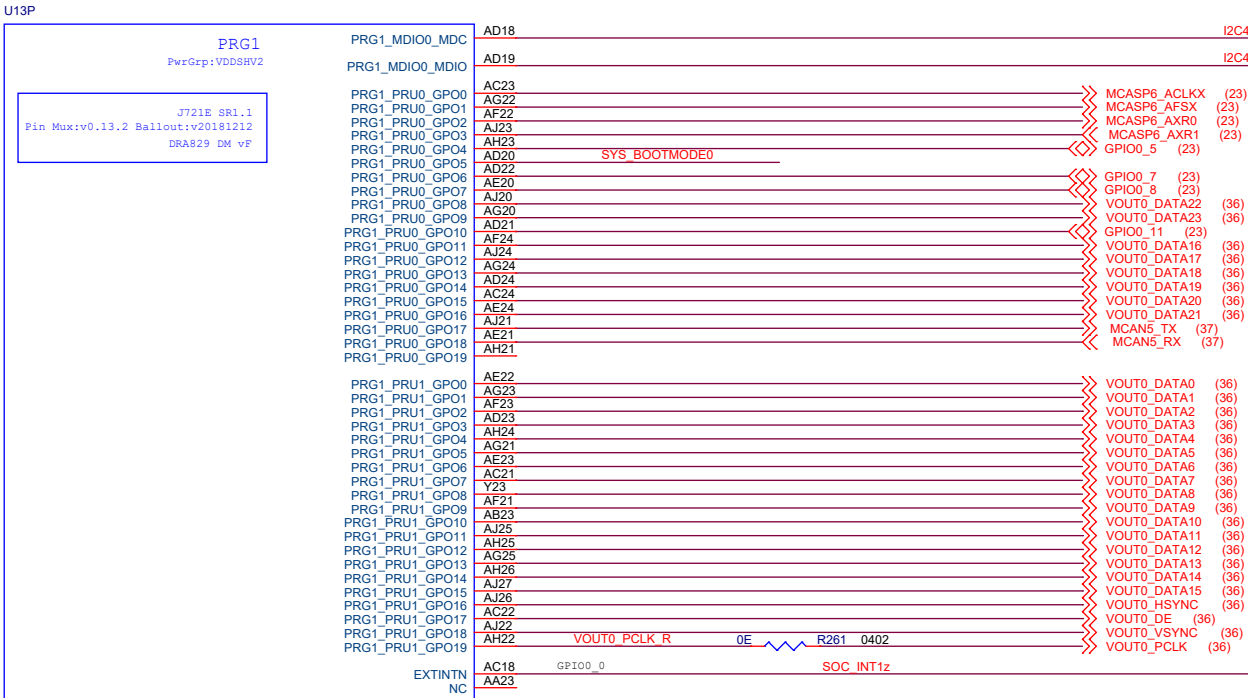
PRG0 & PRG1



Default Boot settings
set to SD boot



Default state of the bootmode pins from CPLD are pulled down

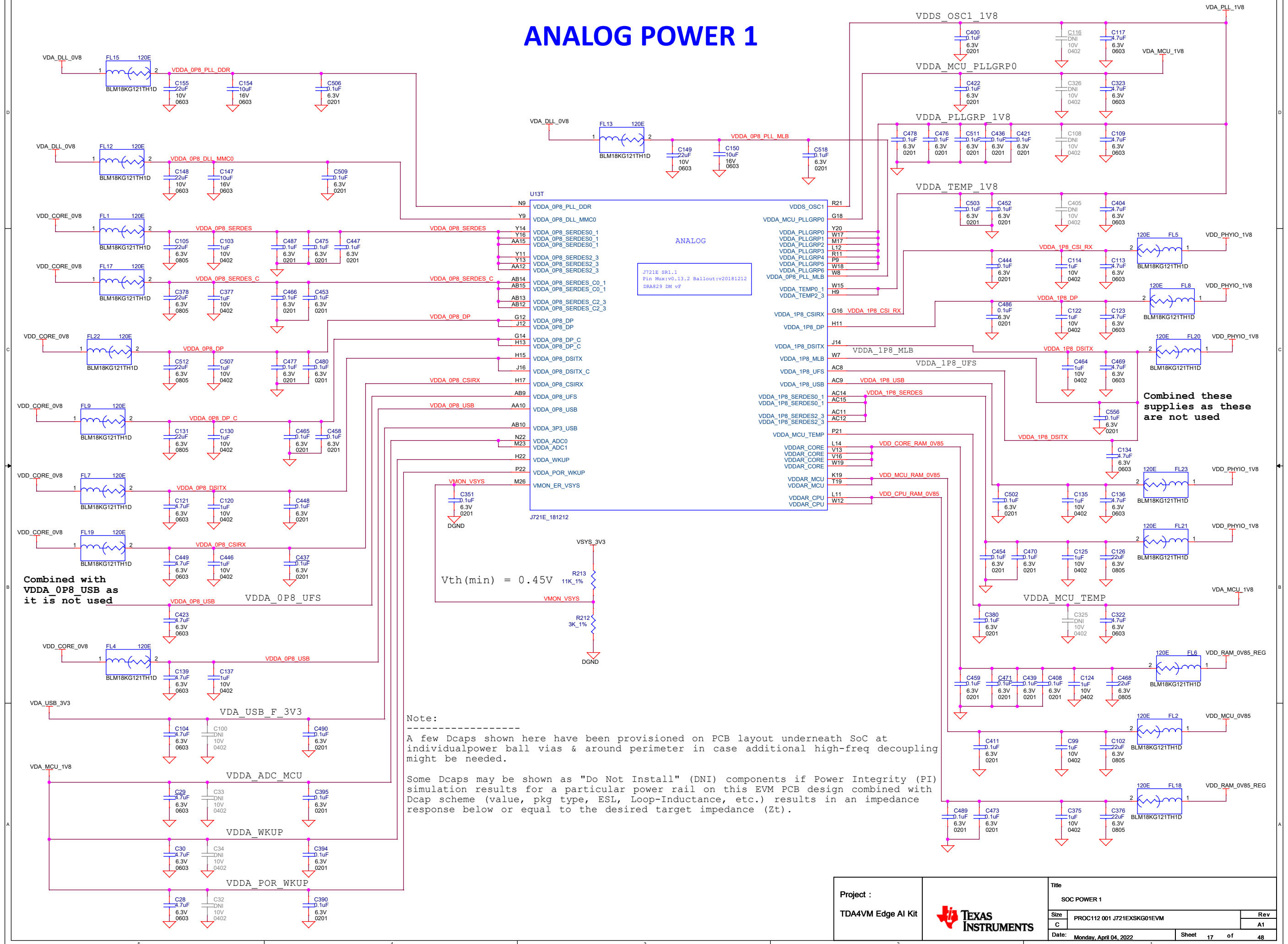


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TDA4VM Edge AI Kit

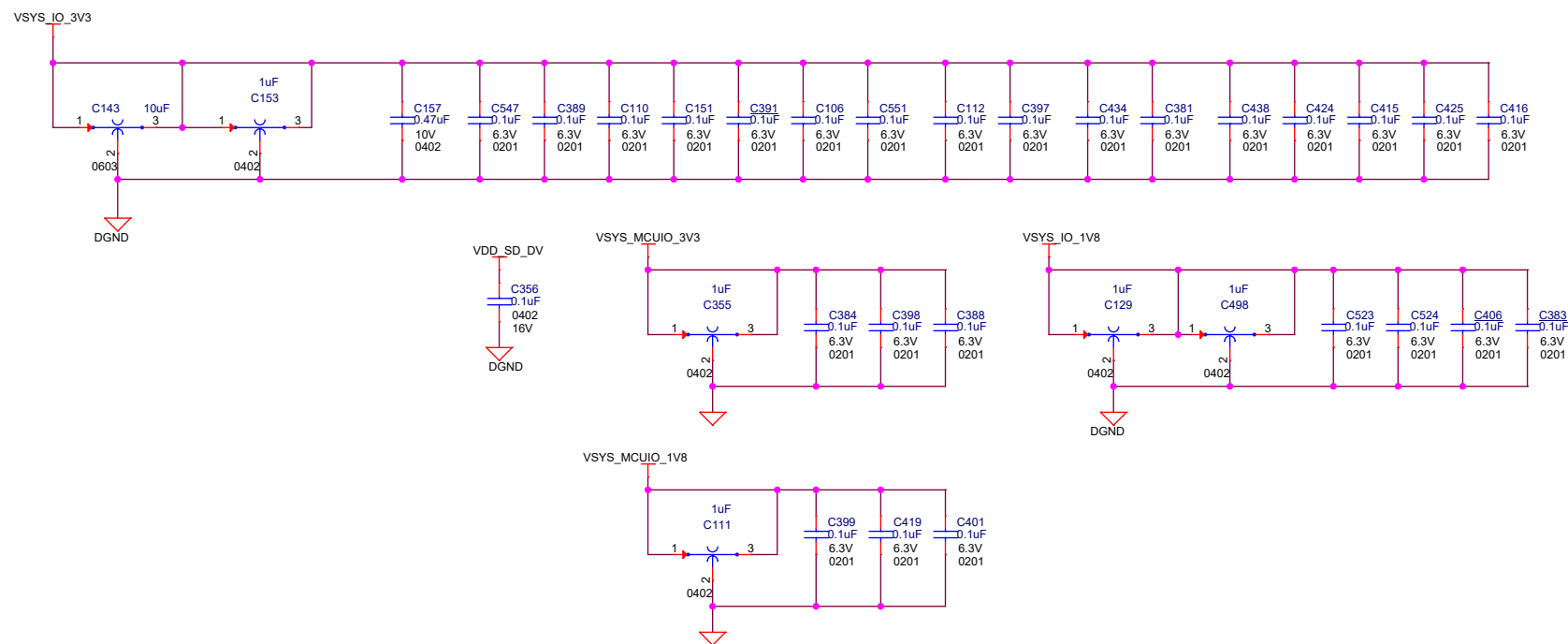
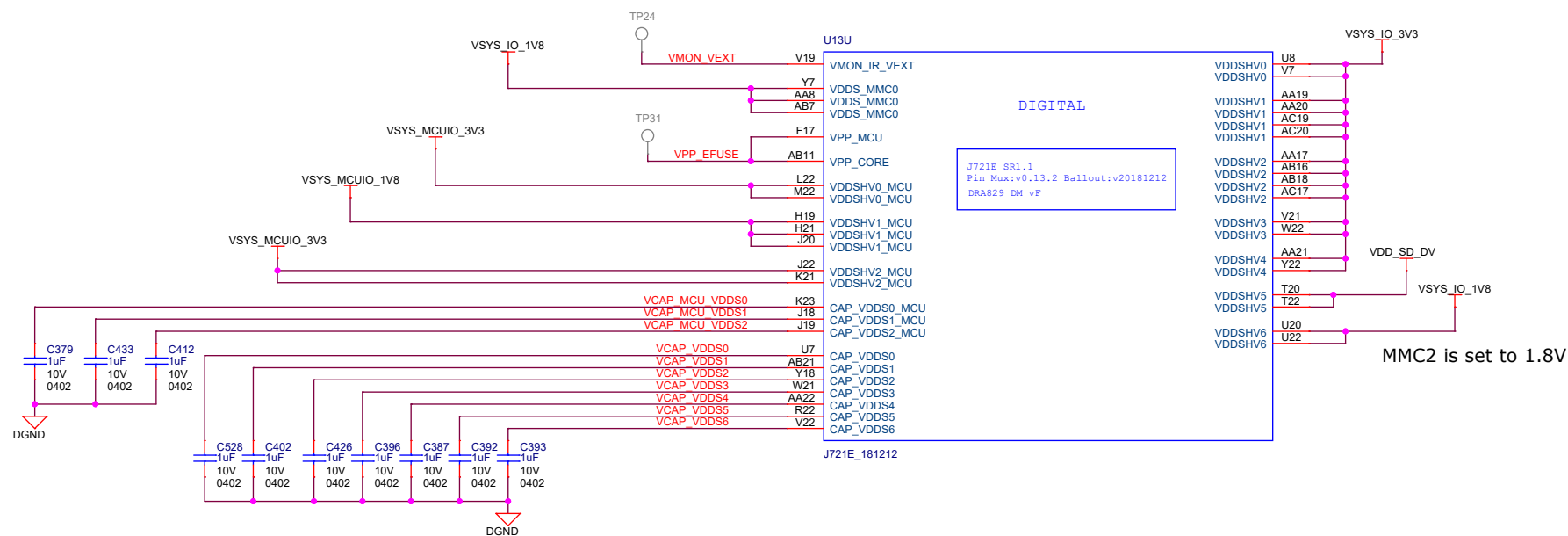


Title PRG		
Size	PROC112 001 J721EXSG01EVM	Rev
C		A1
Date:	Monday, April 04, 2022	Sheet 16 of 48

ANALOG POWER 1



DIGITAL POWER 2



Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

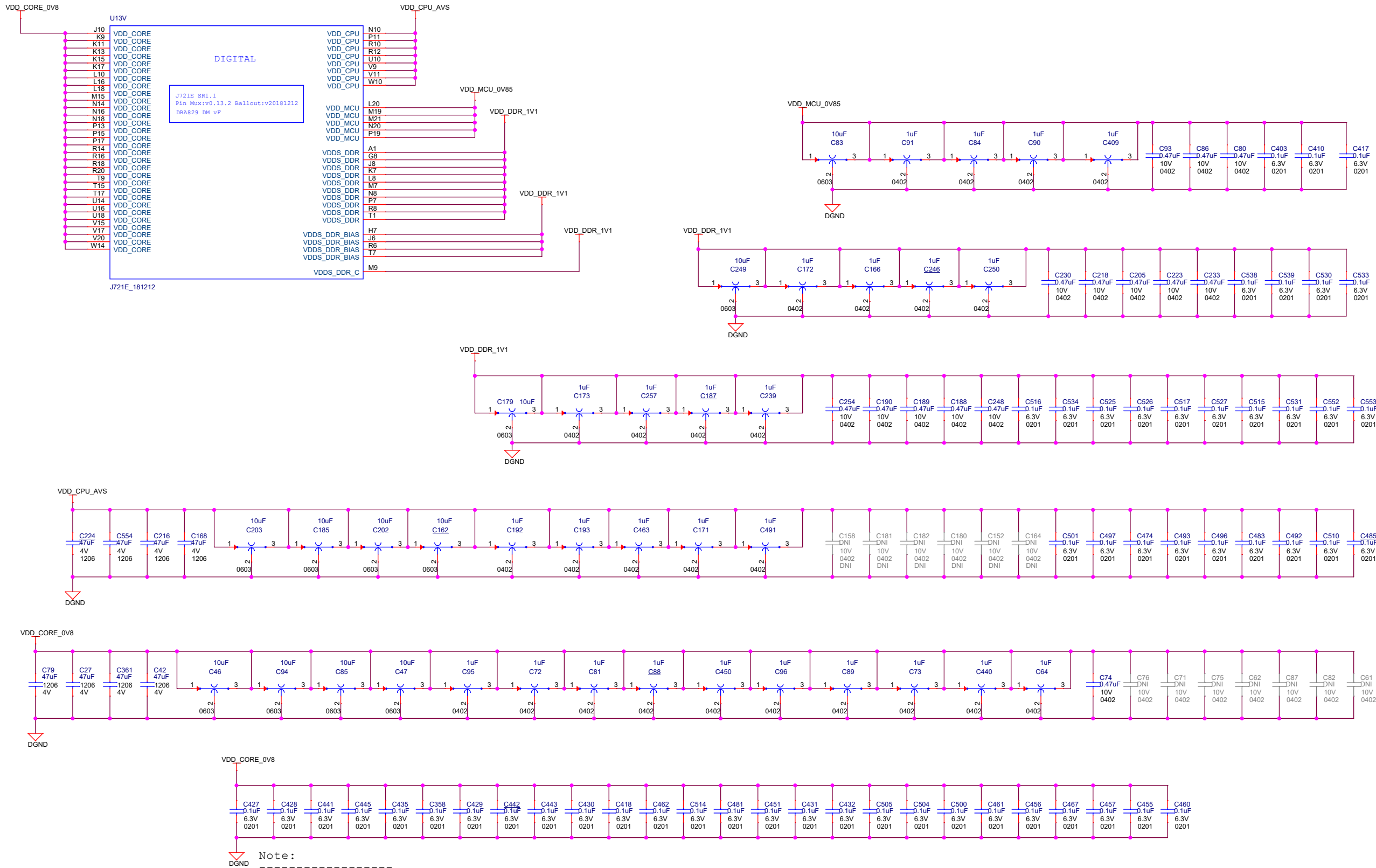
Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Z_t).

Project :
TDA4VM Edge AI Kit



Title		
SOC POWER 2		
Size	Rev	
C	PROC112 001 J721EXSKG01EVM	A1
Date: Monday, April 04, 2022		Sheet 18 of 48

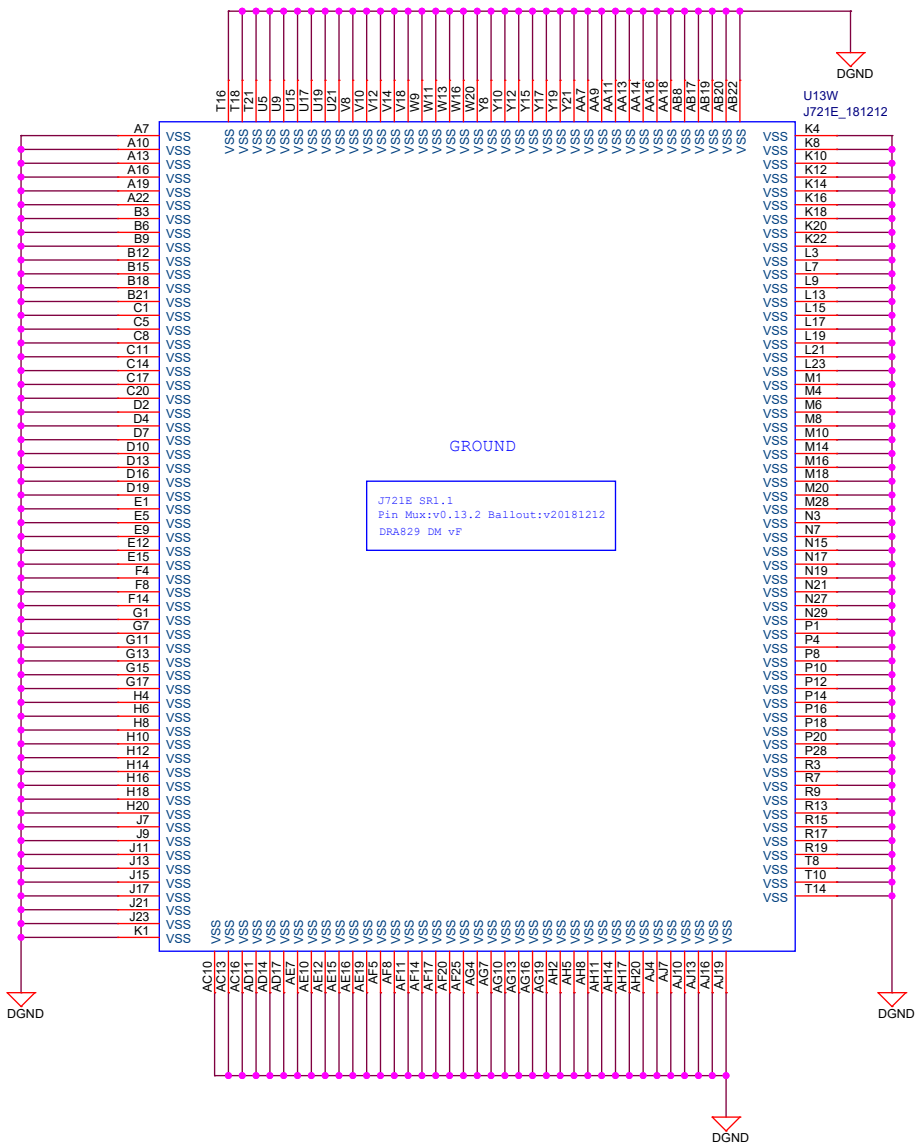
DIGITAL POWER 3



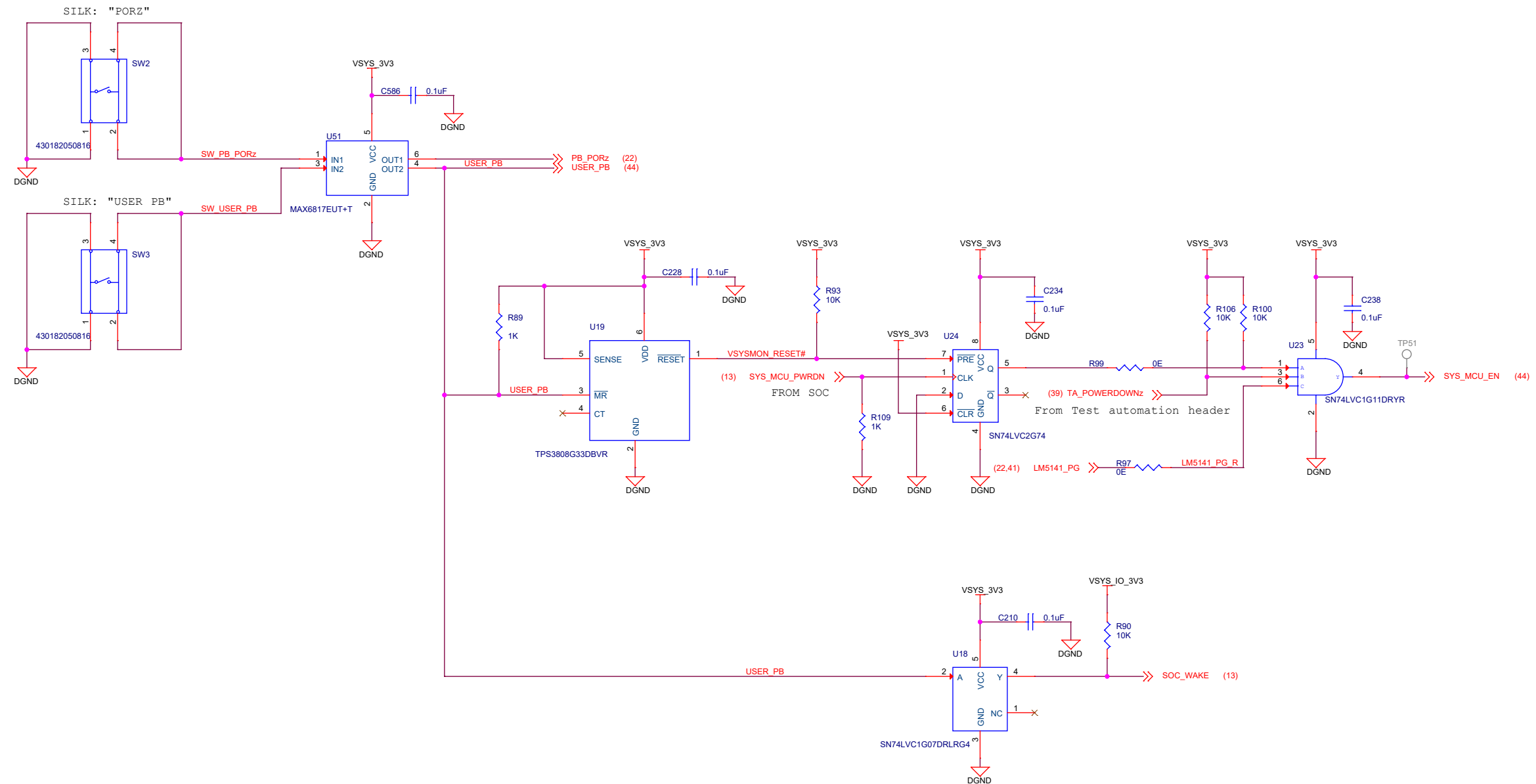
Note:
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Z_t).

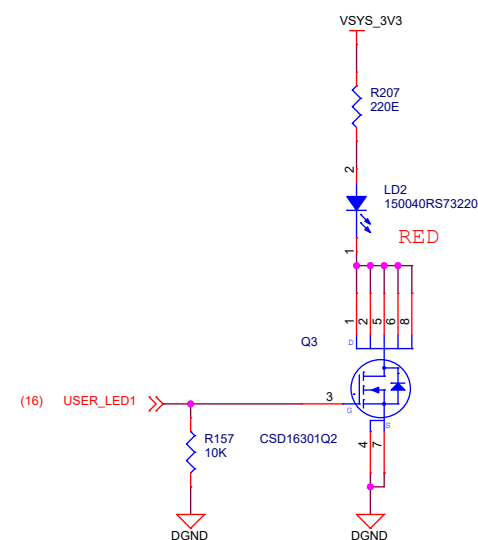
SOC GROUND



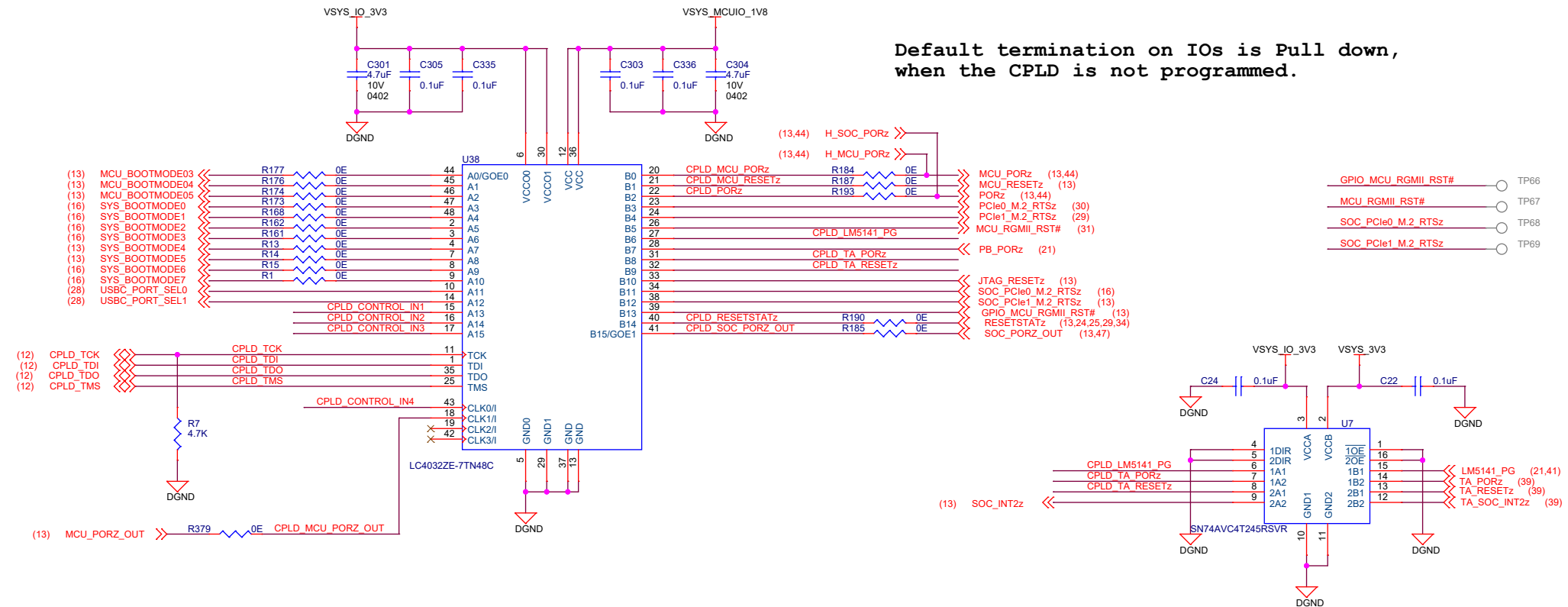
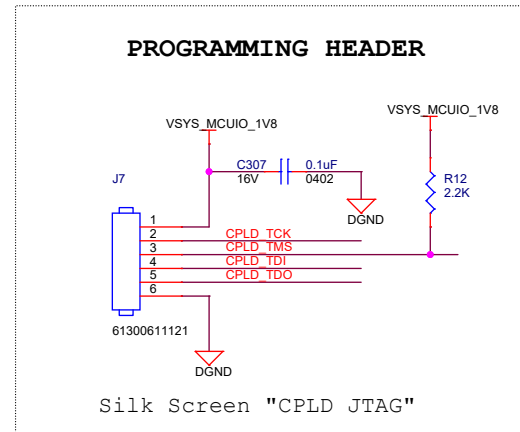
RESET BUTTONs



USER LED

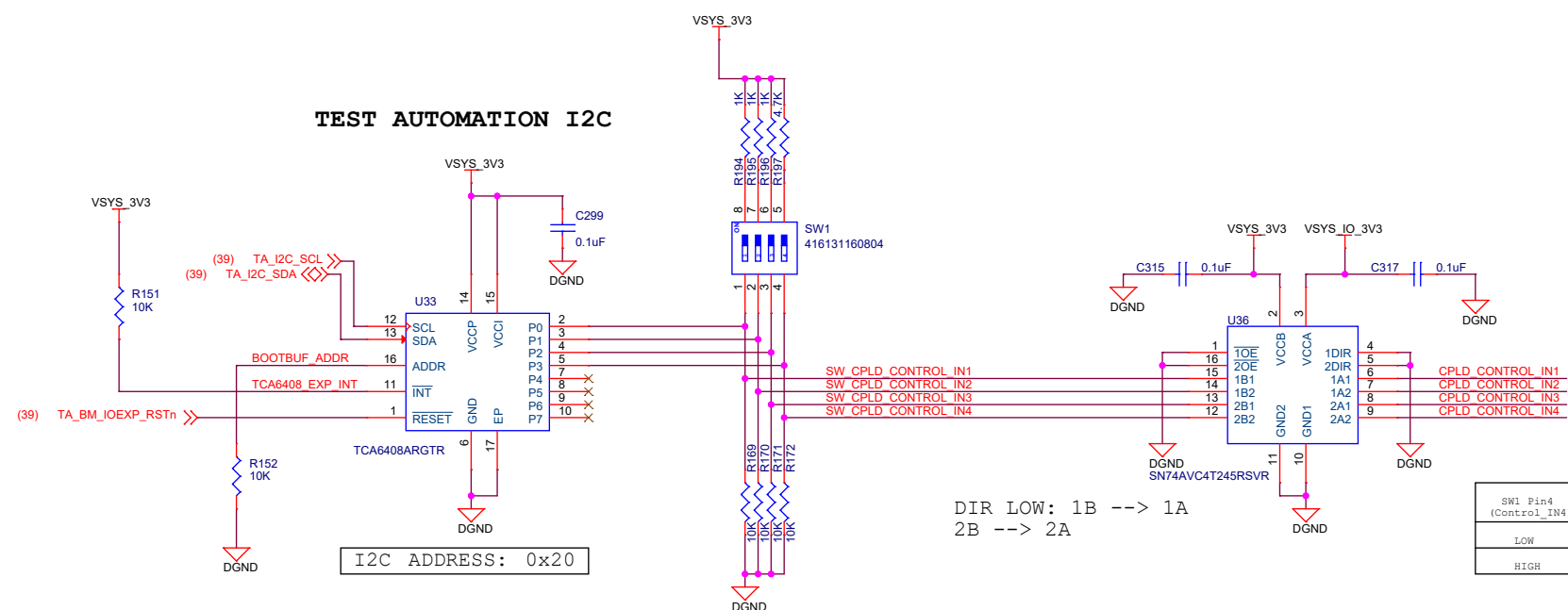


CPLD



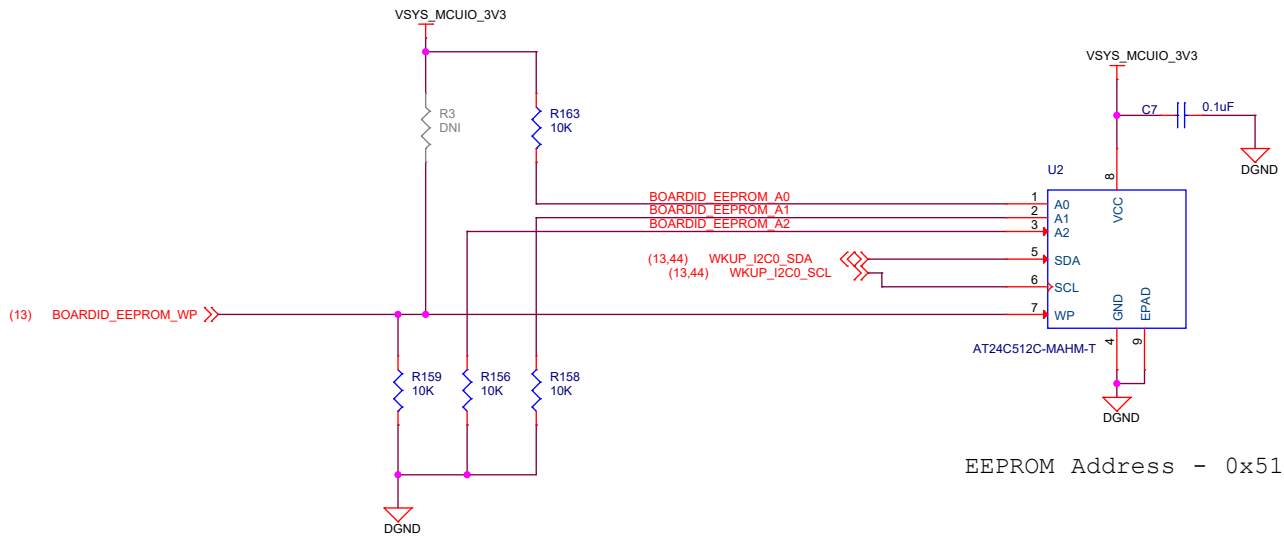
Bootmode Table

SW1.3	SW1.2	SW1.1	BOOTMODE
0	0	0	SD
0	0	1	NO Boot
0	1	0	USB - 0 (DFU)
0	1	1	USB - 1 (DFU)
1	0	0	xSPI - 1S
1	0	1	UART
1	1	0	PCIe
1	1	1	xSPI SFDP

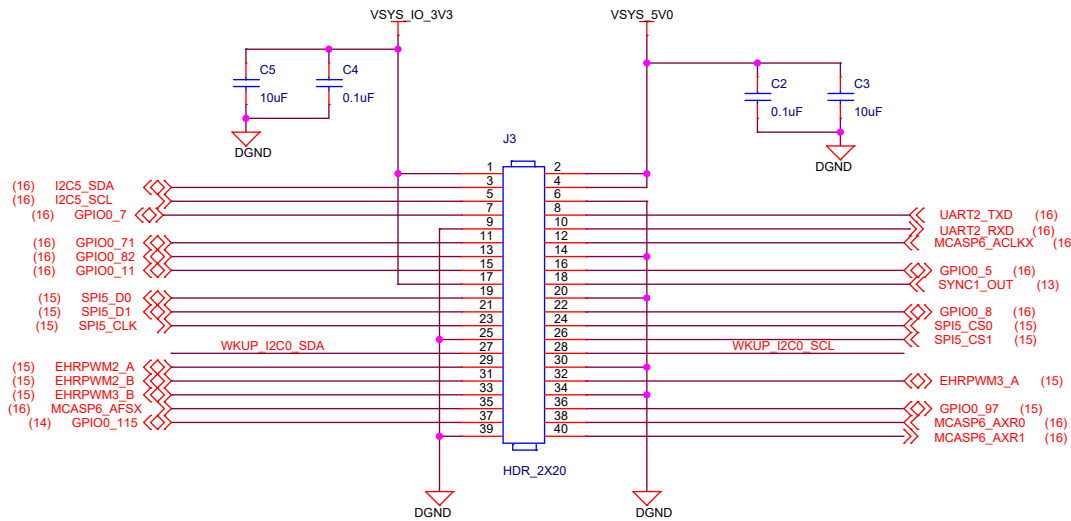


SW1 Pin4 (Control_IN4)	USBC_PORT_SEL1	USBC_PORT_SEL0	Selected USB C Mode
LOW	LOW	LOW	DFP
HIGH	X	HIGH	UFP

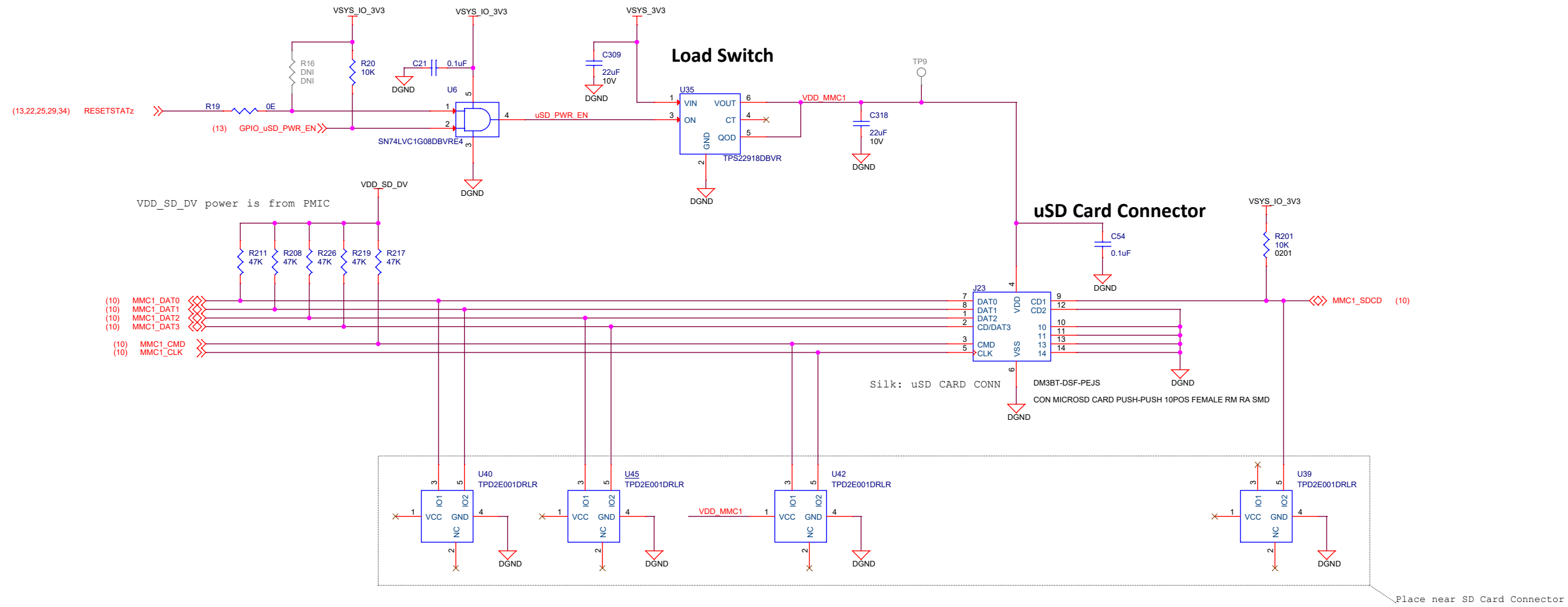
BOARD ID EEPROM



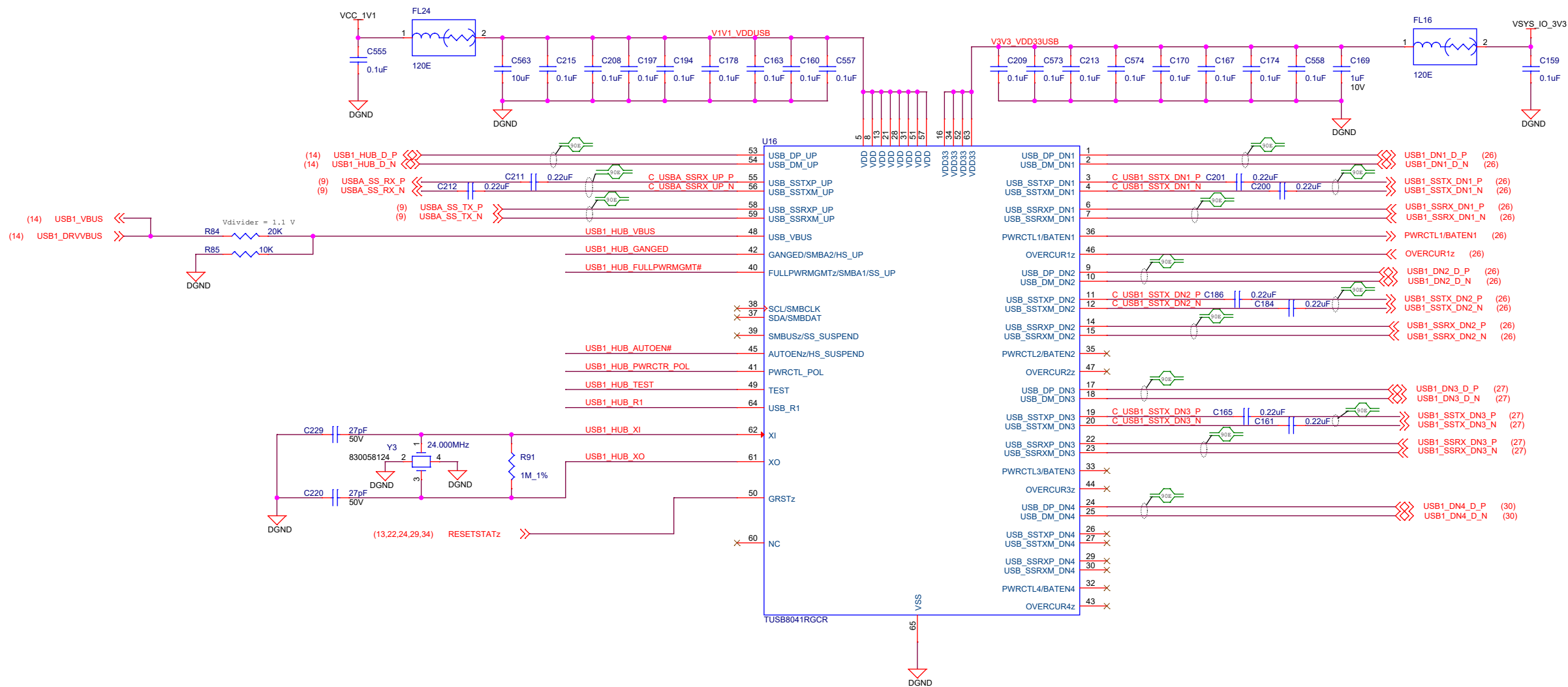
40Pin Expansion Header



Micro SD CARD INTERFACE



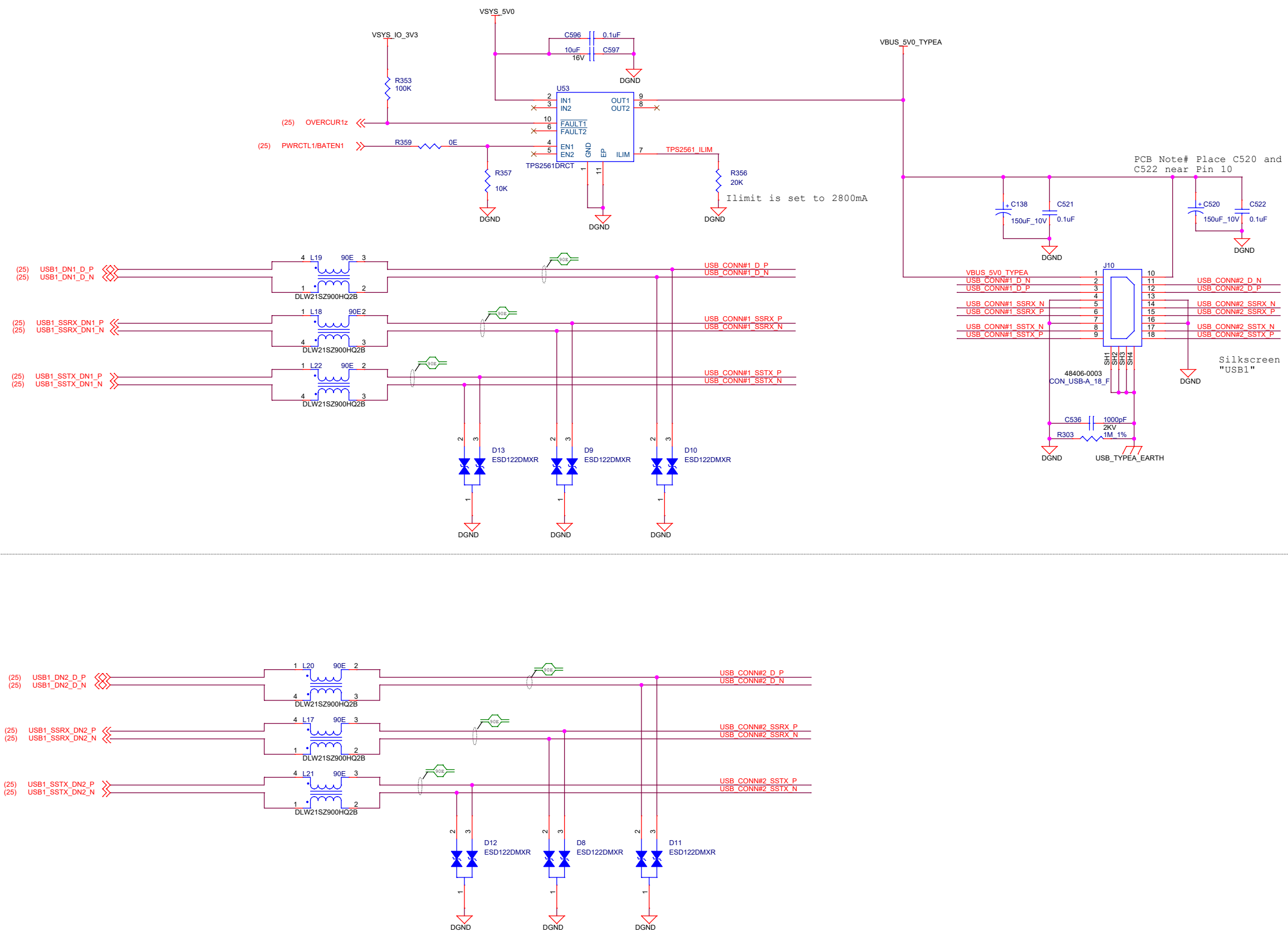
USB3.0 HUB



NOTE :	
#1	USB1_HUB_AUTOEN#
#2	USB1_HUB_PWRCTR_POL
#3	USB1_HUB_FULLPWRMGMT#
#4	USB1_HUB_GANGED
	USB1_HUB_TEST
	USB1_HUB_R1

NOTE :	
#1	Automatic Charge Mode Disabled
#2	PWRCTL Polarity is Active High
#3	Power Switching and Overcurrent Inputs Supported
#4	Ganged Power Control Enabled

USB 3.0 TYPE-A CONNECTORS - 1

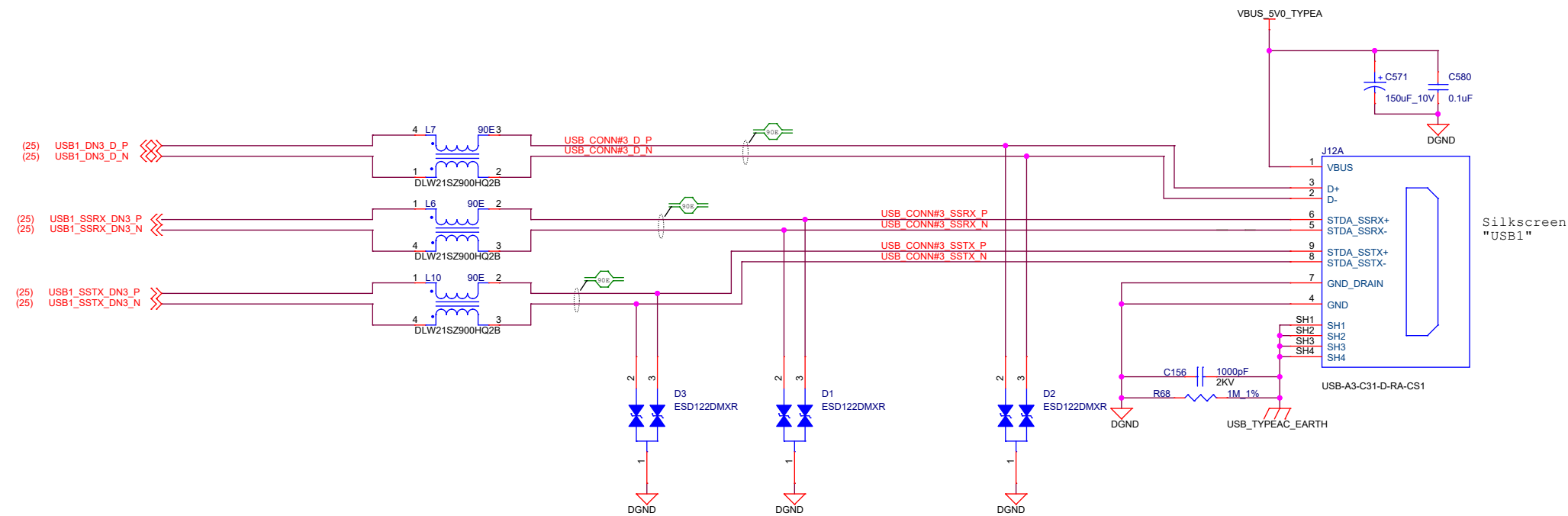


Project :
TDA4VM Edge AI Kit

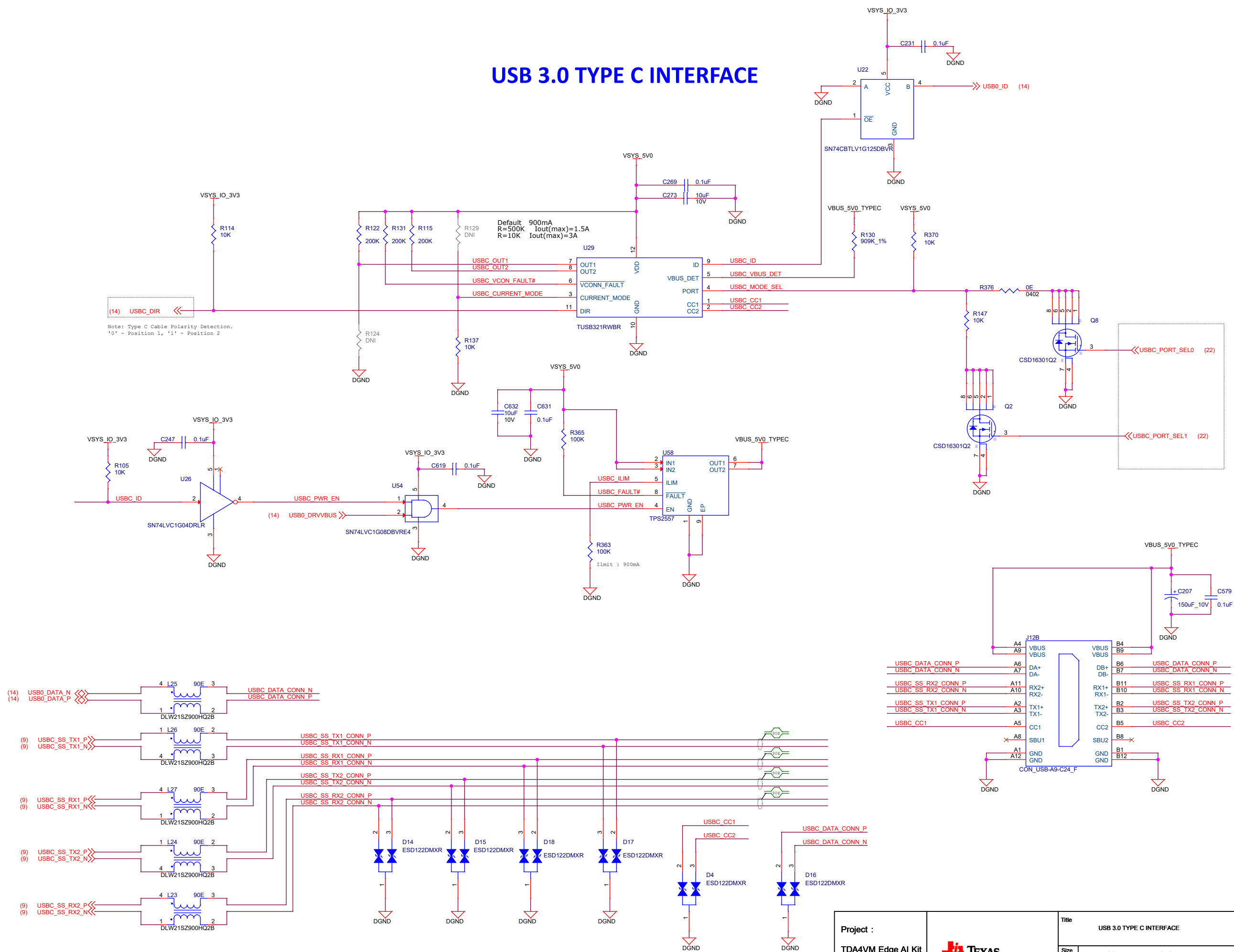


Title USB 3.0 TYPE-A CONNECTORS - 1		
Size C	PROC112 001 J721EXSKG01EVM	Rev A1
Date: Monday, April 04, 2022	Sheet 26 of 48	

USB 3.0 TYPE-A CONNECTORS - 2



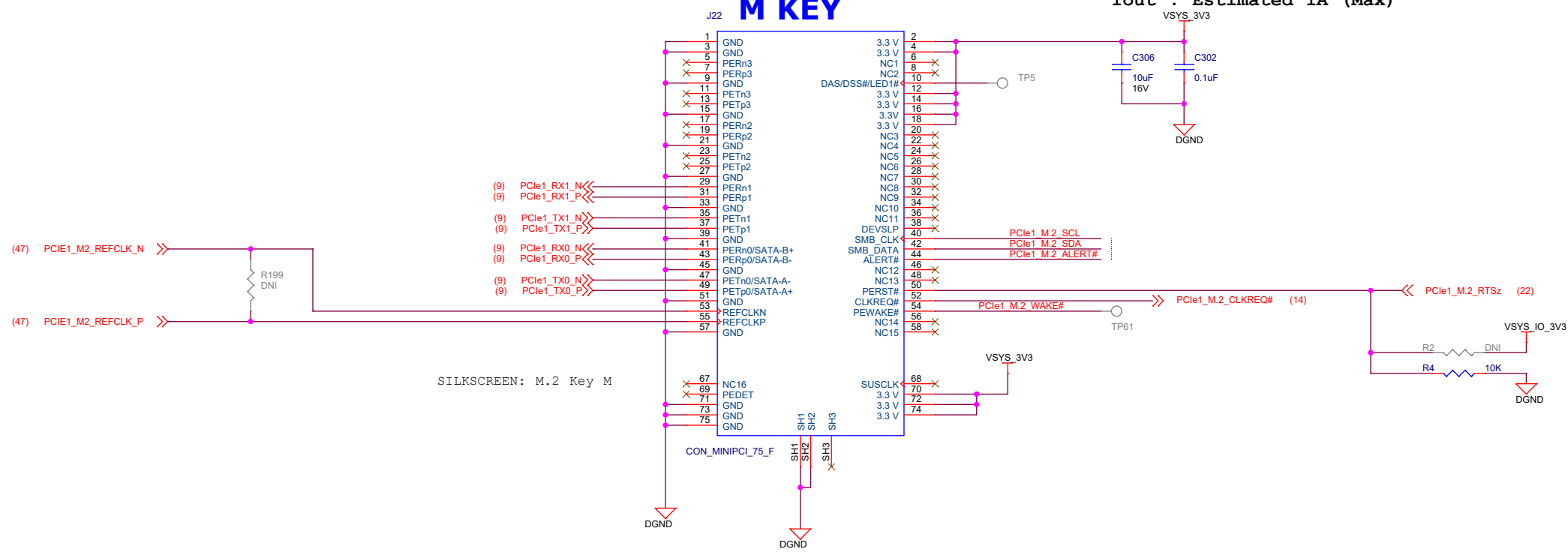
USB 3.0 TYPE C INTERFACE



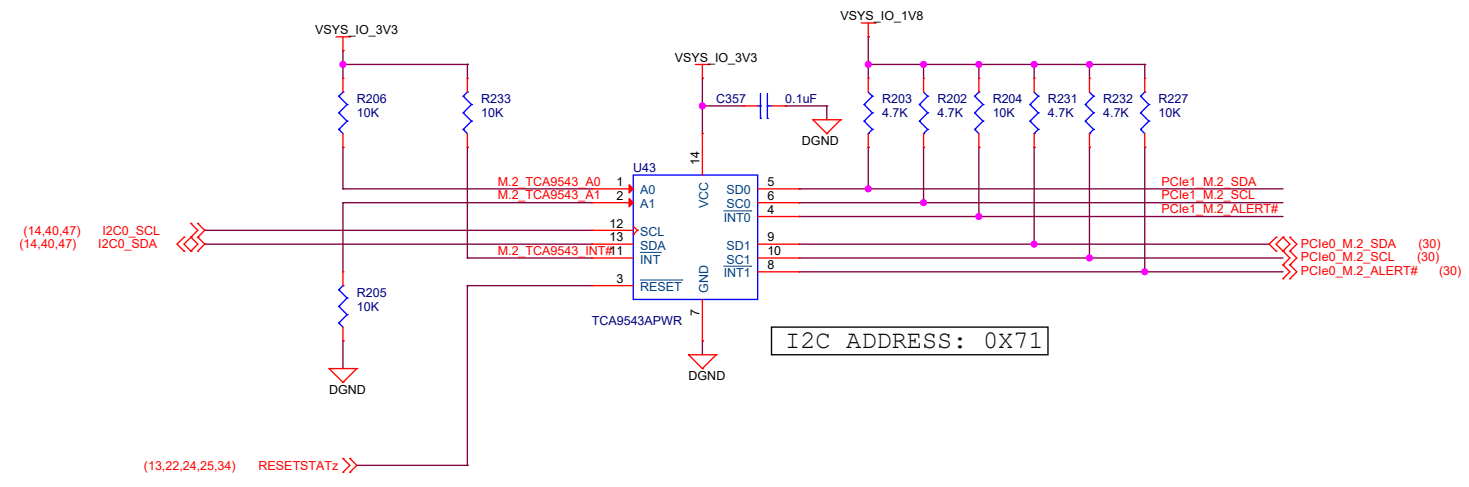
PCIE_M.2_INTERFACE SSD

M KEY

Iout : Estimated 1A (Max)



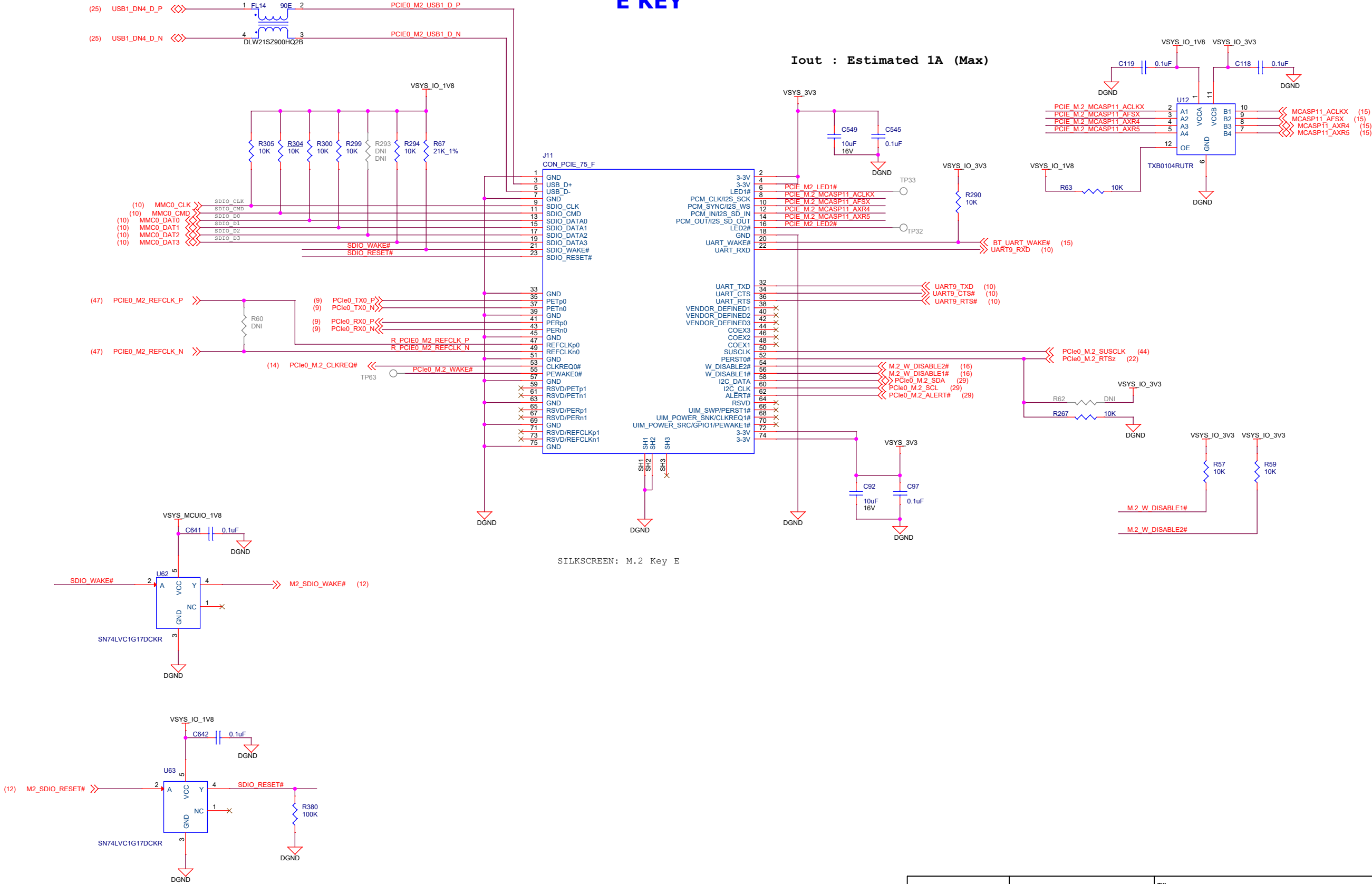
3.3V To 1V8 Level translator



PCIE_M.2_INTERFACE - SDIO

E KEY

Iout : Estimated 1A (Max)

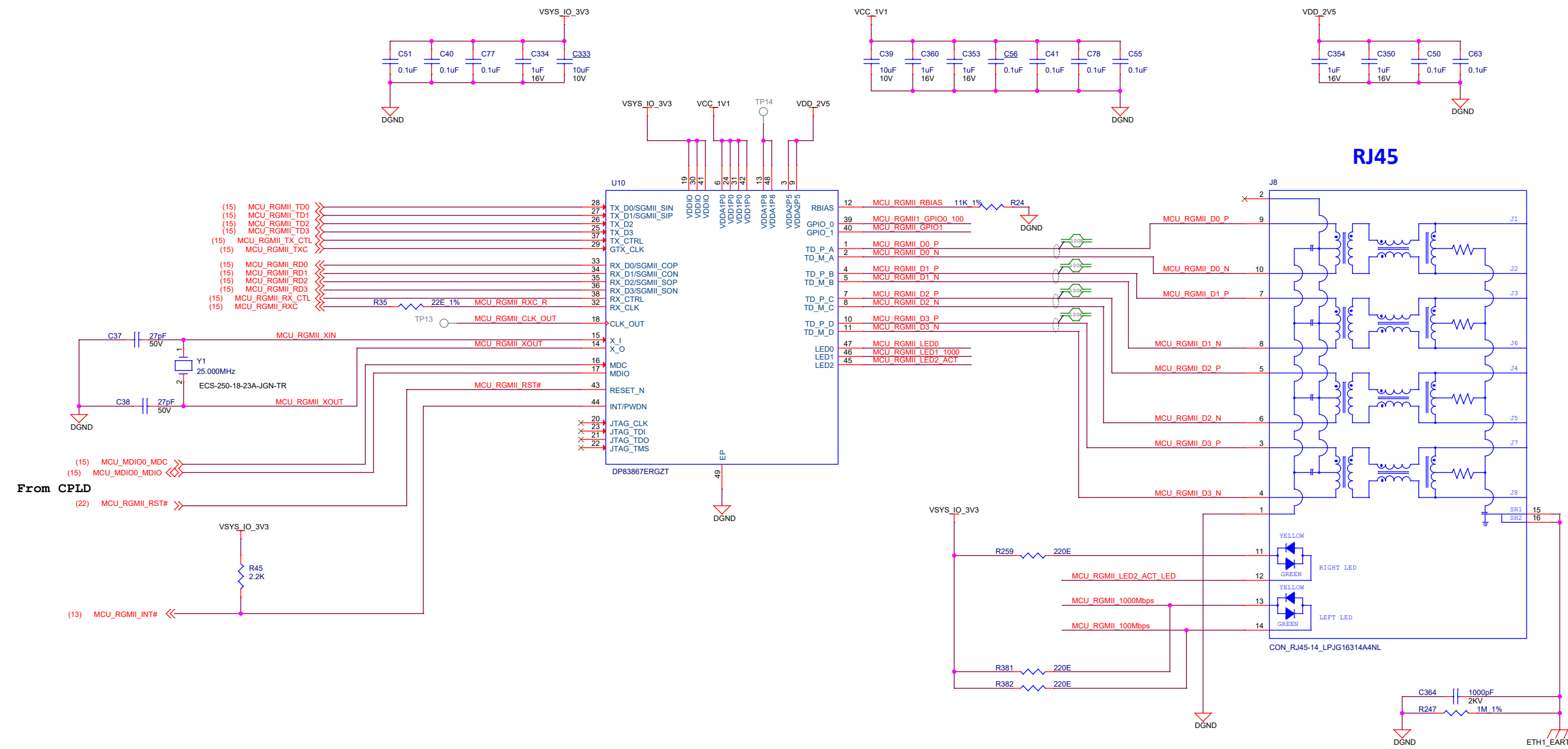


Project :
TDA4VM Edge AI Kit

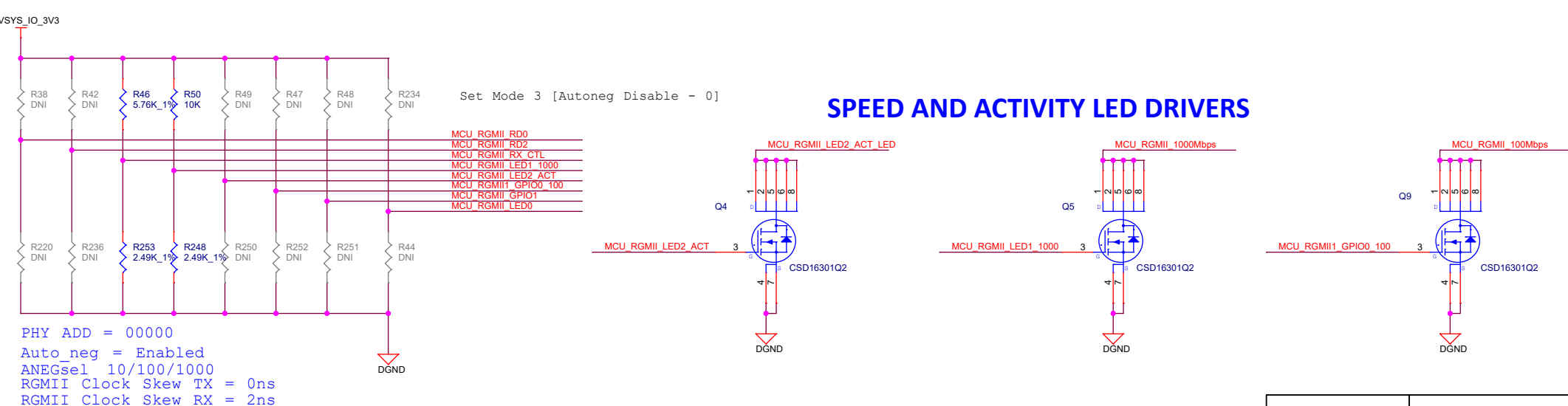


Title PCle_M.2_INTERFACE(E Key)		
Size C	PROC112 001 J721EXSKG01EVM	Rev A1
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MCU GB ETHERNET



SPEED AND ACTIVITY LED DRIVERS

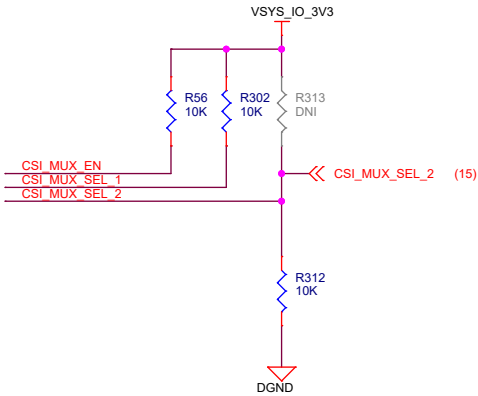
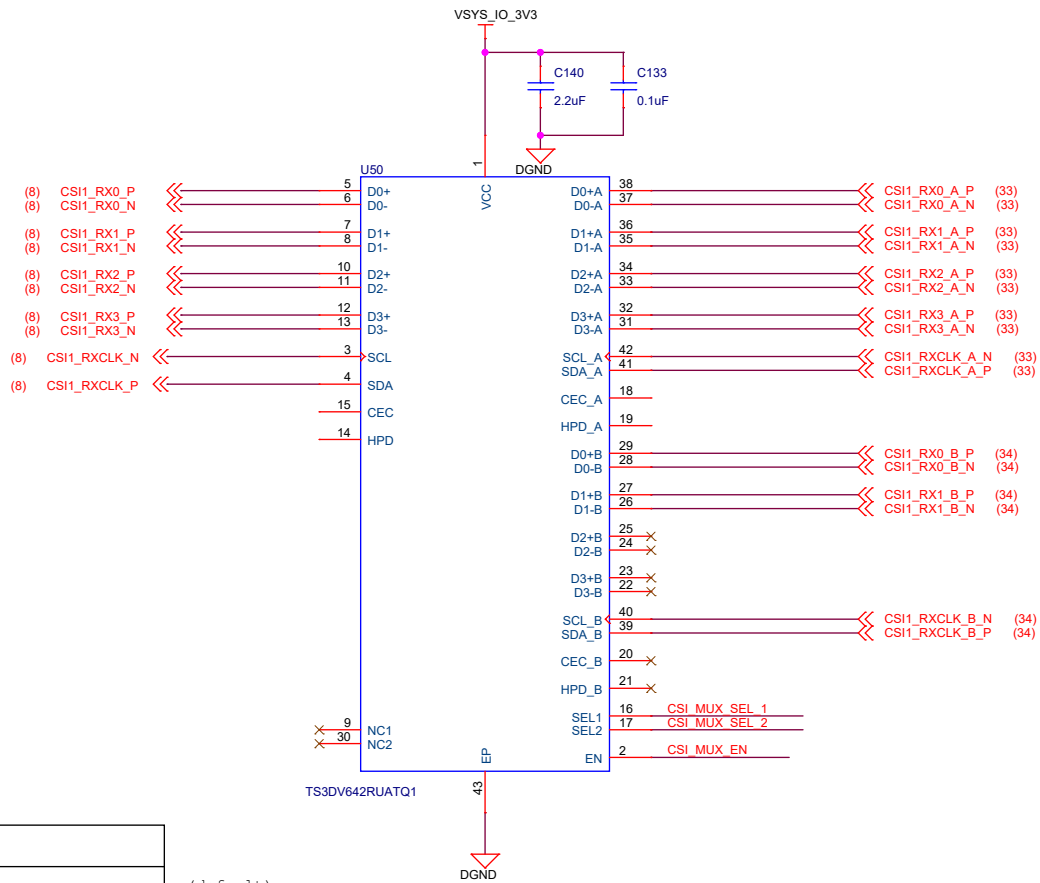
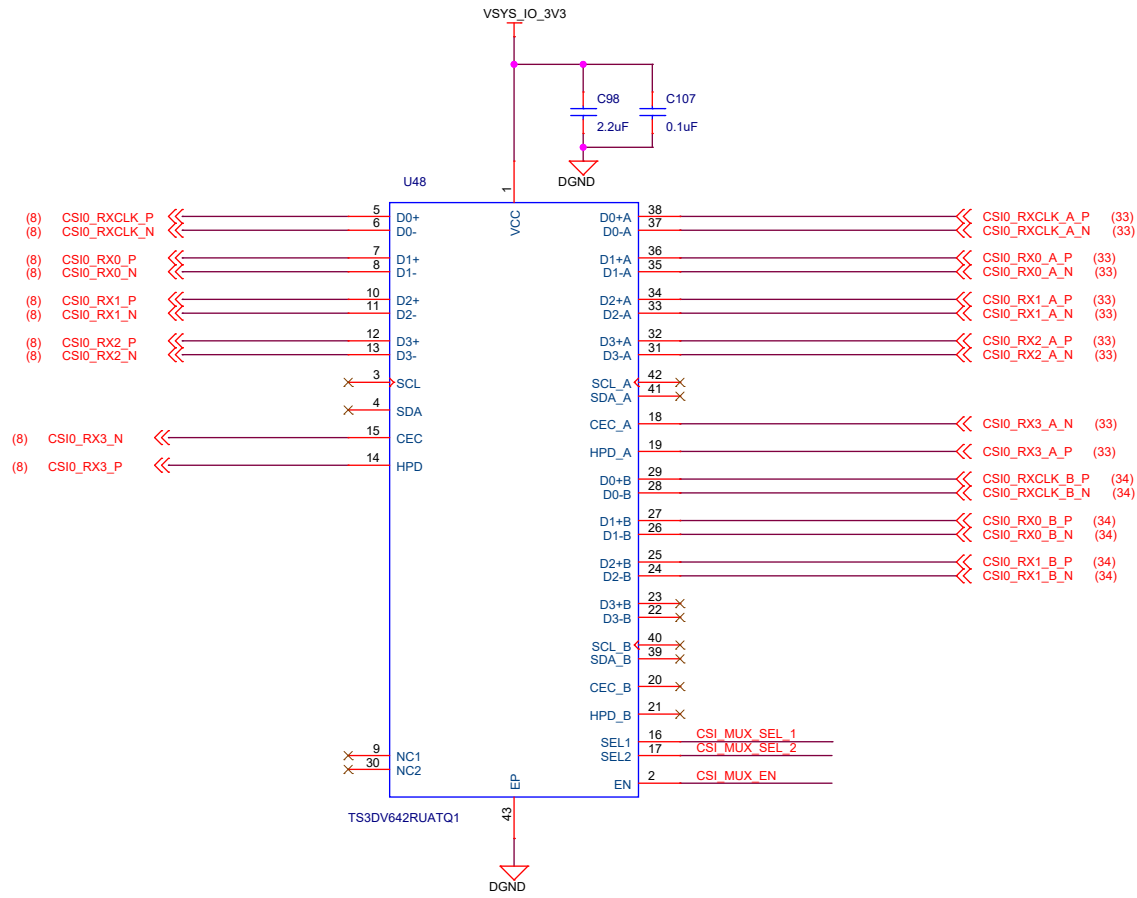


RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

PHY ADD = 00000
Auto_neg = Enabled
ANEGsel 10/100/1000
RGMII Clock Skew TX = 0ns
RGMII Clock Skew RX = 2ns

LED_2-MODE1 & LED_1-MODE2-TX SKEW=0ns
GPIO0-MODE1 & GPIO1-MODE1-RX SKEW=2ns

CSI MUX - DATA



CSI - 1:2 MUX : Truth Table

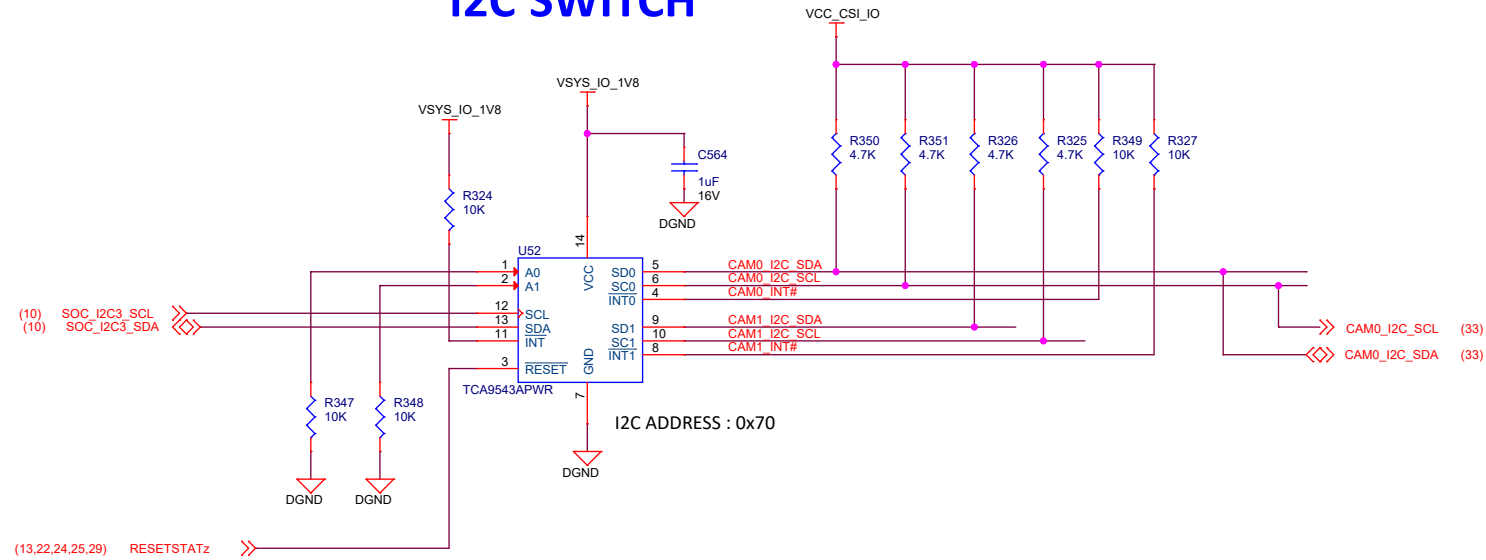
MUX_SEL_2	FUNCTION	
LOW	INPUT<--A port [CSI2 Connector]	(default)
HIGH	INPUT<--B port [FPC Camera Connector]	

1

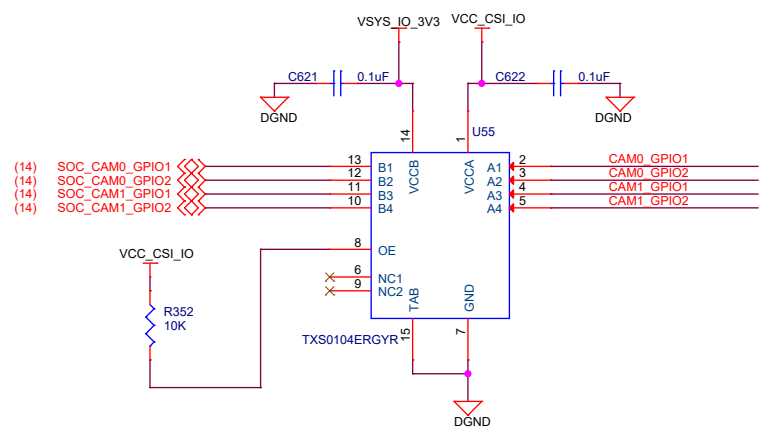


CSI FPC CAMERA CONNECTORS

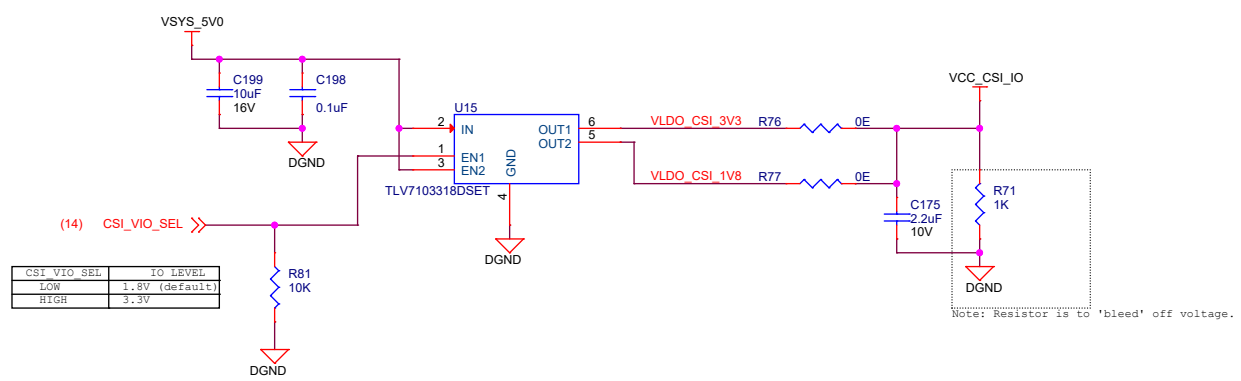
I2C SWITCH



GPIO LEVEL TRANSLATOR

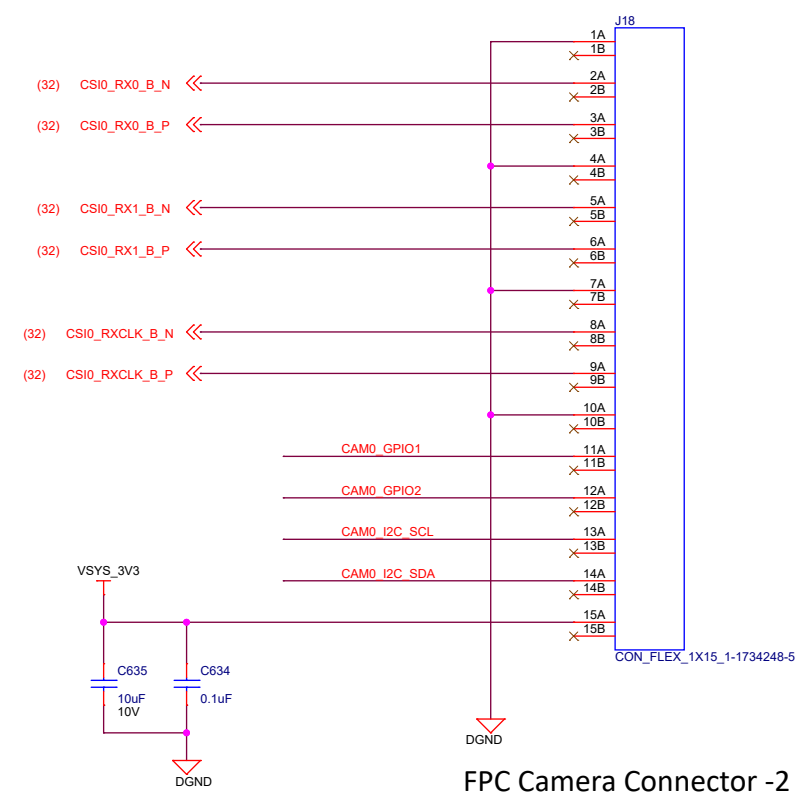


CAMERA IO SUPPLY

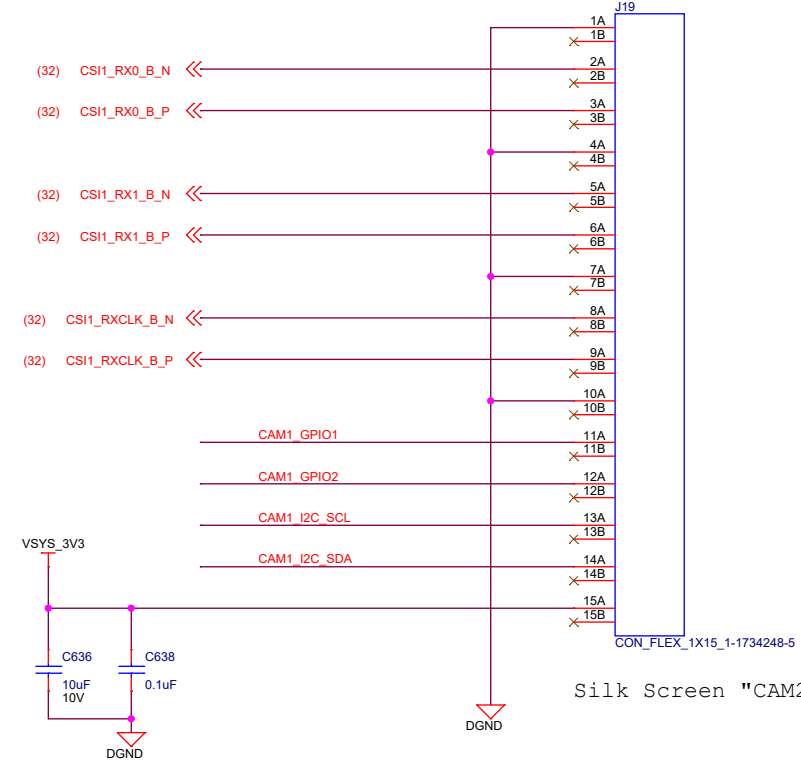


CSI_VIO_SEL	IO_LEVEL
LOW	1.8V (default)
HIGH	3.3V

Silk Screen "CAM1"
FPC Camera Connector -1

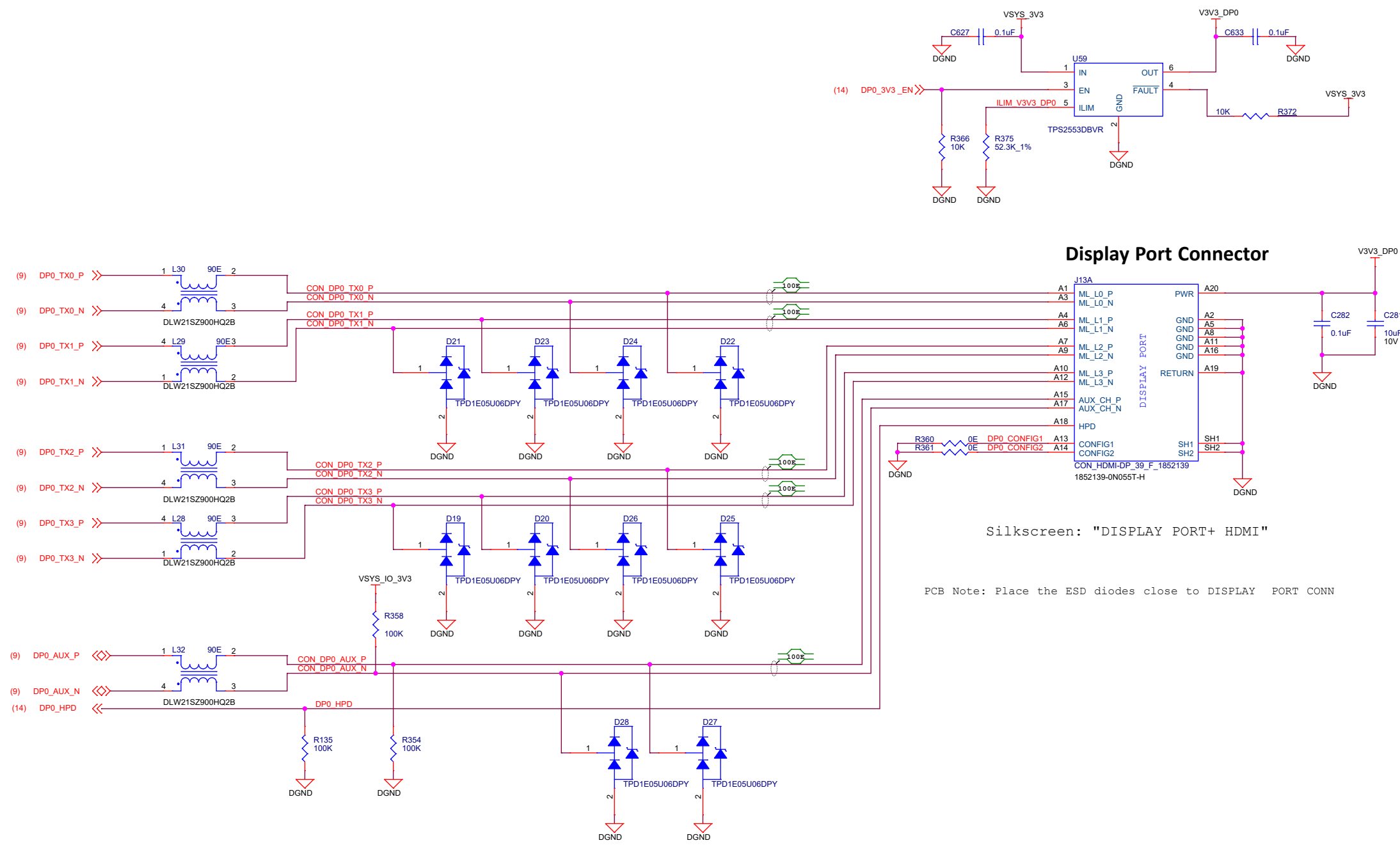


FPC Camera Connector -2



Silk Screen "CAM2"

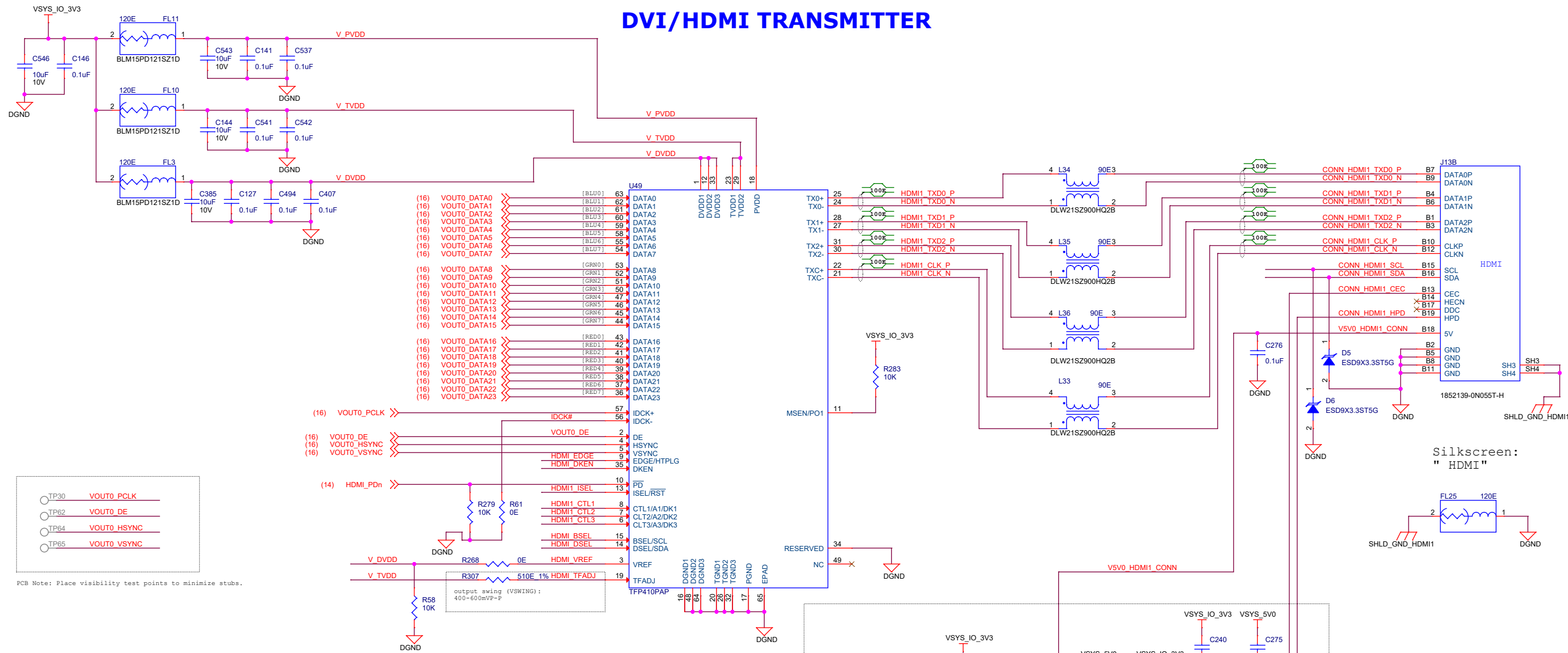
DISPLAY PORT INTERFACE



Silkscreen: "DISPLAY PORT+ HDMI"

PCB Note: Place the ESD diodes close to DISPLAY PORT CONN

DVI/HDMI TRANSMITTER

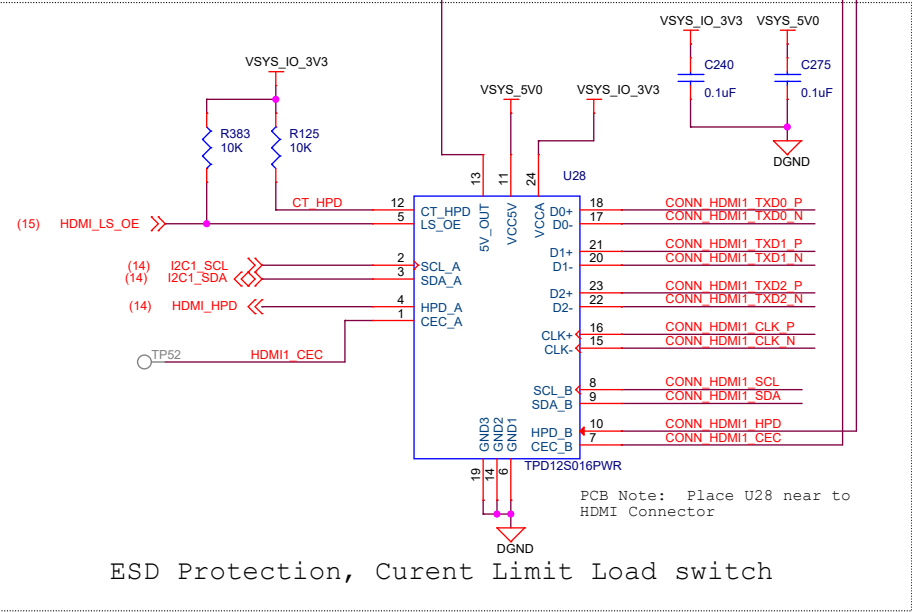


DVI Configuration Settings

VREF	BSEL	EDGE	DSEL	BUS WIDTH	LATCH MODE	CLOCK MODE	CLOCK EDGE
0.55V-0.9V	1	0	0	24-bit	Single-ended	Falling	Single-ended
Default	1	1	0	24-bit	Single-ended	Raising	Single-ended

ISEL:- Low (default): I2C interface is disabled and chip configuration is specified by BSEL, DSEL, EDGE, VREF pins

When ISEL: L, DSEL-H- enables de-skew function (default)

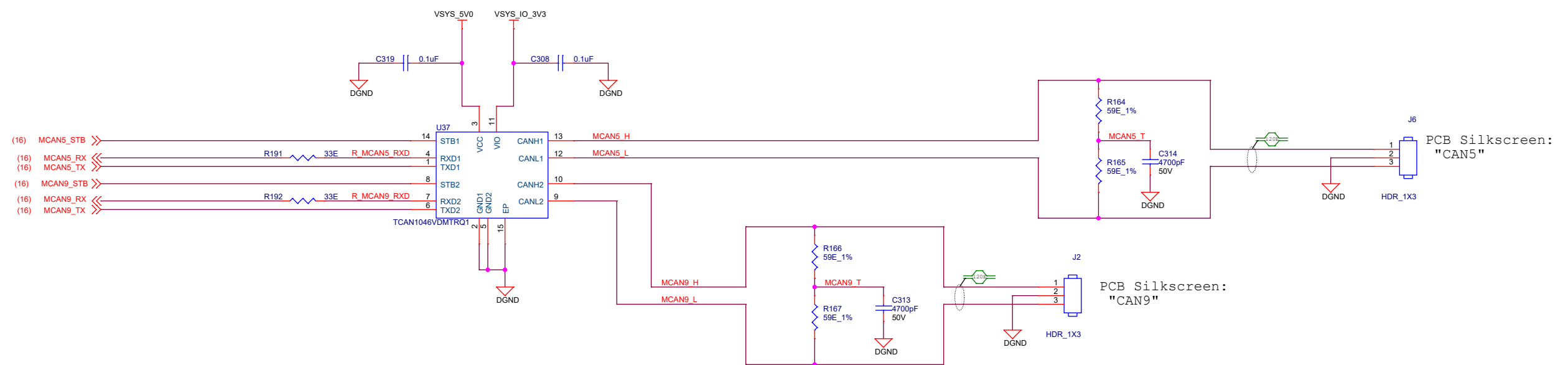
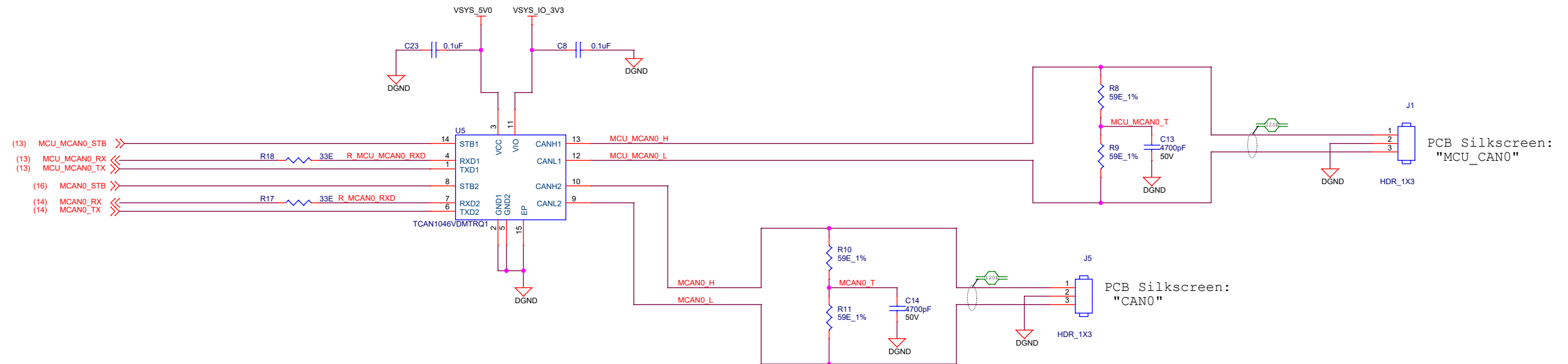


Project :
TDA4VM Edge AI Kit



Title HDMI BRIDGE		
Size C	PROC112 001 J721EXSKG01EVM	Rev A1
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CAN TRANSCEIVERS #2-MAIN DOMAIN



Project :
TDA4VM Edge AI Kit

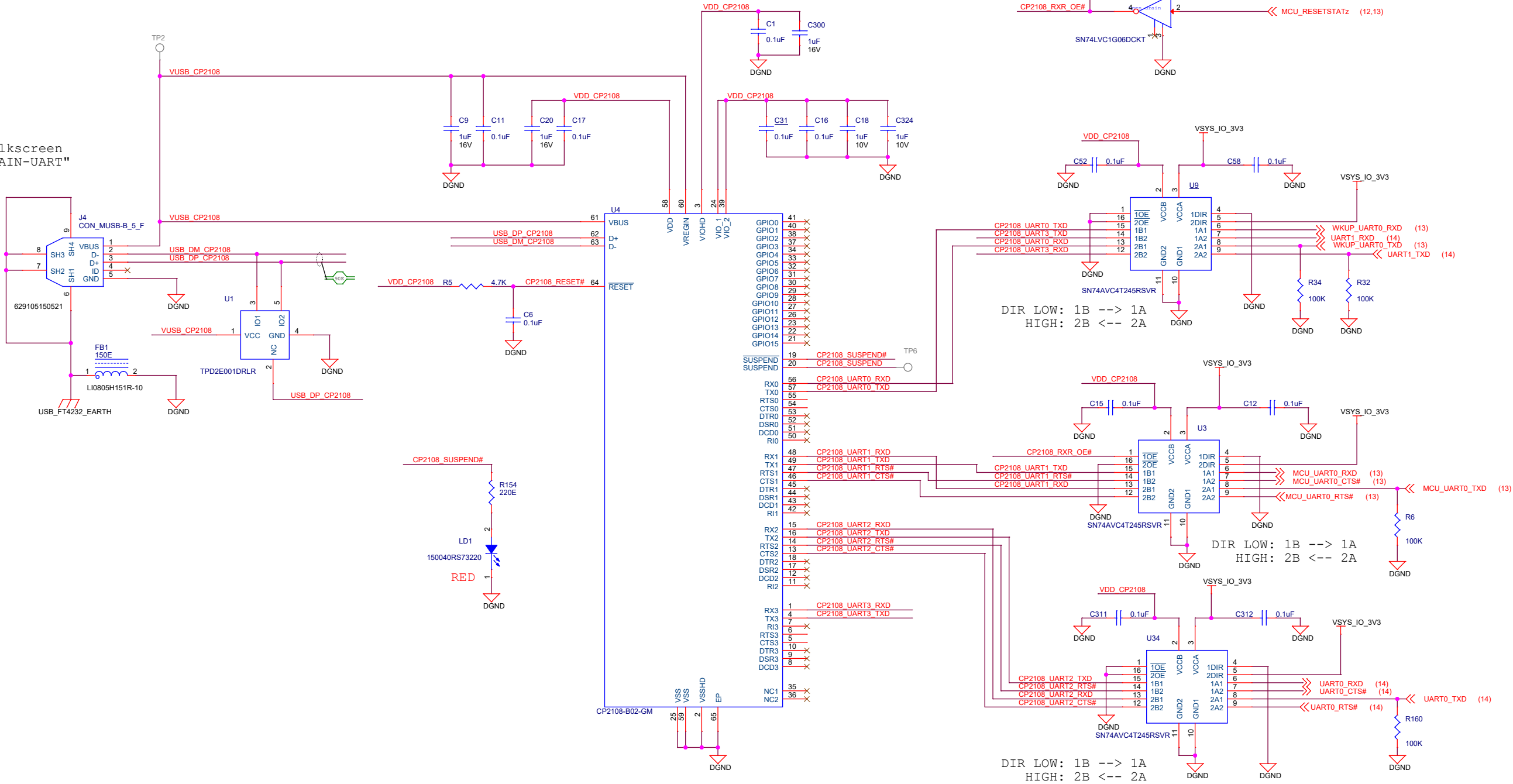


Title	CAN TRANSCEIVERS
-------	------------------

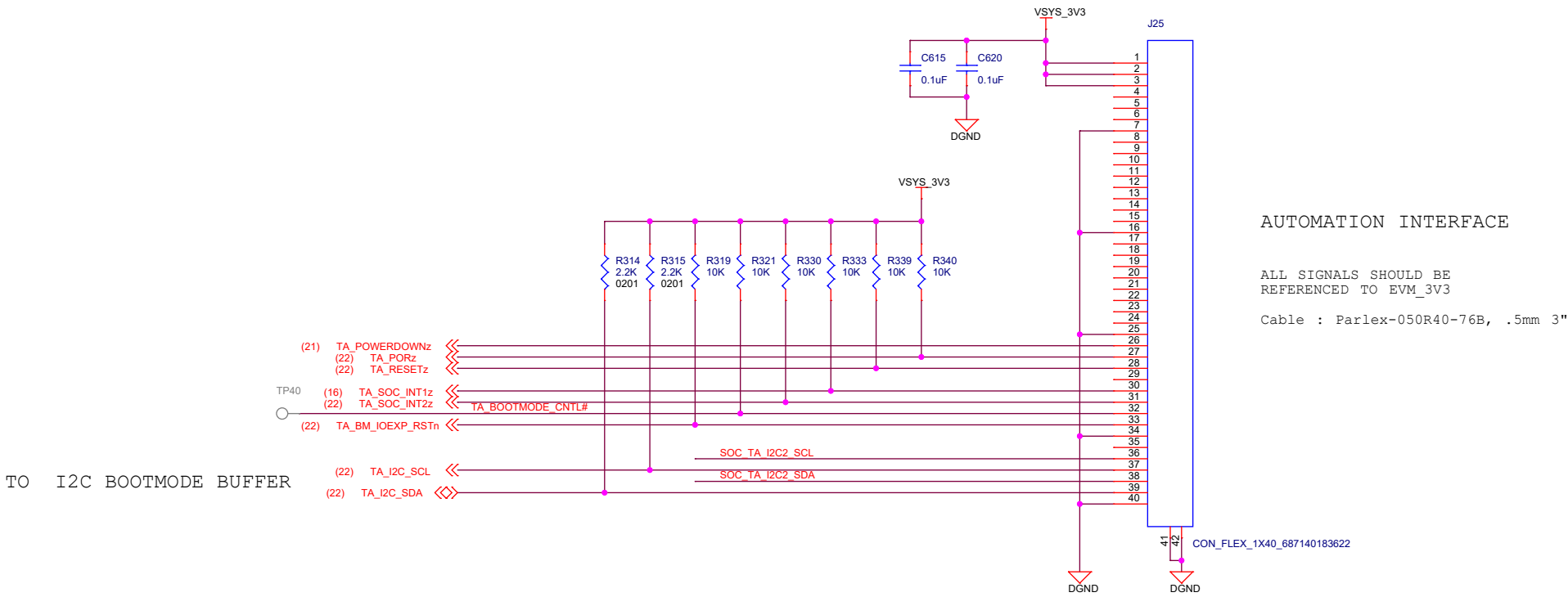
Size	PROC112 001 J721EXSKG01EVM	Rev
C		A1
Date:	Monday, April 04, 2022	Sheet 37 of 48

QUAD PORT CONSOLE

Silkscreen
"MAIN-UART"

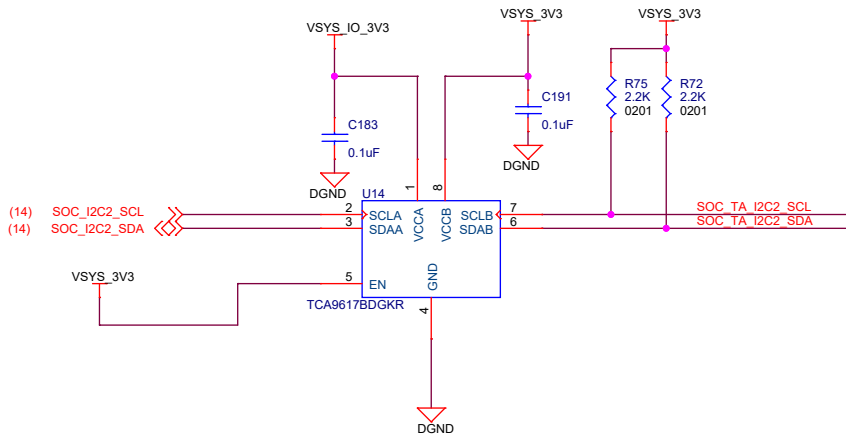


TEST AUTOMATION HEADER



AUTOMATION INTERFACE

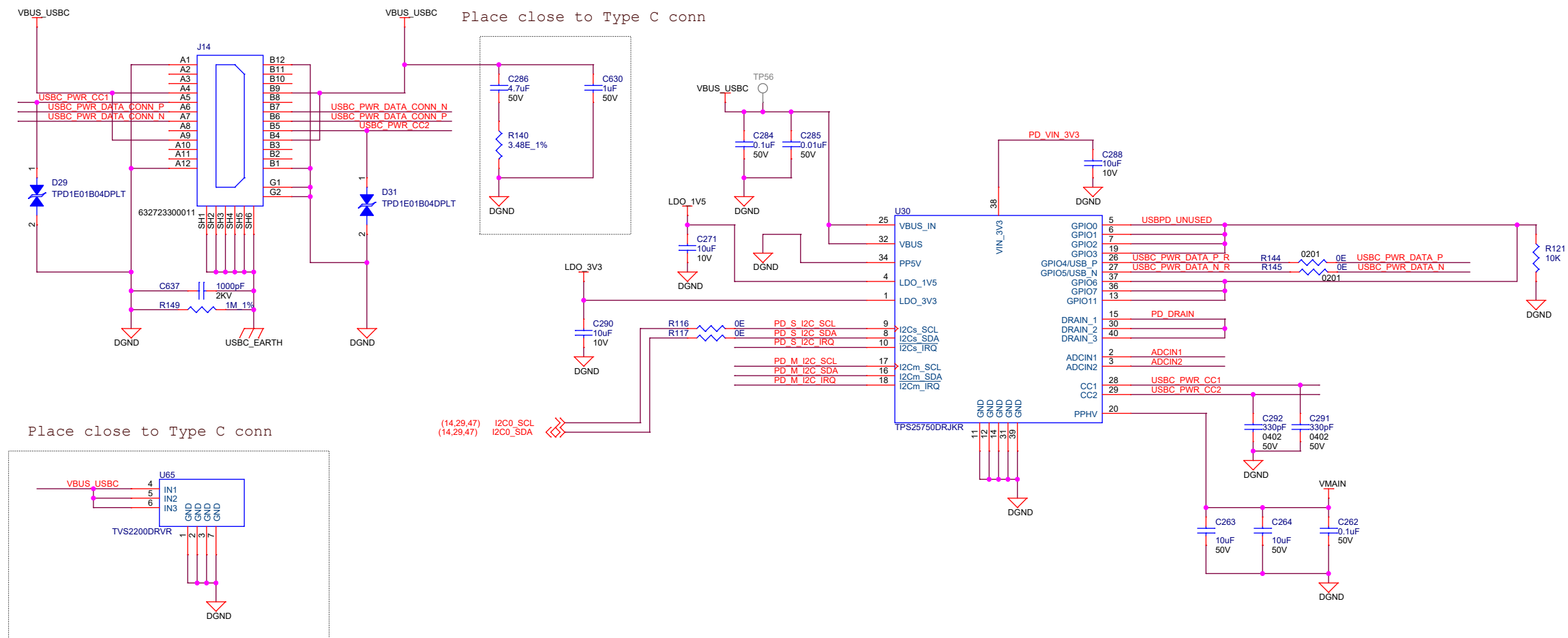
ALL SIGNALS SHOULD BE
REFERENCED TO EVM_3V3
Cable : Parlex-050R40-76B, .5mm 3"



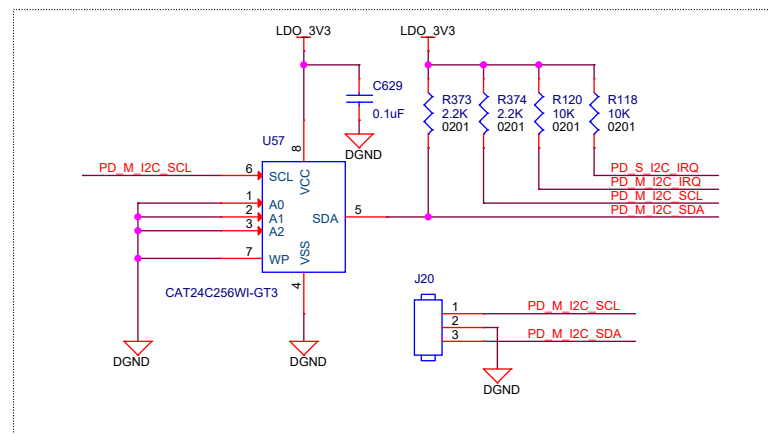
TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

USB-C Power



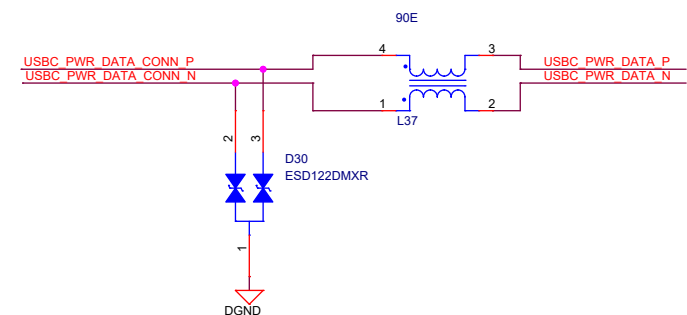
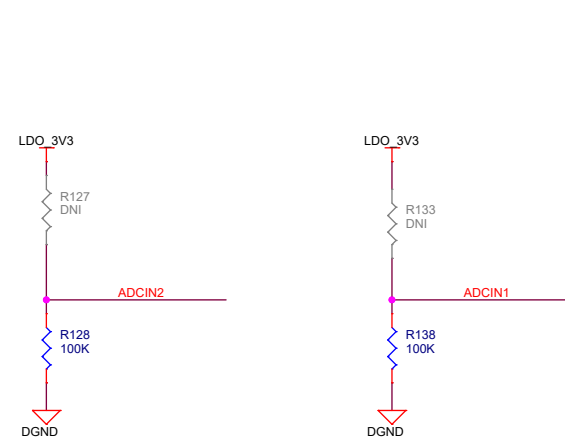
EEPROM & PROGRAMMING HEADER



```

ALWAYS ENABLE SINK
I2C SLAVE ADDRESS 0x20h (#01)

```

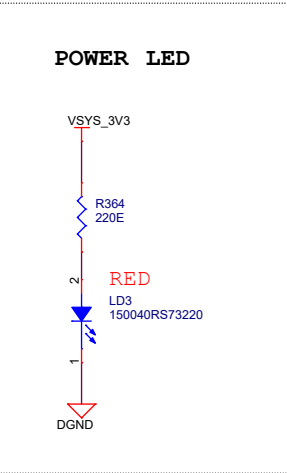
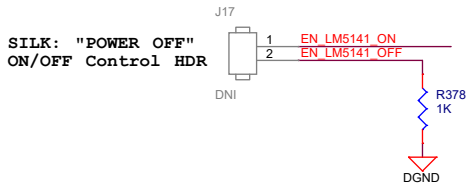
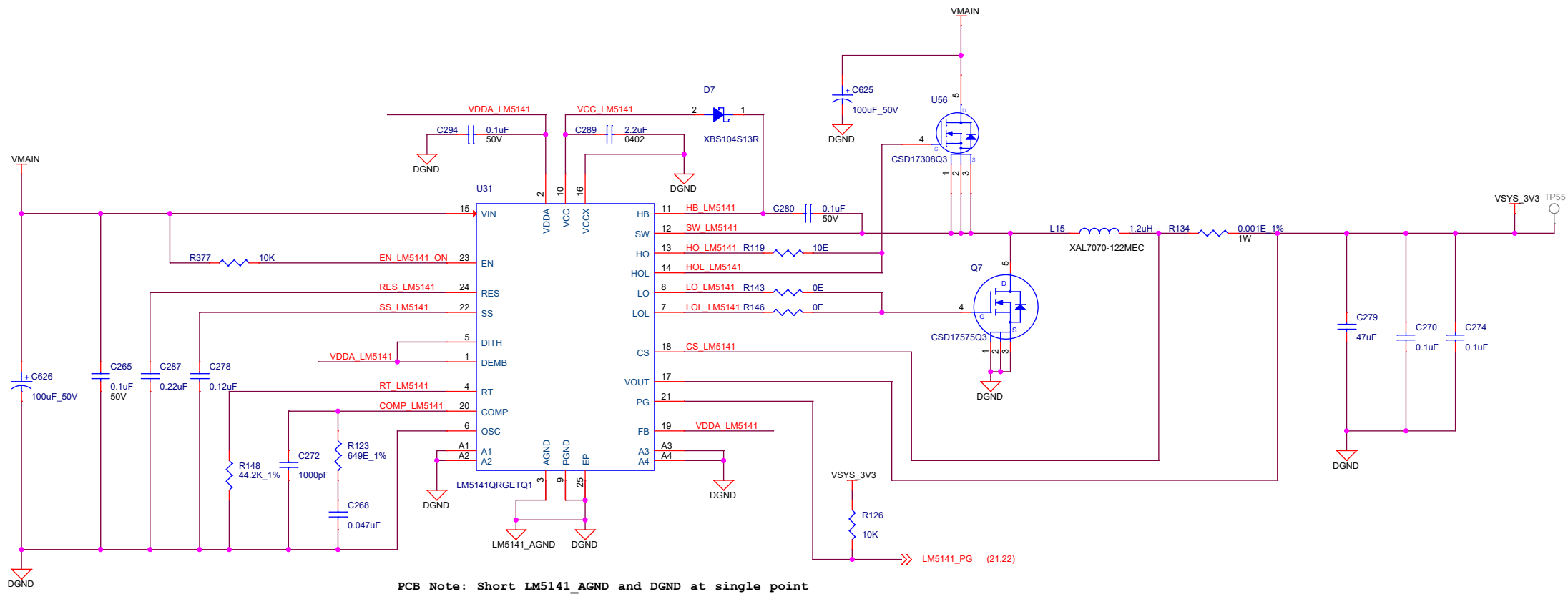
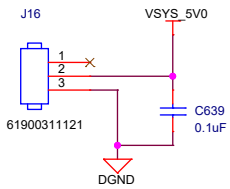


POWER SUPPLY #1

3.3V GENERATION

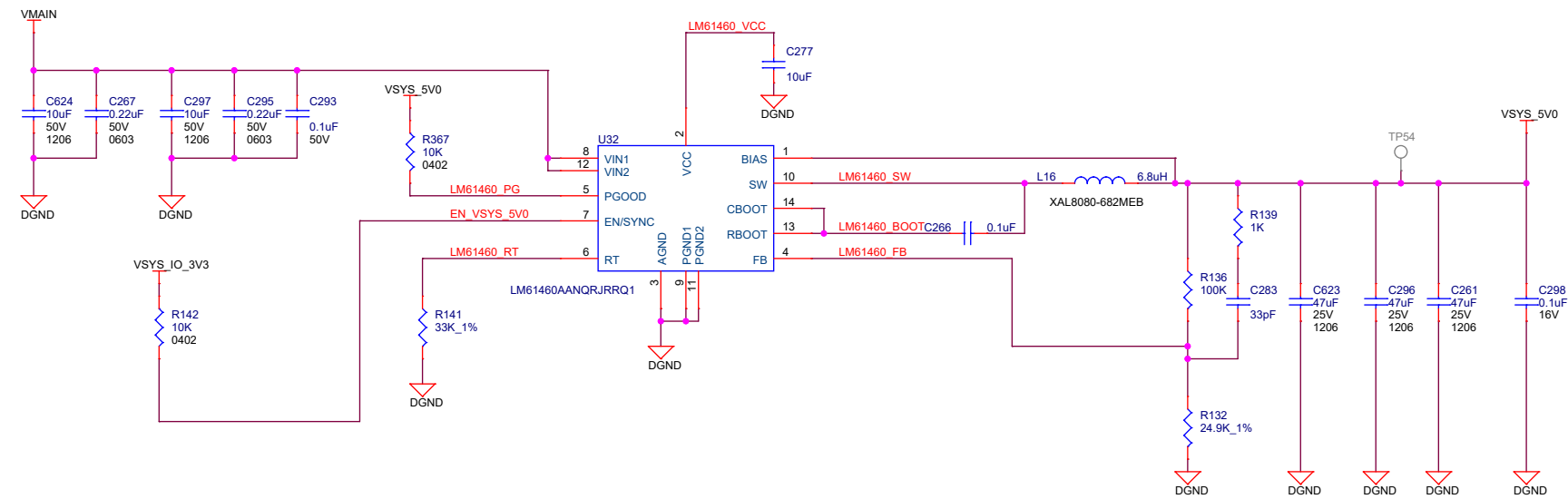
FAN HEADER

TI WEBENCH Simulation Inputs:
Vin (min) = 4.5V Vin (max) = 24V
Vout1 = 3.3V@18.5A
Ta = 25 deg



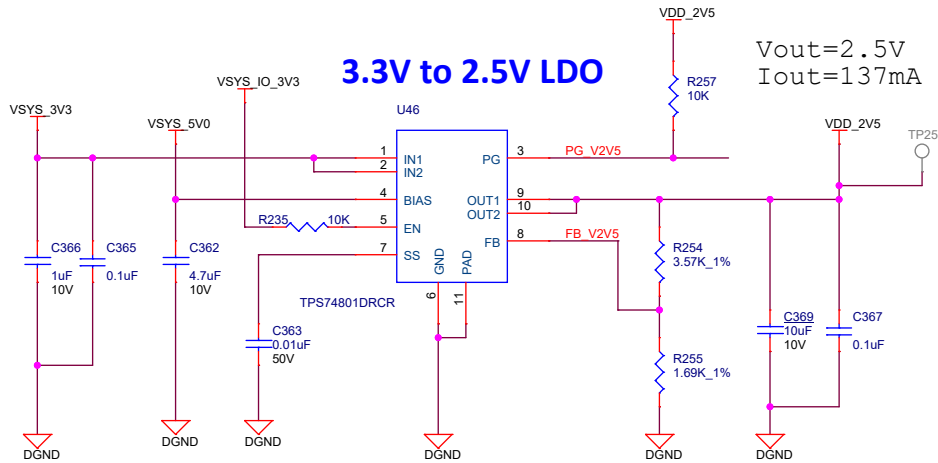
POWER SUPPLY #2

LM61460 5V BUCK REGULATOR
VinMin = 12V
VinMax = 36V
Vout = 5.0V
Iout = 6A

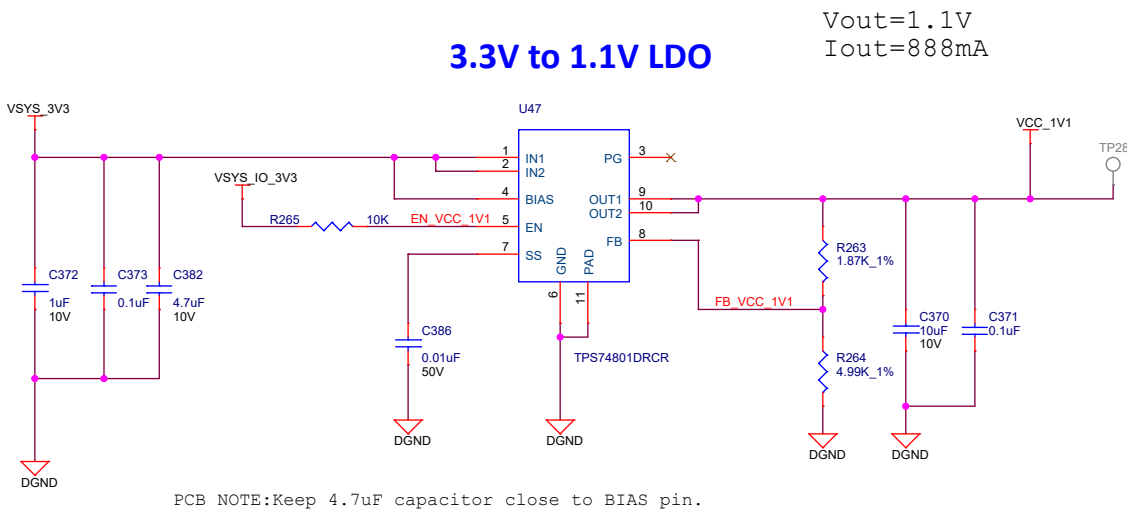


POWER SUPPLY #3

ETHERNET POWER

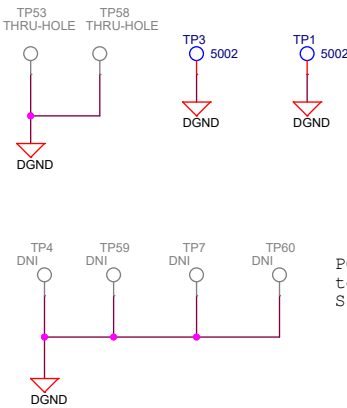


USB HUB & ETHERNET POWER



PCB NOTE:Keep 4.7uF capacitor close to BIAS pin.

GROUND TEST POINTS



PCB NOTE: Spread the SMD test points Top and Bottom Side of PCB

Project : TDA4VM Edge AI Kit		Title POWER SUPPLY #3	
Date: Monday, April 04, 2022		Sheet 43 of 48	Rev A1

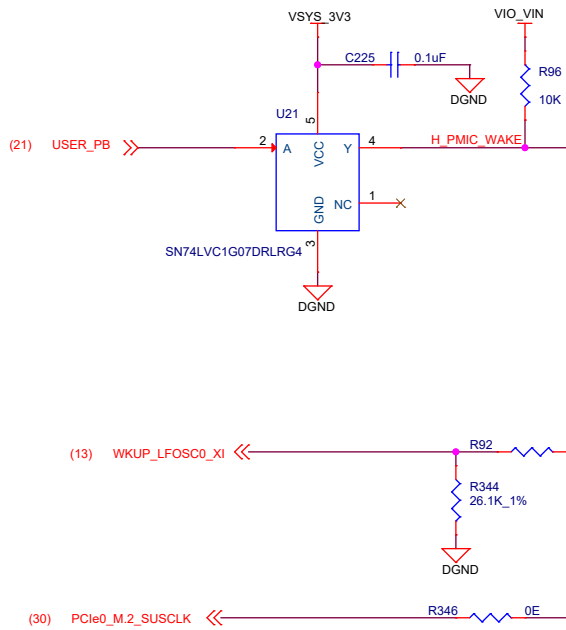
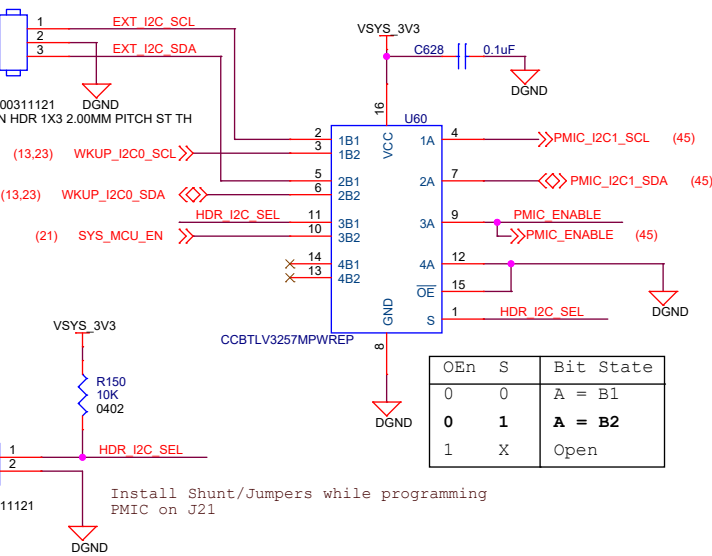
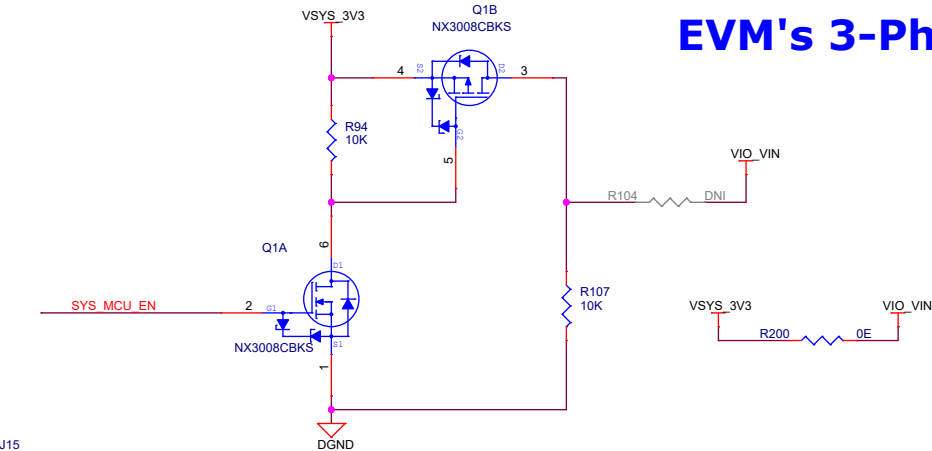
EVM's 3-Phase DUAL PMIC Power Distribution Network (PDN)
(3-Phase Buck supplying VDD_CPU)

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

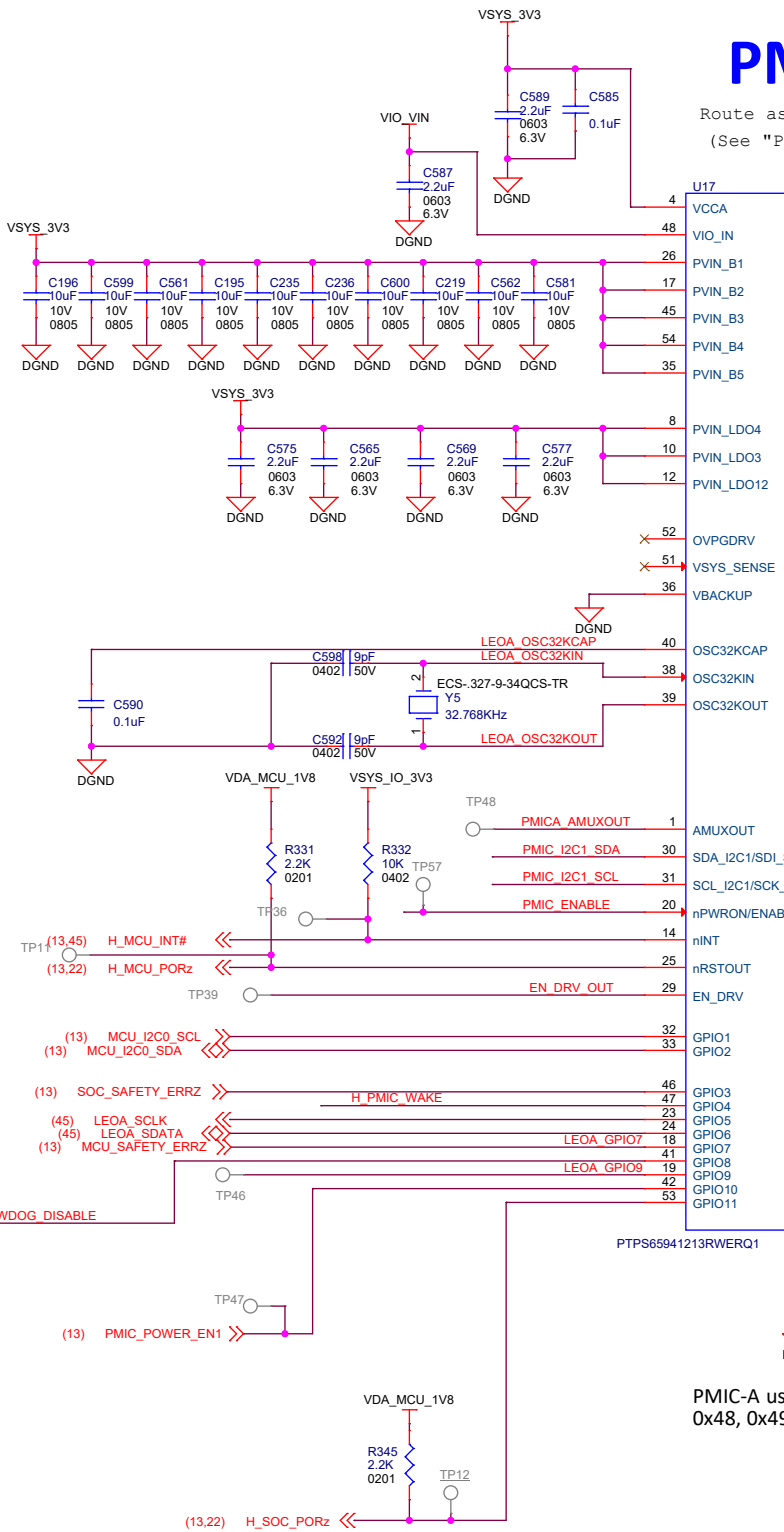
PMIC- A

Route as Pseudo differential pair trace
(See "PCB Notes")



(EVM Bd Setting Default):

LEOA_WDOG_DISABLE	PD (Low)	Enable WDOG
	PU (High)	Disable WDOG



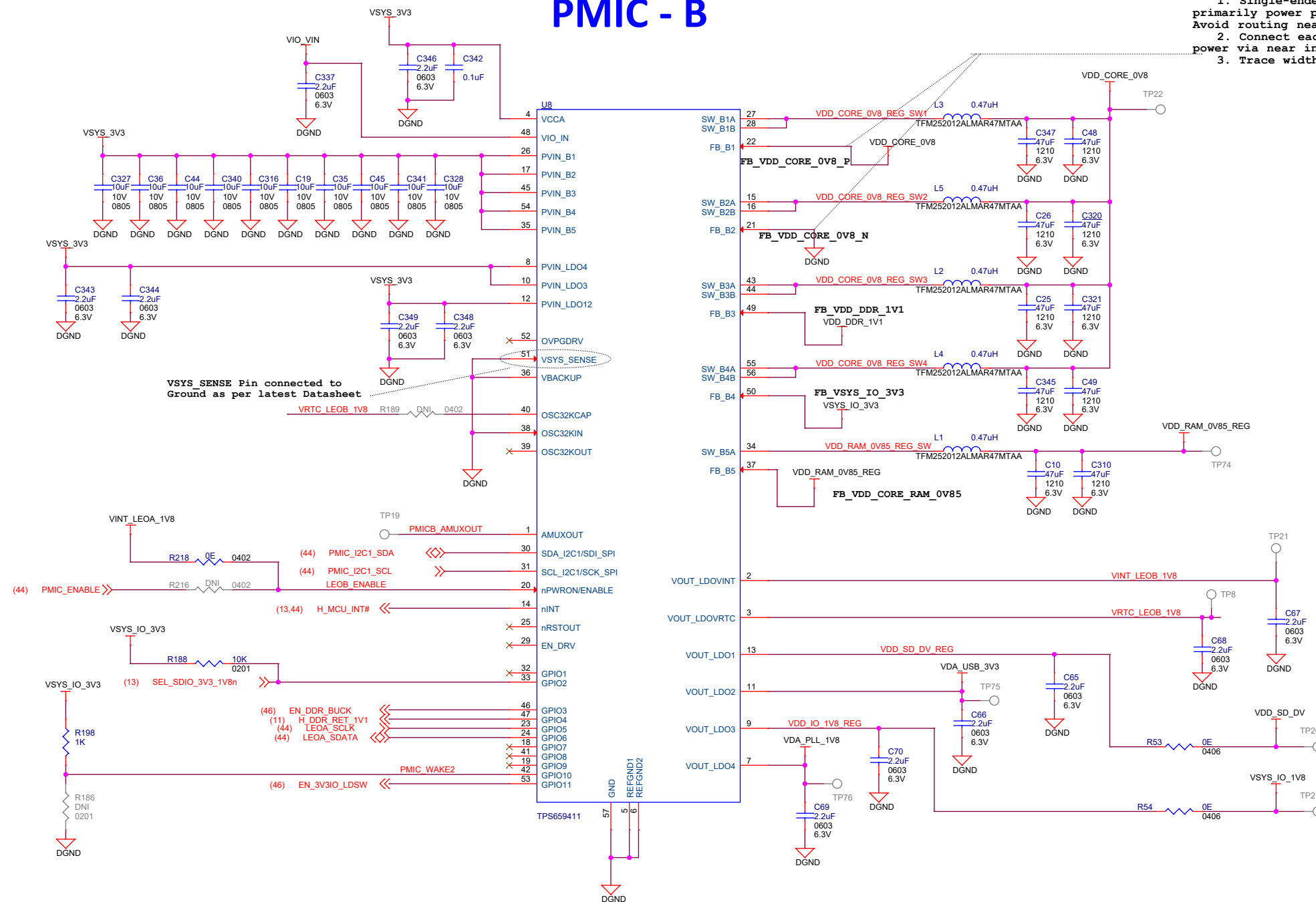
PMIC-A uses default I2C ADDR:
0x48, 0x49, 0x4A & 0x4B

Project :
TDA4VM Edge AI Kit



Title PMIC A		
Size C	PROC112 001 J721EXSKG01EVM	Rev A1
Date:	Monday, April 04, 2022	Sheet 44 of 48

PMIC - B



PMIC-B uses NVM to set I2C ADDR:
0x4C, 0x4D, 0x4E & 0x4F

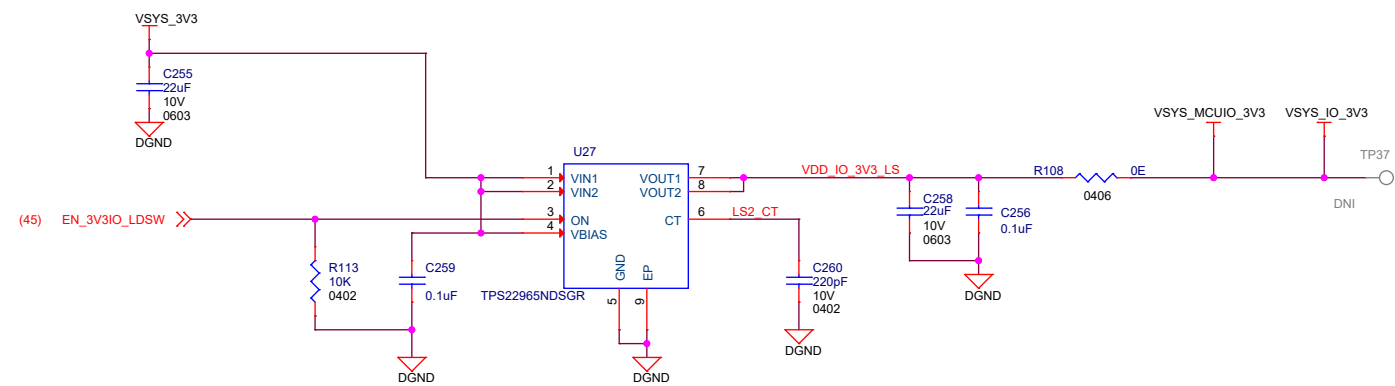
"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:

1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:

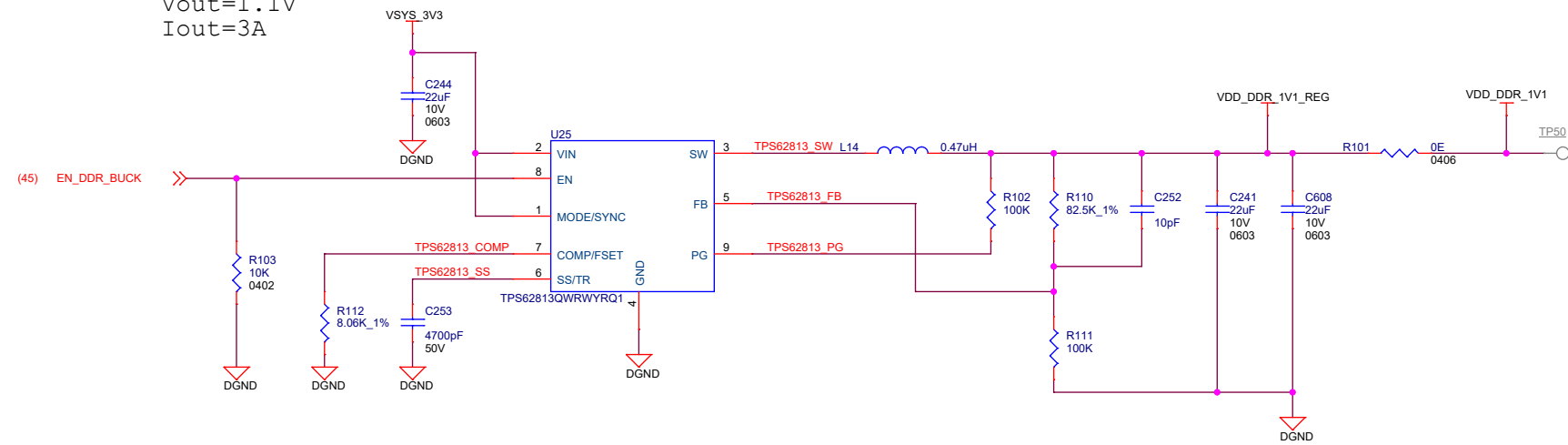
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

3.3V LOAD SWITCH

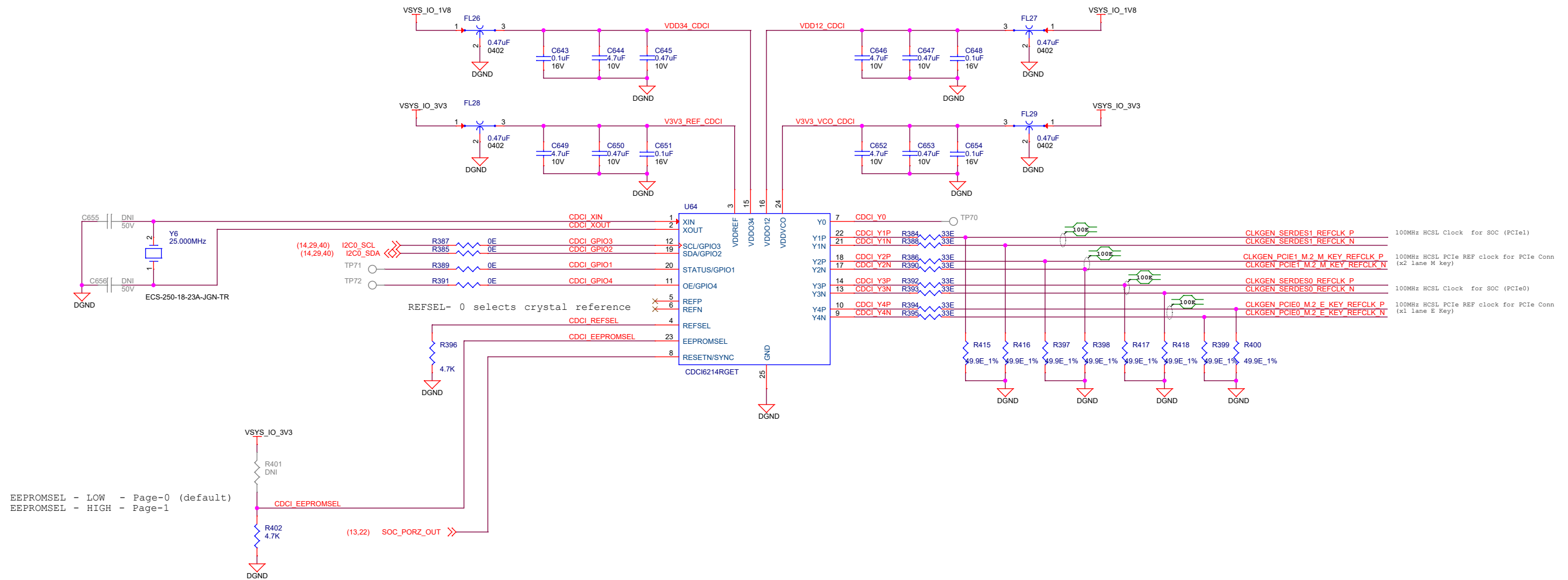


VDD_DDR_1V1 BUCK REG

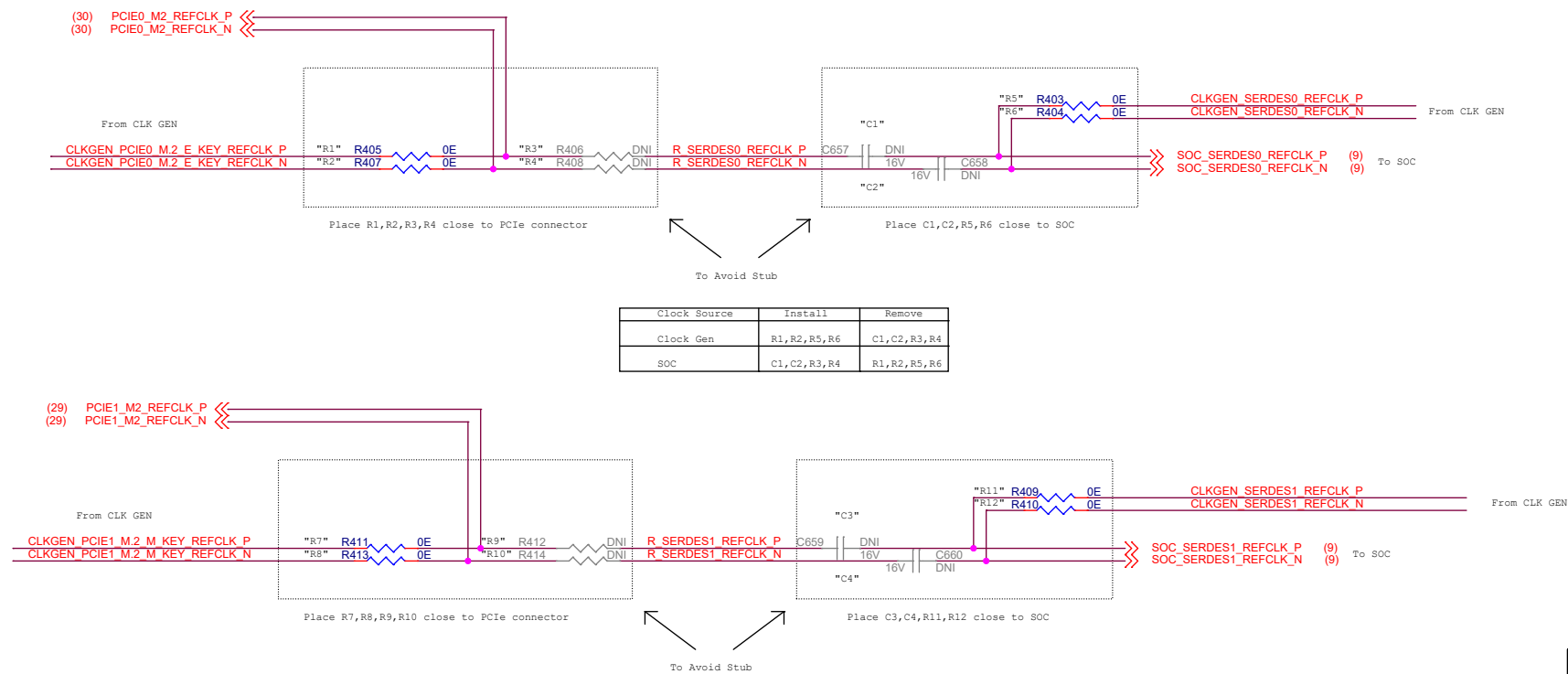
Vout=1.1V
Iout=3A



SERDES CLOCK GENERATOR



CLOCK ROOT SELECTION



Clock Source	Install	Remove
Clock Gen	R1,R2,R5,R6	C1,C2,R3,R4
SOC	C1,C2,R3,R4	R1,R2,R5,R6

Clock Source	Install	Remove
Clock Gen	R7,R8,R11,R12	C3,C4,R9,R10
SOC	C3,C4,R9,R10	R7,R8,R11,R12

Project :
TDA4VM Edge AI Kit



Title		SERDES CLOCK GENERATOR	
Size	PROC112 001 J721EXSKG01EVM	Rev	
C		A1	
Date:	Monday, April 04, 2022	Sheet	47 of 48

NOTES, HW & LABELS

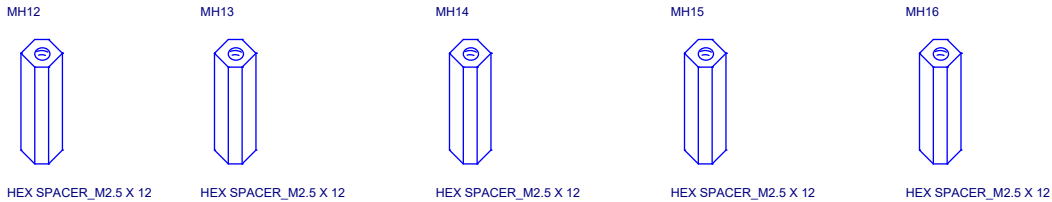
ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

SCREWS



STANDOFFs



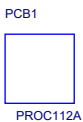
WASHER



FIDUCIALS



BARE PCB



LABELS

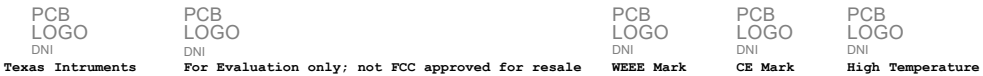
Board Serial No.



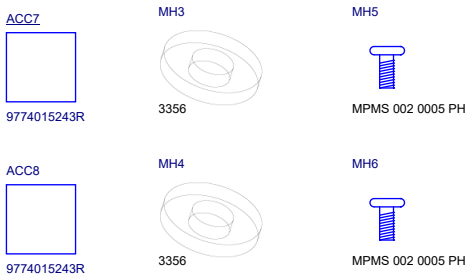
Assembly Revision.



LOGOs



SCREW & WASHER FOR PCIe M.2



HEATSINK AS ACCESSORIES



Project :
TDA4VM Edge AI Kit



Title HARDWARE SCHEMATICS		
Size C	PROC112 001 J721EXSKG01EVM	Rev A1
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